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(54) Abstract Title
Optical data link system

(57) A communication system comprises a data link for transmitting data. A data encoder encodes data to be transmitted over the data link. The data encoder includes a parallel to serial multiplexing encoder for merging one or more digital isochronous data streams, each isochronous data stream having a different data rate, with a plurality of digital asynchronous data streams, each asynchronous data stream having a different data rate to that of the isochronous data streams, to form a single isochronous digital stream. A data decoder decodes data which is received over the data link. The data decoder includes a serial to parallel demultiplexing decoder for separating the digital isochronous data streams and the plurality of digital asynchronous data streams, from the single isochronous digital stream.

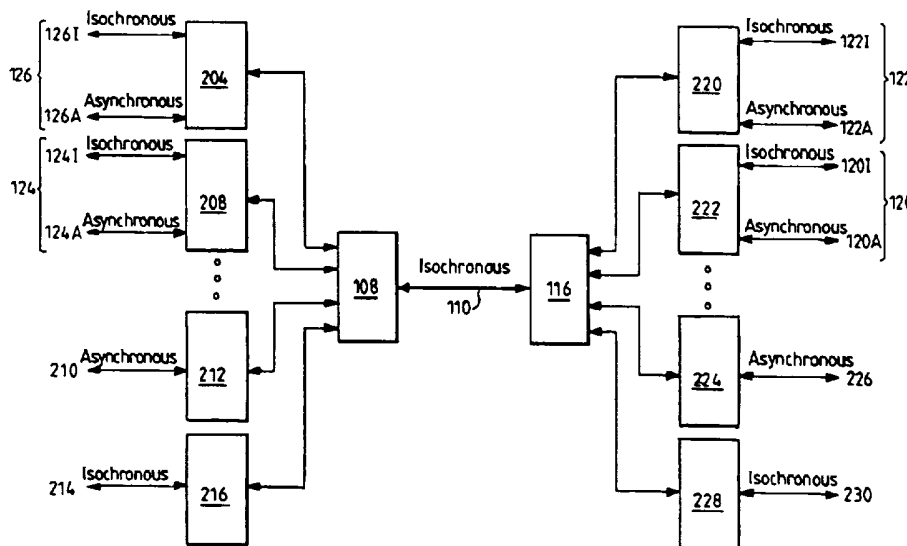


FIG. 2

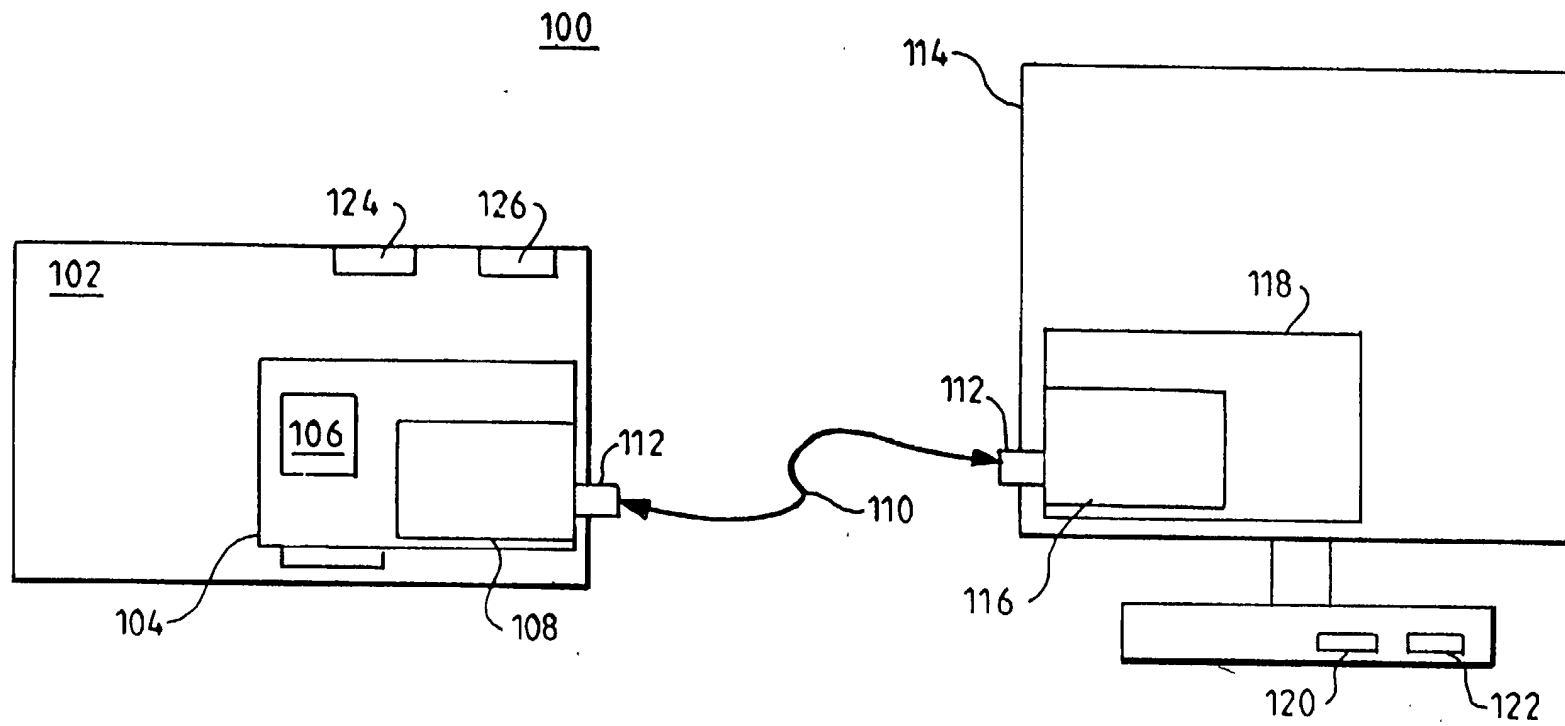


FIG. 1

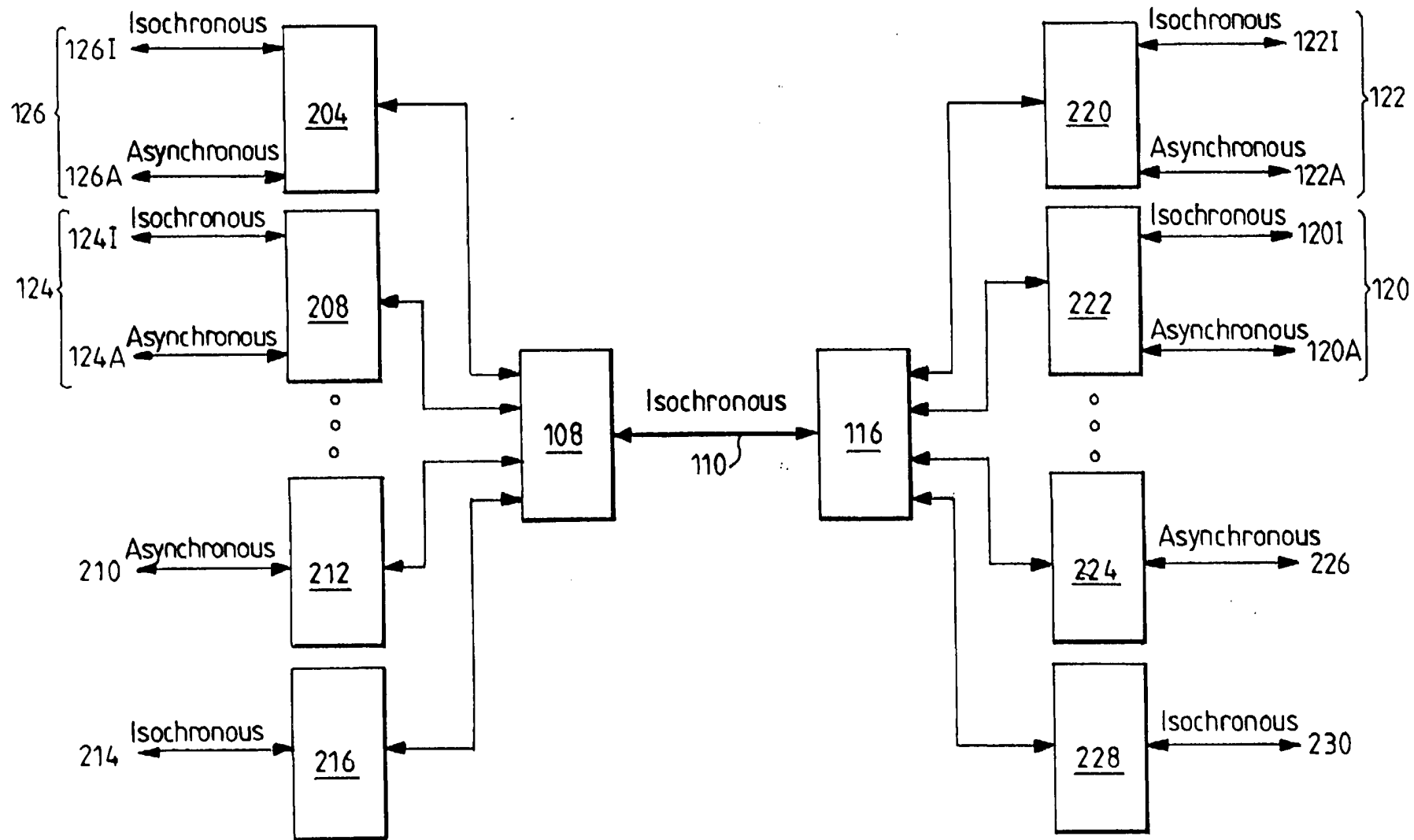
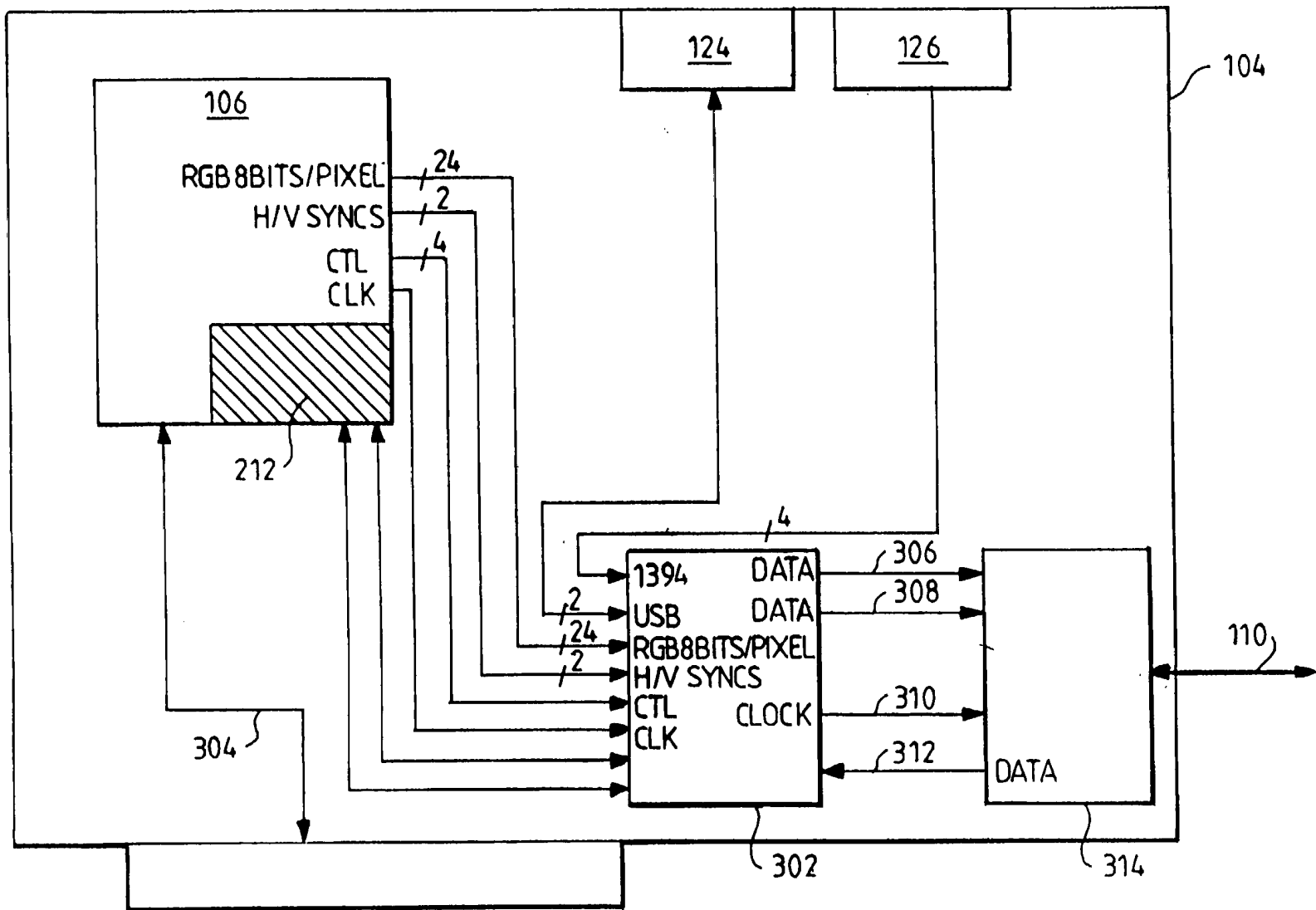


FIG. 2



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FIG. 3

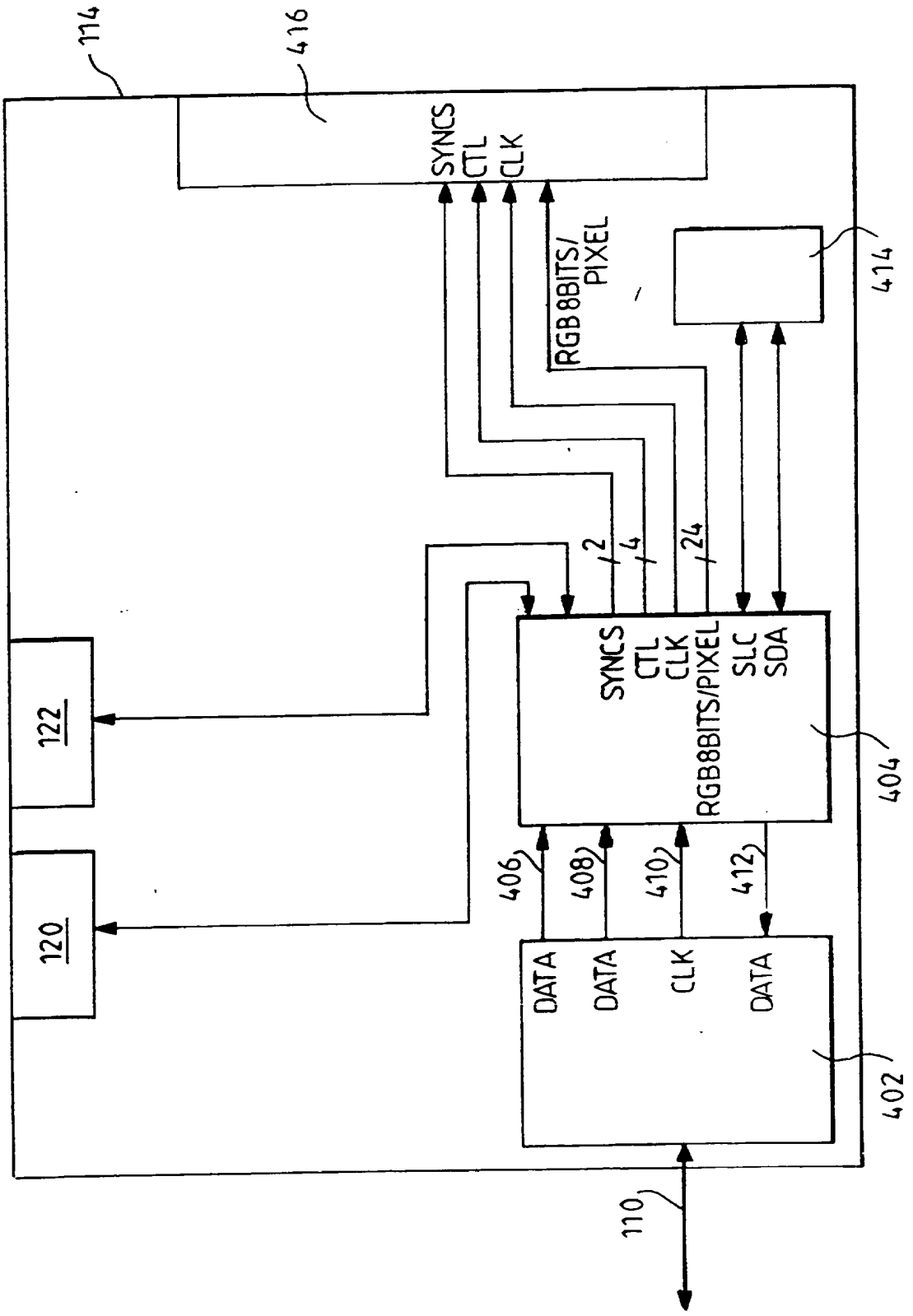


FIG. 4

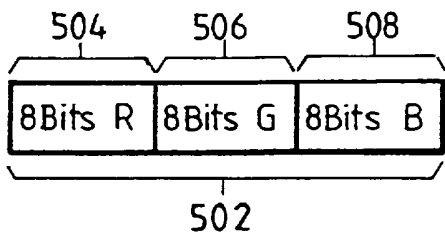


FIG. 5 PRIOR ART

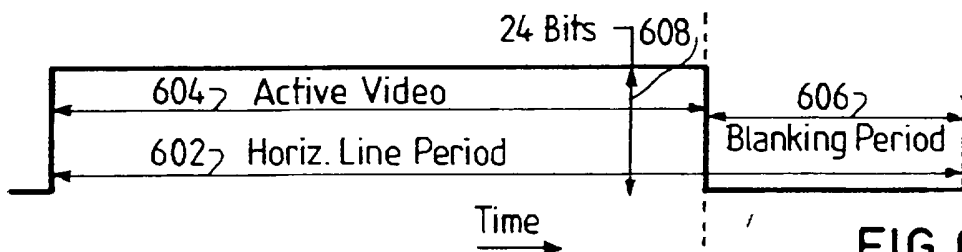


FIG. 6 PRIOR ART

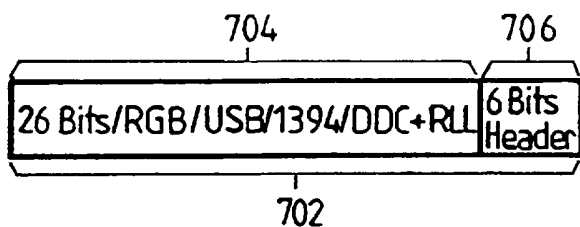


FIG. 7

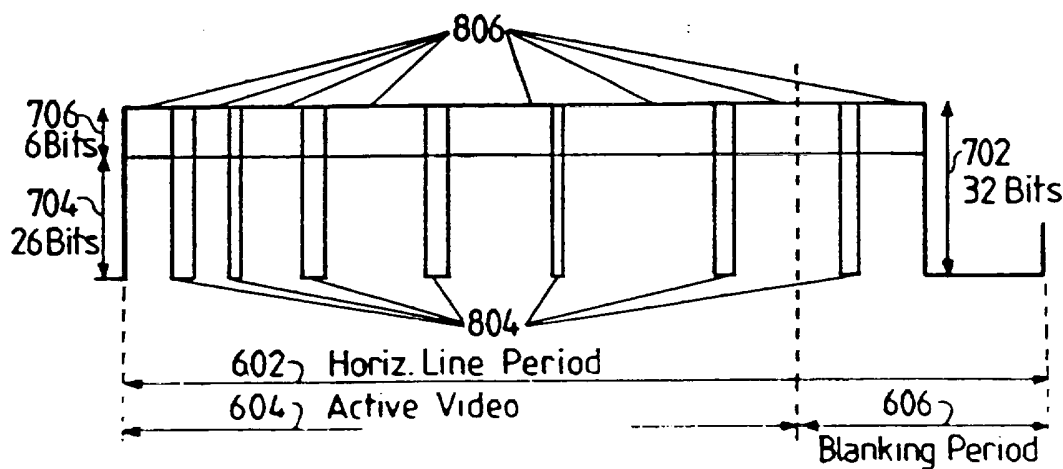


FIG. 8

OPTICAL DATA LINK SYSTEM5 Technical Field

The present invention relates to fibre optic data links and in particular to the merging of multiple separate input data streams into a single data stream for transmission. More particularly, the invention relates to the merging of one or more digital isochronous data streams, each isochronous data stream having a different data rate, with a plurality of digital asynchronous data streams, each asynchronous data stream having a different data rate to that of said isochronous data stream, to form a single isochronous digital stream.

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Background Art

Fibre optic data links are well known and have the advantages of good noise immunity and high bandwidth. The current technology of fibre optic data links is generally designed for telecommunications applications in which communications over distances of tens of kilometres is required with a very low error rate. Such links are asynchronous digital links having multiple input data streams, and include, for example, ISDN. The data structures in the fibre optic link are very different to that used by the equipment between which communication is taking place by means of the fibre optic link.

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Whilst such known fibre optic links work well for telecommunications applications at, for example, 1.0 Gigabits/sec or at 2.4 Gigabits/sec, the cost of the link is high. In telecommunications applications, this cost is shared by the multiple separate pieces of equipment which are using the fibre optic link to communicate.

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The benefits of good noise immunity and high bandwidth mean that the use of fibre optic links for non-telecommunications applications is increasing. Such applications are distinguished from telecommunications applications by virtue of the fact that they rarely exceed 150 metres in length and are frequently as short as 2 metres in length. The cost of a telecommunications type of fibre optic link for such an application is between 10 and 100 times too expensive. The physical size of the equipment for a telecommunications fibre optic data link is too large for

easy incorporation into a personal computer, computer display or an input/output sensor. When used as a data link from a personal computer to a computer display, the video data that is sent from the personal computer to the computer display can be permitted to have transmission errors, but the synchronisation (or control) signals cannot be permitted to have transmission errors, otherwise the displayed image will break up and the errors will be visible to the end user.

US Patent 4,863,233 discloses a system for connecting a personal computer to a computer display using three discrete fibre optic cables for each of the Red, Green and Blue video data. Vertical and Horizontal sync signals are added to, for example, the Red and Blue video fibre optic cables. This system is a digital isochronous link having a single input stream.

US Patent 5,132,828 discloses a system for connecting a personal computer to a computer display using a fibre optic cable for each channel of video, the video signals being analog signals. The gain of a video amplifier is compensated to adjust for variations in the gain of the fibre optic link. US Patent 5,132,827 describes a similar system. These systems are analogue video systems.

The information transmitted over a data link can be split into two types of information, asynchronous data and isochronous data. The transmission of isochronous data requires predictable, periodic access to the data link. The transmission of asynchronous data does not require such predictable, periodic access.

European Patent 0 174 099 A describes a system for connecting a computer to a computer display using a fibre optic cable. The fibre optic link is bidirectional carrying unidirectional isochronous video data from the computer to the computer display and asynchronous keyboard control and sound synthesis data from the computer to the computer display and asynchronous keyboard input data, mouse input data and speech input data from the computer display to the computer. The clock frequency for the control data is at the same rate as that for the video data and the control data is in the same format as the video data. The control data is time domain multiplexed with the video data. This system is a digital isochronous link having a single input stream, together with a bidirectional asynchronous link having a multiple input streams.

US Patent 5,450,411 discloses a system in which non-isochronous data streams are merged together with isochronous data streams to form an asynchronous ATM data stream for transmission over an ATM link.

5 US Patent 5,396,494 discloses a system in which an asynchronous packet transmit bus is provided such that isochronous information packets may be transmitted from a source to a destination with a fixed, constant delay. Arbitration is used between the various transmission sources.

10 US Patent 5,640,392 discloses a system in which isochronous data is received continuously without interruption and irregular asynchronous data is also received. A single isochronous data stream and a single asynchronous data stream is used. FIFOs are used for storing the isochronous and asynchronous data.

15 US Patent 5,392,280 discloses a system in which both synchronous transmission and asynchronous transmission are used in an alternating pattern. This is achieved by cell level dynamic slot allocation.

20 US Patent 5,173,901 discloses a system in which synchronous and asynchronous data streams are transmitted over a single transmission link. The time frames of the input and output cell streams are phase synchronous.

25 US Patent 5,603,058 discloses a video optimised media streamer having communications nodes receiving digital data from a storage node and transmitting the data to adapters for generating isochronous digital data streams:

30 It would be advantageous if a combined high speed unidirectional isochronous data link together with an interleaved medium speed bidirectional isochronous data link could be provided.

Disclosure of the Invention

35 Accordingly the invention provides a communication system comprising: a data link for transmitting data; a data encoder for encoding data to be transmitted on said data link including a parallel to serial multiplexing encoder for merging one or more digital isochronous data streams, each isochronous data stream having a different data rate,
40 with a plurality of digital asynchronous data streams, each asynchronous

data stream having a different data rate to that of said one or more isochronous data streams, to form a single isochronous digital stream; and a data decoder for decoding data received on said data link including a serial to parallel demultiplexing decoder for separating said one or more digital isochronous data streams and said plurality of digital asynchronous data streams, from said single isochronous digital stream.

Brief Description of the Drawings

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a system incorporating the present invention

Figure 2 is a schematic diagram of a system according to the present invention;

Figure 3 is a block diagram of an adapter card used in the system of figure 1; and

Figure 4 is a block diagram of a decoder used in the system of figure 1;

Figure 5 shows the content of a prior art video data stream;

Figure 6 shows the data that is sent for each horizontal line period of the prior art video data stream of figure 5;

Figure 7 shows the content of a first embodiment of the video data stream of the present invention using a 32 bit data width; and

Figure 8 shows the data that is sent for each horizontal line period of the video data stream of figure 7 in which the channel bandwidth is allocated asynchronously on an "as required basis".

Detailed Description of the Invention

The present invention will be described by way of its application to a communications link between a digital adapter in a personal computer and a digital display device. Figure 1 shows such a system 100. The

personal computer 102 includes an adapter card 104 which is connected to an interface bus in the personal computer, such as, for example, a PCI bus. The type of interface bus between the adapter card and the personal computer is not relevant to the operation of the invention.

5 Additionally, the circuitry which will be described with reference to the adapter card may equally well be located on the same circuit card as the processing circuits of the personal computer without affecting the operation of the invention. The adapter card contains a graphics chip set 106 which provides video information for an attached display 114.
10 The adapter card also contains a data encoder 108 for translating the information from the graphics chip set to a format suitable for optical transmission.

The optical data is then transmitted over a bi-directional optical
15 fibre 110 which typically has a length of 2 to 150 metres. The fibre 110 is connected to the personal computer 102 and to the display 114 by means of optical connectors 112, which may be any industry standard optical connector.

20 When the optical data is received in the display 114, it is first decoded by a data decoder 116 to decode the optical data into electrical data. The data then passes to a display driver card where it is converted to a format suitable for driving the display. Typically the display is a flat panel display, although the invention is also
25 applicable to displays other than flat panel displays.

The display also has connections for other input and output data streams such as a USB bus connector 120 and an IEEE 1394 serial bus
30 connector 122. Further details of the USB can be found in "Universal Serial Bus Specification, Version 1.0" and further details of the IEEE 1394 bus can be found in "IEEE Standard 1394-1995 for a High Performance Serial Bus" (ISBN 1-55937-583-3).

The data transmitted to the computer display consists of video data
35 which is either used to update a shadow refresh buffer in the computer display or is used to refresh the CRT directly without a shadow refresh buffer. Table 1 shows the data rate requirements for a computer display having a shadow buffer in the display and Table 2 shows the data rate requirements for a computer display not having a shadow buffer in the
40 display. The present invention is not limited to use only for the formats shown in tables 1 and 2.

Format	Resolution	Frame Rate	Pixel Clock	Data Rate (Post Palette) (Megabits/sec)	
				12bpp	24bpp
VGA	640x480	60	25	300	600
	720x400	70	28	336	672
SVGA	800x600	60	40	480	960
XGA	1024x768	30	23.59	283.08	566.16
SXGA	1280x1024	30	40	480	960
VXGA	2048x2048	30	120	1444	2888
HDTV	1280x720	30	27.64	331.68	663.36
	1920x1080	30	62.20	746.4	1492.8

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Table 1 Update rates for computer displays having shadow buffer in the display

Format	Resolution	Frame Rate	Pixel Clock	Data Rate (Post Palette) (Megabits/sec)	
				12bpp	24bpp
VGA	640x480	60	25	300	600
	720x400	70	28	336	672
SVGA	800x600	60	40	480	960
XGA	1024x768	60	65	780	1560
SXGA	1280x1024	60	112	1344	2688
UXGA	1600x1200	75	250	3000	6000
GXGA	2560x2048	75	384	4600	9200
HDTV	1280x720	60	77.5	930	1860
	1920x1080	30(I)	77.2	926.4	1852.8

Table 2 Refresh rates for computer displays not having a shadow buffer in the display

Additionally, control data for the display is transferred to and from the display using the DDC format. Further information on the VESA Data Display Channel (DDC) can be found in "VESA Display Data Channel (DDC) Standard, Version 3".

Figure 2 shows a schematic diagram of a system according to the present invention. Isochronous IEEE 1394 data is received and transmitted (125I) from IEEE 1394 driver circuits 204. Asynchronous IEEE 1394 data is received and transmitted (126A) from IEEE 1394 driver circuits 204. The isochronous and asynchronous data flows from connection 126 through encoder 108, optical link 110 and decoder 116 as isochronous data to IEEE 1394 driver circuit 220, where it is split into isochronous data 122I and asynchronous data 122A. Isochronous and asynchronous USB data 124I, 124A from connection 124 is transferred in a similar fashion to connections 120A and 120I.

Asynchronous data 210 is received and transmitted from DDC driver circuits 212. The asynchronous data flows through encoder 108, optical

link 110 and decoder 116 to DDC driver circuit 224, where it is transferred to connector 226.

5 Isochronous video data 214 from video driver circuits 216 flows through encoder 108, optical link 110 and decoder 116 to video driver circuit 228, where it is transferred to connector 230. In contrast to the IEEE 1394, USB and DDC data, which are all bidirectional, the video data is unidirectional data only. There may be any number of IEEE 1394, USB or DDC channels, further channels being shown in figure 2 by the 10 three dots between USB driver 208 and DDC driver 212 and by the three dots between USB driver 222 and DDC driver 224.

Figure 3 shows a block diagram of an adapter card 104 used in the system of figure 1. The adapter card 104 has connections 124 for USB 15 data and 126 for IEEE 1394 data. The graphics chip set 106 produces RGB video data, video control data, display synchronisation signals and a clock signal for use by parallel-serial multiplex encoder 302. These video signals are unidirectional isochronous signals and may be typically 12 bit, 18 bit, 24 bit or 32 bit in format. The invention is equally 20 applicable to other numbers of bits, including numbers greater than 32 bits. For the purposes of description, the present embodiment uses 24 bits. Parallel-serial multiplex encoder 302 converts the 24 bit signals to 26 bit signals and run-length limits (RLL) them. 18 bit format signals received by the parallel-serial multiplex encoder are converted 25 to 24 bit signals by setting the additional 6 bits to zero. The video control signals are encoded to provide error detection and correction in parallel-serial multiplex encoder 302. The video control signals include Data Good, H and V sync, start of frame, EDID good, no data, cal max and cal min.

30 Additionally, SDA and SCL data are produced from DDC driver 212 located within the graphics chip set and are received by parallel-serial multiplex encoder 302. The DDC signals are bidirectional, asynchronous signals. Graphics chip set 106 has a connection 304 to the personal 35 computer bus. In the preferred embodiment, the personal computer bus is a PCI bus. In an alternative embodiment, the personal computer bus is an AGP bus. Parallel-serial multiplex encoder 302 also transfers data to and from USB connector 124 and IEEE 1394 connector 126. This USB and 40 IEEE 1394 data can be isochronous or asynchronous data or both and is bidirectional data.

The RLL data codes for digital video data, USB data, IEEE 1394 data, DDC data and control hamming code data are merged clock, embed serialised and then DC balanced as is well known in the art. The merged data is now contained within a n bit word. In the preferred embodiment, the value is 32 bits, 24 bits of video data, 5 bits of IEEE 1394 data, 1 bit of USB data and 2 header bits. It is converted from n bit parallel to serial 2 bits wide by multiplexing with pipeline registers to retime the data. The real time bandwidth within the serial data and within the total refresh time slot is allocated isochronously to meet the bus specifications of USB, IEEE 1394 and the data refresh rate requirements.

Parallel-serial multiplex encoder 302 produces 2 bit wide outgoing data signals 306, 308 and an outgoing clock signal 310 for electro-optical converter 314. The n bit encoded word (2 bits wide) is converted to 4 unique light levels at a laser diode, is merged with the return path optical data and is transmitted to fibre optic cable to the display.

Data is received by parallel-serial multiplex encoder 302 from electro-optical converter 314 over connection 312. The return path optical data is converted to binary electrical signals via a pin diode and the clock is recovered in the electro-optical converter 314. The return path data is transferred to parallel-serial multiplex encoder 302 one bit wide where it is decoded into IEEE 1394 data, USB data and DDC data. It is converted from serial to parallel with pipeline registers to retime the data. The IEEE 1394 data, USB data and DDC data are RLL decoded and then separated to their respective original formats. The IEEE 1394 data, USB data and DDC data are converted to their respective specification electrical levels and protocols before being transferred to connectors 126, 124 and the DDC circuitry 212 of graphics chip set 106.

Connections 306, 308, 310 and 312 are preferably implemented using co-axial cable or similar. In an alternative embodiment, electro-optical converter 314 is located in the same integrated circuit as parallel-serial multiplex encoder 302 and so there are no cable connections as such, the connection being contained within the integrated circuit. Electro-optical converter 314 supplies and receives optical data to bi-directional optical fibre 110.

Figure 4 shows a block diagram of a decoder used in the system of figure 1. Data is received by the optic-fibre receiver circuit 402 from

the optical link 110. The receiver circuit 402 converts the data from the optical link 110 from the 4 unique optical light levels to 2 bit wide electrical data signals 406, 408 and a clock signal 410 for the serial-parallel multiplexer 404. The serial-parallel multiplexer 404 converts the n bit data word supplied to it as 2 bit wide electrical data to parallel data with the use of a demultiplexer with pipeline registers to re-time the data without the use of FIFOs. The Synchronisation codes are decoded and error detected and corrected if required. From this decoded data the IEEE 1394 data, USB data, DDC data and Refresh Data Sections of the n-bit data word are separated and RLL decoded back to the original format of the data. The video refresh data with Synchronisation controls is routed to the display connector 408. The USB data is level and protocol converted and is then routed to the USB connector 120. The IEEE 1394 data is level and protocol converted and is then routed to the IEEE 1394 connector 122.

The adapter card 408 has connections 120 for USB data and 122 for IEEE 1394 data. The return path USB data, IEEE 1394 data and DDC data are RLL converted in serial-parallel multiplexer 404 to binary code, transferred over connection 412 and converted to single level optical data in receiver circuit 402. The return path single level optical data is then merged with the incoming four level optical data. Alternatively, separate fibres may be used for the forward path and for the return path.

In another embodiment of the present invention, a sensor is connected to the personal computer 102. This embodiment is represented by figure 1 but where a sensor replaces the computer display 114. The USB connection 120 and the IEEE 1394 connection 122 remain unchanged. The direction of the unidirectional isochronous data is from the sensor to the personal computer 102, rather than from the personal computer to the computer display 114. DDC data may still be sent from the sensor to the personal computer 102.

ENCODING METHODS

Figures 5 and 6 show a prior art data stream. Although a 24 bit data word is shown, other prior art systems use 18 bits or 12 bits per pixel formats. These 18 bit and 12 bit prior art data streams can also be used with the encoding format of the present invention as well as the 24 bit embodiment described.

Figure 5 shows, at 502, a 24 bit data word, 8 bits of data 504 represented Red video, 8 bits of data 506 representing Green video and 8 bits of data 508 representing Blue video.

5 In the timeline of figure 6, the horizontal line period is represented by line 602 and is the time between consecutive line scans. The active video time is represented by line 604 and the blanking period, during which video is not displayed on the screen is represented by line 606. Line 608 represents that for each displayed pixel, (that is, for
10 each pixel clock period) 24 bits of data are sent.

For each of the embodiments of the present invention now described, the data width is increased from the 24 bit width for the raw data to a greater width so as to include items such as bus data (IEEE1394, USB,
15 DDC), headers, run length limiting, error correction, calibration data and flags.

Figures 7 and 8 show a first embodiment of the data stream format of the present invention which uses a 32 bit data width and the channel
20 bandwidth is allocated asynchronously between video, USB, IEEE1394 and DDC data on an "as required basis", each data type being indicated by the appropriate header. The video pixel clock remains unaltered causing the video and bus information to spill into blanking period. The video information requires buffering to allow it to be retimed.

25 Figure 7 shows, at 702, a 32 bit data width, 26 bits 704 representing Red, Green and Blue video data or USB data or IEEE 1394 data or DDC data as well as RLL data and 6 bits 706 representing header and error correction data. The header identifies which of the various types
30 of data are contained within the 26 bits 704.

In the timeline of figure 8, the horizontal line period is represented by line 602 and is the time between consecutive line scans. The line 702 represents that for each displayed pixel, (that is, for each
35 pixel clock period) 32 bits of data are sent, although the data being sent at a given time does not always relate to the particular pixel being displayed at that given time. The 32 bits shown at 702 in figure 8 represent the 26 bits of data 704 and the 6 bits of data 706 from figure 7. The data shown at 806 represents video information containing Red,
40 Green and Blue video data. The data shown at 804 represents the other data, including USB data, IEEE 1394 data, DDC data as well as RLL data.

Time slots are allocated for such data asynchronously, on an "as required basis", with the 6 bit header indicating the type of the data.

5 The embodiment of figures 7 and 8 has the advantages that the increase in channel data rate is minimised and there is a much reduced latency for data channels. The embodiment of figure 7 and 8 requires a coding arrangement as well as video buffering.

CLAIMS

1. A communication system comprising:

a data link for transmitting data;

a data encoder for encoding data to be transmitted on said data link including a parallel to serial multiplexing encoder for merging one or more digital isochronous data streams, each isochronous data stream having a different data rate, with a plurality of digital asynchronous data streams, each asynchronous data stream having a different data rate to that of said one or more isochronous data streams, to form a single isochronous digital stream; and

a data decoder for decoding data received on said data link including a serial to parallel demultiplexing decoder for separating said one or more digital isochronous data streams and said plurality of digital asynchronous data streams, from said single isochronous digital stream.

2. A system as claimed in claim 1, wherein the format of at least one of the one or more isochronous data streams is isochronous IEEE-1394, isochronous USB, isochronous ZV-Port, RS-442, refresh digital data to a display transducer, update digital data to a display transducer, refresh digital data from a sensor to a system processor transducer or update digital data from a sensor to a system processor transducer.

3. A system as claimed in claim 2, wherein the refresh digital data or the update digital data is in a VESA Plug and Display format, CI 601 format, MPEG2 format or DVD format.

4. A system as claimed in claim 2, wherein the display transducer is a head mounted display or a helmet mounted display.

5. A system as claimed in claim 4, wherein the head mounted display or helmet mounted display has two display transducers, both being addressed by the isochronous data stream.

6. A system as claimed in claim 4, wherein the head mounted display or helmet mounted display further comprises one or more head mounted

cameras, the data being transmitted from the one or more cameras to a processor unit via the asynchronous data stream.

5 7. A system as claimed in claim 4, wherein the head mounted display or helmet mounted display further comprises a head tracking system having multiple light emitting diodes, the light emitting diodes being controlled via the asynchronous data stream.

10 8. A system as claimed in claim 1, wherein the format of at least one of the asynchronous data digital streams is asynchronous USB, asynchronous IEEE-1394, RS-232, ATM, DDC or I²C.

15 9. A system as claimed in claim 2, wherein the output stream format is DDC and the return digital data stream format is DDC.

10. A system as claimed in claim 1, wherein the sensor is a CCD Array.

20 11. A system as claimed in claim 10, wherein the sensor is an image generating sensor, said image generating sensor being a scanning linear array, staring array or a two-dimensional scanning detector.

25 12. A system as claimed in claim 1, wherein the sensor is a multiple sensor package mounted on a rotating mast or periscope and the fibre optic link is connected via a optical slip ring.

13. A system as claimed in claim 1, wherein the connection is a fibre optic link.

30 14. A system as claimed in claim 1, wherein the connection is an electrical wire link.



Application No: GB 9815138.4
Claims searched: 1 to 14

Examiner: Ken Long
Date of search: 15 January 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:
UK Cl (Ed.Q): H4M (MTCX & MTCA)
Int Cl (Ed.6): H04L (25/49 & 12/64)
H04J (3/22)
Other: ONLINE : WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	GB 2157921 A MOTOROLA (page 1 lines 31-36 & 55-63 and page 2 lines 16-18)	1
X	EP 0596652 A1 NATIONAL SEMICONDUCTOR (page 2 lines 6-15 & 54-57, page 3 lines 12-22 & 39-50 and page 5 lines 26-32)	1
X	EP 0596649 A1 NATIONAL SEMICONDUCTOR (page 4 line 36 to page 5 lines 23)	1 and 5
X	US 5654969 TELIA (column 3 lines 27-37 and claim 21)	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.