Design and implementation of an electro-optical backplane with pluggable in-plane connectors

Speaker:

Richard Pitwon Xyratex Technology Ltd

xyratex•

SPIE Photonics West - OPTO Paper: Opto 7607-18

San Francisco Tuesday 26th January 2010 R. Pitwon, K. Hopkins K. Wang, D. R. Selviah, H. Baghsiahi, B. Offrein, R. Dangel, F. Horst, M. Halter, Max Gmür Xyratex Technology Ltd University College London IBM Zürich Vario-optics AG

Opto: 7607-18



Design challenges in data storage systems

Electro-optical backplane with polymer waveguides

Active in-plane optical backplane connector

Demonstration platform











Design challenges in modern data storage systems



Data storage protocol and form factor trends

Disk drive form factors decreasing



Data storage interconnect speeds increasing



 2003
 2004
 2005
 2006
 2007
 2008
 2009
 2010
 2011
 2012
 2013
 2014
 2015

 Source: SCSI Trade Association Sep 08
 www.scsita.org

 SPIE Photonics West 2010
 Opto: 7607-18

Data storage array backplane topology



Redundant dual star architecture

□ Controller modules

Midplane interconnect



Design and performance constraints



Design and performance constraints



Design and performance constraints

- □ Copper layers for power distribution
- □ Copper layers for low speed communication
- □ Optical layers for high speed communication



Electro-optical backplane with polymer waveguides





Source: Exxelis





SPIE Photonics West 2010

Polymer optical waveguide layer



Optical interconnect design



Electro-optical PCB fabrication process

- 1. Deposit lower refractive index polymer (cladding) onto substrate surface
- 2. Cure polymer layer with exposure to ultra-violet light to harden
- 3. Deposit higher refractive index (core) polymer onto lower cladding layer
- 4. Align UV laser write head into position
- 5. Activate laser and move write head to pattern waveguide features in core layer
- 6. Remove uncured portions of the corr layer
- 7. Deposit lower refractive index polyrer onto patterned core layer
- 8. Cure upper cladding layer with UV light



UV Exposure

Electro-optical midplane



Passive alignment and assembly

Mechanical registration features





- Deposit lower cladding layer
- Deposit core layer
- Pattern core layer including registration waveguides
- Deposit upper cladding layer
- □ Remove part of upper cladding for mechanical access
- □ Align MT compliant receptacle with microlens array



Optical connector receptacles



Waveguide insertion loss measurements

- Measured loss without index matching fluid
- Measured loss with index matching fluid
- Calculated loss









Active optical backplane connector









Optical backplane connection architecture



Optical backplane connection architecture

Butt coupled connection without 90° deflection





Single waveguide illuminated



Parallel optical transceiver

- Mechanically flexible optical platform
- □ MT compatible optical interface
- Geometric microlens array
- □ Quad VCSEL driver and TIA/LA
- □ VCSEL / PIN arrays on pre-aligned frame







SPIE Photonics West 2010

Parallel Optical Transceiver

Connector Module



Spring loaded platform

n Microcontroller









Connector Engagement Mechanism

- □ Cam followers guided along cam track
- □ Allows for orthogonal movement of optical platform
- □ Ramped plug for reversible connection



Optical backplane connection architecture





Dual lens coupling interface

Free space coupling arrangement

- Optimised for loss minimisation
- □ Maximum beam expansion



Optical Research and Development Overview

Richard Pitwon

Demonstration assembly



Demonstration platform with peripheral test cards

Electro-optical backplane

Pluggable optical connectors

Compact PCI chassis

High speed switch line cards

XFP front end

Single board computer

SPIE Photonics West 2010



xyratex.

Demonstration assembly



Procedure

10 GbE LAN test traffic @
 10.3 Gb/s into demo front end
 (1st line card)

Data passed acrosspluggable connectors andoptical backplane

Data retrieved through front end of 2nd line card

Procedure

- □ 10 GbE LAN test traffic @ 10.3 Gb/s into demo front end (1st line card)
- Data passed across pluggable connectors and optical backplane
- Data retrieved through front end of 2nd line card

Results

- □ Test data captured with typical peak to peak jitter ~30ps (after front end CDR)
- □ Total optical waveguide interconnect loss ranges from -6 dB to -13 dB









Will write something here

EPSRC DTI

Samtec



Richard Pitwon

Xyratex Technology Ltd Langstone Road, Havant Hampshire PO9 1SA United Kingdom

E-mail: rpitwon@xyratex.com

Authors

Richard Pitwon, Ken Hopkins

Kai Wang, David R. Selviah, Hadi Baghsiahi

Bert Offrein, Roger Dangel, Folkert Horst

Markus Halter, Max Gmür

Xyratex Technology Ltd

University College London

IBM Research GmbH

Varioprint AG