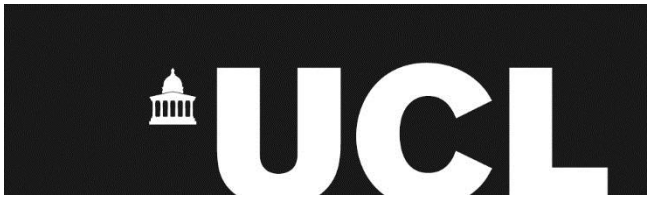
1300-nm InAs/GaAs quantum-dot lasers monolithically grown on silicon substrates

Andrew David Lee

PhD



Dedicated to Dr Tony Winzor, who was the reason I wanted to do a PhD.

Declaration

I, Andrew David Lee, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

Abstract

To imitate the way electrical components evolved from discrete devices to devices integrated on Si platform, the next stage for integrated circuits is to integrate photonic components with electrical components on one chip, with active devices known as optoelectronic integrated circuits (OEIC). An ideal solution for this would be to have an all-Si laser. However due to the indirect bandgap of Si this is difficult to achieve. Therefore attention has been focused on trying to integrate the existing and mature III-V laser technology with Si. The difference in lattice constant between GaAs and Si makes direct, monolithic growth of GaAs on Si difficult due to the generation of high defect densities. But the advances in quantum dot (QD) technology and in III-V buffer layer techniques have led to the improvements of direct growth integration.

In this thesis an AlAs nucleation layer (NL) in the place of a GaAs nucleation layer was found to increase the photoluminescence intensity and reduce defect density in active layers. Lasers were fabricated with lower threshold current densities than similar devices with GaAs NL. Lasing operation at 1.28 μm was achieved up to 63 °C with a threshold current density of 675 A/cm^2 at room temperature.

In addition, Ge-on-Si substrates have been used to demonstrate the lasers on Si substrates with a very low pulsed threshold current density of 64 A/cm^2, which is significantly lower than any other laser integrated with Si substrates. Also this was the first demonstration of a CW laser on Si with a threshold current density of 163 A/cm^2. Lasers were operated up to 30 °C for CW devices and 84 °C for pulsed

devices. The difference in threshold currents and temperature performance between CW and pulsed operation is due to high device resistances caused by a combination of poor contact resistance and the introduction of defects from the Si/Ge interface.

In conclusion, lasers on Si substrates have been fabricated with low threshold current densities. A very low threshold current density of 64 A/cm^2 has been achieved with a Ge-on-Si device and is the lowest result for any type of Si laser at the time of writing, which shows good potential for future integration with Si electronics.

Acknowledgements

I would like to thank my supervisor, Professor Huiyun Liu, without his hard work and attention none of this would have been possible. I would also like to thank Professor Alwyn Seeds for his advice and assistance that he often gave to me.

I also need to thank the other people in the MBE group past and present, particularly, Dr Ting Wang for beginning my fabrication education and KTV education. I would like to thank Dr Qi Jiang for his help in the cleanroom, for not murdering me in cold blood after I dropped a sample he had worked on for two days, and for his company when a cake break or beer was required; finally Dr Frank Tutu, Dr Wu Jiang, and Dr Mingchu Tang also deserve a mention.

I would like to thank others in the department, Dr Kasia Balakier for forgiving me when equipment spontaneously migrated from the 6th floor lab to my lab; Dr Michele Natrella for his constructive criticism of my bakery skills; Steve Etienne of the LCN for fixing a lot of the machines I needed to use; and numerous others who I do not have space to list in full.

I would also like to thank Dr Cyril Renaud and the photonics systems development CDT for providing my funding, and to my fellow CDT students for support during the regular Thursday morning coffee break.

Finally I would like to thank my family and my wife, especially my wife for her unending support and encouragement to submit. Without her I would never have been able to finish.

List of publications

Journal papers

1. J. Wu, **A. Lee**, Q. Jiang, M. Tang; A. Seeds, H. Liu, "Electrically pumped continuous-wave 1.3-μm InAs/GaAs quantum dot lasers monolithically grown on Si substrates," *Optoelectronics, IET*, vol. 8, pp. 20-24 (2014)

2. **A. Lee**, Q. Jiang, M. Tang, Y. Zhang, A. Seeds, H. Liu, "InAs Quantum Dot Lasers on Ge and Si Substrates (invited)" *Selected Topics in Quantum Electronics, IEEE Journal of* , vol. 19, pp. 1901107 (2013)

3. **A. Lee**, H. Liu, A. Seeds, "Semiconductor III-V lasers monolithically grown on Si substrates", *Semiconductor Science and Technology*, vol. 28, 015027 (2013)
4. **A. Lee,** Q. Jiang, M. Tang, A. Seeds, H. Liu, "Continuous-wave InAs/GaAs quantum-dot laser diodes monolithically grown on Si substrate with low threshold current densities." *Optics Express*, vol. *20*, pp. 22181-22187 (2012)
5. T. Wang, **A. Lee**, F. Tutu, A. Seeds, H. Liu, Q. Jiang, K. Groom, "The effect of growth temperature of GaAs nucleation layer on InAs/GaAs quantum dots monolithically grown on Ge substrates." *Applied Physics Letters*, vol. *100*, pp. 052113 (2012)
6. T. Wang, H. Liu, **A. Lee**, F. Pozzi, A. Seeds " 1.3-μm InAs/GaAs quantum-dot lasers monolithically grown on Si substrates." *Optics Express*, vo. *19*, pp. 11381–11386 (2011)

Conference papers

1. Q. Jiang**, A. Lee,** M. Tang, A. Seeds, H. Liu, "Long-wavelength III-V quantum-dot lasers monolithically grown on Si substrates" *5th IEEE International Nanoelectronics Conference (INEC),* January 2013.
2. **A. Lee**, Q. Jiang, M. Tang, A. Seeds, H. Liu, *"InAs/GaAs Quantum Dots Lasers Grown On Ge and Si Substrates" UK Semiconductors Conference*, July 2012
3. **A. Lee**, T. Wang, F. Pozzi, A. Seeds, H. Liu, "A room temperature electrically pumped 1.3-μm InAs quantum dot laser monolithically grown on silicon substrates," *8th IEEE International Conference on Group IV Photonics (GFP), 2011*, vol., no., pp.184-186, 14-16 Sept. 2011
4. **A. Lee**, T. Wang, H. Liu, F. Pozzi, A. Seeds, "1.3μm InAs/GaAs quantum dot lasers monolithically grown on Si substrates" *UK Semiconductors Conference*, July 2012

Table of Contents

Table of Figures

Chapter 1

Chapter 2

Chapter 4

Chapter 5

List of Tables

Chapter 1: Introduction

1.1 Introduction

Ever-higher data rates are required due to the advent of smartphones and streaming services such as the BBC iPlayer and Netflix. Emerging technology will put more pressure on the network. It is predicted that the global IP traffic will be 1.3 zettabytes (IP traffic in 2011 was 369 exabytes) by 2016 [1]. This increased usage is driven by a number of factors: (i) the amount of users is expected increase to 3.4 billion (45% of population by UN estimates); and (ii) there is also an expected increase in users number of devices from 10.3 billion in 2011 to 18.9 billion by 2016. Finally the amount of high quality video streaming (3DTV and HDTV) is expected to increase by up to 5-fold.

Up to now increases in demand for higher computing speeds could be satisfied by decreasing the size and cost of transistors in integrated circuits (IC), making devices smaller and cheaper. Moore's law predicted that the number of transistors capable of being manufactured in a given area at minimum cost would double approximately every 2 years. A variant of Moore's Law is that the number of calculations per second per $1,000 has increased exponentially.

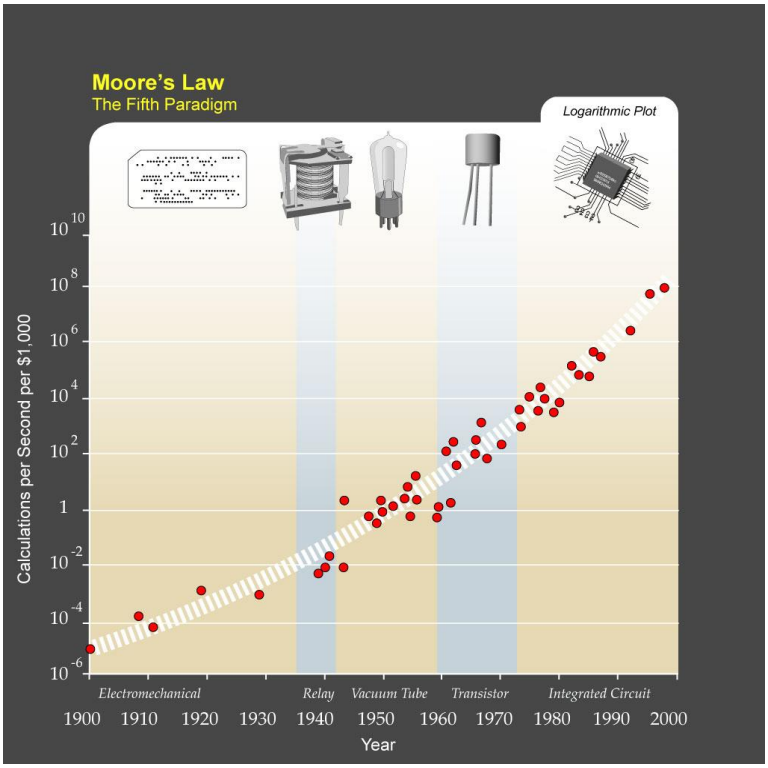


Figure 1.1. Number of calculations per second per $1,000 plotted against year. Paradigm shifts from relays, vacuum tubes, transistors and integrated circuits have enabled this increase [2]. *Permission to reproduce this figure has been granted by Creative Commons License*

As Figure 1.1 illustrates, to continue this increase in processing power, multiple paradigm shifts have been required. An important, relatively recent change was the move from discrete components to integrated components on one chip. The first integrated circuit (IC), shown in Figure 1.2(a), was developed in 1958, simultaneously but independently, by Jack Kilby at Texas Instruments and Robert Noyce at Fairchild Semiconductor Corporation. Kilby, for his part, was awarded a share of the Nobel Prize in Physics in 2000 [3]. This scale of device became known retrospectively as small-scale integration (SSI) as the devices merely consisted of a few transistors on one chip and were only capable of having a low number of logic gates. SSI circuits were used in the 1960's such as in the Apollo guidance computer as shown in Figure 1.2(b). The next step in the late 60's was medium-scale integration (MSI) circuits, where hundreds of transistors per device were integrated onto one substrate. The development of MSI devices was driven by the fact that they could be produced at only slightly higher cost but significantly better performance in comparison to SSI circuits. The same economic factors led to the development of large-scale integration (LSI) in the late 70's. LSI enabled the fabrication of IC having

hundreds of thousands of transistors. The next stage in development was very-large-scale integration (VLSI). Modern VLSI devices now have billions of transistors on one chip shown in Figure 1.2(c-d).

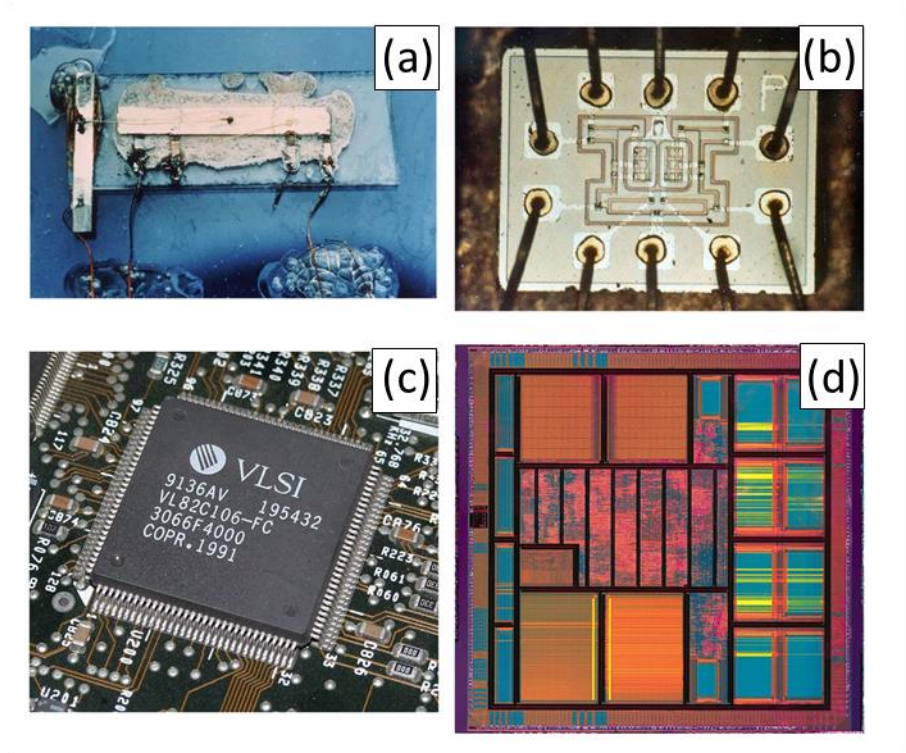


Figure 1.2. (a) Kilby's original integrated circuit. [4] (b)A SSI logical NOR gate from the Apollo guidance computer. [5] c) A typical VLSI chip [6] and (d) a typical VLSI die [7]. *Permission to reproduce this figure has been granted by Creative Commons License*

In 2012, a 22-nm 3-D tri-gate transistors entered high volume fabrication at Intel [8]. More recently, the production of 14-nm transistors has been announced by Intel and Altera [9]. However even researchers at Intel have predicted that there will be a limit to the possible size of transistors [10]. Therefore a new paradigm shift is required, mirroring the way discrete components were replaced by integrated circuits.

1.2 Interconnects

For the development of the IC, it is not sufficient only to produce transistors of small size, but also there must be means for the transistors to communicate with each other. This task is most commonly performed by metal interconnects. Some common minimum requirements for interconnects are that they should offer a low resistivity, and be easy to process and be relatively cheap. The four metals with the lowest resistivity are aluminium, copper, silver and gold. The exceedingly high cost

of gold and silver rules out their usage in interconnects, leaving aluminium and copper. The first IC used aluminium interconnects, as Al was easier to process than Cu but nevertheless offered a low bulk resistivity (2.65 Ω x 10^{-8} m [11]). As dimensions were reduced and the number of interconnects increased, aluminium became insufficient. However it was not straightforward to use copper in device fabrication as copper would diffuse into dielectric films, resulting in poor adhesion to the dielectric. In 1997, IBM and Motorola [12] solved this problem by developing a new fabrication technique known as the Damascene process, which meant that, for the first time, copper could be used for metal interconnects on ICs, instantly improving device performance. Further decreases in component size and increases in number of connections have demonstrated the predictable limitations of copper. Due to the small size of transistors and high speeds, copper interconnects start to have limitations due to its material properties, e.g. losses.

Copper interconnects are used as chip-to-chip and chip-to-module interfaces over traces on printed circuit boards (PCB), chip-to-chip on backplane and in chip-to-chip over copper cable assemblies. A key limitation of copper interconnects is the loss introduced at high frequencies. For example, common copper trace material losses of ~0.15 – 1.5 dB/inch and ~2.0~3.0 dB/inch are incurred at 5 and 12.5 GHz respectively [13]. Further losses such as insertion loss, return loss and cross talk can also become more significant at higher frequencies. In order to accommodate these losses, circuits are designed utilising various methods to counteract loss. This has the downside of increased power usage. This means that for ~ 10 m of interconnect it becomes more effective to use optical interconnects than copper interconnects. Higher operating speeds are decreasing this critical length. Also, the length of copper interconnects in an IC is increasing (due to increase in number of transistors). Above the critical length, the normal methods designed to account for losses have a too high power requirement to make practical [13]. In comparison, optical fibres have virtually no loss even at large distances, with losses of ~ 1 and 0.4 dB/km at 1300 nm for multimode fibre (MMF) and single mode fibre (SMF) respectively [13]. Sending a signal via an optical fibre has a much smaller power usage compared to a copper interconnect as the signal requires little amplification and is immune to electro-magnetic interference. In order to use optical interconnects in links of < 10 m, the photonic integrated circuit (PIC) is required.

1.3 Photonic integrated circuits and Si photonics

Silicon-based PICs can be classified by two broad types, active and passive [14]. A passive PIC is one where the optical function is fixed such as a waveguide. In an active PIC the function is variable. Examples of active PIC are emitters (such as lasers and LEDs), amplifiers, detectors and modulators. Both active and passive Si-based PICs have been demonstrated, such as: modulators [15], waveguides [16] and photo-detectors [17]. However there is still one area that is missing, i.e., an optical source on the Si platform. Most Si-based PICs to date have had "off-chip" actuation and control where the device is controlled "off-chip", for example by making use of wire bonds.

A special case of a PIC is an optoelectronic integrated circuit (OEIC), in which the control is all performed "on-chip" and the electronic and photonic parts of the circuit are integrated on the same chip. OEICs have the potential to be very cost effective, compact, reliable, efficient and highly integrated. In the future they may be able to solve the problems of communications which electronics and photonics alone are not able to solve. OEICs were first envisioned in the 1980s [18]. The two main motivations for developing silicon photonics and OEICs are that:

1. Si photonics will be able to utilise the existing infrastructure of the Si microelectronics industry. This will enable highly sophisticated devices to be fabricated.

2. If photonics components are able to be monolithically integrated with very-large scale integration (VLSI) electronics to create an OEIC, the knowledge, experience, capital investment and tools of the Si industry can be successfully transferred to OEIC with high-volume and low-cost manufacture possible.

Unfortunately, the indirect bandgap of Si creates a problem when designing OEICs. The indirect SI bandgap means that Si cannot easily amplify light. Therefore alternative options are needed for OEICs. These are as follows:

1. Integration of III-V lasers on-chip
2. Off-chip laser that optically pumps multiple Si Raman lasers on-chip
3. Off-chip lasers which can communicate with an OEIC with no lasers on-chip.

Integrating III-V lasers with Si on-chip would be the most appealing option, as it would remove the need to have an off-chip laser, which would add an expense and extra complexity to OEIC manufacture.

1.4 Semiconductor lasers

A laser is an externally pumped self-sustained oscillator consisting of a gain medium inside an optical cavity, which provides feedback [19]. All lasers only vary with the choice of gain medium and pumping mechanism. It will be assumed that the pumping mechanism is current injection. If there is a section of semiconductor material of cavity length L, it can be considered as a Fabry-Perot (FP) cavity as described in Figure 1.3.

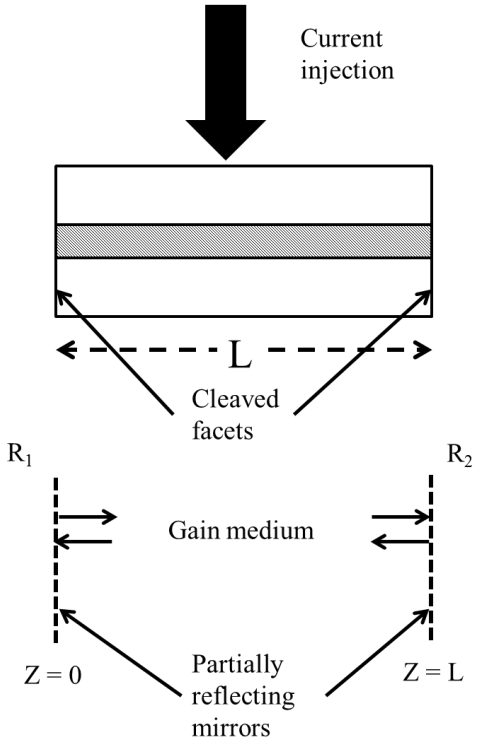


Figure 1.3. Schematic of a semiconductor laser of cavity length L, and its Fabry-Perot (FP) cavity.

The mirrors have a reflectivity of R_1 and R_2. The gain of the cavity is written as g. The cavity will also have an associated loss, which can be due to several mechanisms such as free carrier absorption and scattering at the interfaces between materials. The total absorption can then be written as

$$\alpha = -\Gamma g + \alpha_{int} \qquad \text{Equation 1}$$

where α_{int} is the term representing the internal losses, and Γ is the confinement factor, which accounts for reduction of gain which occurs due to the fact the optical mode spreads beyond the gain region. It represents the fraction of energy contained in the active region.

In order to calculate the threshold gain condition, it is assumed that the laser should be in equilibrium, which means that the total losses equal the total gain. The threshold gain condition can be obtained as

$$\Gamma g = \alpha_m + \alpha_{int} \qquad \text{Equation 2}$$

where

$$\alpha_m = \frac{1}{2L} ln\left(\frac{1}{R_1 R_2}\right). \qquad \text{Equation 3}$$

The losses due to energy leaving the cavity are expressed via α_m. Therefore the gain must balance the losses due to the losses in the cavity. However this is only an approximation as this calculation ignores the contribution of spontaneous emissions. This would act to decrease the threshold gain required to obtain lasing.

Another consideration is that the mirror reflectivity will affect how much power exits the cavity. The useful output power from one facet equals

$$P_{out} = T_1 P_{internal} \qquad \text{Equation 4}$$

where $T_1 = 1 - R_1$ and is the transmission of the mirror R_1 and $P_{internal}$ is the power inside the cavity. However, the second facet will also allow light to be emitted, therefore the total power of light emitted from both facet equals

$$P_{emitted} = T_1 P_{internal} + T_2 P_{internal} \qquad \text{Equation 5}$$

and by rewriting equation 4, the power out from one facet can be written as

$$P_{out} = P_{emitted} \frac{T_1}{T_1 + T_2}. \qquad \text{Equation 6}$$

A typical value for reflectivity of an as-cleaved GaAs facet is ~ 30% [20]. This can be increased by the use of a high reflectivity coating [21,22] on the facet. Alternatively a DBR (distributed Bragg reflector) lasers or can be fabricated where at least one of the mirrors is a Bragg reflector, and the mirrors are external to the cavity [19]. Similar to a DBR laser a DFB(distributed-feedback) laser is a laser where the whole

of the resonator consists of a periodic structure which acts as a distributed reflector and contains a gain medium [19]. However, DBR and DFB semiconductor lasers are more complicated to fabricate than lasers with as cleaved facets because regrowth is required to grow the Bragg reflectors , and therefore only edge emitting lasers were fabricated in this work.

1.4.1 Double heterostructure lasers

The first double heterostructure lasers were fabricated with thicknesses of the active layers in the range of ~ 0.1 – 0.5 μm. However due to advances in growth techniques, it has been possible to grow ever thinner layers, with active areas ~ 10 nm thick. This leads to restriction of the motion of electrons in the well in one dimension and quantisation of the kinetic energy of the electrons, known as the quantum size effect. The property that determines if the quantum size effect becomes significant is the de Broglie wavelength ($\lambda \cong h/p$) [23]. These effects can be compared to the potential well problem in quantum physics, so they are known as quantum well lasers.

1.4.2 Quantum structures

If an electron is confined in an infinite potential well along the z-dimension, the particle is free to travel in the x and y-dimensions. Therefore in the x and y directions, the energy for a continuum of states is

$$E = \left(\frac{\hbar^2}{2m}\right)(k_x^2 + k_y^2) \qquad \text{Equation 7}$$

where k_x and k_y are the wavevector components in the x and y directions, and m is the effective mass of the particle [24]. To obtain the energy levels of the particle in the z direction Equation 7 can be solved using the Schrodinger equation. In the case of an infinite well (where the potential goes to infinity outside of the well and is zero inside) the energy levels and wavefunction are defined as

$$E_n = \frac{\hbar^2}{2m}\left(\frac{n\pi}{L_z}\right)^2 \qquad \text{Equation 5}$$

$$\psi_n = \begin{cases} A \sin\frac{n\pi z}{L_z} \\ 0 \end{cases} \qquad \text{Equation 6}$$

Where n is a positive integer and A is a normalisation constant. This means that the energy of the particles in the z direction are quantized to certain allowed values, with large values of L leading to energies which are no longer quantised. However this is only true in the case of an infinite well. In a more realistic problem a finite well can be used. In this case, the particle can exist outside of the well and the solution of the wavefunction is

$$\psi = \begin{cases} A\exp(k_1 z) & (z \leq 0) \\ B\sin(k_2 z + \delta) & (0 \leq z \leq L_z) \\ C\exp(-k_1 z) & (z \geq L_z) \end{cases} \qquad \text{Equation 7}$$

Where A, B, C and δ are constants. And

$$k_1 = \left[\frac{2m(V-E)}{\hbar^2}\right]^{1/2} \qquad k_2 = \left(\frac{2mE}{\hbar^2}\right)^{1/2}$$

To obtain the energy levels the eigenvalue equation $\tan(k_2 L_z) = k_1/k_2$ must be solved numerically. A schematic of the wavefunctions for a finite well is shown in Figure 1.4.

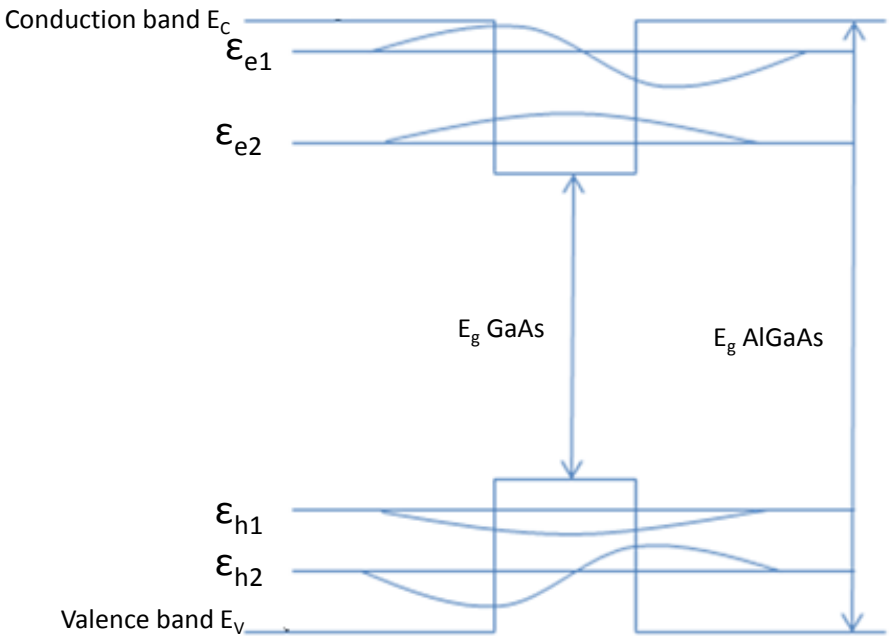


Figure 1.4. Schematic of quantum well energy levels in GaAs/AlGaAs system. Particles can tunnel out of well with energies less than the well depth.

If the confinement is increased into three dimensions then the electron is no longer free to move in any direction and the new energy can be written as

$$E_{n,m,l} = \frac{\hbar^2}{2m}\left(\frac{n\pi}{L_x}\right)^2 + \frac{\hbar^2}{2m}\left(\frac{m\pi}{L_y}\right)^2 + \frac{\hbar^2}{2m}\left(\frac{l\pi}{L_z}\right)^2 \qquad \text{Equation 8}$$

If the electron is confined to a size less than the de Broglie wavelength in each dimension, then this is known as a quantum dot, and brings many advantages due to its special density of states and confinement. In this case the problem has been solved in Cartesian coordinates to keep the solution simple. Although quantum dots are unlikely to be rectangular, it is not necessary to solve using a radial potential as the solution still results in quantised energy levels.

1.4.3 Advantages of quantum dot lasers

The density of states refers to the number of allowed energy states in a certain volume. In the case of a structure with no confinement then this can be calculated by working out the number of filled states in k-space of a sphere of radius k and dividing this by the volume of a single state. As the degree of confinement increases the density of states will change from a 3-dimensional volume to a 2-dimensional volume until the particle is confined in all directions so that the system is a zero-dimensional volume. In the ideal case of a truly zero-size structure, there is no k-space as only certain discrete energies are allowed. Therefore the density of states could just be written as a delta function

$$D_{0D} = 2\delta(E - E_c)\,. \qquad \text{Equation 9}$$

In real systems at practical temperatures, the delta functions are broadened for example inhomogeneous broadening effects such as broadening because of the finite size of the quantum dot. Despite the broadening, the density of states of quantum dot systems are still much wider than in bulk or quantum well systems. This means that there is a large separation of energy between states. Therefore there is a large density of carriers, which could make the energy state resistant to changes in temperature [21]. This means that lasers can be designed with stabilised emission wavelength and less dependence on temperature for threshold [25]. QD lasers have been demonstrated to have very low threshold current densities, as low as 10.4 A/cm^2 [26-28] and very high characteristic temperatures [29,30], which is due to

the discrete density of states. Overall, the laser threshold is reduced and differential gain increased as fewer injected carriers are required for population inversion [31].

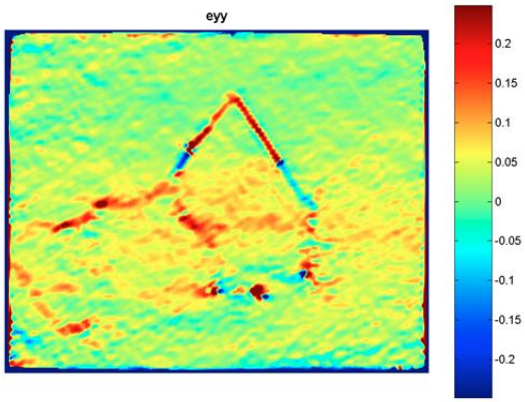


Figure 1.5. Strain analysis of HRTEM image showing strain component in growth direction. *Reprinted with permission from* [32]. *Copyright [2008], AIP Publishing LLC*

In addition to lower threshold currents and improved temperature dependence for QD lasers, there are advantages to using QDs in growth of III-V compounds on Si over quantum well lasers. QDs are able to reduce the possibility of defect propagation into the active layers, as shown in Figure 1.5, where the high shear stresses present between the QD and surrounding material have acted to capture dislocations and prevent them propagating towards the active layers [32]. QD layers have been used successfully in both the buffer layers at III-V/Si interface [33] and also in the active layers. This has led to QD lasers being fabricated on Si operating at room temperature [34].

1.5 Silicon material properties

The barrier to an all-Si laser is its indirect bandgap [35]. An indirect bandgap refers to the fact that the top of the valence band and bottom of the conduction band occur at different values of crystal momentum as shown in Figure 1.6. This means that a direct transition of an electron from the bottom of conduction to top of valence band, leading to the emission of a photon, is not possible. This is because in the case of visible and infrared photons, the momentum of a photon is negligible compared to the energy of the photon, and hence the transition is essentially vertical. Consequently in the case of indirect bandgap materials, a horizontal phonon

transition is required to change the momentum of the electron. However this now means that the process is a two-body process.

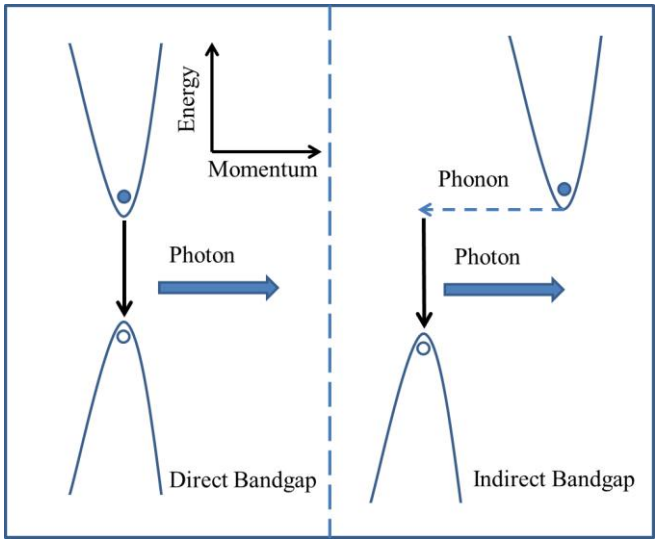


Figure 1.6. Schematic of bandgap alignment for direct and indirect bandgap.

For indirect bandgap materials, the electron has to wait for a phonon in order to be able to undergo a radiative recombination. However, as the lifetime of two-particle radiative emission in Si is long, ~ 1s, the electron is far more likely to undergo non-radiative recombination, as the lifetime of this process is far shorter, in the range of milli to micro seconds [19].

1.5.1 All-Si light amplification

There are methods to get around the indirect bandgap of Si. Possible options for all-Si lasers include the following approaches: utilising the Raman effect in Si, Er doping of Si, and using quantum confinement with Si quantum dots (QD) [36].

Er dopingand Si nanocrystals

Fibres doped with rare-earth metals are used readily to amplify light; the most common example of this is the Er doped fibre amplifier (EDFA) [37]. These rely on transitions between the atomic levels, known as intra-4f transitions, of the rare earth ion for the amplification. However the absorption band is weak and narrow so EDFAs rely on having long interaction distances and a laser that must be tuned to the exact atomic absorption band.

In order to reduce the interaction distance, the Er ions can be implanted in a host material that provides a much larger absorption cross section [38]. Si can provide a particaulay useful host material, as it is transparent to 1.5 μm signal photons, but still provides a larger absorption cross section for pump photons with energies above 1.1 eV. However, the low optical activity of Er in Si and strong termpearature quenching of Er luminescence makes the use of bulk Si impractical [39,40]. An attractive alternative is to implant Er ions into Si nano clusters in silica, rather than bulk silicon,[41].

Optical gain has been demonstrated by the growth of Si nano crystals in silica [42] and light emission has been demonstrated from Si quantum dots [43]. However these devices suffer from low efficiencies (power effiencies < 1%). Also, due to the long lifetime, the maximum modulation frequency is limited to the MHz regime. The efficiency can be improved by addition of Er doping, close to 0.1% [44]. Further improvement is unlikely due to three fundamental reasons: (1) the limited maximum energy of hot electrons in Si, (2) the efficient energy losses such as Auger recombination with free carriers in Si, and (3)the limited maximum density of Er atoms to avoid clustering [45].

Raman Si laser

In order to achieve lasing in a Raman laser, the medium is optically pumped and the pump photons are absorbed and then re-emitted as lower frequency laser-light photons by stimulated Raman scattering [46,47]. The energy difference between the emitted and absorbed photon corresponds to a vibrational frequency of the gain medium.

Continuous-wave Raman lasers using an optical fibre as the game medium were demonstrated in the mid 70's [48]. The Raman effect in silicon was utilized by researchers at Intel to produce the first silicon lasing devices at room temperature [49]. However the lifetime of these lasers have been severely limited by two-photon absorption. Furthermore due to the technique used to obtain lasing, only optically pumped devices are possible.

1.5.2 Alternatives to all-Si lasers

Ge-on-Si laser

Ge is normally classified as an indirect band gap material. However, by incorporating strain and n-type doping into Ge, the material can be engineered to have a direct bandgap [50]. This is because the energy difference between the indirect bandgap and direct bandgap is only 136 meV. The bandgap engineering is performed by adding tensile strain to Ge, to compensate for the difference between the direct (Γ) and indirect (L) conduction band valleys, the energy difference is then further equalised by filling the L conduction valley with electrons via n^+ doping. This is shown in Figure 1.7.

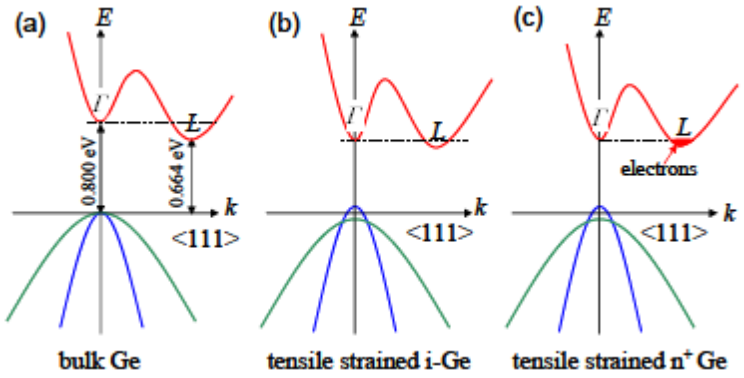


Figure 1.7. (a) Schematic band structure diagram of Ge showing the difference between the direct and indirect bandgaps of Si. (b) The difference can be partially compensated by tensile strain. (c) Remaining difference is compensated for by n^+ doping. *Reproduced with permission from [50].* Copyright [2007] The Optical Society of America.

This technique has been used to demonstrate lasers on Ge-on-Si substrates [51]. However, these devices still have extremely high pulsed threshold current densities, approximately 300 kA/cm^2, which is at least two orders of magnitude higher than devices fabricated by hybrid techniques or monolithic growth where typical threshold currents are significantly less than 1 kA/cm^2. The threshold currents are high because of the small energy difference between the direct and indirect bandgaps, which increases the probability of spontaneous emission.

1.5.3 III-V Lasers on silicon

As the production of a Si or Ge laser is difficult, a tempting alternative is to leverage the long-established semiconductor laser industry. The first laser diode on semiconductor III-V compounds was demonstrated in 1962 [52]. Now the field is very mature and lasers grown on GaAs and InP substrates can be mass-produced at relatively low per-unit cost. III-V based lasers grown directly on Si substrates instead of GaAs and InP substrates would be an ideal solution. However this is a huge challenge due to the large lattice mismatch between Si and GaAs, as conventional growth techniques require lattice matched materials. Any growth is further complicated by the 250% difference in thermal expansion coefficient between Si and GaAs [53]. This means that any crystal growth method leads to the formation of threading dislocations (TD) and anti-phase domains (APD) which severely increase the amount of defects in the active layers of any device and thus increase the threshold current density of any lasing device. Consequently, early devices grown on Si had poor characteristics with high threshold current densities, approximately 7 kA/cm^2 [54,55]. Later devices had lower threshold current densities but also an emission wavelength of 857 nm [56], which is not so useful for telecommunications applications at it is outside the two low loss windows of fibre.

Hybrid techniques

The difficulties caused by the large lattice mismatch between Si and GaAs led research activities on silicon photonics away from direct growth on Si to a hybrid technique. In hybrid techniques, laser structures are grown on GaAs or InP substrates then the active layers removed and bonded onto a Si substrate [57]. There are a variety of different techniques to bond a GaAs wafer to a Si wafer [58]. Wafer bonding can be performed at room temperature. In order to bond the two surfaces, both surfaces must be clean and mirror-polished. Bringing the surfaces in contact with each other at high pressure results in a bond due to the Van der Waals forces between atoms on both surfaces [59].

Another technique is to use a glass-like bonding layer, such as SiO_2, borophosphorosilicate glass, SeS_2, or solutions based on silane and methyl polymers dissolved in an alcohol-acetone mixture [60], the bonding layer is then coated on the surfaces of both materials and raised to high temperature, and the two substrates brought together under high pressure.

By the use of hybrid methods, lasers with thresholds around ~200 A/cm^2 have been shown [61] in pulsed operation by direct fusion bonding. However there are serious issues for this approach. The reliability of the bonding process has yet to be demonstrated [57],[61]. In contrast it has been demonstrated that the direct growth of lasers on Si can lead to excellent repeatability and uniformity of lasers on Si [62]. Also, there are problems due to the differences between thermal expansion coefficient of GaAs and Si. This could bring in reliability issues for bonded devices, when OEICs operate at high temperatures as expected.

1.6 Review of III-V monolithic growth on silicon platform

Recently there has been progress in the field of direct growth of III-V compounds on a Si platform. This section will review some of these work, including GaSb-based QW lasers operating at 1.55 and 2 μm [63,64], InAs QD lasers emitting at 1.05 and 1.3 μm [34,65], and 1.3 μm lasers grown on Ge in CW operation up to 60 °C and pulsed operation above 100 °C [66,67]

1.6.1 Challenges facing monolithic growth

There are three main factors, which make the growth of GaAs on Si a challenging prospect. One is the formation of anti-phase domains (APD), where the atoms of the crystal are no longer in a perfect lattice order, but are in an opposite order. The formation of APDs is caused when growing a polar compound (such as GaAs) on miss-oriented non-polar silicon. The second challenge is the formation of threading dislocations, which are caused by the large lattice mismatch between Si and GaAs. The third is micro-cracks, which are due to the fact that Si and GaAs have different thermal expansion coefficients.

Anti-phase domains

If Si could be produced perfectly flat, the problem of APD formation could be reduced. However, Si has terraces which lead to the emergence of APDs [68]. A technique that has been used to reduce the impact of APD formation is to grow on miscut Si, typically with a miscut of a few degrees [69]. This is shown schematically for the example of AlSb on Si in Figure 1.8, whereby a step height equal to double the spacing of the AlSb lattice has been chosen by choosing the correct miscut angle. However this produces complications in the integration of complimentary-metal-oxide semiconductors (CMOS) technology and III-V lasers on Si as the former is

grown on non-miscut Si substrates. Some work has been down to obtain lasers on non-miscut Si. However to date this has been limited to the demonstration of LEDs [70].

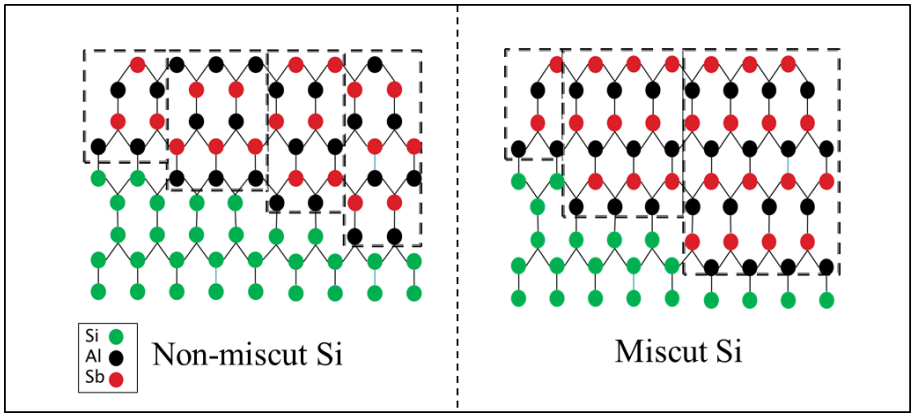


Figure 1.8. Schematic for growth of polar compounds on non-polar substrates. The image on the left shows a substrate that has been cleaved so that the terrace step height is equal to double the bond length so the formation of APDs are limited.

Threading dislocations

Threading dislocations are due to the lattice mismatch between Si and GaAs (~4%). This places strain on the crystal, and results in formation of dislocations. The typical threading dislocation is on the order of $10^{10}/cm^2$, this is compared to the residual value in bulk GaAs which is $\sim 10^3/cm^2$. Threading dislocations are problematic because they act as radiative recombination centres and can promote dark line defects. In order to counteract the formation of dislocations the initial nucleation layer and buffer layers need to be carefully optimised and designed.

Micro-cracks

The mismatch between the thermal expansion coefficients of Si and III-V compounds can result in tensile stress after cool-down of the substrate from the growth temperature. This can lead to small cracks forming in the material. To help prevent micro-cracks, a slow cool-down can be used. Another technique used is to grow a thin layer of compressive material, such as InAlGaAs. This helps to counteract the difference in thermal expansion between layers.

1.6.2 GaSb quantum well lasers on Si

The properties of the initial nucleation layer (NL) for growth of III-V compounds on Si is an important factor for the material quality and the resultant amount of defects

in the active region. It is not as simple as just choosing the compound that needs to be grown in the active layer. AlSb has been shown to handle defects better than other III-V compounds, as the AlSb provides strain relief mechanisms [70]. By using an AlSb NL, a crystalline ensemble is formed which then forms bulk material after further growth. The strain in this bulk material is reduced via crystallographic undulations. The crystallographic undulations provide greater surface area to accommodate strain, and crystallographic undulations are well known in compliant substrate technology [71-72]. The advantage of AlSb NL over other material systems, is that although an AlSb still leads to the growth of misfit dislocations, these dislocations propagate parallel to the surface rather than vertically [70].

An electrically pumped laser on Si has been demonstrated [73]. These lasers were grown by MBE. After a GaSb buffer layer was grown, a 100-nm n-AlGaAsSb layer was grown and then a 1-µm thick n-$Al_{0.9}Ga_{0.1}As_{0.03}Sb_{0,97}$ cladding layer was grown. The active layer made use of 3 $Ga_{0.8}In_{0.2}Sb$ QW separated between two 20-nm thick layers of $Al_{0.35.}Ga_{0.65}As_{0.03}Sb_{0.97}$ and this was all surrounded by two 200-nm thick of $Al_{0.35.}Ga_{0.65}As_{0.03}Sb_{0.97}$ waveguides. The growth was then completed by a 1µm thick p-$Al_{0.9}Ga_{0.1}As_{0.03}Sb_{0,97}$ cladding layer, a 100-nm graded p-AlGaAsSb graded layer and a highly doped 300-nm p-GaSb contact layer. The devices were etched into 100-µm wide mesas and cleaved into 630-µm cavities. The threshold current density at RT was found to be 5 kA/cm^2 at RT. The high threshold current could be explained by a number of factors, such as poor cleaving of Si due to miscut, and/or higher threading dislocation defect densities than on GaSb substrates which would increase optical losses. Finally another problem is the high turn-on voltage, ~ 5 V which is potentially due to the poor conductivity between Si and III-Sb interface.

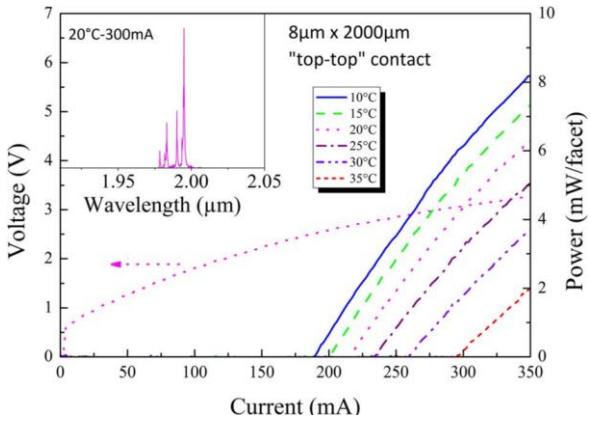


Figure 1.9. CW Optical power versus current for GaSb based lasers on Si emitting at ~2 µm in CW operation and current voltage characteristics. Inset shows the room temperature spectra. *Reprinted with permission from [74]. Copyright [2009] AIP Publishing LLC.*

In order to improve these devices, instead of a "top-bottom" structured device, where the bottom contact is on the substrate, a "top-top" structured device was fabricated. This improved device performance as it lowered the device resistance. This led to devices, which were originally fabricated as "top-bottom" contact devices and weren't able to lase at CW operation [73], being demonstrated in CW operation [74]. A pulsed threshold current density of 900 A/cm^2 was measured for a 2-mm cavity length and 8-μm width. CW operation was achieved up to 35 °C. The current-voltage and current-power relationships are shown in Figure 1.9 with the inset of the figure showing the spectra obtained.

1.6.3 InAs QD lasers grown on Si

Lasers on Si operating at 1 μm

In order to obtain lasers operating at 1.05μm, Si(001) substrates with 4^0 offset towards the [111] plane were used [34]. First a 2-μm GaAs buffer layer was grown via MOVPE. Following this layer a 10-layer InAs QD dislocation filter layer was grown by MBE. InAs QDs were found to best prevent defects propagating into the active layers, which may be because the large size and strain field of InAs QDs can balance the effect of dislocation propagation. The laser structure consisted of a GaAs/$Al_{0.7}Ga_{0.3}As$ separate confinement heterostructures (SCH) QD lasers with p and n doped layers consisting of 1-μm $Al_{0.7}Ga_{0.3}As$ for doped with Be and Si respectively. Broad area lasers were fabricated by conventional techniques and the substrates were thinned to 80 μm to assist in cleaving, which was done along (110) direction. LI measurements were performed on broad area lasers, (600 x 80μm) using a pulsed source (1% duty cycle). The threshold current density was found to be ~900A/cm^2 and a peak spectral output wavelength of 1.05μm was demonstrated.

Following the success in growing a 1.05μm laser the monolithic integration of a laser with modulator was shown in Figure 1.10 [75,76]. A scanning electron microscope image of the laser integrated with modulator is shown in Figure 1.12. More details of growth, and calculations of the groove parameters, such as height and width can be found in Ref. 62. The fabricated devices had a coupling efficiency of above 20% and a modulation depth of ~45% at -3V bias and 100% for -5V bias. The large reverse bias was attributed to the quality of regrowth interface, which has been hypothesised to

contain interfacial defects. Potentially, etching deeper and regrowth on the GaAs buffer layer instead of on the n contact layer could increase material quality and modulator performance.

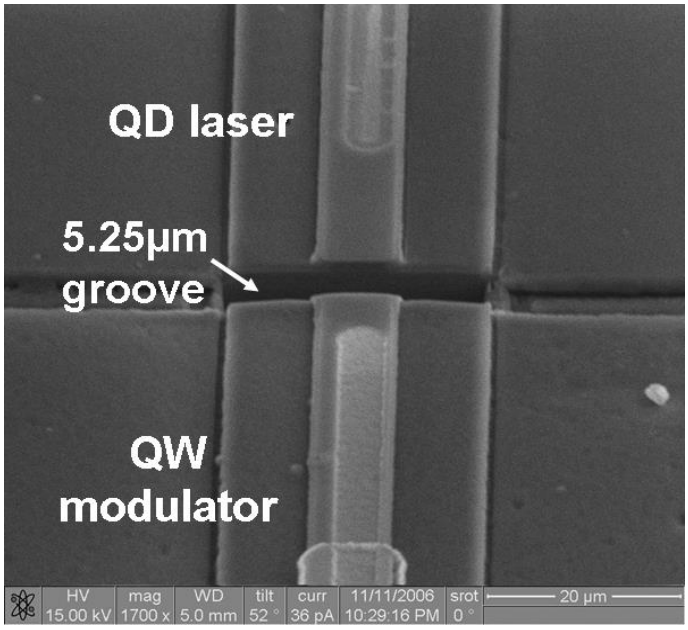


Figure 1.10. Scanning electron microscope image of QD laser integrated with QW modulator. *Reprinted with permission from [76]. Copyright [2007] IEEE Publication.*

Lasers on Si operating at 1.3 μm

Lasers operating at 1.3 μm have been grown on Si (100) with a 4^0 offcut using solid source MBE [65]. It was found that the quality of the active layer strongly depended on the growth temperature of a 5 nm GaAs initial NL. After the growth of a GaAs buffer layer and cladding layers a 5-layer dot-in-well (DWELL) structure was grown, which was identical to a structure previously optimised for growth on GaAs substrates [28]. The 5-layer DWELL structure was grown between 1.5-μm $Al_{0.4}Ga_{0.6}As$ p and n doped cladding layers. Then the growth was completed with a p^+ doped 300 nm contact layer of GaAs. 50-μm broad area lasers were fabricated with Ti/Au contacts for the p metal and Cr/Au on the Si substrate. 3-mm devices were cleaved, and then bar tested without mounting or bonding. The lasers fabricated had a threshold current of 725 A/cm^2 at 1.302μm in pulsed mode at room temperature, as shown in Figure 1.13. The spectra is displayed in the inset of Figure 1.11, the

device had a peak power of around 26 mW. The lasers had no high reflectivity (HR) coating, which would be expected to decrease threshold current. The devices were operated up to 42 ^{0}C and had a characteristic temperature of 44 K.

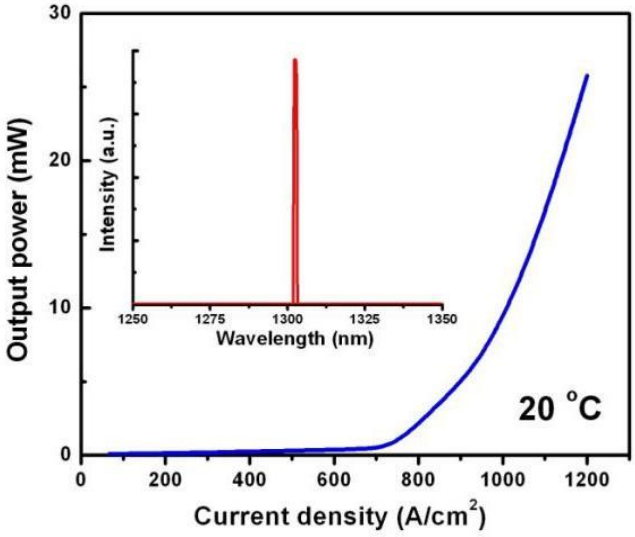


Figure 1.11. Pulsed output power versus current density for an InAs QD laser emitting at 1.3 μm at room temperature in pulsed operation. Inset shows spectra. *Reproduced with permission from [65]. Copyright [2011] The Optical Society of America*.

1.6.4 InAs QD lasers on Ge

Growing lasers on Ge offers many advantages over growth on Si. Firstly, Ge has a lattice constant that it almost lattice matched to that of GaAs (0.08% compared to 4% for Si). In addition there is the likelihood of Ge replacing Si as the p-channel in CMOS devices, due to the higher hole mobility of Ge [77]. These two factors combine to make growth of III-V compounds on Ge substrates a promising prospect. As Ge sounds so promising it might be expected that this would already be a well-developed area. However conventional growth techniques, using As as a initial pre-layer, lead to GaAs material on Ge with poor quality and a large amount of APDs. An example of this growth with formation of APDs is shown Figure 1.12 [78].

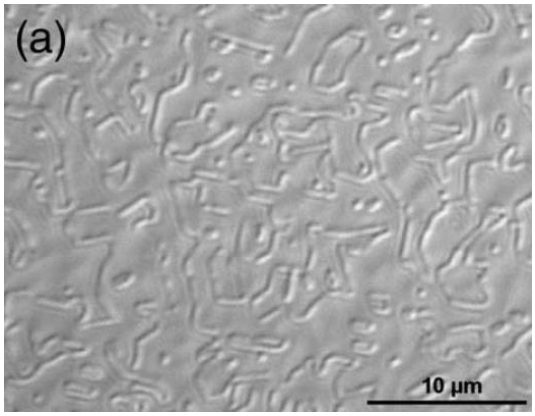


Figure 1.12. Nomarski microscope image of a 1 µm thick GaAs film grown on a non-miscut Ge wafer after defect etching, which reveals the formation of APDs in the material. *Reprinted with permission from [78]. Copyright [2006], AIP Publishing LLC .*

In order to obtain good surface morphology a Ga pre-layer technique was used, where growth of GaAs was initiated with approximately 1 ML of Ga, rather than an As layer [66]. In order to prevent the Ge being terminated with As from the background As pressure during the preparation of the substrate, the main shutter is kept closed over the substrate prior to depositing Ga. Figure 1.13 (a) and (b) shows 5 µm x 5 µm AFM images of 1.2 µm of GaAs grown on Ge with (a) using a As pre-layer and (b) using a Ga pre-layer. Figure 1.13 clearly shows that a better surface morphology is obtained using a Ga pre-layer, as the surface is significantly smoother, indicating growth of single domain GaAs.

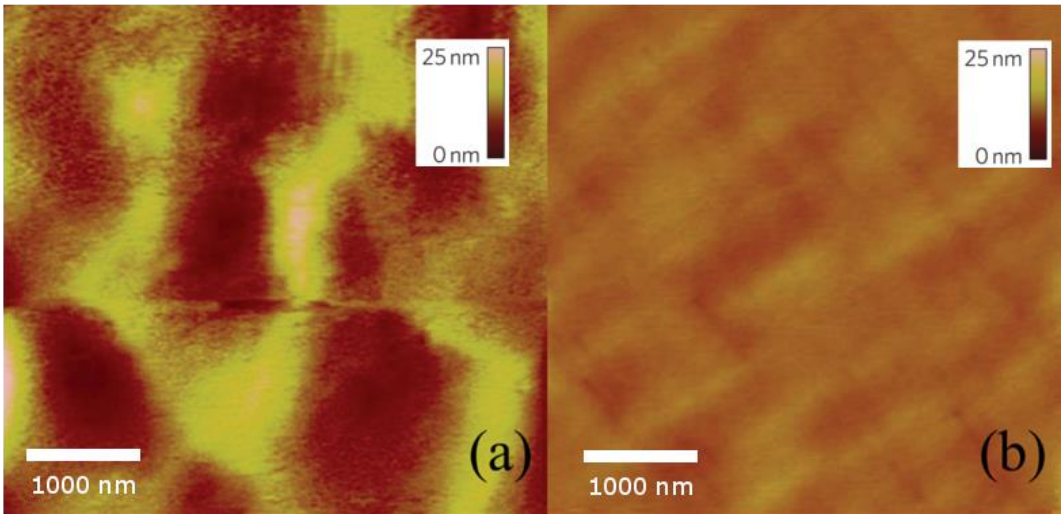


Figure 1.13. 5 µm x 5 µm AFM image of surface morphology after 1.2 µm of growth GaAs. (a) shows the case using a As pre-layer and (b) shows a Ga pre-layer. *Reprinted with permission from* [66]. *Copyright [2011] Macmillan Publishers Ltd*

The details of the Ga pre-layer technique involved keeping the Ge wafer covered by the main shutter until just before the growth of Ga was started. This prevents any As from the MBE background to be deposited on the surface of the Ge. Initially 1.08 MLs of Ga was deposited, then the surface was terminated by opening the As cracker valve. After the nucleation layer of GaA was grown using the Ga prelayer technique 20 MLs of GaAs were grown by migration enhanced epitaxy.

After the growth of a III-V buffer layer the exact same laser structure as in Ref. 13 was grown. Ridges were wet etched to 1.8 µm, with a width of 50 µm, then 500 nm of SiN_x was deposited. In/Ge/Au was used for the n contact layer and Al and Au/Zn/Au for the Ge and GaAs p contact layers respectively. Devices with 5 mm cavity lengths were cleaved and bar-tested. The mirrors were left as-cleaved and had no high reflectivity coating. Lasing occurred at 1.305µm with a threshold current density of 55.2 A/cm^2 under CW current drive and at room temperature. The lasers were operated between 20°C and 60°C with a value of T_0 ~40K, similar to that obtained of a GaAs reference and the power-current measurements can be seen in Figure 1.14 for various temperatures.

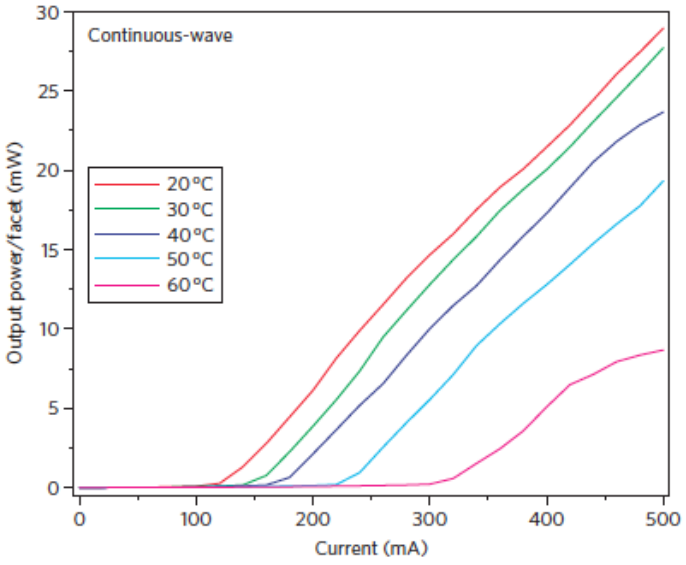


Figure 1.14. CW Output power versus current for lasers in CW operation grown on Ge substrates. *Reprinted with permission from* [66]. *Copyright [2011] Macmillan Publishers Ltd*

1.7 Thesis structure

The organisation of this thesis is as follows. Chapter 1 gives the motivation for research into Si photonics, and the need for a Si or Si integrated source. It discusses some of the background theory of quantum dot lasers. It also reviews current advances in the use of Si as an active material in lasers and describes some of the work that has been done up to now on monolithic integration of III-V compounds on Si and Ge.

Chapter 2 gives details of experimental techniques used in the work, including the details on MBE growth and characterisation of samples and gives details of the device process flow.

Chapter 3 discusses the optimisation of the device processing, particularly the usage of sputtered contacts and wire bonds.

Chapter 4 describes the use of an AlAs nucleation layer instead of a GaAs nucleation layer and the improvement in photoluminescence intensity and device performance.

Chapter 5 describes the growth of an electrically pumped laser on Ge-on-Si substrates. This device operated at a very low threshold current, which is significantly lower than any laser integrated on Si. In addition this was the first quantum dot laser on Si to be operated in CW mode.

Chapter 6 will discuss future work that could be done.

1.8 References

[1] “Cisco® Visual Networking Index (VNI) Forecast (2011-2016).” .

[2] "PPTMooresLawai" by Courtesy of Ray Kurzweil and Kurzweil Technologies, Inc. -Licensed under Creative Commons Attribution

[3] “‘The Nobel Prize in Physics 2000’. Nobelprize.org. 15 May 2013 http://www.nobelprize.org/nobel_prizes/physics/laureates/2000/.”.

[4] “Kilby solid circuit" by Texas Instruments - Licensed under Fair use of copyrighted material

[5] "Agc nor2" Licensed under Public domain

[6] “VLSI Chip" by Appaloosa - Licensed under Creative Commons Attribution

[7] "Diopsis". Licensed under Creative Commons Attribution

[8] “www.intel.com/technology/architecture-silicon/22nm/.” .

[9] “Altera to Build Next-Generation, High-Performance FPGAs on Intel’s 14 nm Tri-Gate Technology.” [Online]. Available: http://newsroom.intel.com/community/intel_newsroom/blog/2013/02/25/altera-to-build-next-generation-high-performance-fpgas-on-intels-14-nm-tri-gate-technology.

[10] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, “Limits to binary logic switch scaling - a gedanken model,” *Proceedings of the IEEE*, vol. 91, no. 11, pp. 1934-1939, 2003.

[11] R. A. Matula, “Electrical resistivity of copper, gold, palladium, and silver,” *Journal of Physical and Chemical Reference Data*, vol. 8, p. 1147, 1979.

[12] “http://www03.ibm.com/ibm/history/ibm100/us/en/icons/copperchip/.” .

[13] Altera, “Overcome Copper Limits with Optical Interfaces,” no. April. 2011.

[14] G. T. Reed, *Silicon Photonics: The State of the Art*. New York, NY, USA: Wiley-Interscience, 2008.

[15] G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, “Silicon optical modulators,” *Nature Photonics*, vol. 4, no. 8, pp. 518-526, Jul. 2010.

[16] J. Leuthold, C. Koos, and W. Freude, "Nonlinear silicon photonics," *Nature Photonics*, vol. 4, no. 8, pp. 535-544, Jul. 2010.

[17] M. Paniccia and N. Photonics, "Integrating silicon photonics," *Nature Photonics*, vol. 4, no. 8, pp. 498-499, Aug. 2010.

[18] R. Soref and J. Larenzo, "All-silicon active and passive guided-wave components for 1.3 and 1.6 μm," *Quantum Electronics, IEEE Journal of*, vol. 22, no. 6, pp. 873-879, Jun. 1986.

[19] G. P. Agrawal and N. K. Dutta., *Semiconductor lasers*, 2nd ed. New York: Van Nostrand Reinhold, 1993

[20] M. Ettenberg, H. Sommers, H. Kressel, H. Lockwood, "Control of facet damage in GaAs laser diodes" *Applied Physics Letters*, 18, 571-573 (1971), DOI:http://dx.doi.org/10.1063/1.1653545

[21] J. Coleman, J. Young, and A. Garg, "Semiconductor quantum dot lasers: a tutorial," *Lightwave Technology, Journal of*, vol. 29, no. 4, pp. 499-510, 2011.

[22] H. L. Huffaker, G. Park, Z. Zou, O. B. Shchekin and D. G. Deppe, "1.3 μm room-temperature GaAs-based quantum-dot laser", *Applied Physics Letters*, **73**, 2564 (1998)

[23] A. I. M. Rae, Quantum Mechanics, (Fourth Edition), CRC Press, 2002

[24] B. H. Bransden, C.J. Joachain, Quantum mechanics (2nd ed.). Essex: Pearson Education., 2000 ISBN 0-582-35691-1.

[25] Y. Arakawa and H. Sakaki, "Multidimensional quantum well laser and temperature dependence of its threshold current," *Applied Physics Letters*, vol. 40, no. 11, p. 939, 1982.

[26] D. Deppe, K. Shavritranuruk, and G. Ozgur, "Quantum dot laser diode with low threshold and low internal loss," *Electronics Letters*, vol. 45, no. 1, pp. 54-56, 2009.

[27] G. Park, O. B. Shchekin, D. L. Huffaker, and D. G. Deppe, "Low-threshold oxide-confined 1.3- μm quantum-dot laser," *Photonics Technology Letters, IEEE*, vol. 12, no. 3, pp. 230-232, 2000.

[28] H. Y. Liu, D. T. Childs, T. J. Badcock, K. M. Groom, I. R. Sellers, M. Hopkinson, R. A. Hogg, D. J. Robbins, D. J. Mowbray, and M. S. Skolnick, "High-performance three-layer 1.3-μm InAs-GaAs quantum-dot lasers with very low continuous-wave room-temperature threshold currents," *Photonics Technology Letters, IEEE*, vol. 17, no. 6, pp. 1139-1141, Jun. 2005.

[29] M. Sugawara and M. Usami, "Quantum dot devices: Handling the heat," *Nature Photonics*, vol. 3, no. 1, pp. 30–31, 2009.

[30] H. Y. Liu, I. R. Sellers, T. J. Badcock, D. J. Mowbray, M. S. Skolnick, K. M. Groom, M. Gutiérrez, M. Hopkinson, J. S. Ng, J. P. R. David, and R. Beanland, "Improved performance of 1.3 μm multilayer InAs quantum-dot lasers using a high-growth-temperature GaAs spacer layer," *Applied Physics Letters*, vol. 85, no. 5, p. 704, 2004.

[31] M. Asada, Y. Miyamoto, and Y. Suematsu, "Gain and the threshold of three-dimensional quantum-box lasers," *Quantum Electronics, IEEE Journal of*, vol. 22, no. 9, pp. 1915-1921, Sep. 1986.

[32] R. Beanland, a. M. Sánchez, D. Childs, K. M. Groom, H. Y. Liu, D. J. Mowbray, and M. Hopkinson, "Structural analysis of life tested 1.3 μm quantum dot lasers," *Journal of Applied Physics*, vol. 103, no. 1, p. 014913, 2008.

[33] Z. Mi, J. Yang, P. Bhattacharya, and D. L. Huffaker, "Self-organised quantum dots as dislocation filters : the case of GaAs-based lasers on silicon," *Electronics Letters*, vol. 42, no. 2, pp. 1-2, 2006.

[34] Z. Mi, P. Bhattacharya, and J. Yang, "Room-temperature self-organised In0. 5Ga0. 5As quantum dot laser on silicon," *Electronics letters*, vol. 41, no. 13, pp. 742–744, 2005.

[35] Charles Kittel, Introduction to Solid State Physics (Wiley: New York, 2004).

[36] L. Pavesi, "Routes toward silicon-based lasers," *Materials Today*, vol. 8, no. 1, pp. 18-25, 2005.

[37] R. Mears, L. Reekie, I. Jauncey, and D. Payne, "Low-noise erbium-doped fibre amplifier operating at 1.54 μm," *Electronics Letters*, vol. 23, no. 19, pp. 1026-1028, 1987.

[38] S. Ramachandran and S. G. Bishop, “Excitation of Er3+ emission by host glass absorption in sputtered films of Er-doped Ge10As40Se25S25 glass,” *Applied Physics Letters*, vol. 73, no. 22, 1998.

[39] A. Polman, G. N. van den Hoven, J. S. Custer, J. H. Shin, R. Serna, and P. F. A. Alkemade, “Erbium in crystal silicon: Optical activation, excitation, and concentration limits,” *Journal of Applied Physics*, vol. 77, no. 3, 1995.

[40] F. Priolo, G. Franzò, S. Coffa, A. Polman, S. Libertino, R. Barklie, and D. Carey, “The erbium-impurity interaction and its effects on the 1.54 μm luminescence of Er3+ in crystalline silicon,” *Journal of Applied Physics*, vol. 78, no. 6, 1995.

[41] J. H. Shin, “Si nanocluster sensitization of Er-doped silica for optical amplet using top-pumping visible LEDs,” *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 12, no. 4, pp. 783-796, Jul. 2006.

[42] L. Pavesi, L. Dal Negro, C. Mazzoleni, G. Franzo, and F. Priolo, “Optical gain in silicon nanocrystals,” Nature, vol. 408, no. 6811, pp. 440–444, Nov. 2000.

[43] P. Fauchet, “Light emission from Si quantum dots,” *Materials Today*, vol. 8, no. 1, pp. 26-33, 2005.

[44] G. Franzò, F. Priolo, S. Coffa, A. Polman, and A. Carnera, “Room-temperature electroluminescence from Er-doped crystalline Si,” *Applied Physics Letters*, vol. 64, no. 17, p. 2235, 1994.

[45] F. Priolo, G. Franzò, S. Coffa, and A. Carnera, “Excitation and nonradiative deexcitation processes of Er in crystalline Si,” *Phyical Review. B*, vol. 57, no. 8, pp. 4443-4455, Feb. 1998.

[46] E. J. Woodbury, W. K. Ng, (November 1962). "Ruby laser operation in the near IR". Proceedings of the Institute of Radio Engineers 50 (11): 2367. doi:10.1109/JRPROC.1962.287964

[47] G. Eckhardt, R. W. Hellwarth, F. J. McClung, S. E. Schwarz, D. Weiner, E. J. Woodbury, (December 1962). "Stimulated Raman Scattering From Organic Liquids". *Physical Review Letters,* **9** (11): 455–457

[48] K. O. Hill, B. S. Kawasaki, D. C. Johnson, D. C. (1976), "Low-threshold cw Raman laser". *Applied Physics Letters.* **29** (3): 181–183.

[49] H. Rong, A. Liu, R. Jones, O. Cohen, D. Hak, R. Nicolaescu, A. Fang, and M. Paniccia, "An all-silicon Raman laser," *Nature*, vol. 433, no. 7023, pp. 292-294, Jan. 2005.

[50] J. Liu, X. Sun, D. Pan, X. Wang, L. C. Kimerling, T. L. Koch, and J. Michel, "Tensile-strained, n-type Ge as a gain medium for monolithic laser integration on Si.," *Optics express*, vol. 15, no. 18, pp. 11272-7, Sep. 2007.

[51] J. Liu, X. Sun, R. Camacho-Aguilera, L. C. Kimerling, and J. Michel, "Ge-on-Si laser operating at room temperature.," *Optics letters*, vol. 35, no. 5, pp. 679-81, Mar. 2010.

[52] R. N. Hall, G. E. Fenner, J. D. Kingsley, T. J. Soltys, and R. O. Carlson, "Coherent Light Emission From GaAs Junctions," *Physical Review Letters,* vol. 9, no. 9, pp. 366-368, Nov. 1962.

[53] C. Choi, R. Ai, and S. Barnett, "Suppression of three-dimensional island nucleation during GaAs growth on Si (100)," *Physical Review Letters*, vol. 67, no. 20, 1991.

[54] R. Fischer, W. Kopp, H. Morkoç, M. Pion, a. Specht, G. Burkhart, H. Appelman, D. McGougan, and R. Rice, "Low threshold laser operation at room temperature in GaAs/(Al,Ga)As structures grown directly on (100)Si," *Applied Physics Letters*, vol. 48, no. 20, p. 1360, 1986.

[55] R. Fischer, W. Masselink, J. Klem, T. Henderson, T. McGlinn, M. Klein, H. Morkoc, J. Mazur, and J. Washburn, "Growth and properties of GaAs/AlGaAs on nonpolar substrates using molecular beam epitaxy," *Journal of Applied Physics*, vol. 58, no. 1, pp. 374–381, Feb. 1985.

[56] H. Z. Chen, A. Ghaffari, H. Wang, H. Morkoç, and A. Yariv, "Low-threshold (~600 A/cm2 at room temperature) GaAs/AlGaAs lasers on Si (100)," *Applied Physics Letters*, vol. 51, no. 17, p. 1320, 1987.

[57] K. Tanabe, D. Guimard, D. Bordel, S. Iwamoto, and Y. Arakawa, "Electrically pumped 1.3 μm room-temperature InAs/GaAs quantum dot lasers on Si substrates by metal-mediated wafer bonding and layer transfer," *Optics Express*, vol. 18, no. 10, pp. 10604-10608, 2010.

[58] Y. B. Bolkhovityanov and O. P. Pchelyakov, "III-V Compounds-on-Si: Heterostructure Fabrication, Application and Prospects," *The Open Nanoscience Journal*, vol. 3, no. 1, pp. 20-33, Oct. 2009.

[59] U. Gosele, Y. Bluhm, G. Kastner, P. Kopperschmidt, G. Krauter, R. Scholz, A. Schumacher, S. Senz, Q.-Y. Tong, L.-J. Huang, Y.-L. Chao, and T.-H. Lee, "Fundamental issues in wafer bonding," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 17, no. 4. pp. 1145-1152, 1999.

[60] U. Gösele and Q. Tong, "Semiconductor wafer bonding," *Annual Review of Materials Science*, 1998.

[61] K. Tanabe, K. Watanabe, and Y. Arakawa, "III-V/Si hybrid photonic devices by direct fusion bonding.," *Scientific reports*, vol. 2, p. 349, Jan. 2012.

[62] A. Y. Liu, C. Zhang, J.Norman, A. Snyder, D. Lubyshev, J. M. Fastenau, A. W. K. Liu, A. C. Gossard, and J. E. Bowers, "High performance continuous wave 1.3 μm quantum dot lasers on silicon", *Applied Physics Letters, **104**, 041104 (2014)*

[63] J. R. Reboul, L. Cerutti, J. B. Rodriguez, P. Grech, and E. Tournié, "Continuous-wave operation above room temperature of GaSb-based laser diodes grown on Si," *Applied Physics Letters*, vol. 99, no. 12, p. 121113, 2011.

[64] J. Tatebayashi, A. Jallipalli, M. N. Kutty, S. Huang, K. Nunna, G. Balakrishnan, L. R. Dawson, and D. L. Huffaker, "Monolithically Integrated III-Sb-Based Laser Diodes Grown on Miscut Si Substrates," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 15, no. 3, pp. 716-723, 2009.

[65] T. Wang, H. Liu, A. Lee, F. Pozzi, and A. Seeds, "1.3-μm InAs/GaAs quantum-dot lasers monolithically grown on Si substrates," *Optics Express*, vol. 2936, no. 2003, pp. 2931-2936, 2011.

[66] H. Liu, T. Wang, Q. Jiang, R. Hogg, F. Tutu, F. Pozzi, and A. Seeds, "Long-wavelength InAs/GaAs quantum-dot laser diode monolithically grown on Ge substrate," *Nature Photonics*, vol. 5, no. 7, pp. 416-419, Jun. 2011.

[67] T. Wang, A. Lee, F. Tutu, A. Seeds, H. Liu, Q. Jiang, K. Groom, and R. Hogg, "The effect of growth temperature of GaAs nucleation layer on InAs/GaAs quantum dots monolithically grown on Ge substrates," *Applied Physics Letters*, vol. 100, no. 5, p. 052113, 2012.

[68] K. Morizane, "Antiphasedomain structures in GaP and GaAs epitaxial layers grown on Si and Ge," *Journal of Crystal Growth*, vol. 38, no. 2, pp. 249-254, 1977.

[69] R. Fischer, D. Neuman, H. Zabel, H. Morkoç, C. Choi, and N. Otsuka, "Dislocation reduction in epitaxial GaAs on Si(100)," *Applied Physics Letters*, vol. 48, no. 18, p. 1223, 1986.

[70] G. Balakrishnan, M. Mehta, M. N. Kutty, P. Patel, A. R. Albrecht, P. Rotella, S. Krishna, L. R. Dawson, and D. L. Huffaker, "Monolithically integrated III-Sb CW super-luminal light emitting diodes on non-miscut Si (100) substrates," *Electronics Letters*, vol. 43, no. 4, pp. 244–245, 2007.

[71] F. E. Ejeckam, M. Seaford, Y. Lo, H. Hou, B.Hammons, "Dislocation-free InSb grown on GaAs compliant universal substrates", Applied Physics Letters, 71, 776-778 (1997)

[72] M. Seaford,P. Hesse, D. Tomich, K. Eyink, "Strain relief by surface undulations of dislocation free MBE grown antimonides on compliant universal GaAs substrates" *Journal of Electronic Materials,* 28(7), 878–880 LA, 1999

[73] L. Cerutti, J. B. Rodriguez, and E. Tournie, "GaSb-Based Laser , Monolithically Grown on Silicon Substrate , Emitting at 1 . 55 μm at Room Temperature," *Photonics Technology Letters, IEEE*, vol. 22, no. 8, pp. 553-555, 2010.

[74] J. B. Rodriguez, L. Cerutti, P. Grech, and E. Tournié, "Room-temperature operation of a 2.25 μm electrically pumped laser fabricated on a silicon substrate," *Applied Physics Letters*, vol. 94, no. 6, p. 061124, 2009.

[75] J. Yang and P. Bhattacharya, "Monolithic Integration of InGaAs – GaAs Quantum-Dot Laser and Quantum-Well Electroabsorption Modulator on Silicon," *Photonics Technology Letters, IEEE*, vol. 19, no. 10, pp. 747-749, 2007.

[76] P. Bhattacharya and J. Yang, "Groove-coupled InGaAs/GaAs quantum dot laser/waveguide on silicon," *Lightwave Technology, Journal of*, vol. 25, no. 7, pp. 1826-1831, 2007.

[77] G. Brammertz, M. Caymax, M. Meuris, and M. Heyns, "GaAs on Ge for CMOS," *Thin solid films*, vol. 517, no. 1, pp. 148-151, Nov. 2008.

[78] G. Brammertz, Y. Mols, S. Degroote, V. Motsnyi, M. Leys, G. Borghs, and M. Caymax, "Low-temperature photoluminescence study of thin epitaxial GaAs films on Ge substrates," *Journal of Applied Physics*, vol. 99, no. 9, pp. 93514-935110, May 2006.

Chapter 2: Experimental methods

2.1 Introduction

This chapter outlines the experimental work associated with this project. Firstly a description of molecular beam epitaxial growth and the advantages of using it. The characterisation and device fabrication techniques used in this work is further discussed. All samples in this thesis have been grown using a Veeco Gen930 molecular beam epitaxy (MBE) system at the Department of Electronic and Electrical Engineering, UCL. The laser fabrication and processing were done in the London Centre for Nanotechnology, UCL. All materials and devices were characterised at the department of Electronic and Electrical Engineering at UCL unless otherwise stated.

2.2 Molecular beam epitaxy

Epitaxial growth is a process of a crystal grown on an existing crystalline substrate due to deposition of new material [1]. Epitaxial growth has been studied for at least 150 years. However the beginnings of a physical description emerged in the 1920's. An important milestone was the coining of the term "epitaxy" by Royer [2] in 1920. The word epitaxy is a combination of the Greek words "epi" and "taxis" meaning "upon" and "order" respectively. This distinguished epitaxial growth from polycrystalline and amorphous growth. An important feature of epitaxial growth is that the new crystal formed has the same orientation as the original crystalline substrate whereas this is not the case in polycrystalline and amorphous growth.

There are now numerous different facilities for performing epitaxial growth. MBE was developed at Bell labs in the late 1960's by Alfred Cho and John Arthur; having been inspired by work performed by Bruce Joyce at the Allan Clark research centre [3-5]. The advantage of MBE over other growth techniques is the possibility of low growth rates, (< 1 ML per second [6]). This means that growth thicknesses can be carefully and accurately controlled. It also has the advantage that *in situ* measurements of the growth are very straightforward and requires very little specialised equipment. A common *in situ* tool used in MBE growth is the reflection high-energy electron diffraction (RHEED) system, which allows properties of epitaxial growth layers to be determined and monitored whilst the growth is happening.

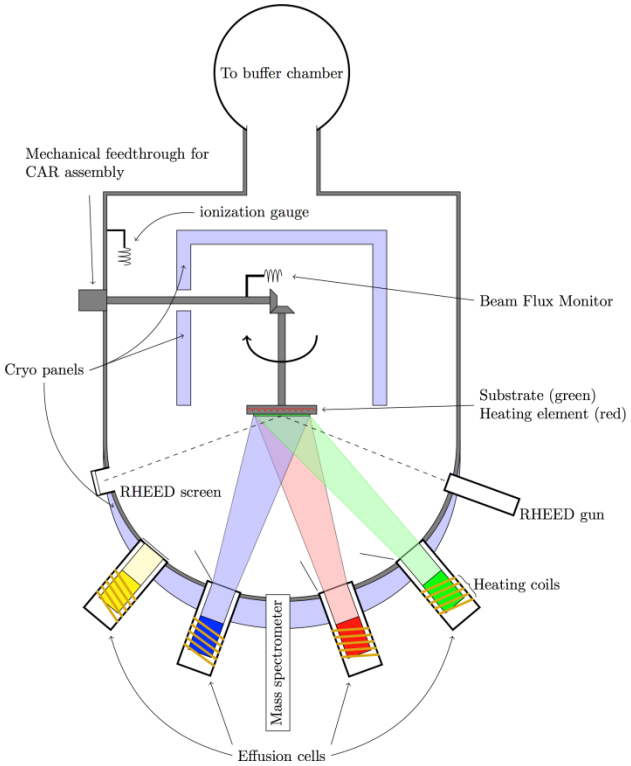


Figure 2.1. Schematic of MBE chamber. *Reprinted with permission from [7]. Creative Commons License*

2.2.1 Process mechanics

In a basic interpretation of MBE, a two-step process is carried out in an ultra-high vacuum (UHV) [1]. In the first step, atoms or simple homo-atomic molecules (such as atomic Ga and As_2 or As_4 for GaAs) are evaporated from solid sources (known as Knudsen cells) then collimated into beams and directed towards a heated substrate.

The substrate is rotated to ensure uniformity of growth. The atoms in the beams have do not interact with each other, hence being known as a beam, and deposit onto the surface in a ballistic process known as molecular flow.. An example of a typical MBE chamber is shown in Figure 2.1. In the second step, the deposited species must migrate on the surface prior to incorporation into the growing material. In this manner the morphology of the film is determined. This depends on numerous factors such as the deposition rates, surface temperature of the substrate and crystallographic orientation. These factors must be optimised for different structures on different substrates, and also different conditions of the chamber.

2.2.2 In situ monitoring

The main advantage for MBE growth over other growth techniques is that not only *in situ* measurements can be performed, but also these measurements can be made during the growth. A ubiquitous technique in MBE growth for monitoring growth is the RHEED system [8]. This works by directing a high-energy beam of electrons (10-20 keV) at a glancing angle (~0.5° – 3.0°) at the surface. The electrons only penetrate a few layers into the surface, and the electrons that emerge are displayed on a phosphorescent screen, giving details about the surface morphology of the substrate. There are three main reasons why RHEED is such a commonly used technique:

1. It is a very easy technique to set up. The only things that are required are an electron gun and a screen.
2. Due to its geometry it is straightforward to set up so that it does not interfere with the molecular beams from the Knudsen cells.
3. It can be used not only *in situ* but also whilst the growth is happening, giving a real time indication of how the growth is progressing.

The main limitation of RHEED is that it only shows a diffraction pattern from the substrate and does not give an image of the substrate. Additionally because the process involves multiple scattering events, there is no way to perform a Fourier transform on the pattern to show an image of the surface. Nevertheless there are several details that can be determined about the growth from the RHEED pattern. The crystallographic symmetry can be inferred from the symmetry of the diffraction pattern. The sharpness of the pattern can be used to find the long-range order in growth and whether the growth is in 3D or 2D form.

Finally one of the most powerful and useful techniques of RHEED is accomplished by observing the intensity of the specular beam (equal incidence and reflected angles) over time. This allows the amount of material deposited to be accurately measured in real time. The specular beam intensity typically takes the form of a sinusoid, which decays over time. As material is deposited the surface becomes rougher, once more than half of the layer has been deposited, further growth will result in the surface becoming smoother and therefore will result in an increasing intensity, a schematic of this process is shown in Figure 2.2.

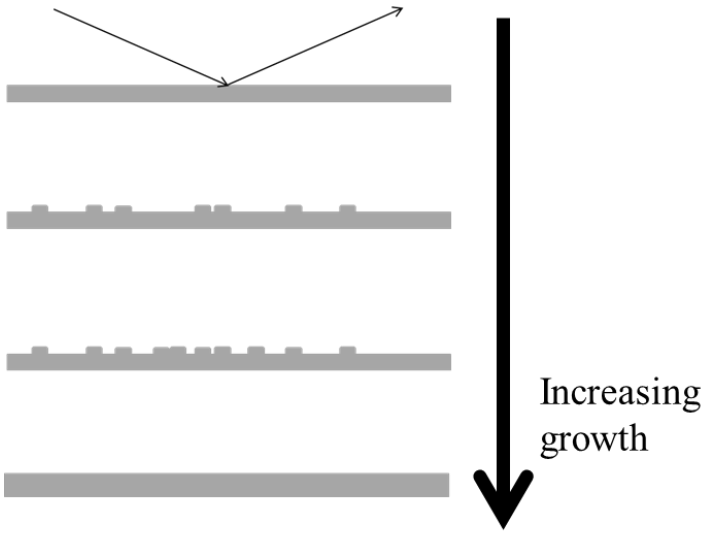


Figure 2.2. Growth of material on substrate leads to reduction then increase in specular intensity as the surface becomes rougher then smooth again.

In Figure 2.2 the growth is layer-by-layer, i.e. that the material is grown in single layers of material of one atom (or molecule) thick, known as a monolayer (ML). Figure 2.3 shows the shape of a typical trace observed. The intensity decays because the ideal case of layer-by-layer growth is not realised. In real systems one layer will start to be grown before the other has finished, so the intensity will never return to the original full amount. The period of the oscillations can be used to determine how long one layer (i.e. a lay one atom or molecule thick, known as a monolayer or 1 ML) takes to grow. It is possible to control growth amounts to within fractions of one ML as long as the shutter speed is faster than the speed to grow one layer. As growth speeds tend to be slow in MBE (typical growth rates can be ~ 1 ML/s), it is

not difficult to obtain a shutter speed faster than the time to grow one layer (shutter speeds can be less than 200 ms [9]).

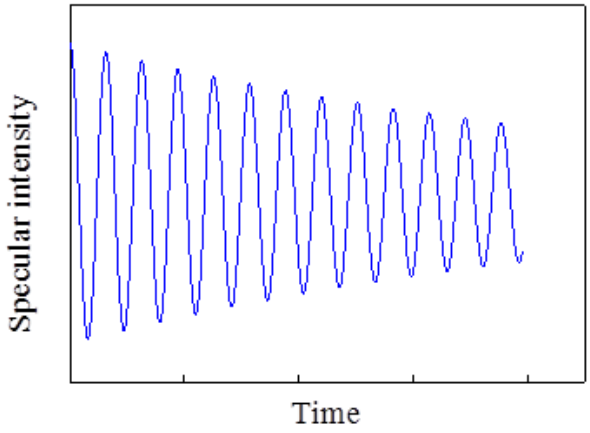


Figure 2.3. Schematic of specular intensity over time. Intensity decreases then results in maximum after one layer of material is grown. The period shows the amount of time for one complete layer to be deposited, which can be used to deposit accurate amounts of growth material.

Method	Materials	Sources	Delivery
MBE	III-V, IV	Elemental	Molecular
MOMBE	III-V	Metal-organic(III), Elemental(V)	Molecular
CBE	III-V	Metal-organic(III), Hydride, Organo-substituted Hydride(V)	Molecular
GSMBE	IV	Hydride, Chloride, Chloro-hydride	Molecular
MOVPE	III-V	Metal-organic(III), Hydride, Organo-substituted Hydride(V)	Hydrodynanmic
VPE	IV	Hydride, Chloride, Chloro-hydride	Hydrodynanmic

Table 2.1 Epitaxial growth techniques [1].

2.2.3 Other epitaxial techniques

There are alternatives to MBE growth, all with their relative merits. A list of techniques is given in Table 2.1. One alternative to the use of molecular flow is to

use hydrodynamic transport from gas sources such as chemical vapour deposition (CVD), which is also known as vapour phase epitaxy (VPE). The growth of III-V compounds uses metal-organic compounds known as precursors and therefore the growth by CVD of III-V compounds is known as metal-organic vapour phase epitaxy (MOVPE) or MOCVD. One of the advantages of MOVPE is that it can be performed without the use of an ultrahigh vacuum, and therefore does not require liquid nitrogen cooling, whereas in comparison liquid nitrogen must be used in an MBE system. Another practical advantage of MOVPE is that when cells are depleted it is more straightforward to replace them as in MBE, when the cell will runs out of material, the chamber must be opened in order to refill the cell. This is an added nuisance as once the chamber is opened it must be heated to high temperatures (known as baking) to reach UHV. However this needs to be considered against the added danger of MOVPE as the gasses used are often toxic.

The main advantage of MBE over MOVPE, especially in research, is the ease of *in situ* diagnostic techniques, whereas MOVPE can only use optical techniques. This means that a large amount of detail can be found out about the growth method, and also the growth thicknesses in MBE can be controlled much more finely than in CVD.

2.3 Characterisation techniques

Characterisation is the way to discover the optical, electrical and structural properties of the substrates after MBE growth. These techniques are used throughout all stages of device design, growth and fabrication process. Atomic force microscopy (AFM) and photoluminescence (PL) studies are used to give a quick indication of the quality of MBE growth as these are straightforward techniques that can be performed at the same day that the substrate is grown. Transmission electron microscopy (TEM) is less straightforward than PL and AFM, as the subsrate requires processing in order to perform measurements. However taking TEM images is useful as it can confirm the results of AFM and PL and to gain useful insights about the crystal growth and any defects such as threading dislocations in the wafer. Once the lasers were fabricated, current-voltage (IV), power – current (LI) and spectra measurements were taken.

2.3.1 Atomic force microscopy

To understand AFM, it is first helpful to give some details on a similar technique known as scanning tunnelling microscopy (STM) [10]. A STM uses an atomically sharp tip a few angstroms above the surface of the sample being imaged. This produces a tunnelling current between the tip and the surface. The scans can have a vertical resolution of ~0.1 Å and a lateral resolution of ~1.0 Å. Scans taken at constant current measure contours of constant Fermi–levels, where the Fermi level is directly related to the charge density of an atom. A STM is only sensitive to charge density of a surface rather than atomic positions. This is a limitation as it means that it can only be used to measure a conducting sample. AFM however can be used to measure the surface profile of insulators and conducting materials [10].

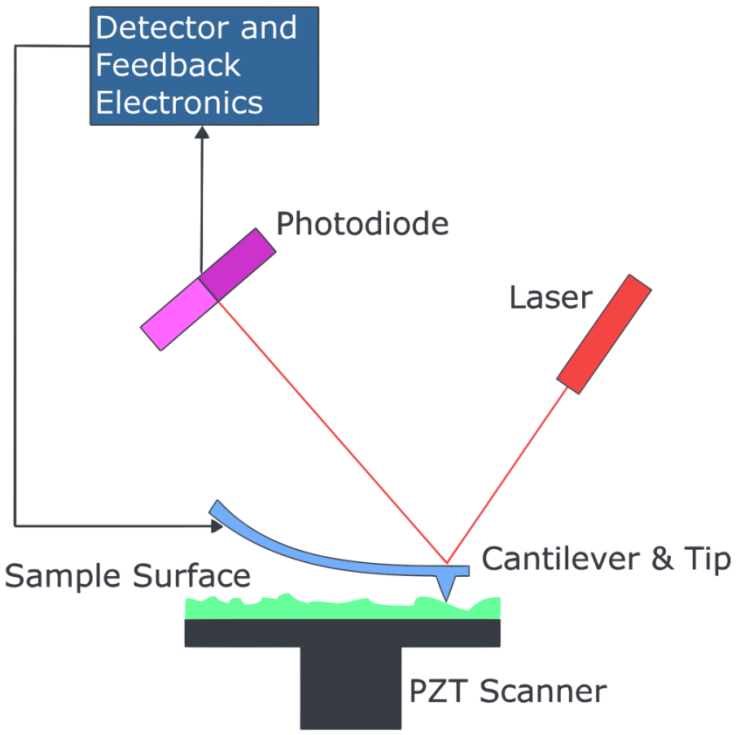


Figure 2.4. Block diagram of typical AFM. The laser and photodiode are used to measure the deflection of the cantilever. *Reprinted with permission.*

In order to manufacture an AFM a STM tip could be mounted on a cantilever. When the tip is brought close to the surface, a force of the same magnitude of inter-atomic forces would be acted upon the tip causing it to deflect. By using a laser and photodiode along with a feedback mechanism, the position of the tip can be detected. Figure 2.4 shows a basic schematic of an AFM system. The tip could be scanned along the surface by keeping the force acting on the cantilever at a constant level.

This would give a measure of the profile of the surface. AFM has some advantages over STM. In particular, the STM relies on a tunnelling current it is sensitive to the electron density of states near the Fermi level which means that in order for STM to work the density of states is required to be non-zero, i.e. the sample must be a conductor. In comparison an AFM feels a force from all electrons, therefore the sample does not need to be a conductor. Another advantage of AFM over STM is that in STM the tip must be within a few angstroms of the surface, whereas this is not the case for AFM. This is because tunnelling currents fall off very quickly with an exponential relationship. An AFM can operate close to the surface (contact mode), or far away from the surface (non-contact mode, ~50-150 Å from the surface). This means that AFM can be used to image nano-scaled-structures which may be damaged or altered due to being put in close proximity to a tip, such as quantum dots, which if the tip is too close could be easily moved or damaged. Furthermore, as high resolution is typically harder to obtain from AFM than STM, it means that AFM is often used to study large areas, up to microns. This is particularly useful in the study of the morphology of QDs as it means that the quality of the growth can be determined by looking at the QDs in multiple small areas on a wafer. A typical (1 μm x 1 μm) image obtained from an AFM is shown in Figure 2.5.

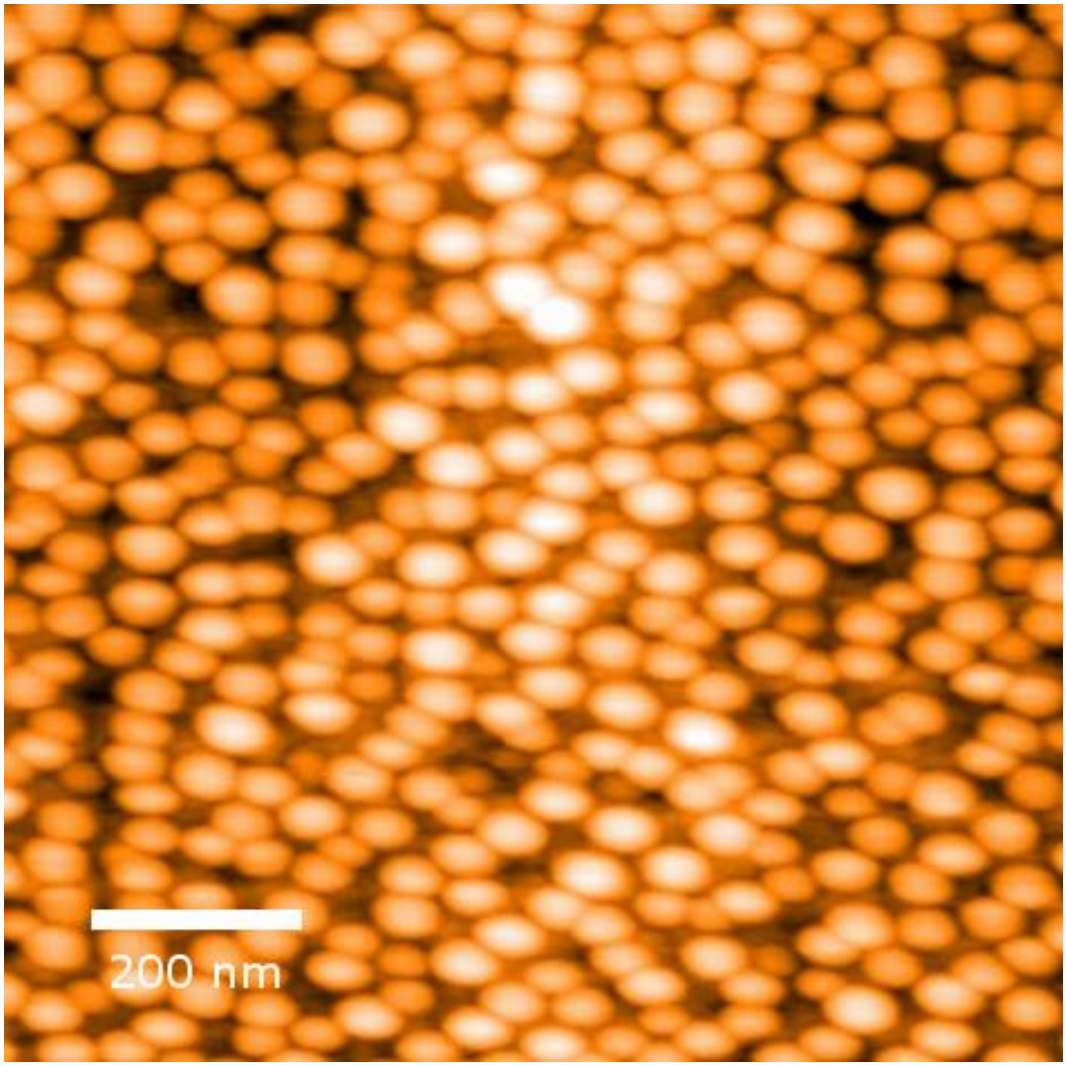


Figure 2.5. AFM 1 μm x 1 μm image of InAs QDs on a Ge-on-Si substrate.

2.3.2 Photoluminescence

Photoluminescence (PL) is the spontaneous emission of light from material under optical excitation [11]. PL characterisation is a useful method to determine material properties, as it is a non-destructive technique. PL spectra can be used to find the transition energies of a sample, therefore it is a convenient technique to characterise lasers active layers. The PL intensity will depend on the density of photo-excited electrons, and so in order to control this, the beam intensity can be controlled. In order to probe the active layers of a sample, the sample should be left uncapped as the penetration of light in semiconductor typically has a penetration depth of ~ 1 μm. This means that PL characterisation is done using test structures where the growth has been stopped after the QD in the active layer.

The PL setup in this work consisted of a green laser, cryostat, and monochromator with a Si detector as seen in Figure 2.6. This enables measurements to be performed from room temperature down to a minimum of 10 K. PL measurements were performed in a closed-cycle He cryostat under 532 nm excitation from a diode-pumped solid-state laser. The laser wavelength was chosen for flexibility in testing different material systems. The PL spectrum was dispersed by a 0.25-m monochromator and detected by a TE-cooled Ge detector. Temperature dependent PL measurements were taken from 10 to 300 K at a laser power of 30 mW.

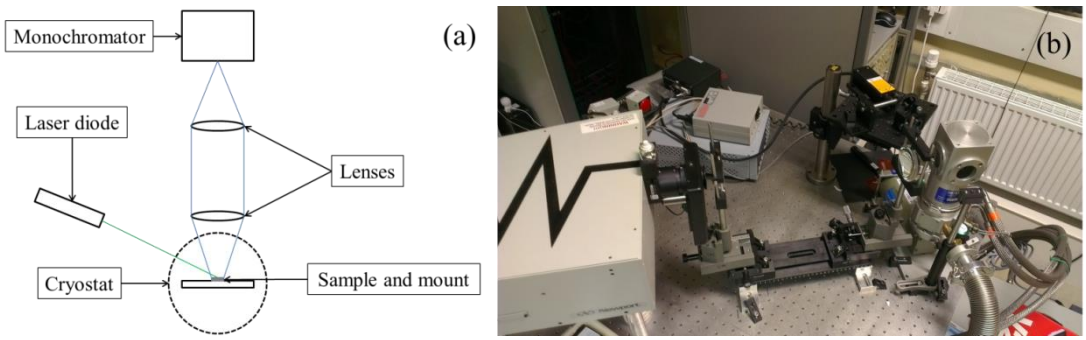


Figure 2.6. (a) Shows schematic of PL measurement set-up. (b) shows an image of PL set-up.

2.3.3 Transmission electron microscopy

Transmission electron microscopy (TEM) is a technique to image a sample using a beam of electrons, which are passed through an extremely thin sample (~100 nm) [12]. These electrons interact with the sample and via this interaction an image is formed. This image can be magnified and detected using a CCD camera. The main advantage of TEM over light microscopes is that electrons have a smaller de Broglie wavelength than photons and therefore can image much smaller features than optical microscopes. The most recent resolution that was reported was by resolving a crystal spacing of less than 50 pm [13]. TEM measurements were performed at the University of Warwick.

2.3.4 Laser characterisation

Once the lasers were cleaved, their optical properties were characterised by taking power-current measurements (LI), current- voltage (IV) measurements and by taking spectra above and below threshold.

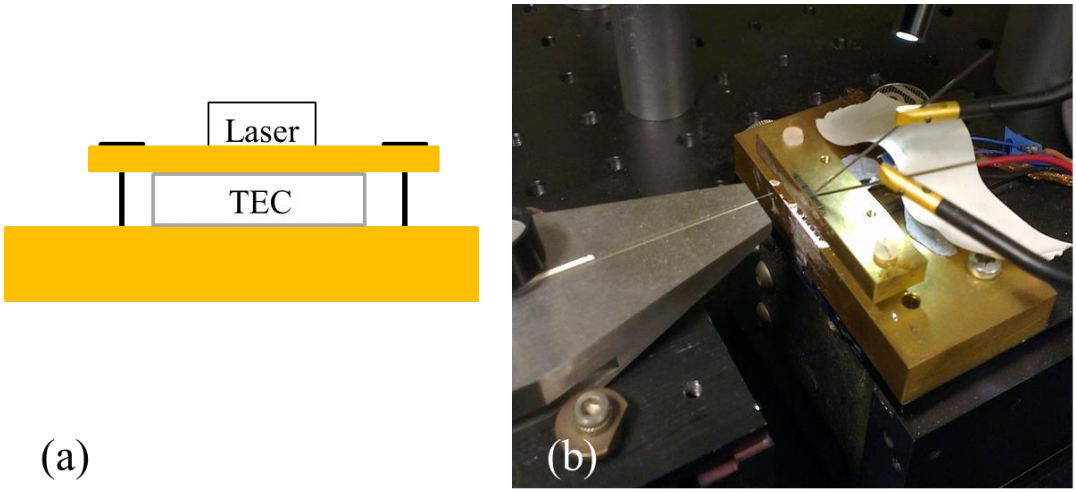


Figure 2.7. (a) shows diagram of experimental setup. It consists of two brass blocks with a TEC (thermoelectric controller) between to control the temperature. The upper brass block is kept in position by two plastic screws. The laser emission can be measured either using a photodetector or by injecting into a fibre connected to a spectrum analyser. (b) shows a photo of this setup with a laser probed and fibre in position. The fibre mount could be replaced by a mount for the photodetector. The laser-under-testing can be either simply placed on the heatsink or if CW measurements are being taken it can be soldered to a heatsink and screwed in place.

The lasers were initially probed directly onto the contacts without any wire bonding as shown in Figure 2.7. The laser was placed on a brass heat sink with a thermoelectric cooling (TEC) controller as shown in Figure 2.7(a). This could vary the temperature in the rage of ~10-100 °C. The temperature sensor was mounted inside the heat-sink. Two current sources were available. A pulsed ILX Lightwave 3545B laser diode controller and a Keithley Series 2400 source measure unit for CW measurements. The pulsed source could operate with duty cycles from 0.01 % to 10 %; pulse widths of 0.1 μs up to 10 μs; and currents up to 3 A. By varying the temperature of the heat-sink estimates of T_0 could be made, as the threshold current is expected to vary proportional to $\exp\left(\frac{T}{T_0}\right)$. A photodetector with as large as possible area was used in order to detect as much power emitted from the laser as possible. Spectra measurements were taken by aligning a cleaved fibre to a cleaved facet and then using a spectrum analyser to measure the spectra of the lasers above and below thresholds. To measure the series resistance of the lasers a Keithely four-point-probe was used. Labview programs were written to control the instruments used in characterisation to speed up the measurements and ensure accuracy.

2.4 Device fabrication

Following MBE growth the substrates were moved to the LCN cleanroom for device fabrication. This involved six main stages, including cleaning, optical lithography, etching, metallisation, lapping and cleaving [14]. The process of the laser fabrication procedure can be explained in simplified manner by looking at Figure 2.8. The process flow is as follows:

1. Etch ridges and contact pits
2. Deposit SiO_2 using plasma-enhanced chemical vapour deposition
3. Open contact windows (for both n and p-type contacts)
4. n and p-type metallisation.
5. Anneal sample in rapid thermal processor (RTP)
6. Sample lapping
7. Cleaving of laser bars
8. Laser mounting and wire bonding

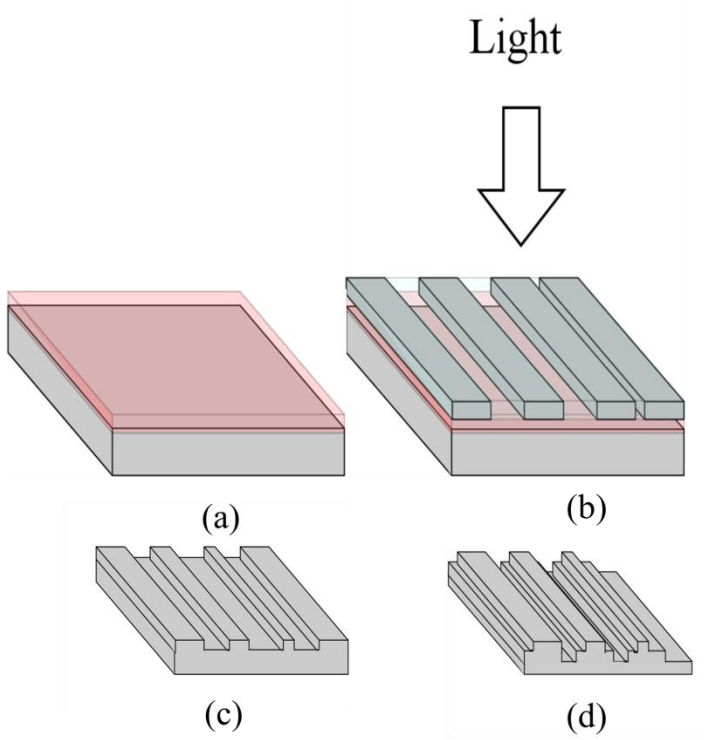


Figure 2.8. Simplified process for top contact laser fabrication as some steps are omitted. (a) shows S1818 resist being spun on sample. (b) shows the mask alignment and subsequent exposure. (c) shows ridges after etching and (d) shows sample after the lower contacts have been etched. The remaining steps would be to deposit silicon oxide, then open the contact window for n and p-type metals and evaporate the contacts.

2.4.1 Cleaning

Substrate cleanliness is a critical aspect in III-V processing, as particles on the surface can cause defects during the fabrication process. Even a small amount of contaminant can have a significant detrimental effect on many processes of fabrication such as metal adhesion, resist application, patterning and wet etching. Therefore care is needed in order to prevent any contamination and to ensure that the same level of cleanliness in the process is kept from start to finish. Organic solvents, typically acetone and iso-propanol (IPA), are used to clean the samples as they will not react with the III-V substrates or metals used.

After the substrates were grown in the MBE chamber, they were stored in the cleanroom until needed. Once the fabrication was started, the wafers were first cleaved, by scribing with a diamond pen into a sample approximately 20 mm x 20 mm depending on the size of the wafer. The cleaved piece was then soaked in acetone then IPA. The IPA dissolves the acetone which ensures that there is no residue from the acetone left on the sample. Then the sample was put into a beaker of acetone and placed into an ultrasonic water-bath for two minutes to remove any small particles from the sample surface, then repeated using IPA. After this step the sample was cleaned with a cotton bud soaked in acetone and then rinsed with IPA. This further ensured that any contaminants were removed from the surface. After this stage the sample was checked under a microscope. This cleaning stage was repeated until there are no particle observed under a microscope.

2.4.2 Photolithography

Photolithography is a technique used in order to pattern wafers. Energy sensitive compounds, known as photoresist can be applied to the substrate by spin coating. When selected areas are exposed the area either becomes soluble (known as a positive resist) or insoluble (negative resist) to the developer. The resist can be exposed using a variety of techniques, such as light (photolithography), electron beams (E-beam lithography) and x-rays (x-ray lithography). In this work only positive photolithography was used.

After the sample was thoroughly cleaned Shipley S1818 resist was deposited using a pipette and the sample spun at 4,000 rpm. This leads to a resist thickness of approximately 1.8 μm, which can be checked after exposure using a profilometer. The sample was then baked on a hot plate for 60s at 115 °C which dries the

photoresist by evaporating the solvent in the resist. At this stage the resist was checked under a microscope to ensure that there were no bubbles in the resist, which could lead to voids.

Edge effects

Problems can arise due to using small samples instead of whole wafers. When photoresist is spun there is a build-up of resist at the edges of the substrate. To counteract this effect substrates have a lip on the edge to ensure that the spun photoresist is not thicker on the edges. However, once the wafer is cleaved into pieces this is no longer the case. One technique is to use a cotton bud soaked in acetone to remove the photoresist on the very edge of the sample after baking. However, this is far from ideal, as fumes of acetone can lead to damage of the photoresist not on the edge, and also this technique reduces the amount of usable area on the surface. Therefore the technique used in this thesis involved placing the sample on a square blue tape of area slightly larger than the sample. This blue tape had a slightly adhesive surface, which ensured that the sample did not come off the chuck when spun, but not too much so that the sample would be damaged when being removed from the tape. This tape was then put on a ¼ inch chuck and the sample covered, over the edges, with photoresist. This was found to greatly reduce the size of any edge effects. The sample was then removed from the tape before being placed on the hot plate.

Mask alignment and exposure

A Karl Suss MJB3 mask aligner was used to align the substrate to the mask and expose the photoresist. First the mask plate was cleaned by rinsing in acetone and IPA then mounted on the mask aligner. The sample was aligned and then put into hard contact and exposed at 50 mJ using a UV-lamp. Developing was carried out using a solution of Microposit MF-26A developer for 45s. Figure 2.9 shows a developed feature; these are used to test the quality of the exposure and development. If overdeveloped then the gaps between the lines will disappear and if underdeveloped the gaps will be too large. After this the sample was then hard baked before wet etching. This ensures that the photoresist itself is not etched by the etching reagent.

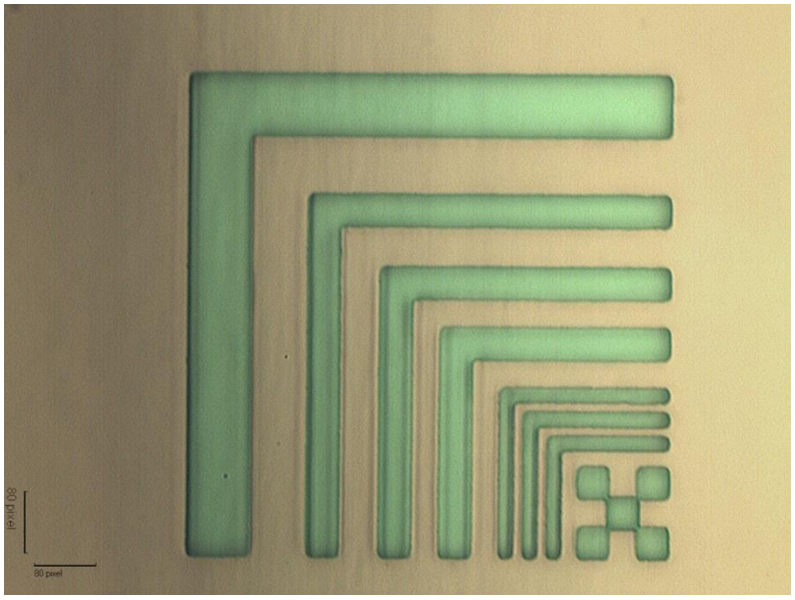


Figure 2.9. Example exposure for S1818 photoresist. Marks here are used to determine if the photoresist has been properly exposed and developed.

Lift-off resist procedure

Lift-off is the process used to make metal contacts on substrate. When depositing metal, the result is a film which covers the entire surface. The lift-off allows the metal in the unwanted areas to be removed. A lift-off resist procedure relies on there being an undercut between two layers of resist. This allows all of the resist to be removed as the solvent used to remove the resist (known as 1165) can get under the resist. If this wasn't the case, the resist would be covered by the evaporated metal. Figure 2.10(a) shows the two layers of resist having been spun. The first is LOR10B, which is then baked for 10 minutes. Then S1818 is spun and baked. LOR10B develops faster than S1818 and is not photosensitive. After exposure (at 50 mJ) and development using MF-316 the lower layer of resist will develop faster leaving an undercut as shown in Figure 2.10(b). Ideally this undercut should be approximately a micron, as the larger the undercut then smaller the resolution of the resultant metal contact pattern. After the metal is evaporated the resist can be removed with a standard solution of 1165 and IPA with the before and after stages being shown in Figure 2.10(c) and (d) respectively.

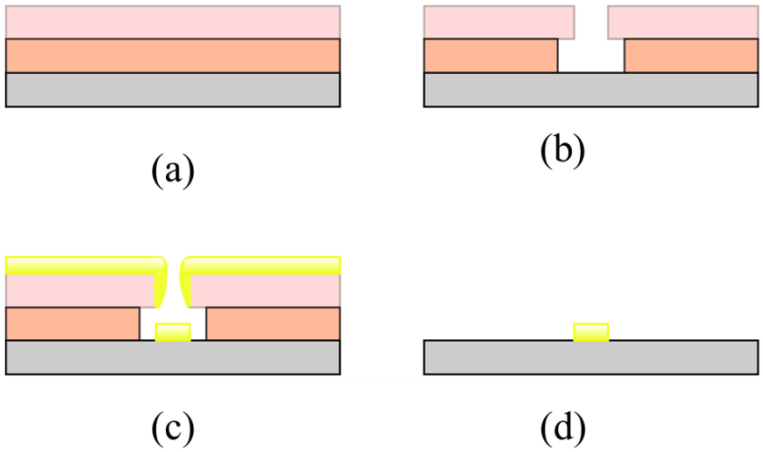


Figure 2.10. Diagrammatic explanation of LOR process. (a) shows the sample after LOR10B and S1818 resists have been spun. (b) shows the resist after exposure and development. As LOR10B is removed faster than S1818 an undercut is formed. (c) shows the sample after metal evaporation. Note that the undercut will allow solvent to attack and remove the resist. (d) shows the ideal result after the resists are removed.

Figure 2.11(a) shows a sample after exposure and development and in the figure you can see a border around the exposed areas. This is because you are looking down through the first layer of resist and you can see the edge of the LOR10B. Figure 2.11(b) shows the same sample after metal evaporation and lift-off.

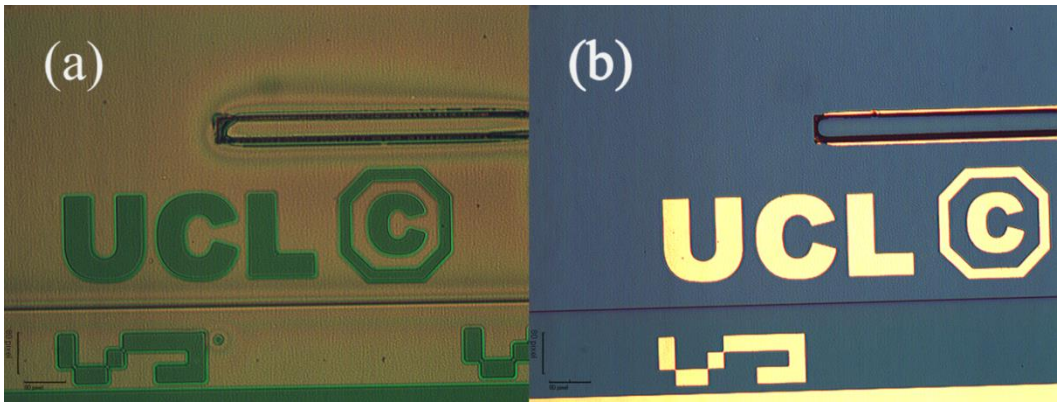


Figure 2.11. (a) shows sample before evaporation and (b) shows sample after evaporation and resist removal.

2.4.3 Metallisation

Metal contacts can be classified by two different types: Ohmic and rectifying (Schottky) contacts. The purpose of an Ohmic contact is to allow current to flow in or out of a semiconductor. Ideally the contact would have a linear I-V relationship, be stable over time and add as little parasitic resistance as possible. When a metal is brought into contact with a semiconductor the valence and conduction bands of the semiconductor will bend, so that the Fermi levels of the metal and semiconductor

equalise [14]. However surface states of semiconductors such as GaAs tend to pin the Fermi level and therefore it is the surface states that typically has a larger effect on barrier height than the metal work function. To conduct electrons through the interface the carriers must be able to pass through the barrier. There are two possible mechanisms for electrons to travel through the barrier:

1. Thermionic emission, where an electron has a high enough thermal energy to pass the barrier.
2. Field emission, where, if the barrier is sufficiently narrow, an electron can tunnel through even if it has less energy than the barrier height.

The current density due to thermionic emission, J, can be expressed as [15]

$$J = J_s \, exp\left(\frac{qV}{kT}\right), for \; V \gg kT/q \qquad \text{Equation 2.1}$$

where T is the absolute temperature, q the electron charge, voltage applied across the barrier and k is Boltzmann's constant. Doping of the semiconductor will decrease the width of the barrier and therefore enable tunnelling. The current density for field emission can be expressed as

$$J \approx \exp\left(-\frac{q\phi_b}{E_\infty}\right)$$

where

$$\mathrm{E}_\infty = \frac{\mathrm{q}\hbar}{2}\sqrt{\frac{\mathrm{N}}{\epsilon \mathrm{m}^*}} \qquad \text{Equation 2.2}$$

N is the doping concentration and m^* is the electron effective mass. Therefore the field emission current will increase with the square root of doping concentration. This means that high doping is required to obtain Ohmic contacts.

2.4.4 Etching

Etching is the removal of material from the substrate. It can be classified in two types: wet and dry etching. Wet etching is the use of liquid etching to remove material [14]. Dry etching makes use of plasma-driven processes. Dry etching in many ways is superior to wet etching as it can offer greater control over parameters, for example dry etching offers anisotropic etching resulting in very vertical sidewalls. This has the effect that the undercutting of mask patterns can be almost negligible. However, the main disadvantage is the complexity of the factors that

must be optimised for successfully controlled etching. For example in wet etching only the choice of chemicals, concentrations and temperature need to be optimised to obtain a certain etch rate and profile. Whereas for dry etching the results are extremely dependent on many parameters such as, gas type, gas flow rate, gas delivery position, pressure, electrode geometry, power density, radio frequency, wafer temperature and wafer material.

In this thesis, only wet etching was used due to the limits on time that could be spent on optimisation of the dry etching, although in the future dry etching could be used to obtain better quality ridge walls and narrower ridges.

Different combinations of compounds can be used to obtain different etch rates. In this thesis, two different combinations of etchants were used to etch III-V based compounds (GaAs and AlGaAs). Originally a solution of 1:1:x H_3PO_4:H_2O_2:H_2O was used where x was 3, 5 and 10. It was found that this led to a selective etch, and therefore the etch rate was difficult to determine. Due to this fact the etching solution was changed to Adachi etchant, which is known to be a non-selective etchant for III-V materials. Adachi is a combination of 1:1:1 of H_2O : K2Cr2O7 : HBr : $C_2H_4O_2$. Therefore the etch rate could be more carefully controlled.

First the sample was etched for 30s, and then measured using a DektakXT profileometer. In order to ensure that the sample was etched at the same rate across the whole sample five points were measured each time as in Figure 2.12. An average would be taken and used to work out the etch rate. The etch rate has to be recalculated each time as the etch rate will depend on the conditions of the cleanroom such as the room temperature. Once the etch rate is calculated, this can be used to determine the required time to complete the etching processes, taking the sample out a few times to check that the rate remains constant. Once the desired etch depth is achieved the photoresist can be removed.

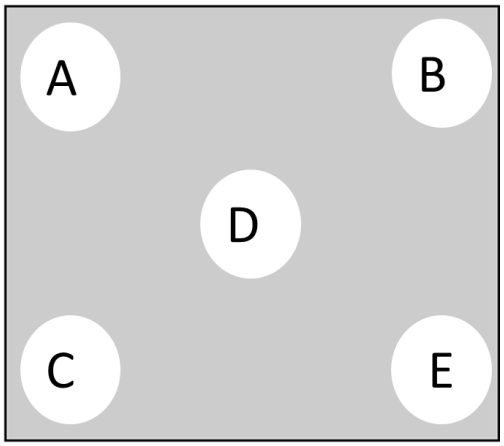


Figure 2.12. Etch depth was measured on five points after each etch to ensure that etch rate was consistent over entire wafer.

For etching of SiO_2 a solution of buffered oxide etch (BOE) was used. This consists of 6:1 by volume ratio of 40% NH_4F to 49% HF in water. The etch rate of this solution is approximately 2 nm/s at 25 °C. The approximate etch time was found by etching a test sample which had been deposited at the same time as the laser samples, and measured using an ellipsometer.

2.4.5 Backend processes

After the samples are annealed, they are taken out of the cleanroom for thinning and cleaving. An example of what such a completed device looks like is given in Figure 2.13.

Figure 2.13. Device with all metal and SiO_2 deposited.

Lapping

Lapping is a process to reduce the thickness of the substrate. There are numerous techniques to do this. In this work, it is done by using an aluminium oxide powder of size 10 and 3 μm suspended in water. The 10-μm powder is used to get close to required thickness and then the 3-μm powder is used to refine the surface, making it smoother. The sample was mounted onto a brass circular block using crystal bond, which is a wax that melts at ~150 °C and is acetone soluble. Therefore the substrate can be easily removed once it was thinned. The samples were then thinned to less than 200 μm. This is in order to make the process of cleaving lasers easier, and it also improves the thermal performance of devices.

After the sample is thinned, Cr/Au or Al/Au depending on the doping of the substrate is evaporated on the back of the substrate. In this work both p-doped and n-doped bulk substrates were used. This is to improve the thermal conductivity between the Si and gold plated heat sink, or if the lasers are bonded, the solder.

Cleaving

A crucial part of the process is the cleaving, as this will determine whether the laser has good or bad facets and the threshold current is dependent on the mirror quality. Cleaving was performed using a Karl Suss RA120 scriber. The scriber is used to make a short scribe in the place where the cleave is desired. Then pressure is placed either side of the cleave with the cleave over the point of a razorblade. Then the process is repeated for the other facet. Typically lasers of length from 1 mm to 5 mm are cleaved. 1mm is approximately the limit that is possible to cleave using this method, as for cavities shorter than 1mm it is difficult to evenly put pressure on both sides at same time. In this fabrication process the lasers are left as-cleaved. Devices that were found to have good performance were wire bonded.

2.5 Conclusion

The advantages of MBE over other techniques were discussed, in regard to the capability to perform in situ measurements, allowing very accurate information about the growth to be understood and hence accurate details on thicknesses grown known. Also the characterisation techniques were discussed. Finally the device fabrication process used in this thesis was reviewed in detail.

2.6 References

[1] K. Barnham and D. Vvedensky, "Low-Dimensional Semiconductor Structures: Fundamentals and Device Applications". Cambridge University Press, 2008.

[2] L. Royer, "Experimental research on parallel growth on mutual orientation of crystals of different species," Bull. Soc. Fr. Mineral, vol. 51, pp. 7-159, 1928.[3] A. Cho, "Molecular beam epitaxy". American Institute of Physics, 1994.

[4] B. A. Joyce and R. R. Bradley, "A study of nucleation in chemically grown epitaxial silicon films using molecular beam techniques I.—experimental methods," Philosophical Magazine, vol. 14, no. 128, pp. 289-299, 1966.

[5] B. A. Joyce, R. R. Bradley, and G. R. Booker, "A study of nucleation in chemically grown epitaxial silicon films using molecular beam techniques III. Nucleation rate measurements and the effect of oxygen on initial growth behaviour," Philosophical Magazine, vol. 15, no. 138, pp. 1167-1187, 1967.

[6] P. Frigeri, L. Seravalli, G. Trevisi, S. Franchi, "Molecular Beam Epitaxy: An Overview", Comprehensive Semiconductor Science and Technology, 2011, Pages 480–522

[7] "GFDL (http://www.gnu.org/copyleft/fdl.html)], via Wikimedia Commons." .

[8] P. K. Larsen and P. J. Dobson, Reflection high-energy electron diffraction and reflection electron imaging of surfaces. Plenum Press, 1988.

[9] http://www.mbe-komponenten.de/products/mbe-components/shutter/rsm.php

[10] Peter Eaton, Paul West, "Atomic Force Microscopy", OUP Oxford, 25 Mar 2010

[11] T. Gfroerer, "Photoluminescence in analysis of surfaces and interfaces," Encyclopedia of Analytical Chemistry, pp. 9209-9231, 2006.

[12] L. Reimer and H. Kohl, "Transmission Electron Microscopy: Physics of Image Formation". Springer, 2008.

[13] R. Erni, M. Rossell, C. Kisielowski, and U. Dahmen, "Atomic-Resolution Imaging with a Sub-50-pm Electron Probe," Physical Review Letters, vol. 102, no. 9, p. 096101, Mar. 2009.

[14] R. Williams, "Modern GaAs processing methods". Artech House, 1990.

[15] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices. John Wiley & Sons, 2006.

Chapter 3: Metal contact optimisation

3.1 Introduction

This chapter describes the optimisation of metallisation procedure of the lasers fabricated in this thesis on GaAs substrates. This was an ongoing task and improvements were constantly being made, so that not all methods outlined in this chapter were used in device fabrication in chapters 4 and 5 due to the day-to-day practicalities of the cleanroom at UCL. Lasers were also fabricated on Ge substrates to further compare fabrication methods.

3.2 Testing of metal contacts

Both the choice of metals for the contact, and the deposition method will have an effect on the performance of laser diodes fabricated. When fabricating a diode, poor IV characteristics, such as a high turn-on voltage or high series resistance, can be caused by a variety of factors. If a normal device is fabricated with standard contacts, it can be hard to determine exactly where the high resistance is originating from. For example, it could be due to a high resistance in the material or due to a poor electrical contact between the metal and semiconductor. The transmission line model (TLM) is a useful technique to estimate the contact resistance and the resistance between the contact and the substrate [1].

A TLM pattern, which can be seen in Figure 3.1, consists of equal sized squares of metal, spaced at intervals which double, at 20, 40, 80 and 160 μm. The area around the rectangle of the TLM patterns was etched away so that current could not spread

outside of this area. If this was not done then the measured resistivity would appear higher as the current would be travelling through a larger area than in the calculation.

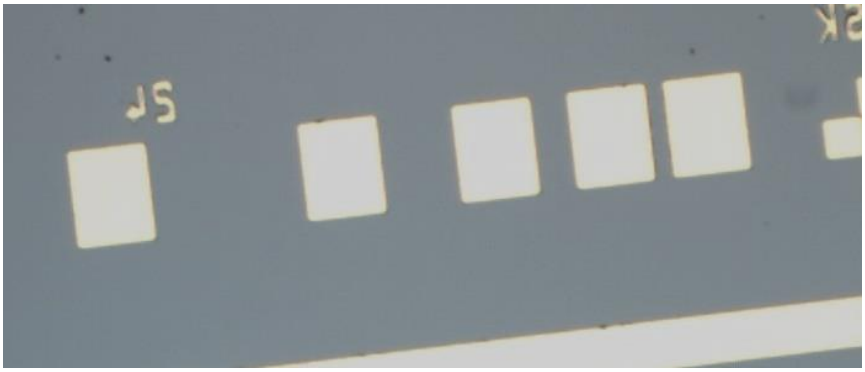


Figure 3.1. Standard TLM pattern used to obtain resistivity of contacts with no etching around pattern.

The choice of metal for contacts depends on whether it is p or n-type contacts. There is a variety of metals, and metal alloys used for metallization. Typically a Au layer is evaporated for the last step in order to have a good surface with a low resistance for wire bonding or direct probing [2]. The contact resistivity not only depends upon the metals used, but also on the doping of the test substrate.

3.2.1 Contacts for n-type GaAs

The first metal that was used as a contact for n-type GaAs was Sn [3], however the introduction of Ni/AuGe contact for a eutectic composition of 88-12 Au-Ge (wt%) and Ni overlayer has become by far the most popular method of n-type contacts [4]. However, as AuGe has a eutectic temperature of 361 °C it is prone to "balling-up", the use of a Ni wetting layer has been cited as a method to avoid this [2]. Balling-up makes the contact unsuitable for small-area devices, and an example of this is shown in Figure 3.2. Further studies have shown that Ni does not only prevent the "balling-up" problem, but also can assist in other areas, such as reduction of surface oxides and reacting with GaAs at low temperatures to form binary and ternary compounds that may be electrically important [5,6]. It is also possible that some of these compounds may assist with the incorporation of Ge as a dopant [5]. The contact

resistivty has been observed to follow an inverse relationship with the level of doping [7].

The Ni/AuGe contact is not without fault though, as it has spiking, poor controllability, poor edge definition, and inadequate thermal stability for many applications. A method around this is to use a rapid thermal annealer (RTA, also known as a rapid thermal processor RTP) and to properly optimise the amount of Ni in the contact [2].

There are alternatives to using Ni/AuGe, for example: methods using solid phase regrowth such as Pd/Ge [8], Si/Pd [9], Pd/In/Pd [10], and Pd/In/Pd/Ge/Pd [11]; or Au/Pt/Ge [12] . In this work Ni/AuGe was chosen as the metal for the n-type contact because of the established success of using Ni/AuGe and due to the high cost, limited availability and more complicated evaporation techniques for other metals.

The metal contacts were deposited using thermal evaporation in an Edwards E306 diffusion pump bell jar evaporator. The metal evaporated consisted of 4 layers. The first was a thin layer of Ni, which acted as an adhesion layer between the GaAs and Au/Ge alloy. Then a layer of Au/Ge alloy was evaporated and followed by another layer of Ni. A thick layer of gold was finally deposited.

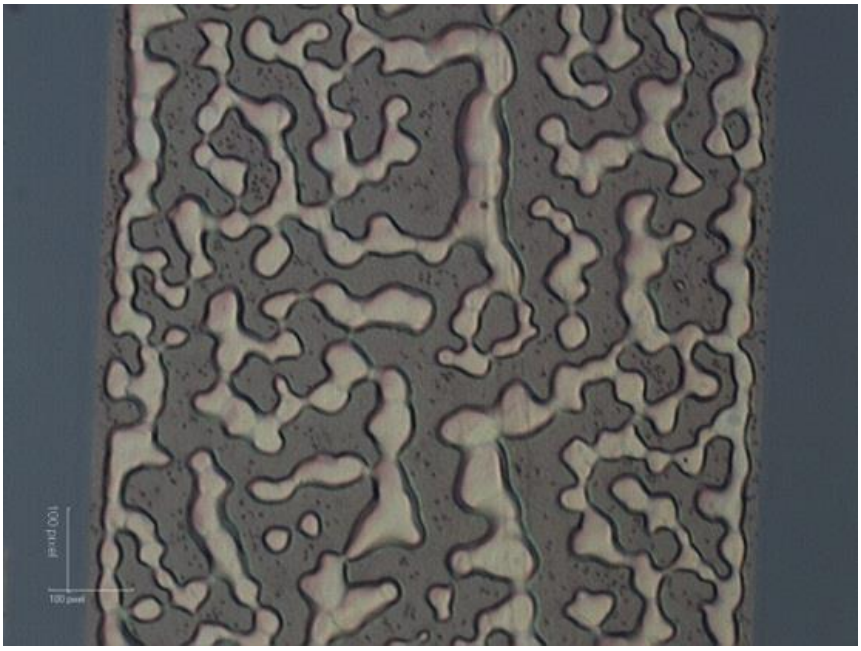


Figure 3.2. Example of Ge “balling up” in Ni/GeAu/Ni/Contacts

First the amounts of Ni and GeAu were optimised in the first three layers. The amounts of metal in the Ni/GeAu/Ni/Au system which were tried were 5/50/x/300

nm where *x* was tried at *x* = 5, 25 , 35 and 50 nm. It was found that *x* = 25nm led the lowest contact resistances, with the higher amounts of Ni leading to contacts which were not mechanically stable enough to be bonded. GeAu thicknesses of above 50 nm was also found to lead to poor mechanical stability of contacts.

Figure 3.3 shows that the lowest resistivity after annealing at 420 °C for 7s is 4.22 × 10^{-6} Ωcm^2. Therefore this amount of metal was used when using n-type contacts on GaAs. In order to obtain a more accurate measurement of the contact resistance, a four-point probe setup was used. In a four-point probe measurement, the current is passed through two of the probes and the voltage is measured through the two remaining probes. As the voltage probes have a very high resistance compared to the resistance of the sample under testing no current will pass through the probes, meaning that the internal resistance of the measuring system will not be measured. When the sample annealed at 420 °C was re-measured the resistivity was found to be 1 x 10^{-6} Ωcm^{-2}.

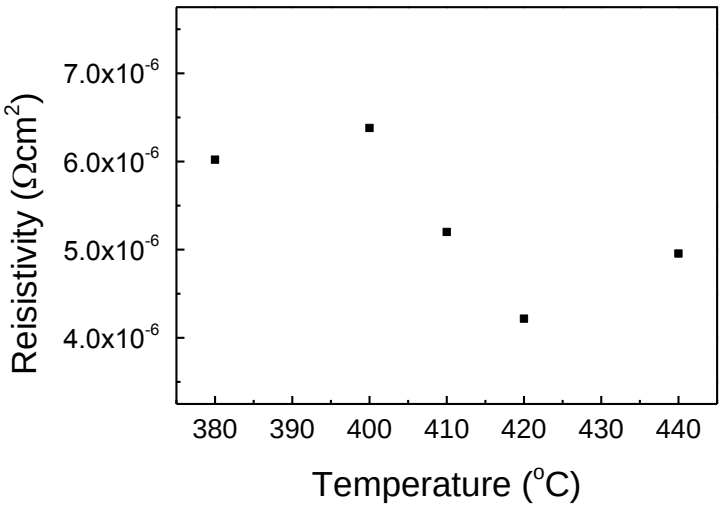


Figure 3.3. Annealing temperatures versus resultant resistivities for Ni/GeAu/Ni/Au. It was found that 420 °C for 7s in a RTP led to the lowest resistance.

3.2.2 Contacts for p-type GaAs

The same considerations for contacts to n-type GaAs also apply for contacts to p-type GaAs. Common metalizations for p-type GaAs are Au/Zn/Au [13] Au/Be [14], and Au/Pt/Ti [15]. The addition of Pt for III-V devices has been shown to act as a

barrier to prevent Au migrating into the GaAs material, causing the degradation in the device performance [16]. Conventionally Ti was used as the first layer, and then a layer of Pt was used between the Au and Ti layers [17]. Further research led to the use of a quaternary layer contact; consisting of Pt/Ti/Pt/Au [18].

Other metals such as Si/Ni/Mg/Ni [19], W/Ni/InMg/Ni [20], and Pd/Sb/Mn/Pd [21] can be used. A detailed review of metal contacts to p-type contacts can be found in [22]

Again, with regard to the availabitly of materials in the clearnorrom, not all metals were tested. Cr/Au, Ti/Au, Ti/Pt/Au, Pt/Ti/Pt/Au and Au/Zn/Au metals were all tested for the p-type metal on GaAs. It was found that the best results were obtained using Au/Zn/Au. At 380 °C the resistivity was found to be 7.44×10^{-5} as shown in Figure 3.4.

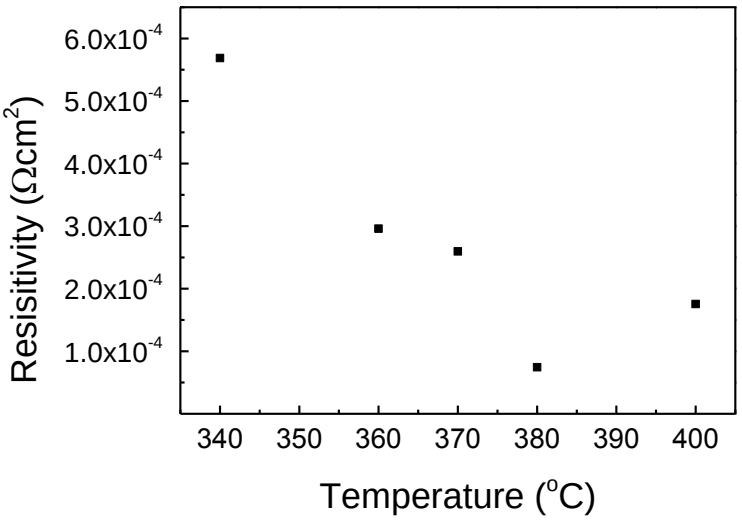


Figure 3.4 Annealing temperatures versus resultant resistivities for Au/Zn/Au. It was found that 380 °C for 7s in a RTP led to the lowest resistance.

Limitations of zinc-containing contacts

Zinc is a difficult metal to use in a cleanroom because it has a low vapour pressure so can easily outgas when not being evaporated [2]. This means that it can damage pumps and also contaminate other evaporations. Therefore, zinc is often confined to a separate evaporator. However, due to a lack of a spare evaporator for the majority of the work in this thesis, any metal combinations containing zinc were avoided even though zinc based contacts would have led to lower resistances and hence better devices. In this section, the alternative choices of Ti/Au contacts or a

combination of Ti/Au and Pt are compared. Also E-beam evaporation and sputtering is compared for deposition of metal contacts.

E-beam and sputter deposition

Typical resistivities for Ti containing recipes were of order 1 $\times 10^{-4}\ \Omega cm^2$. Figure 3.5 shows two TLM patterns on p-doped GaAs annealed at 420 °C. It shows that there is a small difference between the use of the E-beam evaporator and sputtered Ti/Au. E-beam evaporation led to a contact resistivity of 1.1 $\times 10^{-4}\ \Omega cm^{-1}$ whereas sputtered Ti/Au led to a resistivity of 9.4 $\times 10^{-5}\ \Omega cm^{-1}$, which is marginally lower.

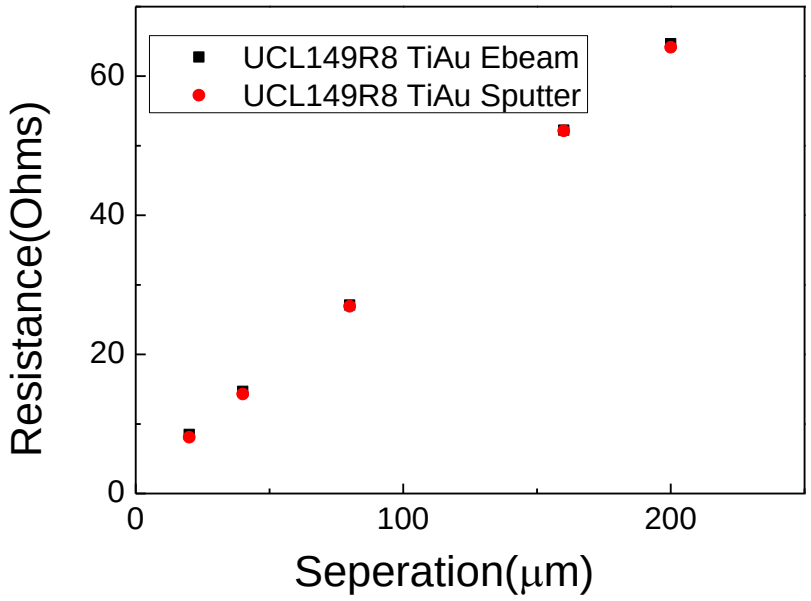


Figure 3.5. TLM pattern comparison for TiAu evaporated in E-beam evaporator versus sputtered Ti/Au.

This is unsurprising, as a large difference would not be expected for the same metals, unless there was a contamination problem with the evaporator. However, even a small difference will be useful as if a large amount of small reductions can be made, this can lead to a large total reduction.

Platinum containing contacts

In this work variations of Ti/Pt/Au and Pt/Ti/Pt/Au were tested and compared to Ti/Au using E-beam evaporation. Sputtered tests were not performed due to the lack of a Pt target. Figure 3.6 shows TLM pattern plots for the three metal

combinations. It was found that Ti/Pt/Au had the lowest resistivity at 8.9 $\times 10^{-5}$ Ωcm^{-1} compared to 1.1 $\times 10^{-4}$ Ωcm^{-1} for Ti/Au and 1.2 $\times 10^{-4}$ Ωcm^{-1} for Pt/Ti/Pt/Au. However, although the contact resistivity is higher for Pt/Ti/Pt/Au than Ti/Pt/Au, it was found that lasers fabricated with the same parameters except for the choice of p-type contact performed better with a Pt/Ti/Pt/Au contact than Ti/Pt/Au contact. Figure 3.8 shows CW LI and VI plots for 50-μm devices fabricated with a Ti/Pt/Au contact. Figure 3.8 also shows the same plot for lasers fabricated with a Pt/Ti/Pt/Au contact. It can be noted that the Pt/Ti/Pt/Au contact provides lasers with significantly lower threshold currents (150 mA compared to 100 mA for 50 μm wide devices). Additionally the use of a Pt/Ti/Pt/Au contact enabled the CW lasing of a 25-μm wide device which had not worked for the Ti/Pt/Au device. This shows the potential of Pt/Ti/Pt/Au as contact material. In future work Pt/Ti/Pt/Au could be sputtered to achieve higher results still. This was not tested in this thesis due to a lack of a platinum source for the sputterer.

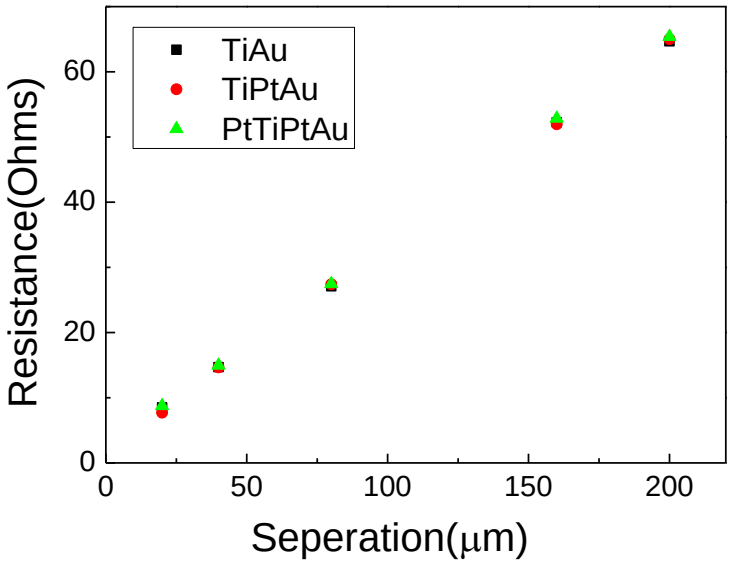


Figure 3.6. TLM patterns for Ti/Au, Ti/Pt/Au and Pt/Ti/Pt/Au for deposition by E-beam.

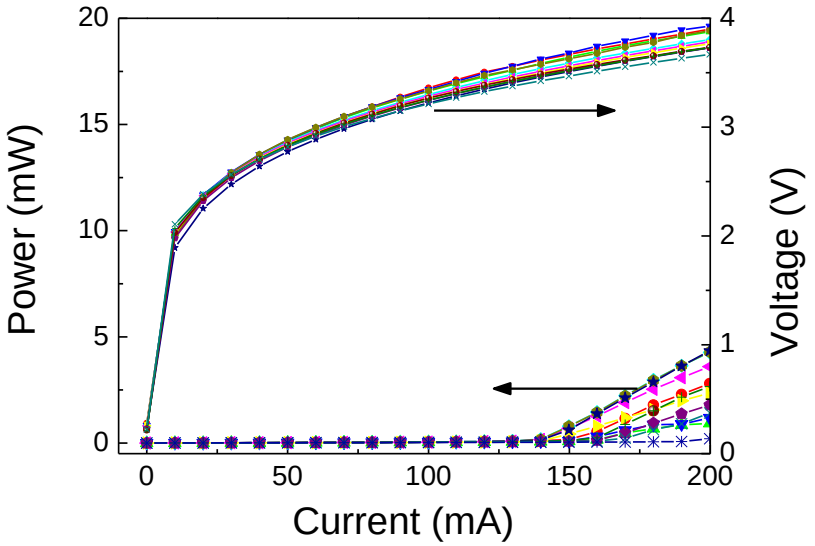


Figure 3.7. CW LI and IV for lasers on GaAs (2mm cavity length, 50 μm width) using Ti/Pt/Au as p-type contact. Threshold current ~150 mA.

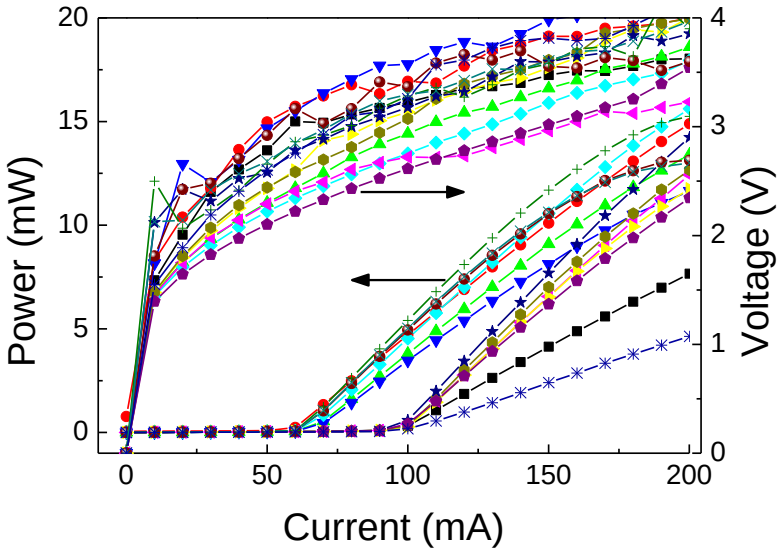


Figure 3.8. CW LI and IV for lasers on GaAs (2mm cavity length, 50 μm and 25 μm widths) using Pt/Ti/Pt/Au as p-type contact. Threshold currents ~100 mA for 50 μm device and ~ 60 mA for 25 μm device. The kinks in some of the IV plots could be due to poor connections between the probe and contact surface.

To test that the fabrication process was properly optimised, laser structures using an InAs/GaAs DWELL structure were grown on GaAs substrates. The same structure had previously been used to achieve record low CW threshold currents at 17 A/cm^2 for a 2 mm x 8 μm device; with a high-reflectivity coating on both facets and peak

power over 100 mW [23]. Broad area lasers with a 50-μm cavity width were fabricated. Two different metal alloys were used for the p-type contacts; Ti/Pt/Au and Au/Zn/Au were tested for the p-type contact. Ni/Ge/Au was used for the n-type contact on both substrates. The lasers were cleaved to 2-mm cavity length and the facets left as-cleaved.

Au/Zn/Au compared to Ti/Pt/Au

Figure 3.9 shows that the CW threshold current when using Au/Zn/Au as the p-type contact is 70 mA. In comparison, when using Ti/Pt/Au the threshold current is increased to 140 mA. This is also lower than the equivalent sized device for Pt/Ti/Pt/Au contacts in Figure 3.8. The turn on voltage when using Au/Zn/Au is lower than when using Ti/Pt/Au, 1.76 V compared to 2.76 V. In addition the series resistance is slightly lower for the Au/Zn/Au p-type contact (5.42 Ω versus 5.72 Ω).

These results confirm that Au/Zn/Au is a better choice for contact material than Ti/Pt/Au as all parameters are improved due to its use and this improvement cannot be ascribed to any other factors as the lasers were fabricated at the same time with the same structure. Further tests of the laser with Au/Zn/Au p-type contacts were performed at high temperatures. In Figure 3.10 it can be seen that the lasers operated in CW mode up to 35 °C but at 40 °C were no longer lasing. In pulsed operation (1% duty cycle, 5 μs pulse width) the lasers were capable of lasing up to 70 °C as seen in Figure 3.11. The same tests were performed using the laser with a Ti/Pt/Au p-type contact are shown in Figure 3.12. The device operated until 55 °C, where the device failed. This is likely to be catostprophic optical damage (COD) [24]. This is where the power density of the semiconducotr junction has been overloaded, and the junctiion has melted and facet recrystalised. This explains why the power has spiked then dropped. COD is a primary faliure mode in semiconductor lasers.

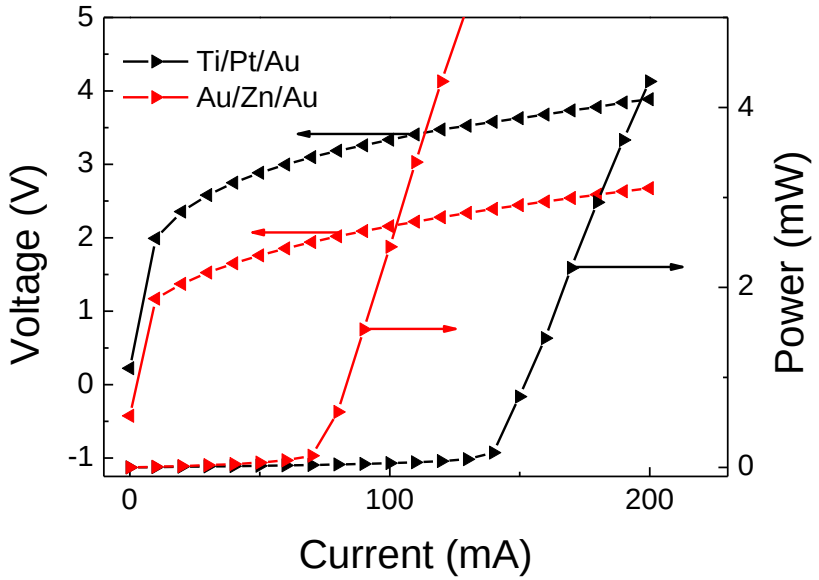


Figure 3.9. CW Power and voltage versus current for 2mm 50 µm lasers on GaAs substrates. Red points show use of Au/Zn/Au as a p-type contact and black points use Ti/Pt/Au as a p-type metal.

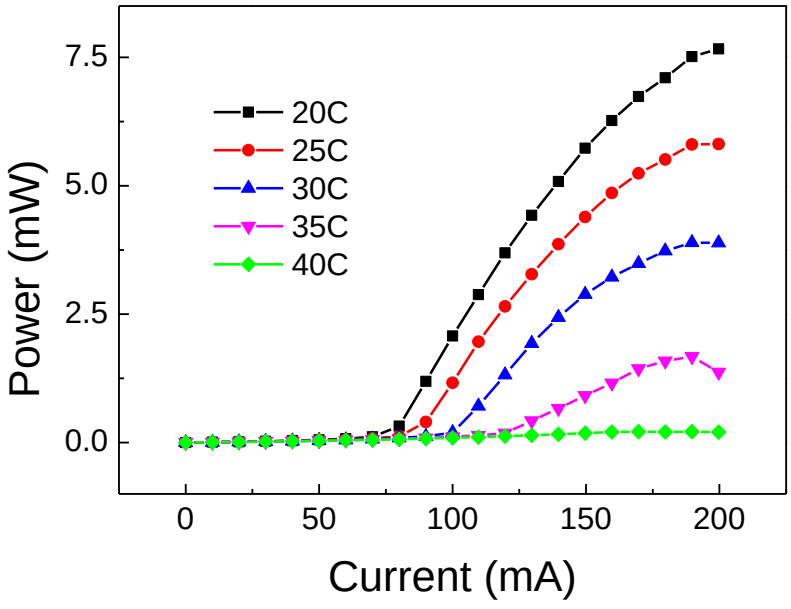


Figure 3.10. CW temperature performance for 2 mm lasers on GaAs with a 50 µm width using Au/Zn/Au as the p-type contact. Lasing was observed up to 35 °C.

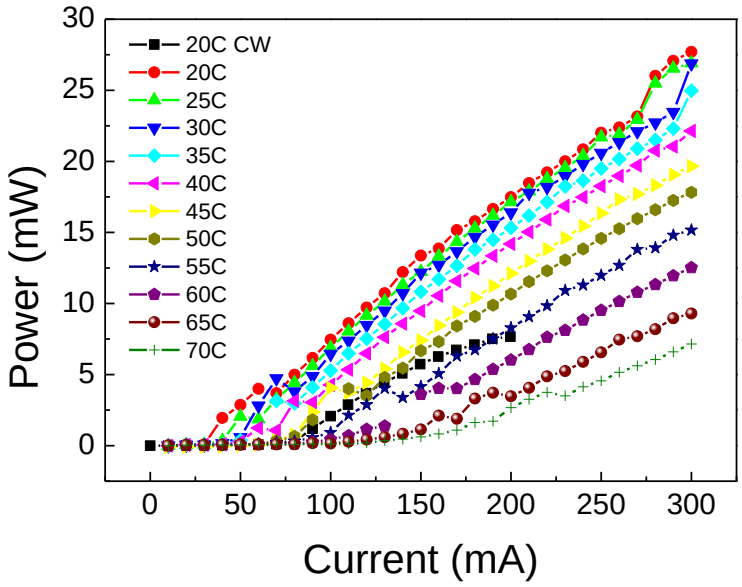


Figure 3.11. Pulsed temperature performance for 2 mm lasers on GaAs with a 50 µm width using Au/Zn/Au as the p-type contact. The shift in power is probably due to the characteristics of the power meter when shifting between ranges of the power meter.

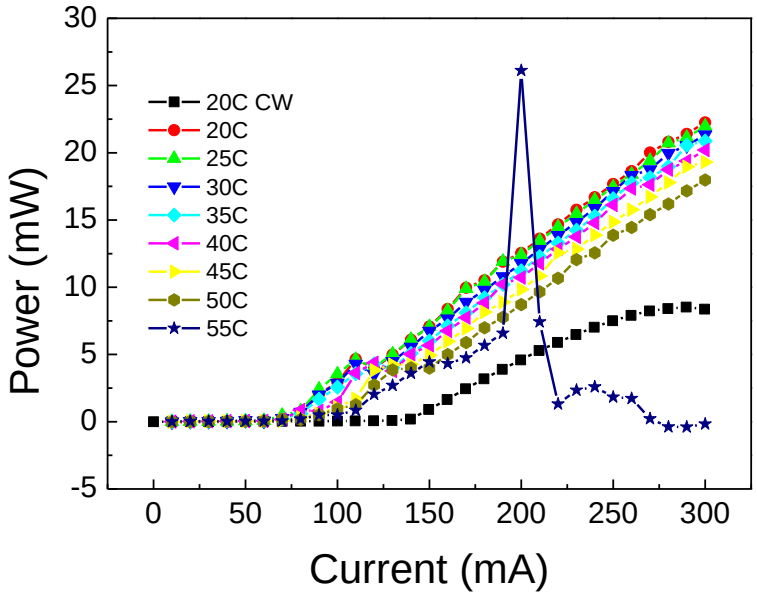


Figure 3.12. Pulsed temperature performance for 2 mm lasers on GaAs with a 50 µm width using Ti/Pt/Au as the p-type contact. At 55 °C COD occurs and the diode is "blown".

The difference in performance of the pulsed and CW lasers could be explained in the following manner. Any heat created in the device needs to be dissipated through the heatsink. However as the laser is not bonded to the heatsink, the result is that the

thermal conductivity between the device and the heatsink will be high because there is an air-gap between the laser and the surface of the heatsink. This means that heat cannot be efficiently transferred away from the laser. Also the fact that the lasers are directly probed onto to the contact pad will also lead to heating at the contact. The probe tips are small, so this can lead to very high current densities and temperatures near the tip. During the testing, the damage of metal has been observed. This makes it necessary to re-probe the laser in a new place.

3.3 Wire bonding

Two techniques that could be used to improve the temperature performance of the lasers once the lasers are fabricated and cleaved into devices: wire bonding and die bonding [2]. The lasers can be die bonded to the heat sink using an In/Ag solder. This will improve the thermal conductivity between the laser and the heatsink. Without the solder there is an air barrier between the laser and heat sink and therefore a high thermal resistance. The second technique is wire bonding. Figure 3.13 shows a schematic diagram of how laser bars are bonded to a bond pad. The bond pad consists of a ceramic tile, which is electrically insulating. This allows the gold pad for the laser substrate contact and bond pads to be electrically isolated. A gold wire is attached onto the laser contact and bonded to an external Au pad. The wire is bonded into place by heating induced by an ultrasonic tip. This has the advantage that the probe will not directly contact the laser contact. Therefore, any heating from the tip will not be transferred into the laser. Here a wedge bonder is used to add Au wires to the laser contacts, and pads for probing.

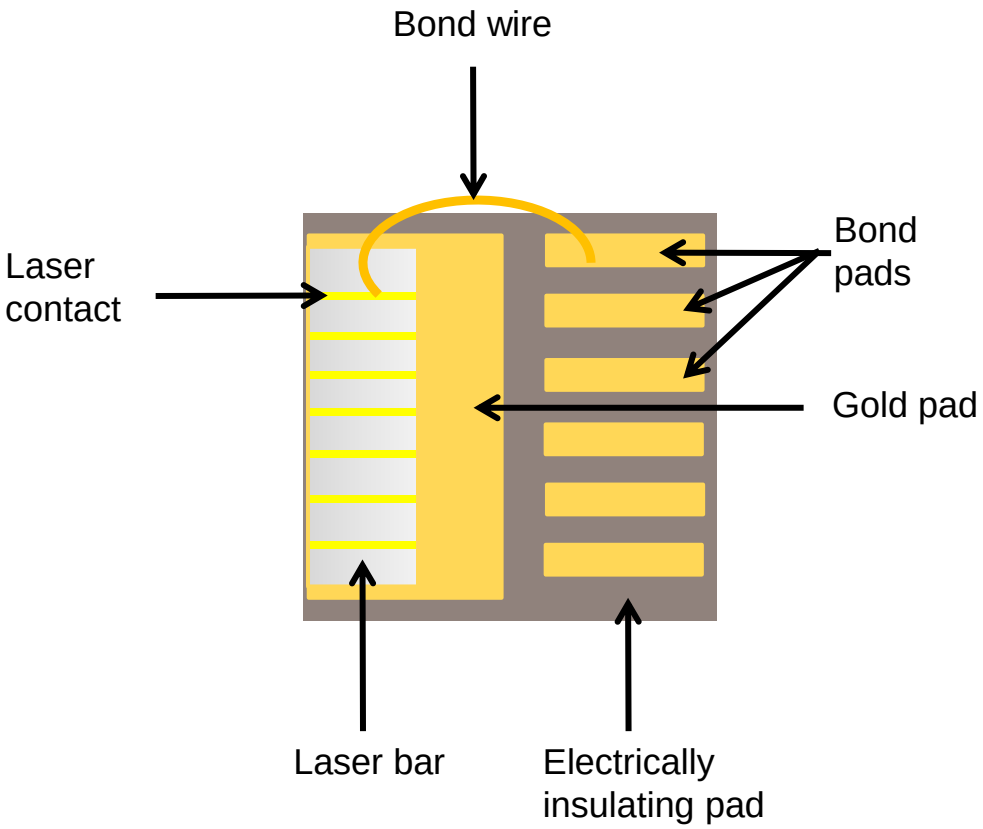


Figure 3.13 Schematic of a laser bar bonded to a bond pad, where one individual laser on the bar has been bonded using a gold wire to a bond pad.

3.3.1 Wire bonding compared to no wire bonding

Figure 3.14 shows the difference in performance between a laser that has not been wire bonded or die bonded and a laser that has been both die and wire bonded. There is a substantial increase in the amount of CW power from the device, with the unbounded device having a maximum CW power < 10 mW at 200 mA whereas the wire and die bonded laser has a power > 30 mW at 200 mA with no roll-off observed. There is also a small decrease in the threshold current, from 70 mA to 55 mA. Figure 3.15 shows the same measurements performed with the laser with Ti/Pt/Au as p-type contact. It also shows a reduction in threshold current (140 mA to 125 mA) and an increase in the output power (~5 mW to ~18 mW).

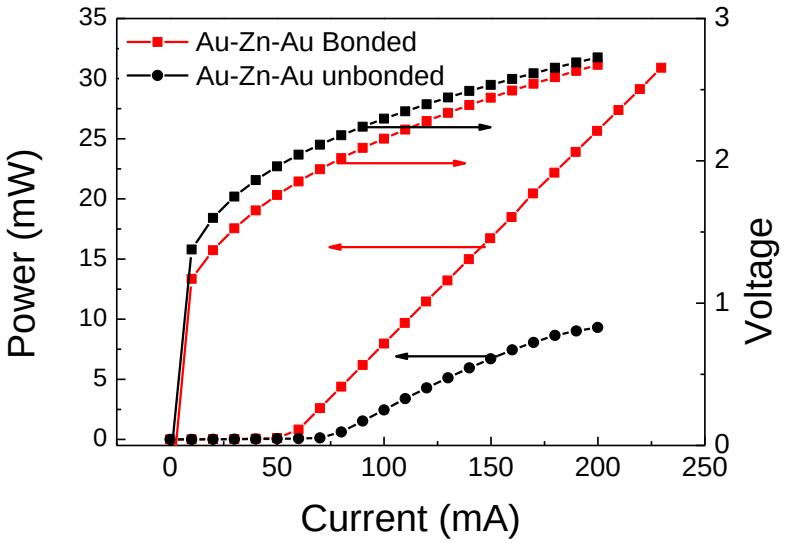


Figure 3.14. CW Current-voltage and current-power relationship showing increase in attainable power for bonded and non-bonded lasers using Au/Zn/Au as the p-type contact.

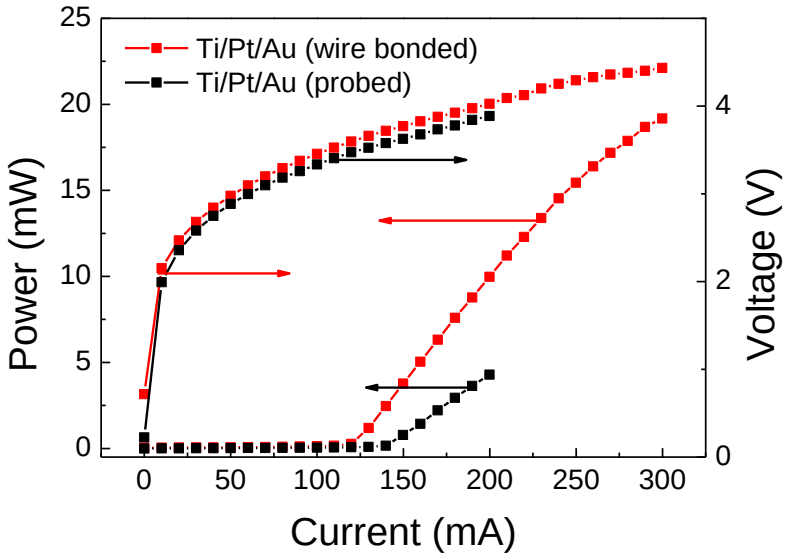


Figure 3.15. CW Current-voltage and current-power relationship showing increase in attainable power for bonded and non-bonded lasers using Au/Zn/Au as the p-type contact

3.3.2 Number of bonds

Another factor to test is the how the number of bonds affect the performance of lasers. This is to determine how much of the increase in power is due to the lasers being die bonded to a heatsink and how much is due to the current being more spread out due to wire bonding. In Figure 3.14 and Figure 3.15 there are six wire bonds equally spaced along a 2-mm cavity. Figure 3.16 shows the IV and LI

characteristics for one laser bar (Au/Zn/Zu p-type contacts) bonded onto a heatsink. On this bar there are multiple lasers with differing amounts of wire bonds to each individual laser. As it can be seen in the figure when there is only one wire bond used there is a thermal roll-over similar to the un-bonded device in Figure 3.9 with a higher power of ~ 20 mW. Increasing the number of wire bonds to two leads to a doubling of the maximum attainable power before roll-off to ~40 mW.

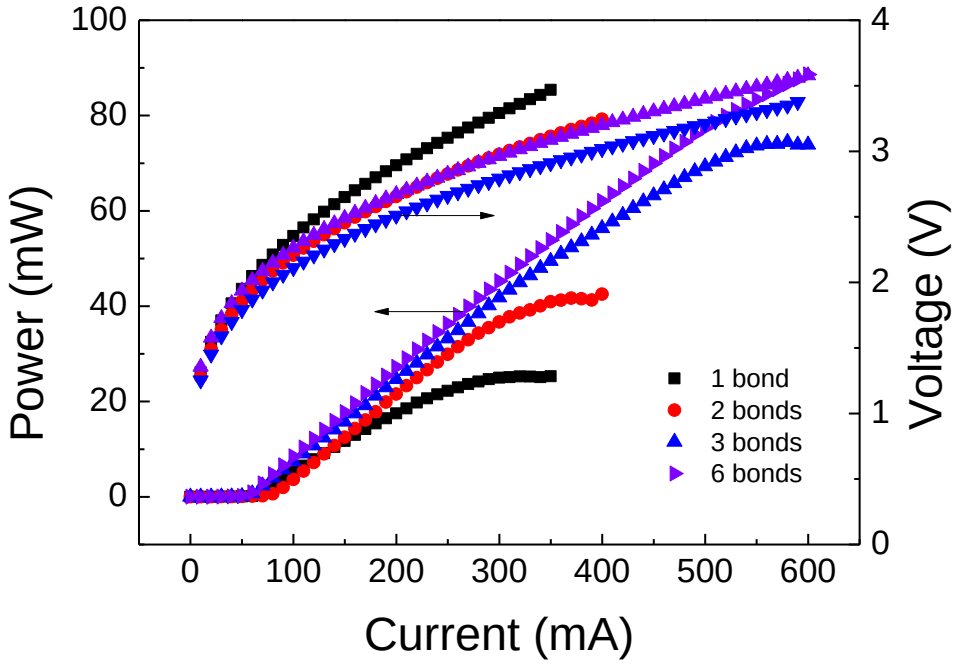


Figure 3.16. CW Current-voltage and current-power relationship for lasers lasers using Au/Zn/Au as the p-type contact, showing dependence on number for wire bonds on output power

3.3.3 Temperature-dependent performance of wire bonded devices

Figure 3.17 shows the CW temperature operation of a laser using Au/Zn/Au as the p-type contact and using six wire bonds to the contact. Lasing is observed up to 70 °C, which is a clear improvement from the value of 35 °C in Figure 3.10. This is due to the improved thermal properties of the device, which leads to less heating at the top p-type contact and better thermal conductivity from the laser to the heatsink.

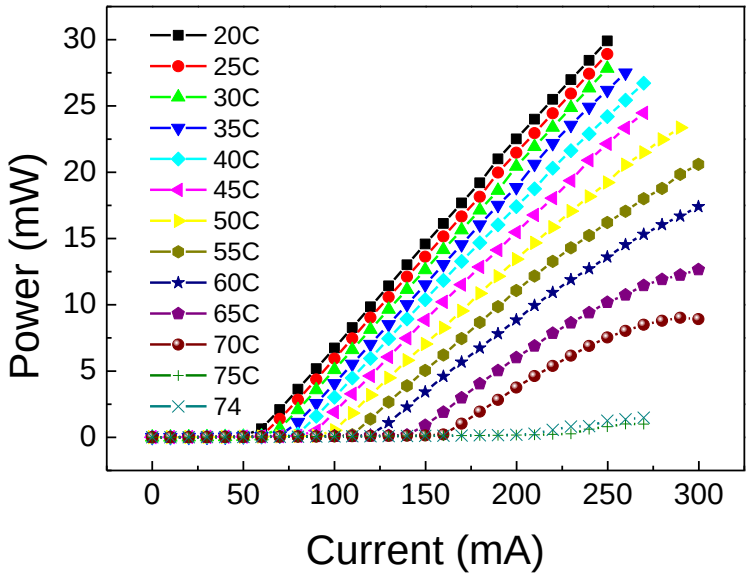


Figure 3.17CW temperature performance of laser on GaAs with 2 mm cavity length and 50 μm width. Lasing is observed up to 70 °C compared to the case of non-wire-bonded devices which only operated up to 35 °C.

3.4 Conclusion

The metal contact deposition and backend processes were optimised. It was found that the use of Au/Zn/Au leads to the lowest contact resistance and best laser performance. Different combinations of Ti/Au and Ti/Pt/Au were tested. Sputtered Ti/Au was marginally better than E-beam evaporated Au, and also had lower chance of contamination due to the ability to pre-sputter the target. The addition of Pt in contacts was also found to improve the contacts and laser performance, where E-beam evaporated Ti/Pt/Au had a lower contact resistivity than Ti/Au. Pt/Ti/Pt/Au was found to have a slightly higher resistivity than Ti/Pt/Au. However it had a better performance when used in the laser fabrication. The temperature operation of lasers fabricated was improved by the use of wire bonding. This greatly improved the lasing threshold current and temperature operation compared to the use of probes alone.

3.5 References

[1] H. H. Berger, "Models for contacts to planar devices," *Solid-State Electronics*, vol. 15, no. 2, pp. 145–158, 1972.

[2] R. Williams, Modern GaAs processing methods. Artech House, 1990.

[3] J. R. Dale and R. G. Turner, "Simple ohmic contacts on gallium arsenide," *Solid-State Electronics*, vol. 6, no. 4, pp. 388–389, Jul. 1963.

[4] N. Braslau, J. B. Gunn, and J. L. Staples, "Metal-semiconductor contacts for GaAs bulk effect devices," *Solid-State Electronics*, vol. 10, no. 5, pp. 381–383, 1967.

[5] Y. Shih, M. Murakami, E. L. Wilkie, and A. C. Callegari, "Effects of interfacial microstructure on uniformity and thermal stability of AuNiGe ohmic contact to n-type GaAs," *Journal of Applied Physics*, vol. 62, no. 2, 1987.

[6] M. Murakami, K. D. Childs, J. M. Baker, and A. Callegari, "Microstructure studies of AuNiGe Ohmic contacts to n-type GaAs," *Journal of Vacuum Science & Technology B*, vol. 4, no. 4, 1986.

[7] N. Braslau, "Summary Abstract: Ohmic contacts to GaAs and GaxAl1−xAs," *Journal of Vacuum Science & Technology B*, vol. 1, no. 3, 1983.

[8] W. Chen, P. Jiao, J. Zhao, S. Wang, S. Guan, and Q. Chen, "The reflectance of solid-phase epitaxial Pd/Ge film on GaAs and its application for VCSELs array," *Solid State Communications*, vol. 88, no. 6, pp. 461–463, Nov. 1993

[9] L. C. Wang, B. Zhang, F. Fang, E. D. Marshall, S. S. Lau, T. Sands and T. F. Kuech (1988) "An investigation of a nonspiking Ohmic contact to n-GaAs using the Si/Pd system", *Journal of Materials Research*, 3, pp 922-930. doi:10.1557/JMR.1988.0922..

[10] L. C. Wang, X. Z. Wang, S. S. Lau, T. Sands, W. K. Chan, and T. F. Kuech, "Stable and shallow PdIn ohmic contacts to n-GaAs," *Applied Physics Letters*, vol. 56, no. 21, 1990.

[11] L. C. Wang, X. Z. Wang, S. N. Hsu, S. S. Lau, P. S. D. Lin, T. Sands, S. A. Schwarz, D. L. Plumton, and T. F. Kuech, "An investigation of the Pd-In-Ge nonspiking Ohmic contact to n-GaAs using transmission line measurement, Kelvin, and Cox and Strack structures," *Journal of Applied Physics*, vol. 69, no. 8, 1991.

[12] C. Lin and C. P. Lee, "Comparison of Au/Ni/Ge, Au/Pd/Ge, and Au/Pt/Ge Ohmic contacts to n-type GaAs," *Journal of Applied Physics*, vol. 67, no. 1, p. 260, 1990.

[13] Y. Lu, T. S. Kalkur, and C. A. Paz de Araujo, "Rapid Thermal Alloyed Ohmic Contacts to p-Type GaAs," *Journal of The Electrochemical Society* , vol. 136 , no. 10 , pp. 3123–3129, Oct. 1989.

[14] T. Ishida, S. Wako, and S. Ushio, "Contact and interconnect formation on compound semiconductor devices by ionized-cluster beam deposition," *Thin Solid Films*, vol. 39, pp. 227–235, Dec. 1976.

[15] G. Stareev, "Formation of extremely low resistance Ti/Pt/Au ohmic contacts to p-GaAs," *Applied Physics Letters*, vol. 62, no. 22, 1993.

[16] D. G. Ivey, "Platinum Metals in Ohmic Contacts to III-V Semiconductors," *Platinum metals review*, vol. 43, no. l, pp. 2–12, 1999.

[17] J.-L. Lee, J. K. Mun, and B.-T. Lee, "Thermal degradation mechanism of Ti/Pt/Au Schottky contact to n-type GaAs," *Journal of Applied Physics*, vol. 82, no. 10, pp. 5011–5016, 1997.

[18] A. Szerling, P. Karbownik, A. Łaszcz, K. Kosiel, and M. Bugajski, "Low-resistance p-type ohmic contacts for high-power InGaAs / GaAs-980 nm CW semiconductor lasers," *Vacuum*, vol. 82, no. 10, pp. 977–981, 2008.

[19] C. C. Han, X. Z. Wang, L. C. Wang, E. D. Marshall, S. S. Lau, S. A. Schwarz, C. J. Palmstro/m, J. P. Harbison, L. T. Florez, R. M. Potemski, M. A. Tischler, and T. F. Kuech, "Nonspiking ohmic contact to p-GaAs by solid-phase regrowth," *Journal of Applied Physics*, vol. 68, no. 11, 1990.

[20] P. -E. Hallali, M. Murakami, W. H. Price, and M. H. Norcott, "Thermally stable ohmic contacts to p-type GaAs. IX. NiInW and NiIn(Mn)W contact metals," *Journal of Applied Physics*, vol. 70, no. 12, 1991.

[21] C. C. Han, X. Z. Wang, S. S. Lau, R. M. Potemski, M. A. Tischler, and T. F. Kuech, "Thermally stable and nonspiking Pd/Sb(Mn) ohmic contact to p-GaAs," *Applied Physics Letters*, vol. 58, no. 15, 1991.

[22] T. C. Shen, G. B. Gao, and H. Morkoc, "Recent developments in ohmic contacts for III--V compound semiconductors," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 10, no. 5, pp. 2113–2132, 1992..

[23] I. R. Sellers, H. Y. Liu, K. M. Groom, D. T. Childs, D. Robbins, T. J. Badcock, M. Hopkinson, D. J. Mowbray, and M. S. Skolnick, "1.3 μm InAs/GaAs multilayer quantum-dot laser with extremely low room-temperature threshold current density," *Electronics Letters*, vol. 40, no. 22, pp. 1412–1413, 2004.

[24] Roland Diehl (2000). "High-power diode lasers: fundamentals, technology, applications", Springer. p. 195.

Chapter 4: Methods to reduce threading dislocations and effects within III-V layers grown on silicon substrates

4.1 Introduction

The so-called "Holy Grail" of silicon photonics is the demonstration of an electrically-pumped laser on a Si platform operated in CW mode, with similar characteristics as the state-of-art GaAs lasers. The first lasers on Si were limited to optically pulsed Raman lasers [1]. At UCL, lasers on Si were demonstrated operating under pulsed conditions [2], with a threshold ~ 725 A/cm^2. For optoelectronic integrated circuits (OEIC) a CW source capable of operating above room temperature is required. This is because CMOS devices often operate at high temperatures (~60 °C), and a requirement of cooling components for the laser would add a very high cost. One of largest stumbling blocks in the path to the successful demonstration of an electrically-pumped CW laser integrated on Si is the difference between the lattice constants of Si and GaAs. The lattice mismatch leads to the formation of threading dislocations (TDs), due to the build-up of strain between Si substrates and GaAs buffer [3], [4]. Although some of TDs are confined to the interface layer, the majority

of TDs can propagate into the III-V active layers, which will lead to high threshold current densities and overall poor device quality.

It has been shown that the amount of defects which propagate into the active layers is sensitive to the initial growth conditions of the nucleation layer (NL) [2] and that the optimal growth temperature for the initial nucleation of GaAs buffer layer on Si substrates was 400 °C. Similarly, it is sensible and logical to assume that the material choice for the initial nucleation layer will have an effect on the growth quality. For example, it has been found that, for the growth of GaSb epilayers on Si substrates, AlSb provides a more effective NL than other materials [5]. In addition, AlAs has previously been used in thick buffer layers in order to grow GaN on Si [6], [7].

In this chapter it was found that the change of laser structure led to an improvement in the lasing threshold current density. Additionally, the use of a thin AlAs NL instead of a GaAs NL was found to decrease the amount of defects in the active layers, confirmed by improvements in photoluminescence intensity and lasing performance. Devices were fabricated with lower threshold current densities of 670 A/cm^2, which is lower than previously reported values of 725 A/cm^2 [2]. Finally lasers with sputtered and wire bonded contacts as described in chapter three were shown to have a significantly lower threshold current density of ~ 365 A/cm^2.

4.2 MBE growth details

All samples were grown using a Veeco solid source molecular beam epitaxy (MBE) system at the Department of Electrical and Electronic Engineering at UCL. The samples were grown on phosphorous-doped N-type Si substrates

In this chapter samples with a GaAs and also AlAs NLs were grown. However many steps of the growth are identical, so can be described in the same section. The differing features will be expanded upon in latter sections. All growth was started on Si (100) with a 4 ° offcut towards the [110] plane. After the substrates were loaded into the chamber, they were heated to 900 °C and held for 10 minutes in order to desorb oxygen from the surface. Following this step the substrate was then cooled to low temperatures to grow the III-V layers.

4.2.1 GaAs nucleation layer optimisation

First a 30-nm GaAs initial NL was grown with a low growth rate. The temperature of this growth was optimised by observing the PL from test structures. Figure 4.1 shows room temperature PL spectra from three samples grown on Si substrates with different growth temperatures for the initial 30-nm GaAs NL along with the PL spectrum of a reference sample grown on GaAs for comparison. The PL has a maximum intensity at ~ 1300 nm for the GaAs sample and ~ 1291 nm for the samples grown on Si substrates. A secondary maximum can be observed at ~ 1220 nm for GaAs sample. This secondary maximum is due to the growth of a wetting layer which is formed when growing QDs. The full-width half-maximum (FWHM) of all 3 samples is ~30 meV, which is comparable to InAs QDs grown on GaAs [8]. The PL intensity is strongly dependent on the initial temperature of the nucleation layer.

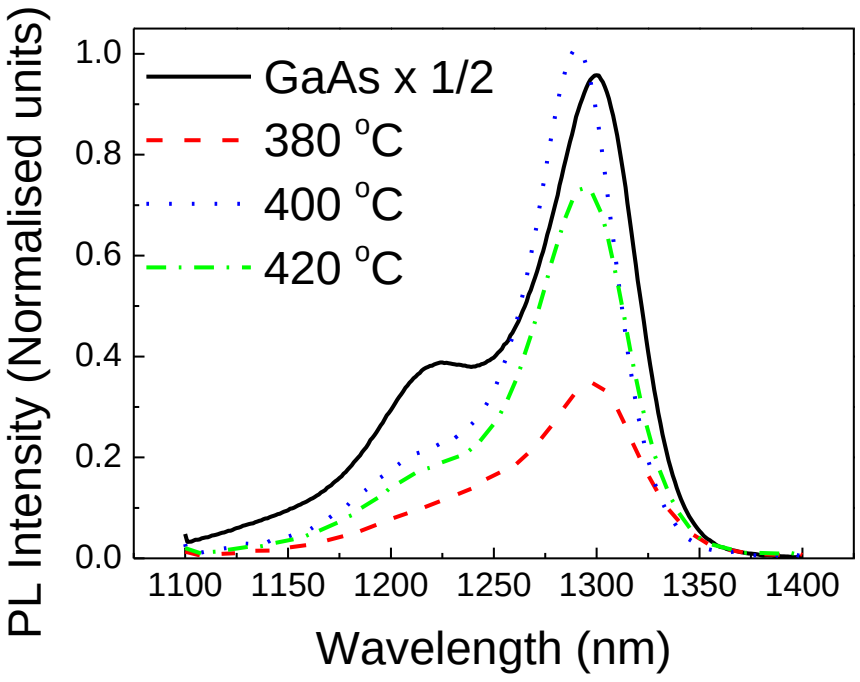


Figure 4.1. RT PL spectra of InAs/GaAs QDs grown on Si substrates with different growth temperatures for the initial GaAs nucleation layer. The RT PL spectrum of InAs QDs grown on GaAs substrate is also shown as a reference.

Afterwards, the temperature was raised to 500 ˚C and 170 nm GaAs was deposited as an intermediate buffer layer, followed by an additional 800-nm GaAs layer at an elevated temperature. Figure 4.2 shows the PL spectra of samples with different

thicknesses of intermediate layers using an initial GaAs NL grown at 400 °C. It is apparent that 170 nm is the optimal thickness for the intermediate NL, as the intensity of the ground state emission is significantly higher than the other two thicknesses. The make-up of the GaAs NL is shown in Table 4.1.

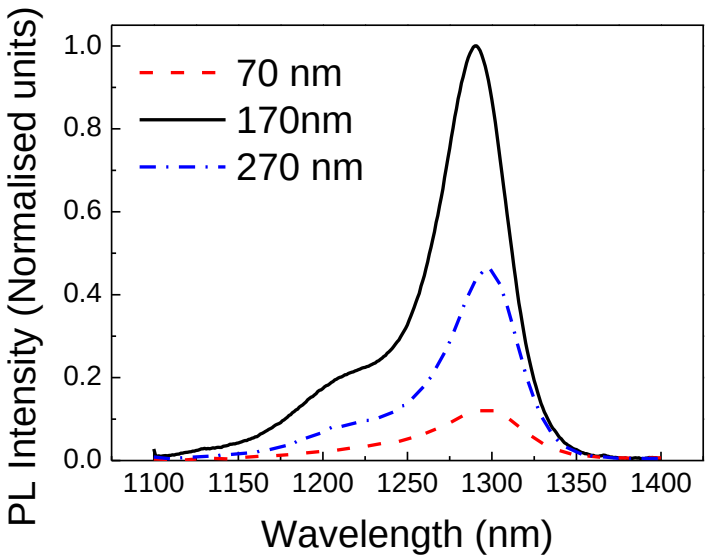


Figure 4.2 RT PL spectra of InAs/GaAs QDs grown on Si substrates with different thicknesses of low temperature growth layers of the GaAs nucleation layer.

800 nm	High temperature buffer layer	580 °C
70,**170**, 270 nm	Intermediate buffer layer	500 °C
30 nm	Initial nucleation layer	380, **400** 420 °C

Table 4.1. Growth temperature of GaAs buffer layer showing growth parameters. The optimised values are shown in bold.

4.2.2 Dislocation filter layers and active layer

From this stage, the growth was the same whether an AlAs or GaAs NL was used. On top of the GaAs buffer layer, multilayer InGaAs/GaAs dislocation filter layers were

grown, which are known to reduce the TD density by orders of magnitude. The dislocation filter layers consisted of two repeats of a five period 10-nm $In_{0.15}Ga_{0.85}As$/10-nm GaAs superlattices and a 350-nm layer of GaAs. The last layer of the filter layer was a 160 nm superlattice consisting of alternating layers of 2-nm GaAs and 2-nm $Al_{0.4}Ga_{0.6}As$.

For the laser active layer, a five layer dot-in-well (DWELL) structure was grown. This structure had previously been optimised for use on a GaAs substrate [9]. Each QD layer consisted of 3.0 MLs of InAs grown on 2-nm of $In_{0.15}Ga_{0.85}As$ and capped by 6-nm of $In_{0.15}Ga_{0.85}As$ at ~510 °C . The DWELLs were separated by 45 nm of GaAs barriers. The DWELL structure was embedded between a 50 nm GaAs layers, which was grown at 580 °C. A 50-nm layer of AlGaAs were used to prevent photogenerated charge carriers migrating to interface or substrate at high temperatures and then capped by 50-nm GaAs. The structure can be seen in Figure 4.3.

Figure 4.3. Cross-sectional schematic of fabricated InAs/InGaAs dot-in-a-well (DWELL) structure on Si substrate.

4.2.3 AlAs nucleation layer

In the previous sub-section, the buffer layer growth using GaAs was optimised. However, the material choice of the nucleation layer has been shown to strongly effect the introduction of TDs.

The effect of using AlAs as the initial NL was investigated. A Si (100) wafer with a 4 ° miscut towards the [110] plane was loaded into the MBE chamber and the same oxide desorption procedure was followed as for previous growth. Then the substrate was cooled to 400 °C for growth of the AlAs nucleation layer. Test samples with a nucleation layer of 2.5, 5 and 10 nm of AlAs were used to investigate the optimal thickness and a reference sample using GaAs as the NL was also grown, all the samples were grown on Si substrates. The growth following the AlAs NL was kept the same as for devices grown with a GaAs NL (as described in 4.2.2). The optimal conditions were determined by AFM and PL studies of the grown samples, and further confirmed by the growth of a laser structure using the optimised value for the AlAs NL. PL and AFM studies are advantageous as they are relatively quick to perform, and can provide crucial insights to the growth quality of substrates. TEM measurements were also taken to investigate the growth, as it can give a good indication of the quality of the dislocation filter layers, and can be used to confirm the conclusions deduced from the AFM and PL results.

AFM studies

In order to investigate the growth mechanism of the AlAs and GaAs nucleation layers, the two samples were grown on Si substrates where the growth was terminated after the growth of a 5 nm of the nucleation layer. The first sample was grown using 5 nm of AlAs and the second sample was grown using 5 nm of GaAs. Then AFM studies were performed for these two samples. Typical images can be seen in Figure 4.5, with (a) showing QDs formed with after 5 nm GaAs NL grown and (b) showing QDs formed after the growth of 5 nm of AlAs. Both images have a 1 μm x 1 μm scale. As can be seen in the figure, the GaAs quantum dots formed are smaller than the AlAs QDs, with a height and width of approximately 4 and 20 nm respectively. In addition, the QD density is approximately 5 x 10^{10} /cm^2. This indicates that the GaAs NL relaxes strain via the formation of coherent islands, similar to the In(Ga)As/GaAs system [10]. The increase in strain by further

x`deposition of GaAs will eventually lead to the coalescence of coherent GaAs dots, and hence the formation of defects in the GaAs buffer layers [11].

In contrast, a lower density of approximately $4 \times 10^9/cm^2$ was obtained for AlAs dots grown on Si. These dots have an irregular shape, and larger average height and width of about 20 and 80 respectively (Figure 4.4(b)). The shape and size of AlAs dots indicate that the AlAs dots are defective [11]. This suggests that the strain energy of a 5 nm AlAs NL grown on Si is mainly relaxed by the formation of defective AlAs dots and defects at the AlAs/Si interface. Therefore, in comparison with the sample with the GaAs NL (Figure 4.4(a)), more defects are confined at the III-V/Si interface and less defects propagating into the GaAs buffer layer are observed for the sample with the AlAs NL.

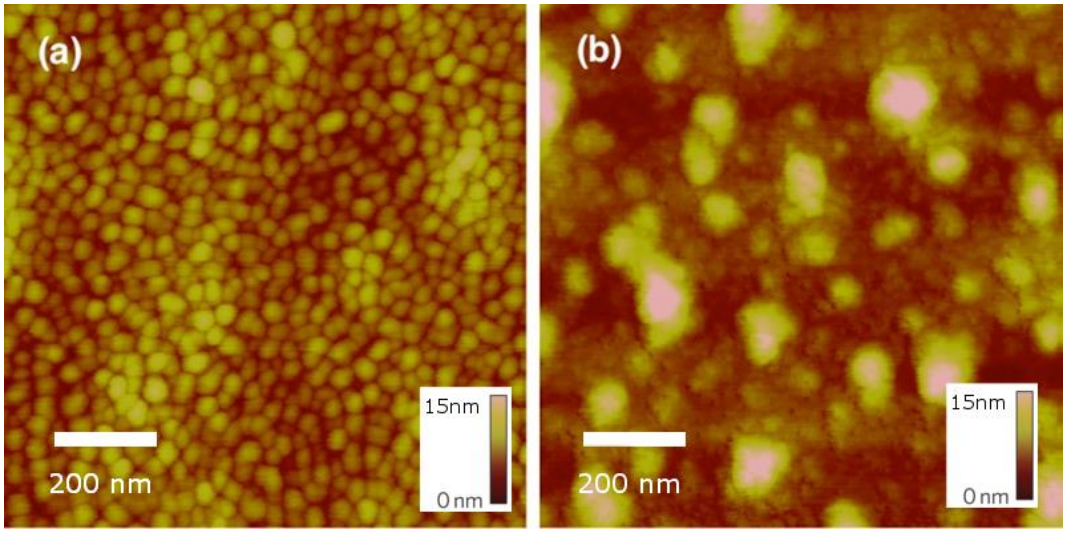


Figure 4.4. AFM image showing (a) 5 nm GaAs NL. (b) 5 nm AlAs NL.

PL Studies

Figure 4.6 shows the room temperature (RT) PL spectra of InAs/GaAs QDs on Si substrates with 5-nm GaAs or 2.5-, 5- and 10-nm AlAs nucleation layers. The InAs/GaAs QDs yield a room temperature (RT) emission at ~1.29 μm with a full width at half maximum (FWHM) of ~ 30 meV for all of the samples, as shown in Figure 4.6. A wetting layer is again obserble at ~ 1.20 μm. Of considerable significance is that the RT integrated PL intensity (IPLI) of the sample with the AlAs NL is about 40% higher than that of the sample with the GaAs NL. It should be mentioned that the sample with the GaAs NL was grown under the same optimised

conditions as the first electrically pumped 1.3-μm InAs/GaAs QD laser monolithically grown on Si substrates [2]. Figure 4.5 gives a clear indication of which thickness of AlAs is the best, as 5-nm AlAs leads to the highest PL intensity at room temperature.

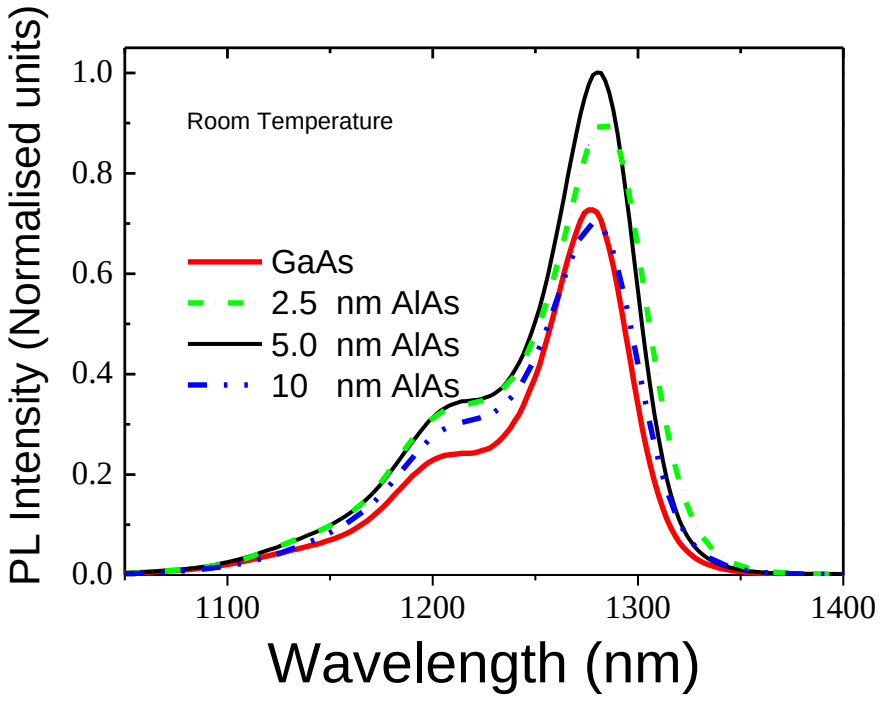


Figure 4.5. Photoluminescence intensity versus wavelength at room temperature for samples with a GaAs NL and 2.5, 5 and 10 nm AlAs NLs.

The comparison of integrated photoluminescence intensities (IPLI) over the temperature range 10-300 K were studied for all samples. Figure 4.6 shows the plot of the 5-nm NL for both GaAs and AlAs, against inverse temperature in Kelvin. Thermal activation energies of about 260 meV are yielded by fitting Arrhenius curves to the temperature dependent PL for both the 5-nm AlAs and GaAs samples in Figure 4.6. 260 meV is close to the energy difference between the QD ground state and InGaAs quantum well in the InAs/InGaAs DWELL structure.

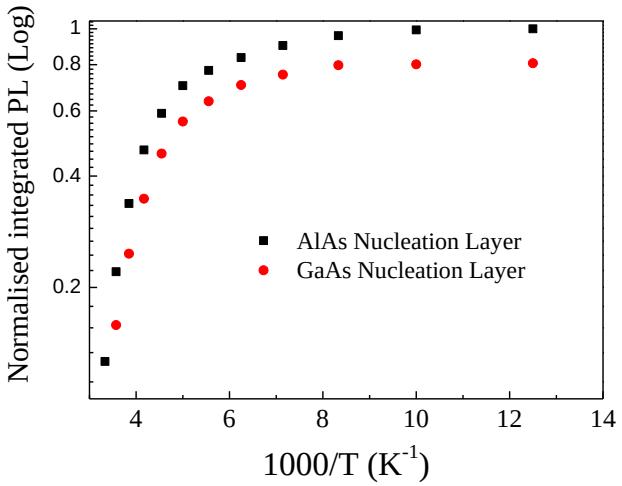


Figure 4.6. Integrated PL intensity versus inverse temperature for 5 nm AlAs and GaAs NLs.

The reduction in the IPLIs of InAs/GaAs QDs with increasing temperature is attributed to the thermal escape of carriers from InAs QD ground states into InGaAs QWs followed by non-radiative recombination in the barriers [15].

Therefore, the enhancement of IPLI for the sample with the AlAs NL could be understood as being due to the reduced density of threading dislocations propagating into the InAs/InGaAs DWELL region.

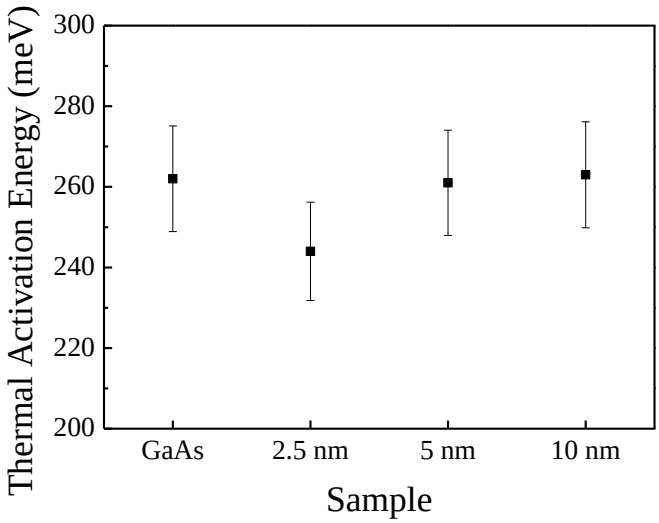


Figure 4.7. Thermal activation of samples shown with 2.5, 5 and 10 nm of AlAs NL and comapred to GaAs NL.

TEM

It is believed that an AlAs NL performs better than a GaAs NL because AlAs, due to the strong intra-atom bonding of Al, is able to confine more threading dislocations at the interface. This leads to a higher density of threading dislocations at the interface, but a lower density of threading dislocations in the active layers. This can be confirmed via transmission electron microscopy. Figure 4.8 shows the interface between, (a) GaAs and Si and (b) AlAs and Si. As can be observed in the figures, there are more threading dislocations in (a) that propagate vertically compared to (b). Also, there is a higher amount of defects in (b) at the interface along with a higher strain observable. This would act to confirm the hypothesis that AlAs can contain more defects than a GaAs NL.

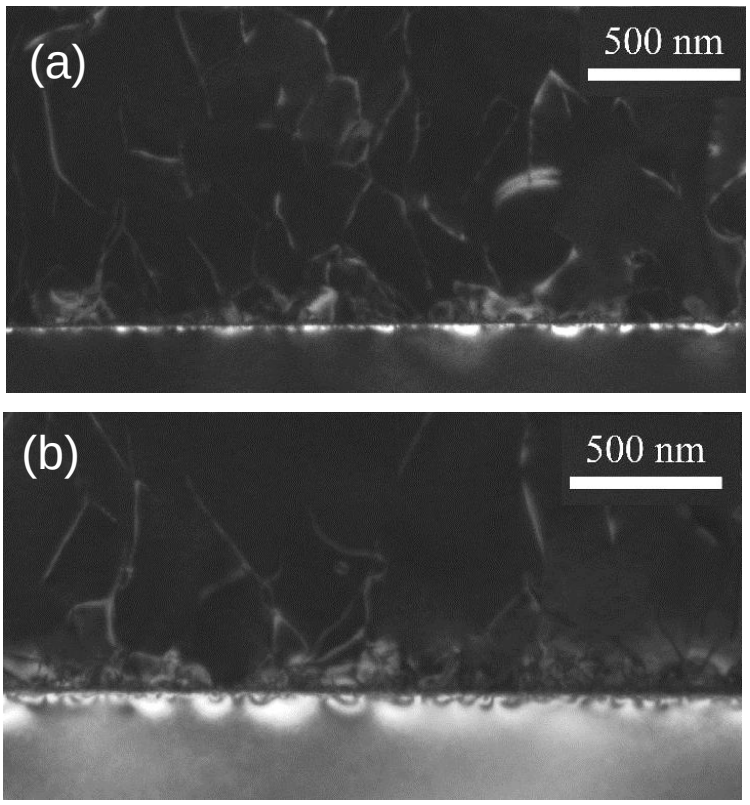


Figure 4.8. TEM image of interface between Si and GaAs. (a) shows interface with 5nm GaAs as NL and (b) shows one with 5 nm AlAs. Then both have same structure for buffer layers.

This was further explored in Figure 4.9, which shows the interface region for samples with a GaAs NL and AlAs NL with thicknesses of 5 nm for both GaAs and AlAs. Figure 4.10 shows the TEM images for the case of 2.5-nm and 10-nm AlAs NL. It is clear to see from the TEM images that the TD density is significantly higher, and that the TDs propagate further into the growth, with many passing through multiple defect filter layers. These results clearly indicate that 5 nm is the optimum thickness for the AlAs NL, and confirms the results of the AFM and PL studies.

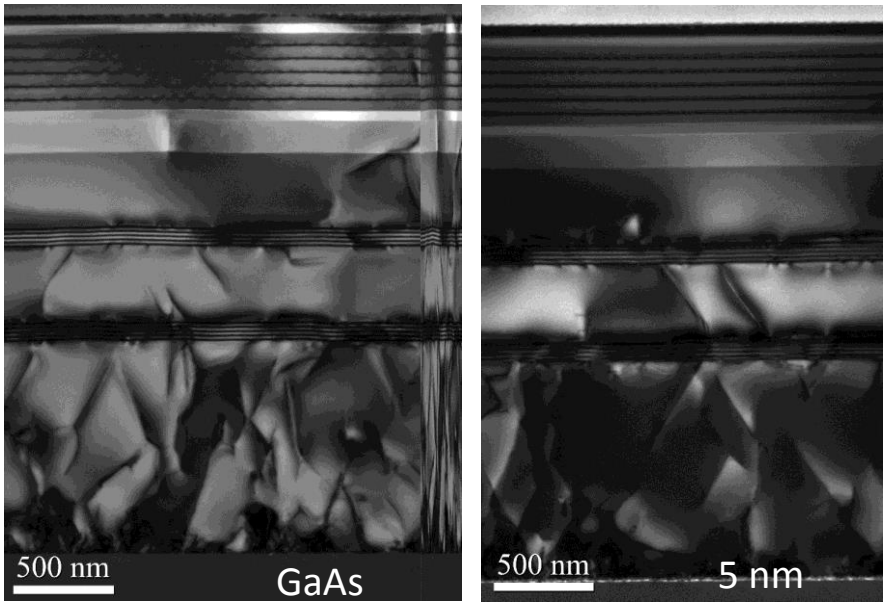


Figure 4.9. TEM images of interface and active region of laser samples with GaAs and a 5 nm AlAs NL. The TEM image shows that there are less threading dislocations which propagate into the active layer of the laser structure

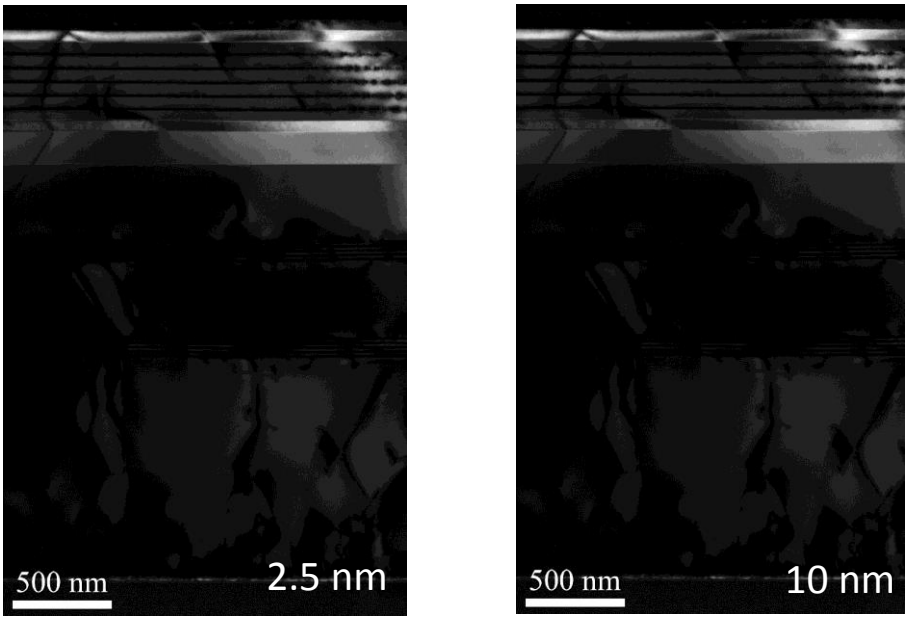


Figure 4.10. TEM images of interface and active region of laser samples with an AlAs NL of 5 nm and 10 nm. It is clear from TEM that there are threading dislocations propagating into the active region in both cases.

Etch-pit density

The defect density at the III-V active region was estimated by etch pit density (EPD) tests for both the sample with the AlAs NL and the one with the GaAs NL. The etchant used for the EPD delineation is a mixture of H_3PO_4, H_2O_2, and H_2O (in a 1:1:3 ratio) [14]. The defect densities of $\sim 3 \times 10^6$ /cm^2 and $\sim 6 \times 10^6$ /cm^2 were obtained for the samples with the AlAs NL and the one with the GaAs NL, respectively.

4.3 Device performance

Lasers were fabricated for both structures using GaAs as an initial nucleation layer and 5-nm AlAs NL.

4.3.1 CW laser using a GaAs Nucleation layer

The main source of defects stems from the difference in lattice constant between Si and GaAs; therefore the majority of the defects are confined to the Si/GaAs interface. In a conventional "top-bottom" structured device the current will be forced to pass through the defect-high interface as depicted in Figure 4.11(a), leading to an increased resistance and heating in the device. To avoid this, a "top-top" structure

can be fabricated, which routes the current to avoid the defect-high density interface as shown in principal in Figure 4.11(b).

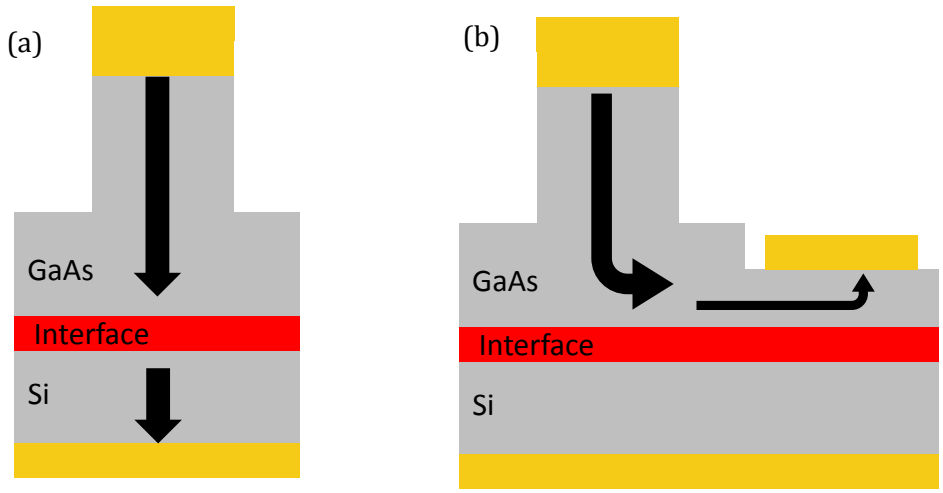


Figure 4.12. Schematic of "top-bottom" and "top-top" contact laser structures. (a) shows the conventional "top-bottom" structure and (b) shows the "top-top" structure, which has the advantage that the current passing through the device avoids the interface region between the Si and GaAs.

Ridge lasers structures were fabricated using a GaAs nucleation layer, with the same optimised growth as described in the previous sections. Cavity widths of 20 μm were etched using a 1:1:1 solution of Adachi etchant and the same etchant was used to etch the pits for the "bottom" n-type contacts. SiO_2 was deposited on the sample using PECVD and the contact windows were etched using HF. The ridge was etched to approximately 1.6 μm, so that the active layer was not etched.

The p-type contact was made using an E-beam evaporation of Ti/Au and the n-type contact made use of thermal evaporation of Ni/Ge/Au. The contacts were annealed in a rapid thermal processor. After lapping the fabricated lasers were cleaved to a cavity length of 3 mm and were hard soldered onto a gold coated copper heatsink then tested by probing.

These lasers were tested at at 8 °C. It was found that the lasers performed in CW operation. Previously only pulsed mode operation was achievable. The LI curve is shown on the left-hand axis of Figure 4.12, with a threshold current of 275 mA which corresponds to a current density of 458 A/cm^2. The lasing spectra of the

device are shown above and below threshold in Figure 4.13. The peak lasing wavelength is 1278 nm. The right-hand axis of Figure 4.12 shows the IV characteristics of the lasing device. It has a series resistance of 4.2 Ω and a turn on voltage of 1.1 V. Although CW lasing was achieved below room temperature, room temperature CW lasing was not observed.

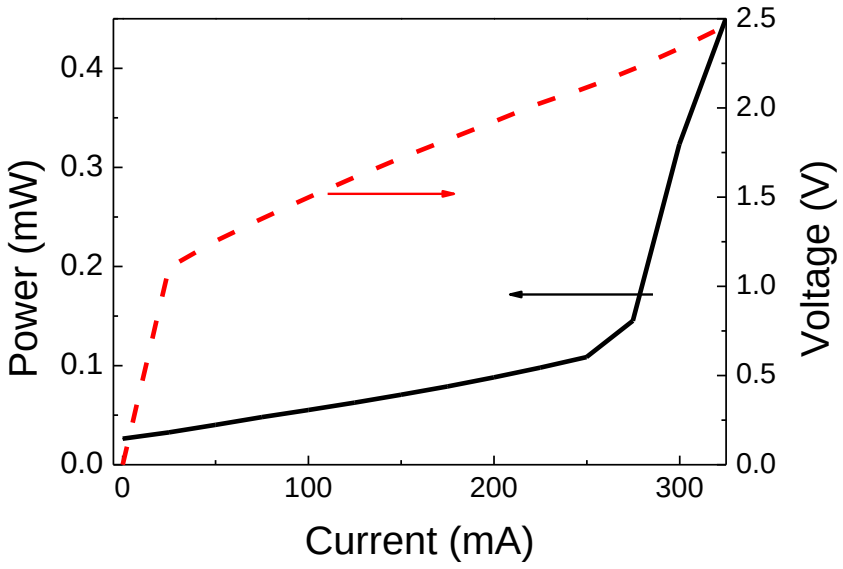


Figure 4.12. CW LI and IV characteristics for device at 8 °C with a GaAs NL at CW operation.

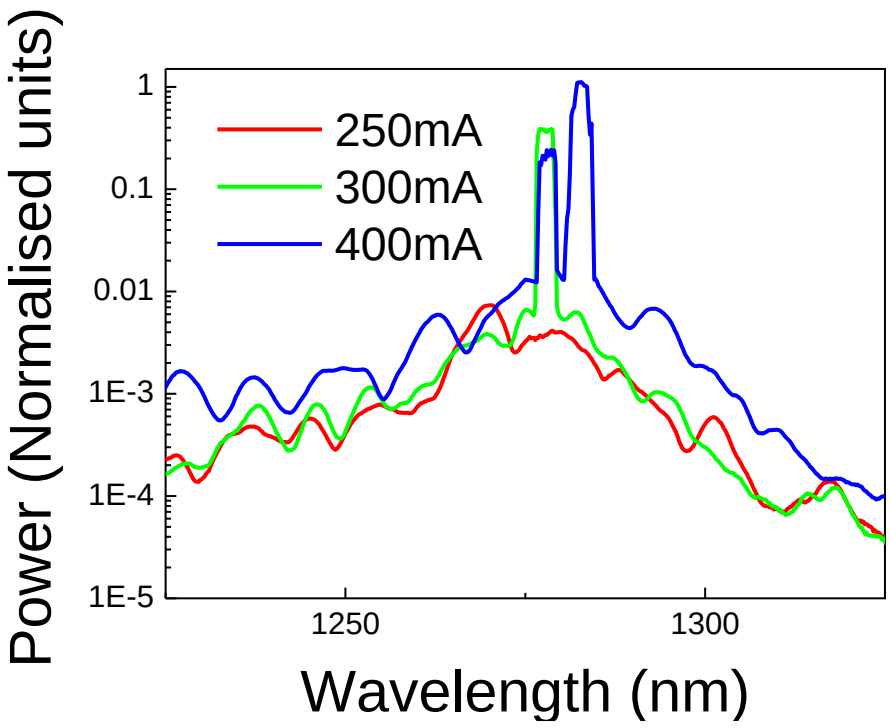


Figure 4.13. CW spectra above and below lasing threshold for laser at 8 °C.

Further improvements in III-V buffer layer technology, such as use of quantum dot filter layers could lead to samples fabricated with lower defect densities in the active layers [15]. This would lead to lower threshold currents due to lower loss in the cavities. Lower threshold currents will enable the lasers to operate at higher temperature due to the reduced thermal heating due to the current. In addition, improvements in the resistance of the contact materials would also lead to devices with lower series resistances, and so also reduced heating in devices. This has the potential of enabling CW lasing of lasers directly grown on Si without the use of intermediate materials such as Ge.

This result shows the potential for CW III-V QD lasers on Si at room-temperature with further work to enable this. The performance of CW lasers grown monolithically on Si has been achieved by the optimisation of the laser structure and nucleation layer. However there is still room for improvement. The extracted external differential quantum efficiency is only 0.6 % for the QD laser sample on Si.

4.3.2 Lasers using AlAs nucleation layer

In order to further investigate the effect of the AlAs NL, Si-based InAs/GaAs laser diodes using an AlAs NL were grown. DWELL structures were fabricated with the same optimised conditions as in reference [2]. Devices with 20 and 50 μm ridges were fabricated by photolithography, wet etching and standard metallisation techniques, as described in chapter 2 and 3. These were then cleaved to 3.5-mm laser bars, with the facets being left as-cleaved. Laser characteristics were measured in pulsed mode using a pulse width of 0.1 μs and duty cycle of 0.01%. These conditions were chosen to minimise thermal heating, in order to minimise the effect of the lasers heating due to the injected current.

The device IV curve can be seen in Figure 4.14, measured using a Keithley 4-point probe. This results in a series resistance of approximately 7.58 Ω. This is higher than in typical GaAs devices, generally of order 1-2 Ω [14]. The reasons for this are twofold. Firstly the choice of metals for n and p contacts has yet to be optimised. Although the contacts are Ohmic, there are still improvements that could be made to obtain lower contact resistances. Secondly, lasers grown on Si, rather than GaAs will have a higher defect density throughout the sample, due to the defects introduced due to the difference in lattice constants between Si and GaAs.

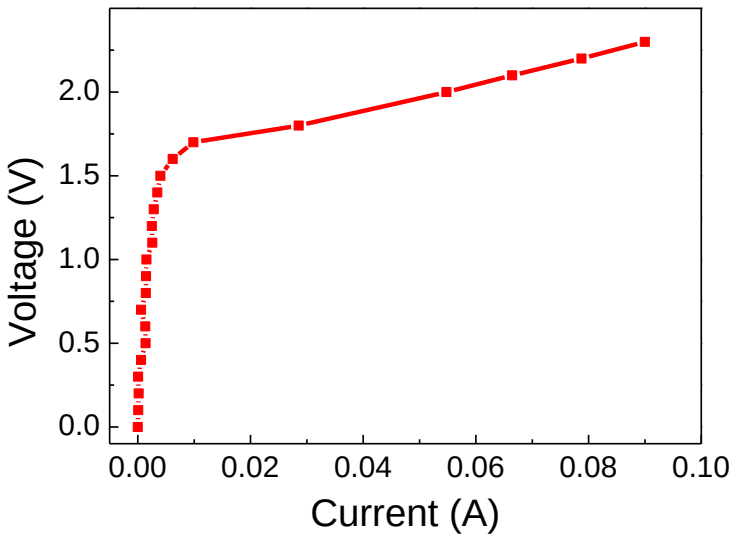


Figure 4.14. Voltage versus current for 50 μm device. Series resistance is ~ 7.58 Ω, which is significantly higher than in devices grown on GaAs.

The spectra output at above threshold current is shown in the inset Figure 4.15, demonstrating RT lasing at 1.286 μm. The main part of Figure 4.15 shows the RT light output against drive (L-I) characteristic for the device with a cavity length of 3.5 mm.

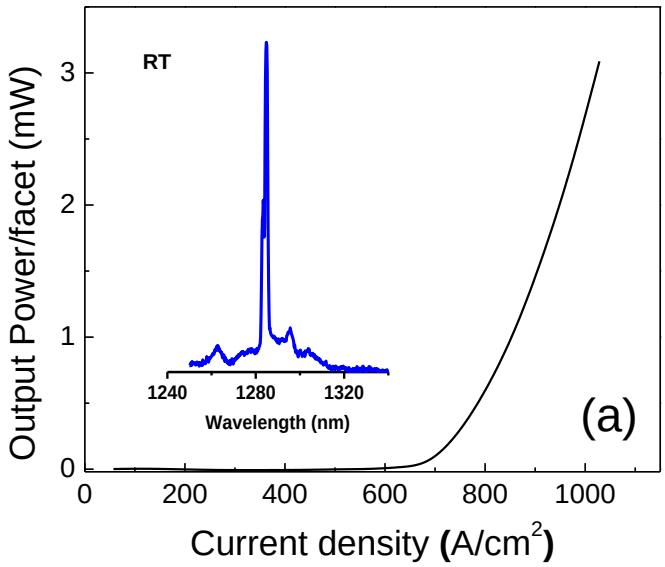


Figure 4.15. Light output versus current for a 3.5 mm cavity with AlAs NL. Threshold current ~675 A/cm^2. Inset shows spectra at room temperature

The RT J_{th} is about 670 A/cm^2, which is lower that the previously reported values of III-V QD lasers monolithically grown on Si substrates, such as 900 A/cm^2 for 1.02-μm QD device and 725 A/cm^2 for 1.3-μm QD laser [2, 15]. Figure 4.16 shows L-I curves for a device with 3-mm length at various temperatures. This QD laser has a 63 °C maximum lasing temperature with a characteristic temperature T_0 of ~40K between 18 and 63 °C , which is comparable to the values of 1.3-μm InAs/GaAs QD lasers grown on GaAs substrates

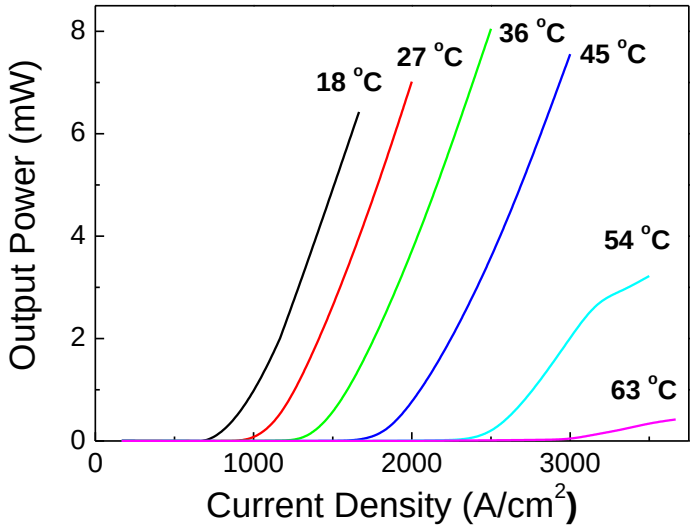


Figure 4.16. Temperature dependent LI showing lasing up to 63C.

4.4 Wire bonded lasers

Chapter 3 discusses wire bonding and the use of sputtered metals, which led to significant improvements in lasing thresholds. In the previous sections the lasers were tested using metal probes, this was because early processing methods led to metals with poor mechanical properties, i.e. the adhesion of the metal to the GaAs was low. This meant that any attempt to wire bond the lasers of sections 4.2.3 and 4.2.3 led to the metal contact being pulled off. Later improvements in processing methods such as cleaning, metal deposition and wire bonding techniques increased the mechanical strength of the metal and the lasers were able to be wire bonded.

Following the improvement of lasers due to sputtered contacts, a laser structure was grown with a sputtered p-type contact, consisting of Ti/Pt/Au. An n-type top contact was used by wet etching to the n-type GaAs layer where Ni/GeAu/Ni/Au was used for the contact, this being the same as in sections 4.2.3 and 4.2.3. Figure 4.17 shows an LI plot for a laser with a 2-mm cavity length and 50-µm width. The lasing threshold has been improved to a value of ~365 A/cm^2 at room temperature.

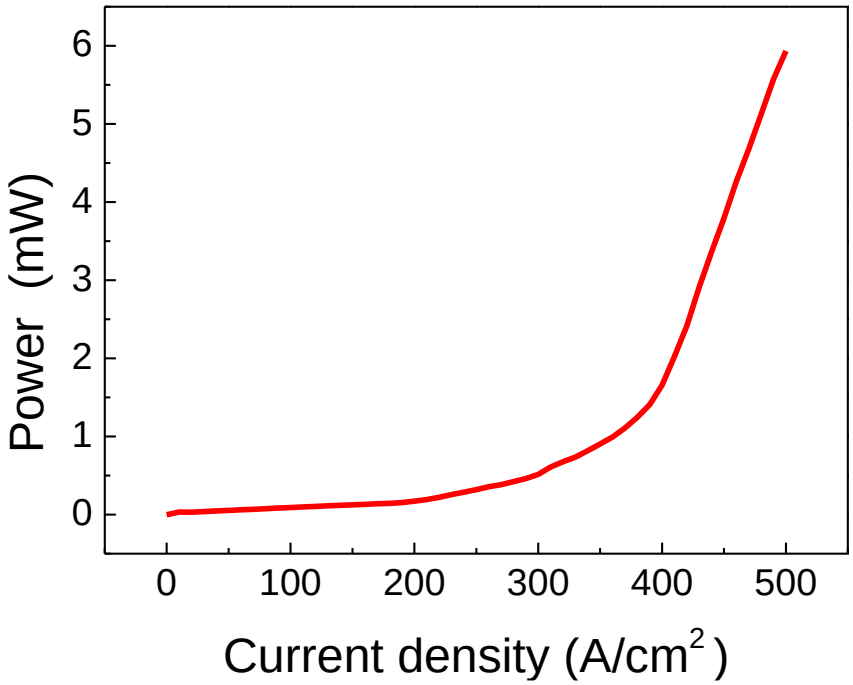


Figure 4.17. Pulsed LI for 2 mm x 50 μm device grown on Si with wire bonded sputtered Ti/Pt/Au contacts.

Although a reduction in lasing threshold was achieved and increase in emitted power, CW lasing at room temperature has yet to be demonstrated from these devices. Further improvements in the MBE growth and fabrication techniques could potentially lead to even lower threshold currents and CW lasing.

4.5 Conclusion

In this chapter, the change of laser fabrication process, from a "top-bottom" structure to a "top-top" structure has been shown to lead to the demonstration of a CW electrically pumped laser on Si. This was due to the fact that the "top-top" structure routes the current away from the defect-high interface between Si and GaAs. It has also been shown that an AlAs nucleation layer in the place of a GaAs improves the measured photoluminescence (PL) intensity. This increased PL intensity was believed to be due to the high bonding strength of Al in the AlAs NL which produces substrates with better threading dislocation (TD) handling

properties. AFM and TEM images confirmed the growth mode and TD handling properties.

Devices were fabricated with lower threshold currents than devices grown using a GaAs NL, with a threshold current density of ~ 670 A/cm^2 compared to 725 A/cm^2. Finally lasers grown on Si were fabricated with sputtered Ti/Pt/Au contacts and wire bonded to contact pads, which resulted in a pulsed threshold current density of ~ 365 A/cm^2 at room temperature for a 2-mm device.

4.6 References

[1] J. T. Clarke, J.-C. Gérard, D. Grodent, S. Wannawichian, J. Gustin, J. Connerney, F. Crary, M. Dougherty, W. Kurth, S. W. H. Cowley, E. J. Bunce, T. Hill, and J. Kim, "A continuous-wave Raman silicon laser," *Nature*, vol. 433, no. 7027, pp. 717–9, Feb. 2005.

[2] T. Wang, H. Liu, A. Lee, F. Pozzi, and A. Seeds, "InAs/GaAs quantum-dot lasers monolithically grown on Si substrates," *Optics express*, vol. 19, no. 12, pp. 11381–11386, Jun. 2011.

[3] H. Y. Xu, Y. N. Guo, Y. Wang, J. Zou, J. H. Kang, Q. Gao, H. H. Tan, and C. Jagadish, "Effects of annealing and substrate orientation on epitaxial growth of GaAs on Si," *Journal of Applied Physics*, vol. 106, no. 8, p. 083514, 2009.

[4] T. Won, G. Munns, R. Houdré, and H. Morkoç, "Interface charge polarity of a polar on nonpolar semiconductor GaAs/Si with Ga and As prelayers," *Applied Physics Letters*, vol. 49, no. 19, p. 1257, 1986.

[5] G. Balakrishnan, S. Huang, L. R. Dawson, Y.-C. Xin, P. Conlin, and D. L. Huffaker, "Growth mechanisms of highly mismatched AlSb on a Si substrate," *Applied Physics Letters*, vol. 86, no. 3, p. 034105, 2005.

[6] A. Strittmatter, A. Krost, M. Straßburg, V. Türck, D. Bimberg, J. Bläsing, and J. Christen, "Low-pressure metal organic chemical vapor deposition of GaN on silicon(111) substrates using an AlAs nucleation layer," *Applied Physics Letters*, vol. 74, no. 9, p. 1242, 1999.

[7] A. Strittmatter, D. Bimberg, A. Krost, J. Bläsing, and P. Veit, "Structural investigation of GaN layers grown on Si (111) substrates using a nitridated AlAs buffer layer," *Journal of Crystal Growth*, vol. 221, no. 1–4, pp. 293–296, 2000.

[8] H. Y. Liu, I. R. Sellers, T. J. Badcock, D. J. Mowbray, M. S. Skolnick, K. M. Groom, M. Gutiérrez, M. Hopkinson, J. S. Ng, J. P. R. David, and R. Beanland, "Improved performance of 1.3 μm multilayer InAs quantum-dot lasers using a high-growth-temperature GaAs spacer layer," *Applied Physics Letters*, vol. 85, no. 5, p. 704, 2004.

[9] H. Y. Liu, I. R. Sellers, T. J. Badcock, D. J. Mowbray, M. S. Skolnick, K. M. Groom, M. Gutiérrez, M. Hopkinson, J. S. Ng, J. P. R. David, and R. Beanland, "Improved

performance of 1.3 μm multilayer InAs quantum-dot lasers using a high-growth-temperature GaAs spacer layer," *Applied Physics Letters*, vol. 85, no. 5, p. 704, 2004.

[10] H.-Y. Liu, B. Xu, Y.-Q. Wei, D. Ding, J.-J. Qian, Q. Han, J.-B. Liang, and Z.-G. Wang, "High-power and long-lifetime InAs/GaAs quantum-dot laser at 1080 nm," *Applied Physics Letters*, vol. 79, no. 18, pp. 2868–2870, 2001.

[11] H. Y. Liu, I. R. Sellers, M. Gutiérrez, K. M. Groom, W. M. Soong, M. Hopkinson, J. P. R. David, R. Beanland, T. J. Badcock, D. J. Mowbray, and M. S. Skolnick, "Influences of the spacer layer growth temperature on multilayer InAs⁄GaAs quantum dot structures," *Journal of Applied Physics*, vol. 96, no. 4, p. 1988, 2004.

[12] D. P. Popescu, P. G. Eliseev, A. Stintz, and K. J. Malloy, "Temperature dependence of the photoluminescence emission from InAs quantum dots in a strained Ga0. 85In0. 15As quantum well," *Semiconductor science and technology*, vol. 19, no. 1, p. 33, 2003.

[13] R. Chen, H. Y. Liu, and H. D. Sun, "Electronic energy levels and carrier dynamics in InAs/InGaAs dots-in-a-well structure investigated by optical spectroscopy," *Journal of Applied Physics*, vol. 107, no. 1, p. 013513, 2010.

[14] R. Williams, *Modern GaAs processing methods*. Artech House, 1990.

[15] Z. Mi, J. Yang, P. Bhattacharya, and D. L. Huffaker, "Self-organised quantum dots as dislocation filters : the case of GaAs-based lasers on silicon," *Electronics Letters*, vol. 42, no. 2, pp. 1–2, 2006.

Chapter 5: Electrically-pumped CW lasers grown on Ge-on-Si

5.1 Introduction

In this chapter electrically pumped CW InAs/GaAs quantum-dot lasers on silicon have been demonstrated using germanium-on-silicon substrates. It is already been demonsrated that Ge substrates can be used to produce lasers with threshold currents almost as low as that of GaAs substrates [1]. Due to the development of high quality photodetectors on Ge-on-Si [2], Ge-on-Si substrates are commercially available, and therefore the growth of III-V materials on Si is a realistic goal to be achieved using Ge-on-Si substrates. The same techniques and know-how that were used to grow lasers on Ge can be transferred to a Ge-on-Si platform.

It is well known that the growth of III-V compounds on Si, such as GaAs on Si, is made complicated due to the differing properties of Si and the III-V compounds. For example, GaAs is a polar compound whereas Si is non-polar. Of particular concern is the high lattice mismatch between Si and GaAs (approximately 4%), which causes the formation of a high density of threading dislocations (TD). If the TD propagates

into the active layers of a lasing structure, this will lead to a deterioration in laser performance, i.e. high threshold currents and poor temperature operation.

In contrast the use of a Ge epi-layer offers a unique advantage, due to the small lattice mismatch between Ge and GaAs (~0.08 %). This small lattice mismatch leads to a significantly reduced TD density. This makes the growth of GaAs on Ge-on-Si a very desirable prospect. Lasers using Ge-on-Si substrates have already been demonstrated with Ge as the active layer [3,4], however these have been severely limited by very high threshold current densities, of order 100's kA/cm^2, where in contrast lasers grown directly on Si in this work have had threshold current density of approximately 675 A/cm^2, and lasers grown on Ge have been demonstrated with CW threshold current density <60 A/cm^2 [1].

5.2 Growth details of GaAs on Ge-on-Si

First a 2-µm layer of Ge was grown by chemical vapour deposition (CVD) on a Si (100) substrate with a 6° offcut towards the [111] plane. This buffer layer had a threading dislocation density of ~ 5 x 10^6 cm^{-2}. Typically, the defect density of GaAs substrates is at least three orders of magnitude less, in the range of (0.1 – 5) x 10^3 cm^{-2}, which is dependent upon the dopant type and concentration [5,6].

III-V structures were grown using a Veeco solid source molecular beam epitaxy (MBE) reactor at the department of Electrical Engineering at University College London. The growth conditions of GaAs on Ge-on-Si were kept similar to growth on Ge and Si [1,7]. The oxygen layer was desorbed from the substrate surface by heating the substrate to 400 °C and holding it for 10 minutes. Then the substrate temperature was heated to 650 °C and held for 20 minutes, and finally reduced to low temperatures (~400 °C, dependent upon the particular growth) for growth of III-V layers. The same Ga pre-layer technique as in Ref. 1 was used. This entailed keeping the Ga shutter shut over the sample until just before growth was commenced, ensuring that any As from the MBE background was not absorbed onto the surface. The Ga pre-layer technique inhibits the formation of anti-phase domains (APD), which lead to the increase of current densities through the device, as they create barriers for the current to travel through. To form the Ga pre-layer, 1.08 ML of Ga was deposited and then the As valve was opened for 1 minute. Following the initial nucleation layer of GaAs, 20 MLs of GaAs were grown by migration enhanced epitaxy using alternating beams of Ga and As_4. After the 20 ML of GaAs, a 2-µm p +

III-V buffer layer with a doping density of $p = 1 \times 10^{19}/cm^3$ was grown. QD laser structures containing five InAs/InGaAs dot-in-well (DWELL) structures were then grown at optimized conditions as on GaAs substrates [7, 8]. Each QD layer consisted of 3.0 MLs of InAs grown on 2 nm of $In_{0.15}Ga_{0.85}As$ and capped by 6 nm of $In_{0.15}Ga_{0.85}As$ at ~510 °C . The DWELLs were separated by 45 nm of GaAs barriers. And were embedded between 50-nm GaAs layers (grown at 580 °C). A 50 nm of AlGaAs layer was used to prevent photogenerated charge carriers migrating to interface or substrate at high temperatures [9]. The DWELL structure was surrounded by 55-nm AlGaAs guiding layers, and 1.5-µm layers of n and p-type doped AlGaAs. Finally a 300 nm n-doped GaAs contact-forming layer was deposited. The grown structure is shown in Figure 5.1.

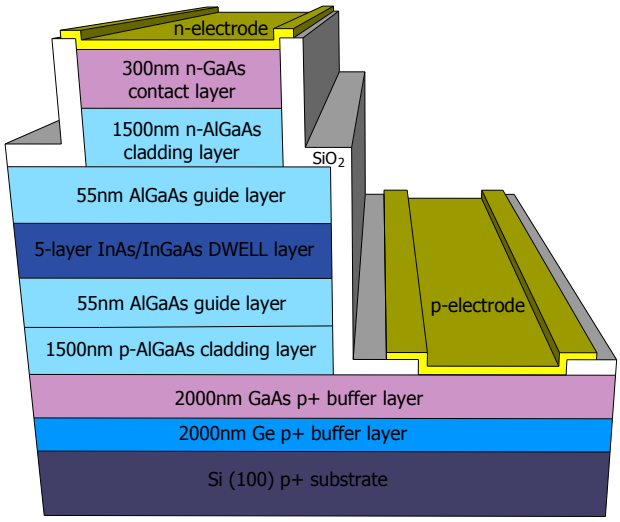


Figure 5.1. Schematic showing structure of InAs/GaAs QD laser grown on Si substrates.

5.3 Optimisation of MBE growth

In the same manner as growth of GaAs on Si was optimised, the growth parameters of GaAs on Ge-on-Si also needed to be optimised in order to obtain lasers with the lowest possible threshold current. Three test samples were fabricated on Ge-on-Si substrates with different growth temperatures of the InAs QD layer, at 590, 600 and 610 °C. Photoluminescence (PL) and atomic force microscopy (AFM) measurements were taken to evaluate the optimum growth conditions and these were confirmed by taking transmission electron microscopy (TEM) measurements.

5.3.1 Photoluminescence

The PL intensities for different samples grown on Ge-on-Si substrates were compared to PL results from growth on a Ge substrate as reference. Figure 5.2 shows the obtained PL spectra for all three samples on Ge-on-Si and the Ge substrate at room temperature at a constant laser excitation power. All samples had a FWHM close to ~ 50 nm which is comparable to results for growth on Si and GaAs. The Ge substrate had a ground-state emission peak at 1290 nm with a FWHM of ~56 nm. The sample grown at 590 °C had a ground state peak at 1284 nm and FWHM ~ 54 nm. The sample grown at 600 °C had a ground peak emission at 1280 nm and FWHM at 48 nm. Finally the sample grown at 610 °C had a peak at 1266 nm and FWHM ~ 45 nm. As the sample grown at 600 °C had the highest PL intensity for samples grown on Ge-on-Si this was investigated further. Second maxima are also visible which show the emission from the wetting layer of the QDs.

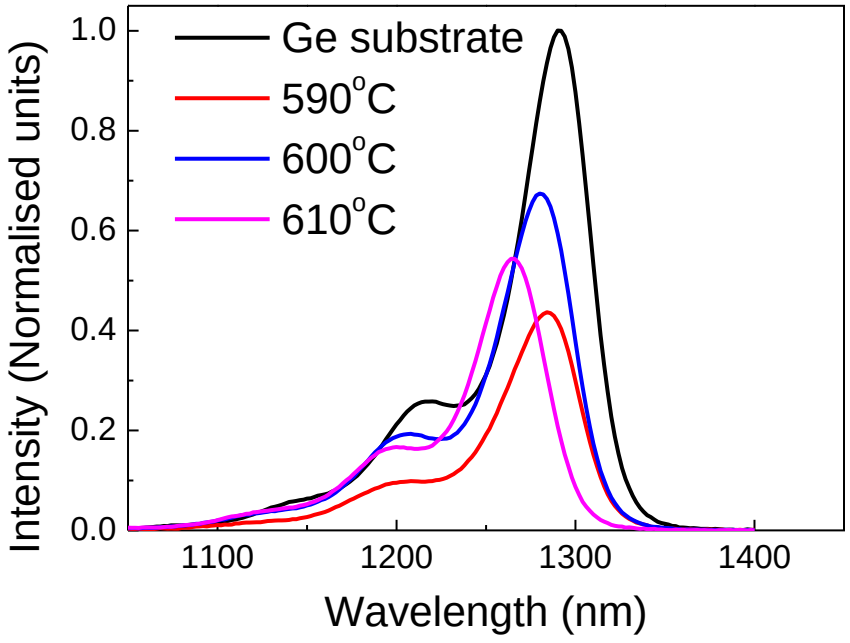


Figure 5.2. PL intensity versus wavelength for all three test samples and a reference Ge sample.

Figure 5.3 shows temperature-dependent PL taken from 10 to 300 K for Ge-on-Si samples at constant power. This shows that the ground state remains unsaturated up to low temperatures. The ground state moves from ~1280 nm at room temperature (300K) to 1198 nm at 120 K. In addition, power dependent

measurements were also taken for the sample grown at 600 °C to further investigate the properties of the quantum dots. In Figure 5.4 there is little saturation of the ground state until higher incident energies meaning that the quantum dots have a small amount of defects.

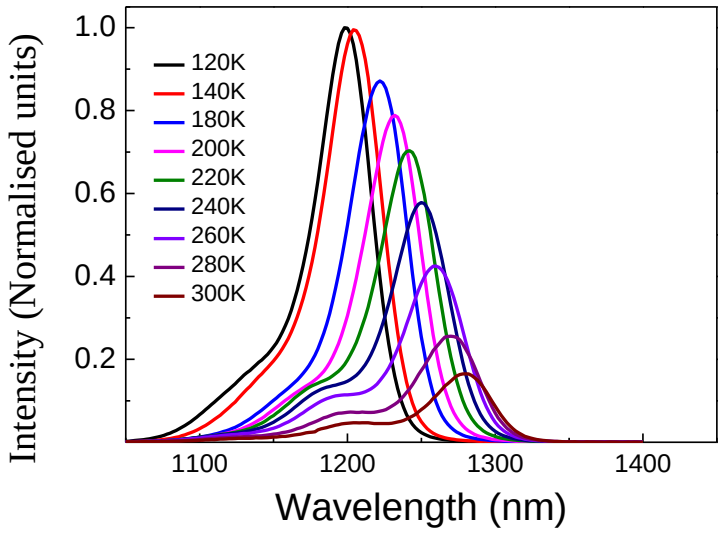


Figure 5.3. PL intensity versus temperature from 10K to 300K at constant power for the sample grown at 600 °C

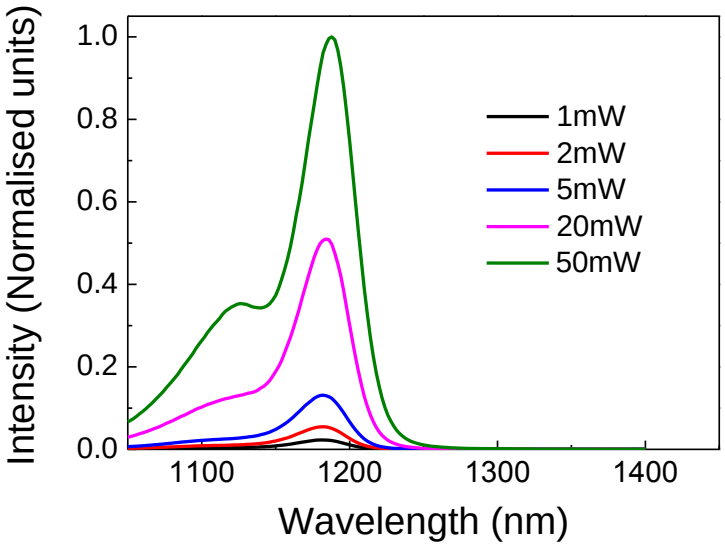


Figure 5.4. PL intensity versus wavelength of sample UCL114R3 for 1, 2, 5, 20 and 50 mW of incident power for the sample grown at 600 °C.

5.3.2 Atomic force microscopy

AFM images of uncapped QDs were also taken using a Nanosurf AFM, and a typical result is shown in Figure 5.5. This corresponds to a high density of ~ 3.5 x 10^{10}/cm^2. They are also relatively uniform, which is important as any distribution in size and shape of the quantum dots will broaden the density of states; leading to a broadened gain profile and higher threshold current. A qualitative example of this is shown in Figure 5.6.

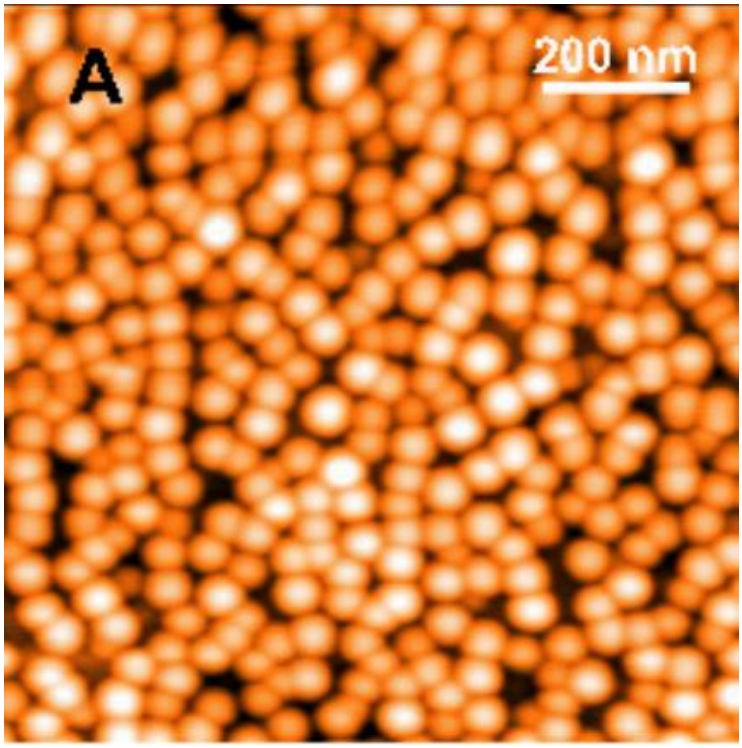


Figure 5.5. 1 μm x 1 μm AFM image of InAs/GaAs QDs grown on a Ge-on-Si substrate.

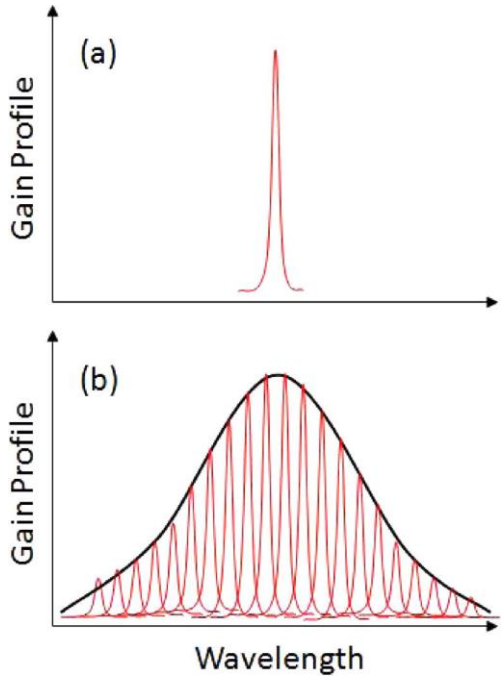


Figure 5.6. A qualitative example of gain profile of: (a) a single quantum dot and (b) an ensemble of quantum dots.

5.3.3 Transmission electron microscopy

In addition to PL studies, TEM studies of Ge, Ge-on-Si and GaAs were made. Figure 5.7 shows TEM images of the active regions of DWELL structures grown on (a) GaAs, (b) Ge and (c) Ge-on-Si substrates. The layers in the figures are almost indistinguishable. QDs in the image are all approximately a similar size with no TDs visible in the active layers.

PL, AFM and TEM results all suggest that the active layer quality is almost as good as lasers grown on Ge and GaAs substrates. This means that it would be possible to fabricate lasers with good device properties.

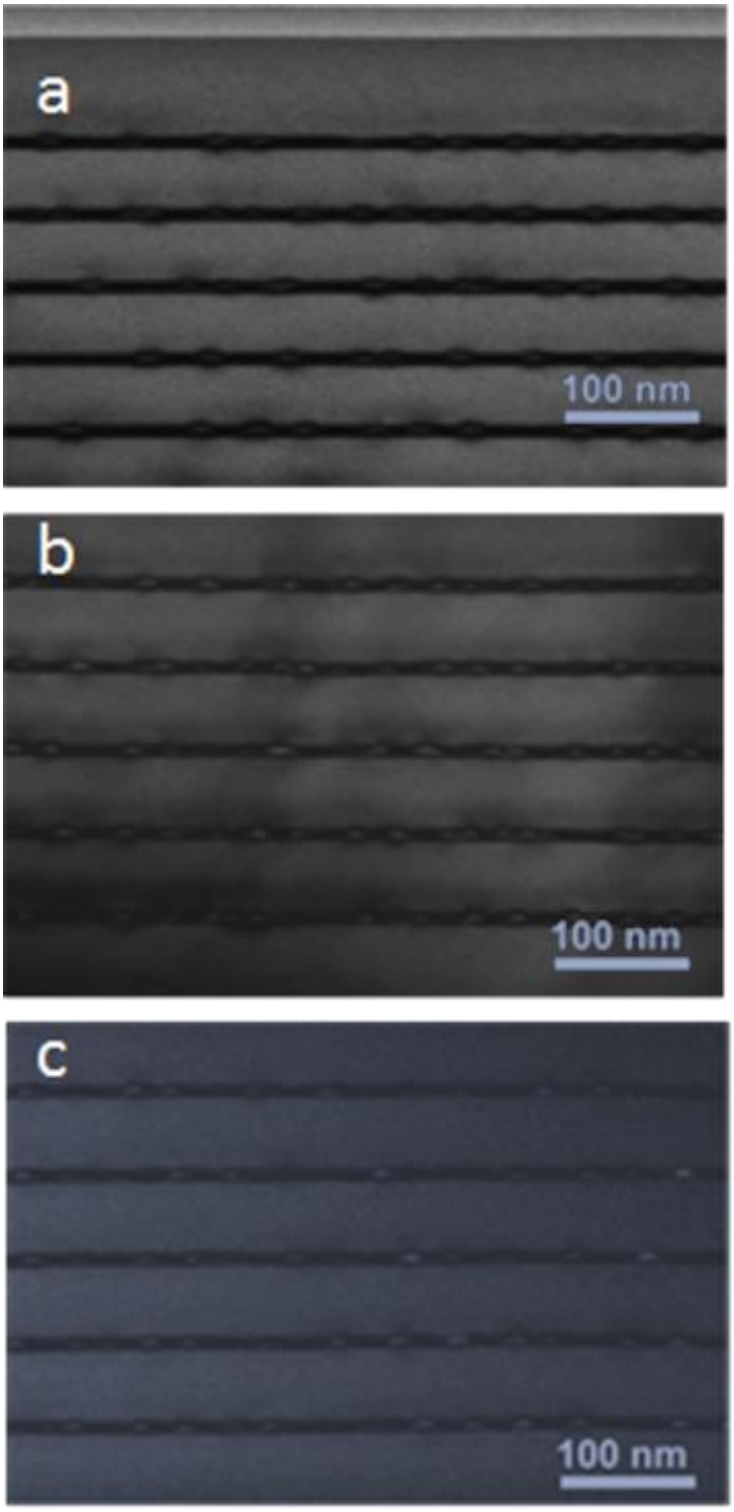


Figure 5.7. Dark field TEM images of the QD laser active region on (a), GaAs substrate; (b), Ge substrate and (c), Ge-on-Si substrate. Laser fabrication.

5.4 Lasers on Ge-on-Si substrates

More detailed information on device fabrication is given in chapters 2 and 3. Photolithography was used to define ridges of 20 μm, which were then wet etched using Adachi etchant (1:1:1 HBr:CH_3COOH:$K_2Cr_2O_7$). The pits were etched in order to allow p-type contacts to be deposited. Before metallisation a 300-nm layer of SiO_2 was formed on the surface using PECVD and contact windows were etched using HF. As the Si substrate was p-doped, Ni/GeAu/Ni/Au (5/50/25/250 nm) was used for the n-type contact with and Ti/Pt/Au (10/50/250 nm) was evaporated using an E-beam evaporator. The device structure can be seen in Figure 5.1, in which the p-type contact was used on the top of the GaAs buffer layer, not the back of the Si substrate. This was achieved by wet etching down to the III-V buffer layer. The reason for this architecture was that it was important to avoid the interface between Ge and Si, and Ge and GaAs as there is a high density of defects at these interfaces. After metallisation and annealing, the devices were thinned to facilitate cleaving improve the device thermal resistance. Devices of 3.0- and 3.5-mm cavity lengths were cleaved with the facets being left as cleaved. Devices were bar tested using probes, without any wire bonding.

5.4.1 3.0-mm devices

Figure 5.8 shows the power-current (LI) measurements for 3-mm-long Ge-on-Si based InAs/GaAs QD laser in pulsed mode at various substrate temperatures. This Si-based InAs/GaAs QD laser has a maximum lasing temperature at 84 °C with a characteristic temperature, T_0, of ~37 K between 21 °C and 84 °C .

Temperature-dependent output LI measurements under CW operation are shown in Figure 5.9 and the spectra above and below threshold is shown in Figure 5.10 with a peak emission wavelength of 1290 nm. Continuous-wave laser operation is achieved up to 30 °C with a T_0 of ~23 K between 12 and 30 °C The poor T_0 values observed here is mainly due to hole excitation out of the lasing state [10]. T_0 values have been increased, by p-type modulation doping of the QDs in the active layers which suppresses hole excitation, even approaching to $T_0 \approx \infty$ for GaAs-based InAs QD lasers [11].

The next step toward increasing the temperature stability and CW operation temperature for Si-based QD lasers are can be realised by further exploiting p-type modulation doping of the QDs into these laser structures

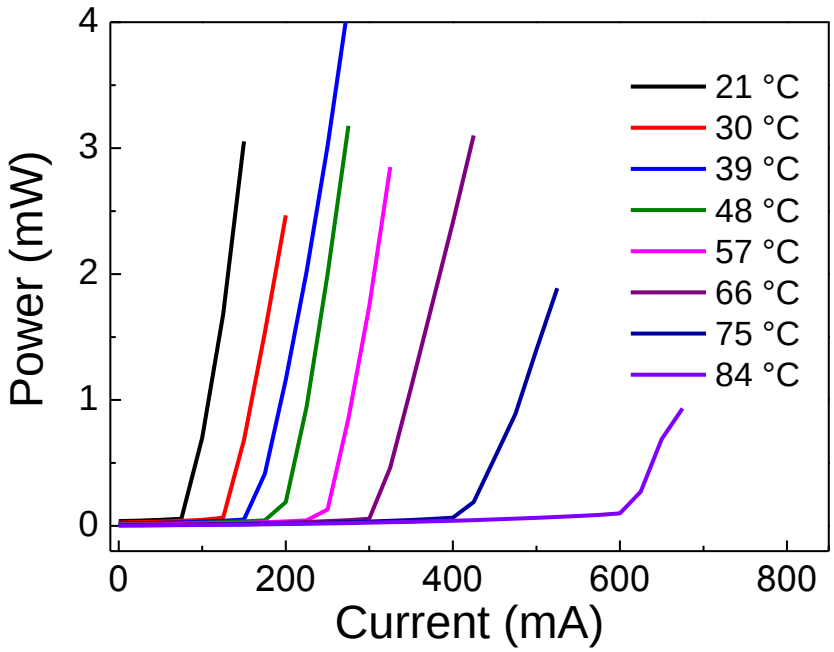


Figure 5.8. Light output versus current for temperatures up to 84 °C under pulsed conditions for a 3.0 mm cavity length and 20 μm width.

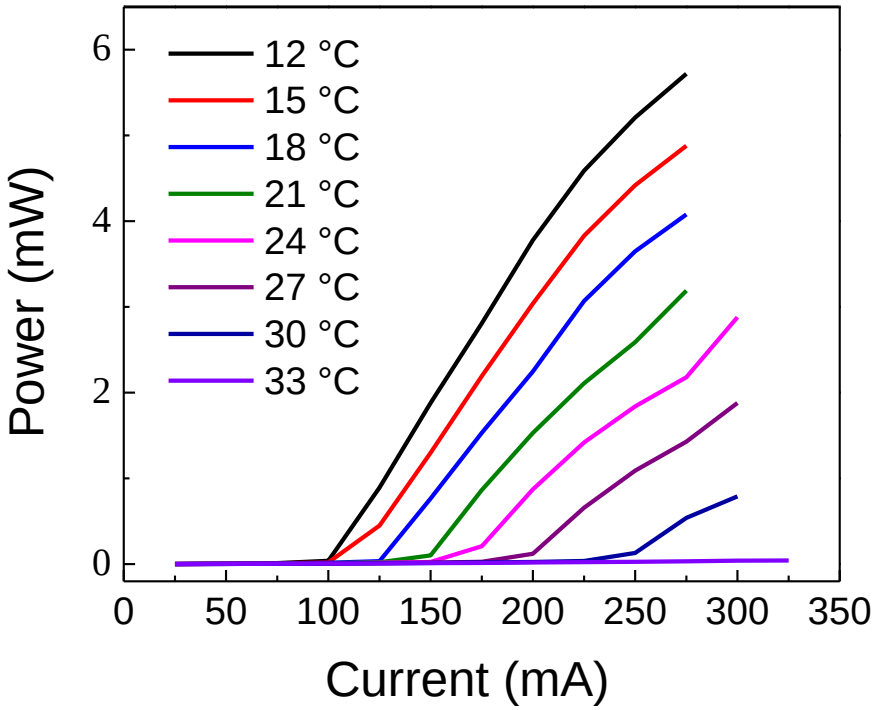


Figure 5.9. Light output versus current for temperatures up to 30 °C under CW conditions for a 3.0 mm cavity length and 20 μm width.

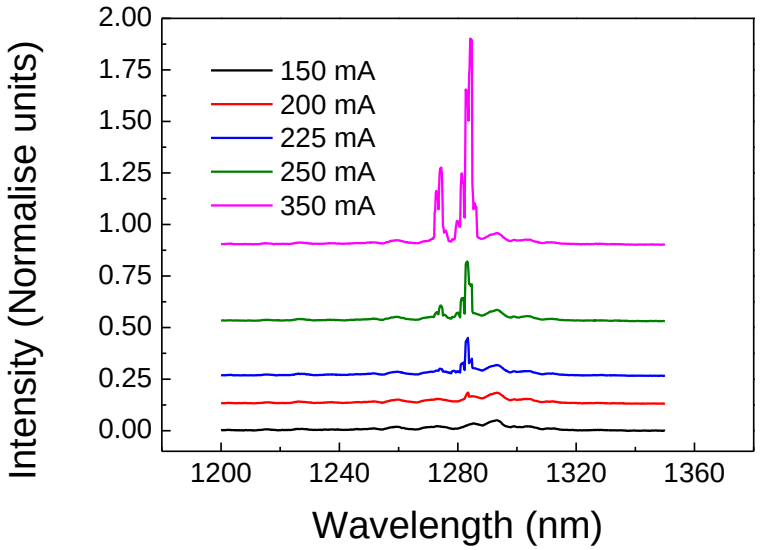


Figure 5.10. CW Spectra for 3.0 mm device at 20 °C. Spectra are shown with a cumulative 8% of intensity.

5.4.2 3. 5 mm device

Lower RT threshold current densities were observed for the 3.5-mm-long device. Figure 5.11 shows the LI measurements for a 3.5-mm device at room temperature in pulsed operation. The inset of Figure 5.11 shows an expanded view around threshold. The lasing current threshold is approximately 45 mA in pulsed mode, with a duty cycle of 0.2 % and pulse width of 1 μs. The maximum power is approximately 93 mW for an injection current of 350 mA (external quantum efficiency η_{ex}=37.5%), with no evidence of power saturation up to this current.

The threshold current density (J_{th}) under pulsed mode is as low as 64.3 A/cm^2, which corresponds to about 12.9 A/cm^2 for each of the five QD laser layers. This very low J_{th} is comparable to the best-reported values for GaAs-based InAs QD laser diodes with as-cleaved facets, such as 39 A/cm^2 for a five-QD-layer device [12], 32.5 A/cm^2 for a three-QD-layer device [13] and 10.5 A/cm^2 for a single-QD-layer device [14] and is similar to the results of lasers obtained on Ge substrates, 55 A/cm^2 [1]. The same cavity width and length is shown in CW operation in Figure 5.12. However, this leads to a significantly increased threshold current of ~114 mA (compared to 45 mA for the device measured in pulsed mode).

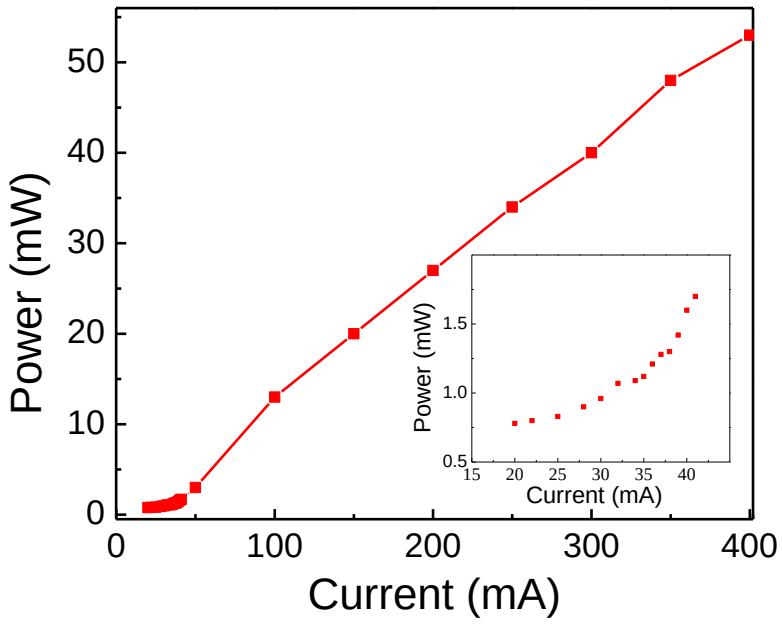


Figure 5.11. Power output versus current for 3.5mm device with 20 μm width. Inset shows enlarged image around threshold corresponding to a threshold current of ~45 mA or 64 A/cm^2.

The lasing threshold current of 114 mA corresponds to a CW threshold current of ~ 163 A/cm^2 for a device with a 3.5-mm cavity, which is much higher than the pulsed result but still significantly lower than any result to date for lasers fabricated on Si substrates by any method . For example direct growth has led to electrically pumped lasers operated in pulsed mode with lasers being demonstrated emitting at 1.05, 1.3 and 2.0 μm on Si substrates with threshold current densities 900, 725 and 900 A/cm^2 respectively [7,15, 16] or a hybrid technique such as bonding which led to a pulsed threshold current of 205 A/cm^2 [17]. A maximum output of approximately 3.7 mW at 150 mA was recorded.

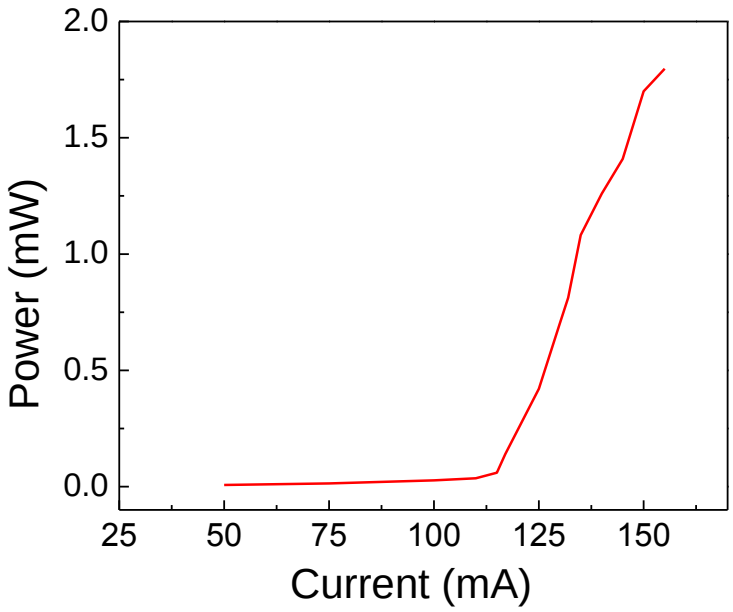


Figure 5.12. shows power versus current for 3.5 mm device under CW conditions at room temperature with threshold current ~114mA or current density ~ 163 A/cm^2.

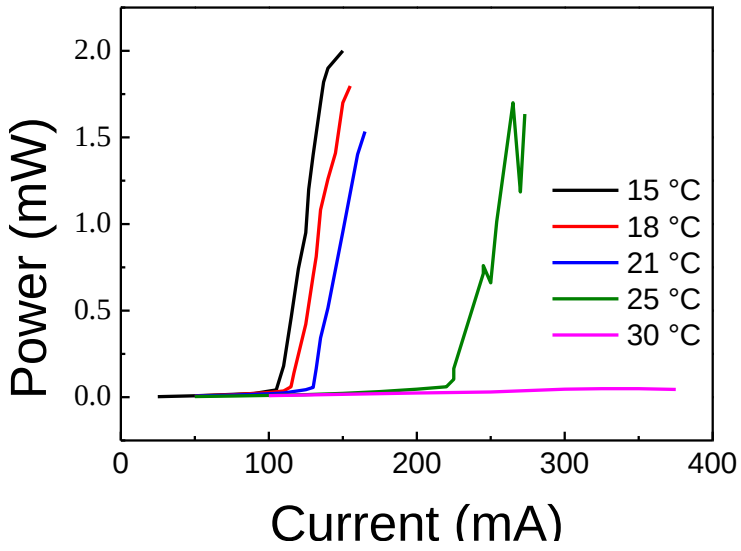


Figure 5.13. CW LI measured up to 30 °C. For an InAs/GaAs QD laser with a 3.5 mm cavity length.

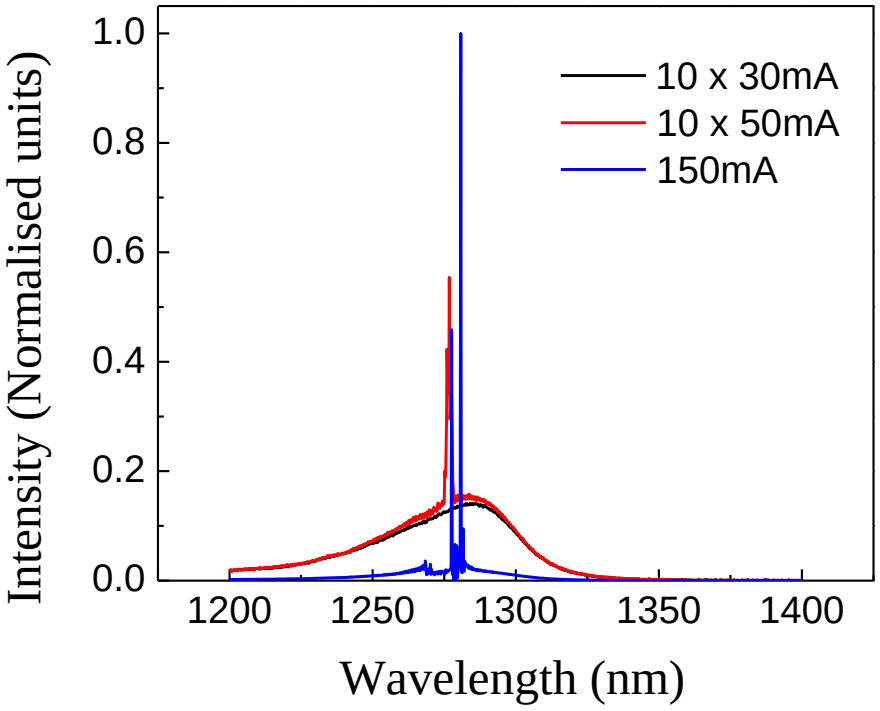


Figure 5.14. Pulsed spectra showing lasing above and below threshold for a 3.5 mm device. Intensity values for 30 and 50 mA are multiplied by 10 for convenience.

Figure 5.14 shows the spectra for devices operated in pulsed mode where a peak wavelength of 1.28 μm can be observed at a current of 50 mA. Multimode lasing spectrum appears with increasing the injection current to 150 mA. Spontaneous

emission in CW operation can be observed in Figure 5.15 at a peak wavelength of approximately 1.28 μm with a FWHM of 1.5 nm at a current of 135 mA with higher currents leading to multimode spectra and increased emission wavelength.

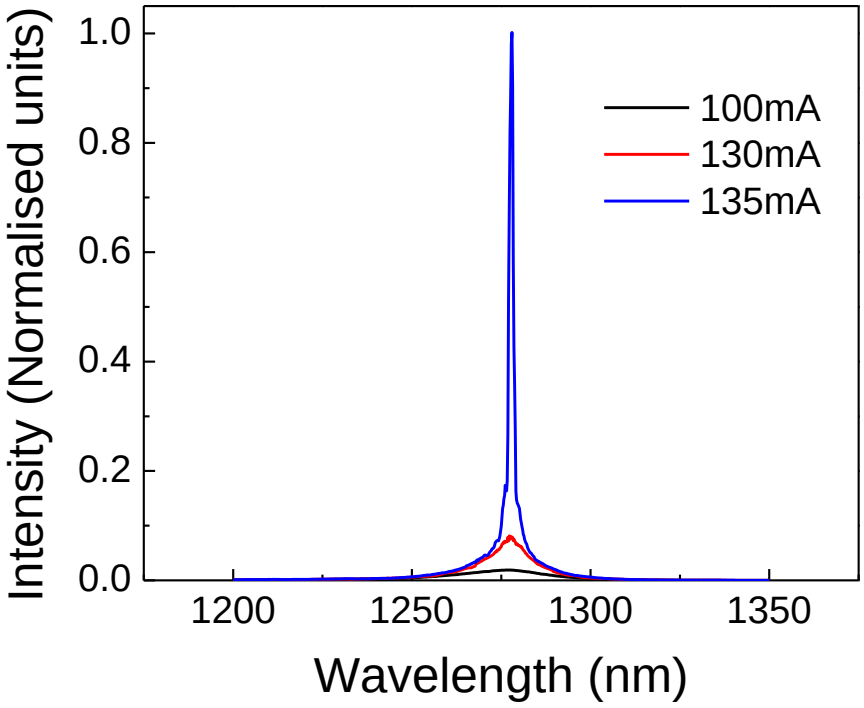


Figure 5.15 CW spectra obtained showing lasing above and below threshold current for a 3.5 mm device.

5.4.3 High Resistance of devices

The voltage/current (V-I) characteristics of 3.5-mm-long device is shown in Figure 5.16, from which it can be seen that the turn-on voltage is ~0.8 V with series resistance of ~ 5.0 Ω. This gives an explanation of why the pulsed and CW performance is significantly different as higher currents will lead to increased heating in the device, and therefore affect the device performance. Improvements to the device resistance would lead to improvements in laser performance.

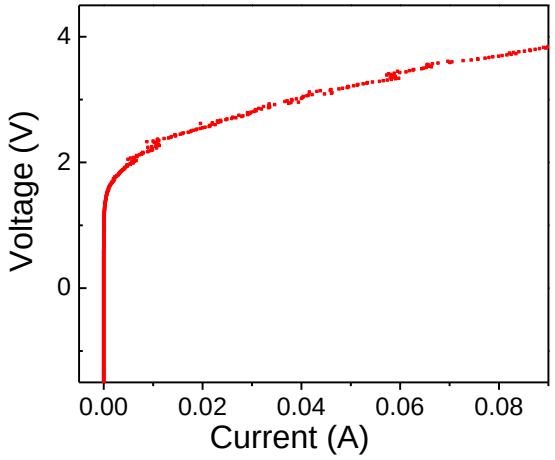


Figure 5.16 Voltage versus current for 3.5 mm device. Resistance is about 5 Ω.

5.5 Improving device performance

Threading dislocations at the interface and any defects propagating into the active layer cause an increase in the laser resistance; any defects in the active layer will additionally cause an increase in losses in the cavity and therefore an increase in the lasing threshold current. There are numerous ways which could be used to improve the resistance and defect density in the device in future investigations.

5.5.1 Wire bonding

In chapter 3 it was shown that wire bonding significantly decreased the threshold current of the laser under testing and lead to a much higher output power; in the case of GaAs lasers the power was increased by an order of magnitude. Wire bonding has the potential to lead to a similar improvement of laser properties of lasers on Ge-on-Si. Wire bonding of the devices on Ge-on-Si was attempted, but due to problems with adhesion of the SiO_2 to GaAs, and metal contact layers to SiO_2 any bonds made would result in the contacts being pulled off from the surface. Further optimisation of the SiO_2 deposition and metal deposition could improve the adhesion and allow metal bonds to be made.

5.5.2 GaAs buffer layer

The device performance could be further improved through using a low-defect-density Ge buffer layer on Si substrate and/or dislocation filter layer, such as QD dislocation filter layer used in reference [15]. In the past, techniques used have taken advantage of the built-in strain that arises from strained quantum wells or superlattices [18,19,20] causing dislocations to be bent to move parallel to the interface not propagating into the active layer. However this technique can be seriously limited by the introduction of defects form the buffer layers themselves in the strained layers. A way around this is to use defect free self-organised quantum dots. Stranski-Krastanow QDs have the capability to create large strain fields in the material they are imbedded in [21, 22] and in addition it is possible to grow multiple stacks of quantum dots which are defect free [8, 23]. Quantum dots, due to their large strain field, are able to supress defect formation in the active layers [24, 25, 26]. QD filter layers have been shown in reference [15] to reduce the threshold current of QD lasers on Si from > 1500 A/cm^2 to ~ 900 A/cm^2 for 600 × 80 μm devices under pulsed conditions.

5.5.3 Ge buffer layer

The resistive characteristics of the devices in this chapter are higher than devices fabricated on Ge [1]. This could be understood in terms of the higher defect density of (~5 × 10^6/cm^2) the Ge buffer layer on Si substrate used in this work, compared to the typical value of defect density (about 5 × 10^3/cm^2) for GaAs substrates. Advances in techniques of growth of Ge on Si have demonstrated defect densities on Si(100) approximately an order of magnitude lower than the substrates used in this chapter [27]. The work in reference [27] had defect density of 7 x 10^5 cm^{-2}. This was enabled by the use of reactive thermal chemical vapour deposition (RTCVD)[28, 29, 30] instead of the conventional CVD. In RTCVD the precursors for growth are chosen so that they will increase the surface reaction rate and therefore decrease the growth temperature required. Germanium tetrafluoride (GeF_4) was used as the Ge precursor and disilane (Si_2H_6) as the reductant gas. For a thin buffer layer of 780 nm a RMS surface roughness of 1.44 nm was shown. The use of this substrate would significantly improve both the resistance of the laser and the quality of III-V growth; improving the defect density in the active layer.

5.6 Conclusion

Due to the ever decreasing scale of Si micro-electronics, with the latest transistors from Intel being demonstrated at a size of 22nm [31], Ge epilayers are a promising alternative to Si as a p-type channel in optoelectronic integrated circuits (OEIC), because Ge has a four times larger hole mobility compared with Si [32]. Furthermore, the production of low-defect Ge-on-Si substrates is now a mature technology and high-quality Ge-on-Si substrates are commercially available [2, 33].

A standard five-layer InAs/GaAs DWELL structure was epitaxially grown on a Ge-on-Si substrate. A very low RT pulsed J_{th} of 64 A/cm^2, a CW RT J_{th} of 163 A/cm^2, RT output power of ~93 mW, and lasing up to 84 °C have been demonstrated for 20-μm-wide laser diodes with either 3.5-mm-long or 3-mm-long cavities.

Further enhancements in laser performance are expected by improving the quality of defect density on surface of Ge-on-Si and also more advanced buffer layer technology. Finally the series resistance is higher than similar devices fabricated, therefore by reducing the contact resistance of the devices further reductions in threshold current could be achieved. The demonstration of the first RT CW operated Si-based quantum-dot laser is an essential step towards the integration of III-V photonic components into OEIC.

5.7 References

[1] H. Liu, T. Wang, Q. Jiang, R. Hogg, F. Tutu, F. Pozzi, and A. Seeds, "Long-wavelength InAs/GaAs quantum-dot laser diode monolithically grown on Ge substrate," *Nature Photonics*, vol. 5, no. 7, pp. 416–419, Jun. 2011.

[2] J. Michel, J. Liu, and L. C. Kimerling, "High-performance Ge-on-Si photodetectors," *Nature Photonics*, vol. 4, no. 8, pp. 527–534, Jul. 2010.

[3] J. Liu, X. Sun, R. Camacho-Aguilera, L. C. Kimerling, and J. Michel, "Ge-on-Si laser operating at room temperature.," *Optics letters*, vol. 35, no. 5, pp. 679–81, Mar. 2010.

[4] R. E. Camacho-Aguilera, Y. Cai, N. Patel, J. T. Bessette, M. Romagnoli, L. C. Kimerling, and J. Michel, "An electrically pumped germanium laser.," *Optics express*, vol. 20, no. 10, pp. 11316–20, May 2012.

[5] "http://www.axt.com/." .

[6] "http://www.wafertech.co.uk/products/gallium-arsenide-gaas/." .

[7] T. Wang, H. Liu, A. Lee, F. Pozzi, and A. Seeds, "InAs/GaAs quantum-dot lasers monolithically grown on Si substrates," *Optics express*, vol. 19, no. 12, pp. 11381–11386, Jun. 2011.

[8] H. Y. Liu, I. R. Sellers, T. J. Badcock, D. J. Mowbray, M. S. Skolnick, K. M. Groom, M. Gutiérrez, M. Hopkinson, J. S. Ng, J. P. R. David, and R. Beanland, "Improved performance of 1.3 μm multilayer InAs quantum-dot lasers using a high-growth-temperature GaAs spacer layer," *Applied Physics Letters*, vol. 85, no. 5, p. 704, 2004.

[9] H. Y. Liu, I. R. Sellers, M. Gutiérrez, K. M. Groom, R. Beanland, W. M. Soong, M. Hopkinson, J. P. R. David, T. J. Badcock, D. J. Mowbray, and M. S. Skolnick, "Optimizing the growth of 1.3-μm InAs/InGaAs dots-in-a-well structure: Achievement of high-performance laser," *Materials Science and Engineering: C*, vol. 25, no. 5–8, pp. 779–783, 2005.

[10] H. Y. Liu, D. T. Childs, T. J. Badcock, K. M. Groom, I. R. Sellers, M. Hopkinson, R. A. Hogg, D. J. Robbins, D. J. Mowbray, and M. S. Skolnick, "High-performance three-layer 1.3-μm InAs-GaAs quantum-dot lasers with very low continuous-wave room-

temperature threshold currents," *Photonics Technology Letters, IEEE*, vol. 17, no. 6, pp. 1139–1141, Jun. 2005.

[11] M. Sugawara and M. Usami, "Quantum dot devices: Handling the heat," *Nature Photonics*, vol. 3, no. 1, pp. 30–31, 2009.

[12] F. K. Tutu, I. R. Sellers, M. G. Peinado, C. E. Pastore, S. M. Willis, a. R. Watt, T. Wang, and H. Y. Liu, "Improved performance of multilayer InAs/GaAs quantum-dot solar cells using a high-growth-temperature GaAs spacer layer," *Journal of Applied Physics*, vol. 111, no. 4, p. 046101, 2012.

[13] I. R. Sellers, H. Y. Liu, K. M. Groom, D. T. Childs, D. Robbins, T. J. Badcock, M. Hopkinson, D. J. Mowbray, and M. S. Skolnick, "1.3 μm InAs/GaAs multilayer quantum-dot laser with extremely low room-temperature threshold current density," *Electronics Letters*, vol. 40, no. 22, pp. 1412–1413, 2004.

[14] D. Deppe and K. Shavritranuruk, "Quantum dot laser diode with low threshold and low internal loss," *Electronics …*, vol. 45, no. 1, pp. 54–56, 2009.

[15] Z. Mi, J. Yang, P. Bhattacharya, and D. L. Huffaker, "Self-organised quantum dots as dislocation filters : the case of GaAs-based lasers on silicon," *Electronics Letters*, vol. 42, no. 2, pp. 1–2, 2006.

[16] J. R. Reboul, L. Cerutti, J. B. Rodriguez, P. Grech, and E. Tournié, "Continuous-wave operation above room temperature of GaSb-based laser diodes grown on Si," *Applied Physics Letters*, vol. 99, no. 12, p. 121113, 2011.

[17] K. Tanabe, K. Watanabe, and Y. Arakawa, "III-V/Si hybrid photonic devices by direct fusion bonding.," *Scientific reports*, vol. 2, p. 349, Jan. 2012.

[18] R. Fischer, D. Neuman, H. Zabel, H. Morkoç, C. Choi, and N. Otsuka, "Dislocation reduction in epitaxial GaAs on Si(100)," *Applied Physics Letters*, vol. 48, no. 18, p. 1223, 1986.

[19] S. M. Bedair, T. P. Humphreys, N. a. El-Masry, Y. Lo, N. Hamaguchi, C. D. Lamp, a. a. Tuttle, D. L. Dreifus, and P. Russell, "Defect reduction in GaAs grown by molecular beam epitaxy using different superlattice structures," *Applied Physics Letters*, vol. 49, no. 15, p. 942, 1986.

[20] M. Yamaguchi, M. Sugo, and Y. Itoh, "Misfit stress dependence of dislocation density reduction in GaAs films on Si substrates grown by strained-layer superlattices," *Applied Physics Letters*, vol. 54, no. 25, p. 2568, 1989.

[21] H. Jiang and J. Singh, "Strain distribution and electronic spectra of InAs/GaAs self-assembled dots: An eight-band study," *Phys. Rev. B*, vol. 56, no. 8, pp. 4696–4701, Aug. 1997.

[22] A. D. Andreev, J. R. Downes, D. A. Faux, and E. P. O'Reilly, "Strain distributions in quantum dots of arbitrary shape," *Journal of Applied Physics*, vol. 86, no. 1, p. 297, 1999.

[23] B. Kochman, A. D. Stiff-Roberts, S. Chakrabarti, J. D. Phillips, S. Krishna, J. Singh, and P. Bhattacharya, "Absorption, carrier lifetime, and gain in InAs-GaAs quantum-dot infrared photodetectors," *Quantum Electronics, IEEE Journal of*, vol. 39, no. 3, pp. 459–467, 2003.

[24] K. K. Linder, J. Phillips, O. Qasaimeh, X. F. Liu, S. Krishna, P. Bhattacharya, and J. C. Jiang, "Self-organized In[sub 0.4]Ga[sub 0.6]As quantum-dot lasers grown on Si substrates," *Applied Physics Letters*, vol. 74, no. 10, p. 1355, 1999.

[25] Z. Mi, P. Bhattacharya, and J. Yang, "Room-temperature self-organised In0. 5Ga0. 5As quantum dot laser on silicon," *Electronics letters*, vol. 41, no. 13, pp. 742–744, 2005.

[26] Z. I. Kazi, T. Egawa, M. Umeno, and T. Jimbo, "Growth of In[sub x]Ga[sub 1 - x]As quantum dots by metal--organic chemical vapor deposition on Si substrates and in GaAs-based lasers," *Journal of Applied Physics*, vol. 90, no. 11, pp. 5463–5468, 2001.

[27] K. Tao and J. Hanna, "Epitaxial growth of germanium-rich silicon–germanium films on Si(001) substrate by reactive thermal chemical vapor deposition," *Applied Surface Science*, vol. 282, pp. 472–477, Oct. 2013.

[28] M. Yamamoto, J. Hanna, and M. Miyauchi, "New low pressure chemical vapor deposition technique for Ge crystalline thin films," *Applied Physics Letters*, vol. 63, no. 18, p. 2508, 1993.

[29] M. Yamamoto, Y. Takada, and J. Hanna, "Selective growth of Ge in GeF4-Si2H6 system," *Applied Physics Letters*, vol. 64, no. 25, p. 3467, 1994.

[30] J. Hanna and K. Shimizu, "Low-temperature growth of polycrystalline Si and Ge films by redox reactions of Si2H6 and GeF4," *Journal of Organometallic Chemistry*, vol. 611, no. 1–2, pp. 531–536, 2000.

[31] K. J. Kuhn, M. D. Giles, D. Becher, P. Kolar, A. Kornfeld, R. Kotlyar, S. T. Ma, A. Maheshwari, and S. Mudanai, "Process Technology Variation," *Electron Devices, IEEE Transactions on*, vol. 58, no. 8, pp. 2197–2208, 2011.

[32] G. Brammertz, M. Caymax, M. Meuris, and M. Heyns, "GaAs on Ge for CMOS," *Thin solid films*, vol. 517, no. 1, pp. 148–151, Nov. 2008.

[33] T. Akatsu, C. Deguet, L. Sanchez, F. Allibert, D. Rouchon, T. Signamarcheix, C. Richtarch, A. Boussagol, V. Loup, F. Mazen, J.-M. Hartmann, Y. Campidelli, L. Clavelier, F. Letertre, N. Kernevez, and C. Mazure, "Germanium-on-insulator (GeOI) substrates—A novel engineered substrate for future high performance devices," *Materials Science in Semiconductor Processing*, vol. 9, no. 4–5, pp. 444–448, Aug. 2006.

Chapter 6: Conclusion

6.1 Introduction

The aim of this work was to produce high-performance III-V lasers on Si platform with low threshold currents. InAs/InGaAs Dot-in-well (DWELL) laser diode structures were fabricated both on Si and Ge-on-Si substrates.

In chapter 2 the laser fabrication process is described. And in chapter 3, the process was optimised paying special attention to the process of metallisation, and mounting and wire bonding.

In chapter 4 lasers were fabricated on a Si substrate using a GaAs nucleation layer. By using a new device structure and by optimising the growth temperature of the initial nucleation layer and thickness of low temperature growth layers, a CW electrically pumped laser on Si around room temperature was demonstrated. Furthermore the use of a 5-nm AlAs nucleation layer instead of the previous GaAs nucleation layer led to an improvement in the threshold current density compared to previous work [1]. Due to the strong bonding strength of Al in AlAs defects were confined in the interface between Si and GaAs.

In chapter 5 lasers were grown on Ge-on-Si substrates. As Ge has a low lattice mismatch between GaAs it is relatively straightforward to grow lasers on Ge [2]. By growing a thin layer of Ge onto a Si, a virtual substrate is created which has the advantages of Ge combined with Si. These lasers had the lowest pulsed threshold

current density at time of writing this thesis of any laser grown on a Si substrate at 64 A/cm^2. The laser of chapter 5 also was shown to have a low CW threshold current density of 164 A/cm^2, which is considerably lower than the previous, albeit pulsed, lasing result of 205 A/cm^2 [3].

6.2 Further improvements

6.2.1 Miscut Si

Currently all growth in this thesis has been done on miscut substrates in order to reduce formation of threading dislocations [4-6]. However given the end goal of this research, to integrate lasers with CMOS technology, it would be desirable to be able to grow laser structures on Si(100) with no miscut. This has been attempted by other groups, but with results limited to light-emitting diodes (LEDs) [7]. To date no laser has been grown on non-miscut Si.

6.2.2 Device size

So far only broad-area lasers have been fabricated with 20- and 50-μm cavity widths and with relatively long cavities of 2 mm to 3.5 mm. Narrow ridge lasers have many advantages over broad area lasers, for example lower heating in the active region. Also a narrow ridge allows a single mode laser to be fabricated, which is highly desirable in the communications field.

6.2.3 P-type modulation doping

P-type modulation doping of the active layer was first predicted in the late 1980's to improve the characteristic temperature of QD lasers [8]. It is analysed in more detail in Ref. 9 and recently p-type modulation has produced lasers with very high characteristic temperatures above 650 K for temperatures up to 80 °C [10]. It would be expected that this technique can be used on lasers on Si, Ge or Si-on-Ge to also improve the characteristic temperature of devices fabricated at UCL. Laser structures at UCL have already been grown and currently are being fabricated at the LCN cleanroom. Results would be expected shortly for lasers grown on Ge. Ge has been chosen as it has a lower defect density and lower threshold currents than current lasers fabricated on Si, but still has some of the material issues associated with growing on Si such as the formation of APDs.

6.2.4 Reduction of defects

In this work only quantum well buffer layers were used to filter out threading dislocations. Other work has shown quantum dot filter layers to more effectively reduce the density of threading dislocations in the active regions of lasers [11]. This technique should be carefully optimised as the QDs can introduce defects themselves. Also annealing of samples in the past has shown to reduce defect densities.

6.2.5 Series resistance improvement of contacts

Problems affecting the cleanroom at UCL have led to lasers being fabricated with higher than expected series resistances, particularly in the case of the Ge-on-Si lasers in chapter 4, where the resistance was considerably higher than a typical GaAs device and also higher than a device on Si. A reduction in series resistance would lead to a lower threshold current. Also, lower currents would have the additional affect to reduce Ohmic heating (which is equal to I^2/R) in the device and therefore allow higher temperature operation and lead to a smaller difference between pulsed and CW threshold currents.

6.2.6 Lifetime tests

Once devices with reasonable threshold currents at both pulsed and CW operation are fabricated, it will be useful to test lifetimes to see how the output power scales over time, as any device in an OEIC will be required to operate for long periods of time in order to make it cost effective.

6.2.7 Integration

QD lasers integrated with other photonic components have already been demonstrated such as grove-coupled modulators [12]. As a start, a more simple structure, such as a laser with an integrated waveguide could be fabricated. This would remove the need for regrowth in the MBE chamber, which risks contamination of the growth chamber. Further work would need to be done to design a mask set to allow the fabrication an integrated structure. Also the facets could no longer be produced by cleaving, so FIB etching would be required.

6.2.8 Dry etching

Currently in the fabrication process, the ridges have been etched via wet etching. Dry etching would allow greater control over etch depth and lead to more uniform etching, with near vertical walls and flat profiles [13]. This would lead to a more consistent etch, and therefore greater yield of devices, as wet etching results in range of etch depths across a sample, where the edges are etched more than the centre.

6.2.9 Wire and die bonding

Currently lasers have been tested on a heat sink without any bonding. Bonding the lasers onto a heat sink using either solder or indium paste would lead to a better thermal conductivity, which would allow heat from the device to be more quickly conducted away. This would improve the temperature and CW operation of devices. Wire bonding would also improve the device performance as it would allow the current to be more evenly distributed across the device as currently lasers are tested using a single probe per contact.

6.2.10 High reflectivity coating

High reflectivity (HR) coating on facets is a well-established technique to improve gain in a device and therefore decrease the threshold current density [14], [15]. This is because it acts to increase the reflectivity of facets of a laser.

6.2.11 Gain measurements

Optimising gain in the laser structure is also important as the amount of gain in a cavity dictates the threshold current. By taking gain measurements this would allow this optimisation, however these have measurement have not been taken yet due to limitations of the experimental setup and time constraints which prohibited the design of a new mask.

References

[1] T. Wang, H. Liu, A. Lee, F. Pozzi, and A. Seeds, "1.3-μm InAs/GaAs quantum-dot lasers monolithically grown on Si substrates," *Optics express*, vol. 2936, no. 2003, pp. 2931–2936, 2011.

[2] H. Liu, T. Wang, Q. Jiang, R. Hogg, F. Tutu, F. Pozzi, and A. Seeds, "Long-wavelength InAs/GaAs quantum-dot laser diode monolithically grown on Ge substrate," *Nature Photonics*, vol. 5, no. 7, pp. 416–419, Jun. 2011.

[3] K. Tanabe, K. Watanabe, and Y. Arakawa, "III-V/Si hybrid photonic devices by direct fusion bonding.," *Scientific reports*, vol. 2, p. 349, Jan. 2012.

[4] A. Jallipalli, M. Kutty, G. Balakrishnan, J. Tatebayashi, N. Nuntawong, S. Huang, L. Dawson, D. Huffaker, Z. Mi, and P. Bhattacharya, "1.54 lm GaSb/AlGaSb multi-quantum-well monolithic laser at 77K grown on miscut Si substrate using interfacial misfit arrays," *Electronics Letters*, vol. 43, no. 22, 2007.

[5] J. Tatebayashi, A. Jallipalli, M. N. Kutty, S. Huang, K. Nunna, G. Balakrishnan, L. R. Dawson, and D. L. Huffaker, "Monolithically Integrated III-Sb-Based Laser Diodes Grown on Miscut Si Substrates," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 15, no. 3, pp. 716–723, 2009.

[6] K. Morizane, "Antiphasedomain structures in GaP and GaAs epitaxial layers grown on Si and Ge," *Journal of Crystal Growth*, vol. 38, no. 2, pp. 249–254, 1977.

[7] G. Balakrishnan, M. Mehta, M. N. Kutty, P. Patel, A. R. Albrecht, P. Rotella, S. Krishna, L. R. Dawson, and D. L. Huffaker, "Monolithically integrated III-Sb CW super-luminal light emitting diodes on non-miscut Si (100) substrates," *Electronics Letters*, vol. 43, no. 4, pp. 244–245, 2007.

[8] Y. Takahashi, T Arakawa, "Theoretical analysis of gain and dynamic properties of quantum-well box lasers," *Optoelectronics*, vol. 3, no. 2, p. 155, 1988.

[9] O. B. Shchekin and D. G. Deppe, "1.3 μm InAs quantum dot laser with T[sub o]=161 K from 0 to 80°C," *Applied Physics Letters*, vol. 80, no. 18, p. 3277, 2002.

[10] S. S. Mikhrin, A. R. Kovsh, I. L. Krestnikov, A. V. Kozhukhov, D. A. Livshits, N. N. Ledentsov, Y. M. Shernyakov, I. I. Novikov, M. V. Maximov, V. M. Ustinov, and Z. I. Alferov, "High power temperature-insensitive 1.3 μm InAs/InGaAs/GaAs quantum

dot lasers," *Semiconductor Science and Technology*, vol. 20, no. 5, pp. 340–342, May 2005.

[11] Z. Mi, J. Yang, P. Bhattacharya, and D. L. Huffaker, "Self-organised quantum dots as dislocation filters : the case of GaAs-based lasers on silicon," *Electronics Letters*, vol. 42, no. 2, pp. 1–2, 2006.

[12] P. Bhattacharya and J. Yang, "Groove-coupled InGaAs/GaAs quantum dot laser/waveguide on silicon," *Lightwave Technology, Journal of*, vol. 25, no. 7, pp. 1826–1831, 2007.

[13] K. Hikosaka, T. Mimura, and K. Joshin, "Selective Dry Etching of AlGaAs-GaAs Heterojunction," *Japanese Journal of Applied Physics*, vol. 20, no. 11, pp. L847–L850, 1981.

[14] D. Deppe, S. Freisem, and G. Ozgur, "Very low threshold current density continuous-wave quantum dot laser diode," *Semiconductor Laser*, pp. 33–34.

[15] H. Y. Liu, D. T. Childs, T. J. Badcock, K. M. Groom, I. R. Sellers, M. Hopkinson, R. A. Hogg, D. J. Robbins, D. J. Mowbray, and M. S. Skolnick, "High-performance three-layer 1.3-μm InAs-GaAs quantum-dot lasers with very low continuous-wave room-temperature threshold currents," *Photonics Technology Letters, IEEE*, vol. 17, no. 6, pp. 1139–1141, Jun. 2005.