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Low-Power Low-Voltage Analogue-to-Digital Converter Design for Mobile Video and Wireless Applications

By

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Abstract

With the rapid embracing and deployment of Wideband Code Division Multiple Access (WCDMA)-based Third Generation (3G) mobile networks [1] in Europe and East Asia and with the ratification of the Digital Video Broadcast – Handheld (DVB-H) - terrestrial television for battery-powered mobile devices standard in Europe [2], minimization of hand-set power consumption is becoming a key requirement. Higher baseband bandwidth is necessary for these enhanced wireless and mobile broadcast services, which translates to an increase in battery power utilization over existing second generation (2.xG) technology-enabled devices.

The Analogue-to-Digital Converter (ADC) that does the transformation of received analogue baseband signals to the digital domain for digital demodulation and data extraction consumes some portion of the receiver front-end power budget and its minimization will contribute significantly to overall elongation of mobile device battery life. This research focuses on the design of power-efficient Nyquist and Over-sampled ADCs for DVB-H and GSM/WCDMA applications with the specific contributions to knowledge being the determination of optimal partitioning of pipeline ADCs for low power consumption, novel sampling switch linearization circuit for use in the design of high dynamic range Delta-Sigma ($\Delta\Sigma$) ADCs and novel power and area efficient background calibration schemes for low-voltage high-speed 12-bit and higher resolution pipeline ADCs. A number of silicon devices were designed and fabricated (or in the process of fabrication) in the course of the research viz.

- A 10-bit 20.48 MS/s 1.5 V optimally partitioned pipeline ADC silicon in 0.35 μm CMOS technology for mobile DVB-H with measured results showing only 19 mW power consumption, 100 MHz Effective Resolution Bandwidth (ERBW), 56 dB Signal-to-Noise Ratio (SNR), 60 dB Spurious Free Dynamic Range (SFDR) and an ultra-low 0.19 pJ/conversion energy consumption, one of the lowest reported for a measured device in the literature.
- A 13-bit 26 MS/s 135 kHz bandwidth, 2.7 V switched-capacitor $\Delta\Sigma$ ADC silicon in 0.35 μm BiCMOS technology for GSM frequencies with linearised sampling switch, achieving measured performance of 85.8 dB SFDR, 83.5 dB SNR and consuming 7 mW.
- An 11-bit 153.6 MS/s 1.92 MHz bandwidth, 2.7 V switched-capacitor $\Delta\Sigma$ ADC silicon in 0.35 μm BiCMOS technology for WCDMA frequencies with linearised

sampling switch, achieving measured performance of 76.9 dB SFDR, 72 dB SNR and consuming 14 mW.

- A 12-bit 120 MS/s 1.2 V pipeline ADC with novel digital background calibration in 0.12 μm CMOS technology with over 85.5 dB simulated SFDR, 72.1 dB simulated SNR and consuming an estimated 100 mW.

Acknowledgements

I still can remember that day in the latter part of 2001 when I accosted Dr. Robin Miller, my then Manager and asked about the possibility of working part-time on my PhD and my employer, Sony UK partly sponsoring me. It was however a pyrrhic victory when the PhD approval eventually came but the group I was working for had ceased to exist and Dr. Miller no longer in Sony to hear the news. Many thanks however, to him for all his effort to make it all happen and to Trisha Western, our then Human Resources Manager for authoring all the required paperwork and contracts. I could then begin the search for a suitable university and finally ended up in November 2002 with a young dynamic analogue integrated circuit design research group in University College London (UCL) headed by Dr. Andreas Demosthenous after a series of interviews.

I am also very grateful to Dr. Chris Clifton, our then Director of Wireless Technologies who actually took time off his busy schedule to visit UCL with me in order to chart out my progress path and agree a research focus. His advice on my focusing on ADC research was visionary as little would we have known then how the dependency of telecommunication and broadcast sub-systems on data converters will increase with the incessant shrink in device geometry.

Appreciation also goes to Murakami-san, Managing Director of the Sony UK Semiconductor Design Centre, Tanabe-san, my present Manager and General Manager of Wireless IC products, Dr. Sam Atungsiri, Consultant DSP Engineer and one of my industrial supervisors, Dr. Randeep Soin (my other industrial supervisor and a former Sony employee), Kawasaki-san (my former Manager) and Anthony Eaton (my former Manager and a former Sony employee) for all their support during the research period. In addition, Sony SDC is much appreciated for partly funding the research and for creating a stimulating environment for research work.

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Glossary of Terms

3-D	3-Dimensional
3GPP	3rd Generation Partnership Project
8-PSK	8-Phase Shift Keying
AC	Alternating Current
ACL	Closed Loop Gain
ADC	Analogue-to-Digital Converter
ADSL	Asymmetric Digital Subscriber Line
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AMC	Adaptive Modulation and Coding
AMPS	Advance Mobile Phone Service
AOL	Open Loop Gain
BBIC	Baseband Integrated Circuit
BER	Bit Error Rate
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BW	Bandwidth
CDMA	Code Division Multiple Access
CEPT	Conference of European Posts and Telegraphs
CIC	Cascaded Integrator Comb
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
C/N	Carrier-to-Noise Ratio
COFDM	Coded Orthogonal Frequency Division Multiplexing
CS	Circuit Switched
CSI	Channel State Information
CT	Continuous Time
DAC	Digital-to-Analogue Converter
D-AMPS	Digital Advance Mobile Phone Service
dBFS	dB Full-Scale
DC	Direct Current
DEM	Dynamic Element Matching
DFT	Discrete Fourier Transform

DNL	Differential Nonlinearity
D-QPSK	Differential Quadrature Phase Shift Keying
DR	Dynamic Range
ΔΣ	Delta-Sigma
DT	Discrete Time
DTT	Digital Terrestrial Television
DTV	Digital Television
DVB	Digital Video Broadcast
DVB-C	Digital Video Broadcast, Cable
DVB-H	Digital Video Broadcast, Handheld
DVB-S	Digital Video Broadcast, Satellite
DVB-T	Digital Video Broadcast, Terrestrial
DWA	Data Weighted Averaging
E-DCH	Uplink Enhanced Dedicated Channel
EDGE	Enhanced Data rates for Global Evolution
E-GSM	Enhanced Global System for Mobile communications
ELG	European Launching Group
ENOB	Effective Number of Bits
ERBW	Effective Resolution Bandwidth
ETSI	European Telecommunication Standards Institute
EVM	Error Vector Magnitude
FDM	Frequency Division Multiplexing
FDMA	Frequency Division Multiple Access
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FOM	Figure of Merit
FPGA	Field Progammable Gate Array
GaAs	Gallium Arsenide
GBW	Gain Bandwidth Product
GMSK	Gaussian-filtered Minimum Shift Keying
GPRS	General Packet Radio Services
GSM	Groupe Spécial Mobile
GSM	Global System for Mobile communications

HDTV	High Definition Television
HSDPA	High Speed Downlink Packet Access
HS-DSCH	High-Speed Downlink Shared Channel
HSUPA	High Speed Uplink Packet Access
I	In-phase
ICI	Inter-Channel Interference
IF	Intermediate Frequency
ILA	Individual Level Averaging
INL	Integral Nonlinearity
$\hat{I}_{or}$	Total WCDMA received power spectral density at antenna
IP	Internet Protocol
ISDN	Integrated Services Digital Network
ISI	Inter-Symbol Interference
LMS	Least Mean Square
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MDAC	Multiplying Digital-to-Analogue Converter
MHP	Multimedia Home Platform
MiM	Metal-insulator-Metal
MOS	Metal Oxide Semiconductor
MoU	Memorandum of Understanding
MP3	Motion Picture expert group-1, audio layer 3
MPEG	Motion Pictures Expert Group
MSB	Most Significant Bit
MTBF	Mean-Time-Between-Failure
NF	Noise Figure
NICAM	Near Instantaneous Companded Audio Multiplex
nMOS	*n*-channel Metal Oxide Semiconductor
NMT	Nordic Mobile Telephone
NTF	Noise Transfer Function
OFDM	Orthogonal Frequency Division Multiplexing
OOB	Out of Band

Opamp	Operational Amplifier
OSR	Over-Sampling Ratio
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PiP	Poly-insulator-Poly
PLL	Phase Locked Loop
PM	Phase Margin
pMOS	*p*-channel Metal Oxide Semiconductor
PN	Pseudo Noise
PS	Packet Switched
PSK	Phase Shift Keying
Q	Quadrature
QAM	Quadrature Amplitude Modulation
QPSK	Quaternary Phase Shift Keying
RAM	Random Access Memory
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RMS	Root Mean Square
RRC	Root-Raised-Cosine
RS	Reed Solomon
SAR	Successive Approximation Register
SAW	Surface Acoustic Wave
SC	Switched Capacitor
SF	Spreading Factor
SFDR	Spurious Free Dynamic Range
SFN	Single Frequency Network
SHA	Sample-and-Hold Amplifier
SiGe	Silicon Germanium
SiP	System-in-a-Package
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
$SN_{th}R$	Signal-to-Thermal Noise Ratio
SoC	System-on-a-Chip

SQNR	Signal-to-Quantization Noise Ratio
SR	Slew Rate
STF	Signal Transfer Function
TACS	Total Access Communication System
TDMA	Time Division Multiple Access
THD	Total Harmonic Distortion
TS	Transport Stream
UHF	Ultra High Frequency
UMTS	Universal Mobile Telecommunications System
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency
WCDMA	Wideband Code Division Multiple Access

1 Introduction

"The entrance of thy words giveth light; it giveth understanding unto the simple" Ps. 119:130 KJV

1.1 Historical Overview of Digital Communication Systems

Historically, some form of wireless communication has been essential to the very existence of humans and animals alike. The bees for example do a dance (visual communication) to alert other bees to the presence of nectar. Monkeys make a whoopee sound (auditory communication) when they have found food. In the pre-historic times predating what we know now as wireless communication, human beings communicated by means of fire, smoke and drums or by the use of emissaries (a precursor of the structured ubiquitous and archetypal national postal systems). The race between wire-line and wireless communication development was in a sense neck to neck with Samuel Morse, a painter perfecting the Morse code (a variable-length ternary code [3]) and telegraph in 1837, which was then used in 1844 to send the first telegraph message between two American cities. By 1864, James Clerk Maxwell had formulated the electromagnetic theory and inferred the existence of radio waves using the well-known Maxwell equations, which were verified experimentally by Heinrich Hertz in 1887. By 1875, Alexander Graham Bell had invented the wire-line telephone with Almon Brown Strowger's automatic electromechanical switch replacing the erstwhile manual telephone exchange in 1897.

But it was not until Guglielmo Marconi received the first transatlantic wireless transmission in St. Johns, Newfoundland on December 12, 1901 from Poldhu, Cornwall, England, 2100 miles away [4] that communication transcended geographical and continental boundaries. John Ambrose Fleming, then Professor of Electronic Engineering at University College London and a consultant to British Marconi designed the equipment used by Marconi and invented the vacuum tube diode in 1904 paving the way for transcontinental telephony and the dawn of analogue wireless communication in 1913.

Edwin Howard Armstrong invented the super-heterodyne receiver in 1918 (the architecture is still in use today in various guises) paving the way for commercial radio and television broadcast reception. Harry Nyquist's classic and visionary 1928 paper [5] on the correct reception of telegraph signals in dispersive media eventually became the bedrock of digital communication in the future. With better understanding of the nature of wireless signals and the characteristics of the transmission channel, many researchers invented

modulation schemes, optimal reception channel filters, and complex schemes for the representation of baseband signals with the World War II acting as the major catalyst for the then ground-breaking advancements in telecommunications.

By 1948, Jean Claude Shannon established the theoretical foundations of digital communications with his classic paper on the mathematical theory of communication [6], showing that data rate could be increased ad infinitum without affecting the probability of error so long as the data rate was still within the channel capacity, a startling revelation at that time. This was followed by significant research in coding theory and the development of various error correcting codes in order to reach Shannon's theoretical channel capacity limit and thus, allow efficient communication and channel bandwidth utilization.

The solid-state transistor then came into the picture in 1948 when three Bell Laboratory scientists invented it [7] (for which they received the 1956 Nobel Prize in Physics). This stimulated innovation in other quarters with Robert Noyce of National Semiconductors inventing the planar integrated circuit in 1958. Noyce's patent was five months later than Texas Instrument's Jack Kilby's monolithic integrated circuit invention but Noyce's planar technique became commercially dominant. This spawned numerous analogue integrated circuits, logic and memory chips as well as single-chip microprocessors, thus making digital signal processing suddenly fast, power-efficient and affordable - completely transforming the digital communication landscape forever.

The availability of microprocessors naturally led to the development of personal computers, packet switching, computer networks and the Arpanet (1971). This was later renamed the Internet in 1985 and commercialized in 1994 after the invention of hyper-text transport protocol (http), hyper-text markup language (html) and the world wide web (www) caused an astronomical explosion in the Internet's usage and popularity.

From the invention of the television in 1926 by John Logie Baird [8] to the late 1980s, analogue terrestrial broadcast was vogue. This was however plagued by reception problems as a result of multi-path, interference and fading issues, thus motivating research into the possibility of terrestrial digital broadcast. Commercial digital video broadcast was eventually achieved in the late 1990s largely as a result of work done by the Digital Video Broadcast (DVB) working group [1] since September 1993. Cable (DVB-C) and satellite (DVB-S) media were initially used for digital broadcast with the extension to the terrestrial transmission channel (DVB-T) as soon as digital modulation schemes and encoding algorithms were robust enough to address the issues that originally affected analogue

terrestrial broadcast. The first DVB-T commercial service was launched in the United Kingdom in November 1997.

Mobile communications on the other hand had its roots in military communication with point-to-point analogue modulation based radios already in use by World War II. Multi-point 1st generation analogue mobile communication was finally commercialized in the mid eighties with the Advance Mobile Phone Service (AMPS) system in use in the United States and Asia, the Total Access Communication System (TACS) in the United Kingdom and the Nordic Mobile Telephone (NMT) system in use in Scandinavia. By 1992, Europe had gone digital with the 2nd generation TDMA-based Global System of Mobile Communication (GSM) and America following suit with D-AMPS. Japan also introduced IS-95, a form of CDMA in the mid nineties. By the late nineties, packet switching was in use with the introduction of General Packet Radio Services (GPRS) and Enhanced Data rates for Global Evolution (EDGE), 2.5G enhancements to GSM, which is still in use in over 200 countries and by almost two billion subscribers worldwide [9].

While subscribers were experiencing the multimedia messaging benefits of the 2.5G services, the 3rd Generation Partnership Project (3GPP) was already scoping out a Universal Mobile Telecommunication System (UMTS) that would use some form of CDMA and provide high data-rates with efficient use of bandwidth. This has now been deployed in parts of Europe, Asia and America and with Mbps data rates using High Speed Downlink Packet Access (HSDPA) and video streaming capability, is poised to completely eclipse GSM in the near future.

As it became apparent that the evolution of mobile handset design was inevitable, (with high-resolution colour displays and cameras becoming commonplace on lighter, smaller and more power efficient phones), the DVB consortium in the early 21st century mulled over the possibility of deploying robust digital terrestrial television for battery-powered mobile devices with guaranteed reception even at high speeds. DVB-Handheld (DVB-H) was then developed and standardized in 2004 and is similar to DVB-T with the broadcast data transmitted as IP packets (to allow for time-slicing at the receiver for power consumption reduction) and a novel Forward Error Correction (FEC) algorithm developed to aid robust reception at high velocities. Trials have actually been done at close to Mach-1 speeds with excellent reception quality [10] and 2006 will be the year that will revolutionize the traditional ways in which multimedia, music, radio and television are enjoyed. The power-efficient WCDMA/DVB-H/MP3/Camera-phone will thus be where all these cutting edge developments in wireless communication will eventually converge.

1.2 Motivation for the Research Work

For the subscriber to receive voice, video, broadcast and data, content depictive of the previously outlined advancements in digital wireless communication, a suitable tuner or receiver front-end is required. Fig. 1.1 is a simplified diagram of a direct conversion receiver/tuner used for DVB-H reception. The surface acoustic wave (SAW) filter is used to steeply reject RF signals within the immediate vicinity of the wanted signal band. The low noise amplifier (LNA) amplifies the received signal whilst adding little noise in the process. The phase locked loop (PLL) generates the RF waveforms for use in the in-phase (I) and quadrature (Q) paths of the receiver. The mixer translates the RF input signal directly to baseband. Additional band-limiting is done using an integrated channel filter and an automatic gain control (AGC) loop used to further amplify the wanted signal. Finally, the I/Q analogue-to-digital converters (ADCs) convert the I/Q channel outputs to the digital domain for subsequent digital signal processing and extraction of the transmitted MPEG2 audio and video program.

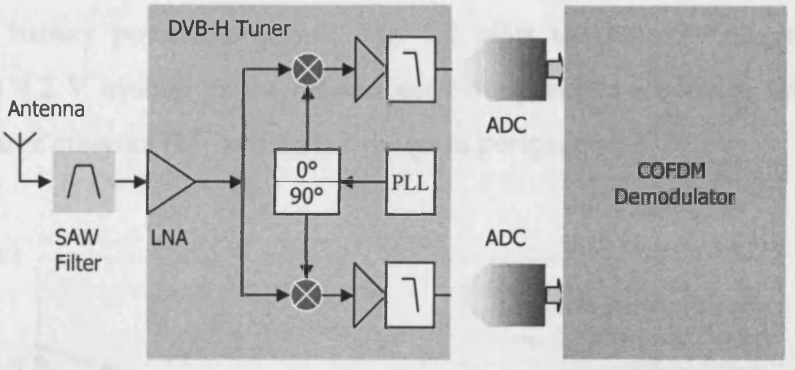


Fig. 1.1 Simplified block diagram of a direct conversion tuner for DVB-H reception.

In the days of analogue wireless communication, the demodulated analogue baseband output was the desired information. For digital wireless communication, the traditional modulation schemes are only used as bearers of the encoded packetised digital data. The analogue baseband output still needs to be accurately translated to the digital domain with adequate Signal-to-Noise Ratio (SNR) to facilitate digital demodulation, error correction and decoding of the transmitted packets. And this is where the ADC comes into the picture. The ADC's noise floor must be such that its effect on the input baseband signal's Carrier-to-Noise Ratio (C/N) is negligible. In addition, the use of a high dynamic range ADC eases the complexity of the analogue channel filter design and eliminates the need for trimming or

calibration of the baseband filter characteristics whilst translating additional filtering requirement to the digital domain where it can be done more precisely and efficiently.

Table 1.1 is the representative breakdown of power consumption for the individual blocks comprising a typical DVB-T/H tuner and demodulator subsystem [11]-[16].

Table 1.1 Power Consumption Break-down for DVB-T Demodulator Subsystem.

References	Blocks	Power Consumption (mW)
[11]	LNA & RF Filter	21
[12]	Mixer, VCO & PLL	47
[13]	I and Q AGC	65.4
[14]	I and Q Baseband Filter	50
[15]	I and Q ADCs	120
[16]	Digital Demodulator	307

It can thus be seen that the ADC power consumption is a sizeable portion of the overall power budget. Hence, if low-power techniques can be developed and used for the design of the ADCs the DVB-T subsystem's consumption will reduce, immediately translating to mobile device battery power elongation. Fig. 1.2 plots the battery voltage of a 1.5 Ah (Ampere-hour) 4.2 V mobile phone lithium-ion battery versus discharge time for various constant discharge currents [17] to help put things in perspective.

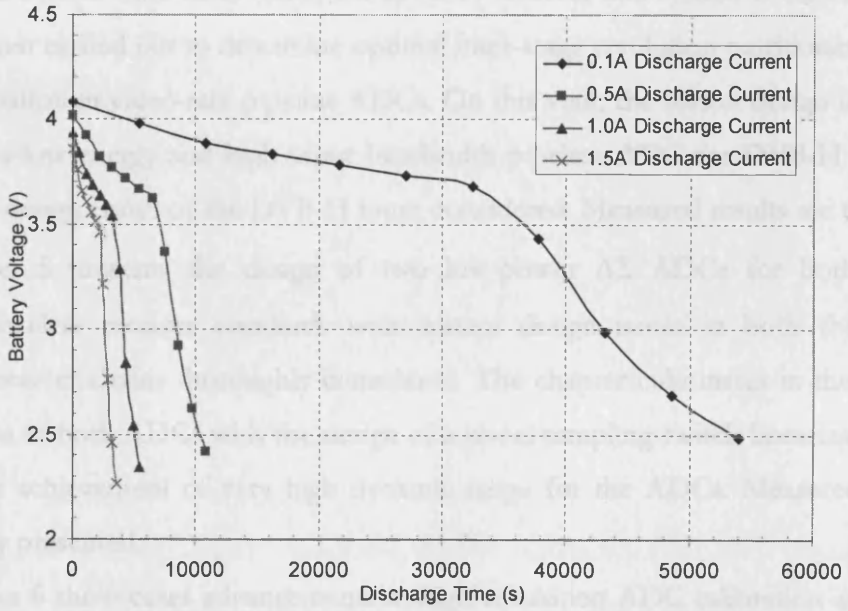


Fig. 1.2 Discharge profile of a 4.2 V 1.5 Ah lithium-ion battery.

This research thus focused on the minimization of power consumption in video-rate pipeline ADCs by the optimization of inter-stage resolution partitioning, the design of a novel switch linearization circuit to address sampling switch linearising issues affecting low-power switched-capacitor ΔΣ ADCs and the development of low power and low silicon overhead calibration schemes for high-speed and high-resolution pipeline ADCs. The research spawned four silicon devices in total with the designs done using CMOS and BiCMOS 0.35μm and 0.12μm process technologies and easily portable to lower geometry technologies.

1.3 Thesis Organization

The thesis is made up of seven chapters. Chapter 2 reviews ADC fundamentals with properties of quantization noise examined, ADC terminologies explained and ADC testing methodologies described.

Chapter 3 goes further, with all available ADC architectures presented and described in detail. The trade-offs between architectures is explained and data presented to illustrate the resolution versus power consumption versus sampling speed segments that the various architectures fall into; a useful means of determining the appropriate architecture to use for a given wireless communication or broadcast receiver subsystem design.

In Chapter 4, the cost benefit of a multiple-die System-in-a-Package (SiP) solution over a monolithic System-on-a-Chip (SoC) for DVB-H receiver sub-system is stated. Systematic analysis is then carried out to determine optimal inter-stage resolution partitioning for lowest power dissipation in video-rate pipeline ADCs. On this vein, the silicon design of a reduced-voltage, ultra-low energy and high input bandwidth pipeline ADC for DVB-H is presented with system design issues of the DVB-H tuner considered. Measured results are then shown.

Chapter 5 presents the design of two low-power ΔΣ ADCs for both GSM and WCDMA wireless receiver standards with system design issues in both the GSM and WCDMA receiver chains thoroughly considered. The chapter culminates in the system and circuit design of both ADCs with the design of a novel sampling switch linearization scheme enabling the achievement of very high dynamic range for the ADCs. Measured results are subsequently presented.

Chapter 6 show-cases advancements in high-resolution ADC calibration and proposes two equivalent low-power background calibration scheme for high-speed high-resolution pipeline ADCs. Circuit design of a background calibrated 12-bit pipeline ADC using the proposed scheme is then described and system-level simulation results presented.

Conclusions are then suitably drawn in Chapter 7 and potential areas for further research in the quest for high-performance ADC power consumption minimization identified.

1.4 Research Contributions

The main contributions of this research to the body of knowledge can be summarized as follows:

- Determination of optimal inter-stage partitioning for lowest power dissipation in moderate resolution pipeline ADCs. This enabled the design of a video-rate low-power ADC with the lowest reported energy efficiency to date.
- Novel switch linearization circuit for switched capacitor ADC sampling switch. This lineariser circuit allowed for over 12 dB ADC dynamic range improvement in comparison with ADC sampling switch implementation using prior art (transmission gates) and was successfully verified in silicon for both a GSM and WCDMA $\Delta\Sigma$ ADC.
- Proposal of novel low-power background calibration schemes for high-speed high-resolution pipeline ADCs that was suitable for implementation in battery-powered mobile devices. Circuit and layout design of a 12-bit ADC was then done to demonstrate the scheme with the silicon design planned for fabrication in November 2006.

1.5 Publications

The following papers were accepted for both journal and conference publications within the period of the research:

- A Segmented Analog Calibration Scheme for Low-Power Multi-Bit Pipeline ADCs *by O. A. Adeniran and A. Demosthenous, accepted for publication in the December 2006 IEEE International Conference on Electronics, Circuits and Systems (ICECS 2006) proceedings.*

- An Ultra Energy-Efficient, Wide-Bandwidth Video Pipeline ADC Using Optimized Architectural Partitioning *by O. A. Adeniran and A. Demosthenous, submitted to the IEEE Transactions on Circuits and Systems I – Regular Papers, revised May 2006, August 2006 and awaiting publication.*

- A 19.5 mW 1.5 V 10-bit Pipeline ADC for DVB-H Systems in 0.35 μm CMOS *by O. A. Adeniran and A. Demosthenous, in Proc. 2006 IEEE International Symposium on Circuits and Systems (ISCAS 2006), Kos island, Greece, pp. 5351-5354, May 2006.*

- A 92 dB 560 MHz 1.5 V 0.35 μm CMOS Operational Transconductance Amplifier *by O. A. Adeniran and A. Demosthenous, in Proc. the 2005 European Conference on Circuit Theory and Design (ECCTD 2005), Cork, Ireland, pp. 325-328, August 2005.*

- Optimization of Bits-per-Stage for Low-Voltage Low-Power CMOS Pipeline ADCs *by O. A. Adeniran and A. Demosthenous, in Proc. the 2005 European Conference on Circuit Theory and Design (ECCTD 2005), Cork, Ireland, pp. 55-58, August 2005.*

- A CMOS Low-Power ADC For DVB-T And DVB-H Systems *by O. A. Adeniran, A. Demosthenous, C. Clifton, R. Soin and S. Atungsiri in Proc. 2004 IEEE International Symposium on Circuits and Systems (ISCAS 2004), Vancouver, Canada, pp. 209-212, May 2004.*

In addition, a journal paper stemming from the work described in Chapter 5 is currently in preparation.

2 Analogue to Digital Converter Fundamentals

"The law of the Lord is perfect converting the soul" Ps. 19:7 KJV

Virtually all real-life phenomena produce effects that are continuous in nature from human nerve signals of minuscule electrical magnitude to seismic tremors of significantly higher intensity. To further perceive, transport, analyze or archive these continuous-time analogue signals a means must exist for conversion from physical to electrical form. This is usually achieved via a variety of transducers ranging from strain gauges to the ubiquitous microphone. The analogue electrical outputs of these transducers is then translated to the digital domain where the signal can no longer be corrupted by media ageing and the superior processing power of digital signal processors, dedicated microprocessors and the flexibility of software can be annexed for robust data extraction, demodulation or analysis. The ADC is the bridge between the continuous-time analogue domain and discrete-time digital domain. Since ADCs are sampled sub-systems, some signal pre-conditioning is usually required to preserve signal integrity in the digital domain. This chapter will cover signal characteristics and conditioning issues with the terminologies associated with sampled signals in general and ADCs in particular elucidated. Issues and constraints of ADC testing methodologies will be considered.

2.1 Analogue and Discrete-time Signals

Fig. 2.1 shows an analogue sinusoidal waveform of frequency f_{sig} represented by the equation below with overlaid harmonics at $(2 \cdot n + 1) \cdot f_{sig}$ for integer $n = 2$ and 4 and periodically sampled at times $T = 1/f_{clk}$ where the sampling frequency, $f_{clk} \geq 2 \cdot f_{sig}$ to obey the Nyquist Criterion [5]:

$$V_{sig}(t) = A \cdot \sin(2\pi f_{sig} t). \tag{2.1}$$

If for example, $V_{sig}(t)$ is sampled twice within a period at its maxima and minima (magenta circle in Fig. 2.1), all three waveforms of different frequencies are coincident at the sampling points. Coherent sampling thus cannot distinguish between a signal sampled at the Nyquist rate and its harmonics, as the Fourier transform of the discrete-time data will represent the three waveforms with a single tone at f_{sig}, a problem known as aliasing which may or may not be desirable depending on whether signal sub-sampling is the original intent. This illustration has employed a simple sinusoid but the phenomenon is directly applicable to

both periodic and random signals. In general, if a signal of bandwidth f_{bw} is sampled at rate f_{clk} where $f_{clk} \geq f_{bw}$, aliasing will be significantly minimized if the signal is constrained within f_{bw} by the use of a suitable anti-alias filter prior to discrete-time sampling.

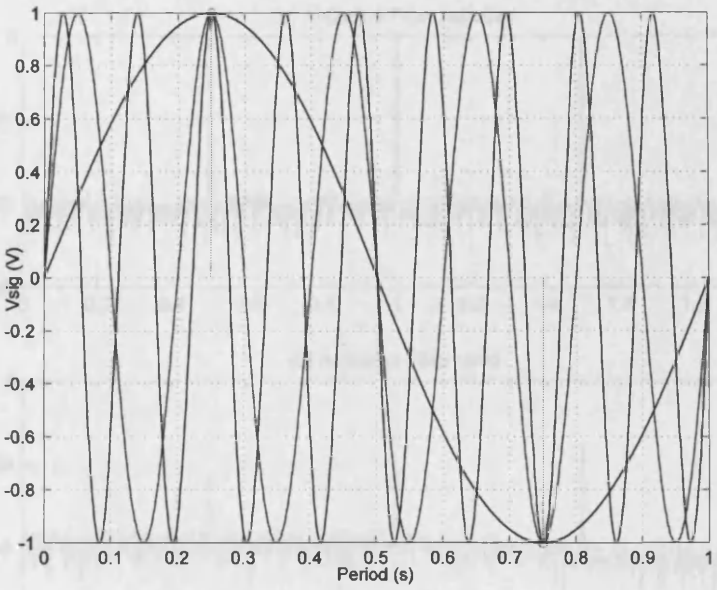


Fig. 2.1 Representative sinusoidal waveform with overlaid 5th and 9th harmonics.

Fig. 2.2 depicts the sampler with a 6th order Butterworth filter used for anti-aliasing.

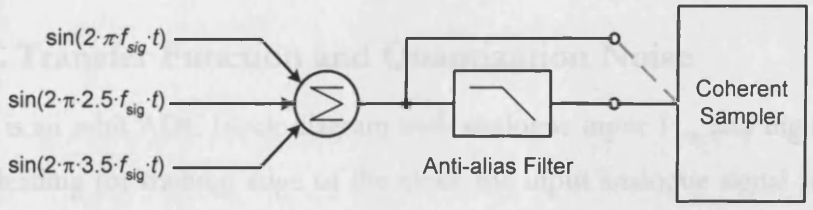


Fig. 2.2 Descriptive coherent sampling subsystem with anti-aliasing filter included.

Three noisy sinusoids, one at f_{sig} and the others at $2.5 \cdot f_{sig}$ and $3.5 \cdot f_{sig}$ are generated using Matlab® and applied to the 6th order Butterworth anti-alias filter input prior to sampling at exactly $f_{clk} = 4 \cdot f_{sig}$. Fig. 2.3 is the normalized (to $0.5 * f_{clk}/f_{sig}$) in-band power spectrum of the pre and post-anti-alias-filtered sampled data with better than 40dB rejection of aliased signals obtained (the $2.5 \cdot f_{sig}$ alias undergoes less filtering because of its proximity to f_{sig}). Ideally, the anti-alias filter stop-band rejection should be high enough to attenuate the aliases to levels comparable to the noise floor. This complicates the analogue filter design considerably, hence the use of pseudo over-sampling in most systems to ease the filter design (i.e. a 20.48MS/s Nyquist ADC used for 4 MHz broadcast video digitization). This issue is further exacerbated in ADCs used for sub-sampling as a result of the closer proximity of in-band and out-of-band Intermediate Frequency (IF) signals (i.e. designing a filter that rejects a

64MHz tone with the wanted tone at 62 MHz is a non-trivial task). To relieve the filter complexity issue for sub-sampling applications, the undesired signal may be allowed to fold down into baseband and is subsequently taken out using digital signal processing.

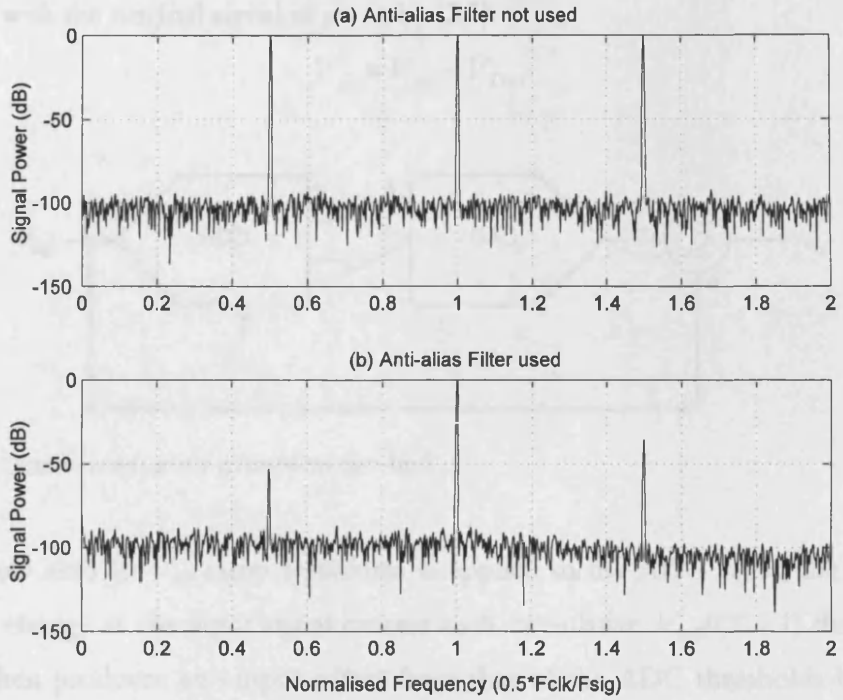


Fig. 2.3 Sampled signal spectra (a) without and (b) with anti-alias filtering used.

2.2 ADC Transfer Function and Quantization Noise

Fig. 2.4 is an n-bit ADC block diagram with analogue input V_{sig} and digital outputs b_{n-1} to b_0. At the leading (or trailing) edge of the clock the input analogue signal is sampled and quantized to a precision determined by the resolution (number of output bits) of the ADC. The analogue input and digital outputs of the ADC can be related by (2.2):

$$V_{ref} \cdot \left(b_0 \cdot 2^{-n} + b_1 \cdot 2^{1-n} + ... + b_{n-2} \cdot 2^{-2} + b_{n-1} \cdot 2^{-1}\right) = V_{sig} \pm V_Q \qquad (2.2)$$

where V_{ref} is the ADC analogue reference voltage (to which cumulative fractions the input signal is compared), b_{n-1} … b_0 are the ADC output bits and V_Q the quantization error or noise which in an ideal ADC is bounded between $\pm 1/2^{n+1}$ or ± ½ LSB (Least Significant Bits).

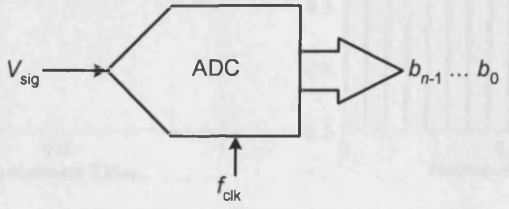


Fig. 2.4 Ideal n-bit ADC block diagram.

To extract the quantization error from our hypothetical *n*-bit ADC, the test-bed block diagram in Fig. 2.5 will be required with an ideal *n*-bit Digital to Analogue Converter (DAC) with output V_{DAC} used to convert the quantized digital signal back to analogue for comparison with the original signal as given by (2.3).

$$V_Q = V_{sig} - V_{DAC} \tag{2.3}$$

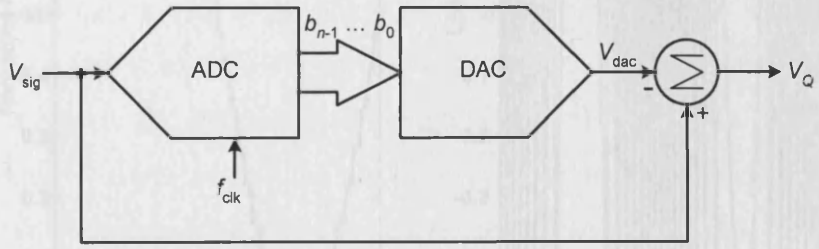


Fig. 2.5 Quantization error extraction test-bed.

If a slow zero to V_{ref} ramp waveform is applied to the ADC input, the ADC digital outputs will change as the input signal crosses each cumulative $V_{ref}/(2^n - 1)$ threshold level. The DAC then produces an output offset from that of the ADC thresholds by ½ LSB as illustrated in Fig. 2.6. It can also be observed that the quantization noise, V_Q follows the familiar saw-tooth waveform pattern but is bounded between ± ½ LSB limits.

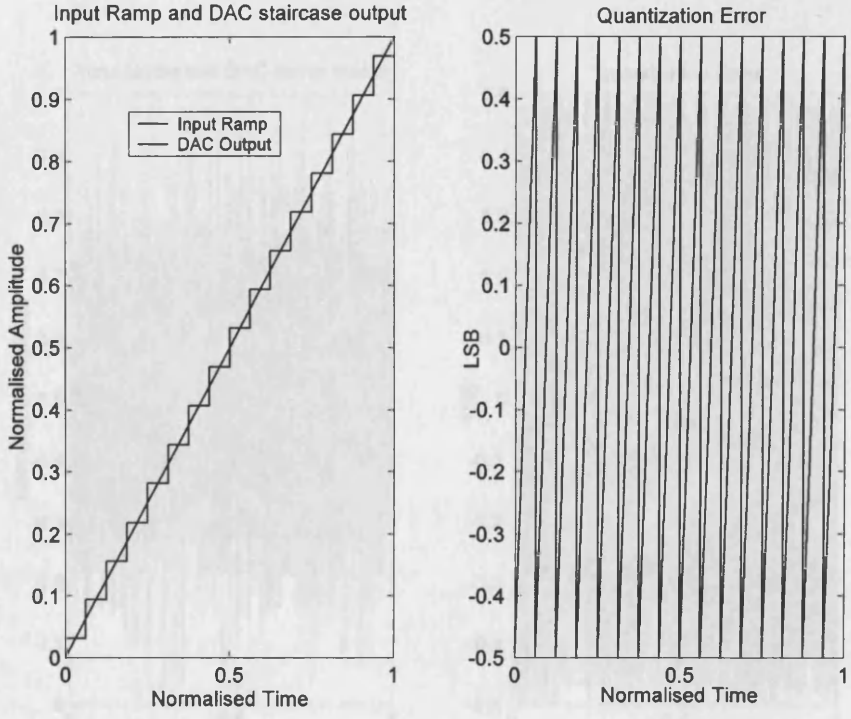


Fig. 2.6 ADC quantization noise with ramp input.

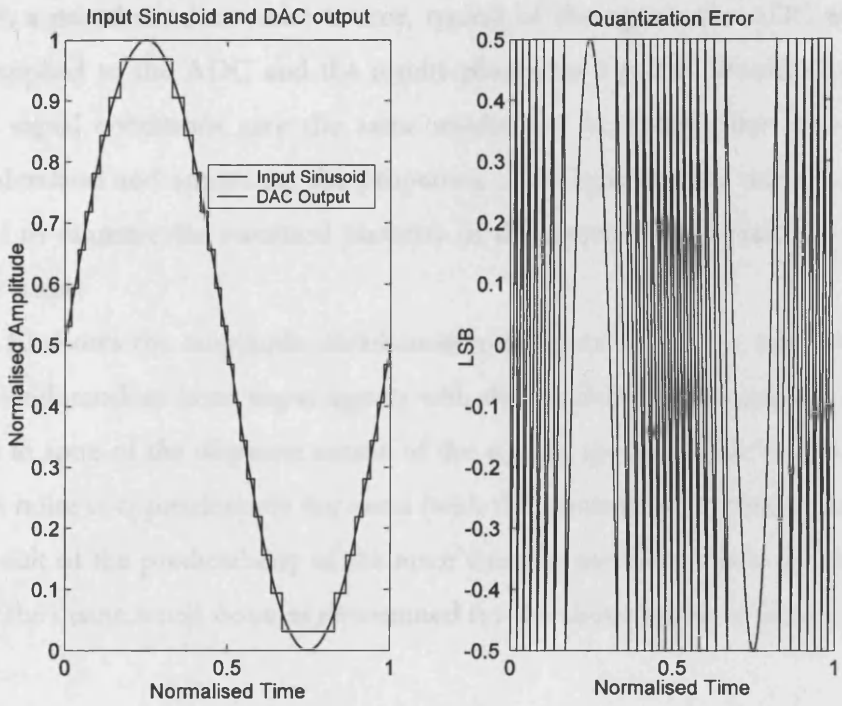


Fig. 2.7 ADC quantization noise with sinusoidal input.

On the other hand, if a sinusoid is applied to the input of the ADC, a different quantization noise profile results (Fig. 2.7) but which is still within the ± ½ LSB bounds. If again, a Gaussian noise source with outputs constrained to the ADC input limits is applied to the ADC inputs, the noise-like quantization error in Fig. 2.8 results.

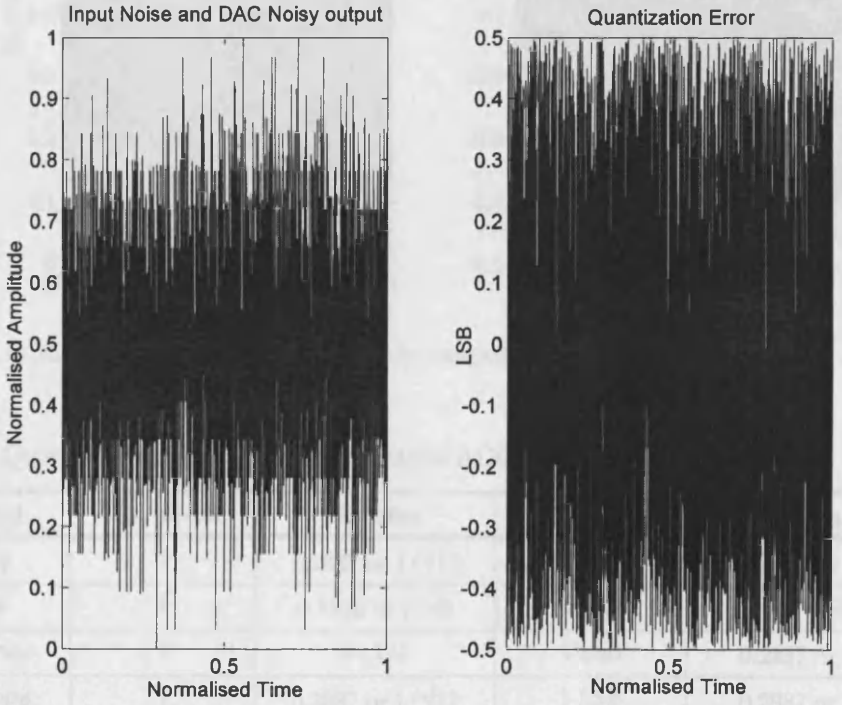


Fig. 2.8 ADC quantization noise with Gaussian noise input.

Finally, a pseudorandom noise source, typical of the signals the ADC will digitize in real life, is applied to the ADC and the results plotted in Fig. 2.9. Would all of the above ADC input signal conditions give the same results for the quantization noise energy? In order to understand and appreciate the properties of the quantization noise or error, it will be beneficial to examine the statistical property of the above input signals and the resultant quantization noise.

Fig. 2.10 shows the amplitude distribution histograms of a ramp, sinusoidal Gaussian noise and pseudorandom noise input signals with their associated quantization errors. It can be seen that in spite of the disparate nature of the signals, the amplitude distribution of their quantization noise is approximately the same (with the sinusoid quantization noise slightly in error as a result of the predictability of the error contribution of its peaks and troughs). The *rms* value of the quantization noise as determined for the above inputs is listed in Table 2.1.

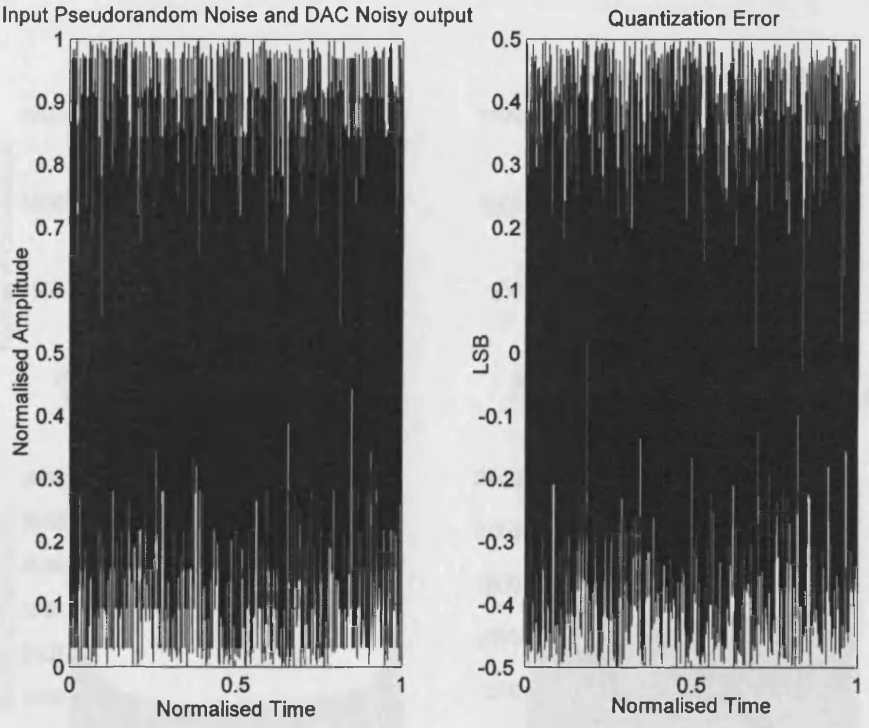


Fig. 2.9 ADC quantization noise with pseudo-random noise input.

Table 2.1 Quantization noise energy for disparate ADC input signals.

Input Signal	V_{sig} pk-pk	V_{sig} rms	V_Q pk-pk	V_Q rms
Slow Ramp	1	0.2887 or $1/\sqrt{12}$	1 LSB	0.2887 or $1/\sqrt{12}$ LSB
Sine Wave	1	0.3536 or $1/\sqrt{8}$	1 LSB	0.3068 LSB (6% error)
Gaussian Noise	1	0.1192	1 LSB	0.2887 or $1/\sqrt{12}$ LSB
Random Noise	1	0.2887 or $1/\sqrt{12}$	1 LSB	0.2887 or $1/\sqrt{12}$ LSB

The above results can also be obtained analytically [18] by assuming a stochastic input signal with the quantization noise uniformly distributed between ± ½ LSB. The probability density function $f_Q(V)$ will be a constant as in Figure 2.10, i.e.

$$\int_{-\infty}^{\infty} f_Q(V)\mathrm{d}V = 1 \tag{2.3}$$

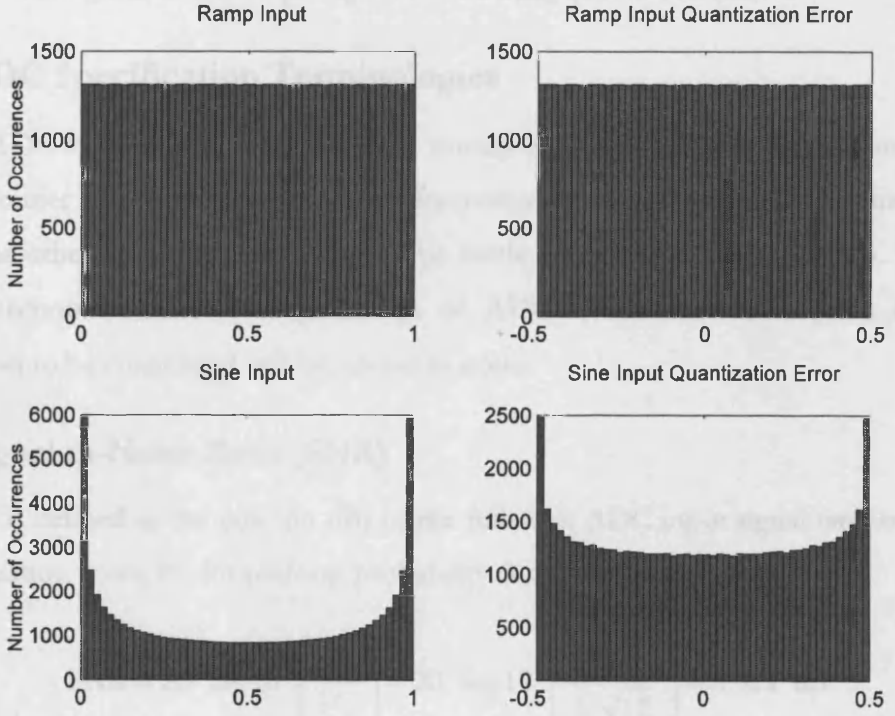
The *rms* value of the quantization noise is then given by:

$$V_{Q(rms)} = \left[\int_{-\infty}^{\infty} V_Q^2 f_Q(V)\mathrm{d}V\right]^{1/2} = \left[\int_{-1/2}^{1/2} V_Q^2 \mathrm{d}V\right]^{1/2} = \left[\frac{1}{3}\cdot\left(\frac{1}{2^3} - -\frac{1}{2^3}\right)\right]^{1/2} \tag{2.4}$$

i.e.

$$V_{Q(rms)} = \frac{1}{\sqrt{12}}\mathrm{LSB} \tag{2.5}$$

In general, the *rms* value of ADC quantization noise is always $1/\sqrt{12}$ LSB if it is uniformly distributed between ± ½ LSB.



(Figure continues in next page)

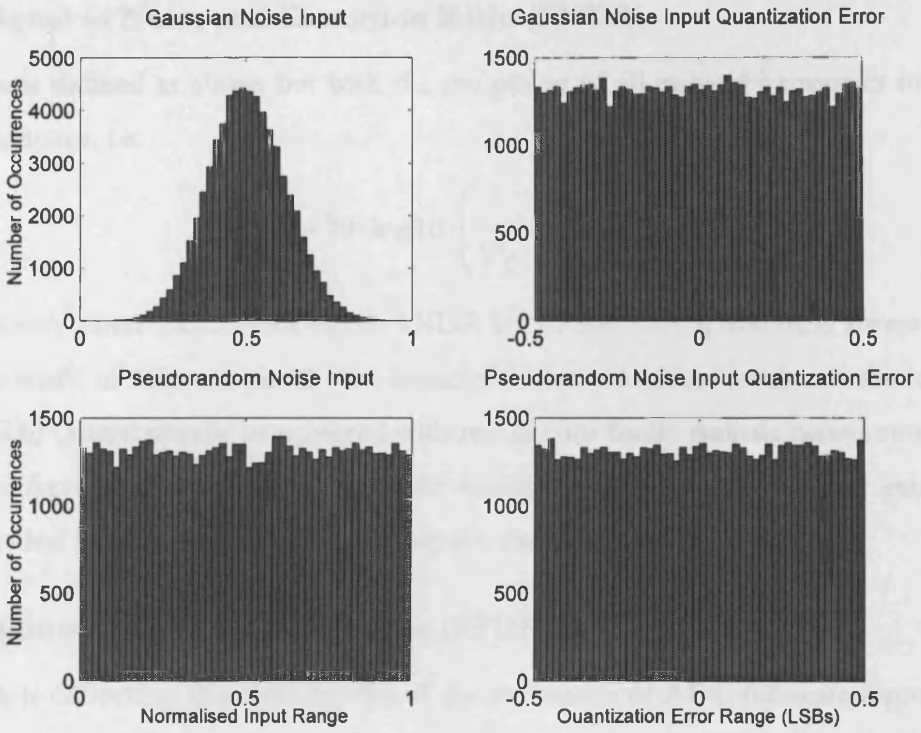


Fig. 2.10 Histograms of ADC input signals and resulting quantization noise.

2.3 ADC Specification Terminologies

All ADC specification parameters are usually extracted from the digital outputs using discrete Fourier transforms for noise or frequency-related specifications or time-domain analysis for other specifications. This will be further expatiated in Section 2.4. Since the previous section examined the properties of ADC quantization noise, the first ADC specification to be considered will be related to noise.

2.3.1 Signal-to-Noise Ratio (SNR)

This is defined as the ratio (in dB) of the full-scale ADC input signal *rms* power to the *rms* quantization noise, i.e. for uniform probability density input signals,

$$\mathrm{SNR} = 20 \cdot \log 10 \cdot \left(\frac{V_{\mathrm{sig}}}{V_Q} \right) = 20 \cdot \log 10 \cdot \left(\frac{2^n / \sqrt{12}}{1/\sqrt{12}} \right) = 6.02n \ \mathrm{dB} \qquad (2.6)$$

where n is the ADC resolution. The characterization of an ADC is usually done using a sinusoidal input (*rms* value of $1/\sqrt{8}$) with the SNR re-defined as:

$$\mathrm{SNR} = 20 \cdot \log 10 \cdot \left(\frac{2^n / \sqrt{8}}{1/\sqrt{12}} \right) = 20 \cdot \log 10 \cdot \left(\frac{2^n / \sqrt{12}}{1/\sqrt{12}} \cdot \sqrt{\frac{3}{2}} \right) = 6.02n + 1.76 \ \mathrm{dB} \qquad (2.7)$$

2.3.2 Signal to Noise and Distortion Ratio (SNDR)

This is defined as above but with the *rms* power of all in-band harmonics included in the denominator, i.e.

$$\text{SNDR} = 20 \cdot \log 10 \cdot \left(\frac{V_{\text{sig}}}{V_Q + V_{\text{harmonics}}} \right) \text{dB} \tag{2.8}$$

For a perfectly linear ADC, SNR equals SNDR but in real ADCs, SNDR is always less than SNR as a result of inherent circuit non-linearity (to be considered later) and the ideal $6.02n$ SNR of (2.6) cannot usually be achieved with real circuits under realistic power consumption budgets (effects of circuit noise, incomplete amplifier settling, finite amplifier gain, etc will dilute the ideal SNR as considered in subsequent chapters).

2.3.3 Spurious Free Dynamic Range (SFDR)

This is defined as the ratio (in dB) of the *rms* power of ADC full-scale input signal to the *rms* power of the highest spurious signal (harmonics inclusive) in the ADC output spectrum after discrete Fourier transform of the output data i.e.

$$\text{SFDR} = 20 \cdot \log 10 \cdot \left(\frac{V_{\text{sig}}}{V_{\text{spurious}}} \right) \text{dB} \tag{2.9}$$

2.3.4 Total Harmonic Distortion (THD)

This is the ratio of the *rms* sum of the second to sixth in-band harmonics of the ADC output spectrum to the full-scale input signal, i.e.

$$\text{THD} = 20 \cdot \log_{10} \cdot \left(\frac{\sqrt{V_{\text{harmonic2}}^2 + V_{\text{harmonic3}}^2 + \ldots + V_{\text{harmonic5}}^2 + V_{\text{harmonic6}}^2}}{V_{\text{sig}}} \right) \text{dB} \tag{2.10}$$

If the dominant spurious tone is an input signal harmonic and all other harmonics and spurs are sufficiently small in magnitude relative to it, THD (dB) is then approximately equal to – SFDR (dB).

2.3.5 Resolution

This has already been implicitly defined and is the number of ADC output bits, i.e. *n*-bits. It is also a measure of the smallest distinct analogue level that the ADC can effectively resolve, i.e. an *n*-bit ADC can resolve input signal differences to a precision of $V_{\text{ref}}/2^n$, where V_{ref} is the full-scale ADC input voltage.

2.3.6 Effective Number of Bits (ENOB)

As mentioned in Sections 2.3.1 and 2.3.2, sinusoidal input signals (band-pass filtered for high spectral purity) are usually employed in the characterization of ADCs, and the actual ADC SNR is far from ideal. Rearranging (2.7) thus gives:

$$\text{ENOB} = n_{\text{effective}} = \frac{\text{SNR}_{\text{measured}} - 1.76}{6.02} \tag{2.11}$$

where the ADC ENOB is a measure of the accuracy (the precision of the converter transfer response) of the ADC. For real Nyquist ADCs, ENOB is less than actual ADC resolution (ENOB can be greater than ADC resolution for over-sampled ADCs).

2.3.7 Sample Rate

This is the ADC clock rate or the rate at which the input is sampled and digital data is churned out of the ADC. It can vary between a few Hz to a few GHz depending on the ADC architecture and application [19].

2.3.8 Effective Resolution Bandwidth (ERBW)

This is defined as the ADC input frequency at which the measured ENOB reduces by 0.5 LSB (-3 dB frequency) relative to measured ENOB for low-frequency inputs of the same magnitude. For Nyquist ADCs, ERBW is typically a half of the sample rate, but can be significantly higher than the sample rate if the ADC is designed for sub-sampling applications.

2.3.9 Sub-sampling

In wireless receiver subsystems, the ADC may be used to directly sample the comparatively higher Intermediate Frequency (IF) output of the front-end mixer at a lower clock rate. The wanted band then aliases into the ADC's Nyquist band and is thus down-converted. This process is called sub-sampling or under-sampling and a classic example is the sub-sampling of the 36.57 MHz IF output of a digital television broadcast tuner at 18.28 MS/s using a Nyquist ADC with relaxed anti-alias filtering [20]. The 4 MHz in-phase (I) and quadrature (Q) bands can then be simultaneously recovered from the digitized and down-converted IF using a single high-ERBW ADC with 9.14 MHz down-converted bandwidth (Nyquist) available.

2.3.10 Over-Sampling Ratio (OSR)

This is defined as the ratio between the ADC sample rate and the Nyquist signal bandwidth as given below:

$$\mathrm{OSR} = \frac{f_{\mathrm{clock}}}{2 \cdot f_{\mathrm{bandwidth}}}. \tag{2.12}$$

OSR is unity for Nyquist ADCs and greater than unity (typically between 16 and 512) for over-sampled ADCs [21].

2.3.11 Integral Nonlinearity (INL)

In Fig. 2.6, it was observed that the quantization noise of an ideal ADC was bounded within ± ½ LSB for a ramp input. The quantization noise of a real ADC under exactly the same excitation condition may or may not be within the ±½ LSB bounds. The array of deviation in quantization noise between the real ADC case and the ideal ADC for every output code is thus the integral nonlinearity (INL) i.e.

$$\mathrm{INL}\left[1,\ldots 2^n\right] = V_{Q(\mathrm{idealADC})}\left[1,\ldots 2^n\right] - V_{Q(\mathrm{realADC})}\left[1,\ldots 2^n\right]. \tag{2.13}$$

This also is equivalent to drawing a straight line between the ADC zero-scale and full-scale output codes and finding the array of the deviation of each code from the corresponding mid-point on the straight line. This is illustrated in Fig. 2.11.

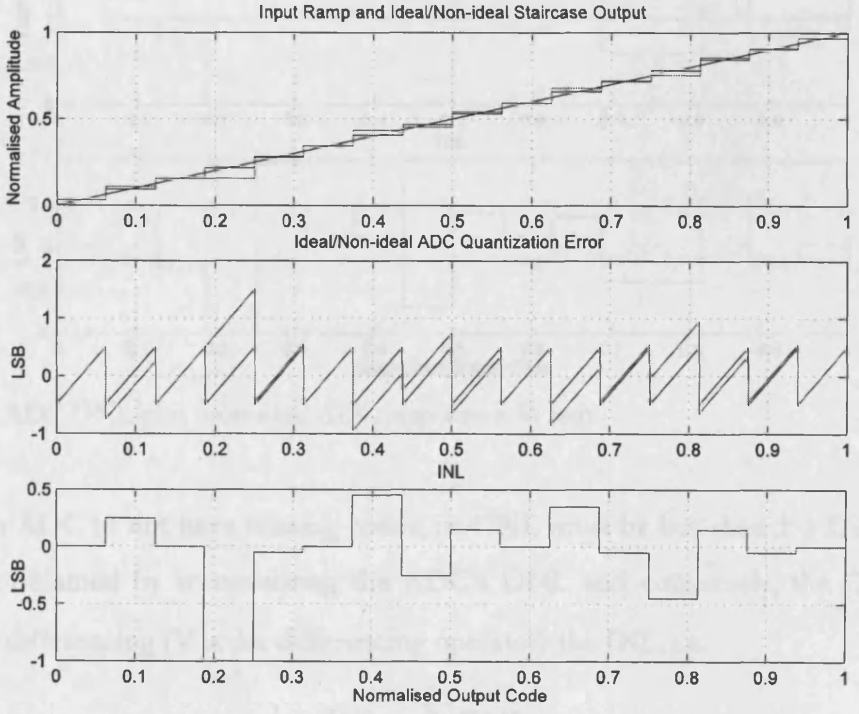


Fig. 2.11 ADC INL plot (non-ideal ADC response is in red).

A best-fit straight line may also used but the added complexity of best-fit algorithms (i.e. least mean squares [22]) has made the simpler end-to-end straight line method more popular [23]. An ideal ADC has zero INL.

2.3.12 Differential Nonlinearity (DNL)

DNL can be defined as the array of the difference between consecutive code transitions of an ADC and consecutive code jumps of the ideal case for all output codes. This is further illustrated in Fig. 2.12. The minimum and maximum DNL extremes are usually quoted in the ADC specification tables, and for a precision ADC should be between ± ½ LSB (DNL is zero for an ideal ADC). If an ADC exhibits DNL that is equal to ± 1 LSB, it may be characterized by *missing codes* (output code does not change with corresponding change in the input signal) as illustrated in Fig. 2.12.

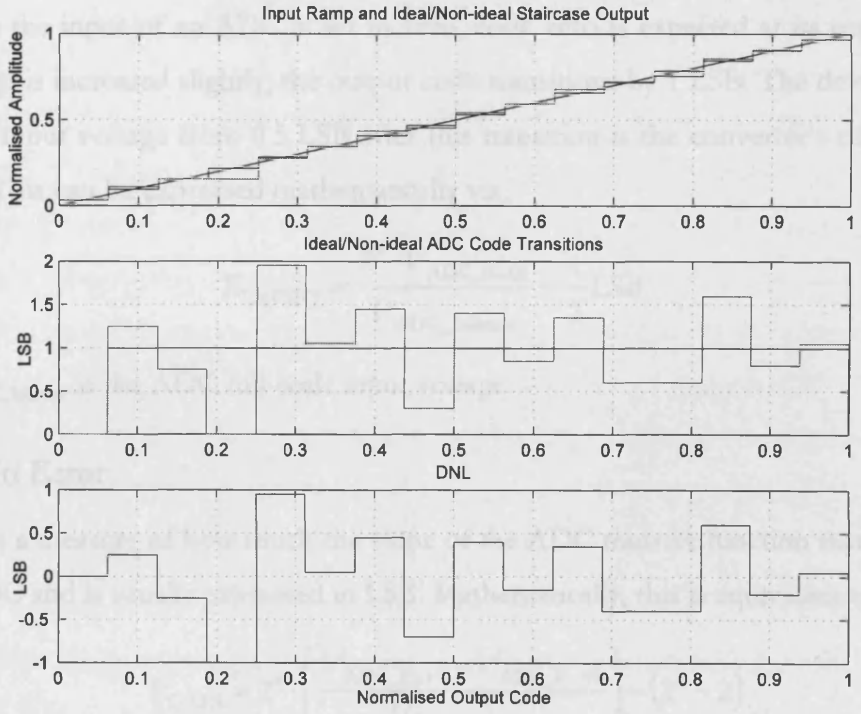


Fig. 2.12 ADC DNL plot (non-ideal ADC response is in red).

For an ADC to not have missing codes, its DNL must be less than ± 1 LSB. The INL can also be obtained by accumulating the ADC's DNL and conversely, the DNL can be obtained by differencing (∇ is the differencing operator) the INL, i.e.

$$\mathrm{INL} = \sum_{-\mathrm{LSB}}^{+\mathrm{LSB}} \mathrm{DNL} \tag{2.14}$$

$$\mathrm{DNL} = \nabla(\mathrm{INL}). \tag{2.15}$$

2.3.13 Monotonicity

An ADC is said to be monotonic if the rate of change of the ADC output with respect to its input is always positive, that is:

$$\frac{dV_{\mathrm{ADC\_out}}}{dV_{\mathrm{ADC\_in}}} > 0. \tag{2.16}$$

If the ADC's DNL is bound between ± 1 LSB limits, the ADC is guaranteed monotonic. Thus, a monotonic ADC may have missing codes but an ADC exhibiting missing codes may not necessarily be monotonic. However, an ADC with no missing codes is inherently monotonic. An ADC with INL of ± 0.5 LSB is also guaranteed monotonic with no missing code.

2.3.14 Offset Error

When the input of an ADC is set to zero, code zero is expected at its output. As the input voltage is increased slightly, the output code transitions by 1 LSB. The deviation of the normalized input voltage from 0.5 LSB after this transition is the converter's offset error in LSB units. This can be expressed mathematically viz.

$$E_{\mathrm{OFFSET}} = \frac{2^n \cdot V_{\mathrm{ADC\_0...01}}}{V_{\mathrm{ADC\_fullscale}}} - \frac{1}{2}\mathrm{LSB} \tag{2.17}$$

where $V_{\mathrm{ADC\_fullscale}}$ is the ADC full-scale input voltage.

2.3.15 Gain Error

This is a measure of how much the slope of the ADC transfer function matches that of an ideal ADC and is usually expressed in LSB. Mathematically, this is equivalent to:

$$E_{\mathrm{GAIN}} = 2^n \cdot \left(\frac{V_{\mathrm{ADC\_1...11}} - V_{\mathrm{ADC\_0...01}}}{V_{\mathrm{ADC\_fullscale}}} \right) - \left(2^n - 2\right). \tag{2.18}$$

Gain and offset errors can usually be calibrated out from an ADC in software or hardware. They are normally removed from the ADC output data before INL and DNL computations are carried out. Fig. 2.13 further illustrates this:

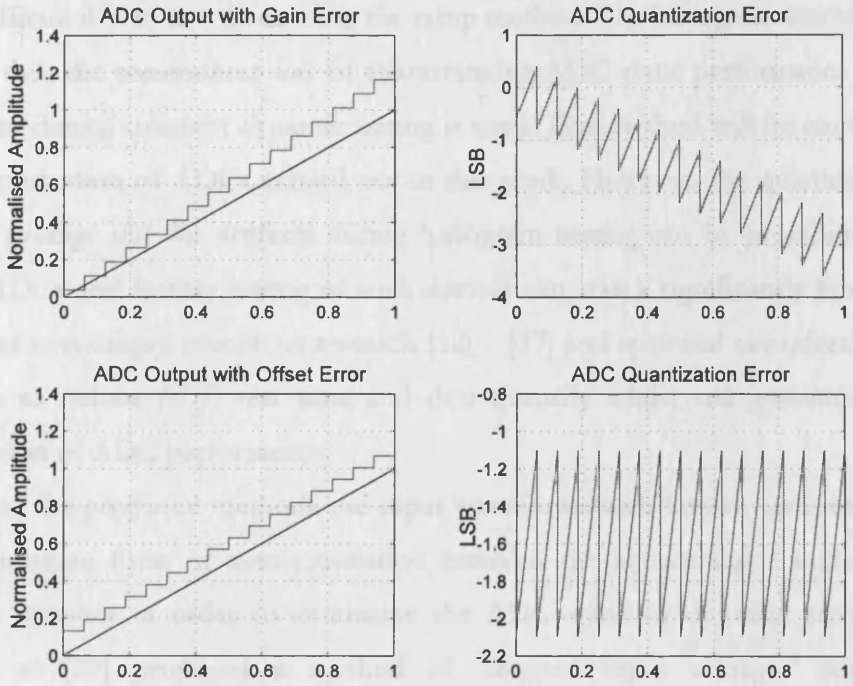


Fig. 2.13 Transfer response of ADCs with both offset and gain errors.

2.4 ADC Testing

Essentially, ADCs are tested statically (DC) for DNL and INL errors and dynamically (AC) for SNR, SNDR and SFDR at desired input frequencies and specified sample rates. For dynamic testing, a spectrally pure and band-limited sine wave is used as input to the ADC. A spectrally pure clock source coherent in relation to the input frequency (the ratio between the two must be a prime number to eliminate the need for windowing of the sampled data prior to fast Fourier transform as outlined in the IEEE ADC testing standards 1057 [24] and 1241 [25]) is then used to sample the input and the output data collected for real-time or offline processing. The SNR, SNDR and SFDR are then computed from the power spectral density of the sampled data [26].

To fully characterize the ADC statically, a ramp input is ideally required. This can be close to impossible to generate for a number of reasons. For example, if a k samples/s n-bit ADC of full-scale amplitude V_{sig} is to be characterized, the ramp input needs to have a slope of:

$$\frac{dV_{ramp}}{dt} = 2^{-(n+1)} \cdot V_{sig} \cdot k \quad . \tag{2.19}$$

This yields 0.763 V/s for a 100 kS/s 16-bit ADC with V_{sig} = 1 V. Such an ADC will take about 2 s to characterize and a 0.5 Hz ramp waveform is required for the testing which is too low for conventional signal generators to produce. The higher the resolution of the ADC,

the more difficult it is to test them using the ramp method. The histogram method [24], [25], [27], [28] is thus the commonest way of characterizing ADC static performance as the same data collected during coherent dynamic testing is used. This method will be employed for all static characterization of ADCs carried out in this work. However, the quantity of samples required to average out the artifacts during histogram testing can be prohibitive for high-resolution ADCs and factory testing of such devices can take a significantly long time. This drawback has encouraged numerous research [32] – [37] and spawned considerable literature on schemes to reduce ADC test time and data quantity whilst still guaranteeing precise characterization of ADC performance.

Most of the proposed methods use input waveforms with known statistical properties and perform some form of auto-correlation between the known input statistics and the output data statistics in order to determine the ADC static or dynamic errors. In 1983, Souders et al [29] proposed a method of 'stepped input voltages' for the static characterization of ADCs. Clayton et al [26] in 1986 proposed the well-known sine wave input for the dynamic characterization of ADCs using Fast Fourier Transforms. A maximum-length sequence input waveform is suggested in [30] for static testing of a successive approximation ADC and extended for dynamic testing using Walsh functions by Brandolini et al [28] in 1992. Koltik et al [31] in 1988 previously used a complex maximum-length sequence based input with controlled statistical properties for ADC characterization with Muginov et al [32] introducing statistical data processing of results obtained using Koltik et al's method in 1997 to shorten overall ADC test time. Mendonça et al [33] and Holub et al [34] in 1999 respectively suggested the use of non-stationary frequency input with short-time post-ADC Fourier analysis and a wide-band chirp input signal to achieve a significant reduction in test time. In 2004, Kale et al [35] proposed an extremely fast INL reconstruction method based on parametric spectral estimation that required only about eight thousand samples to completely characterize the INL of any n-bit ADC. Finally, Wegener and Kennedy [36] in 2005 described a model-based testing scheme for production environment ADCs that was time-efficient and robust to testing uncertainty.

2.5 ADC Performance Figures of Merit

A number of ADC performance figure-of-merits (FOMs) exist in the literature [37]-[40] but only two are popularly used and will be employed in this work. The first of them is ADC energy per conversion and is defined as [37], [38]

$$\mathrm{FOM}_1 = \frac{P}{2^{\mathrm{ENOB}} \times 2 \cdot \mathrm{ERBW}} \tag{2.20}$$

where P is the power consumption. The second commonly used FOM considers the actual ADC sampling rate f_s and supply voltage V_{DD} [39], [40] and is given below:

$$\mathrm{FOM}_2 = \frac{P \cdot V_{DD}}{2^{\mathrm{ENOB}} \times f_s}. \tag{2.21}$$

FOM_1 is ideally suited to ADCs designed for high ERBW and FOM_2 for ADCs compliant only to Nyquist bandwidth.

2.6 Conclusions

This chapter has outlined the fundamental terminologies associated with ADC characterization. The effect of aliasing on the ADC output spectrum was considered. The similitude of ADC quantization noise under different input signal conditions and characteristics was elucidated. Finally testing methodologies for reducing the evaluation time for moderate to high-resolution ADCs and commonly used ADC performance FOMs were then presented.

3 Analogue to Digital Converter Architectures

"...the worlds were framed by the word of God..." Heb. 11:3 KJV

Applications requiring the use of ADCs for digital translation prior to subsequent digital signal processing span over nine orders of sampling rate magnitude with one extreme being a 24-bit 7.5 S/s Delta-Sigma (ΔΣ) ADC for process control [41] and another an 8-bit 20 GS/s CMOS time-interleaved ADC for ultra-high bandwidth digital sampling oscilloscopes [42]. But which ADC architectures are ideally suited to which applications? This chapter examines all available ADC architectures and presents theoretical basis for their operation and pitfalls. A review done in 2005 by Thomas et al [19] on the majority of ADCs spanning most available architectures and published within the last few years is then presented. The composite plots illustrate the trends and architectural diversity for a given ADC resolution and sampling rates. The Flash, Two-Step, Folding and Interpolating, Pipeline, Time-Interleaved, Algorithmic/Cyclic, Successive Approximation, Integrating and ΔΣ ADC architectures are covered.

3.1 The Flash ADC Architecture

Flash ADCs are parallel converters and have the highest speed of any ADC architecture. They utilize a comparator per quantization level ($2^n - 1$ comparators in total) where n is the number of bits. The reference voltage, V_{ref} is divided into 2^n values, which are then applied to each comparator. An output word is thus generated per clock cycle. The high-speed advantage is however offset by the doubling in silicon area (and power consumption) per bit of increased resolution. A 7-bit flash ADC requires 127 comparators while an 8-bit one utilizes 255 comparators. Accuracy is determined by the extent of matching of the reference voltage divider resistor string and the offset of the comparators. The block diagram of an n-bit flash ADC is shown in Fig. 3.1 comprising a bank of comparators and a thermometer-to-binary decoder. Traditionally, flash converters are limited to about 8-bit resolution and up to 2 GS/s using CMOS technology [43]-[44] with one of the fastest monolithic flash ADC reported to date being a 4 GS/s 6-bit design in 0.13 μm CMOS [45].

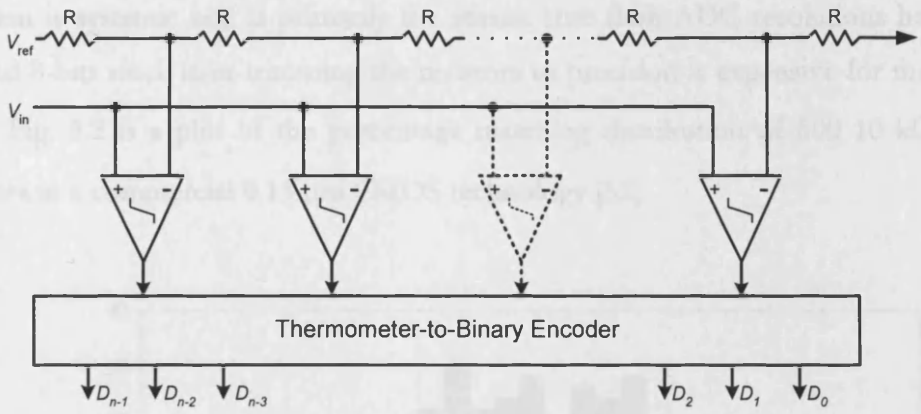


Fig. 3.1 Block diagram of an *n*-bit Flash ADC.

The following issues affect the performance and accuracy of flash ADCs and must be considered in their design:

3.1.1 Comparator Input Offset

To achieve *n*-bit flash ADC accuracy, comparators with input-referred offset voltage better than $V_{ref}/2^{n+1}$ must be used failing which, the ADC will exhibit missing codes and a compromised SNDR. A number of techniques in addition to auto-zeroing have been used to alleviate this problem such as switched-capacitor offset cancellation technique [46], a form of circuit-level spatial filtering of the error [47], digitally driven offset trimming [48] – [49], calibrated redundancy [50] and background calibration [51]. Some of the above methods require clocking with others requiring an accurate reference voltage source for foreground or background calibration.

3.1.2 Comparator Input capacitance

A typical comparator employed in a high-speed CMOS flash ADC may have input capacitances of up to 100 fF. This translates to a total ADC input capacitance of about 26 pF for an 8-bit design, thus limiting the speed of the converter and necessitating the use of a high-speed, high-dissipation buffer to drive the ADC inputs. Interpolating the comparator threshold levels can significantly reduce the number of comparators physically connected to the ADC input. This yields another class of converters that will be considered shortly.

3.1.3 Resistor Network Mismatch

Since integrated linear resistors are realized using polysilicon and lithographically implemented on the silicon die, they typically only match to about ±1%, translating to a maximum flash ADC resolution of about 6-bits without any mitigation techniques. This

problem is systemic and is primarily the reason true flash ADC resolutions have not gone beyond 8-bits since laser-trimming the resistors to precision is expensive for mass-produced parts. Fig. 3.2 is a plot of the percentage matching distribution of 500 10 kΩ polysilicon resistors in a commercial 0.13 μm CMOS technology [52].

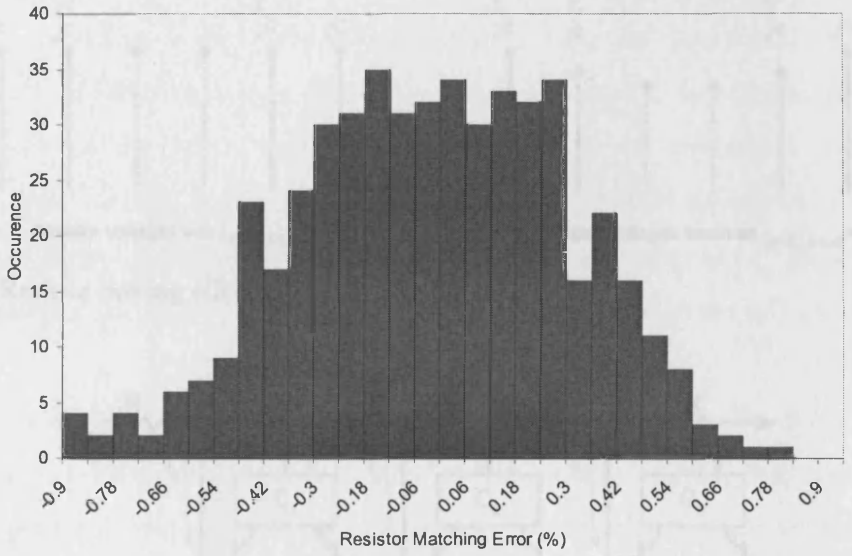


Fig. 3.2 Statistical distribution of polysilicon resistor matching for 500 resistors.

3.1.4 Resistor Voltage Bowing Effect

Fig. 3.3 illustrates this phenomenon, which is particular to bipolar flash ADC designs. The bipolar comparators' input transistor base current is derived from the resistor ladder. The signal-dependent cumulative bleeding of the available ladder current creates a 'bow' in the ladder voltages and affects the ADC linearity. Consider a 2-bit flash ADC scenario depicted in Fig. 3.4.

Three comparators and four resistors are required. Because the comparator input is a long-tailed pair, the transistor connected to a resistor node will be on until the input voltage at the second transistor's base is higher, thus turning it off. Hence, since V_{c3} is the lowest potential on the resistive ladder, all three comparator reference input currents are flowing until just before comparator C_3's output flips. Conversely, only one comparator input current is flowing prior to C_1 turning on. Using Kirchhoff's current law and the above observation,

$$\frac{V_{\text{ref}} - V_{\text{c1}}}{R} = i_c + \frac{V_{\text{c1}}}{3R} \tag{3.1}$$

$$\frac{V_{\text{c1}} - V_{\text{c2}}}{R} = i_c + \frac{V_{\text{c2}}}{2R} \tag{3.2}$$

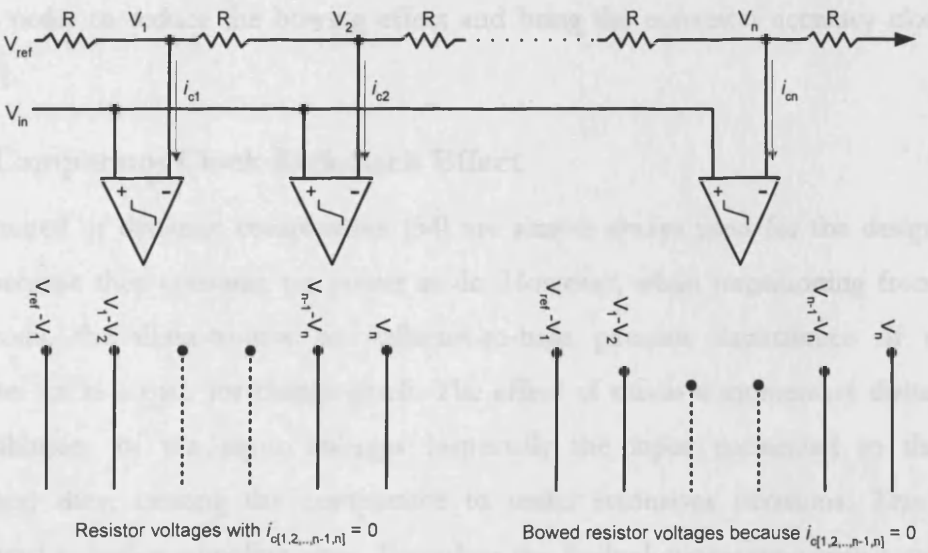


Fig. 3.3 Resistor bowing effect in an n-bit bipolar flash ADC

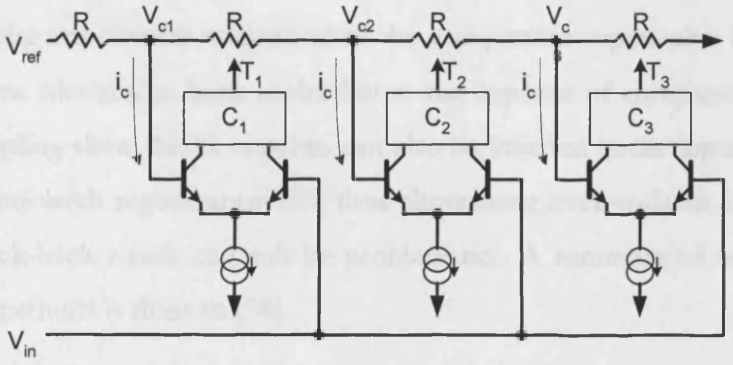


Fig. 3.4 Bipolar 2-bit flash ADC.

$$\frac{V_{c2}-V_{c3}}{R}=i_c+\frac{V_{c3}}{R} \tag{3.3}$$

Solving (3.1) to (3.3) for the resistor node voltages yield:

$$V_{c1}=\frac{3V_{ref}-3i_cR}{4} \tag{3.4}$$

$$V_{c2}=\frac{3V_{ref}-7i_cR}{6} \tag{3.5}$$

$$V_{c3}=\frac{3V_{ref}-13i_cR}{12} \tag{3.6}$$

The error terms $3i_cR/4$, $7i_cR/6$ and $13i_cR/12$ deviate the nodal voltages from their ideal values with the deviation greatest at the centre node, V_{c2}. Thus, additional circuitry is used in bipolar flash ADCs to force this voltage to its ideal value [18]. For higher-resolution designs with greater comparator counts, this scheme is extended to even more nodes in the resistor

chain in order to reduce the bowing effect and bring the converter accuracy closer to the ideal [53].

3.1.5 Comparator Clock Kick-back Effect

Latched or dynamic comparators [54] are almost always used for the design of flash ADCs because they consume no power at dc. However, when transitioning from track to latch mode, the drain-to-gate or collector-to-base parasitic capacitance of the input transistors act as a path for charge glitch. The effect of this is a momentary disturbance of the equilibrium of the input voltages (especially the input connected to the higher-impedance) thus, causing the comparator to make erroneous decisions. This effect is pronounced at higher sampling rates. Preceding the latched comparator with a continuous-time pre-amplifier helps alleviate this problem but at the expense of additional power dissipation.

Matching the impedances connected to the comparator inputs also helps as the kick-back effect is now identical at both nodes but at the expense of comparator-to-comparator input signal sampling skew. MOS switches can also be inserted in the input signal paths and opened just before latch regeneration [55] thus eliminating track-to-latch kick-back (but not latch-to-track kick-back which can still be problematic). A summary of some further kick-back reduction methods is done in [56].

3.1.6 Bubble Errors

This happens when a lone 'one' suddenly shows up in a string of 'zeros' or vice-versa for the thermometer outputs of the flash comparators and is primarily caused by comparator metastability, noise, slew-rate limitation, etc. A popular way of removing single bubbles errors originally proposed in [57] is the use of 3-input NAND gates as shown in Fig. 3.5. A wired-OR method was used in [58] for the removal of double bubble errors. A few other bubble removal methods are given in [18].

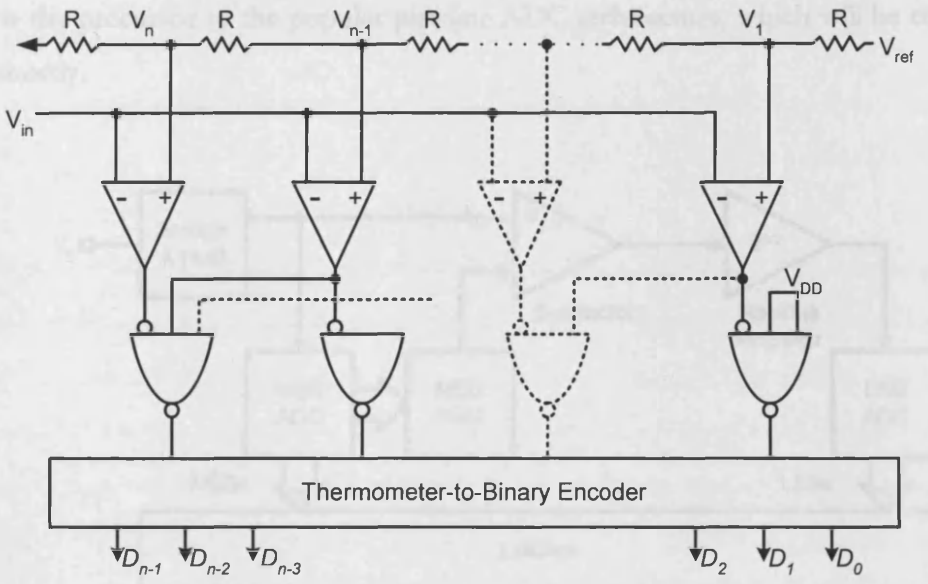


Fig. 3.5 Single bubble removal method using 3-input NAND gates.

3.1.7 Encoder Propagation Delay

Since flash ADCs are used for applications requiring high sampling rates, the thermometer-to-binary encoder design must be such that its output are available in a few hundreds of picoseconds in some cases and completely impervious to bubble errors, which increase in number as sample rates become higher. As such, the design of a high-speed, fault tolerant encoder is non-trivial. The Binary or Gray code ROM-based encoder is the simplest and the most popular as it is easy to implement on silicon as a fully parallel layout. However, it consumes power at high speeds and is somewhat slow [59]. Also, combining it with the 3-input NAND gate scheme in Section 3.1.5, will only correct a single bubble error within three thermometer-code bits. The Wallace tree encoder [60] – [62] is faster than the ROM-based encoder and corrects for global bubble errors but at the expense of more hardware and power. The Fat tree encoder was proposed in [63] as suitable for ultra-high-speed low-power flash ADC design but has a more complex layout implementation. A brief study of encoders is documented in [64].

3.2 Two-Step Flash ADC Architecture

The two-step flash or parallel feed-forward ADC is an attempt to address the flash ADC silicon area and power consumption issues by reducing the number of comparators from $2^n - 1$ to $2 \cdot (2^{n/2} - 1)$. An 8-bit, two-step flash ADC thus requires 30 comparators in comparison with the 255 needed by its flash equivalent. This is achieved by separating the converter into two complete Flash sub-ADCs with feed-forward circuitry as shown in Fig.

3.6. It is the precursor to the popular pipeline ADC architecture, which will be considered in detail shortly.

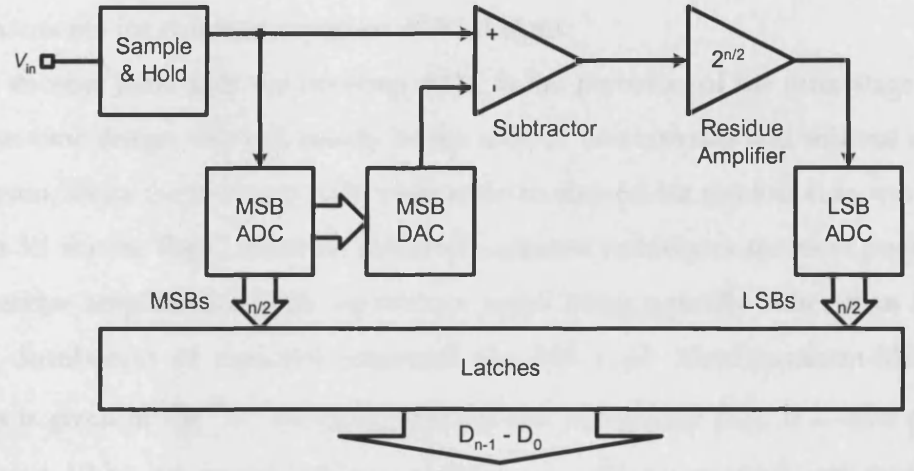


Fig. 3.6 Block diagram of a two-step flash ADC.

The first sub-ADC generates an estimate of the input signal's value (coarse conversion) at the initial clock cycle while the second one carries out a fine conversion the next cycle. The ADC output is thus available after two global clock cycles. The tradeoff however is that conversion time is now twice as long as with the flash ADC and the fact that the first $n/2$-bit flash ADC and DAC has to have n-bit accuracy. If single-bit resolution redundancy is used in the first sub-ADC with some form of digital error correction scheme [65] applied, the first $1+n/2$ flash sub-ADC need only be $1+m/2$-bit accurate, but the constraints on its DAC remains unchanged. As inter-stage subtractor and residue amplifier settling dynamics and bandwidth constraints not erstwhile present in the flash ADC come into play, the two-step ADC becomes somewhat limited in sampling rate with the fastest reported to the best of the author's knowledge being a 160 MS/s 10-bit design in 0.18 μm CMOS [66].

Another issue is the dependency of the residue amplifier accuracy on its open-loop gain (A_{OL}). An n-bit two-step flash ADC will need a residue amplifier with a closed loop gain (A_{CL}) of $2^{n/2}$ and an accuracy (ΔA_{CL}) of $1/(2^{n+1})$ if $(n/2)$-bit flash sub-ADCs are used for the two implicit converters.

For the case of a 14-bit implementation, the residue amplifier has to have $A_{CL} = 128$ (42.1dB) and $\Delta A_{CL} = 0.0000305\%$. Using feedback theory and the assumption that A_{CL} will approach $1/\beta$ (where β is the feedback factor and is 1/128 for the 14-bit implementation) as A_{OL} increases and that $\Delta A_{CL} = 0.5$ LSB, we obtain the amplifier loop gain:

$$|A_{OL}| = \beta^{-1} \cdot \left(2^{n-1} + 1\right) = 4194432 \quad \text{or} \quad 132.45 \text{ dB} \tag{3.7}$$

This is very challenging to attain for an on-chip amplifier of excellent bandwidth with reasonable power dissipation. Gain enhancement techniques may be utilized to achieve such gain requirements for switched-capacitor ADC designs.

Yet another issue with the two-step ADC is the precision of the inter-stage gain. In a continuous-time design, this will usually be the ratio of two resistors and without some form of calibration, limits the two-step ADC realization to about 6-bit resolution as was illustrated in Section 3.1 for the flash converter. Switched capacitor techniques are more popularly used for the residue amplification with capacitance ratios being typically better than 0.5%. The statistical distribution of capacitor mismatch for 500 1 pF Metal-Insulator-Metal (MIM) capacitors is given in Fig. 3.7 for a 0.13 μm process technology [52]. It is thus possible to realize about 10-bit resolution without trimming or calibration using switched capacitor techniques (or up to 12-bit resolution [67] if capacitors match to 0.1%).

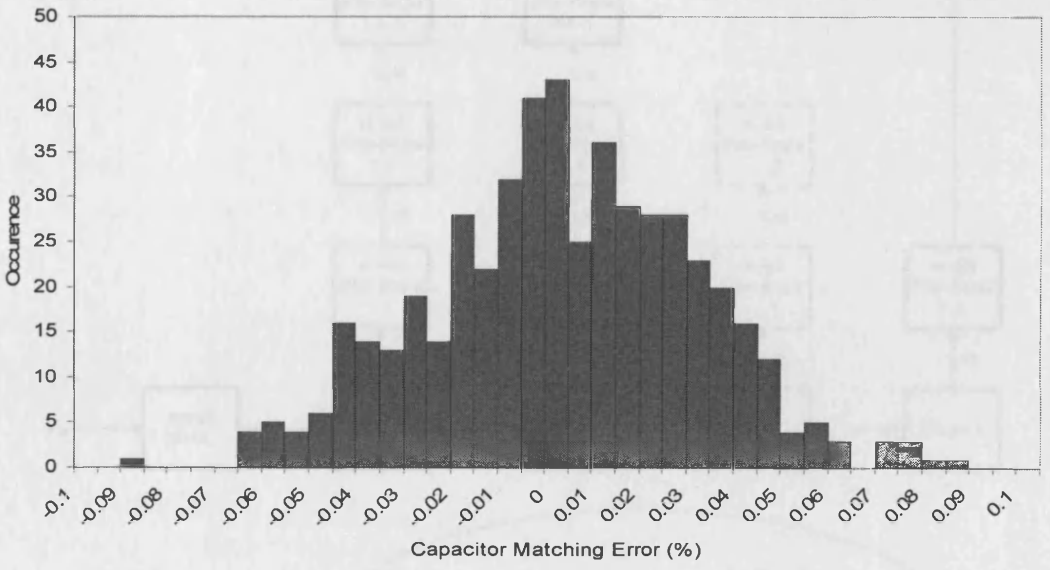


Fig. 3.7 Statistical distribution of MiM capacitor matching for 500 capacitors.

Since the residual amplifier's $|A_{OL}|$ doubles with each bit increase in resolution, two-step flash ADCs are limited to about 12-bit resolution ($|A_{OL}|$ = 524288 or 114.39 dB) or to the calibration accuracy of the resistor or capacitor ratio devices whichever is the least challenging to achieve.

3.3 Pipeline ADC Architecture

If the two-step ADC in Section 3.2 is extended to k-steps of m-bit sub-ADCs where $k > 2$, $m \geq 1$ and the digital data-path pipelined using staggered flip-flop arrays to produce output data at the global sampling clock rate, the pipeline ADC is born. Ideally, an n-bit pipeline ADC with no redundancy mechanism is partitioned such that $n = k \cdot m$ (m does not have to be the same for all stages). These converters are thus able to achieve relatively fast speeds and relatively high resolution with the highest resolution reported being 16-bit [68] and one of the fastest being 400 MS/s [69]. Fig. 3.8 is the block diagram of an n-bit pipeline ADC.

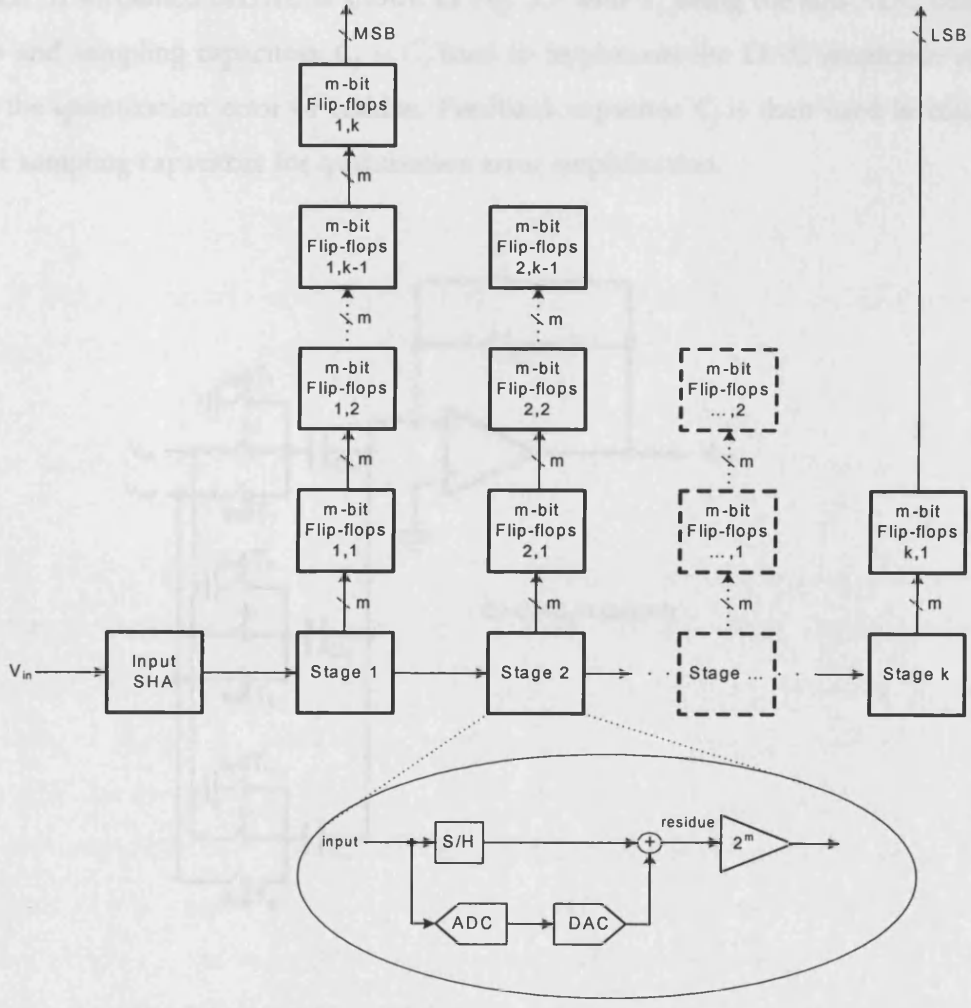


Fig. 3.8 Block diagram of an n-bit pipeline ADC where $n = k \cdot m$.

The dedicated input SHA first converts the input to an un-quantized discrete-time signal. Then the first sub-ADC quantizes the sampled input to an m-bit value. The first sub-DAC converts this value back to analogue thus allowing the subtractor block to determine the quantization error. This error ideally, should be $\leq \pm 1/2$ LSB as illustrated in Chapter 2. The residue amplifier amplifies this error by a factor of 2^m to restore amplitude level to the dynamic range of the next pipeline level. This is then sampled and the process repeated. A sub-DAC is not required for the final pipeline stage. Thus, the values held by the flip-flops at the k^{th} clock cycle are the n-bit equivalent of the 1^{st} clock cycle analogue input.

Typically, the sub-DAC, subtractor and residue amplifier blocks are combined into a single switched-capacitor circuit called a multiplying-DAC or MDAC [70] requiring only one amplifier. A simplified MDAC is shown in Fig. 3.9 with T_x being the sub-ADC comparator outputs and sampling capacitors $C_1 - C_d$ used to implement the DAC amplitude steps and extract the quantization error or residue. Feedback capacitor C_f is then used in conjunction with the sampling capacitors for quantization error amplification.

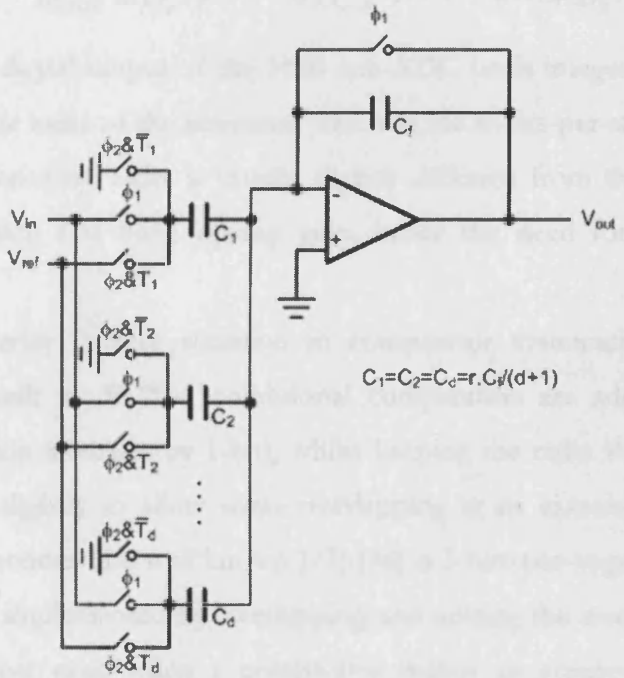


Fig. 3.9 n-bit MDAC block diagram. The & symbol is the logical AND operation.

The pipeline ADC's main merit is its high throughput. However, there is an n-clock-cycle latency which may not be an issue depending on whether the ADC is required in a feedback control system or not. To save power, the input SHA is usually dispensed with at the expense of overall ADC linearity degradation as a result of aperture error [71]. This issue

will be further considered in Chapter 4. The pipeline ADC, like its two-step counterpart, is dependent on the most significant stages for accuracy. A slight error ε in the first stage will result in an output-referred error $\varepsilon \cdot 2^n$ at the end of conversion. Hence, for high performance, digital error correction must be used to alleviate the first stage's sub-ADC comparator offset issue. Finally, the amplifier gain and device matching issues must be contained as explicated in Section 3.2 or calibration used. Once the early stages are guaranteed precise, die area and power consumption can be considerably reduced by the use of less accurate circuits for the least significant stages [72], [108].

3.3.1 Digital Error Correction in Pipeline ADCs

Consider the above hypothetical n-bit, m-bits-per-stage ADC. If no inter-stage redundancy is present and m-bit resolution is employed across the stages, k-1 m-bit MDACs and k m-bit sub-ADCs are required in total with the overall ADC output word given by the following generic equation:

$$D_{OUT} = D_k \cdot r^{(n/m)-1} + D_{k-1} \cdot r^{(n/m)-2} + \cdots + D_2 \cdot r + D_1 \tag{3.8}$$

where D_k is the digital output of the MSB sub-ADC (with integer values ranging from 0 to $2^m - 1$) and r is the radix of the converter which in the m-bits-per-stage case is ideally equal to 2^m. The actual converter radix is usually slightly different from the ideal case as a result of capacitor mismatch and finite opamp gain, hence the need for calibration or mismatch shaping.

This converter is very sensitive to comparator systematic offset errors since no redundancy is built in. If $2^m - 1$ additional comparators are added to the sub-ADC (its effective resolution increases by 1-bit), whilst keeping the radix the same and the threshold points changed slightly to allow some overlapping at its extreme bounds (Fig. 3.10), the pipeline ADC becomes the well known [73]-[74] m.5-bits-per-stage ADC with simple digital error correction implemented by overlapping and adding the inter-stage outputs. Thus, no information is lost even when a comparator makes an erroneous decision because the succeeding stage's comparators have enough range to digitize the residue.

This redundancy allows the use of comparators with offsets as high as $\pm V_{ref}/(2^{m+1})$, a significant improvement over the required $\pm V_{ref}/(2^{n+1})$ comparator accuracy of the m-bit-per-stage ADC. The final digital output of an n-bit, m.5-bits-per-stage ADC is given by the following expression:

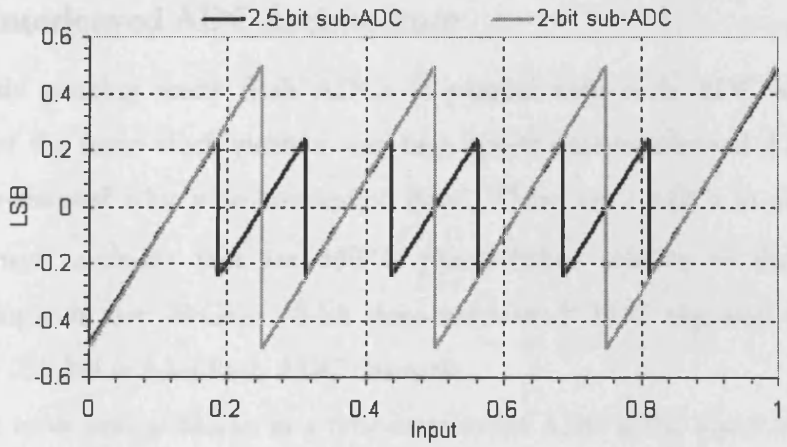


Fig. 3.10 Residue vs. input for an m-bit and m.5-bit MDAC.

$$D_{\text{OUT}} = D_k \cdot \frac{r^{(n/m)-1}}{2} + D_{k-1} \cdot \frac{r^{(n/m)-2}}{2} + \cdots + D_2 \cdot \frac{r}{2} + D_1 \tag{3.10}$$

where the sub-ADCs now have integer values ranging from 0 to $2^{m+1} - 2$. Pipeline ADC digital error correction will be treated in more depth in Chapter 6.

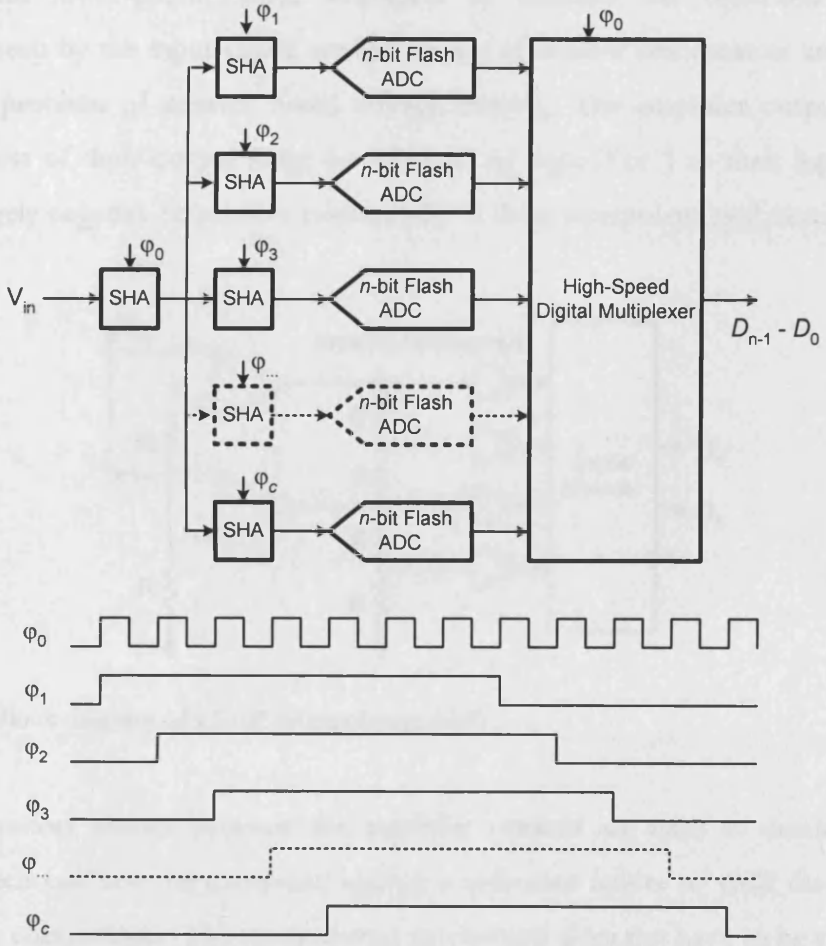


Fig. 3.11 A c-channel n-bit time-interleaved ADC.

3.4 Time-Interleaved ADC Architecture

Concurrently running many flash ADCs in parallel with each ADC sampling at a different phase of the same clock yields a very high speed time-interleaved ADC [75]. Fig. 3.11 depicts an c-channel n-bit time-interleaved ADC. There are c ADCs in all, each being clocked at f_s/c with c clocks that are $360°/c$ phase-shifted relative to themselves. An outstanding example is the 20 GS/s 8-bit time-interleaved ADC reported in 2003 [42] employing eighty 250 MS/s 8-bit flash ADC channels.

One of the most critical blocks in a time-interleaved ADC is the input SHA, which is required to sample the input at f_s. If the global sampling rate is too prohibitive, the SHA may be realized in a different process technology such as Gallium Arsenide (GaAs) [76]. In addition, all c-channels must be very well matched, as any static difference between the channels will result in undesirable tones within the band of interest.

3.5 Folding and Interpolating ADC Architecture

Interpolating converters are essentially flash converters with their dynamic comparators preceded with lower-count, linear amplifiers to facilitate the reduction of the total capacitance seen by the input signal, enable the use of coarser comparators and to implicitly address the problem of resistor nodal voltage bowing. The amplifier outputs are usually linear for most of their output range but saturate to logic 0 or 1 as their input differential becomes largely negative or positive respectively. A 2-bit interpolate-by-2 version is depicted in Fig. 3.12.

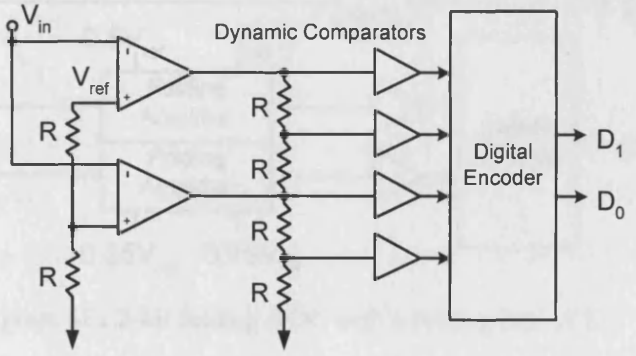


Fig. 3.12 Block diagram of a 2-bit interpolating ADC.

The resistors strings between the amplifier outputs are used to create interpolated voltages, which can now be compared against a reference ladder to yield the thermometer output of the comparators. The interpolation mechanism does not have to be solely resistive. Capacitors [77] and current sources [57] have also been used.

The interpolating converter however is still saddled with 2^n–1 comparators. To address this, the *folding ADC architecture* is used (Fig. 3.13) with the folding amplifiers carrying out pre-comparator analogue processing on the input signal. A single-fold folding amplifier is simply two cross-coupled differential amplifiers. With the inputs swept from zero-scale to full-scale, the output of the amplifier will transition twice (Fig. 3.13) thus allowing the representation of the original 2^n quantized signal levels with two $2^{n/2}$ signal levels. The number of output transitions of a folding amplifier the folding rate of the ADC. With a folding rate of two, reduction of the number of comparators required from $2^n - 1$ to approximately $2 \cdot (2^{n/2} - 1)$ as with the two-step ADC is achieved; the only difference being that the folding ADC's throughput is twice that of the two-step ADC. Also, the folding block's output frequency is the product of the ADC sample rate and the folding rate which will limit the achievable folding rate in fast converters.

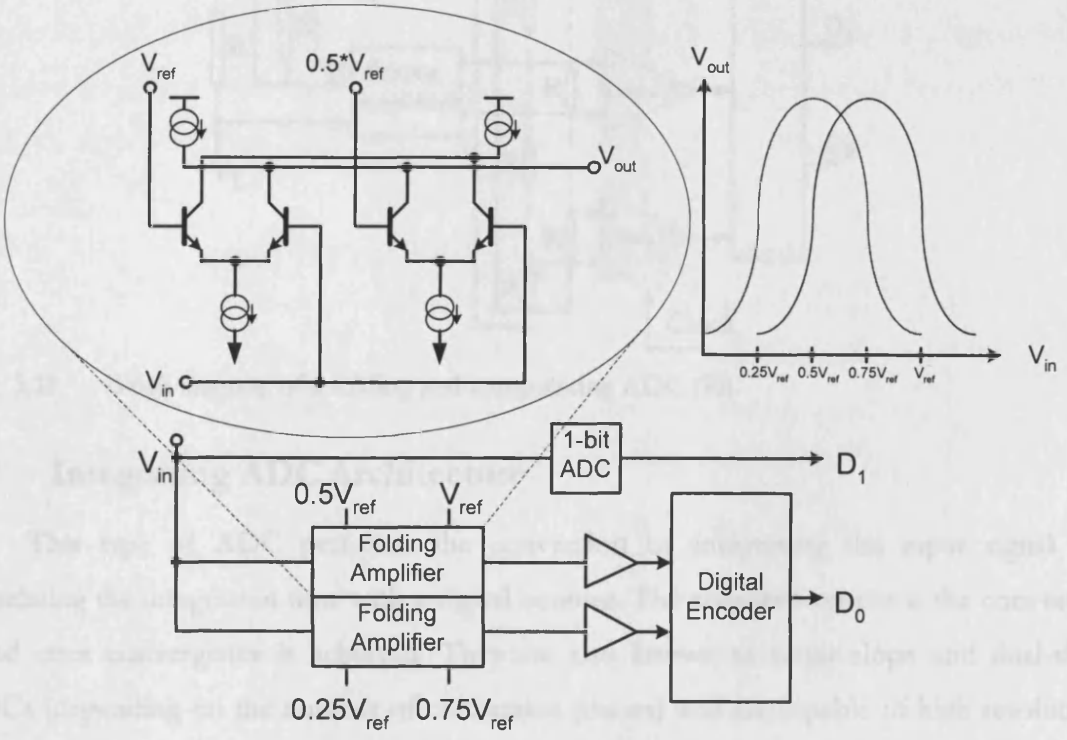


Fig. 3.13 Block diagram of a 2-bit folding ADC with a folding rate of 2.

To reduce the folding ADC's input capacitance (of the same order as a flash ADC), interpolation is then used, hence the name of this class of ADCs. Fig. 3.14 shows an 8-bit folding and interpolating converter with a folding rate of 8 and interpolation factor of 2, which is also the fastest folding and interpolation ADC reported to date: a 2 GS/s 8-bit design in Silicon Germanium (SiGe) technology [78].

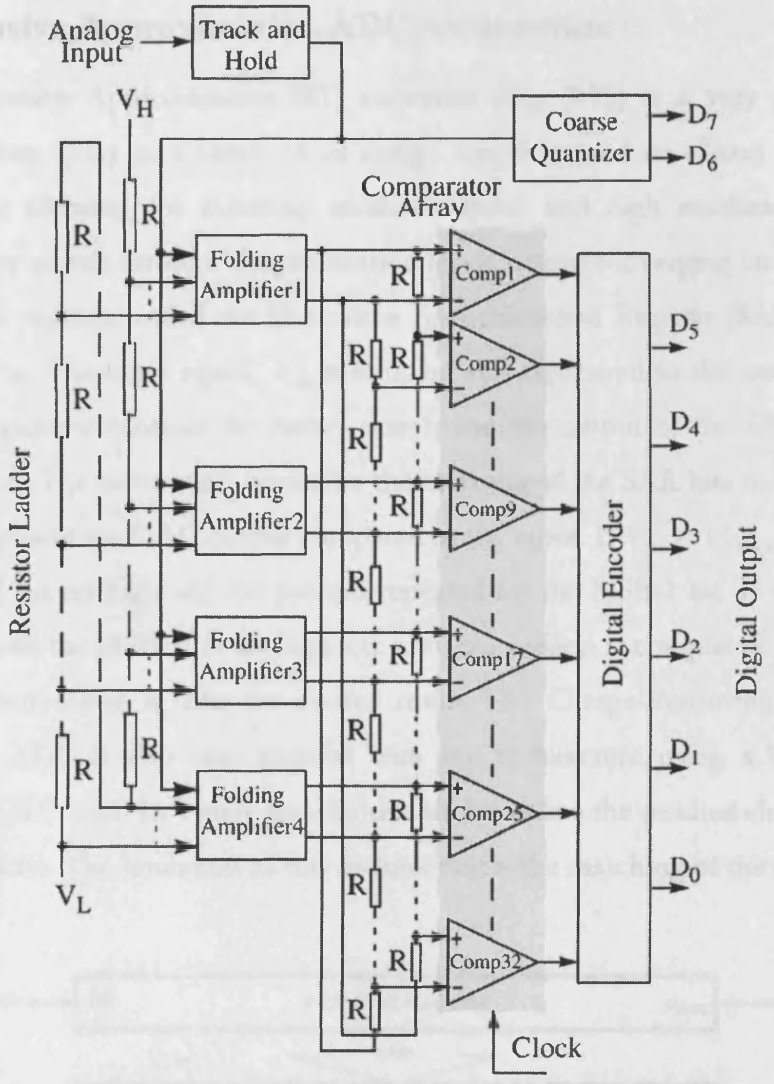


Fig. 3.14 Block diagram of a folding and interpolating ADC [78].

3.6 Integrating ADC Architecture

This type of ADC performs the conversion by integrating the input signal and correlating the integration time with a digital counter. The counter's output is the conversion word once convergence is achieved. They are also known as single-slope and dual-slope ADCs (depending on the number of conversion phases) and are capable of high resolutions with relatively slow conversion speeds. They are reasonably inexpensive and as a result, are used for slow-speed cost-conscious applications. Their clock speed is usually $f_s \cdot 2^{n+1}$ where $f_s/2$ is the Nyquist bandwidth. A 12-bit single-slope ADC with 20 kHz Nyquist bandwidth will thus require a rather high 163.84 MHz clock hence their use in only low-bandwidth applications [79]. Recently, the focus of research in the literature has been on time-to-digital converters with low energy efficiency and significantly lower sampling clock overhead than the integrating ADC architecture with [80] achieving convergence in only five clock cycles for a 12-bit design using a successive sub-ranging technique.

3.7 Successive Approximation ADC Architecture

The Successive Approximation [81] converter (Fig. 3.15) is a very popular ADCs architecture in use today as a result of its design simplicity and its silicon area utilization efficiency whilst allowing for relatively moderate-speed and high resolution. It basically performs a binary search through all quantization levels before converging on the final digital answer. An *n*-bit register, called the Successive Approximation Register (SAR) controls the conversion timing. The input signal, V_{in} is sampled and compared to the output of an *n*-bit DAC. The comparator controls the binary search and the output of the SAR is the actual digital conversion. The conversion begins by the resetting of the SAR bits to zero. The MSB is then taken high and the DAC output compared to the input. If $V_{in} > V_{DAC}$, the MSB is left high, the MSB-1 bit set high and the process repeated for the MSB-1 bit. If $V_{in} < V_{DAC}$, the MSB is set low and the MSB-1 bit set high, etc until conversion is completed. The content of the SAR after conversion is then the desired result. The Charge-Redistribution Successive Approximation ADC is also very popular with the architecture using a binary-weighted capacitor array DAC with the binary search done to determine the residual charge on each of the DAC capacitors. The limitation of this architecture is the matching of the capacitors.

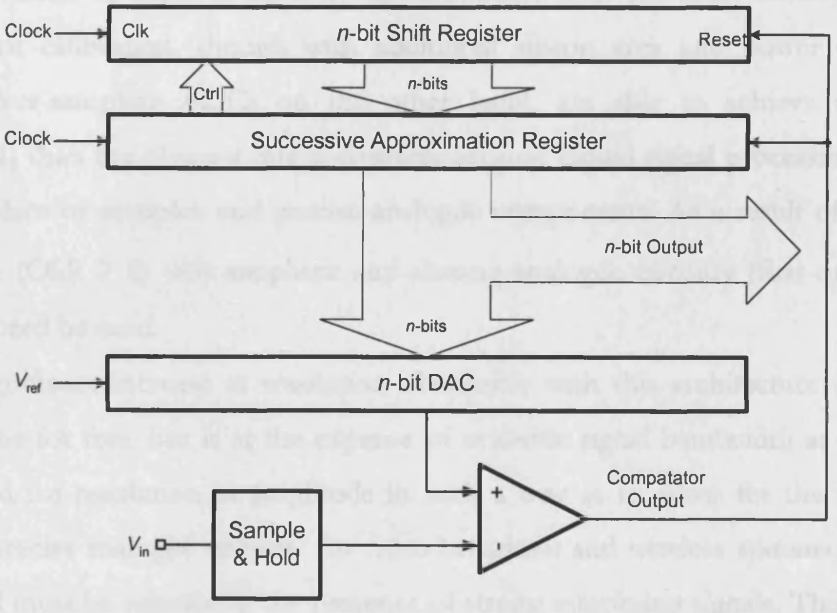


Fig. 3.15 The successive approximation ADC.

One of the earliest SAR-based ADCs reported was the all-MOS charge redistribution design by Gray et al [82] in 1975, with 10-bit conversion achieved in 20 μs, a modest duration by today's standards. At another end of the spectrum, eight 75 MS/s 6-bit

successive approximation ADCs were parallelized to achieve 600 MS/s throughput at 10 mW in [83] using a 90 nm CMOS process technology.

3.8 Cyclic/Algorithmic ADC Architecture

This class of converters is a cross between the successive approximation converter architecture and the pipeline ADC topology, in the sense that the cyclic ADC resolves the input signal bit-wise as with the successive approximation ADC. It also extracts and amplifies quantization error per resolved bit(s) as with the pipeline ADC, but with the use of a single amplifier and MDAC subsystem. Conversion thus takes place in at least n clock cycles for an n-bit cyclic ADC as additional clock cycles may be required to implement switched-capacitor means of eliminating sampling capacitor mismatch for the quantization error amplifier [84]. Advancements in process technology has enabled cyclic/algorithmic converters designs of up to 16-bits at moderate sampling speeds with [85] reporting a 16-bit 500 kS/s 6.1 LSB INL design without trimming or calibration in 0.13 μm CMOS.

3.9 ΔΣ ADC Architecture

As can be inferred from the above sections, Nyquist Rate ADCs require high accuracy analog components in order to achieve high resolution. This is usually accomplished using some form of calibration, though with additional silicon area and power consumption overhead. Over-sampling ADCs on the other hand, are able to achieve much higher resolution [41] than the Nyquist rate converters because digital signal processing techniques are used in place of complex and precise analogue components. As a result of their higher sampling rate (OSR $\geq$ 8) only simplistic anti-aliasing analogue circuitry (first-order filters in some cases) need be used.

The significant increase in resolution obtainable with this architecture unfortunately does not come for free, but is at the expense of available signal bandwidth as resolution in time is traded for resolution in amplitude in such a way as to allow for the utilization of relatively imprecise analogue circuits. In video broadcast and wireless systems, a very weak desired signal must be selected in the presence of strong interfering signals. This necessitates the use of a wide-band ADC that can digitize both the desired and adjacent channel interferers resulting in more stringent dynamic range requirements not easily achievable using Nyquist rate ADCs.

Over-sampled ADCs or ΔΣ ADCs are ideally suited to such wireless and broadcast applications (GSM, UMTS, DVB-H) because the adjacent channel interferers fall into the

same band as the shaped quantization noise. Hence, the same digital decimation filter can simultaneously remove the interferers and quantization noise. Essentially, a ΔΣ ADC comprises a multi-order ΔΣ modulator clocked at the sample rate, a multi-rate digital decimation filter to decimate the pulse-density output of the modulator to close to, or the Nyquist rate and some additional digital filtering for the removal of residual out-of-band quantization noise Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) digital filters may be used with the former possibly contributing undesirable delay to the system if the required number of taps is prohibitively long and the latter more computationally efficient but must be carefully designed to guarantee stability. Fig. 3.16 is the simplified block diagram of a first-order single-bit quantizer ΔΣ modulator. It comprises an integrator (a delay element), a 1-bit ADC (comparator) and a 1-bit DAC (a couple of switches interconnecting $+V_{ref}$ or $-V_{ref}$ to a common node). It can be shown that in the frequency domain, the quantization error (the difference between the ADC output and input) path has a high-pass response and the desired signal path, a low-pass response. Thus, quantization noise is pushed out of the bandwidth of interest [86].

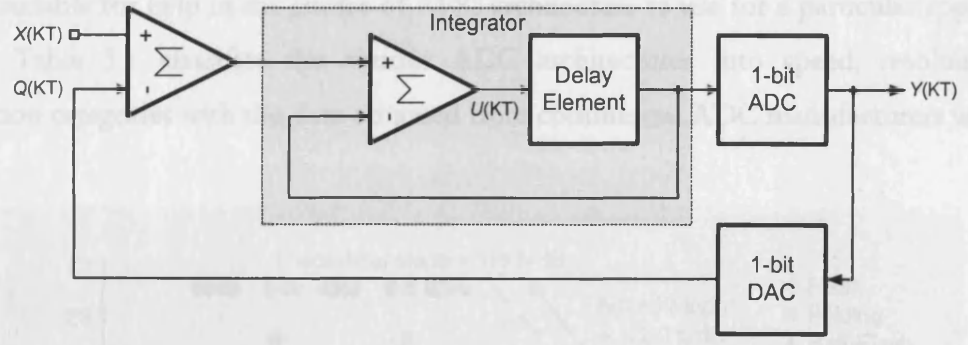


Fig. 3.16 First-order ΔΣ modulator.

Higher order modulators provide better noise shaping. Higher-level quantization (2-bit or more) also improves noise shaping but at the expense of the ADC and DAC deviating from the ideal and necessitating more careful design and dynamic element matching schemes. Increasing the OSR also improves the noise shaping but at the expense of power consumption. Stability issues also have to be addressed for modulators with orders higher than two. As such, it is not uncommon for higher-order modulators to be realized from a cascade of second-order stages. Discrete-Time (DT) ΔΣ modulators consume more power than the Continuous-Time (CT) modulators and require integrators with Gain Bandwidth Product (GBW) an order of magnitude higher than their CT counterparts. CT modulators

have an implicit anti-aliasing filter and consume lower power but are more sensitive to clock jitter and extra loop delay [87] with the minimization of the clock jitter achieved in the literature with the use of switched-capacitor feedback DAC and return-to-zero with constant impulse length signaling schemes [88]. This class of ADC will be further expatiated in Chapter 5.

3.10 Conclusions

This chapter has covered most of the available ADC topologies whilst outlining their theoretical basis and explicating their fundamental limitations. Figs 3.17 and 3.18 are a selection of some of the cutting edge CMOS ADC designs done over the last few years and spanning all architectures [19]. The x-axis in both figures is the logarithm of sampling rate and covers over nine orders of magnitude (Hz to GHz). The y-axis of Fig. 3.17 is the resolution of the ADC and the corresponding axis in Fig. 3.18 the ADC power consumption. It can thus be seen that in spite of the overlap across architectures, some architectural dominance (the pipeline, successive approximation and $\Delta\Sigma$ architectures especially stand out) exist depending on desired resolution, sampling speed and power consumption with the figures suitable for help in the choice of ADC architecture to use for a particular application. Finally, Table 3.1 classifies the various ADC architectures into speed, resolution and application categories with the data obtained from commercial ADC manufacturers websites.

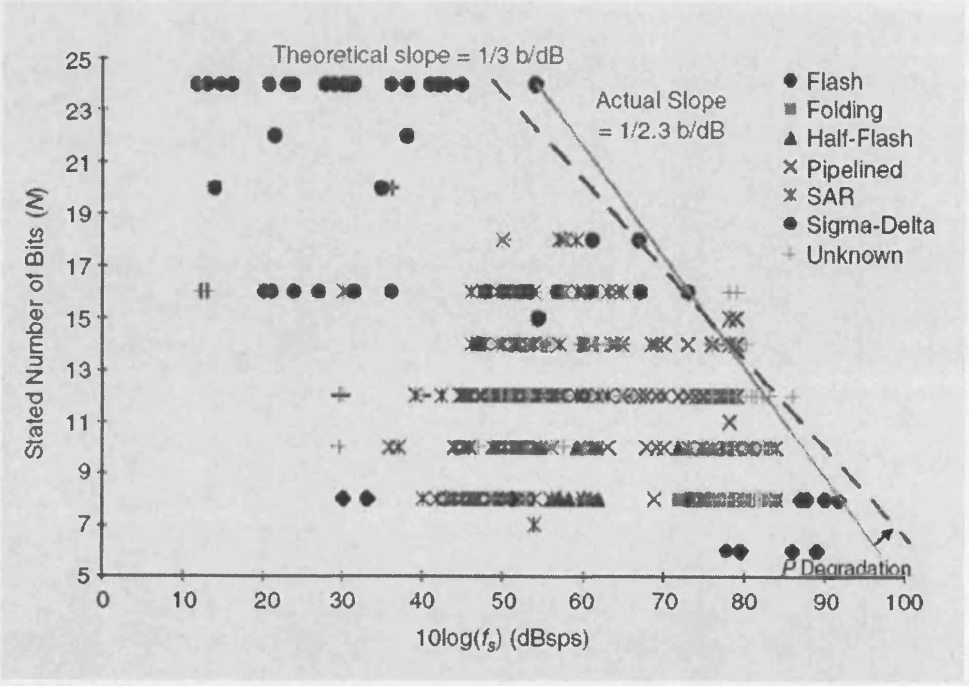


Fig. 3.17 Plot of selected ADC resolution vs. logarithm of sample rate [19].

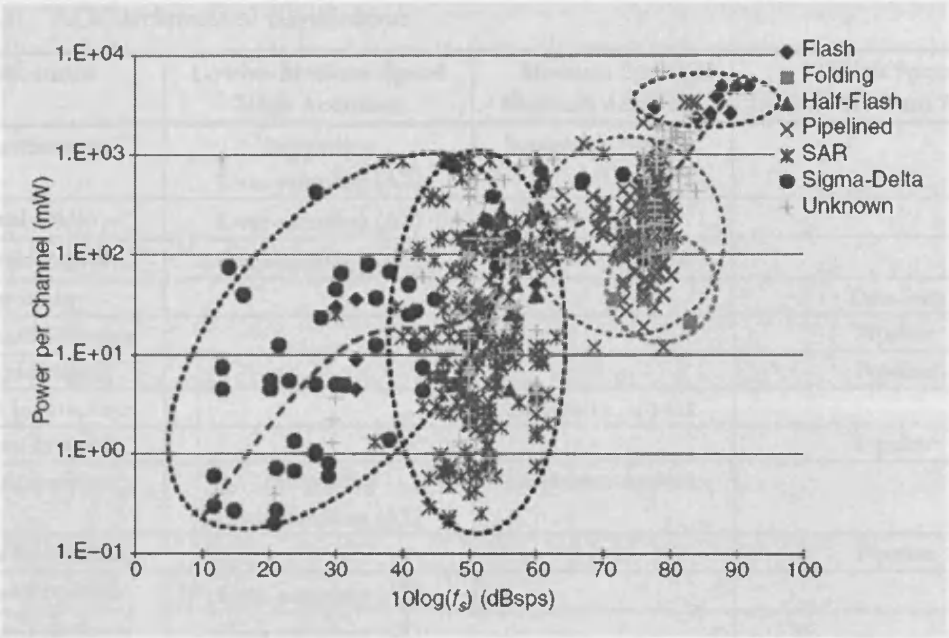


Fig. 3.18 Plot of selected ADC power consumption vs. logarithm of sample rate [19].

Table 3.1 ADC architectural classification.

Applications	Low-to-Medium Speed High Accuracy	Medium Speed Medium Accuracy	High Speed Low-to-Medium Accuracy
Instrumentation	Integrating Over-sampling (ΔΣ)	Successive Approx.	
Digital Audio	Over-sampling (ΔΣ)		
Process Control	Over-sampling (ΔΣ)	Successive Approx.	
Astronomy			Two-Step
Ultrasound Scanners			Pipeline
Medical Imaging			Pipeline
Medical Instruments		Successive Approx.	
Infrared Imaging			Pipeline
Data Acquisition	Integrating Over-sampling (ΔΣ)	Successive Approx.	
Wireless Base-station			Pipeline
Wireless Receivers	Over-sampling (ΔΣ)		
Wire-line Telephony	Over-sampling (ΔΣ)		
Rader			Pipeline
Digital Camera		Algorithmic	Pipeline
Professional Camera			Pipeline
Document Scanners			Pipeline
LCD Displays			Flash/Two-Step
Plasma Displays			Flash/Two-Step
Television			Pipeline
Set-top Box			Pipeline
Video Projectors			Flash/Two-Step
High-Definition TV			Folding/Interpolating Pipeline
ISDN	Over-sampling (ΔΣ)		Pipeline
ADSL	Over-sampling (ΔΣ)		Folding and Interpolation
High-speed Instrumentation			Flash Pipeline
Oscilloscopes			Flash/Two-Step Pipeline
Digital Oscilloscopes			Time-Interleaved Pipeline
Spectrum Analyser			Flash Pipeline Time-Interleaved
Direct RF Conversion			Folding & Interpolation Flash
Direct IF Conversion	Over-sampling (ΔΣ)		Pipeline

4 Pipeline ADC Design for Mobile DVB-H Receivers

'For everyone that asketh receiveth ..." Matt. 7:8 KJV

The pipeline ADC architecture is the most popular topology for video-rate converter designs [89]-[93] because of its comparable speed with the parallel or flash architecture and significantly smaller implementation area and power dissipation. The high-speed performance is possible because inherent to the pipeline architecture is the ability to concurrently process different input samples at the clock rate using a bank of analog 'registers' or stages. Once the pipeline is primed, converted digital data is always available at every clock cycle.

The relatively high bandwidth and moderate resolution required for video digitization already biases the pipeline ADC architecture as the candidate of choice for DVB-T/H [94], [14] with the ΔΣ ADC a close second. The higher clock rate required for ΔΣ ADC even at moderate OSRs translates to increased power dissipation further delineating the pipeline architecture as the one of choice, with the penalty being the requirement of a baseband channel filter with extremely steep roll-off [14]. This chapter thus begins with an overview of DVB-H itself and the system considerations for a DVB-H receiver chain from the antenna to the ADC output. The merits of SiP over SoC as a vehicle for system implementation is then expatiated with some commercial examples used as illustration and justification for the reduced voltage pipeline ADC design given. Subsequently, systematic analysis is done to determine the optimal inter-stage resolution partitioning of the ADC pipeline for lowest power consumption. The optimization results are presented. Detailed circuit design is then carried out for the ADC and experimental results presented for the fabricated silicon.

4.1 DVB-H Overview

This section is an overview of DVB-H and charts the development of the standard from its more established terrestrial sibling. The orthogonal frequency division multiplexing concept is also discussed. Finally, the motivation for the choice of SiP over SoC for the DVB-H subsystem is presented.

4.1.1 DVB Historical Overview

*Until late 1990, digital television broadcasting to the home was thought to be impractical and costly to implement. During 1991, broadcasters and consumer equipment manufacturers discussed how to form a concerted pan-European platform to develop digital terrestrial TV. Towards the end of that year, broadcasters, manufacturers of consumer electronics and regulatory bodies came together to discuss the formation of a group that would oversee the development of digital television in Europe.

This group was called the European Launching Group (ELG) and expanded to include the major European media interest groups, both public and private, the consumer electronics manufacturers, common carriers and regulators. It drafted a Memorandum-of-Understanding (MoU) establishing the rules by which this new and challenging game of collective action would be played. The MoU was signed by all ELG participants in September 1993, with the Launching Group renaming itself the Digital Video Broadcasting Project (DVB). Development work in digital television, already underway in Europe, moved into top gear.

Around this time a separate group, the Working Group on Digital Television, prepared a study of the prospects and possibilities for digital terrestrial television in Europe. The highly respected report introduced important new concepts, such as proposals to allow several different consumer markets to be served at the same time (e.g. portable television and high-definition television, HDTV).

In conjunction with all this activity, change was coming to the European satellite broadcasting industry, and it was becoming clear that the then state-of-the-art satellite systems would have to give way to an all-digital technology. The DVB Project provided the forum for gathering all the major European television interests into one group. It promised to develop a complete digital television system based on a unified approach.

It became clear that satellite and cable would deliver the first broadcast digital television services. Fewer technical problems and a simpler regulatory climate meant that they could develop more rapidly than terrestrial systems. Market priorities meant that digital satellite and cable broadcasting systems would have to be developed rapidly. Terrestrial broadcasting would follow.

By 1997 the development of the DVB Project had successfully followed the initial plans, and the project had entered its next phase, promoting its open standards globally, and making digital television a reality. DVB standards were adopted worldwide and became the benchmark for digital television worldwide.

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* The historical information used in most of Section 4.1.1 was obtained from http://www.dvb.org [2].

The DVB Project expanded into new areas when it took over the activities of the Multimedia Home Platform (MHP) Launching Group. This resulted in the release of the first DVB-MHP specification in June 2000.

In May 2001 a new commercial and technical strategy for DVB (DVB2.0) was adopted to build a content environment that combines the stability and interoperability of the world of broadcast with the vigour, innovation and multiplicity of Internet services.

2003 brought the 10th anniversary of the DVB Project with European content providers already considering using digital television spectrum for transmission to PDAs, mobile phones and laptop computers. This is now called Digital Video Broadcast Handheld (DVB-H) and was ratified as a new mobile DVB handheld technical specification in 2004 [95]. DVB-H, a "one-to-many" broadcast system, is being designed as a mobile transmission standard for terrestrial digital TV. It allows the distribution of music, video or other multimedia content to a very large audience through mobile devices. Extensive testing [10] has validated the new standard's stationary and motional robustness thus gaining it world-wide acceptance and making DVB-H a truly global mobile TV standard.

Finally, commercial rollout of DVB-H services has already begun in Finland with the network going live in 2007. A consortium of DVB-H providers in Germany ran a partial service for the World Cup in June 2006 and will deploy full commercial services by early 2007 [96].

4.1.2 DVB Classification and COFDM Demodulator Architecture

DVB is classified into 3 main transmission specifications namely Digital Video Broadcasting – Satellite (DVB-S), Digital Video Broadcasting – Cable (DVB-C) and Digital Broadcasting – Terrestrial (DVB-T). The new DVB-H specifications add Internet Protocol (IP) packetization, time-slicing and robust forward error correction (FEC) algorithms [97] to the older DVB-T standards to enable coherent reception on a mobile, hand-held, battery-powered device.

DVB-S transmission standard is Quadrature Phase Shift Keying (QPSK) modulation based. DVB-C uses 64-Quadrature Amplitude Modulation (64-QAM). DVB-T, the youngest and the most sophisticated of the three main specifications, is based on Coded Orthogonal Frequency Division Multiplexing (COFDM) and can use QPSK, 16-QAM and 64-QAM modulation schemes. DVB-H is thus more of a mobile receiver standard for the reception of DVB-T services. Fig. 4.1 below is a simplified block diagram of a COFDM demodulator depicted as a "black box" in the DVB-H sub-system illustrated in Fig. 1.1.

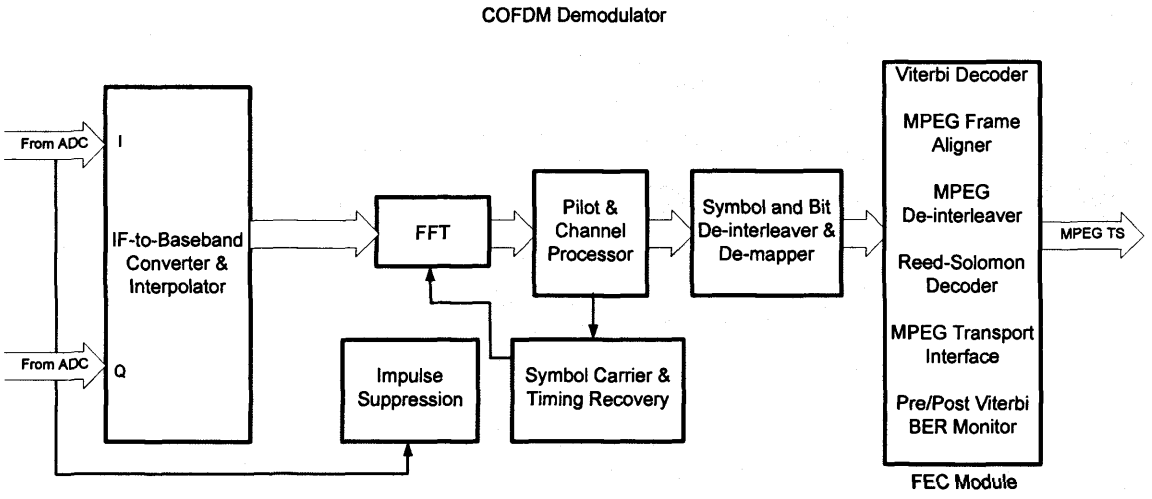

Fig. 4.1 Block diagram of a COFDM demodulator.

Sampling for example, a hypothetical 36.389 MHz Intermediate Frequency (IF) signal using a 20.48 MS/s ADC results in a digital, spectrally inverted OFDM signal centred at 4.571 MHz. Spectral restoration is done by the IF-to-Baseband Converter/Interpolator block. Adjacent undesirable channels down-sampled with the desired IF (i.e. analogue near instantaneous compander and multiplexer, NICAM signals) are filtered prior to the Fast Fourier Transform (FFT) block. The Symbol Carrier & Timing recovery block calibrates out frequency offsets and helps determine the optimum point to trigger the FFT in order to minimize Inter-Symbol Interference (ISI). The Symbol and Bit De-interleaver block restores all the bits interleaved in carriers and all the carriers interleaved in symbols by the transmitter to their original order. Interleaving is usually done to the data before transmission to enhance the performance of the receiver's convolutional decoder in the presence of multi-path delay effects.

Forward Error Correction (FEC) and Frame alignment is done by the FEC module using convolutional (Viterbi) and Reed-Solomon block decoding. The MPEG Transport Interface finally outputs the MPEG-2 video and audio broadcast data in parallel or serial format depending on the application requirements. A dedicated MPEG decoder ASIC (or software) will then extract the desired video and audio information from the MPEG Transport Stream (MPEG TS). The section below tersely describes the COFDM modulation scheme and the process of DVB-T data encapsulation and transmission.

4.1.3 COFDM Fundamentals

OFDM is a modulation and multiplexing technique that allows the robustness of the system to multi-path propagation, fading and interference – problems prevalent in the simpler Phase Shift Keying (PSK) and QAM based digital modulation systems. In a single carrier system, a swift increase in the number of errors is exhibited as the signal level is reduced (fading) or interference level is increased. In a multi-carrier system, on the other hand, only a small percentage of the sub-carriers will be affected. Error correction coding can then be used to correct for erroneous sub-carriers. The concept of using parallel data transmission and Frequency Division Multiplexing (FDM) was published in the mid 1960s with a U.S patent filed and issued in January 1970 [98].

In the classical FDM, the signal frequency band is divided into N non-overlapping frequency sub-channels. Each sub-channel is modulated with a separate symbol and then the N sub-channels are frequency multiplexed. Avoidance of spectral overlap of channels is done to eliminate inter-channel interference, but this leads to inefficient use of the available spectrum. To improve spectral efficiency, the mid 1960 methods proposed the overlapping of the sub-channels in which each channel carrying a signaling rate s, is spaced s Hz apart in frequency (orthogonality) to avoid the use of high-speed equalization and to combat impulsive noise and multi-path distortions.

Coded Orthogonal Frequency Division Multiplexing (COFDM) is thus OFDM with forward error correction channel coding applied to facilitate its use in highly selective channels (i.e. DVB-T). Fig. 4.2 shows that a savings of about 50% in bandwidth is achieved by using OFDM over classical FDM (N here is sub-carrier number and R, sub-carrier spacing). The equation below gives the orthogonality condition for a pair of sub-carriers at frequencies $g\omega$ and $b\omega$:

$$\begin{aligned} \int_{\pi}^{\pi} (\sin g\omega t \cdot \sin b\omega t) d\omega t &= 0, g \neq b \\ &= \pi, g = b \end{aligned} \tag{4.1}$$

The word orthogonal means there is a precise mathematical relationship between the frequencies of the carriers in the system. Thus, with the orthogonality requirements of (4.1) obeyed, it is possible to receive all signals in the overlapped sidebands without adjacent channel interference. The receiver translates each sub-carrier to DC and integrates the resulting signal over a symbol period to recover the raw data. If the other sub-carriers alias down to frequencies that, in the time domain, have an integer number of cycles within the symbol period, T, then the integration process results in zero contribution from all these

other sub-carriers. Thus, the sub-carriers are linearly independent if the sub-carrier spacing is a multiple of $1/T$.

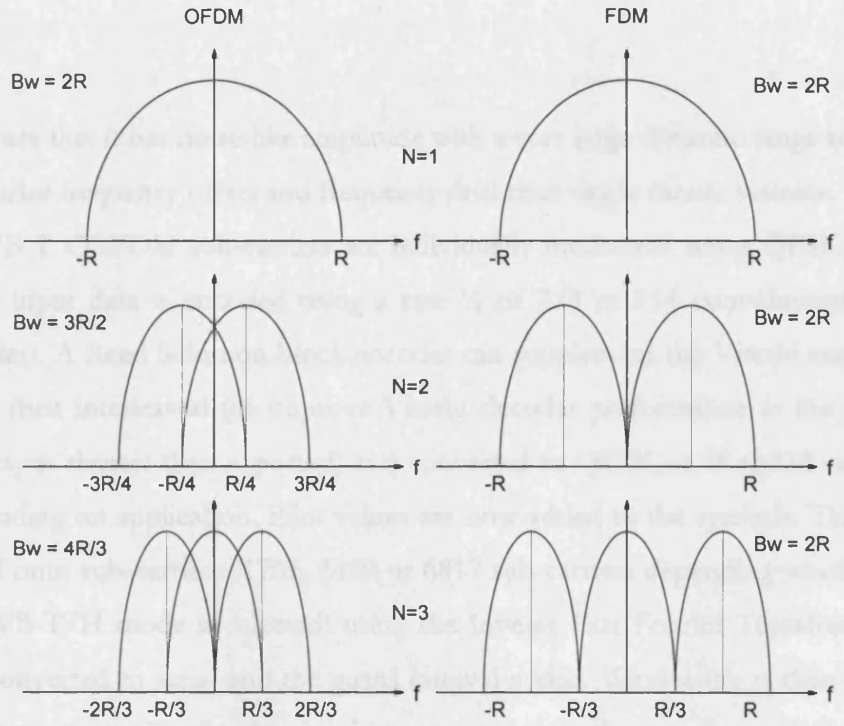

Fig. 4.2 OFDM multi-carrier technique vs. FDM multi-carrier technique.

If a Discrete Fourier transform (DFT) is done at the receiver, and correlation values are calculated with the centre frequency of each sub-carrier, the transmitted data is received with no crosstalk. Completely digital implementations of the Fast Fourier Transform, FFT (an efficient implementation of the DFT requiring $N \log N$ operations rather than N^2) can thus be done eliminating the banks of sub-carrier oscillators and coherent demodulators necessary for FDM. COFDM thus has the following advantages:

- Makes efficient use of the spectrum by allowing overlap as explained above.
- More resistant to frequency selective fading as a result of the large number of carriers and the inclusion of channel state information in the transmitted data.
- Lost symbols can be recovered with adequate channel coding and time/frequency interleaving of coded data prior to OFDM carrier assignment and modulation.
- Inter-Symbol Interference and Inter-Frequency Interference can be eliminated with the use of a cyclic prefix (guard interval).

- Maximum likelihood convolutional decoding, i.e. soft-decision Viterbi decoding can be used with reasonable complexity.
- Provides good protection against co-channel interference and impulsive parasitic noise.

Its drawbacks are that it has noise-like amplitude with a very large dynamic range and is more sensitive to carrier frequency offset and frequency drift than single carrier systems.

The DVB-T COFDM sub-carriers are individually modulated using QPSK or QAM. Firstly, binary input data is encoded using a rate ½ or 2/3 or 3/4 convolutional encoder (Viterbi encoder). A Reed Solomon block encoder can supplement the Viterbi encoder. The coded data is then interleaved (to improve Viterbi decoder performance at the receiver if multi-path delay is shorter than expected) and converted to QPSK or 16 QAM or 64 QAM symbols depending on application. Pilot values are now added to the symbols. The symbols are modulated onto sub-carriers (1705, 3409 or 6817 sub-carriers depending whether 2 K, 4 K[†] or 8 K DVB-T/H mode is selected) using the Inverse Fast Fourier Transform (IFFT). Outputs are converted to serial and the guard interval added. Windowing is then applied to get a narrower spectrum. Finally, the signal is converted to analogue using an I-Q modulator and up-converted to UHF, amplified and then transmitted through the antenna. A reverse process now occurs at the receiver as explained in Section 4.1.2.

4.1.4 SoC or SiP for DVB-H?

Fig. 4.3 illustrates the implementation of the entire RF-to-DSP DVB-H subsystem on silicon using the SoC and SiP methods.

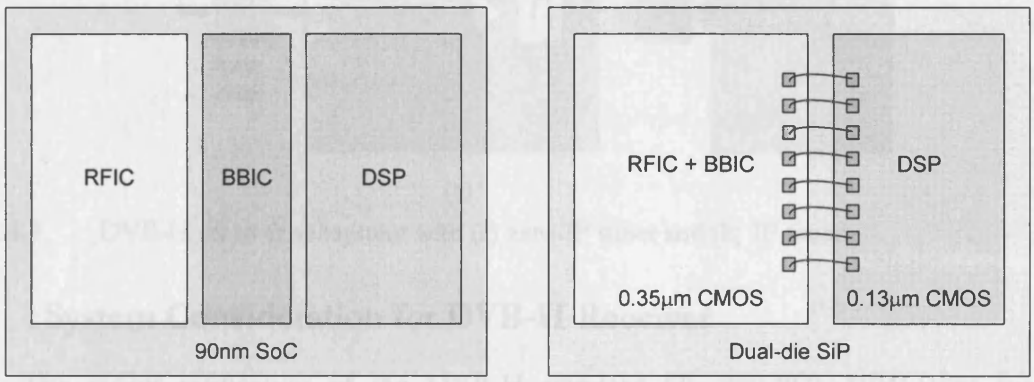

Fig. 4.3 SoC and SiP methods for the DVB-H sub-system silicon implementation

[†] 4 K mode is new to DVB-H and was added to improve network planning flexibility [96].

Monolithic RFIC, BBIC and DSP SoC design is non-trivial [99]-[100], can be prone to yield issues and expensive for less than 0.18 μm CMOS process technology. System in a Package (SiP) is a more compelling, higher yield and cost-effective option with more efficient system partitioning across cheaper process technologies [101]-[102]. The SoC vs. SiP comparison work in [103] gives a more balanced view of the issue primarily because in wireless cellular handset design, the terms SoC and SiP may be a misnomer since in either case, multiple dies will be enclosed in a package to reduce overall printed circuit board footprint.

Designing CMOS mixed-signal sub-systems in an SiP at reduced voltages in lower-cost sub-micron technologies (say 0.35 μm) eliminates the need for level translators between them and the finer-line (e.g. 0.13 μm) all-digital sub-systems when multiple dies are used in a lateral or stacked (3-D) SiP, translating to significant cost savings in comparison with an expensive monolithic SoC designed in an advanced (say 90 nm) technology.

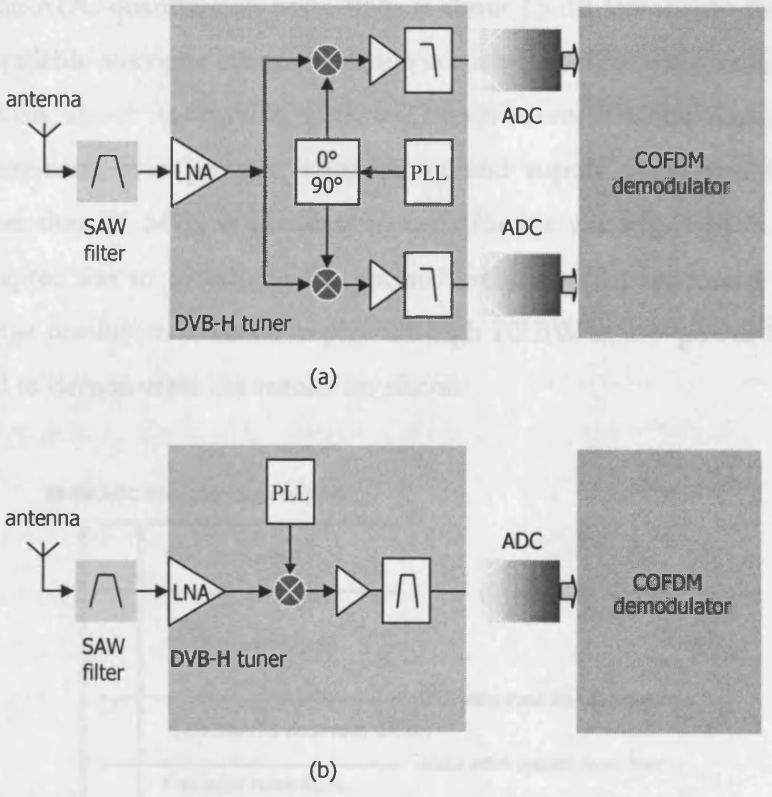

Fig. 4.4 DVB-H receiver subsystem with (a) zero-IF tuner and (b) IF tuner.

4.2 System Consideration for DVB-H Receiver

The recent ratification of the DVB-H standard [2], [95]-[97], [104]-[105] for the reception of TV programs on battery-powered mobile phones and personal digital assistants (PDAs), has created a great demand for power efficient ADCs with wide input-bandwidth and low-voltage operation. Such wide-bandwidth converters are suitable for both direct-

conversion (Fig. 4.4a) and IF conversion (Fig. 4.4b) DVB-H receiver architectures adding flexibility to the receiver design. The IF-conversion architecture may be preferred because it alleviates the local oscillator re-radiation, front-end linearity and baseband dc offset problems of the direct-conversion architecture [106], requiring only a single high Effective Resolution Bandwidth (ERBW) ADC to directly sub-sample the IF signal (typically between 30-70 MHz in DVB-H). The ERBW of an ADC is the input frequency at which the ADC effective number of bits (ENOB) degrades by 0.5 LSB. With the incessant shrinking of CMOS process technology feature length and the reduction of area overhead in the implementation of robust DSP algorithms, an alternative option may be to employ the lower-area, infinite image-rejection (theoretically), zero-IF architecture in spite of the above mentioned pitfalls and utilize advanced DSP algorithms to eliminate the I and Q impairments [107] thereby restoring the distorted symbol constellation.

Fig. 4.5 shows the antenna-referred partitioning of the DVB-H receiver dynamic range [95], [105]. If the ADC quantization noise floor is about 15 dB lower than the thermal noise floor and the available analogue channel filtering is such that all blocker levels are attenuated to a residual 15 dB, about 50 dB ADC SNR will be sufficient. A 10-bit ADC can more than meet this requirement over process, temperature and supply variations. In addition, an ERBW of higher than 70 MHz is adequate to cater for the various DVB-H tuner IFs. The goal of this chapter was to determine the optimal architectural partitioning of the pipeline ADC's inter-stage resolution in order to provide high ERBW at low-power for the DVB-H application, and to demonstrate the results on silicon.

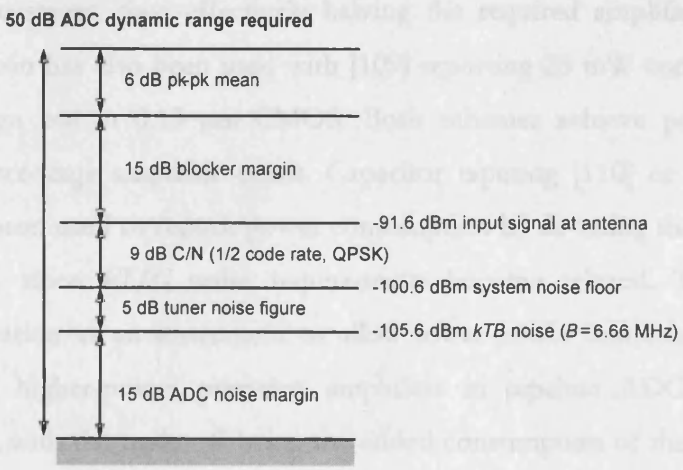

Fig. 4.5 ADC dynamic range specification.

4.3 Architectural Analysis of Pipeline ADC Design for DVB-H

Fig. 4.6 shows the block diagram of a generic pipeline ADC consisting of an input Sample-and-Hold Amplifier (SHA) and k cascaded pipeline stages, each resolving m bits.

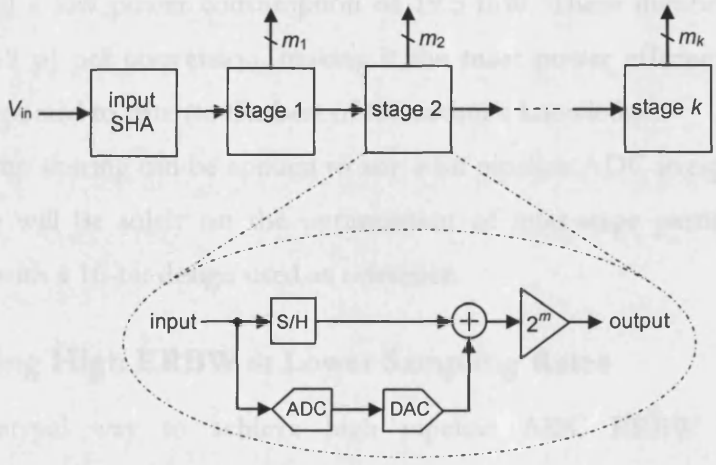

Fig. 4.6 Generic pipeline ADC block diagram.

The principal contributors to power consumption are the SHA and inter-stage amplifiers with the sub-ADC comparators increasing in number and consuming more power for higher inter-stage resolutions. The input SHA is usually omitted to reduce overall power consumption but at the expense of ADC aperture error which will be explained in Section 4.3.1. A slight increase in the resolution of the first ADC stage can also help to alleviate the noise requirement and power consumption of subsequent stages in the pipeline.

A number of approaches have been used in the literature for the reduction of power consumption in pipeline ADCs with [108] proposing the concept of opamp sharing between successive pipeline stages, thus effectively halving the required amplifier count. Multi-bit inter-stage resolution has also been used with [109] reporting 28 mW consumption for a 80 MS/s 10-bit design but in 0.13 μm CMOS. Both schemes achieve power reduction by decreasing the inter-stage amplifier count. Capacitor tapering [110] or scaling across the pipeline has also been used to reduce power consumption by de-rating the capacitor size for subsequent stages since kT/C noise requirements become relaxed. The use of digital background calibration as an instrument to allow lower-power imprecise amplifiers to be used in place of higher-power precision amplifiers in pipeline ADC design has been proposed in [111], with the trade-off being the added consumption of the calibration engine versus the power savings with the use of imprecise amplifiers.

The basics is revisited by analyzing the classical pipeline architecture to determine optimal inter-stage partitioning for low-power and high ERBW 10-bit ADC design at *reduced*

supply voltages for the SiP reasons promulgated in Section 4.1.4. A 1.5-V, 20.48 MS/s, 10-bit pipeline ADC suitable for sub-sampling a DVB-H tuner IF output is subsequently designed to validate the analysis. The ADC was fabricated in a standard 3.3-V, 0.35 μm CMOS technology, employs an optimal 2.5-2.5-2.5-4 bits-per-stage pipeline topology, has an ERBW of 100 MHz and a low power consumption of 19.5 mW. These numbers yield an energy efficiency of 0.19 pJ per conversion, making it the most power efficient 10-bit video-rate pipeline ADC reported to date (to the best of the author's knowledge).

Since opamp sharing can be applied to any *n*-bit pipeline ADC irrespective of bits-per-stage, the focus will be solely on the optimization of inter-stage partitioning at reduced supply voltages with a 10-bit design used as reference.

4.3.1 Achieving High ERBW at Lower Sampling Rates

The archetypal way to achieve high pipeline ADC ERBW for sub-sampling applications is to precede the pipeline with a wide-bandwidth dedicated SHA. Once the SHA has converted the input signal to the discrete-time domain, the pipeline can now quantize the held signal accurately without overly contributing signal-dependent distortion or noise. The drawback of the input SHA is significant increase in power consumption for the overall ADC. As a result, this block is removed leading to aperture timing error [112]-[113], the relative uncertainty between sub-ADC and Multiplying Digital-to-Analog Converter (MDAC) input signal sampling points (and not actual sampling clock jitter issues). This needs to be addressed by the matching of the first-stage MDAC and sub-ADC comparator sampling networks in terms of topology and time-constants (Fig. 4.7). To further explicate this, consider that the ADC input is a high-frequency signal of

$$V_{\text{in}}(t) = A\sin(2\pi f_{\text{in}} t) \tag{4.2}$$

where A is the amplitude and f_{in} is the signal frequency. The slope of this signal is steepest as it passes through its zero-crossing point (e.g., $t = 0$). Evaluating the derivative of (1) at $t = 0$ yields

$$\frac{\mathrm{d}V_{\text{in}}(t)}{\mathrm{d}t} = A2\pi f_{\text{in}} \tag{4.3}$$

The aperture timing error, Δt can then be given by

$$\Delta t = \frac{V_{\text{error}}}{A2\pi f_{\text{in}}} \tag{4.4}$$

where V_{error} is the amplitude error (or noise) as a result of aperture uncertainty. If V_{error} is to be less than ±0.5 LSB for an n-bit ADC, maximum allowable aperture timing error becomes

$$\Delta t_{max} = \frac{1}{2^{n+1} \cdot 2\pi f_{in}} \tag{4.5}$$

or 0.8 ps for a 10-bit ADC sub-sampling a 100 MHz signal. Similar analysis as in (4.2) to (4.5) is also valid for the estimation of the pipeline ADC sampling clock jitter requirements. This jitter equally affects the MDAC and the sub-ADC with 0.8 ps as obtained from (4.5) being the maximum clock jitter that the sub-sampling pipeline ADC can tolerate.

For an n-bit pipeline ADC with m-bit inter-stage resolution and digital error correction implemented, (4.5) becomes

$$\Delta t_{pipeline\_max} = \frac{1}{2^{m+1} \cdot 2\pi f_{in}} \tag{4.6}$$

with the maximum tolerable aperture timing error being relaxed to about 200 ps for a 2.5 bits-per-stage 10-bit pipeline ADC.

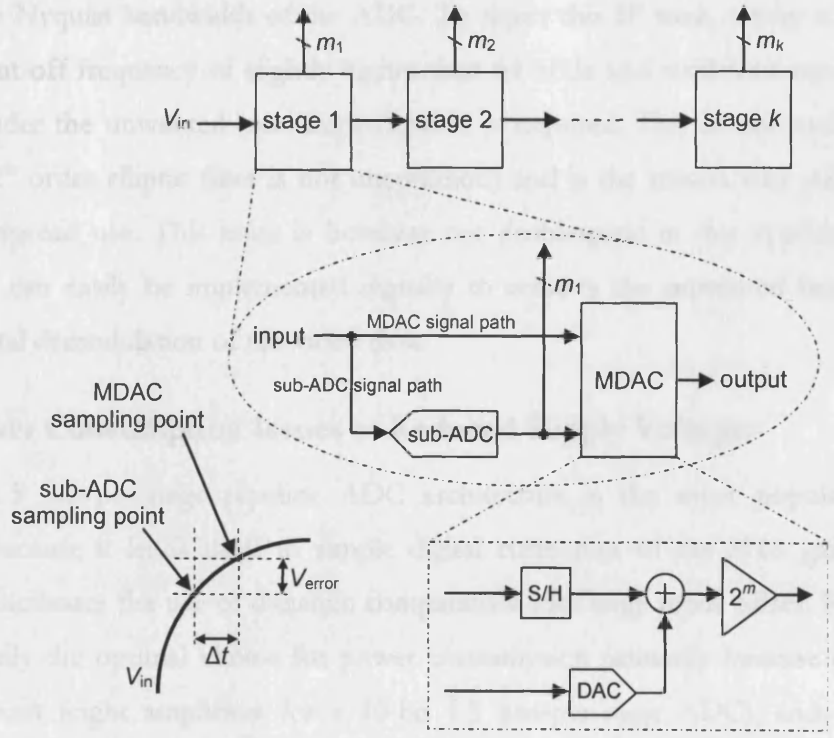

Fig. 4.7 Pipeline ADC block diagram illustrating the aperture error problem.

To minimize aperture uncertainty between the first MDAC and sub-ADC comparator paths as shown in Fig. 4.7, the clock distribution buffer must be appropriately sized to increase the clock edge slope. In addition, the following relation must approximately hold for

the first sub-ADC's comparator pre-amplifier and MDAC input network time-constants [113]:

$$\frac{C_{\text{comp}}}{g_{m\_\text{comp}}} \approx R_{\text{switch}} \cdot C_{S1} \tag{4.7}$$

where g_{m_comp} is the first sub-ADC's comparator preamplifier transconductance, C_{comp} is the comparator pre-amplifier's input capacitance, R_{switch} is the first MDAC sampling switch on-resistance, and C_{S1} is the first MDAC sampling capacitor. Finally, the closed-loop bandwidths of the MDAC Operational Transconductance Amplifier (OTA) and the comparator must be slightly higher than, or of similar order as their input network time-constants to minimize metastability errors.

It must also be mentioned at this stage that sub-sampling ADCs are particularly susceptible to noise and IF out-of-band signals folding in-band. For example, if a hypothetical 64 MHz IF signal is sub-sampled at 20 MS/s and there exists another signal at 66 MHz, two tones, the wanted at 4 MHz and the unwanted at 6 MHz will show up within the 10 MHz Nyquist bandwidth of the ADC. To reject this IF tone, a very steep anti-alias filter with cut-off frequency of slightly higher than 64 MHz and sufficient attenuation at 66 MHz to render the unwanted tone imperceptible is required. This is extremely difficult to design (a 12^{th} order elliptic filter is not uncommon) and is the reason why sub-sampling is not in widespread use. This issue is however not problematic in this application because steep filters can easily be implemented digitally to remove the unwanted baseband signal prior to digital demodulation of the video data.

4.3.2 Power Consumption Issues at Reduced Supply Voltages

The 1.5 bits-per-stage pipeline ADC architecture is the most popular inter-stage resolution because it lends itself to simple digital correction of the SHA gain and offset errors, and facilitates the use of dynamic comparators with large input offset. However, it is not necessarily the optimal choice for power consumption primarily because of the higher amplifier count (eight amplifiers for a 10-bit 1.5 bits-per-stage ADC), and the fact that amplifier power consumption in switched capacitor circuits actually increases at reduced supply voltages [114], [115]. The latter may be explained as described in [115] and repeated here for completeness: Firstly, power consumption for a single-stage CMOS amplifier (i.e., an OTA) is proportional to the product of the bias current and supply voltage

$$P \propto I_{\text{bias}} \times V_{DD}. \tag{4.8}$$

Secondly, for accurate settling into a capacitive load C_L, the OTA GBW has to be much higher than the sampling frequency f_s, hence

$$\text{GBW} \approx 10 f_s \propto \frac{G_m}{C_L} \tag{4.9}$$

with $G_m \propto C_L$, where G_m is the OTA transconductance. At the onset of slewing, I_{bias} must be large enough to charge or discharge C_L at the Slew-Rate (SR), hence

$$I_{bias} \propto C_L . \tag{4.10}$$

Thirdly, the Signal-to-(thermal) Noise Ratio ($SN_{th}R$) of the high-resolution ADC for which the OTA will be used is given by

$$SN_{th}R \propto \frac{(\alpha V_{DD})^2 C_L}{kT} \tag{4.11}$$

where $0.25<\alpha<0.75$ typically; T is the absolute temperature and k is the Boltzmann's constant. From (4.8), (4.9) and (4.11), it can be seen that the following relation holds

$$P \propto \frac{kT(SN_{th}R)}{\alpha V_{DD}} \tag{4.12}$$

showing that for a given $SN_{th}R$, OTA power consumption is *inversely proportional* to supply voltage using the same CMOS process technology. For a fixed $SN_{th}R$ high ERBW ADC design, power consumption increases for both larger geometry CMOS processes (as a result of lower MOS transistor transconductance parameter, K and higher device parasitics requiring more supply current), and newer smaller geometry CMOS technologies (as a result of lower operating supply voltages necessitating larger sampling capacitors in order to still meet desired $SN_{th}R$ in spite of compromised input voltage swing) with [116] suggesting an optimum geometry of circa 0.25 μm – 0.35 μm.

Higher inter-stage resolutions help to mitigate the higher power consumption issue for low-voltage ADCs, since MDAC amplifier count is reduced. Multi-bit first-stage quantizers have been used in the literature primarily to relax the linearity requirements of subsequent stages rather than for power reduction with [117] achieving 85 dB SFDR without trimming, calibration or dithering for a 14-bit ADC at 340 mW using a 4-bit first-stage quantizer. Some prior work has been done on the optimization of pipeline stages with [118] proposing an optimum of between 3-to-4 bits-per-stage but with the use of a time-multiplexed architecture that employed two opamps per-stage, which is not power efficient. A cascade of 3-3-3-3-3-3-3 for a 5 V, 5 MS/s, 15-bit pipeline ADC design was proposed in [72] as simultaneously optimal in both power consumption and area. However, [72] and [118] focused on higher-

voltage ADC designs where the challenges of input/output swing limitations, amplifier settling accuracy and increase in power consumption as a result of reduced supply voltages were not an issue.

Some approximate mathematical relations exist for the n-bit overall resolution, m.5-bit inter-stage resolution pipeline ADC component count in Fig. 4.7 (exact count can only be obtained empirically from desired ADC architectural partitioning), and are given by

$$N_{\text{amplifier}} \approx \frac{n-2}{m} \tag{4.13}$$

$$N_{\text{comparator}} \approx \left(\frac{n}{m}\right)\left(2^{m+1}-2\right) \tag{4.14}$$

$$N_{\text{flip-flop}} \approx (m+1)\left(\frac{N_{\text{amplifier}}+1}{2}\right)\left(N_{\text{amplifier}}+2\right). \tag{4.15}$$

Equation (4.13) is an approximation of the total number of MDAC amplifiers required for the n-bit $m.5$-bits-per-stage ADC, i.e. for a 10-bit 1.5-bit-per-stage ADC, eight amplifiers are required. Equation (4.14) approximates the total number of comparators required for all sub-ADCs and (4.15) the total flip-flop count for the ADC's digital pipeline with all other ancillary logic excluded.

4.3.3 Amplifier Power Consumption

Fig. 4.8 is the simplified diagram of a typical ADC MDAC. The MDAC uses a single amplifier to realize the SHA and residue amplification functions. At the first-phase (ϕ_1), the input signal is sampled onto C_S (sampling capacitor). The sub-ADC (Fig. 4.7) also samples the signal at this instance with the DAC providing the quantized value (V_{DAC}) of the input signal.

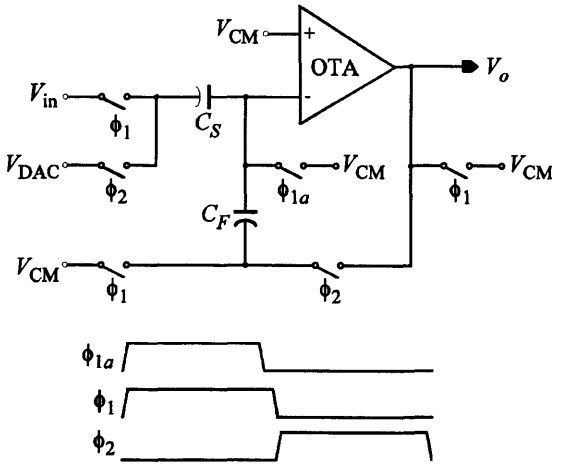

Fig. 4.8 Simplified ADC MDAC diagram.

At the second-phase (ϕ_2), the sampled signal is subtracted from the DAC output and held on the amplifier feedback capacitor C_F. The ratio of C_F to C_S gives the amplifier feedback factor f, where $f = 2^{-m}$. By holding the amplifier input at the common-mode voltage (V_{CM}) during sampling, the effect of amplifier input parasitic capacitance on C_S is alleviated. If a single-pole roll-off characteristic is assumed, ADC ERBW can be approximated by ERBW $\approx$ GBW$\times f$ where GBW is the amplifier's gain-bandwidth product. The total load capacitance seen by the MDAC amplifier is given by

$$C_L = (1+f)C_F + C_S + C_{\text{sub-ADC}} + C_p \tag{4.16}$$

where $C_{\text{sub-ADC}} = (2^{m+1}-2)C_{\text{comp}}$ is the total sub-ADC comparator input capacitance and C_p is the amplifier output node parasitic capacitance.

Assuming an n-bit ADC design is required to accommodate a maximum peak-peak input signal of amplitude A, the minimum input amplitude (*rms* value) it can process is $A/(2^n\sqrt{12})$. Referring all inter-stage sampling capacitor kT/C noise to the ADC input, the ADC *rms* noise voltage is given by

$$V_{\text{noise\_rms}} = \sqrt{kT\left(\frac{1}{C_{S1}} + \frac{1}{2^m C_{S2}} + \frac{1}{2^{2m} C_{S3}} + \ldots + \frac{1}{2^{\{(n/m)-1\}m} C_{S\{(n/m)-1\}}}\right)} \tag{4.17}$$

where C_{Si} the ith-stage sampling capacitor. From (4.17) it can be seen that the dominant contributor to ADC thermal noise is the first-stage sampling capacitor. The first-stage also defines overall ADC ERBW as elucidated in Section 4.3.1. Switch on-resistance noise, amplifier noise and clock phase noise contribute to the overall ADC noise floor but are usually designed to contribute much less (typically < 20 dB) than kT/C to overall system noise and are not considered further in this analysis. If $\sqrt{(kT/C)}$ noise voltage is to be less than $\pm$0.5 LSB of the ADC, the desired first-stage sampling capacitor size is given by

$$C_{S1} = \frac{48kT2^{2n+1}}{A^2}. \tag{4.18}$$

Combining (4.16) and (4.18) and the fact that $C_F = f \cdot C_S = 2^{-m}$, the total load the MDAC OTA will see (if no capacitor scaling is used) is given by

$$C_L = \left(\frac{2^{2m}+2^m+1}{2^{2m}}\right)\left(\frac{48kT2^{2n+1}}{A^2}\right) + (2^{m+1}-2)C_{\text{comp}} + C_p. \tag{4.19}$$

In addition, the OTA needs to have a dc gain of greater than $2^{(n+m)}$ to guarantee n-bit settling accuracy. Possible candidate OTA topologies for the target 10-bit ADC are the gain-

enhanced telescopic OTA, the gain-enhanced folded-cascode OTA and the two-stage Miller OTA.

4.3.3.1 Single-Stage OTA

The fully-differential gain-enhanced telescopic OTA (Fig. 4.9) is suitable for high-gain and high-speed applications, with gain boosting provided by the two auxiliary amplifiers (A_1 and A_2), each designed to consume about 1/8 of main OTA current.

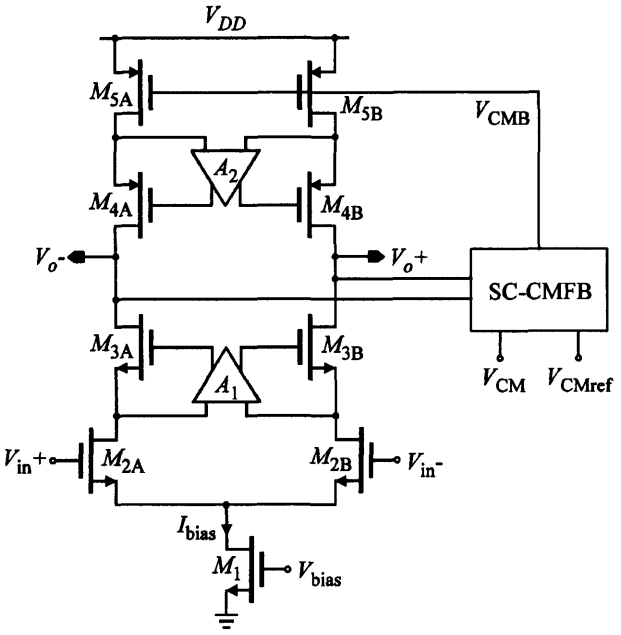

Fig. 4.9 Fully-differential gain-enhanced telescopic OTA schematic.

Maximum differential output swing for this topology is

$$V_{o\_max} = 2\{V_{DD} - (V_{OD1} + V_{OD2} + V_{OD3} + V_{OD4} + V_{OD5})\} \tag{4.20}$$

where V_{ODi} is the overdrive voltage for transistor M_i. Its main drawback is that only about 1-V_{ppd} output swing is available at 1.5 V supply voltage (with transistor overdrive voltages of about 0.2 V), but its low input-referred noise voltage allows the use of reduced input amplitude whilst still exceeding 10-bit ADC requirements. It also consumes about half the power of a gain-enhanced folded-cascode OTA of comparable performance. Its output common-mode level may be stabilized by a Switched Capacitor Common-Mode FeedBack (SC-CMFB) circuit and frequency compensation provided by its load capacitors C_L. A first-order system can be used to model its settling characteristics. For such a system, the response to a step input is given by

$$V_o(t) = A(1 - e^{-t/\tau}) \tag{4.21}$$

where τ is the time-constant. The relative error term ε (i.e., the normalized difference between the ideal output and actual output), is thus given by

$$\varepsilon = \frac{A - V_o}{A} = e^{-t/\tau} \tag{4.22}$$

An n-bit design requires that ε is less than $1/2^{(n+1)}$ within half a sampling period. Thus, the settling time (in time-constants) including an additional time-constant for slewing overhead is

$$\tau_{\text{settling}} = [1 + (n+1)\ln 2]\tau . \tag{4.23}$$

Hence, the SR of the fully-differential single-stage OTA used in an f_s-samples/s ADC is given by

$$\text{SR} = 2f_s A[1 + (n+1)\ln 2] = I_{\text{bias}}/2C_L . \tag{4.24}$$

Substituting (4.19) in (4.24) yields the required current consumption of the OTA (excluding auxiliary amplifier consumption)

$$I_{\text{bias}} = 4f_s A[1 + (n+1)\ln 2] \times \left\{ \left(\frac{2^{2m} + 2^m + 1}{2^{(2m-2n-1)}} \right) \left(\frac{48kT}{A^2} \right) + (2^{m+1} - 2)C_{\text{comp}} + C_p \right\} \tag{4.25}$$

where $C_p \approx C_{gd3} + C_{db3} + C_{gd4} + C_{db4}$. The product of (4.13), (4.25) and V_{DD} yields the total ADC amplifier power consumption. The OTA GBW is given by

$$\text{GBW} = \frac{\sqrt{2K_n I_{\text{bias}}(W_2/L_2)}}{2\pi C_L} \tag{4.26}$$

and the ADC ERBW then becomes

$$\text{ERBW} = \frac{2^{-m}\sqrt{2K_n I_{\text{bias}}(W_2/L_2)}}{2\pi C_L} . \tag{4.27}$$

To maximize ERBW at low-voltage, the output node parasitic capacitances have to be minimized (difficult given the 0.2 V overdrive voltage target), and input transistors aspect ratio (W_2/L_2) maximized to the optimal point beyond which their parasitic capacitances reduce the closest non-dominant pole frequency and curtails the obtainable ERBW.

4.3.3.2 Two-Stage Miller OTA

If a higher ADC full-scale voltage is required, the fully-differential Miller OTA with a telescopic first-stage (Fig. 4.10) is a good choice.

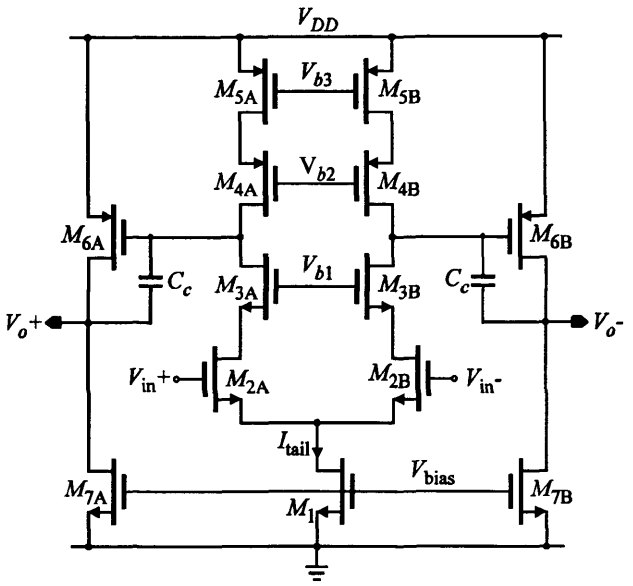

Fig. 4.10 Fully-differential Miller OTA schematic.

Maximum differential output swing for this topology is

$$V_{o\_max} = 2\{V_{DD} - (V_{OD6} + V_{OD7})\} \tag{4.28}$$

and is about 2-V_{ppd} at 1.5 V supply voltage (with transistor overdrive voltages of about 0.25 V). Frequency compensation is provided by capacitors C_c. The well-known second-order settling characteristics can be used to model its settling dynamics. For a step input, the output of a second-order system is given by

$$V_o(t) = A\left[1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-(\zeta/\tau)t} \sin\left(\frac{\sqrt{1-\zeta^2}}{\tau}t + \arctan\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right] \tag{4.29}$$

where ζ is the system damping constant ($\zeta = 0.6125$ is required for a Phase Margin (PM) of 60°). For PM < 76°, the total under-damped settling time (to the relative accuracy $\varepsilon = 1/2^{(n+1)}$) including an additional time-constant for slewing overhead is roughly approximated by [119]

$$\tau_{settling} = \left\{1 + \frac{2}{k_s}\left[(n+1)\ln 2 - \frac{1}{2}\ln\left(1 - \frac{k_s}{4}\right)\right]\right\}\tau \tag{4.30}$$

where $k_s = \sin^2(\text{PM})/\cos(\text{PM})$. Hence, the SR of the fully-differential Miller OTA used in an f_s-samples/s ADC is given by

$$\text{SR} = 2f_s A\left\{1 + \frac{2}{k_s}\left[(n+1)\ln 2 - \frac{1}{2}\ln\left(1 - \frac{k_s}{4}\right)\right]\right\} = I_{bias}/2C_c \tag{4.31}$$

where C_c is about $0.22C_L$ for 60° PM if $g_{m6} \approx 10g_{m2}$. However, it is more realistic for C_c to be about $0.5C_L$ for $g_{m6} \approx 4g_{m2}$ (or even $C_c = C_L$ for $g_{m6} \approx 2g_{m2}$), otherwise, transistors M_6 become prohibitively large, contribute even further to the output nodes parasitics and consume more power if sized for $g_{m6} = 10g_{m2}$. For $C_c = C_L$, the drain current of M_{6A} (and M_{6B}) is $2I_{bias}$. Hence, total OTA current consumption is

$$I_{total} = 20 f_s A\left\{1+\frac{2}{k_s}\left[(n+1)\ln 2-\frac{1}{2}\ln\left(1-\frac{k_s}{4}\right)\right]\right\} \times\left\{\begin{array}{l}\left(\frac{2^{2m}+2^m+1}{2^{(2m-2n-1)}}\right)\left(\frac{48kT}{A^2}\right) \\ +(2^{m+1}-2)C_{comparator}+C_{parasitics}\end{array}\right\} \quad (4.32)$$

The product of (4.13) and (4.32) and V_{DD} yields the total ADC amplifier power consumption. The OTA GBW is approximately that of the single-stage OTA and is given by

$$\text{GBW} \approx \frac{\sqrt{2K_n I_{bias}(W_2/L_2)}}{2\pi C_L} \quad (4.33)$$

and the ADC ERBW then becomes

$$\text{ERBW} \approx \frac{2^{-m}\sqrt{2K_n I_{bias}(W_2/L_2)}}{2\pi C_L} . \quad (4.34)$$

For comparable settling and GBW at reduced supply voltages, the differential Miller OTA will consume about four times the power of the gain-enhanced telescopic OTA but with twice the output swing. As a result, the best OTA choice for high ERBW and minimal power consumption is the single-stage OTA. It may be argued that a doubling in amplitude requirement translates to a quartering of the sampling capacitor size for the Miller OTA whilst allowing consumption levels to approach that of the single-stage OTA, but the single-stage OTA will still settle quicker because of its inherent first-order settling characteristics and higher frequency non-dominant poles and is thus preferred.

4.3.4 Comparator Power Consumption

For ≤ 3.5 bits-per-stage resolution, dynamic comparators can be used for the inter-stage ADCs since they do not consume power at dc. However, they will need to be preceded by continuous-time preamplifiers to reduce the effect of clock feed-through and switch charge injection on the signal and reference voltages. These preamplifiers are designed for low gain (< 10) and comparable SR with the inter-stage amplifiers. For > 3.5 bits-per-stage resolutions, auto-zeroing comparators [120] are required to meet the higher accuracy

requirements consuming more power. In general, the power consumption of a single comparator can be approximated by

$$P_{\text{comparator}} \approx \sqrt[3]{m} V_{DD} \left[\text{SR} (C_{\text{preamp}} + C_{\text{latch}}) + I_K f_s \right] \tag{4.35}$$

where C_{preamp} and C_{latch} are the parasitic capacitance at the preamplifier output node and the regenerative latch input capacitance, respectively. The $m^{1/3}$ parameter is included to model comparator accuracy effect on power consumption as bits-per-stage increases. I_K is a parameter that represents the current consumed by the dynamic portions of the comparator as the clock waveforms cross the device switching thresholds and is about 2 μA/MHz for the target 0.35 μm CMOS technology. The product of (4.35) and (4.14) gives the total consumption of all sub-ADCs.

4.3.5 Flip-Flop and Clock Generator Power Consumption

Power dissipation in digital CMOS circuits is given by [121]

$$P_{\text{digital}} = p_r (C_p V_{DD}^2 f_{\text{clk}}) + I_{\text{static}} V_{DD} + I_{\text{leakage}} V_{DD} . \tag{4.36}$$

The first term in (4.36) represents the dynamic power dissipation, p_r is the probability that a switching activity will occur, C_p is the loading capacitance and f_{clk} is the clock frequency. The second and third terms in (4.36) represent the static and leakage power consumption, respectively. In a well-designed digital circuit using sub-micron CMOS technologies, the static and leakage dissipation are generally small enough to be negligible (this is not the case for deep sub-micron 90 nm and 65 nm technologies as leakage is actually significant and can be quite dominant). Hence, the dynamic dissipation is dominant with p_r ranging between 0.2 and 0.8. Standard D flip-flop cells are used in the design with the technology vendor providing the normalized switching dissipation parameter for all logic devices. The dissipation parameter for a D-flip-flop is about 1.14 μW/MHz.

4.3.6 Results of Optimization

The analysis addressed above has been applied to the design of three 1.5 V, 10-bit pipeline ADCs with $f_s \approx$ ERBW/5 (f_s = 1 MS/s, 20.48 MS/s and 100 MS/s) and with m varying from 1 to 5 bits (1.5 to 5.5 bits with redundancy included). Both single-stage gain-enhanced OTAs and two-stage Miller OTAs were consecutively used in the pipeline ADC modeling. The MDACs were modeled for two consumption scenarios: power-scaled (subsequent pipeline stages' MDAC capacitors are reduced to correspond with the lower kT/C requirements) and non-power-scaled (the same first-stage MDAC is used for all

pipeline stages), using CMOS level-1 equations in Matlab® with parameters for the available 3.3-V, 0.35 μm CMOS technology (V_{Tp} = -0.65 V, V_{Tn} = 0.5 V, K_p = 58 μA/V^2, K_n = 170 μA/V^2). In another scenario, a 4.5-bit sub-ADC was used for only the first stage and the modeling repeated as explained above, with and without power scaling for the single-stage MDAC OTA. In all, 6 scenarios were modeled (single-stage OTA with and without power scaling, Miller OTA with and without power scaling and 4.5-bit sub-ADC1/single-stage OTA with and without capacitor scaling). The results presented represent the total power consumption of all stages of the pipeline ADC at each of the 3 sampling rates. The size of the first MDAC sampling capacitor was 2 pF to meet 1-V_{ppd} thermal noise requirements. The following assumptions were made in the modeling:

- Power consumption of the clock generator and digital error correction blocks is equivalent to that of 40 flip-flops clocked at the ADC sample rate.
- No extra ancillary logic for calibration functionality.
- Regularity of pipeline bits-per-stage (i.e. for 2.5 bits-per-stage, 2.5-2.5-2.5-2.5-2 partitioning is used) except for the case where a 4.5-bit sub-ADC was used in the first-stage of the pipeline with regularity subsequently maintained.
- Minimum feedback capacitor size of 100 fF is assumed whenever the calculated value as a result of power-scaling is 100 fF or less. This is to guarantee feedback ratio precision in the chosen technology.
- Ideal inter-stage DACs are assumed.
- Sub-ADC comparators are exactly the same for all pipeline stages.
- ADC input amplitude is 1-V_{ppd} for both OTA topologies.

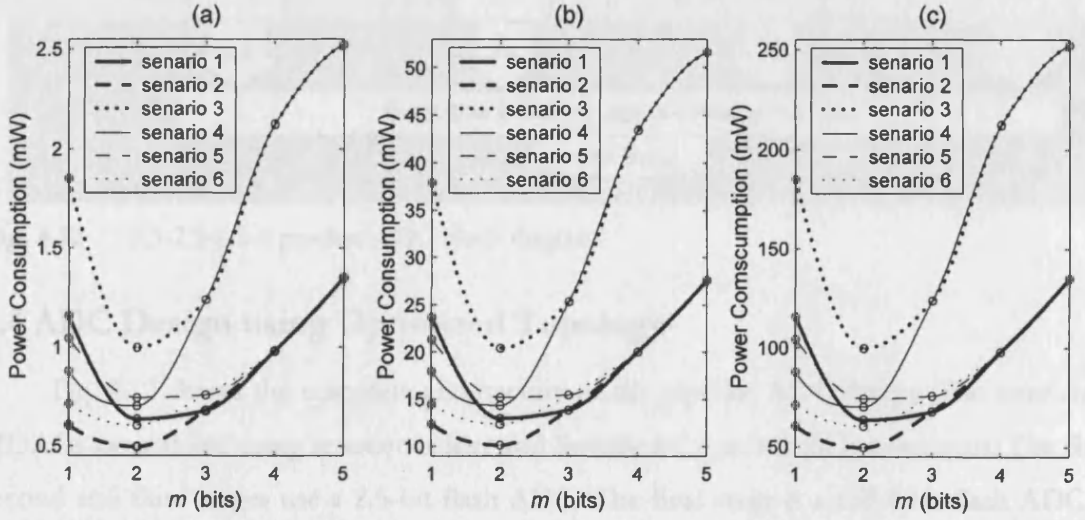

Fig. 4.11 ADC optimization results with f_s = (a) 1 MS/s, (b) 20.48 MS/s and (c) 100 MS/s.

A plot of all results is shown in Figs. 4.11(a), 4.11(b) and 4.11(c) respectively for (a) f_s = 1 MS/s, (b) f_s = 20.48 MS/s, and (c) f_s = 100 MS/s. The 6 scenarios considered are: scenario 1 (thick solid line) – single-stage MDCA OTA without capacitor scaling, scenario 2 (thick dashed line) – single-stage MDAC OTA with capacitor scaling, scenario 3 (thick dotted line) – two-stage MDAC OTA without capacitor scaling, scenario 4 (thin solid line)– two-stage MDAC OTA with capacitor scaling, scenario 5 (thin dashed line) – single-stage MDAC OTA with 4.5-bit first-stage sub-ADC and without capacitor scaling, and scenario 6 (thin dotted line) – single-stage MDAC OTA with 4.5-bit first-stage sub-ADC and with capacitor scaling.

From these plots it can be concluded that 2.5 bits-per-stage partitioning is optimal for 10-bit resolution with or without capacitor scaling and irrespective of OTA topology and sampling rate. For this inter-stage resolution, scenario 2 (single-stage MDAC OTA with capacitor scaling) is the best option for lowest overall ADC power consumption. The next best option is scenario 6 (single-stage MDAC OTA with capacitor scaling and with a 4.5-bit first stage sub-ADC), whereas scenario 3 (two-stage Miller OTA without capacitor scaling) is the worst choice. The next section describes the circuit design of the prototype 1.5 V, 20.48 MS/s, 10-bit ADC for DVB-H receivers to validate the architectural partitioning analysis. The ADC uses the gain-enhanced telescopic OTA, but MDAC sampling capacitor scaling was not used due to lack of layout optimization time.

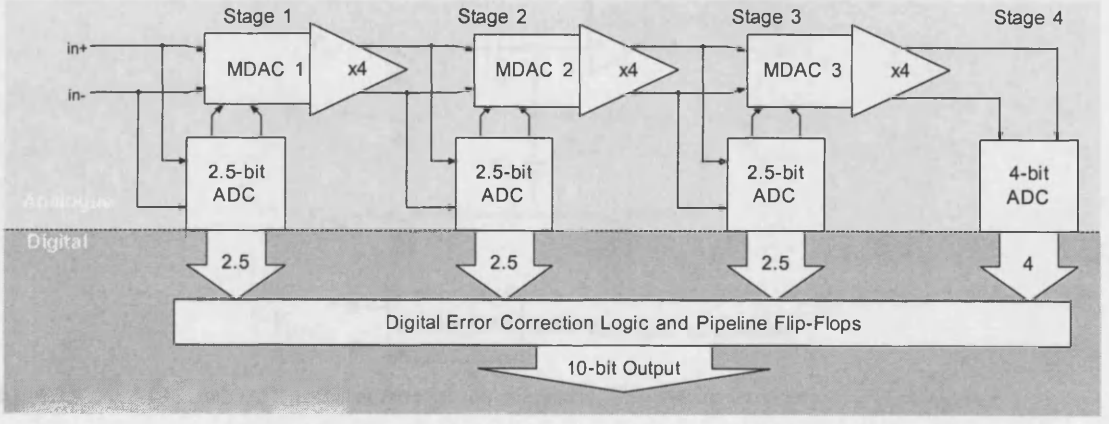

Fig. 4.12 2.5-2.5-2.5-4 pipeline ADC block diagram.

4.4 ADC Design using Optimized Topology

Fig. 4.12 shows the complete architecture of the pipeline ADC design. The inter-stage MDACs are realized using resistive ladder and Switched Capacitor (SC) techniques. The first, second and third stages use a 2.5-bit flash ADC. The final stage is a full 4-bit flash ADC to slightly reduce amplifier count by 1. Fully-differential signal and reference paths are used for

the entire ADC. Clock generator and biasing circuits were also designed but are not considered here for brevity.

4.4.1 MDAC/SHA

Each MDAC comprises a SHA and a resistive DAC. The latter uses the reference ladder of the flash sub-ADC to reduce reference power consumption. The sub-ADC comparator outputs are boosted and used to switch out the correct ladder voltage onto the DAC output nodes. Since the first MDAC's input sampling switches discretely sample a time-variant input signal, they need to be highly linear to reduce the signal distortion introduced as a result of sampling. All other switches (and in fact, *all* subsequent MDAC sampling switches) sample a completely settled time-invariant discrete-time signal and as such do not introduce distortion, do not have to be highly linear and can be made smaller in size than the sampling switches. The MDAC sampling switches are thus bootstrapped [115] to linearise them. Fig. 4.13 shows the MDAC architecture with the highly linear bootstrapped switches highlighted.

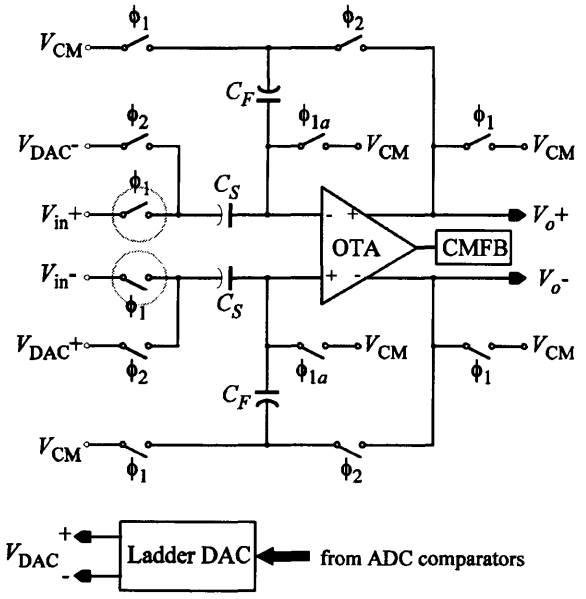

Fig. 4.13 ADC MDAC architecture block diagram. The linear switches are highlighted.

The circuit operation is as follows. At ϕ_1, the first MDAC samples the input signal onto sampling capacitor C_S. At the falling edge of ϕ_1, the signal is frozen onto C_S. The DAC gives the analog representation of the ADC digital output. Capacitor C_F is now flipped across the OTA. At the same instant, the top plate of C_S is connected to the DAC output. The OTA differential output finally settles to $(C_S/C_F) \times (V_{in} - V_{DAC})$ within half a period. At the falling

edge of ϕ_2, the succeeding stage repeats the procedure using the output of the preceding stage as its input signal. A SC-CMFB network (Fig. 4.14) is used to regulate the output common-mode level without increasing OTA power consumption.

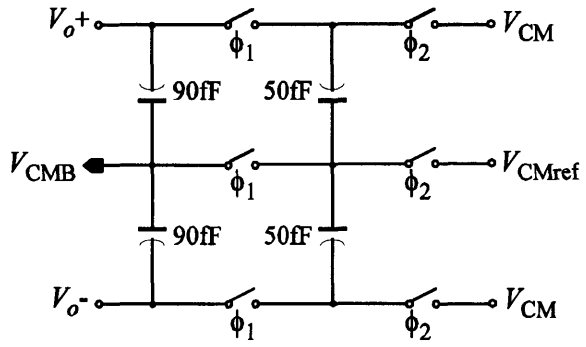

Fig. 4.14 Switched-capacitor CMFB circuit.

A 2 pF sampling capacitor is used in the design to give additional margin on thermal noise floor albeit with some dissipation overhead. The OTA closed-loop bandwidth (ADC ERBW) is designed to be of the same order as the comparator and sampling switch time-constant in order to minimize the first-stage aperture error.

4.4.2 MDAC Switch Design

Two sets of *n*MOS switches were thus designed for the MDAC; one with its gate boosted to almost twice the 1.5 V supply voltage to reduce its on-resistance and the other bootstrapped [115] by superimposing the input voltage (V_{in}) at the switch's source terminal on the supply voltage (V_{DD}) connected to the switch's gate when switch is on. This then keeps the gate-to-source voltage constant with varying input signal ($V_G = V_{DD} + V_{in}$; $V_{GS} = V_{DD}$) ensuring that the bootstrapped switch's on-resistance is virtually constant with varying input voltage. Figs. 4.15 and 4.16 are the schematics of the switches with their associated circuits. Since a standard 3.3-V CMOS technology was used for this work, the boosted switches were utilized well within their normal operation conditions.

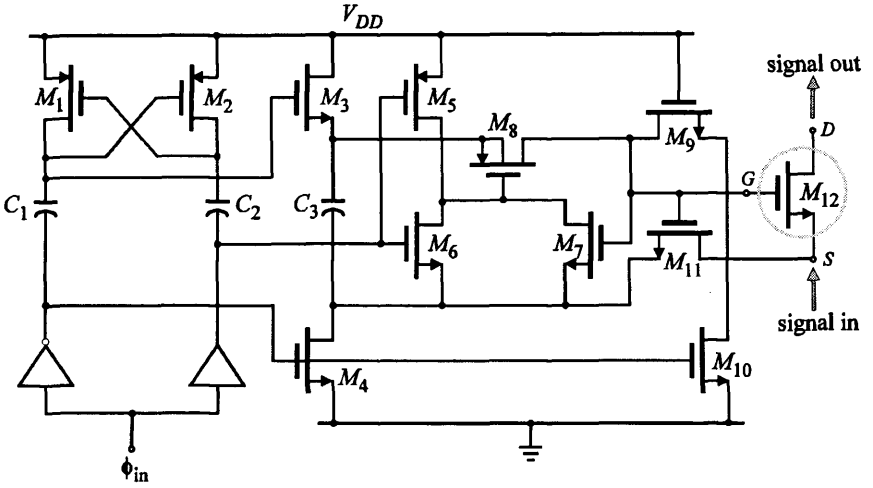

Fig. 4.15 Bootstrapped switch (M_{12}) schematic [115].

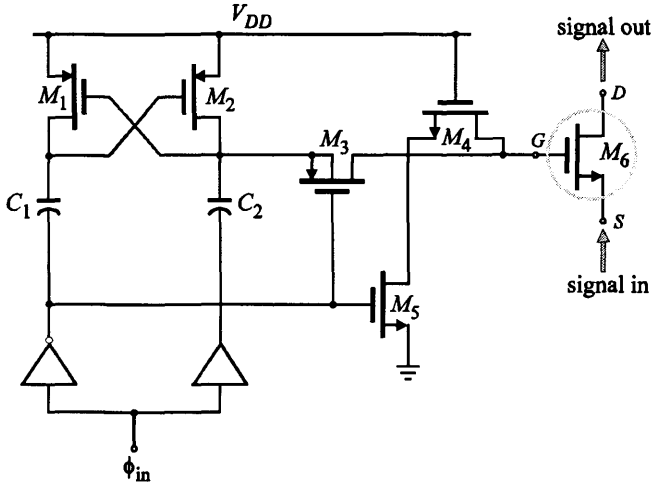

Fig. 4.16 Boosted switch (M_6) schematic.

The bootstrapped switch circuit operates as follows. Initially there is no charge on the three capacitors and upon ϕ_{in} going low, the top plate of C_2 is pushed momentarily high and M_2 (and M_3) are turned on. M_2 pulls the top plate of C_2 to V_{DD}, which turns M_1 on. The top plates of C_1, C_2 and C_3 are then kept floating at V_{DD}. M_4 pulls the bottom plate of C_3 to 0V. M_5 stays on ensuring that charge transfer transistor M_7 remains off. Series transistors M_9 and M_{10} hold the gate of the switch (M_{12}) at approximately 0V, thus the switch is effectively off. Upon ϕ_{in} going high, the top plate of C_2 is pushed to about $2V_{DD}$. M_1 comes on and maintains the top plate of C_1 at V_{DD} keeping M_2 and M_3 off. The top plate of C_3 is left floating at V_{DD}. C_3 then forms a battery across M_7 turning it on. M_{11} and M_{12} also turn on with M_{11} keeping the bottom plate of C_3 at V_{INPUT} by feedback action enabling it to hold the gate-to-source voltage of M_{12} constant at V_{DD} for all input voltages.

The operation of the boosted switch is simpler. When the top plate of C_2 is pushed to about $2V_{DD}$ as ϕ_{in} goes high, M_3 applies the boosted potential (less some drop across M_3) to the gate of M_6. When ϕ_{in} goes low, M_4 and M_5 combine to pull the gate of M_6 to 0V. M_4 is placed in series with M_5 to ensure that M_5 sees a maximum potential of V_{DD} (rather than $2V_{DD}$) across its channel. Figs 4.17(a) and 4.17(b) compare the on-resistance and the 5 MHz tone frequency spectrum for both switches (aspect ratio of 32 μm/0.35 μm). The second harmonic at the output of the bootstrapped switch is more than 10 dB lower than for the boosted switch.

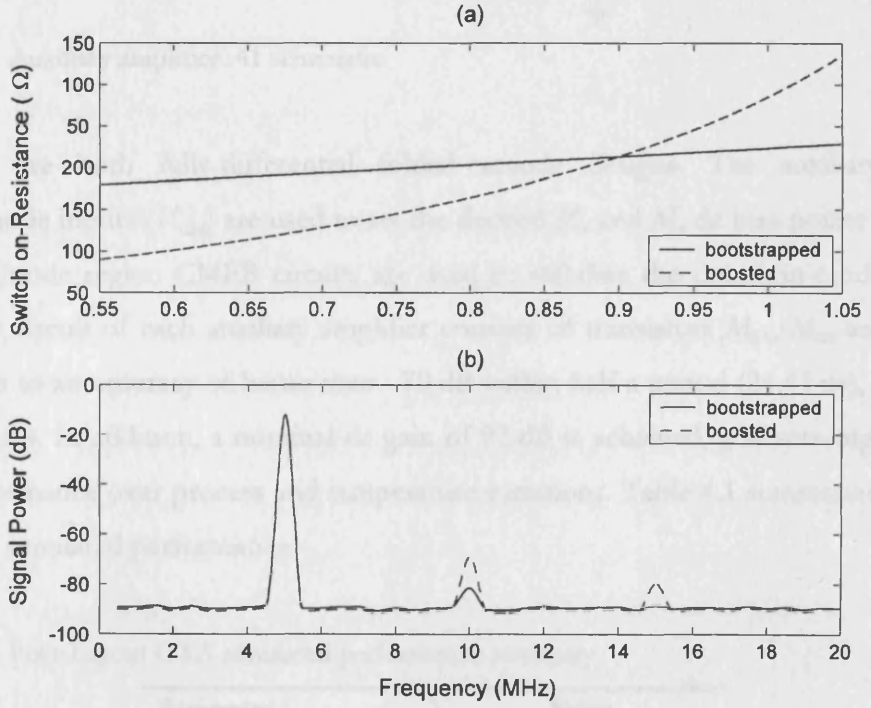

Fig. 4.17 Simulated bootstrapped and boosted *n*MOS switch resistance and spectrum

4.4.3 SHA OTA

As mentioned in Section II-F, the gain-enhanced telescopic OTA (Fig. 4.9) was chosen, primarily because of its fast-settling with lower power consumption than other OTA topologies. The regulation of cascode transistors M_3 and M_4 using the auxiliary amplifiers A_1 and A_2 enhances their output impedances, significantly increasing dc gain and preserving the desired GBW. A SC-CMFB circuit is used to average the differential outputs and regulate M_5 biasing (V_{CMB}) accordingly. The CMFB clocks are boosted to guarantee low switch on-resistance at 1.5 V supply voltage. Fig. 4.18 is the schematic of auxiliary amplifier A_1 (A_2 is a flip version of A_1 with *n*MOS inputs).

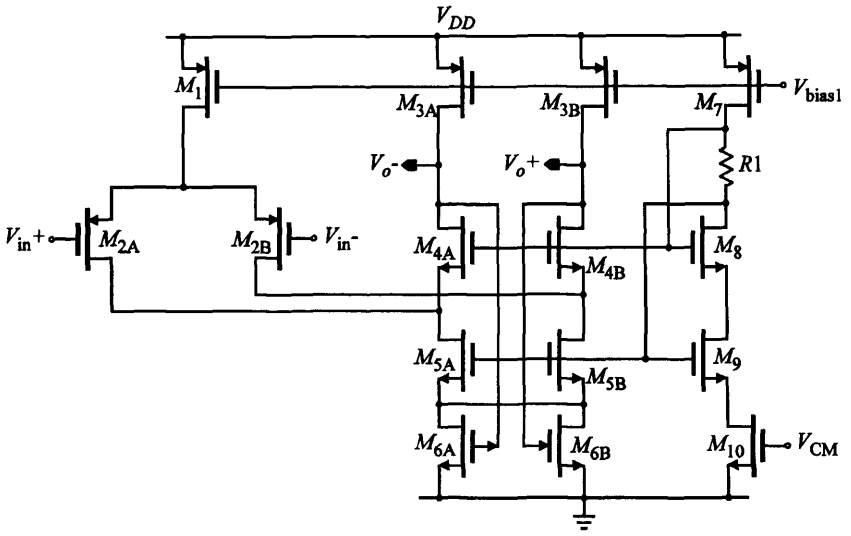

Fig. 4.18 Auxiliary amplifier $A1$ schematic.

They are both fully-differential folded-cascode designs. The auxiliary amplifier common-mode inputs (V_{CM}) are used to set the desired M_3 and M_4 dc bias points in the main amplifier. Triode region CMFB circuits are used to stabilize the common-mode response. The CMFB circuit of each auxiliary amplifier consists of transistors M_{6A}, M_{6B} and M_{10}. The OTA settles to an accuracy of better than –70 dB within half a period (24.41 ns), at a closed-loop gain of 4. In addition, a nominal dc gain of 92 dB is achieved, guaranteeing more than 72 dB performance over process and temperature variations. Table 4.1 summarizes the OTA post-layout simulated performance.

Table 4.1 Post-Layout OTA simulated performance summary.

Parameter	Value
DC gain	92 dB
GBW	560 MHz
Phase margin	62°
SR	450 V/μs
Differential CMOR	1.38 V
Input-referred noise	8 nV/√Hz
24.4 ns settling	-70 dB
Supply voltage	1.5 V
Power consumption	3.75 mW
Area	0.03 mm²

4.4.4 Dynamic Comparator

Fig. 4.19 depicts the differential comparator used for the flash ADCs. It is a modification of the dynamic comparators described in [120] and [122] dissipating zero power at dc and allowing the use of a differential reference.

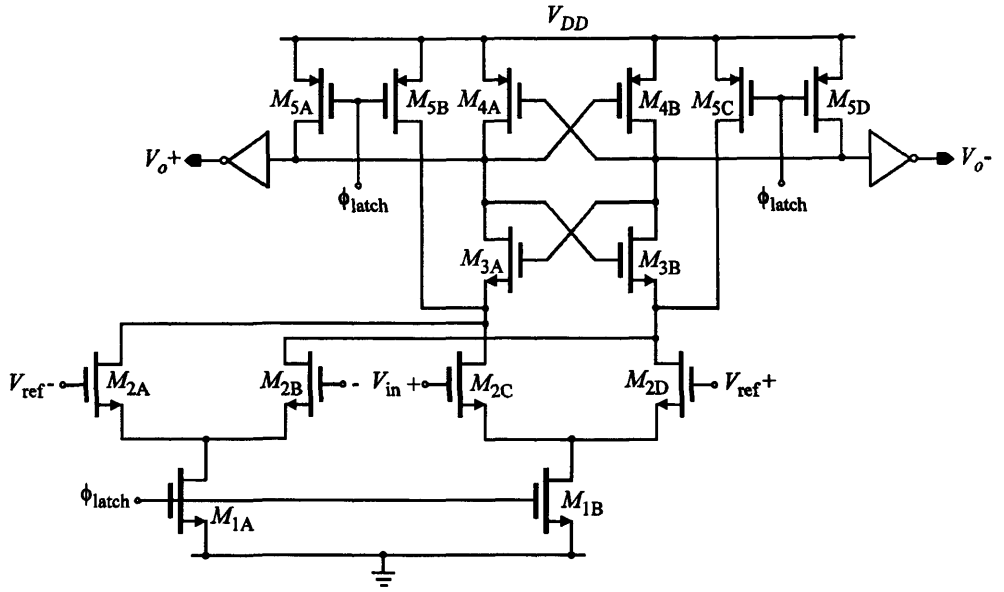

Fig. 4.19 Dynamic comparator schematic.

When ϕ_{latch} is low, M_{1A} and M_{1B} are off and the regenerative latch (M_{3A}, M_{3B}, M_{4A}, M_{4B}) is in *reset*-mode. Switch transistors M_{5A}, M_{5B}, M_{6A} and M_{6B} pull the outputs of the latch and gain transistors (M_{2A}, M_{2B}, M_{2C}, M_{2D}) to V_{DD}, to allow a shorter recovery time when the comparator leaves the reset-mode. As ϕ_{latch} goes high, the gain transistors turn on, amplifying the differential signal at the inputs which is further amplified by the positive feedback action of the latch as the comparator goes into *latch*-mode. The latch output is then applied to inverters sized in such a way as to lower the threshold point to prevent errors as a result of comparator metastability. Thus, all outputs remain at zero until the comparator has enough overdrive to cause one output to toggle high. To mitigate charge injection and kickback effects, the dynamic comparator is preceded by a continuous-time, fully-differential preamplifier with resistive loading (not shown). Total power consumption of a single preamplifier and comparator stage is about 220 μW.

4.5 Experimental Results

The converter was fabricated in the austriamicrosystems 0.35 μm CMOS process [123]. Fig. 4.20 is a microphotograph of the converter.

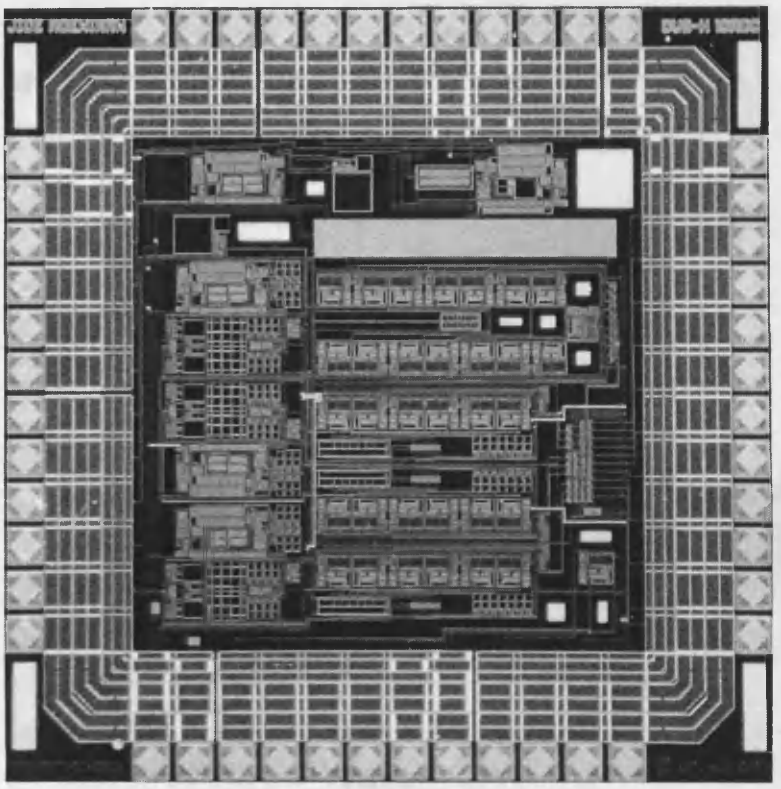

Fig. 4.20 ADC chip microphotograph.

The device was mounted on an evaluation board and a transformer (Mini-Circuits T1-1T) used to convert the single-ended output of the signal generator to the differential signals required by the ADC. A 9th order elliptic filter was used for anti-aliasing the ADC inputs to enable characterization of the ADC for up to 100 MHz input signals. Fig. 4.21 is the block diagram of the test-bench setup.

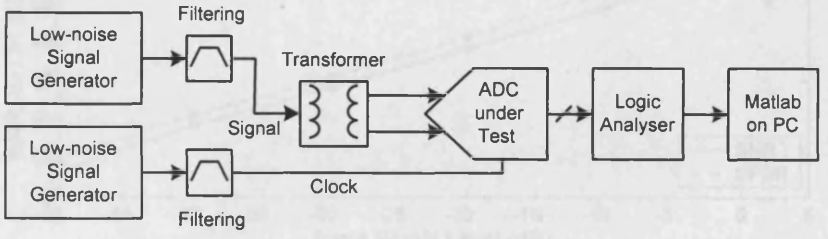

Fig. 4.21 ADC test-bench setup.

2^{16} data samples were acquired per test using a logic analyzer (Hewlett Packard 16700 mainframe). This was then transferred via a floppy disk to a computer for analysis using Matlab®. SNR and SFDR performance was evaluated at 20.48 MS/s using a 4.1 MHz tone. Linearity performance data was acquired for a 9.742 kHz tone and processed using the

histogram method. Twenty fabricated samples were received in total with 100% device yield. Fig. 4.22 shows the ADC output spectrum for a full-scale 4.1 MHz tone.

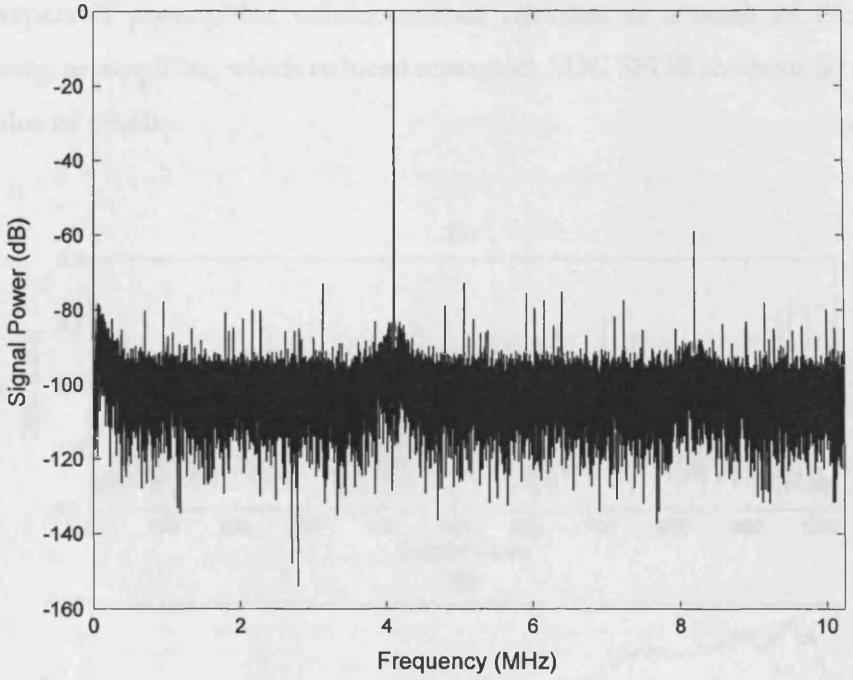

Fig. 4.22 ADC power spectrum with 4.1 MHz tone.

Fig. 4.23(a) is the SNR and SFDR performance versus input signal amplitude. Fig. 4.23(b) is the ADC SNR and SFDR versus input signal frequency with good SNR performance up to the ERBW of 100 MHz, proving that the ADC is excellent for IF sub-sampling applications.

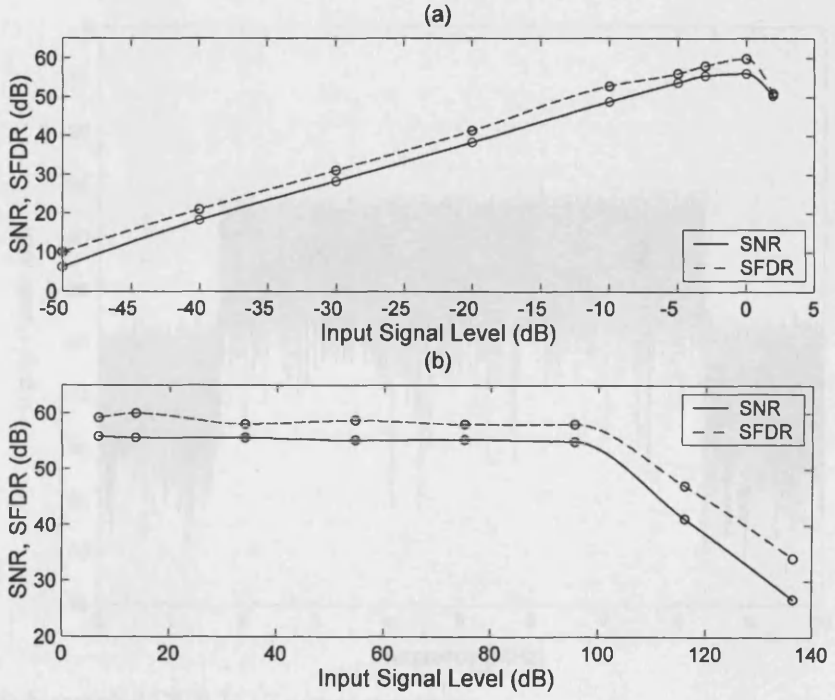

Fig. 4.23 (a) SNR and SFDR versus input amplitude and (b) versus input frequency.

DNL and INL results are plotted in Figs 4.24(a) and 4.24(b), respectively. The 3.4 LSB |INL| value is attributed partly to internal DAC resistor matching errors and partly to poor comparator preamplifier common-mode rejection as a result of the use of the resistive loading preamplifier, which reduced measured ADC SFDR to about 60 dB from the simulated value of 65 dB.

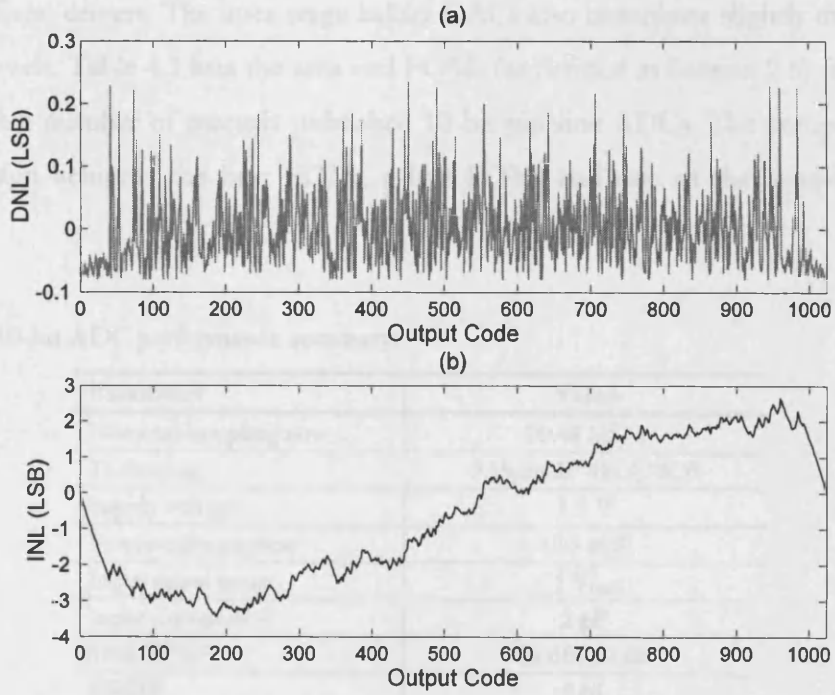

Fig. 4.24 (a) ADC DNL plot. (b) ADC INL plot.

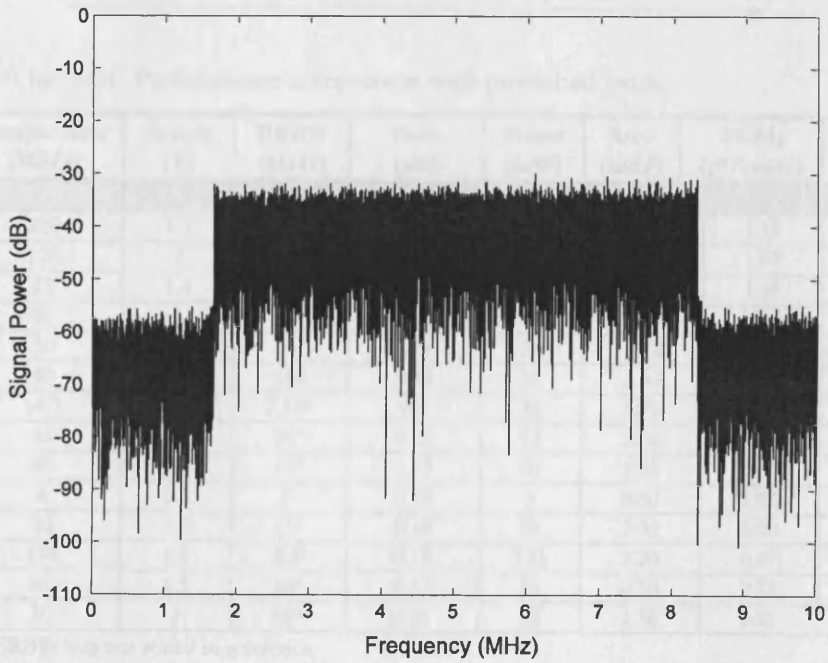

Fig. 4.25 Sub-sampled DVB-H IF power spectrum.

A DVB-H test generator was then used to generate a 6.66 MHz-bandwidth time-sliced 4K-mode rate ½ data-stream at an IF of 35.96 MHz. The 35.96 MHz signal was then applied directly to the ADC inputs. Fig. 4.25 is the down-converted 6.66 MHz DVB-H power spectrum.

Table 4.2 is a summary of the ADC performance. The difference in measured ADC consumption and the results of the architectural partitioning model is primarily due to digital I/O pad buffers/drivers. The inter-stage ladder DACs also contribute slightly to the elevated dissipation levels. Table 4.3 lists the area and FOMs (as defined in Section 2.5) for this design together with a number of recently published 10-bit pipeline ADCs. The comparison shows that this design achieves the best FOM_1, a low FOM_2 and one of the lowest silicon area values.

Table 4.2 10-bit ADC performance summary.

Parameter	Value
Nominal sampling rate	20.48 MS/s
Technology	0.35μm 2P 4M CMOS
Supply voltage	1.5 V
Power consumption	19.5 mW
Input signal range	1 V_{ppd}
Input capacitance	2 pF
SNR/SFDR	56 dB/60 dB
ENOB	9.01
INL	-3.4 LSB/2.7 LSB
DNL	-0.1 LSB/0.3 LSB
Core size	1.3 mm^2

Table 4.3 10-bit ADC Performance comparison with published work.

Reference	Sample Rate (MS/s)	Supply (V)	ERBW (MHz)	Tech. (μm)	Power (mW)	Area (mm^2)	FOM_1 (pJ/conv.)	FOM_2 (pJ·V/conv.)
This work	**20.48**	**1.5**	**100**	**0.35**	**19.5**	**1.30**	**0.19**	**2.77**
[89]	220	1.2	110*	0.13	135	0.50	1.19	1.43
[90]	120	2	60*	0.3	75	30	1.07	2.14
[91]	25	1.4	16	0.35	21	2.24	1.43	2.56
[92]	80	3	99	0.18	69	1.85	0.54	4.02
[93]	30	2	15*	0.3	16	3.12	1.30	2.60
[113]	40	3	100	0.35	55	2.60	0.38	5.66
[115]	14.3	1.5	7.15*	0.6	36	5.75	3.66	5.49
[124]	40	2.5	20*	0.25	12	0.70	0.32	0.79
[125]	20	2.5	10*	0.25	20	1.25	1.77	4.42
[126]	4	1.5	2*	0.18	3	0.60	1.03	1.54
[127]	50	1.5	25*	0.18	29	1.30	1.00	1.50
[128]	150	1.8	400	0.18	123	2.20	0.47	4.54
[129]	80	1.5	40*	0.13	33	0.30	0.71	1.07
[130]	30	3	60*	0.25	60	1.36	0.91	10.97

* $f_s/2$ used since ERBW was not stated in reference

4.6 Conclusions

An architectural partitioning optimization analysis of the classical pipeline ADC has been carried out for high-bandwidth and low-power mobile video applications. It is found that 2.5-bit inter-stage resolution is optimal for 10-bit pipeline ADC resolutions irrespective of sampling rate. The design of a 1.5-V, 20.48 MS/s, 10-bit pipeline ADC for sub-sampling a DVB-H tuner IF output was then done to validate the architectural optimization findings. Experimental results have been presented with the converter achieving 100 MHz ERBW and the best energy efficiency reported for a CMOS 10-bit video-rate pipeline ADC. The optimization analysis presented here allows a quick turnaround time in the design of power-optimized pipeline ADCs.

5 Delta-Sigma ADC Design for Mobile GSM & WCDMA Receivers

"It is more blessed to give than to receive" Acts 20:35 KJV

As the boundary between the digital and analogue subsystems of mobile communication receivers shift closer and closer to the antenna (with the ultimate software-defined radio [131] being a flexible software-configurable DSP subsystem preceded by a high-speed, extremely high dynamic range ADC with an antenna at its input), the high dynamic range required in the baseband or IF ADCs becomes more challenging to achieve, especially at elevated sample rates. Dimensioning the receiver chain in such a way as to take optimal advantage of both the analogue and digital domains [132] is the short term strategy before the ultimate software radio nirvana is physically reached. Since these receivers are used in battery-powered devices and require high SNRs, ΔΣ ADCs have been increasingly used in cellular receivers [133]-[137] since their SNR/mW ratio is one of the highest amongst all available ADC topologies and analogue domain device mismatch can usually be shaped out of band.

One issue however prevalent in switched-capacitor ΔΣ ADC design is the linearity of the input sampling switch. In continuous-time ΔΣ ADC designs, the sampling switch is within the forward path of the ΔΣ modulator loop and thus its nonlinearity does not affect the overall performance of the ADC. This is not the case with its switched-capacitor sibling as the switch is outside of the loop and thus defines overall fidelity within the wanted band from a tonal point of view. This problem is further exacerbated in older and relatively inexpensive standard CMOS process technologies where all devices have moderate threshold voltages and exotic low threshold voltage devices are unavailable.

To address this issue, a novel switch linearization circuit is proposed in this chapter and the dynamic range improvement achieved as a result of the circuit validated with the design of two high-dynamic range switched-capacitor ΔΣ ADCs for both GSM and WCDMA cellular reception standards. An overview of the two radio standards is initially carried out with ADC dynamic range requirements considered. Subsequently, a terse description of ΔΣ modulation fundamentals is done (detailed in Appendix A) with the linearity issues plaguing discrete-time switched-capacitor designs highlighted. The novel switch linearization scheme

is then described. Detailed circuit design and experimental results for both the GSM and WCDMA ADCs are presented and conclusions suitably drawn at the end of the chapter.

5.1 GSM System Overview

[‡]In the early parts of the 1980s, analog cellular telephone systems were experiencing rapid growth in Europe, particularly in Scandinavia and the United Kingdom, but also in France and Germany with each country's system proprietary and incompatible with each other; an undesirable situation from an equipment manufacturing and product marketing point of view. This prompted the Conference of European Posts and Telegraphs (CEPT) in 1982 to form a study group called the Groupe Spécial Mobile (GSM) to study and develop a pan-European public land mobile system to meet the following criteria:

- Good subjective speech quality
- Low-cost terminal and service
- International roaming capability
- Handheld terminals support
- Ease of upgrade for new services and facilities
- Spectral efficiency
- ISDN compatibility

In 1989, GSM responsibility was transferred to the European Telecommunication Standards Institute (ETSI), and phase I of the GSM specifications were published in 1990. Commercial service began in 1991 with 36 GSM networks already live in 22 countries by 1993. Although standardized in Europe, GSM is not only a European standard. Over 200 GSM networks (including DCS1800 and PCS1900 in America) are operational in more than 110 countries around the world. In the beginning of 1994, there were 1.3 million subscribers worldwide, which had grown to almost 2 billion by 2006 and the GSM acronym now aptly standing for Global System for Mobile communications.

5.1.1 GSM Radio Link Considerations

Table 5.1 is the current allocation of frequency spectrum for both uplink and downlink GSM transmission [139]:

‡ Materials used to write this overview were obtained from www.gsmworld.com [9] and John Scourias' public domain term paper [138]

Table 5.1 GSM uplink and downlink frequency spectrum allocation.

Parameter	GSM850	E-GSM900	DCS1800	PCS1900
Mobile Transmit	824 MHz	880 MHz	1710 MHz	1850 MHz
Base Receive	849 MHz	915 MHz	1785 MHz	1910 MHz
Base Transmit	869 MHz	925 MHz	1805 MHz	1930 MHz
Mobile Receive	894 MHz	960 MHz	1880 MHz	1990 MHz

5.1.1.1 Multiple Access and Channel Structure

Since radio spectrum is a limited resource shared by all users, a method must be devised to divide up the bandwidth among as many users as possible. The method chosen by GSM is a combination of Time- and Frequency-Division Multiple Access (TDMA/FDMA). The FDMA part involves the division by frequency of the (maximum) 25 MHz bandwidth into 124 carrier frequencies spaced 200 kHz apart. One or more carrier frequencies are assigned to each base station. Each of these carrier frequencies is then divided in time, using a TDMA scheme. The fundamental unit of time in this TDMA scheme is called a *burst period* which lasts 15/26 ms (or approx. 0.577 ms) with 156.25 bits transmitted in 0.577 ms duration, giving a gross bit rate of 270.833 kbps.

5.1.1.2 Channel Coding and Modulation

Because of natural and man-made electromagnetic interference, the encoded speech or data signal transmitted over the radio interface must be protected from errors. GSM uses convolutional encoding and block interleaving to achieve this protection. The exact algorithms used differ for speech and for different data rates.

To further protect against the burst errors common to the radio interface, each sample is interleaved. The 456 bits output by the convolutional encoder are divided into 8 blocks of 57 bits, and these blocks are transmitted in eight consecutive time-slot bursts. Since each time-slot burst can carry two 57 bit blocks, each burst carries traffic from two different speech samples.

This digital signal is then modulated onto the analog carrier frequency using Gaussian-filtered Minimum Shift Keying (GMSK). GMSK was selected over other modulation schemes as a compromise between spectral efficiency, complexity of the transmitter, and limited spurious emissions. The complexity of the transmitter is related to power consumption, which should be minimized for the mobile station. The spurious radio emissions, outside of the allotted bandwidth, must be strictly controlled so as to limit

adjacent channel interference, and allow for the co-existence of GSM and other radio standards.

5.1.2 GSM Enhancements

Two main enhancements to GSM, General Packet Radio Service (GPRS) and Enhanced Data-rate for GSM Evolution (EDGE) were respectively introduced in 2000 and 2003 [9]. Both are described below.

5.1.2.1 GPRS

GPRS was a step towards third generation mobile networks by adding packet data feature to the GSM network, allowing both Packet Switched (PS) and Circuit Switched (CS) traffic to exist in the GSM infrastructure theoretically increasing data throughput to about 170 kbps from GSM network's 9.6 kbps and 14.4 kbps. The end user also enjoyed some cost savings in addition to the enhanced experience because packet switching reduced dialup charges for periodic update applications like internet email. GPRS also supported the Internet Protocol (IP), bursty traffic and unbalanced traffic flow with pioneer GPRS networks launched in 2000 supporting over 50 kbps data rates.

5.1.2.2 EDGE

EDGE provided up to three times the data capacity of GPRS with the use of the 8-PSK modulation scheme (GPRS uses GMSK). Using EDGE, operators can handle three times more subscribers than GPRS; triple their data rate per subscriber, or add extra capacity to their voice communications. EDGE uses the same TDMA frame structure, logic channel and 200 kHz carrier bandwidth as existing GSM networks, allowing seamless integration of EDGE (by simple software-upgrade).

EDGE allows the delivery of advanced mobile services such as the downloading of video and music clips, full multimedia messaging, high-speed colour Internet access and e-mail on the move. The relatively inexpensive upgrade of existing GPRS networks to EDGE meant that as at April 2006, there were 139 commercial GSM/EDGE networks in 78 countries, out of a total of 192 EDGE deployments in 102 countries [140].

5.2 WCDMA System Overview

[§]In older analogue frequency division multiple access (FDMA) systems, the user occupies one frequency channel for transmit and one for receive for the duration of a phone

[§] This overview was excerpted from WCDMA/UMTS Wireless Networks Technical Brief, www.tektronikx.com [141].

call. These transmit and receive channels are busy until a call has been completed. During peak hours or festive periods like the annual New Year Eve celebrations in the City of London, many subscribers are unable to access the system which results in lost revenue for a network operator, and increased frustration for a user.

TDMA systems improved on this capacity issue by further subdividing a given bandwidth into time slots. In this way, multiple users can use the same duplex pair simultaneously. CDMA and WCDMA systems use a much broader bandwidth than either FDMA or TDMA systems. Instead of dividing users up by frequency or time, they are divided into codes, specific data streams assigned to particular users. All users transmit at the same time and multiple users share the same frequency carrier. Each mobile user is uniquely identified by a specialized code and frequency.

5.2.1 Frequency Reuse

Traditional FDMA or TDMA cellular systems have a frequency reuse method where frequencies are only duplicated within a certain pattern. This reduces the likelihood of interference between two neighboring cell sites that are both using the same channel. CDMA and WCDMA take a much different approach in that the same frequency is used at every site (Fig. 5.1). In the case of CDMA, forward links are separated from each other not by frequencies, but by Pseudo Noise (PN) offsets. In the case of WCDMA, forward links are separated from each other by Scrambling Codes.

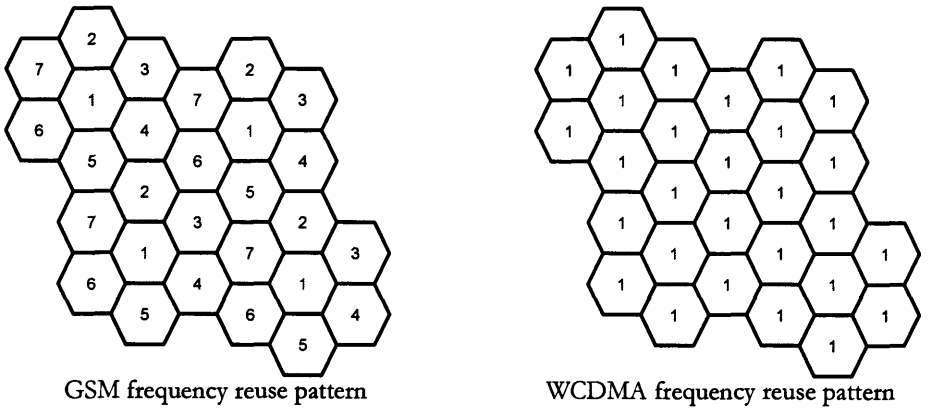

Fig. 5.1 GSM and WCDMA frequency reuse pattern.

5.2.2 Signal Coding and Spreading

Unlike TDMA signals, WCDMA signals use all available bandwidth for each RF channel. Code channel separation is accomplished by digitally coding individual channels and not by frequency separation. A particular subscriber's receiver looks for the unique code

assigned to it and the rest of the channels are indistinguishable from noise. Each channel is uniquely identified by the carrier frequency and the code. WCDMA specifications allow 3.84 MHz for a signal bandwidth. For example, digitized voice or actual data at a rate of 12.2 kbps is "spread" using a code which is running at 3.84 Mbps code rate. The resulting spread bits are called chips and the transmitted spread rate is expressed as 3.84 Mcps for WCDMA. This is comparable to a bandwidth of 1.92 MHz. The subscriber mobile receiver will see this spread signal together with noise, interference, and messages on other code channels in the same RF frequency slot. The interference can come from other users in the same cell and interference from neighboring cells. The receiver's demodulator/correlator then reapplies the code and recovers the original data signal.

5.2.2.1 Coding

Two binary sequences of equal length are defined as being orthogonal if the result of passing them through an exclusive-OR operation, results in an equal number of 1's and 0's. When data streams are first exclusive-ORed with orthogonal codes and then merged, they can later be separated.

5.2.2.2 Spreading

Orthogonal codes can be used to "spread" a user data sequence, such as digitized voice or actual data. For example, each binary "1" will become "0110" and each binary "0" the inverse, "1001" if exclusive-ORed with the orthogonal code "1001". Orthogonal codes used in WCDMA vary in length from 4 to 512 bits. The 1s and 0s of the resultant data stream from the exclusive-OR process are called "chips". WCDMA systems have a fixed chip rate of 3.84 Mcps (mega chips per second). The code length is called the spreading factor (SF). Longer codes provide a more robust system but at lower individual user channel data rate.

5.2.3 RF Downlink and Uplink

The RF signal transmitted from the base station to the subscriber mobile phone is referred to as the downlink or forward link. The RF signal transmitted from the mobile phone is referred to as the uplink or reverse channel. The transmitted RF signal from the base station is a complex QAM (Quadrature Amplitude Modulated) type of signal. An example of a root-raised-cosine (RRC) filtered I/Q QPSK (Quadrature Phase Shift Keying) constellation display is shown in Fig. 5.2. It can thus be seen that the symbols represented by the modulated RF signal need to be demodulated and decoded within discrete decision

points in the constellation in order to be error free. Table 5.2 is the current Bands I to IX allocation of frequency spectrum for both uplink and downlink WCDMA transmission [142]:

Table 5.2 WCDMA uplink and downlink frequency spectrum allocation.

Bands	Uplink (Mobile to Base station)		Downlink (Base station to Mobile	
I	1920 MHz	1980 MHz	2110 MHz	2170 MHz
II	1850 MHz	1910 MHz	1930 MHz	1990 MHz
III	1710 MHz	1785 MHz	1805 MHz	1880 MHz
IV	1710 MHz	1755 MHz	2110 MHz	2155 MHz
V	824 MHz	849 MHz	869 MHz	894 MHz
VI	830 MHz	840 MHz	875 MHz	885 MHz
VII	2500 MHz	2570 MHz	2620 MHz	2690 MHz
VIII	880 MHz	915 MHz	925 MHz	960 MHz
IX	1749.9 MHz	1784.9 MHz	1844.9 MHz	1879.9 MHz

Increasing degradation of received RF signal, due to impairments such as interference or noise, will spread the points out until errors begin to occur (Fig. 5.3). Base station transmitter modulation inaccuracy or RF path distortion may cause the points to spread. Error Vector Magnitude (EVM) is a measurement which evaluates the signal quality and is computed from the vector difference between the actual received signal and a calculated, ideal reference signal (Fig. 5.4). The WCDMA standards specify EVM tolerances [142].

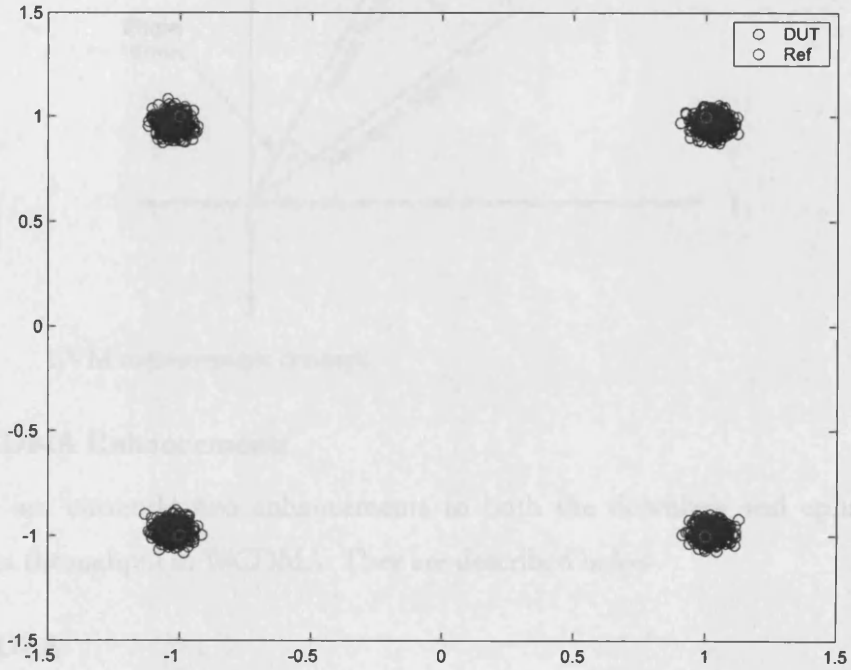

Fig. 5.2 QPSK constellation display.

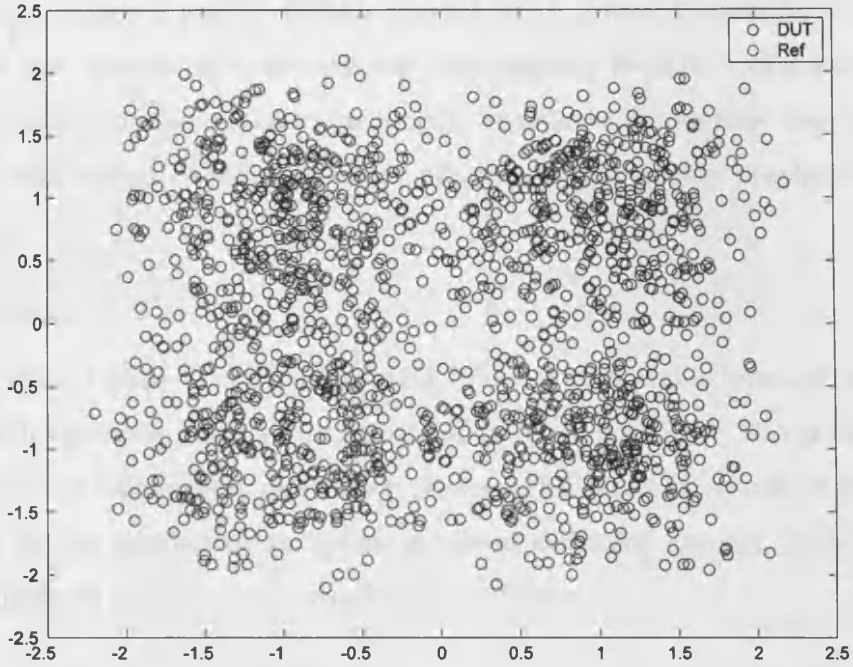

Fig. 5.3 QPSK constellation display with severe channel impairment.

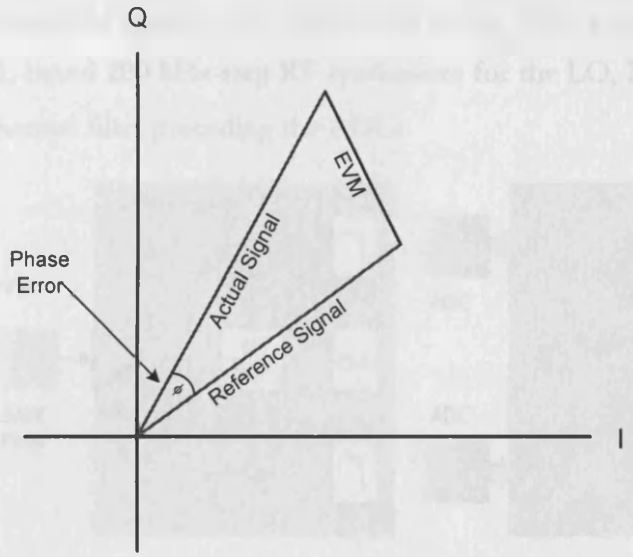

Fig. 5.4 EVM measurement concept.

5.2.4 WCDMA Enhancements

There are currently two enhancements to both the downlink and uplink paths for elevated data throughput in WCDMA. They are described below.

5.2.4.1 HSDPA

High Speed Downlink Packet Access (HSDPA) provides a smooth evolutionary path for WCDMA networks allowing for a theoretical data capacity of up to 14.4 Mbit/s in the downlink (currently 3.6 Mbit/s with HSDPA Category 6 and 7.2 Mbit/s with HSDPA Category 8) and was designed to increase the available WCDMA data rate by a factor of 5 or

more. HSDPA defines a new W-CDMA channel, the high-speed downlink shared channel (HS-DSCH) that operates in a different way from existing W-CDMA channels, but is only used for downlink communication to the mobile. To achieve this elevated data rate, adaptive modulation and coding (AMC) is used in addition to fast packet re-scheduling and re-transmission.

5.2.4.2 HSUPA

High-Speed Uplink Packet Access (HSUPA) is a data access protocol for WCDMA networks with extremely high upload speeds of up to 5.76 Mbit/s. This is made possible without the use of higher order modulation schemes (for the conservation of mobile phone battery life) by the creation of an uplink enhanced dedicated channel (E-DCH) and link adaptation methods similar to those employed by HSDPA.

5.3 GSM ADC Dynamic Range

Fig. 5.5 is a simplified diagram of a direct-conversion GSM receiver with a low noise amplifier (LNA), PLL-based 200 kHz-step RF synthesizer for the LO, I/Q mixers, baseband gain amplifier and channel filter preceding the ADCs.

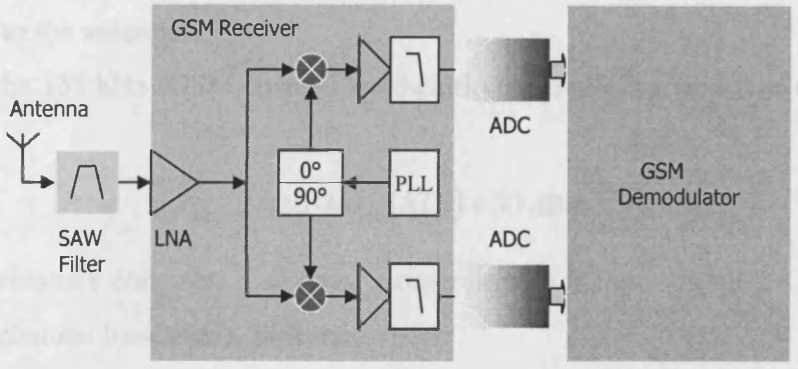

Fig. 5.5 Simplified block diagram of a direct conversion GSM receiver subsystem.

In any digital cellular receiver, the specified bit error rate, BER (0.1% for GSM [139]) must be achieved for minimum and maximum receiver input sensitivities in the present of in-band blockers, out-of-band blockers, in-band noise and co-channel/adjacent channel interference. The 0.1% BER is equivalent to a Carrier-to-Noise Ratio (C/N) of 9 dB at the input of the digital GSM demodulator [143]. Fig. 5.6 is the blocking profile for E-GSM [143].

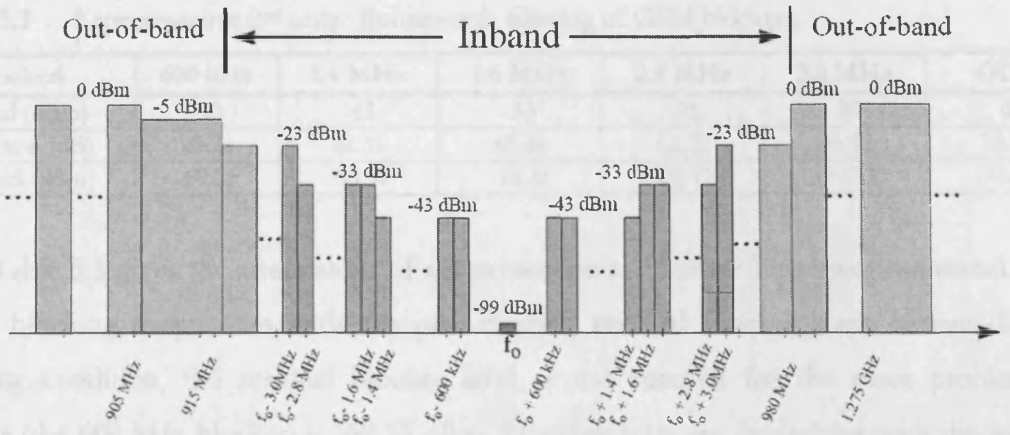

Fig. 5.6 E-GSM blocking profile [143].

It can thus be seen that the with the out-of-band blockers at 0 dBm and the desired signal at -99 dBm, the dynamic range required to demodulate the wanted signal at C/N of 9 dB is in excess of 108 dB, clearly impossible from a circuit design perspective, especially for the LNA and mixer dynamic range. To mitigate this, external surface acoustic wave (SAW) filters are typically used to reduce the levels of the out-of-band (OOB) blockers to more manageable levels. The following analysis attempts to determine the required ADC dynamic range for GSM from a noise and linearity perspective under relaxed channel filtering with all signals referred to the antenna.

Firstly, the 135 kHz (GSM channel bandwidth) thermal noise power at the antenna is given by:

$$P_{\text{thermal}} = 10 \cdot \log_{10}(kTB) + 30 \text{ dBm} \tag{5.1}$$

where k is Boltzmann's constant, T ambient temperature in Kelvin (300 K or 27° assumed) and B 135 kHz channel bandwidth. This then yields:

$$P_{\text{thermal}} = 10 \cdot \log_{10}\left(1.38 \times 10^{-23} \times 300 \times 135 \times 10^{3}\right) + 30 \text{ dBm} = -122.53 \text{ dBm} \tag{5.2}$$

Minimum sensitivity at the antenna [138] is -104 dBm. With C/N of 9 dB, the receiver is allowed to add some noise to the wanted signal corresponding to its maximum allowable Noise Figure (NF) and given by:

$$NF(\text{dB})_{\max} = -104 - 9 - (-122.53) = 9.53 \text{ dB} \tag{5.3}$$

Typically, the ADC quantization noise floor is made 20 dB lower than the system noise floor to reduce the ADC effect on system noise to less than 0.1 dB. Thus, dynamic range with only the smallest wanted signal considered is:

$$DR_{\text{signal}} = -104 - (-122.53) + 20 = 38.53 \text{ dB} \tag{5.4}$$

Table 5.3 Representative 2nd order Butterworth filtering of GSM blockers.

Blockers	600 kHz	1.4 MHz	1.6 MHz	2.8 MHz	3.0 MHz	OOB
Actual (dBm)	-43	-43	-33	-33	-23	0
Rejection (dB)	26.23	42.51	45.46	62.72	66.32	70.54
Filtered (dBm)	-69.23	-85.51	-78.46	-95.72	-89.32	-70.54

Table 5.3 gives the attenuation of a representative 2nd order Butterworth channel filter at the blocking frequencies with the post-filtering residual blocker levels shown. Under blocking condition, the residual blocker level at the antenna for the most problematic blocker (the 600 kHz blocker) is -69.23 dBm. Blocking tests are carried out with the wanted signal at -99 dBm (Fig. 5.10), 5 dB higher than -104 dBm minimum sensitivity, yielding the residual portion of the required ADC dynamic range:

$$DR_{\text{blocker}} = -69.23 - (-99) + 5 = 34.77 \text{ dB} \tag{5.5}$$

An additional 6 dB must be added to (5.5) to account for the blocker peak level. Also, the peak-to-average ratio of the modulation scheme (about 3.5 dB for EDGE) must be included as well. This brings the blocker related dynamic range to:

$$DR_{\text{blocker\_peak}} = 34.77 + 6 + 3.5 = 44.27 \text{ dB} \tag{5.6}$$

Since the maximum wanted signal power is -15 dBm [138], about 50 dB of coarse automatic gain control (AGC) range will be required in the receiver chain (fine AGC will be done in the digital domain). Finally, combining (5.4) and (5.6) gives the total required ADC dynamic range.

$$DR_{\text{ADC}} = DR_{\text{signal}} + DR_{\text{blocker\_peak}} = 38.53 + 44.27 = 82.8 \text{ dB} \tag{5.7}$$

It can thus be seen that an ADC with DR of 83 dB will meet the GSM requirements under relaxed analogue filtering. This allows imprecise un-trimmed channel filters to be used with additional filtering done more precisely in the digital domain, simultaneously with the removal of the $\Delta\Sigma$ ADC out-of-band quantization noise and requiring no extra digital hardware. Fig. 5.7 summarizes the above considerations.

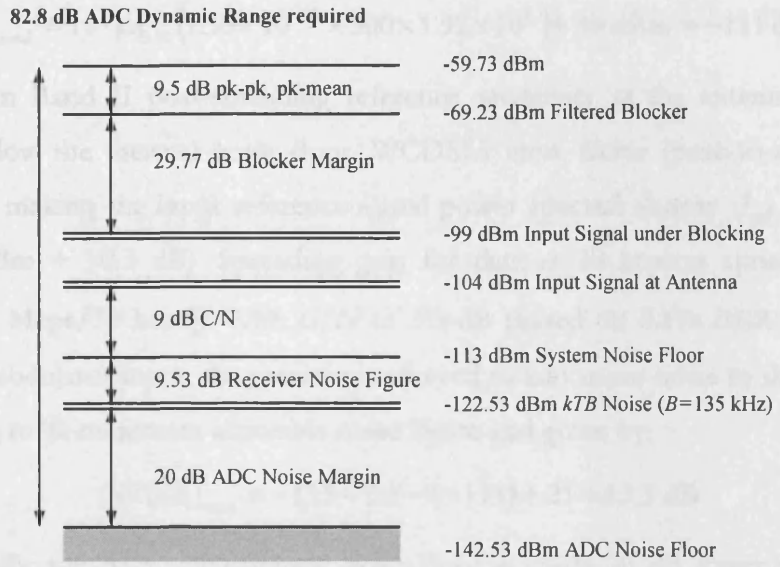

Fig. 5.7 GSM ADC dynamic range specification.

It is also pertinent that the ADC linearity be adequate enough (SFDR (dB) ≥ 3 dB + SNR (dB)) as any intermodulation distortion present will simply elevate the system noise floor.

5.4 WCDMA ADC Dynamic Range

Similar consideration as was carried out for GSM in Section 5.3 will be done for WCDMA in this section. Fig. 5.8 is a simplified WCDMA receiver diagram.

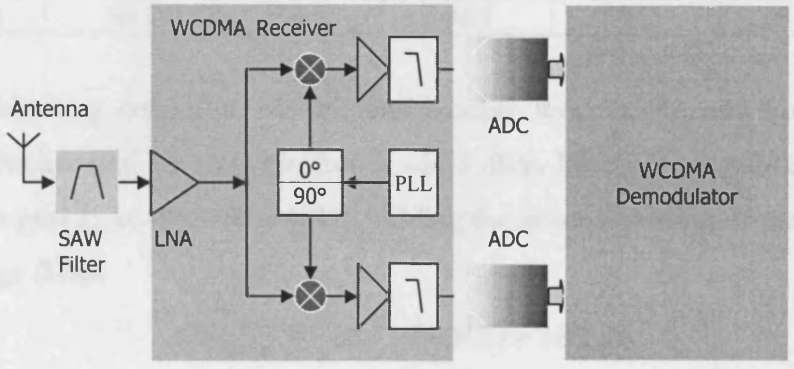

Fig. 5.8 Simplified diagram of a direct conversion WCDMA receiver subsystem.

The spread-spectrum nature of WCDMA means that the actual spectrum is noise like and buried within thermal noise. Firstly, using (5.1), the 1.92 MHz (WCDMA channel bandwidth) thermal noise power at the antenna is given by:

$$P_{\text{thermal}} = 10 \cdot \log_{10}\left(1.38 \times 10^{-23} \times 300 \times 1.92 \times 10^{6}\right) + 30 \text{ dBm} = -111 \text{ dBm} \quad (5.8)$$

Minimum Band II post-spreading reference sensitivity at the antenna [142] is -115 dBm, 4dB below the thermal noise floor. WCDMA crest factor (peak-to-average ratio) is 10.3 dB [142] making the input reference signal power spectral density ($\hat{I}_{or}$) equal to -104.7 dBm (-115 dBm + 10.3 dB). Spreading gain for data at 30 kcps is approximately 21dB ($10 \cdot \log_{10}$ [3.84 Mcps/30 kcps]). With C/N of 3.5 dB (based on 0.1% BER requirement) at the digital demodulator input, the receiver is allowed to add some noise to the wanted signal corresponding to its maximum allowable noise figure and given by:

$$NF(\text{dB})_{\max} = -115 - 3.5 - (-111) + 21 = 13.5 \text{ dB} \quad (5.9)$$

Typically, the ADC quantization noise floor is made 20 dB lower than the system noise floor to reduce the ADC effect on system noise to less than 0.1 dB. Thus, dynamic range with only the smallest wanted reference sensitivity signal considered is (Fig. 5.9):

$$DR_{\text{signal}} = -94.7 - (-111) - 13.5 + 20 = 22.8 \text{ dB} \quad (5.10)$$

Table 5.4 gives the attenuation of a representative 2nd order Chebyshev channel filter at the blocking frequencies with the post-filtering residual blocker levels shown.

Table 5.4 Representative 2nd order Chebyshev filtering of WCDMA Blockers.

Blockers	2.7 MHz	3.5 MHz	5.9 MHz	10 MHz	15 MHz	OOB
Actual (dBm)	-57	-44	-44	-56	-44	-15
Rejection (dB)	8.1	12.5	22.4	34.5	49.9	54
Filtered (dBm)	-65.1	-56.5	-66.4	-90.5	-93.9	-69

Under blocking condition, the residual blocker level at the antenna for the most problematic blocker (the 3.5 MHz blocker) is –56.5 dBm. Blocking tests are carried out with the reference signal $\hat{I}_{or}$ at –94.7 dBm [141], yielding the residual portion of the required ADC Dynamic Range (DR):

$$DR_{\text{blocker}} = -56.5 - (-94.7) = 38.2 \text{ dB} \quad (5.11)$$

An additional 6 dB must be added to (5.5) to account for the blocker peak level. The peak-to-average ratio of the modulation scheme (10.3 dB) has already been included in (5.10). This brings the blocker related dynamic range to:

$$DR_{\text{blocker\_peak}} = 38.2 + 6 = 44.2 \text{ dB} \quad (5.12)$$

Since the maximum wanted $\hat{I}_{or}$ signal power is -25 dBm [141], about 30 dB of coarse automatic gain control (AGC) range will be required in the receiver chain (fine AGC will be

done in the digital domain). Finally, combining (5.10) and (5.12) gives the total required ADC dynamic range.

$$DR_{ADC} = DR_{signal} + DR_{blocker\_peak} = 22.8 + 44.2 = 67 \text{ dB} \tag{5.13}$$

It can thus be seen that an ADC with DR of 67 dB will meet the WCDMA requirements under relaxed analogue filtering. This allows imprecise un-trimmed channel filters to be used with additional filtering done more precisely in the digital domain simultaneously with the removal of the ΔΣ ADC out-of-band quantization noise and requiring no extra digital hardware. Fig. 5.9 summarizes the above considerations.

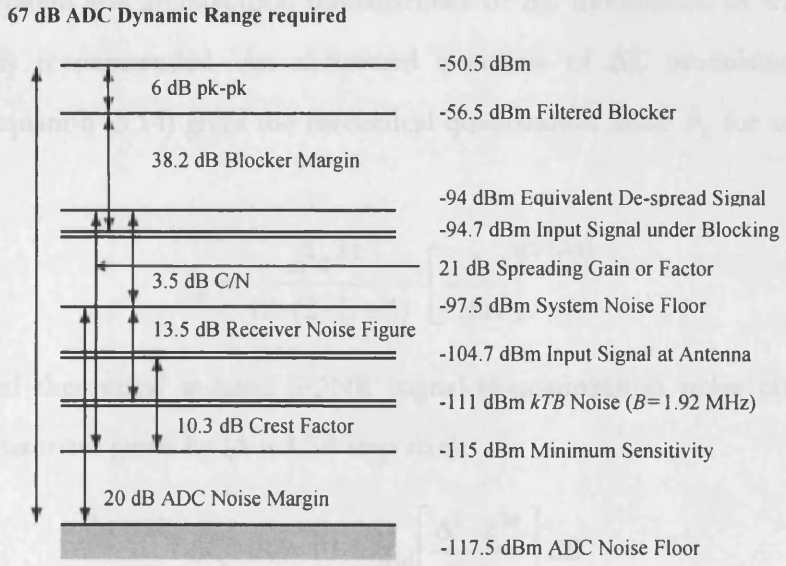

Fig. 5.9 WCDMA ADC dynamic range specification.

It is also important that the ADC linearity be adequate enough (SFDR (dB) ≥ 3 dB + SNR (dB)) as any intermodulation distortion present will simply elevate the system noise floor.

5.5 ΔΣ Modulation

Over-sampling converters utilize a modulator in the analogue domain for discretization of the input signal and digital filtering to remove out-of-band quantization noise and decimate the data-stream to Nyquist. Originally, delta modulation scheme was proposed by De Jaeger in 1952 [144] for the analogue modulator by inserting an integrator in the modulator's feedback path. Unfortunately, the non-idealities of the integrator limited the overall modulator linearity and accuracy. Also, a differentiated version of the analogue input was available at the digital output which may or may not be desirable.

Inose et al later removed the integrator from the feedback path and placed it in the feed-forward path in 1963 [145]-[146], thus inventing the delta-sigma (ΔΣ) modulation scheme. This widely accepted and now ubiquitous scheme was significantly more robust to the accuracy issues that plagued its older sibling and could pass the input signal to the digital domain unchanged. The ΔΣ modulator is an over-sampled ADC. It can be made to operate in continuous-time (s-domain) or in discrete-time (z-domain), the latter using switched-capacitor schemes [147]. Switched-current schemes [148] has also been used but failed to catch on commercially due to speed, component mismatch and yield issues. An overview of ΔΣ ADCs for wireless transceivers is carried out in [149]. There are numerous literature and books on the system and architectural fundamentals of ΔΣ modulation of which [122] and [155] are highly recommended. An abstracted overview of ΔΣ modulation is given in Appendix A. Equation (5.14) gives the theoretical quantization noise P_E for any L-order ΔΣ modulator:

$$P_E = \frac{\Delta^2 \pi^{2 \cdot L}}{12 \cdot (2 \cdot L + 1)} \cdot \left[\frac{1}{\mathrm{OSR}} \right]^{(2 \cdot L + 1)} \tag{5.14}$$

with the desired theoretical in-band SQNR (signal-to-quantization noise ratio) obtainable using an n-bit quantizer given by (Δ is LSB step size):

$$\mathrm{SQNR} = 10 \cdot \log_{10} \left[\frac{\Delta^2 \cdot 2^{2n}}{8 \cdot P_E} \right] \mathrm{dB} \tag{5.15}$$

5.6 Sampling Switch Linearity Issues in Discrete-time ΔΣ Modulators

The parasitic insensitive integrator, one of the various integrator topologies used in a switched-capacitor ΔΣ modulator is illustrated in Fig. 5.10.

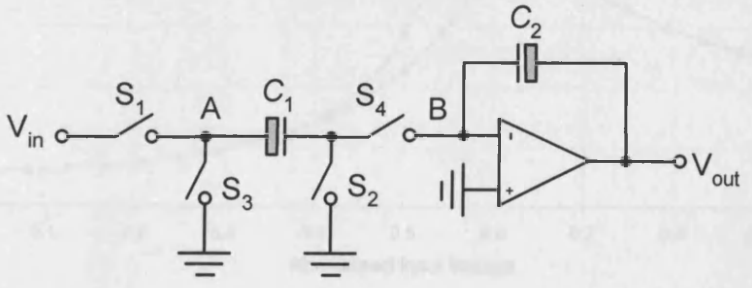

Fig. 5.10 Parasitic-insensitive integrator topology.

The time-varying input signal is periodically sampled onto sampling capacitor C_1 by switch S_1 external to the ΔΣ modulator loop and accumulated onto the integrating capacitor, C_2. As such, the sampling switch impairments do not enjoy any noise shaping as will the switches within the loop. For this reason, any switch non-linearity will get modulated onto the sampled input waveform thereby creating undesirable in-band harmonics and compromising the ΔΣ modulator's SFDR. As mentioned in the introductory section of this chapter, this switch linearity problem is a real issue in older and relatively inexpensive standard CMOS process technologies where all devices have moderate threshold voltages and exotic low threshold voltage are unavailable.

Typically, this switch is a *p*MOS or *n*MOS device or a transmission gate with the latter preferred as a result of its higher dynamic range and the fact that charge injection can be reduced by dimensioning the complementary devices equally (this is further expatiated below). A thorough analysis of MOS sampling switches and prevalent issues when used in switched-capacitor design is given in [189] with Gray et al [84] and Haigh et al [190] originally carrying out pioneering work in developing the well known non-overlapping four-phase clocking scheme for the reduction of sampling switch signal-dependent charge-injection in switched-capacitor circuit design. Fig. 5.11 is a plot of the on-resistance of *p*MOS, *n*MOS and CMOS switches versus input voltage (normalized to 2.7 V supply voltage) for equally dimensioned devices in a 0.35 μm technology (W = 32 μm, L = 0.4 μm, V_{Tn} = 0.58 V, V_{Tp} = -0.65 V).

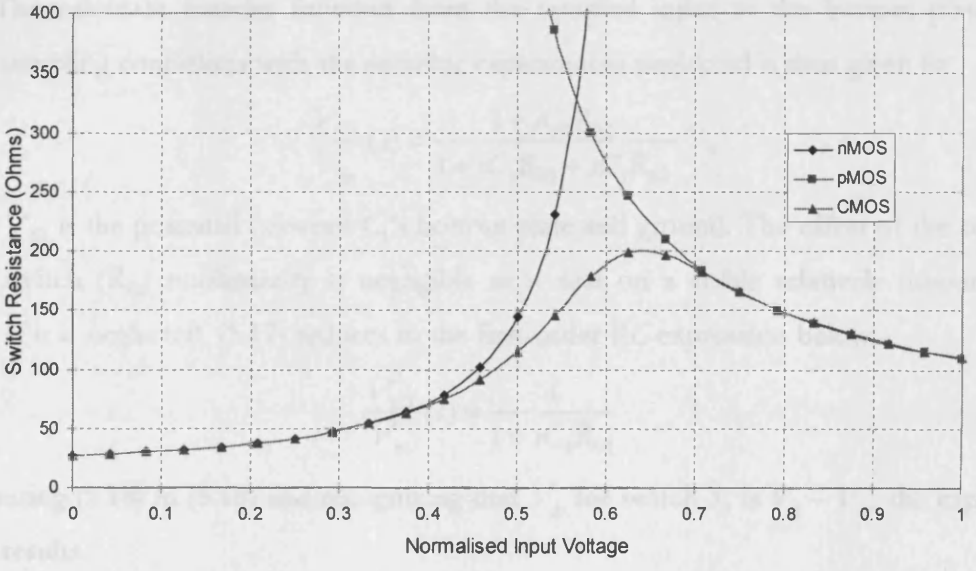

Fig. 5.11 CMOS, *n*MOS and *p*MOS sampling switch resistance versus input.

The following expression gives the CMOS switch on-resistance R_{switch} to the first-order.

$$R_{switch} \cong \frac{1}{K_n \frac{W}{L}\left(V_{gsn} - V_{Tn}\right) + K_p \frac{W}{L}\left(V_{sgp} - \left|V_{Tp}\right|\right)} \tag{5.16}$$

But even to a first order approximation (5.16), the on-resistance of the transmission gate is non-linear with respect to its input voltage when in an on-state. The gate-to-channel capacitances are also non-linear and input-dependent contributing even further to the sampling distortion but can be minimized or even eliminated by connecting the device's bulk terminal to the source terminal (this is only possible for the *n*MOS device if a twin-tub process technology is available) and by using the parasitic-insensitive topology with non-overlapping four-clock phases [84], [190], which also minimizes the effect of the gate-to-source/drain parasitic capacitances. Fig. 5.12 depicts the non-linear sampling switch (R_{S1}) in sampling mode.

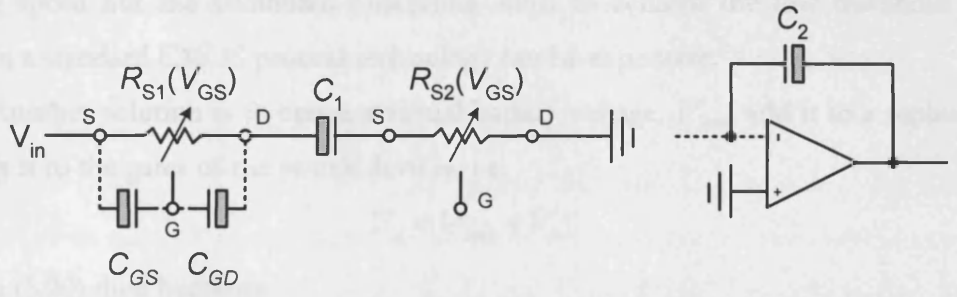

Fig. 5.12 Non-linear sampling switch representative diagram.

The s-domain transfer function from the sampled input to the bottom plate of C_1 under sampling conditions with the parasitic capacitances neglected is thus given by

$$\frac{V_{C1}}{V_{in}}(s) = \frac{1 + sC_1R_{S2}}{1 + sC_1R_{S1} + sC_1R_{S2}} \tag{5.17}$$

where V_{C1} is the potential between C_1's bottom plate and ground. The effect of the common mode switch (R_{S2}) nonlinearity is negligible as it acts on a stable relatively time-invariant signal. If it is neglected, (5.17) reduces to the first-order RC expression below:

$$\frac{V_{C1}}{V_{in}}(s) = \frac{1}{1 + sC_1R_{S1}} \tag{5.18}$$

Substituting (5.16) in (5.18) and recognizing that V_{gs} for switch S_1 is $V_g - V_{in}$, the expression below results.

$$\frac{V_{C1}}{V_{\text{in}}}(s)=\frac{K_n\frac{W}{L}(V_{gn}-V_{Tn}-V_{\text{in}})+K_P\frac{W}{L}(V_{\text{in}}-V_{gp}-|V_{Tp}|)}{K_n\frac{W}{L}(V_{gn}-V_{Tn}-V_{\text{in}})+K_p\frac{W}{L}(V_{\text{in}}-V_{gp}-|V_{Tp}|)+sC_1} \tag{5.19}$$

Rearranging (5.19) gives a quadratic expression in V_{in} the solution of which will yield the higher-order harmonics of V_{in}, the by-product of switch resistance nonlinearity:

$$V_{C1}(s)=\frac{K_n\frac{W}{L}(V_{gn}-V_{Tn}-V_{\text{in}})\cdot V_{\text{in}}+K_p\frac{W}{L}(V_{\text{in}}-V_{gp}-|V_{Tp}|)\cdot V_{\text{in}}}{K_n\frac{W}{L}(V_{gn}-V_{Tn}-V_{\text{in}})+K_p\frac{W}{L}(V_{\text{in}}-V_{gp}-|V_{Tp}|)+sC_1}. \tag{5.20}$$

Various methods have been employed in the literature to address this issue with the simplest being the arbitrary increase of the aspect ratio of the device until the on-resistance error term with varying input is small enough to be negligible [170]. This is however unsuitable for high-speed design. Fujimori et al [180] used minimum-length lower threshold voltage devices as switches in order to reduce non-linear on-resistance and still achieve good sampling speed but the additional processing steps to achieve the low threshold voltage devices in a standard CMOS process technology can be expensive.

Another solution is to create a virtual battery voltage, V_{batt}, add it to a replica of V_{in} and apply it to the gates of the switch devices, i.e.

$$V_g=V_{\text{batt}}+V_{\text{in}} \tag{5.21}$$

Equation (5.20) then becomes

$$V_{C1}(s)=\frac{K_n\frac{W}{L}(V_{\text{batt}}-V_{Tn})\cdot V_{\text{in}}+K_p\frac{W}{L}(-V_{\text{batt}}-|V_{Tp}|)\cdot V_{\text{in}}}{K_n\frac{W}{L}(V_{\text{batt}}-V_{Tn})+K_p\frac{W}{L}(-V_{\text{batt}}-|V_{Tp}|)+sC_1} \tag{5.22}$$

a linear expression in V_{in}. If a pre-charged capacitor C_{batt} is used as the virtual battery it becomes the well-known bootstrapping scheme which has also been employed for switch linearization in the literature [169], [185] - [188] with the input signal superimposed on the control voltages of an *n*MOS switch gate to hold the gate-to-source voltage constant and thus achieve constant on-resistance to a first-order approximation over the entire input range. A replica sampling switch network was used in [192] to achieve over 105 dB SFDR in a 1.1 MHz bandwidth. Fig. 5.13 illustrates the bootstrapping circuit [193] for *n*MOS sampling switch.

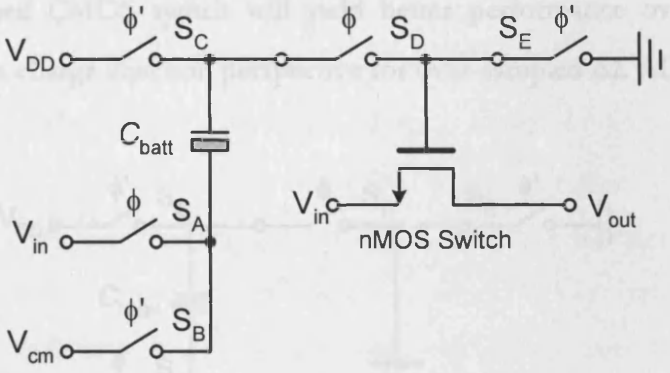

Fig. 5.13 Bootstrap circuit using *n*MOS sampling switches.

The operation is explained as follows. When clock ϕ is low, switches S_B, S_C and S_E are closed. The input common mode voltage, V_{cm} is thus applied to the bottom plate of C_{batt}. The supply voltage, V_{DD} is applied to C_{batt}'s top plate and the gate of the *n*MOS switch is held low by S_E turning it off. When ϕ goes high, S_B, S_C and S_E are opened and S_A and S_D closed. The difference between V_{in} and V_{cm} is thus applied to C_{batt}'s bottom plate and its top plate connected to the gate of the *n*MOS switch. The switch's gate voltage is thus

$$V_{gn} = V_{DD} + V_{in} \tag{5.23}$$

where $V_{batt} = V_{DD} + V_{in} - (V_{in} + V_{cm})$. V_{gsn} is thus fixed at $V_{DD} - V_{cm}$ for most input voltages (within the limits of reasonable and finite on-resistance of switches S_A and S_D) and the switch is guaranteed linear. Typically, S_A, S_B and S_E are *n*MOS devices and the rest *p*MOS devices. All switches are sized an order of magnitude smaller than the dimensions of the main linearised *n*MOS switch to minimize the depletion of C_{batt}'s charge by switch parasitics. The dimensions of C_{batt} must be determined such that it is an order of magnitude higher than the dominant parasitic, namely that of the linearised switch.

In order to further enhance the switch linearity and increase available dynamic range, this work extends the *n*MOS bootstrapping concept by replacing the *n*MOS device with a transmission gate as shown in Fig. 5.14. The justification for this is given below.

Firstly, using the parasitic insensitive topology (Fig. 5.12) and respectively turning off of switches S_2 and S_4 just slightly before S_1 and S_3 [84], [190] during the transition from sample-mode to hold-mode addresses the issue of signal-dependent charge injection (to a first order) from switch channel capacitance, gate-to-drain overlap capacitance, junction capacitance and sampling capacitor bottom-plate parasitics point of view.

Secondly, the use of fully-differential paths also minimizes even-order nonlinearities as a result of the above. CMOS or *n*MOS switch linearization in addition alleviates the effect of signal-dependent switch on-resistance on ADC sampling non-linearity and it is shown below

that the bootstrapped CMOS switch will yield better performance over a bootstrapped *n*MOS switch from a charge injection perspective for over-sampled ΔΣ ADC application.

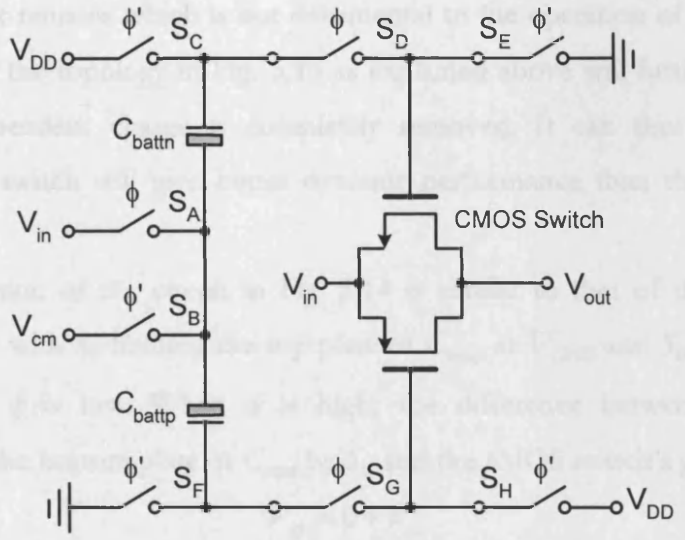

Fig. 5.14 Simplified CMOS sampling switch linear iser circuit.

Thirdly, consider the case of S_1 in Fig. 5.10 being an *n*MOS switch. It can be shown [189], [191] that if S_1 is turned off, charge will be injected onto node A diluting the originally sampled charge, with the potential at node A given by:

$$V_A \approx V_{\text{in}}\left(1+\frac{WLC_{\text{ox}}}{C_1}\right)-\frac{WLC_{\text{ox}}}{C_1}\left(V_{DD}-V_{Tn}\right) \tag{5.24}$$

Equation (5.24) contains a signal-dependent portion (gain error) and if body effect is neglected, a signal-independent portion (offset error). The dummy *n*MOS device method of cancellation is not very effective for this application because of the inequality of the split charge between the source and the drain of the *n*MOS sampling switch. Conversely, if a CMOS switch comprising equally dimensioned *n*MOS and *p*MOS devices is employed; overall switch on-resistance is slightly less than that of a single *n*MOS switch. In addition, the opposite charge packets injected by the complementary devices will tend to cancel each other (with slight error due to the inequality of *p*MOS and *n*MOS gate-drain overlap capacitances which is neglected here). Thus, the voltage at node A is now given by:

$$V_A = V_{\text{in}} + \frac{WLC_{\text{ox}}\left(V_{DD}-V_{\text{in}}-V_{Tn}\right)+WLC_{\text{ox}}\left(V_{\text{in}}-\left|V_{Tp}\right|\right)}{C_1} \tag{5.25}$$

yielding

$$V_A = V_{in} + \frac{WLC_{ox}}{C_1}(V_{DD} - |V_{Tp}| - V_{Tn}) \tag{5.26}$$

i.e. the signal-dependent portion of the injected charge is completely cancelled to a first order and only the offset remains which is not detrimental to the operation of the ΔΣ modulator. Finally, the use of the topology in Fig. 5.10 as explained above will further ensure that any residual signal-dependent charge is completely removed. It can thus be seen that the linearised CMOS switch will give better dynamic performance than the linearised *n*MOS switch.

The operation of the circuit in Fig. 5.14 is similar to that of the *n*MOS lineariser circuit in Fig. 5.13 with S_F holding the top plate of C_{battp} at V_{GND} and S_H turning the *p*MOS device off when ϕ is low. When ϕ is high, the difference between V_{in} and V_{cm} is superimposed on the bottom plate of C_{battp} by S_G and the *p*MOS switch's gate voltage is thus

$$V_{gs} = 0 + V_{in} \tag{5.27}$$

where $V_{batt} = V_{in} - (V_{in} - V_{cm})$. V_{gsp} is thus fixed at $-V_{cm}$ for most input voltages (within the limits of reasonable and finite on-resistance of switches S_A and S_G) and the *p*MOS switch is also guaranteed linear. In this way, the combination of the *p*MOS and *n*MOS switches enhances overall switch on-resistance linearity and dynamic range.

Fig. 5.15 is a plot of linearised *n*MOS, *p*MOS and CMOS switch resistance against normalized input voltage. Fig. 5.16 is a comparative plot of the Total Harmonic Distortion (THD) of the conventional CMOS switch and the linearised CMOS switch for 1 MHz input signal with > 20 dB improvement achieved in simulation over the conventional un-linearized CMOS switch for the desired input range switch using this circuit. The plots below were created whilst the CMOS switches were in their on-state. The *p*MOS device bulks were connected to the source to eliminate bulk modulation dependence. The *n*MOS device bulks were connected to V_{GND} to emulate a single-tub *n*-well CMOS process technology and make the circuit more generic (the actual process technology employed for the design was a twin-tub one). Fig. 5.17 is the initial transistor-level schematic of the CMOS lineariser circuit and Fig. 5.18 the simulated gate voltages of the linearised and conventional CMOS switches for comparison with the same parameters as used to obtain Fig. 5.11.

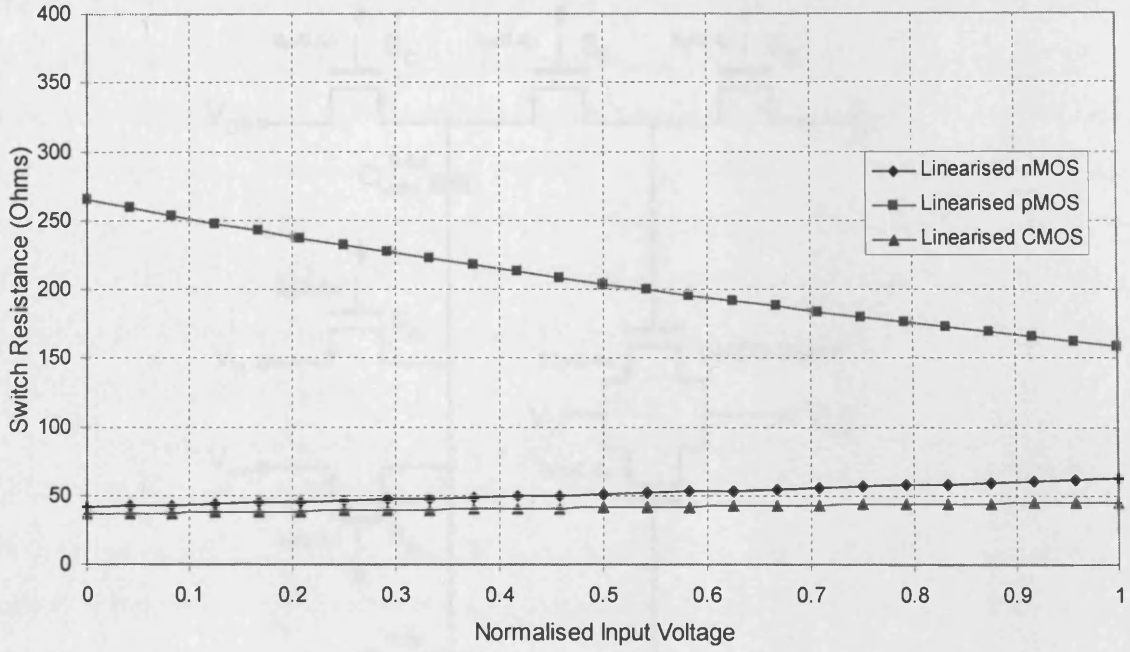

Fig. 5.15 Linearised CMOS, *n*MOS and *p*MOS sampling switch resistance versus input.

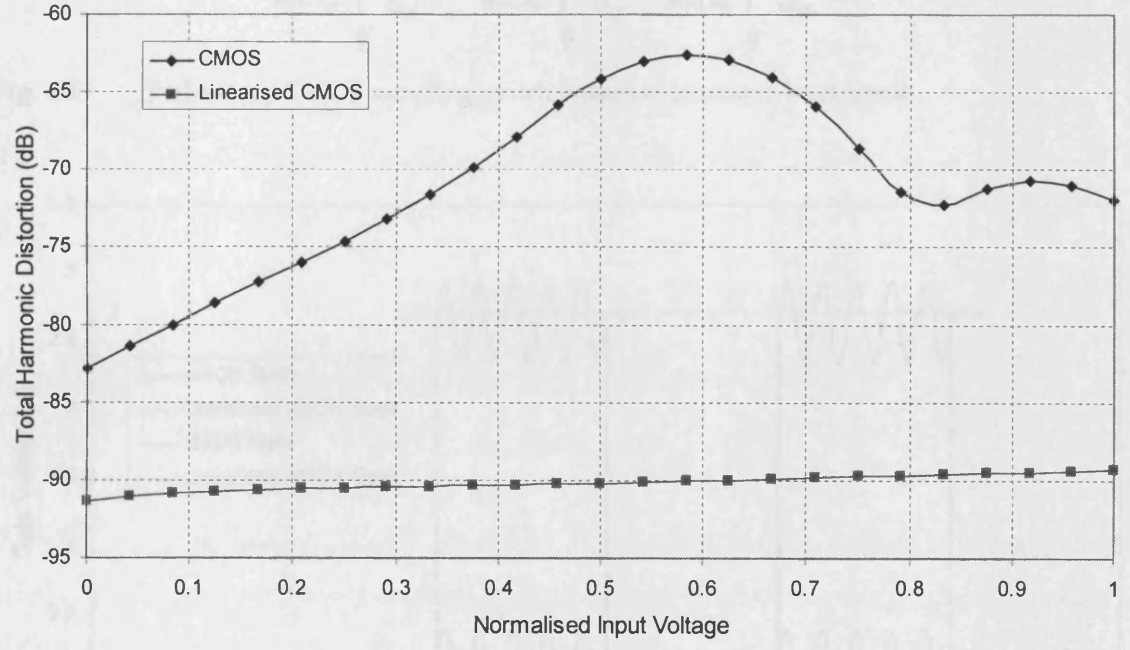

Fig. 5.16 Linearised CMOS and conventional CMOS THD plot versus input voltage.

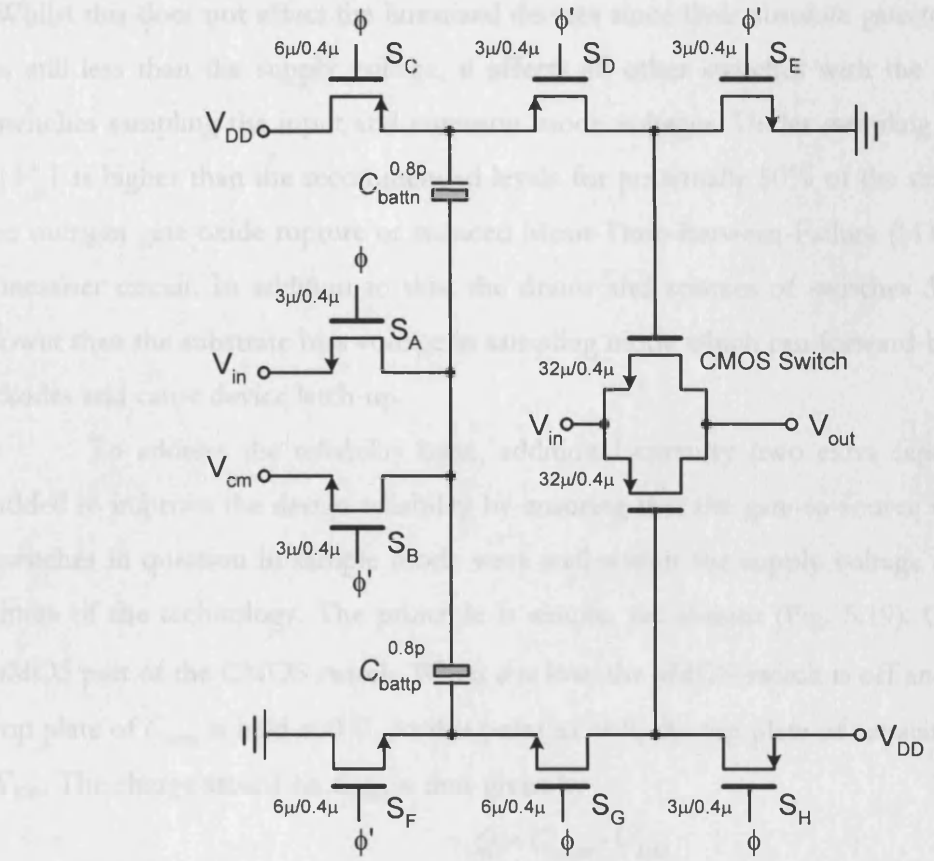

Fig. 5.17 Preliminary CMOS sampling switch linearisers transistor-level circuit.

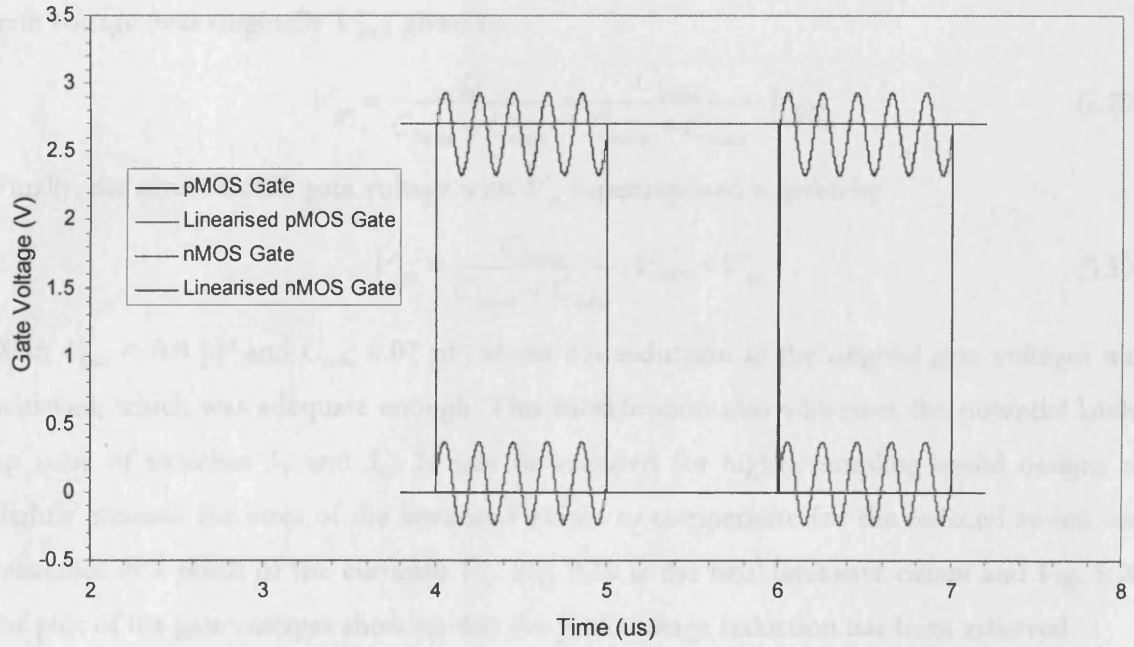

Fig. 5.18 Gate voltages of linearised and conventional CMOS switches.

It will be observed from Fig. 5.18 that the peak gate voltage of the linearised CMOS devices is higher than V_{DD} for the *n*MOS device and lower than V_{GND} for the *p*MOS device.

Whilst this does not affect the linearised devices since their absolute gate-to-source voltages is still less than the supply voltage, it affects all other switches with the exception of the switches sampling the input and common mode voltages. Under sampling conditions, their $|V_{gs}|$ is higher than the recommended levels for potentially 50% of the time. This can lead to outright gate oxide rupture or reduced Mean-Time-Between-Failure (MTBF) [194] of the linearisers circuit. In addition to this, the drains and sources of switches S_F and S_G will be lower than the substrate bias voltage in sampling mode which can forward-bias their junction diodes and cause device latch-up.

To address the reliability issue, additional circuitry (two extra capacitors) was then added to improve the design reliability by ensuring that the gate-to-source voltages of all the switches in question in sample mode were well within the supply voltage and the reliability limits of the technology. The principle is simple, yet elegant (Fig. 5.19). Consider only the *n*MOS part of the CMOS switch. When ϕ is low, the *n*MOS switch is off and its gate plus the top plate of C_{extra} is held at 0 V. At this point as well, the top plate of capacitor C_{battn} is held at V_{DD}. The charge stored on C_{battn} is thus given by

$$Q = C_{battn} \cdot V_{DD} \tag{5.28}$$

When ϕ is high, the bottom plate of both capacitors are dynamically driven by V_{in}. The static charge on C_{battn} is now shared between itself and C_{extra} with the new static nMOS gate voltage (was originally V_{DD}) given by

$$V_{gn} = \frac{Q}{C_{battn} + C_{extra}} = \frac{C_{battn}}{C_{battn} + C_{extra}} \cdot V_{DD} \tag{5.29}$$

Finally, the actual *n*MOS gate voltage with V_{in} superimposed is given by

$$V_{gn} = \frac{C_{battn}}{C_{battn} + C_{extra}} \cdot V_{DD} + V_{in} \tag{5.30}$$

With C_{batt} = 0.8 pF and C_{extra} 0.07 pF, about 8% reduction in the original gate voltages was achieved, which was adequate enough. This modification also addresses the potential latch-up issue of switches S_F and S_G. It may be required for higher-sampling speed designs to slightly increase the sizes of the linearised switch to compensate for the reduced switch on-resistance as a result of the curtailed V_{gs}. Fig. 5.19 is the final linearisers circuit and Fig. 5.20 the plot of the gate voltages showing that the peak voltage reduction has been achieved.

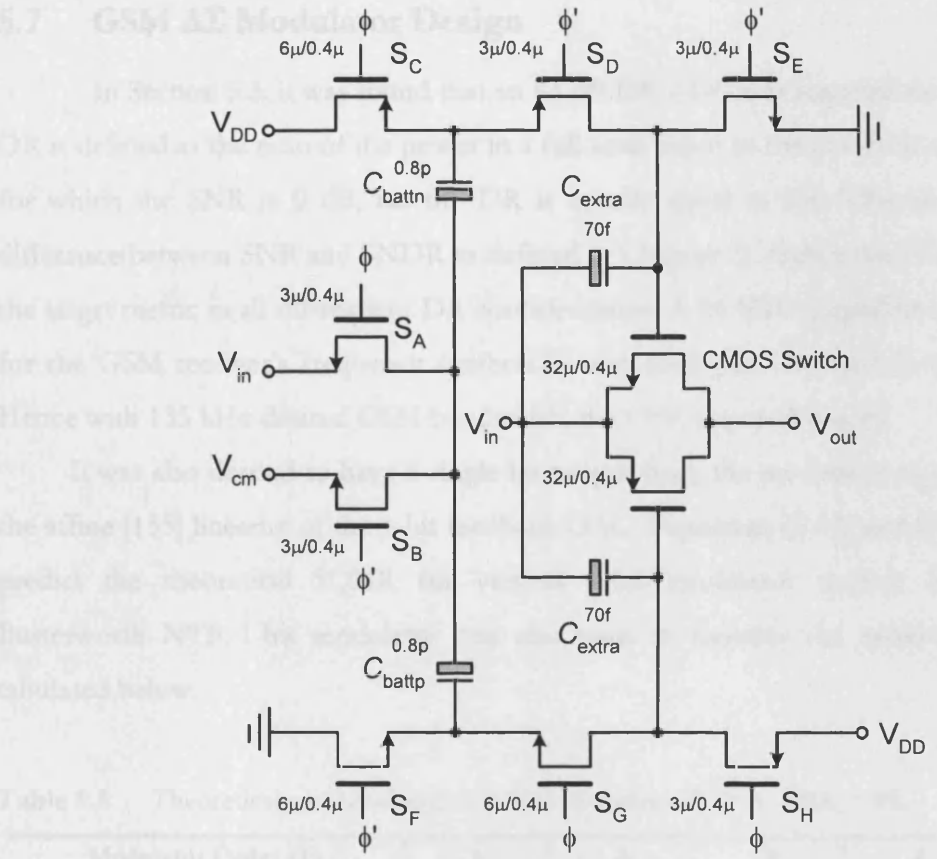

Fig. 5.19 Final CMOS sampling switch linearisers transistor-level circuit.

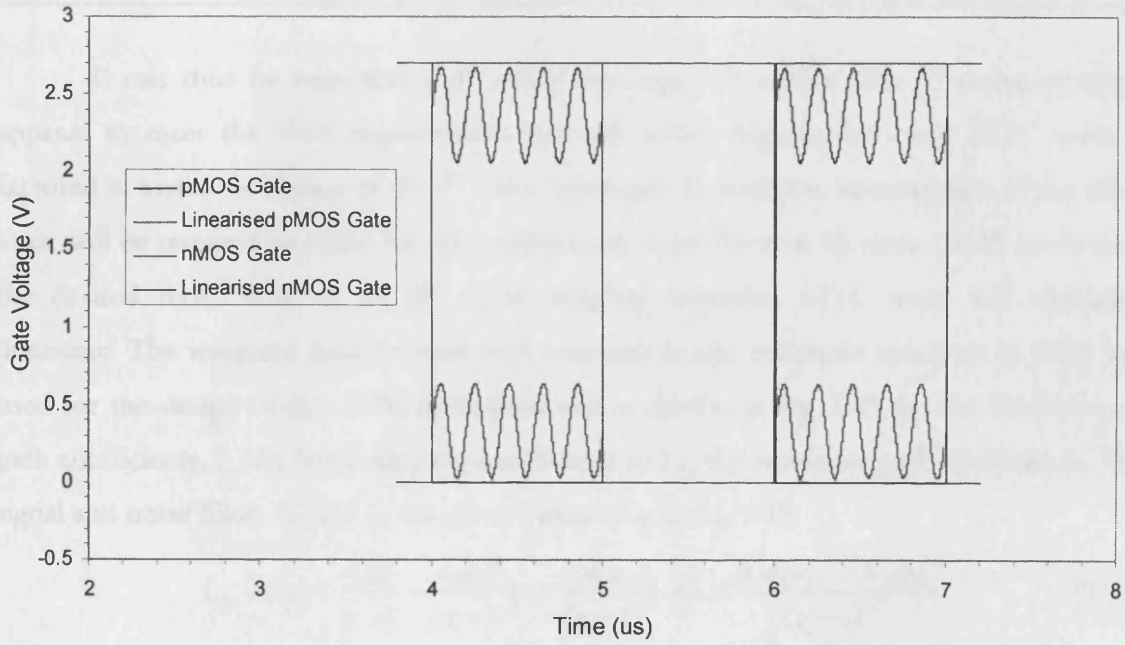

Fig. 5.20 Gate voltages of final linearised and conventional CMOS switches.

5.7 GSM ΔΣ Modulator Design

In Section 5.3, it was found that an 83 dB DR ADC was required for GSM. The term DR is defined as the ratio of the power in a full-scale input to the power of a sinusoidal input for which the SNR is 0 dB, i.e. the DR is exactly equal to the full-scale SNR (note the difference between SNR and SNDR as defined in Chapter 2). Hence the SNR will be used as the target metric in all subsequent DR considerations. A 26 MHz crystal was already available for the GSM receiver's frequency synthesizer and could also be used as the ADC's clock. Hence with 135 kHz desired GSM bandwidth, the OSR required was 96.

It was also desired to have a single-bit output from the modulator to take advantage of the affine [155] linearity of the 1-bit feedback DAC. Equations (5.14) and (5.15) were used to predict the theoretical SQNR for various 1-bit modulator orders. A model of the Butterworth NTF 1-bit modulator was also used to simulate the system and the results tabulated below.

Table 5.5 Theoretical and simulated GSM ΔΣ modulator SQNR (OSR = 96)

Modulator Order (*L*)	**1**	**2**	**3**	**4**	**5**
A. SQNR (dB) from (5.40)	62.08	94.00	125.16	155.96	186.53
B. Modulator model SQNR (dB)	56.36	76.11	89.38	96.57	100.81
Difference between **A** and **B** (dB)	5.72	17.89	35.78	59.39	85.72

It can thus be seen that a 4th order topology will suffice (the 3rd order topology appears to meet the SNR requirements but will suffer degradation once kT/C noise is factored in hence the choice of the 4th order topology). In addition, optimization of the zeros at dc will be required in order for the quantization noise floor to be about 20dB lower than the desired ADC SNR of 83 dB since sampling capacitor kT/C noise will ultimately dominate. The weighted feed-forward with summation and resonator structure in [122] was used for the design of the GSM modulator and is shown in Fig. 5.21 (a_x the feed-forward path coefficients, b_x the feedback path coefficients and c_x the resonator path coefficients. The signal and noise filters L_0 and L_1 are given below (for $c_1 = c_2 = 0$):

$$L_0 = L_1 = \frac{a_1 b_1}{z-1} + \frac{a_1 a_2 b_2}{(z-1)^2} + \frac{a_1 a_2 a_3 b_3}{(z-1)^3} + .. + \frac{a_1 a_2 a_3 \cdot .. \cdot a_N b_N}{(z-1)^N} \tag{5.31}$$

where N as used here is the order of the modulator topology. The Signal Transfer Function (STF) and NTF are thus given below:

$$NTF(z) = \frac{1}{1+L_1(z)} = \frac{(z-1)^N}{(z-1)^N + a_1 b_1 (z-1)^{N-1} + a_1 a_2 b_2 (z-1)^{N-2} + .. + a_1 a_2 a_3 \cdot .. \cdot a_n b_n} \tag{5.32}$$

$$\mathrm{STF}(z) = \frac{L_0(z)}{1 - L_1(z)} \approx 1 \tag{5.33}$$

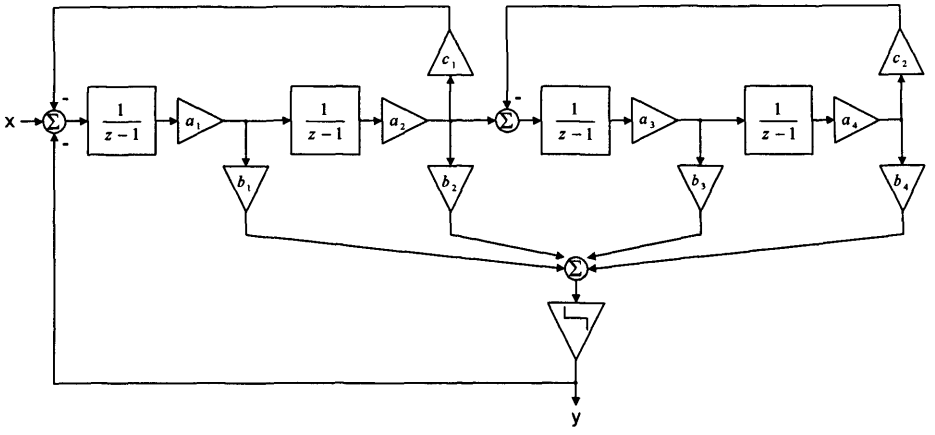

Fig. 5.21 GSM 4th order modulation architecture.

This topology is readily amenable to switched-capacitor implementation. Any change in c_x moves the conjugate zeros vertically away from z = 1+j0 and not along the unit circle leading to some instability. A minuscule shift from dc (z = 1+j0) will however approximate the unit circle trajectory and enable the realization of a passable but inexact Inverse Chebyshev NTF (exact Inverse Chebyshev NTFs cannot be realized using this structure as a result of the aforementioned stability issue and because of the difficulty of realizing delay-less switched-capacitor integrators). Peaking is also exhibited by the STF of this structure at higher frequencies and care must be taken in the design of the anti-alias filter to mitigate this.

Having chosen a suitable quantizer resolution, OSR and loop filter structure, the next step was to specify the NTF and derive from it, the loop filter transfer functions, L_0 and L_1 which incidentally is equivalent for this topology. The heuristic approach of Lee et al in [157] was followed to design an NTF with a peak out-of-band gain of 1.5 or slightly less for stability (1.3 was chosen). The discrete filter design toolkit in Matlab® was iteratively used to design a 4th order Butterworth high-pass filter with a gain of 1.3 resulting in a 3dB frequency of 829.27 kHz. The final transfer function given below.

$$NTF_{\text{Butterworth}}(z) = \frac{(1 - z^{-1})^4}{z^4 - 3.4767z^3 + 4.5628z^2 - 2.6765z + 0.5917} \tag{5.34}$$

Comparing the coefficients in (5.34) to (5.32) yields the loop filter coefficients tabled below (all b's set to 1 to prevent integrator overflow):

Table 5.6 Modulator loop filter coefficients for Butterworth NTF.

I	1	2	3	4
a_i	0.524	0.250	0.142	0.064
b_i	1	1	1	1
c_i	0	0	-	-

This was then quantized to the values in Table 5.7.

Table 5.7 Quantized modulator loop filter coefficients for Butterworth NTF.

I	1	2	3	4
a_i	1/2	1/4	1/8	1/16
b_i	1	1	1	1
c_i	0	0	-	-

Extensive simulations were then done in Matlab® to ascertain the stable input range of the modulator under dc and a 13 MHz square wave excitation. It was found that the modulator was stable for 75% of full-scale input amplitude at all in-band input frequencies with SQNR of about 96 dB as in Table 5.7 for the Butterworth NTF. Subsequently, c_1 was iteratively introduced in order to shift a pair of conjugate zeros away from dc to just close to the edge of the 135 kHz wanted band. With c_1 = 0.00625, the notches in the modulator spectral plot appeared at about 115.7 kHz and SQNR had improved to 106.5 dB, 3.5 dB more than the desired 103 dB and almost 10 dB higher than with the Butterworth NTF (c_2 was not used as it was too small for circuital realization). Fig. 5.22 is the modulator power spectrum from system simulation.

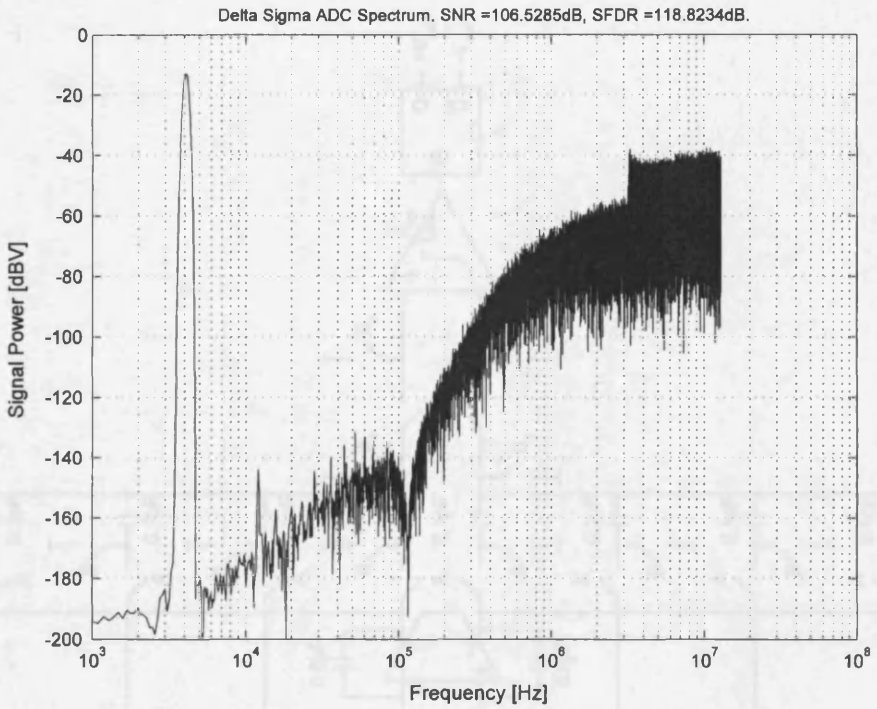

Fig. 5.22 GSM ΔΣ modulator power spectrum plot with the zero at 115.7 kHz.

The simplified schematic of the GSM ΔΣ modulator is shown in Fig. 5.23. A cross-coupled NAND-gate-based clock generator block was used to generate the desired non-overlapping 4-phase clocks [84], [190], with the timing relation of the various clocks shown in Fig. 5.24. Also, a fully-differential BiCMOS folded-cascode OTA with MOS inputs and silicon germanium bipolar cascode devices (Fig. 5.25) was used for the first integrator's OTA. The bipolar cascode device enabled the achievement of excellent bandwidth at high dc gain by pushing all non-dominant poles into the GHz region. The remaining three integrators used a CMOS folded-cascode OTA shown in Fig. 5.26.

Table 5.8 summarizes the OTA performance with the BiCMOS one consuming 1.44 mA current and the three CMOS ones each consuming 0.24 mA current. An integrated band-gap voltage source was used to generate a low temperature coefficient 20 μA current from which all OTA bias voltages were derived. The biasing circuit is shown in Fig. 5.27 with the dynamic comparator circuit shown in Fig. 5.28. Switched-capacitor CMFB network as used in Chapter 4 was used for regulating the bias voltage (V_{BIAS1}) of the lower nMOS current sources in the OTAs. The common mode voltage and 1-bit DAC negative and positive reference voltages (1.35 V, 0.85 V and 1.85 V respectively) were generated off-chip.

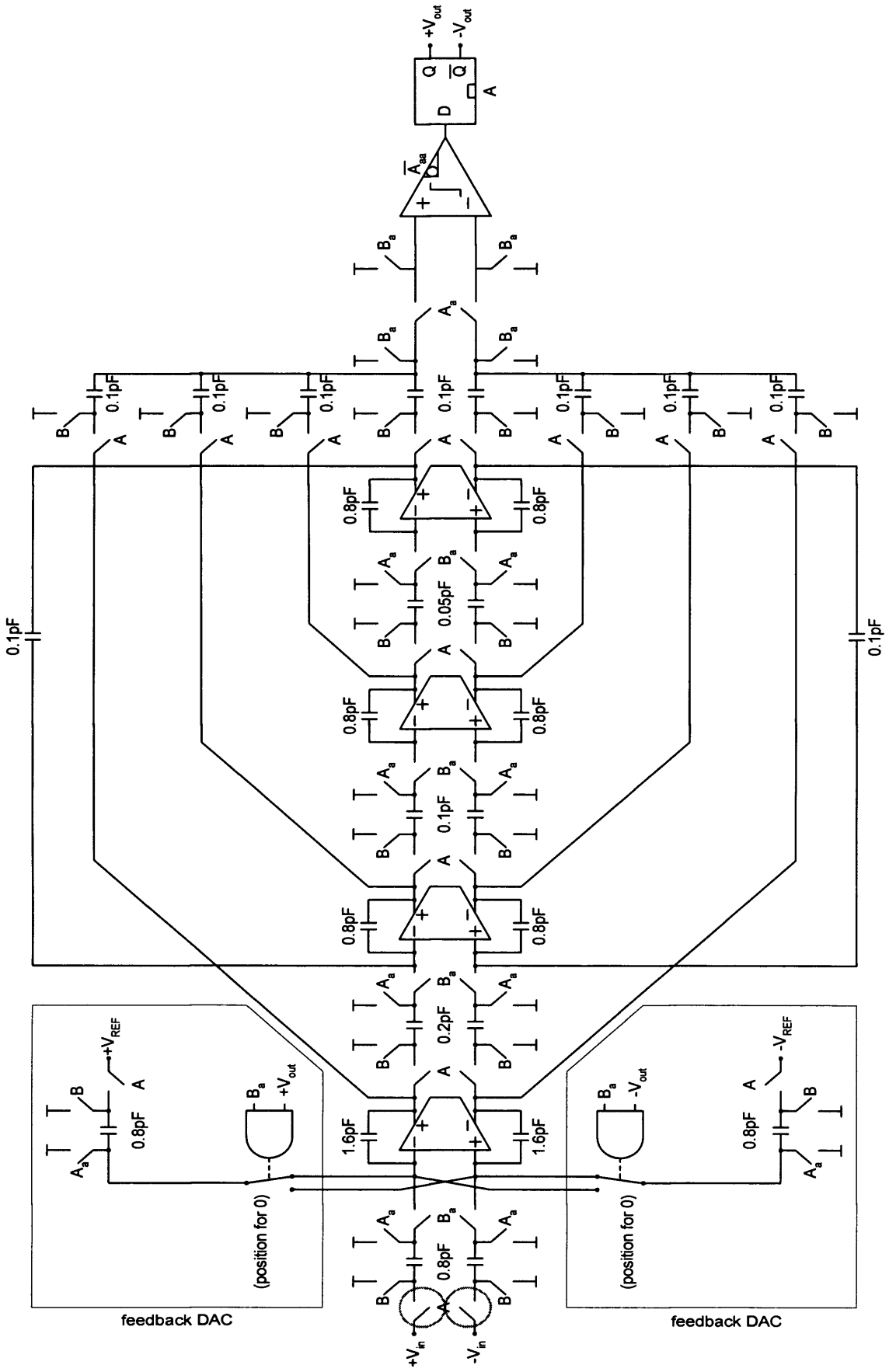

Fig. 5.23 Simplified GSM ΔΣ modulator schematic with linearised switches circled.

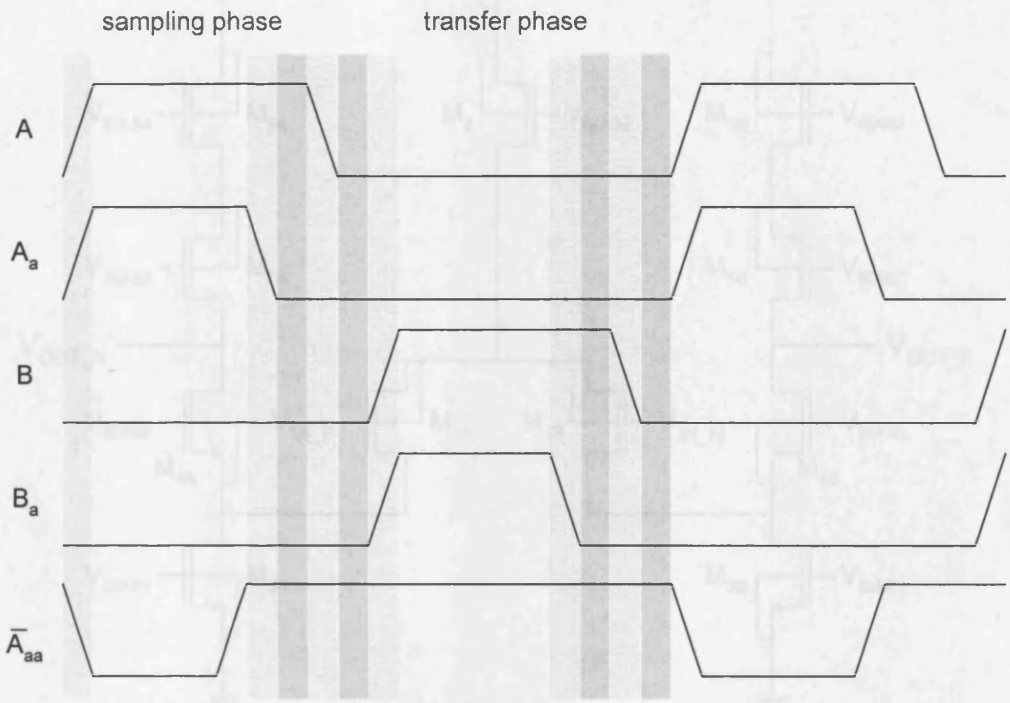

Fig. 5.24 Clock generator timing diagram with optimum 4-phase scheme [84], [190] used.

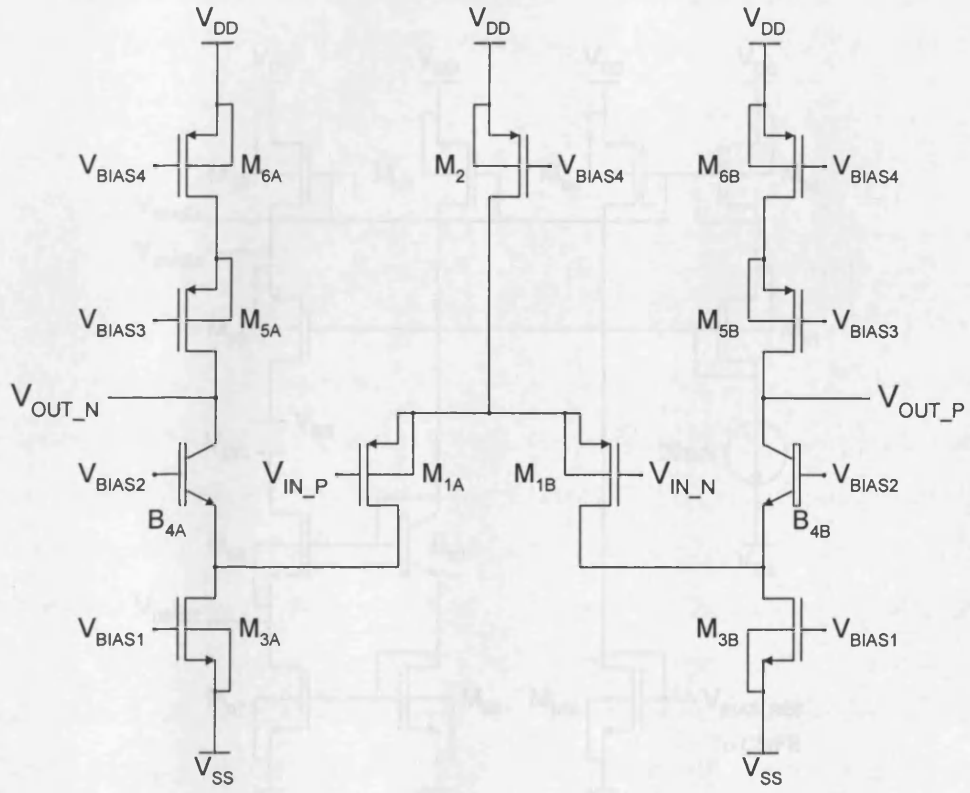

Fig. 5.25 BiCMOS folded cascode OTA for the GSM ΔΣ modulator's 1st integrator.

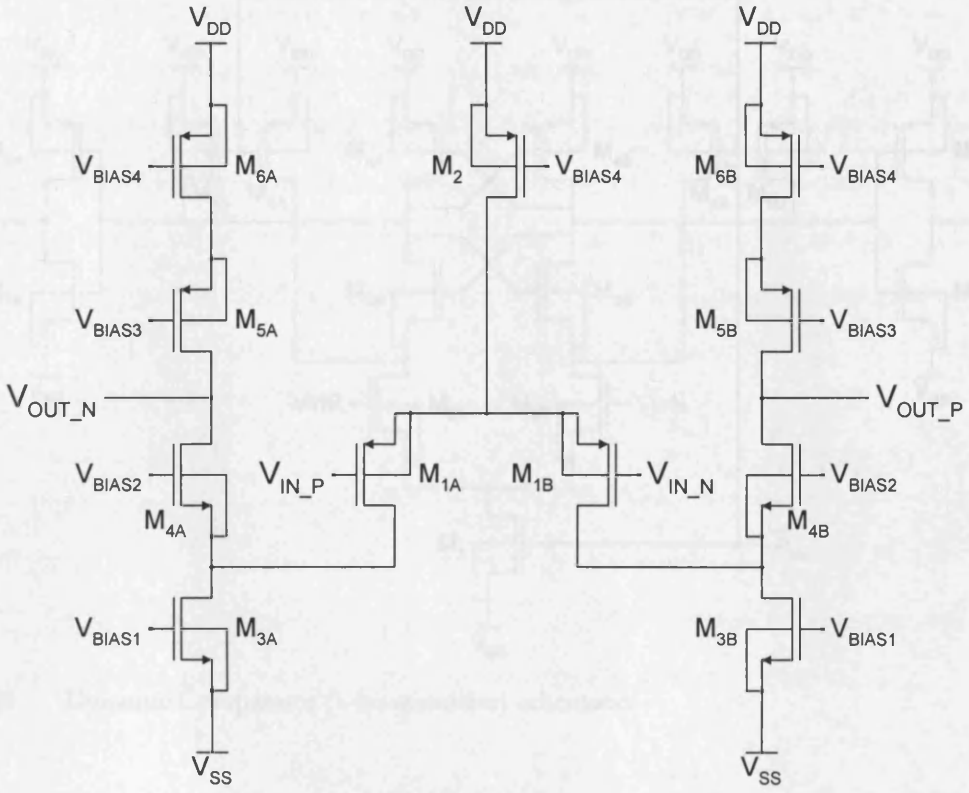

Fig. 5.26 CMOS folded cascode OTA for the GSM ΔΣ modulator's 2nd-4th integrator.

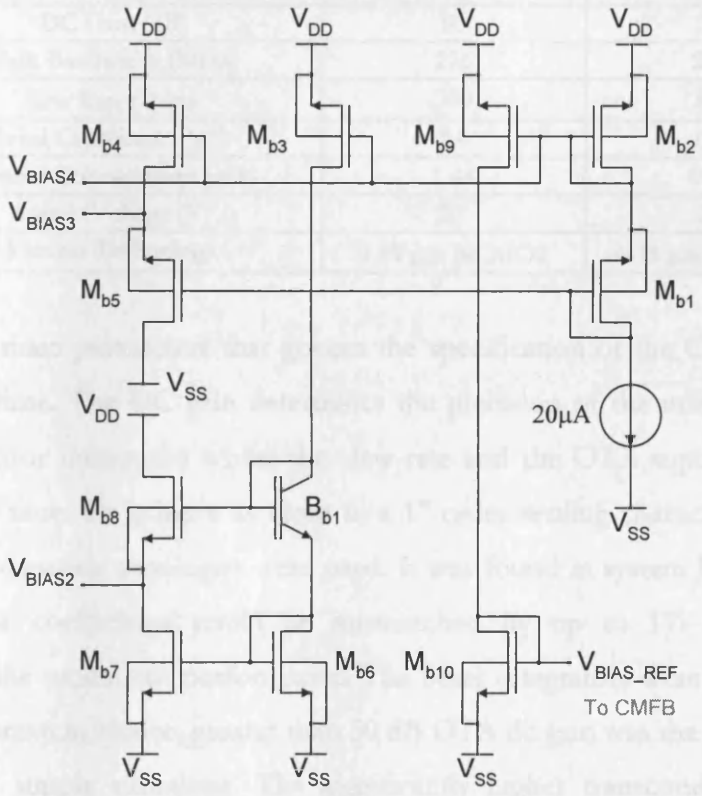

Fig. 5.27 OTA biasing circuit schematic.

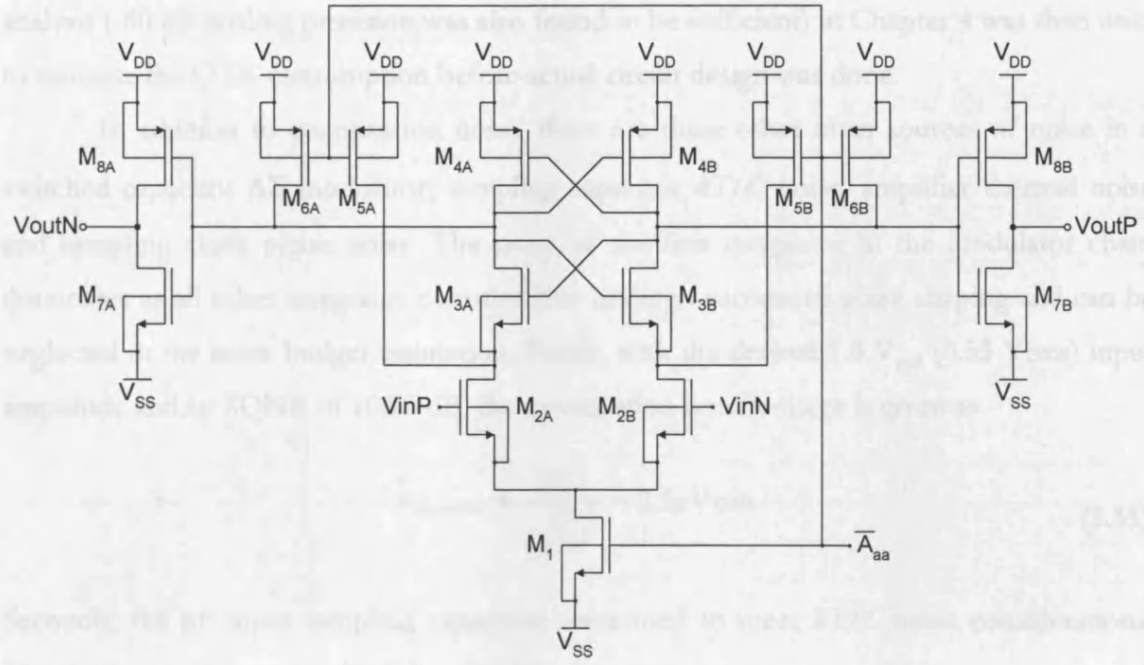

Fig. 5.28 Dynamic Comparator (1-bit quantizer) schematic.

Table 5.8 GSM ΔΣ modulator OTA performance summary.

Parameters	BiCMOS OTA	CMOS OTA
Phase Margin (°)	83	81
DC Gain (dB)	80	53
Gain Bandwidth (MHz)	276	222
Slew Rate (V/μs)	300	300
Load Capacitance (pF)	2.4	0.8
Current Consumption (mA)	1.44	0.24
Supply Voltage (V)	2.7	2.7
Process Technology	0.35 μm BiCMOS	0.35 μm BiCMOS

The two main parameters that govern the specification of the OTA are the dc gain and the settling time. The DC gain determines the precision of the integration coefficients (neglecting capacitor mismatch) whilst the slew-rate and the OTA topology determine the amplifier settling time. To achieve as close to a 1st order settling characteristics as possible, the above folded-cascode topologies were used. It was found in system level simulation that the 1st integrator coefficients could be mismatched by up to 1% without significant deterioration of the modulator performance. The other integrators were even more tolerant to coefficient mismatch. Hence, greater than 50 dB OTA dc gain was the target over process, temperature and supply variations. The significantly higher transconductance and lower parasitics of the bipolar common-base device enabled the achievement of greater than 80 dB nominal dc gain for the BiCMOS OTA (worst-case was 65 dB). The slew-rate and settling

analysis (-60 dB settling precision was also found to be sufficient) in Chapter 4 was then used to estimate the OTA consumption before actual circuit design was done.

In addition to quantization noise, there are three other main sources of noise in a switched capacitor ΔΣ modulator; sampling capacitor kT/C noise, amplifier thermal noise and sampling clock phase noise. The noise of the first integrator in the modulator chain dominates as all other integrator contributions undergo successive noise shaping and can be neglected in the noise budget estimation. Firstly, with the desired 1.5 V_{ppd} (0.53 Vrms) input amplitude and an SQNR of 106.5 dB, the quantization noise voltage is given as

$$\bar{v}_{quantize} = \frac{0.53}{10^{\frac{106.5}{20}}} = 2.5\mu Vrms \tag{5.35}$$

Secondly, 0.8 pF input sampling capacitors were used to meet kT/C noise considerations. The thermal noise as a result of the sampling capacitors is approximated by

$$\bar{v}_{thermal} \approx \sqrt{\frac{4kT}{OSR \cdot C}} = 14.7\mu Vrms \tag{5.36}$$

Cadence® SpectreRF® was used to simulate the total noise of the folded cascode amplifier and the noise integrated over the desired 10 kHz to 135 kHz bandwidth. The result is given below.

$$\bar{v}_{amplifier} = 2.6\mu Vrms \tag{5.37}$$

The phase noise profile of the internal non-overlapping clock generator circuit was also integrated within the above bandwidth and the result is

$$\bar{v}_{clock} = 25\mu Vrms \tag{5.38}$$

Total noise is thus

$$\bar{v}_{noise} = 10^{-6}\sqrt{2.5^2 + 2.6^2 + 14.7^2 + 25^2} = 29.22\mu Vrms \tag{5.39}$$

Finally, expected modulator SNR is given by

$$SNR = 20 \cdot \log_{10}\left(\frac{0.53}{29.22\mu}\right) = 85.2\ dB \tag{5.40}$$

Simulated power consumption of the entire modulator was about 7 mW at 2.7 V operation.

5.8 WCDMA ΔΣ Modulator Design

In Section 5.4, it was found that a 67dB SNR ADC was required for WCDMA. A 153.6 MHz signal will be used as the ADC's clock. Hence with 1.92 MHz desired WCDMA bandwidth, the OSR required was 40. Equations (5.14) and (5.15) were used to predict the theoretical SQNR for various 1-bit modulator orders. A model of the Butterworth NTF 1-bit modulator was also used to simulate the system and the results tabulated below.

Table 5.9 Theoretical and simulated WCDMA ΔΣ modulator SQNR (OSR = 40).

Modulator Order (L)	1	2	3	4
A. SQNR (dB) from (5.40)	50.67	74.99	98.55	121.74
B. Modulator model SQNR (dB)	46.15	57.69	62.62	62.65
Difference between **A** and **B** (dB)	4.52	17.30	35.93	59.09

It can thus be seen that a 4th order topology will only suffice if NTF zeros are shifted from dc. SQNR dominates kT/C noise in this application. The same NTF as in (5.34) was used to obtain peak out-of-band gain of 1.3. This corresponded to a 3 dB frequency of 4.899 MHz. The WCDMA ΔΣ modulator was also stable at all in-band frequencies for 75% of full-scale input amplitude.

The next step was now to iteratively shift c_1 from dc until the transfer function conjugate zeros were positioned just at the edge of the 1.92 MHz pass-band. This was achieved with $c_1 = 0.035$ with the notch appearing at 1.62 MHz and SQNR improving by 10 dB to 72.85 dB. c_2 was also not used as for the GSM design. In the circuit implementation, coefficient a_4 was fixed at 1/8; the same as a_3 because of the difficulty in realizing the required 12.5 fF sampling capacitor in layout if the original value of 1/16 was used. Fig. 5.29 is the modulator power spectrum from system simulation. At the elevated sampling rate of 153.6 MHz, MOS-only amplifiers could not deliver the > 1 GHz gain bandwidths required hence BiCMOS OTAs were used for all 4 integrators. The first OTA was the higher-performance lower noise design and consumed the most current (2.88 mA). The other OTAs each consumed 0.48 mA current. Table 5.10 below summarizes the OTA performance.

Simulated modulator power consumption was about 14 mW. 0.1 pF input sampling capacitors and 0.2 pF integrating capacitors were used with the noise budget considerations given below.

$$\bar{v}_{quantize} = \frac{0.53}{10^{\frac{72.85}{20}}} = 120.7\mu Vrms \tag{5.41}$$

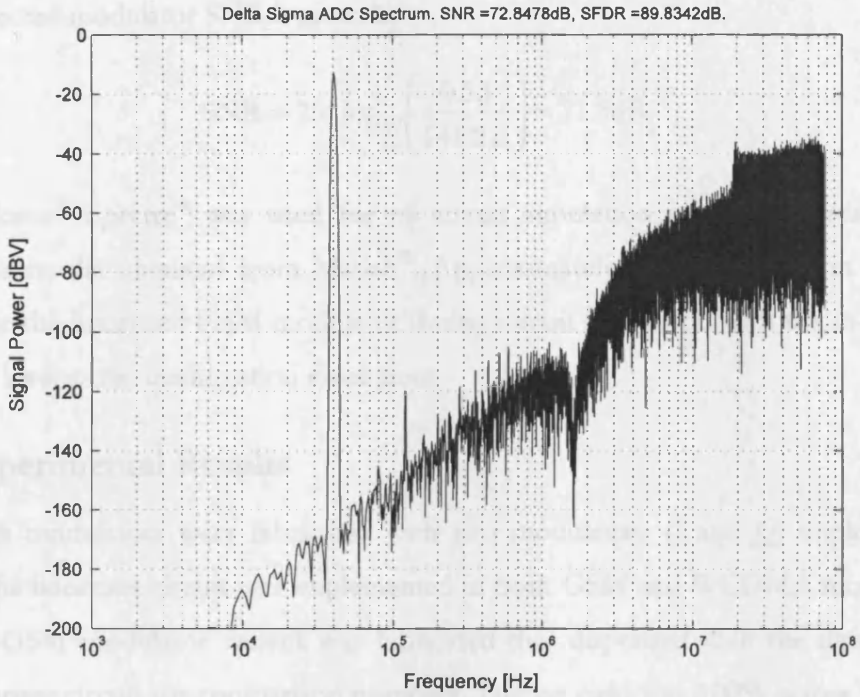

Fig. 5.29 WCDMA ΔΣ modulator power spectrum plot with the zero at 1.62 MHz.

Table 5.10 WCDMA ΔΣ modulator OTA performance summary.

Parameters	BiCMOS OTA 1	BiCMOS OTA 2
Phase Margin (°)	50	67.5
DC Gain (dB)	81.6	79.8
Gain Bandwidth (MHz)	1500	639
Slew Rate (V/μs)	2700	1628
Load Capacitance (pF)	0.8	0.25
Current Consumption (mA)	2.88	0.48
Supply Voltage (V)	2.7	2.7
Process Technology	0.35μm BiCMOS	0.35μm BiCMOS

The thermal noise as a result of the 0.1pF sampling capacitors is approximated by

$$\bar{v}_{thermal} \approx \sqrt{\frac{4kT}{OSR \cdot C}} = 64.3\mu Vrms \tag{5.42}$$

Integrated amplifier noise (10 kHz to 1.92 MHz) is

$$\bar{v}_{amplifier} = 3\mu Vrms \tag{5.43}$$

Integrated clock generator phase noise (10 kHz to 1.92 MHz) is

$$\bar{v}_{clock} = 35\mu Vrms \tag{5.44}$$

Total noise is thus

$$\bar{v}_{noise} = 10^{-6}\sqrt{3^2 + 35^2 + 64.3^2 + 120.7^2} = 141.2\mu Vrms \tag{5.45}$$

Finally, expected modulator SNR is given by

$$\mathrm{SNR} = 20 \cdot \log_{10}\left(\frac{0.53}{141.2\mu}\right) = 71.5\mathrm{dB}. \tag{5.46}$$

Cadence® Spectre® was used for all circuit simulation and SQNR results closely matched the results obtained from Matlab®. Approximately 30 dB increase in SFDR was observed for the linearised GSM modulator during circuit simulation with the in-band tones at the same level as the quantization noise floor.

5.9 Experimental Results

Both modulators were fabricated with two modulators (*I* and *Q*) implemented on each die. The linearisation circuit was implemented in both GSM and WCDMA modulators. In addition, a GSM modulator variant was fabricated that dispensed with the input sampling switch linearisation circuit for comparison purposes. Device yield was 100% across 20 samples. Measurements were carried out using a 110 dB SNR Rohde and Schwarz UPL audio signal generator for the input signal and a Hewlett Packard low-noise RF generator for the clocks. A third-order *L-C* transitional filter (500 kHz cut-off frequency for GSM, 6 MHz cutoff for WCDMA) was used on the evaluation printed circuit board (PCB) for anti-aliasing. Single-ended to differential conversion was done using dual operational amplifiers with Texas Instrument OPA2227 part used for the GSM evaluation board and Analog Devices AD8058 part used for the WCDMA evaluation board. 2^{17} output data points for GSM and 2^{15} data points for WCDMA were iteratively collected using a Hewlett Packard 16700 logic analyzer mainframe and post-processed using Matlab®. Fig. 5.30 is a block diagram of the GSM and WCDMA ΔΣ modulator test setup.

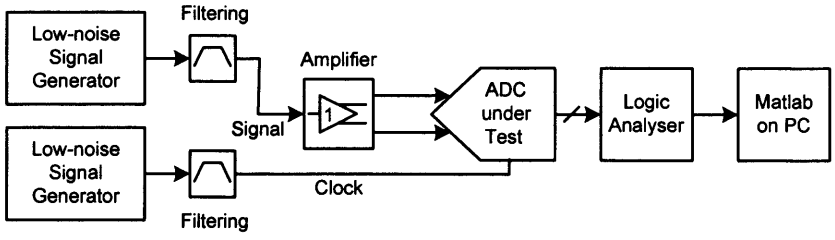

Fig. 5.30 GSM and WCDMA ΔΣ modulator test setup.

5.9.1 GSM ΔΣ ADC Silicon

Fig. 5.31 is the microphotograph of the GSM ADC.

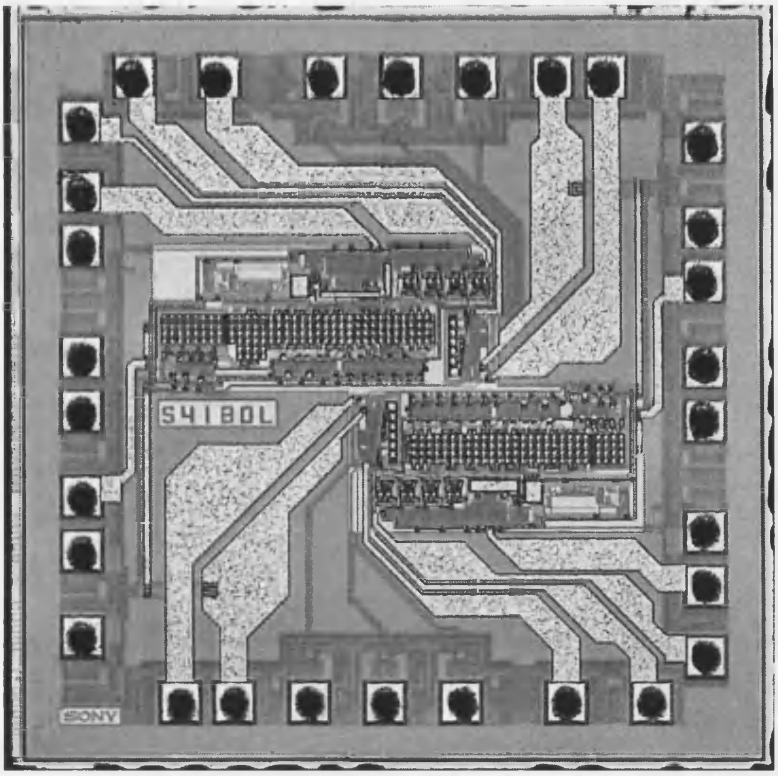

Fig. 5.31 GSM ΔΣ modulator microphotograph.

The ADC occupied about 0.2 mm^2 silicon area. Below are the power spectral plots for the linearised and non-linearised GSM ADC showing about 12 dB improvement in SFDR as a result of the lineariser circuit with over 83 dB SNR and over 85 dB SFDR measured.

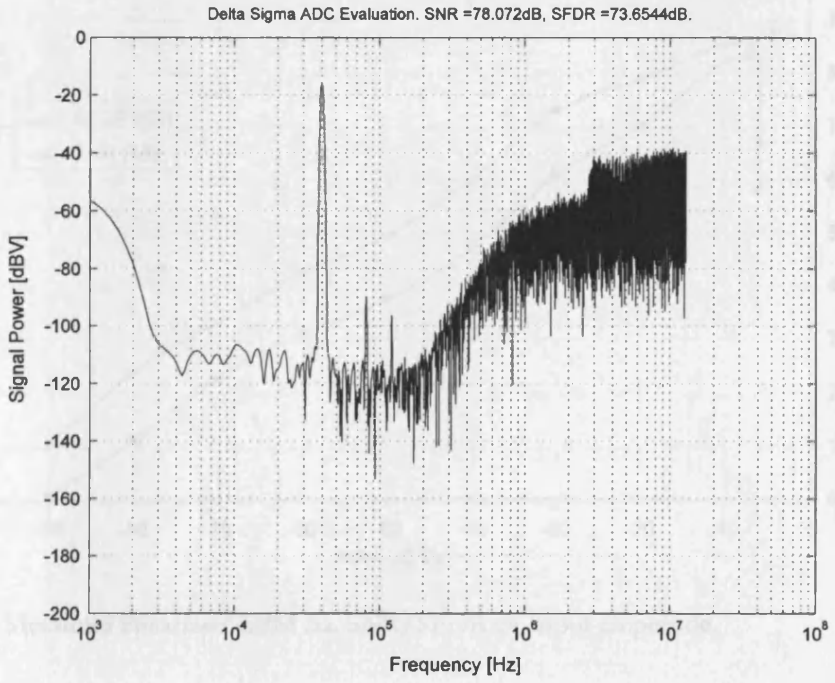

Fig. 5.32 Measured un-linearized GSM ΔΣ modulator power spectrum.

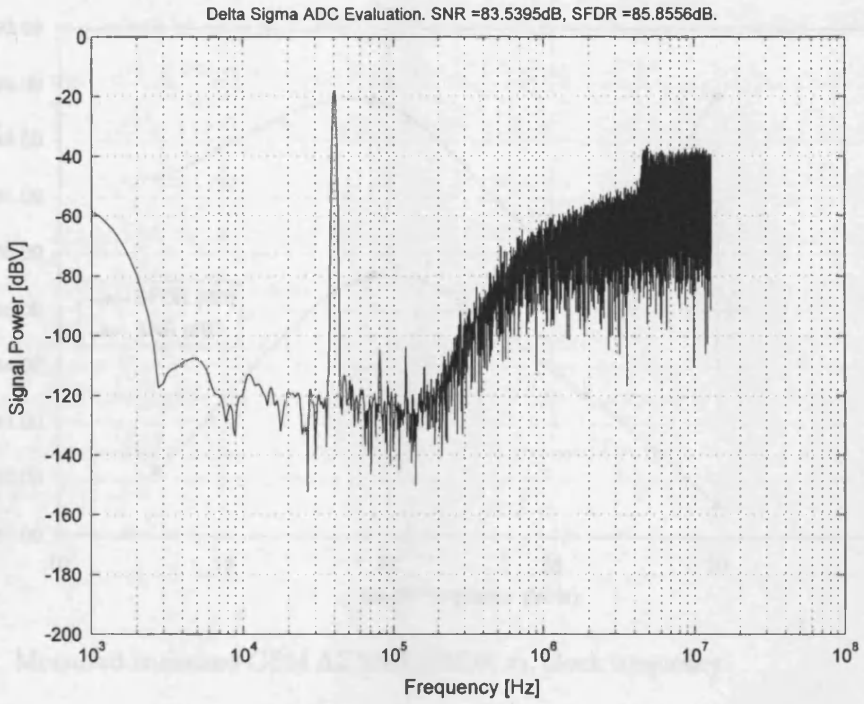

Fig. 5.33 Measured linearized GSM ΔΣ modulator power spectrum.

The zero at 115 kHz is not visible in the above spectrum because thermal noise dominates as expected. The GSM ADC was then characterized for SNR and SFDR over input amplitude and frequency. The results are shown in Figs 5.34 and 5.35.

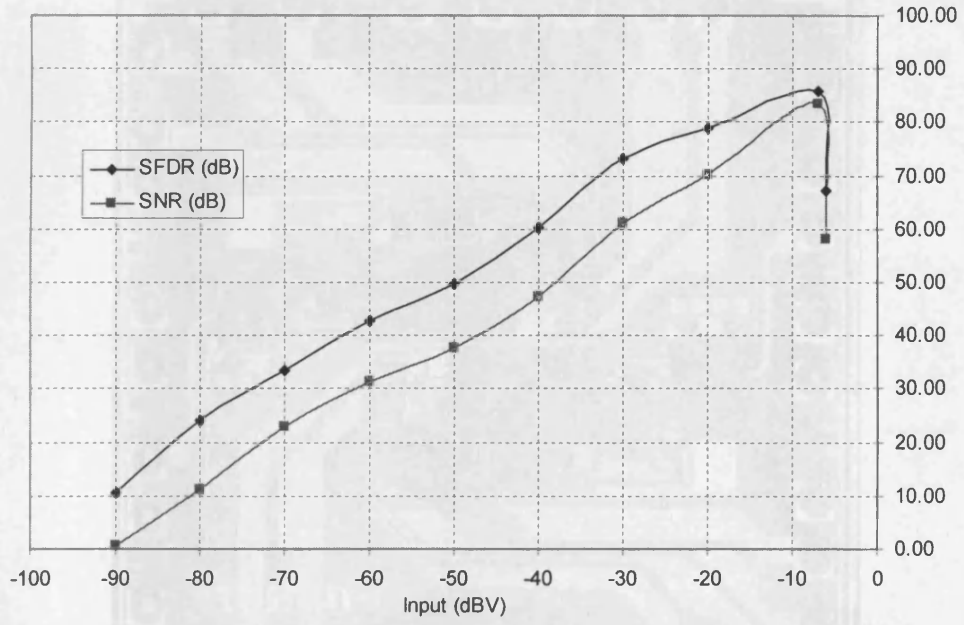

Fig. 5.34 Measured linearized GSM ΔΣ SNR/SFDR vs. input amplitude.

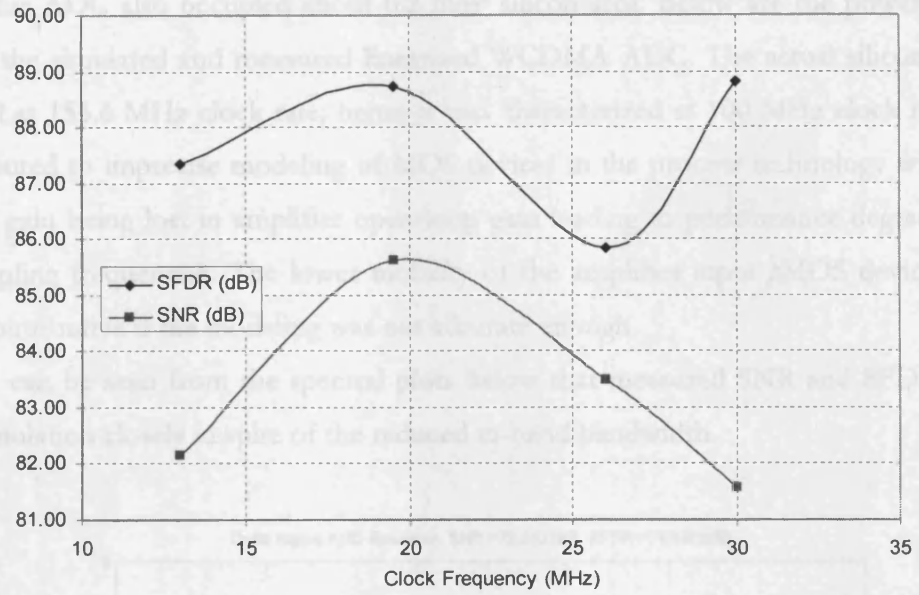

Fig. 5.35 Measured linearized GSM ΔΣ SNR/SFDR vs. clock frequency.

5.9.2 WCDMA ΔΣ ADC Silicon

Fig. 5.36 is the microphotograph of the WCDMA ADC (to save layout time, the same reticule was used for both GSM and WCDMA ADC with the OTAs replaced and excess components (unit capacitors) left unconnected on the WCDMA die.

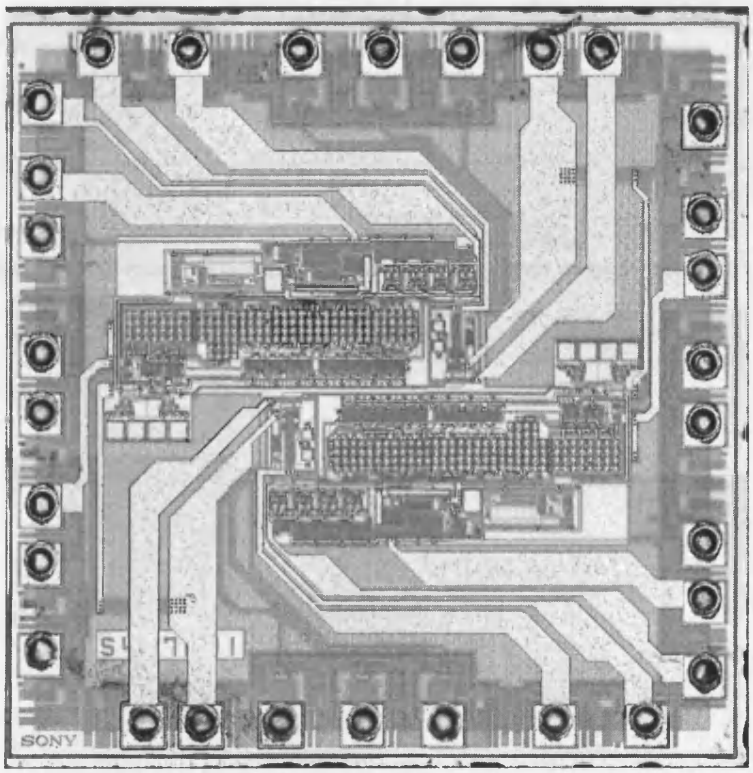

Fig. 5.36 WCDMA ΔΣ modulator microphotograph.

This ADC also occupied about 0.2 mm^2 silicon area. Below are the power spectral plots for the simulated and measured linearized WCDMA ADC. The actual silicon did not work well at 153.6 MHz clock rate; hence it was characterized at 100 MHz clock rate. This was attributed to imprecise modeling of MOS devices in the process technology with up to 20 dB of gain being lost in amplifier open-loop gain leading to performance degradation at high sampling frequencies. The lower mobility of the amplifier input *p*MOS devices could also be contributive if the modeling was not accurate enough.

It can be seen from the spectral plots below that measured SNR and SFDR results match simulation closely in spite of the reduced in-band bandwidth.

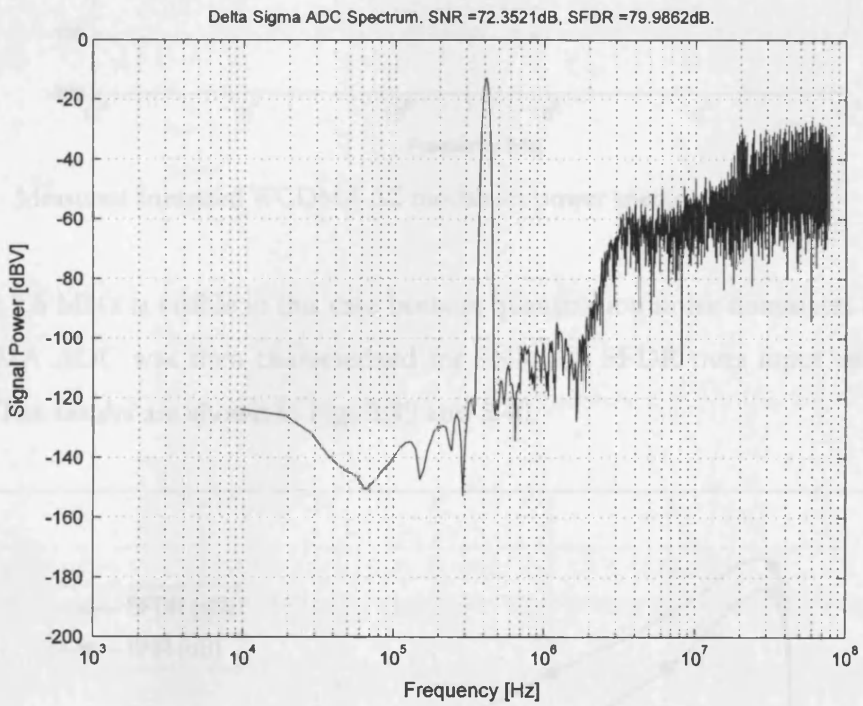

Fig. 5.37 Simulated linearized WCDMA ΔΣ modulator circuit power spectrum.

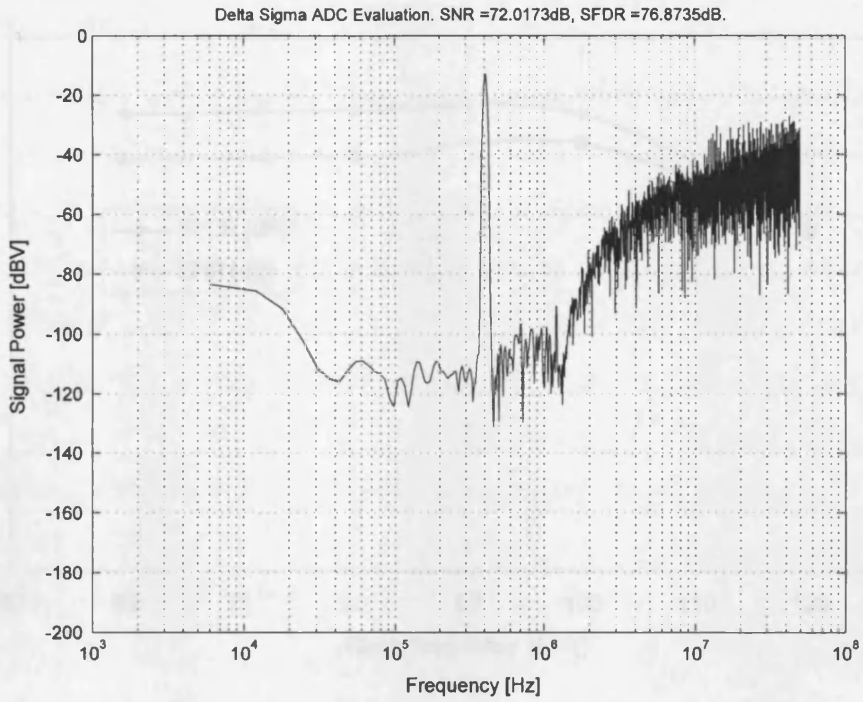

Fig. 5.38 Measured linearized WCDMA ΔΣ modulator power spectrum.

The zero at 1.6 MHz is visible in this case because quantization noise dominates as expected. The WCDMA ADC was then characterized for SNR and SFDR over input amplitude and frequency. The results are shown in Figs 5.39 and 5.40.

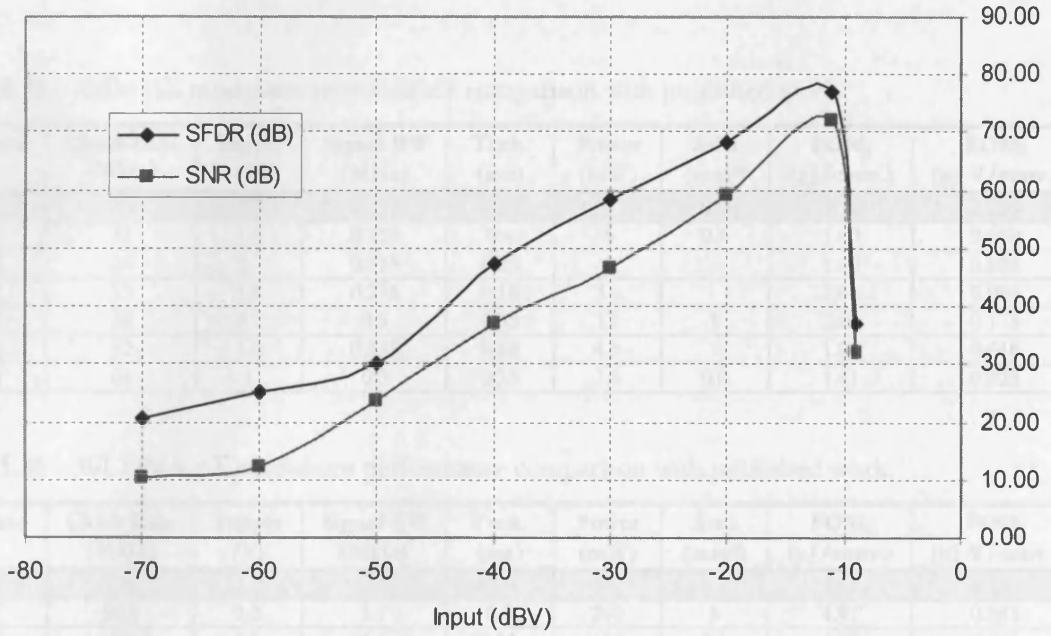

Fig. 5.39 Measured linearized WCDMA ΔΣ SNR/SFDR vs. input amplitude.

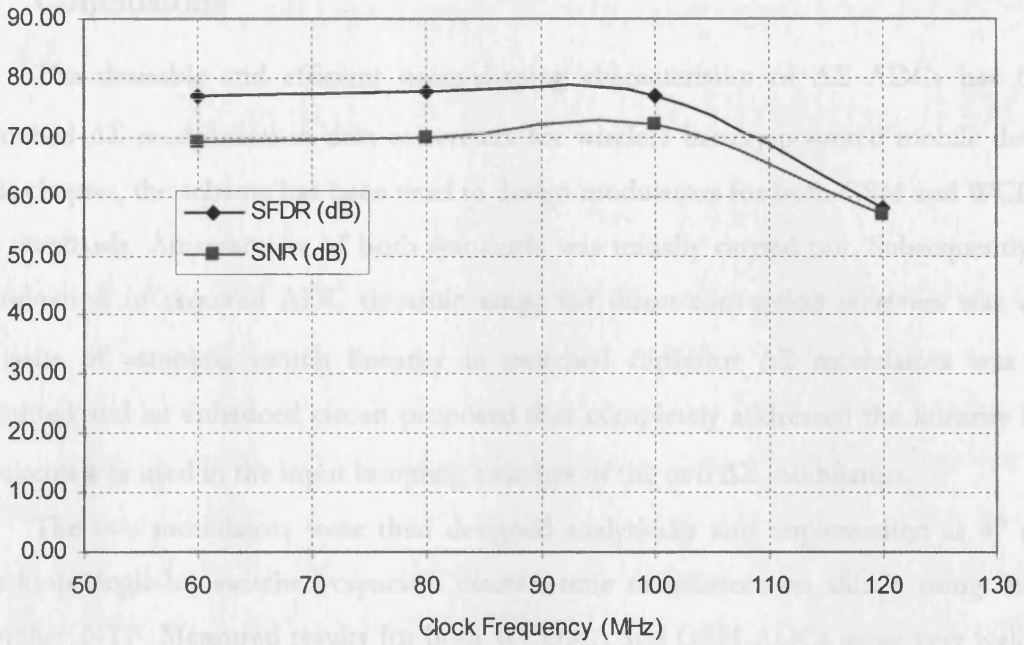

Fig. 5.40 Measured linearized WCDMA ΔΣ SNR/SFDR vs. clock frequency.

The tables below compare published switched-capacitor low-pass modulator work to both the GSM and WCDMA modulators using the FOMs defined in equations (2.20) and (2.21) in Chapter 2. SNR was used for ENOB calculation and the Nyquist bandwidths were used as ERBW.

Table 5.11 GSM ΔΣ modulator performance comparison with published work.

Reference	Clock Rate (MHz)	Supply (V)	Signal BW (MHz)	Tech. (μm)	Power (mW)	Area (mm^2)	FOM_1 (pJ/conv.)	FOM_2 (pJ·V/conv.)
This work	**26**	**2.7**	**0.135**	**0.35**	**7**	**0.2**	**2.11**	**0.059**
[134]	13	1.8	0.135	0.4	5	0.4	1.60	0.060
[194]	26	2.7	0.135	0.25	4	-	1.00	0.028
[196]	53	1.8	0.276	0.18	15	-	2.64	0.050
[197]	32	2.7	0.5	0.35	12	1	2.07	0.175
[198]	32	1.8	0.135	0.18	4.5	-	1.02	0.016
[200]	64	1	0.5	0.13	7.4	0.6	1.61	0.025

Table 5.12 WCDMA ΔΣ modulator performance comparison with published work.

Reference	Clock Rate (MHz)	Supply (V)	Signal BW (MHz)	Tech. (μm)	Power (mW)	Area (mm^2)	FOM_1 (pJ/conv.)	FOM_2 (pJ·V/conv.)
This work	**100**	**2.7**	**1.25**	**0.35**	**14**	**0.2**	**1.72**	**0.116**
[170]	52.8	3.3	1.1	0.5	200	5	4.97	0.683
[191]	64	3.3	1.1	0.35	180	2.6	4.08	0.463
[195]	50	1.8	1	0.18	18.8	6.5	3.64	0.262
[198]	32	1.8	1.92	0.18	7	-	3.15	0.681
[199]	32	1.8	2	0.18	150	2.86	3.25	0.731
[201]	70.4	2.5	2.2	0.25	66	2.78	2.56	0.400

5.10 Conclusions

The desirable and efficient noise-shaping characteristics of ΔΣ ADCs has firmly entrenched ΔΣ modulation in data-converters for wireless battery-powered mobile devices. In this chapter, the scheme has been used to design modulators for both GSM and WCDMA radio standards. An overview of both standards was initially carried out. Subsequently, the determination of required ADC dynamic range for direct-conversion receivers was done. The issue of sampling switch linearity in switched capacitor ΔΣ modulators was then highlighted and an enhanced circuit proposed that completely addressed the linearity issue. This circuit was used in the input sampling switches of the two ΔΣ modulators.

The two modulators were then designed analytically and implemented as 4^{th} order single-loop single-bit switched-capacitor discrete-time modulators on silicon using Inverse Chebyshev NTF. Measured results for both WCDMA and GSM ADCs agree very well with simulation with the WCDMA ADC failing to reach the designed 153.6 MHz clock rate as a result of process related issues. It was subsequently characterized at up to 100 MHz and surpassed expectation. Table 5.13 is a summary of both the GSM and WCDMA ADC performance. Digital decimation of the modulator outputs to Nyquist was not implemented on silicon as a result of time constraints and will be considered in the future.

Table 5.13 GSM and WCDMA ΔΣ ADC performance summary.

Parameters	Specification	Measured	Specification	Measured
	GSM ADC		WCDMA ADC	
SNR (dB)	83	83.5	67	72
SFDR (dB)	85	85.8	70	76.9
Sampling Rate (MHz)	26	26	153.6	100
Signal Bandwidth (MHz)	0.135	0.135	1.92	1.25
Power Consumption (mW)	7	7	14	14
Input Amplitude (Vppd)	1.5	1.5	1.5	1.5
3σ Input Offset (mV)	5	3	7	5
Supply Voltage (V)	2.7	2.7	2.7	2.7
Silicon Area (mm^2)	0.2	0.2	0.2	0.2
Process Technology	0.35 μm 1P 4M SiGe BiCMOS with M3M4 MiM capacitors			

6 Calibration Techniques for High Resolution Multi-Bit Pipeline ADCs

"Iron sharpeneth iron ..." Pro. 27:17 KJV

With the high-speed and low silicon estate merits of the pipeline ADC architecture elucidated in Chapters 3 and 4, it is apparent that overall n-bit ADC linearity is only guaranteed if the first few sub-DACs are at least n-bit linear. This is difficult to achieve for >10-bit resolution without trimming, device averaging, noise-shaping or some form of calibration, since capacitors in a switched-capacitor DAC design will only match to about 0.1% at best. Resistor matching in ladder or R-2R DACs is even worse. About 14-bit performance has been achieved without trimming, averaging, dithering or calibration in [193], but with large device areas to guarantee matching, which increased power consumption and slightly compromised the high-frequency performance of the design as a result of large device parasitics. Laser trimming the pipeline ADC's sub-DACs to the required precision is a very expensive process and is unsuitable for low-cost devices. In addition, since it is a one-off irreversible procedure, aging effects and temperature will still affect the performance of the laser-trimmed ADC. Device averaging techniques are ideally suited to over-sampling designs (OSR $\geq$ 2) with [39] achieving 100 dB SFDR for a 14-bit over-sampled pipeline ADC using capacitor averaging techniques. Analog and digital calibration techniques have also been used in the literature [203]-[211], but tend to consume higher power and area as a result of significant hardware redundancy. Dithering and mismatch-shaping [212] have also been used to design over-sampled pipeline ADCs, but effective bandwidth is reduced as a result of the over-sampling, and additional logic is usually required to filter the out-of-band noise.

This chapter examines the various available calibration schemes in the literature and highlights their limitation from a power consumption perspective. It then describes in detail, a novel segmented calibration scheme for multi-bit quantizers that has small area overhead, consumes low power and enables the use of the ADC over its entire Nyquist bandwidth. Subsequently, circuit design and simulated results for a 12-bit, 120 MS/s ADC designed using the proposed calibration scheme is presented with conclusions following.

6.1 Correctible Pipeline ADC Errors

The main errors plaguing the pipeline ADC architecture are sub-ADC comparator offset errors, sub-DAC matching errors, inter-stage gain errors and inter-stage amplifier offset errors. Since the inter-stage amplifiers drive a succeeding sub-ADC, their offset errors can usually be lumped together with that of the succeeding ADC comparators and treated as one entity. This section is based on the above supposition.

6.1.1 Comparator Offset Error

Fig. 6.1 depicts an n-bit pipeline ADC with each stage containing an m-bit sub-ADC (quantizer) and sub-DAC, a subtractor and a quantization error amplifier.

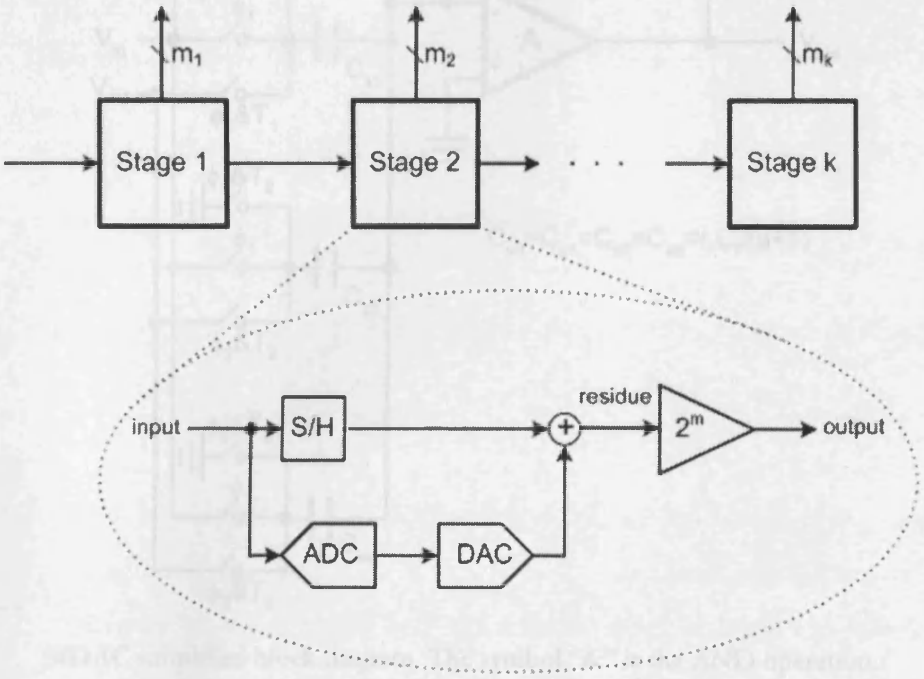

Fig. 6.1 Pipeline ADC block diagram.

The sub-DAC, subtraction and amplification functions are usually combined in a switched-capacitor circuit called a multiplying DAC (MDAC) and a single-ended version is shown in Fig. 6.2. T_1, T_2 ... T_d are the thermometer-code output of the sub-ADC and the subscript d is 2^m-1. C_{s0} to C_{sd} are the input sampling capacitors. C_f is the feedback capacitor. For a 12-bit, 2-bits-per-stage ADC with no redundancy, five 2-bit MDACs and six comparators are required with the overall ADC output word given by the following generic equation:

$$D_{OUT} = D_k \cdot r^{(n/m)-1} + D_{k-1} \cdot r^{(n/m)-2} + \cdots + D_2 \cdot r + D_1 \qquad (6.1)$$

where D_k is the MSB sub-ADC's digital output (with integer values ranging from 0 to $2^m - 1$) and r is the radix of the converter which in the 2-bits-per-stage case is ideally equal to 4. The actual converter radix is usually slightly different from the ideal case as a result of capacitor mismatch and finite opamp gain, hence the need for calibration or mismatch shaping.

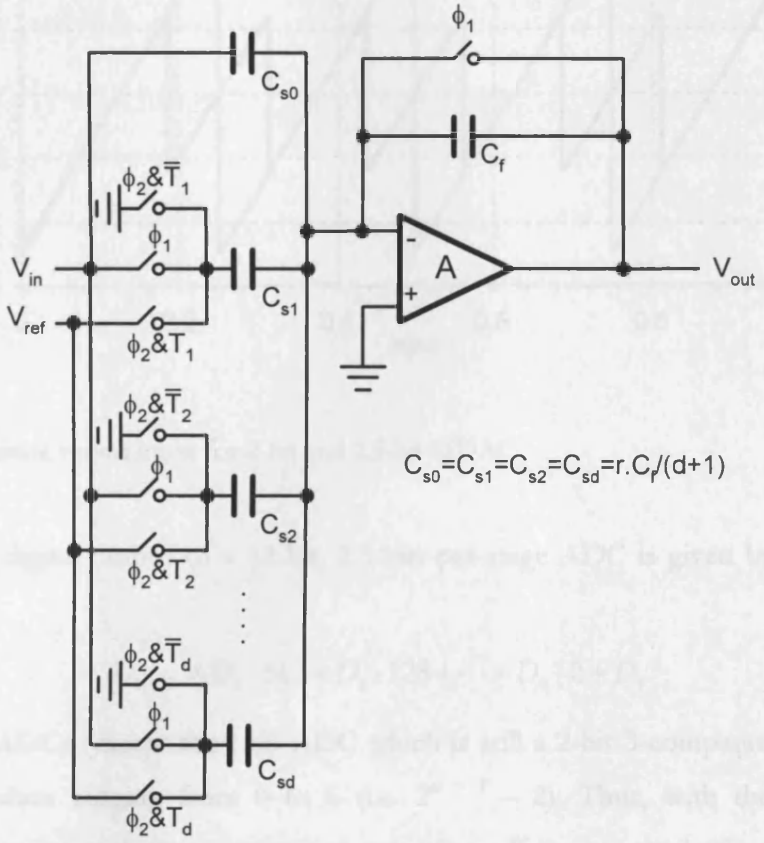

Fig. 6.2 MDAC simplified block diagram. The symbol "&" is the AND operation.

Equation (6.1) reduces to the following expression for the 12-bit, 2-bits-per-stage case:

$$D_{OUT} = D_6 \cdot 1024 + D_5 \cdot 256 + \cdots + D_2 \cdot 4 + D_1 \qquad (6.2)$$

This converter is very sensitive to comparator systematic offset errors since no redundancy is built in. If $2^m - 1$ additional comparators are added to the sub-ADC, whilst keeping the radix the same and the threshold points changed slightly to allow some overlapping at its extreme bounds (Fig. 6.3), the pipeline ADC becomes the well known [73]-[74] *m*.5-bits-per-stage ADC with simple digital error correction implemented by overlapping and adding the inter-stage outputs. Thus, no information is lost even when a comparator makes an erroneous decision because the succeeding stage's comparators have enough range to digitize the

residue. This redundancy allows the use of comparators with offsets as high as $\pm V_{ref}/(2^{m+1})$, a significant improvement over the required $\pm V_{ref}/(2^{n+1})$ comparator accuracy of the *m*-bit-per-stage ADC.

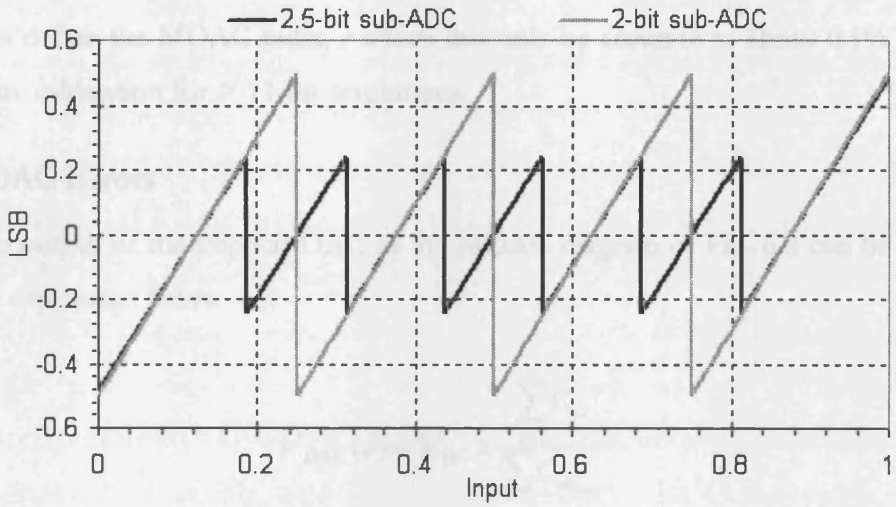

Fig. 6.3 Residue versus input for 2-bit and 2.5-bit MDAC.

The final digital output of a 12-bit, 2.5-bits-per-stage ADC is given by the following expression:

$$D_{OUT} = D_6 \cdot 512 + D_5 \cdot 128 + \cdots + D_2 \cdot 2 + D_1 \tag{6.3}$$

where the sub-ADCs (except the LSB ADC which is still a 2-bit 3-comparator design) now have integer values ranging from 0 to 6 (i.e. $2^{m+1} - 2$). Thus, with the use of slight redundancy, the issue of comparator and amplifier offset is completely addressed in a pipeline ADC.

6.1.2 MDAC Gain Error

Since each MDAC comprises an amplifier of open loop dc gain A in addition to sampling and feedback capacitors as shown in Fig. 6.2, their radices will differ with variance akin to that of the statistical distribution of the capacitor mismatch. Modifying (6.1) thus gives:

$$D_{OUT} = D_k \cdot r_1^{(n/m)-1} + D_{k-1} \cdot r_2^{(n/m)-2} + \cdots + D_2 \cdot r_k + D_1 \tag{6.4}$$

where $r_1, r_2, \ldots, r_k$ are MDAC radices for stages 1 to k which ideally should equal 4 for a 2.5-bits-per-stage partitioning. Considering only a single composite input capacitor C_i and the feedback capacitor C_f, the radices can be expressed in the general form below:

$$r_x = \frac{A \cdot C_{ix}}{C_{ix} + A \cdot C_{fx}} \approx \frac{C_{ix}}{C_{fx}} \quad \text{as } A \to \infty \tag{6.5}$$

In reality, A is not infinite but the criteria for (6.5) to be valid for all r_x is that $A \geq 2^{n+1+m}$. Once the requirement for A in (6.5) is met, the ratio between the sampling and feedback capacitors define the MDAC radix, r which can only be accurate to about 0.1% at best and will require calibration for > 11-bit resolutions.

6.1.3 DAC Errors

The output of the implicit DAC in the MDAC diagram of Fig. 6.2 can be generalized using the expression below

$$V_{DAC}(d) = V_{ref} \times \frac{\sum_{i=1}^{d} C_{si}}{\sum C_{sd_{max}}} \tag{6.6}$$

with the main source of error being the matching of the unit-sized input sampling capacitors $C_{s0} \ldots C_{sd}$. The MDAC topology in Fig. 6.2 allows the lumping together of both the sampling capacitor and the feedback capacitor with DAC errors and MDAC gain (radix) errors calibrated out simultaneously with the composite MDAC output equation given by:

$$V_{MDAC} = \frac{(C_{s0} + C_{s1} + C_{s2} + \ldots + C_{sd}) \cdot V_{in} - (T_1 \cdot C_{s1} + T_2 \cdot C_{s2} + \ldots + T_d \cdot C_{sd}) \cdot V_{ref}}{C_f} \tag{6.7}$$

where ideally, $C_{s0} = C_{s1} = C_{s2} = C_s \ldots = C_{sd} = 0.5C_f$.

6.2 ADC Calibration Schemes

Since mismatch, dynamic element randomization and spectral error shaping techniques [177] – [184] are ideally suited to over-sampled architectures; calibration techniques are mainly used for Nyquist architectures. Calibration of a pipeline ADC can be done digitally [204] – [209] (the DAC and radix errors are digitally extracted be means of statistical correlation and corrected in the digital domain), in analog [210] (smaller ratios of the mismatched devices are switched in or out under digital control to correct errors in the analog domain) and can be carried out in the fore-ground (normal operation of the ADC is disrupted in order to carry out the calibration procedure), or discretely in the background without affecting the ADC operation with the latter the most preferred option. An all-analogue capacitor error averaging technique has also been used in the literature [39] with over 100 dB SFDR obtained for a 14-bit 12 MS/s design, the overhead being a global clock

rate of twice the ADC sample rate. As explained in Section 6.1, digital error correction already alleviates comparator and MDAC amplifier offset errors leaving sub-DAC and radix errors, which can be significantly reduced by calibration. Galton [213] proposed a digitally intensive algorithm that can cancel DAC mismatch noise in pipeline ADCs with the use of statistical correlation using a pseudorandom generator but may not be power efficient at high sampling speeds. Keane et al [207] in addition proposed a similar digitally intensive statistic-based algorithm for background calibration of radix errors.

A number of the calibration research in the literature duplicates the entire ADC pipeline to allow for the calibration of the redundant ADC while the main ADC is in use. The main ADC is then periodically swapped for calibration and vice-versa. Moreover, an embedded precision signal source is employed for use in the calibration process, which further adds to the silicon area. The segmented scheme that will be proposed shortly selectively calibrates only the MDACs and uses V_{ref} as a precision calibration reference, thus negating the need for an integrated precision signal source. Error comparison is also done digitally, dispensing with the requirement for an ultra-low offset analogue comparator and only a redundant MDAC is needed, with a low-power (n + 2)-bit 2nd-order delta-sigma ($\Delta\Sigma$) ADC used to digitize the MDAC output for calibration. More than adequate signal-to-quantization noise ratio (SQNR) is achievable with a 2nd order single-bit quantizer $\Delta\Sigma$ ADC of high OSR with scaled OTA biasing for reduced power consumption.

Since only the MDAC is calibrated, the dual-port RAM required for the storage of calibration settings is just a few bytes in size with negligible area overhead and may be realized using flip-flops and some glue logic for addressing and I/O functions. Segmented MDAC calibration has been used previously in the literature with [214] employing a pseudorandom sequence to simultaneously dither the mismatch spectrum of each MDAC. The radix errors are then extracted by correlation in the digital domain. Power consumption and area is high as a result of the use of a calibrator block per MDAC and the extra logic required for spectral correlation. The continuously calibrated 12-bit ADC in [214] also uses a redundant 1.5-bit MDAC (a sample-and-hold amplifier and 15 MDACs used in all, adding to the area and power overhead) for the continuous calibration of only the first two MSBs. In addition, a variable voltage source is integrated and the calibration algorithm is different from that used in this work.

References [215]-[218] also employ an auxiliary array of fine capacitors for the tuning of the MDAC capacitor mismatch as used in this work; the difference being the fact that an

ultra-low offset analogue comparator is not required here since the comparison between the digitized MDAC output and the expected output is computed to n+2-bit precision digitally.

6.3 Proposed Low-Power Segmented Calibration Scheme I

Fig. 6.4 is a demonstrative block diagram of the proposed analog calibration architecture for a 12-bit, 2.5-bits-per-stage pipeline ADC. Each MDAC is swapped out in sequence and replaced with the pre-calibrated redundant MDAC. Once the first MDAC is calibrated, it is swapped back in place and the process repeated for the 2nd MDAC, etc. Fig. 6.6 is the flowchart of the pipeline ADC operation under calibration. MDAC kT/C-based capacitor scaling [218] can still be used across the pipeline with this scheme to save amplifier power consumption if calibration is limited to the first two MDACs (of the same physical dimension), with the redundant MDAC an exact copy of MDACs 1 and 2 to guarantee thermal noise constraint levels. The calibration concept is described below for the 12-bit ADC implementation.

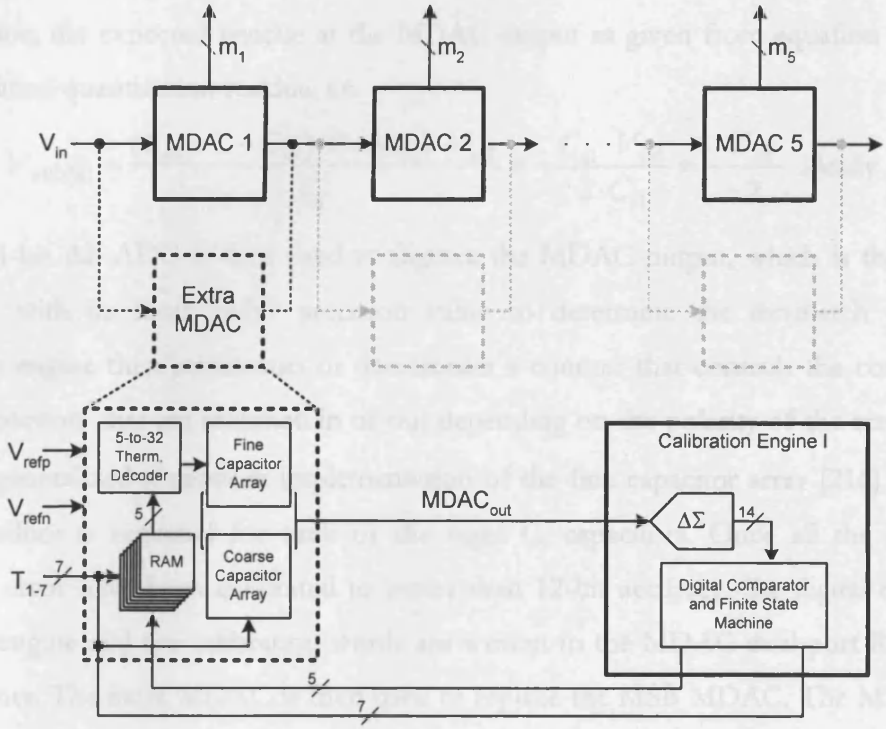

Fig. 6.4 Proposed segmented calibration architecture I.

Consider the case where V_{ref} is applied to the input and all input sampling capacitors switched in (i.e. $T_1 \ldots T_d = 1$). Equation (6.7) then reduces to:

$$V_{MDAC} = \frac{(C_{s0} + ... + C_{sd}) \cdot V_{ref} - (C_{s1} + ... + C_{sd}) \cdot V_{ref}}{C_f} = \frac{C_{s0} \cdot V_{ref}}{2 \cdot C_{s0}} = \frac{V_{ref}}{2} \text{ ideally.} \quad (6.8)$$

Since capacitor mismatch will make (6.8) to be in error and since the feedback capacitor is twice the unit sampling capacitor size, we introduce uncorrelated sampling and feedback capacitor error terms δ_s and δ_f and include in (6.8) to obtain:

$$V_{MDAC} = \frac{(C_{s0} + \delta_s) \cdot V_{ref}}{(C_f + \delta_f)} = \frac{(C_{s0} + \delta_s) \cdot V_{ref}}{2 \cdot (C_{s0} + \delta_f)} = \frac{V_{ref}}{2} \cdot \frac{C_{s0} + \delta_s}{C_{s0} + \delta_f} \quad (6.9)$$

Equation (6.9) shows that it is possible to correct for δ_s whilst simultaneously correcting for δ_f (i.e. calibrating such that $\delta_s = \delta_f$). Hence there is no need to physically calibrate C_f. Under uncorrelated worst-case δ_s and δ_f error of ±1%, the MDAC is in error by approx. 2% (< 0.01% error is required for 12-bit accuracy). If various combinations of an array of 64 $C/256$ capacitors (fine capacitors) are switched across C_s (coarse capacitors), it is possible to calibrate to a precision of ±0.5 LSB DNL and INL accuracy at 12-bit resolution.

A typical calibration procedure will begin in this fashion. First, the extra MDAC's V_{in} is grounded and V_{ref} applied to the MDAC reference input. C_{s1} is then switched in. For exact C_{s1} capacitor, the expected residue at the MDAC output as given from equation (6.7) is the ideal amplified quantization residue, i.e.

$$V_{MDAC} = \frac{(C_{s0} + ... + C_{sd}) \cdot 0 - (C_{s1}) \cdot V_{ref}}{C_f} = -\frac{C_{s1} \cdot V_{ref}}{2 \cdot C_{s1}} = -\frac{V_{ref}}{2} \text{ ideally.} \quad (6.10)$$

A 14-bit ΔΣ ADC is then used to digitize the MDAC output, which is then digitally compared with its ideal 14-bit precision value to determine the mismatch error. The calibration engine then increments or decrements a counter that controls the combinations of fine capacitors that are switched in or out depending on the polarity of the error. Fig. 6.5 depicts a generalized π-network implementation of the fine capacitor array [216] around C_s. The procedure is repeated for each of the eight C_s capacitors. Once all the MDAC C_s mismatch error have been calibrated to better than 12-bit accuracy, the digital comparator stops the engine and the calibration words are written to the MDAC dual-port RAM for all C_s capacitors. The extra MDAC is then used to replace the MSB MDAC. The MSB MDAC is then calibrated and replaced. The next MDAC is also swapped out, calibrated and replaced until all MDACs requiring calibration are calibrated as depicted in the flowchart in Fig. 6.6. The calibration words in the RAM are subsequently used to permanently switch in fine capacitors as required for each coarse capacitor. Hence, there is no need to switch fine capacitors during high-speed normal operation.

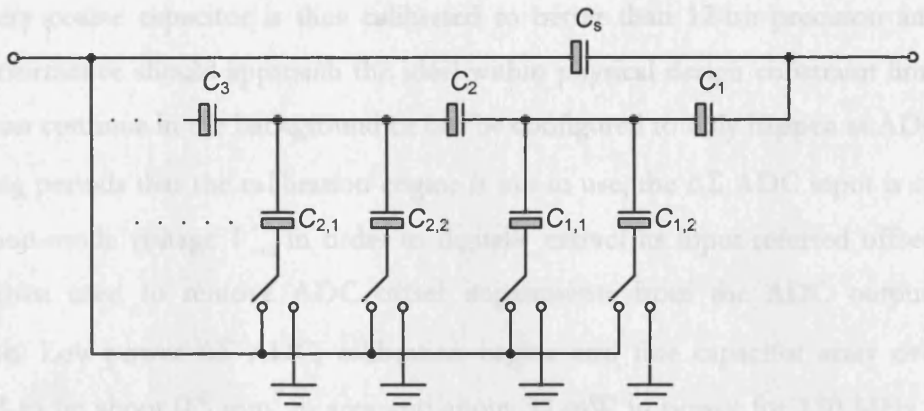

Fig. 6.5 A generalized π-network implementation of fine capacitor array.

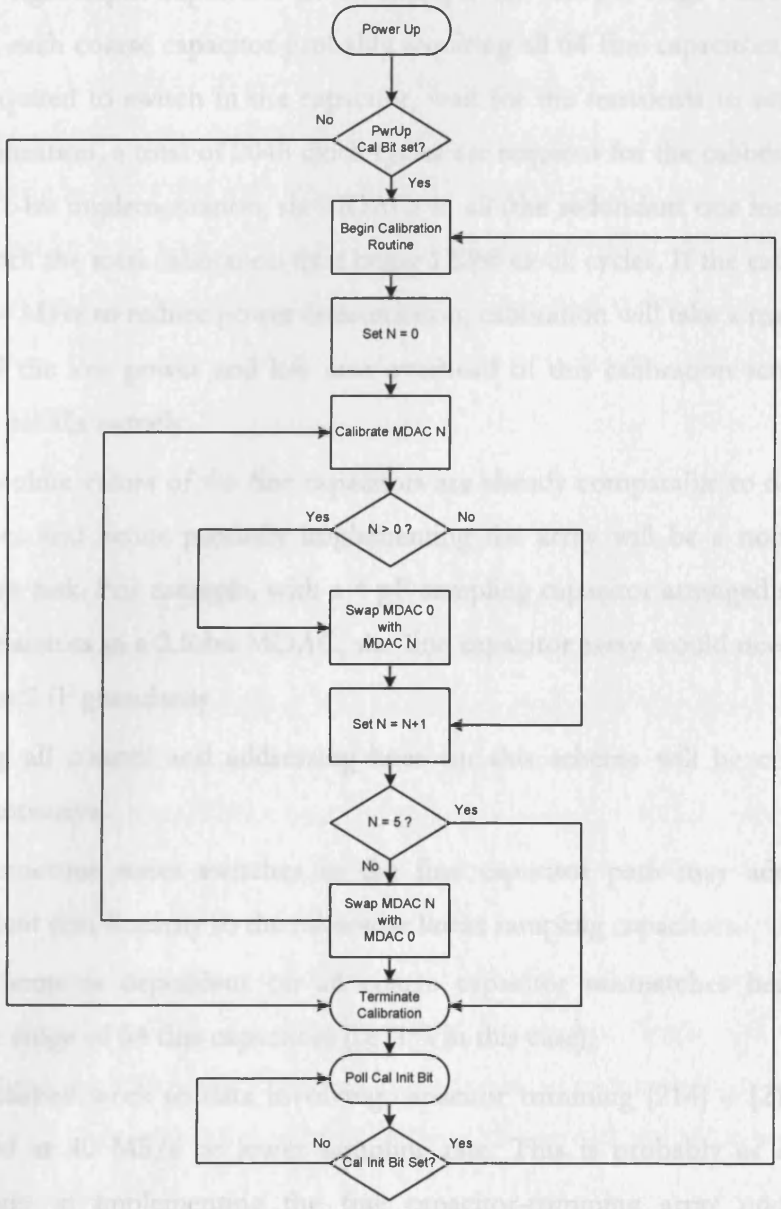

Fig. 6.6 Calibrated pipeline ADC operation flowchart.

Every coarse capacitor is thus calibrated to better than 12-bit precision and overall ADC performance should approach the ideal within physical design constraint limits. This process can continue in the background or can be configured to only happen at ADC power-up. During periods that the calibration engine is not in use, the ΔΣ ADC input is connected to common-mode voltage V_{cm} in order to digitally extract its input-referred offset voltage. This is then used to remove ADC offset impairments from the ADC outputs during calibration. Low-power ΔΣ ADC, calibration engine and fine capacitor array overhead is estimated to be about 0.5 mm^2 in area and about 30 mW in power for 120 MHz sampling clock, using a 0.13 μm CMOS technology.

Since all eight input capacitors in an example 2.5-bits-per-stage MDAC need to be calibrated with each coarse capacitor probably requiring all 64 fine capacitors; and with four clock cycles required to switch in the capacitor, wait for the transients to settle, and repeat the residue digitization, a total of 2048 clock cycles are required for the calibration of a single MDAC. In a 12-bit implementation, six MDACs in all (the redundant one included) need to be calibrated with the total calibration time being 12288 clock cycles. If the calibration engine is clocked at 2.4 MHz to reduce power consumption, calibration will take a maximum of 5.12 ms. In spite of the low power and low area overhead of this calibration scheme, there are some potential pitfalls namely:

- The absolute values of the fine capacitors are already comparable to device and track parasitics and hence precisely implementing the array will be a non-trivial layout-intensive task. For example, with a 4 pF sampling capacitor arranged as eight 500 fF unit capacitors in a 2.5-bit MDAC, the fine capacitor array would need to be precise to about 2 fF granularity.
- Routing all control and addressing lines for this scheme will be complicated and layout intensive.
- The numerous series switches in the fine capacitor path may add some input-dependent non-linearity to the otherwise linear sampling capacitors.
- The scheme is dependent on all coarse capacitor mismatches being within the capture range of 64 fine capacitors (i.e. 1% in this case).
- All published work to date involving capacitor trimming [214] – [216], [219] were designed at 40 MS/s or lower sampling rate. This is probably as a result of the challenges in implementing the fine capacitor-trimming array under high-speed operation.

As a result another scheme that is a direct offshoot from the above was investigated and is described in the next section.

6.4 Proposed Low-Power Segmented Calibration Scheme II

Fig. 6.7 illustrates the new scheme. In this case, the fine capacitor array and each localized MDAC RAM are dispensed with and instead, a larger single block of RAM (divided into addressable *d*-word pages, with each word 14-bit wide and one page per MDAC) used in the logic with the capacitor errors estimated and corrected digitally. Consider again, a situation where the calibration proceeds as in the previous section for the first MDAC. The residues (ideally $V_{ref}/2$) for each switched-in unit capacitor are digitized as before using the low-speed 14-bit ΔΣ ADC. These values are then subtracted digitally from the 14-bit digital equivalent of $V_{ref}/2$ and the mismatch errors stored in RAM for each of the *d* sampling capacitors in the MDAC being calibrated. An extra bit is required in the data-path for signed arithmetic representation of the mismatch error. Thus, all individual unit capacitor mismatch information is available to ±13-bit precision for each calibrated MDAC and can be used to regenerate the table of errors for each thermometer code during normal operation.

For example, if C_{s1}'s error was δ_1, C_{s2}'s error δ_2, etc, for the sub-ADC thermometer code output 0000001 under normal operation, the MDAC's residue error will be δ_1. For code 0000011, the error will be $\delta_1 + \delta_2$. And finally, for thermometer code 1111111, the error will be $\delta_1 + \delta_2 + \ldots + \delta_d$. These regenerated errors can then be added to the sub-ADC's digital binary outputs before aggregating with the rest of the pipeline digital outputs as before. Thus, this scheme refers the error to the digital domain and corrects it with the use of a dynamic code-dependent digital offset. The procedure is repeated for each MDAC swapped out for calibration. The post-sub-ADC/MDAC *logic* blocks depicted in Fig. 6.7 are wired to the calibration engine via a 102-bit bus comprising six signed 13-bit error data for each MDAC in the forward direction plus six 3-bit coarse capacitor address data (equivalent to m_x') from each sub-ADC in the reverse direction. The coarse capacitor address data tells the calibration engine which coarse capacitors it is currently using and the engine puts the required 14-bit error word on the relevant MDAC's data bus. Each *logic* block will thus require a 14-bit adder, which may be implemented using a simple lookup table since 3 bit MSB output data is being added to a 14-bit error with most of the error being in the LSB portion of the 14-bit word.

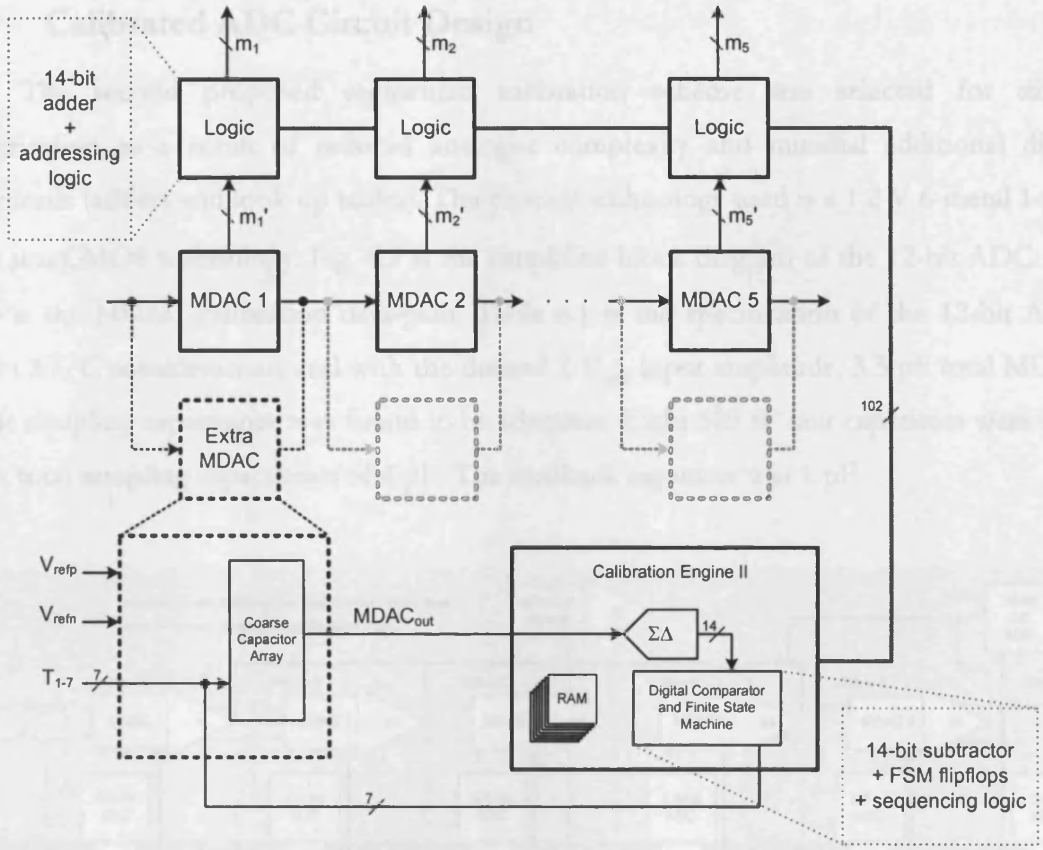

Fig. 6.7 Proposed segmented calibration architecture II.

Equation (6.4) then becomes

$$D_{OUT} = (\varepsilon_k + D_k)\cdot r_1^{(n/m)-1} + (\varepsilon_{k-1} + D_{k-1})\cdot r_2^{(n/m)-2} + \cdots + (\varepsilon_2 + D_2)\cdot r_k + D_1 \qquad (6.11)$$

where ε is the regenerated errors in the digital domain truncated to *n*-bits. The area and power overheads are similar to the previous calibration scheme with less complexity in the analogue implementation. Fig. 6.8 shows the calibration flowchart for a single MDAC.

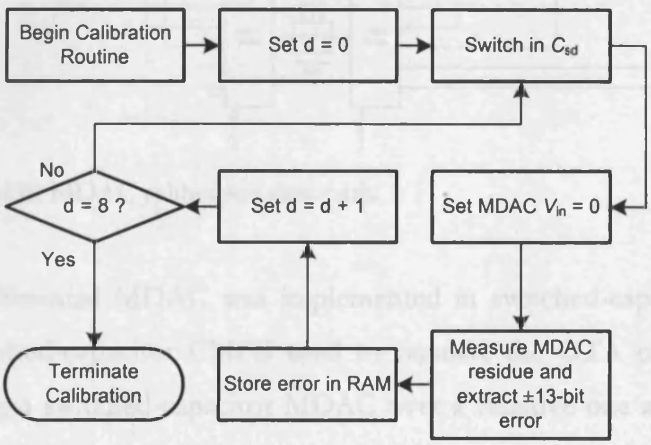

Fig. 6.8 MDAC calibration procedure flowchart.

6.5 Calibrated ADC Circuit Design

The second proposed segmented calibration scheme was selected for silicon qualification as a result of reduced analogue complexity and minimal additional digital overheads (adders and look-up tables). The process technology used is a 1.2 V 6-metal 1-poly 0.13 μm CMOS technology. Fig. 6.9 is the simplified block diagram of the 12-bit ADC. Fig. 6.10 is the MDAC calibration data-path. Table 6.1 is the specification of the 12-bit ADC. From kT/C considerations and with the desired 2 V_{ppd} input amplitude, 3.3 pF total MDAC input sampling capacitance was found to be adequate. Eight 500 fF unit capacitors were used for a total sampling capacitance of 4 pF. The feedback capacitor was 1 pF.

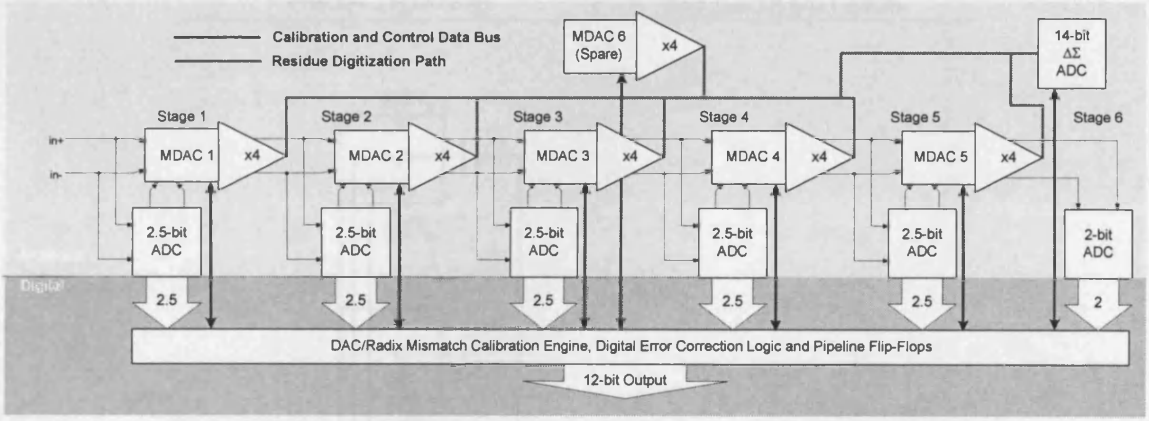

Fig. 6.9 12-bit 2.5-bit-per-stage ADC block diagram.

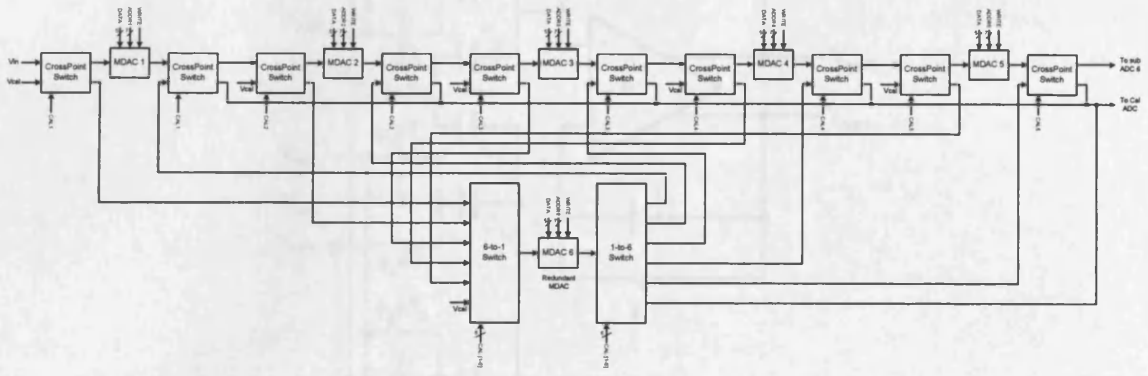

Fig. 6.10 12-bit ADC MDAC calibration data-path.

Each fully differential MDAC was implemented in switched-capacitors as shown in Fig. 6.11 with switched-capacitor CMFB used to regulate the OTA output voltages. The motivation for using a switched-capacitor MDAC over a resistive one as used in Chapter 4 was that the switched-capacitor MDAC was more amenable to unit device (capacitor) calibration implementation. In addition, the matching of capacitors is better than that of

resistors (as shown in Chapter 3) by an order of magnitude. The dynamic comparator topology used in Chapter 4 was used for the sub-ADCs.

Table 6.1 Calibrated 12-bit pipeline ADC specifications

Parameters	Specification
SNR (dB)	> 70
SFDR (dB)	> 75
DNL (LSB)	± 0.5
INL (LSB)	± 1
Sampling Rate (MHz)	120
Power Consumption (mW)	< 120
Input Amplitude (V_{ppd})	2
Supply Voltage (V)	1.2
Silicon Area (mm^2)	< 1
Process Technology	0.13 μm 1P 6M CMOS

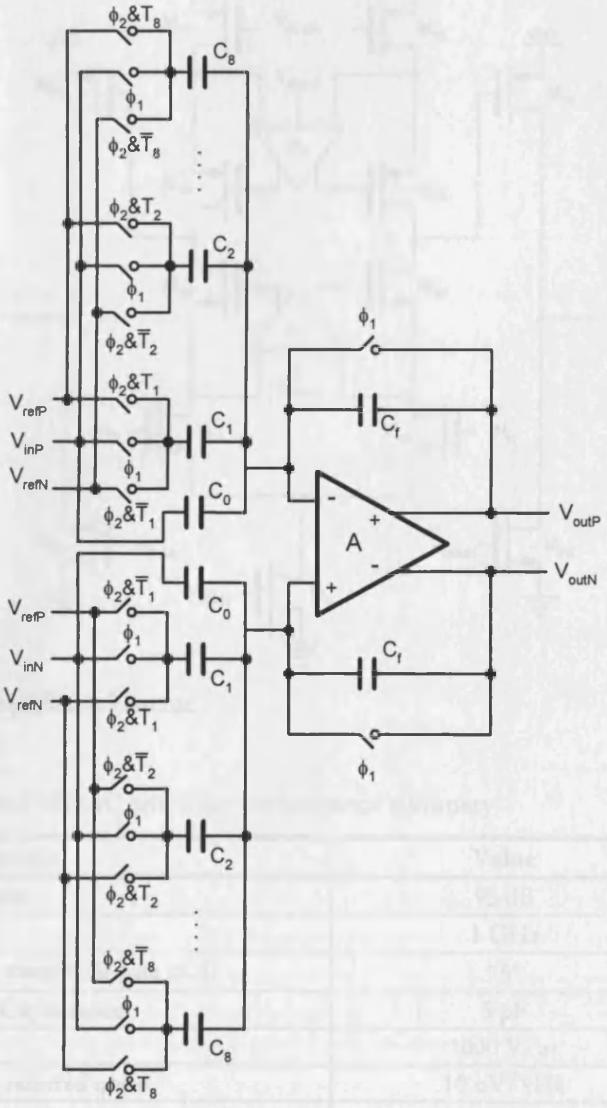

Fig. 6.11 Calibrated MDAC schematic.

All MDAC switches were implemented using exotic low-threshold voltage pMOS and nMOS devices available in the process technology, hence no need for clock boosting or switch bootstrapping. The optimal four-phase clocking scheme [84], [190] was also used. The MDAC amplifiers were 2-stage cascode-compensated topology with cascoded gain-boosted first-stage. This topology was found to be suitable from a dc gain, gain bandwidth and output swing point of view and from the observation that the amplifier input will never see the full ADC amplitude (i.e. only the maximum residue, or $V_{ref}/4$ will ever appear at the amplifier inputs since it is used in a radix = 4 MDAC). Fig. 6.12 is the MDAC amplifier schematic. The auxiliary amplifiers A_1 and A_2 are implemented using folded cascode OTAs as in Chapter 4.

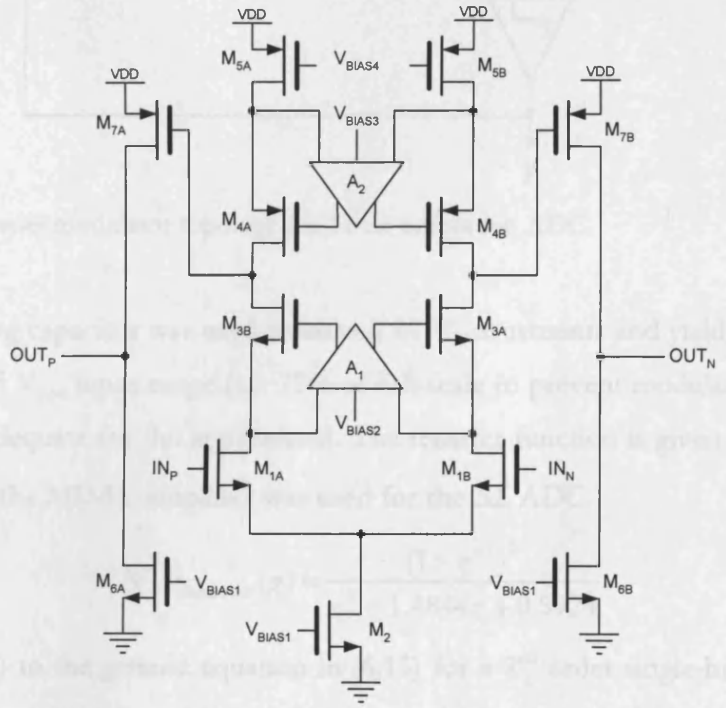

Fig. 6.12 MDAC amplifier schematic.

Table 6.2 Simulated MDAC amplifier performance summary.

Parameter	Value
DC gain	95 dB
GBW	1 GHz
Phase margin (at gain of 4)	75°
Load Capacitance	5 pF
SR	1000 V/μs
Input-referred noise	10 nV/√Hz
4.1 ns settling error (gain of 4)	-83 dB
Supply voltage	1.2 V
Power consumption	15 mW

Table 6.2 above is the MDAC amplifier performance summary with higher than 90dB dc gain required for the application. A 2nd order switched-capacitor 2.4 MS/s ΔΣ ADC was then designed with OSR = 512, a Butterworth NTF and out-of-band gain of 1.3. Fig. 6.13 is the modulator topology.

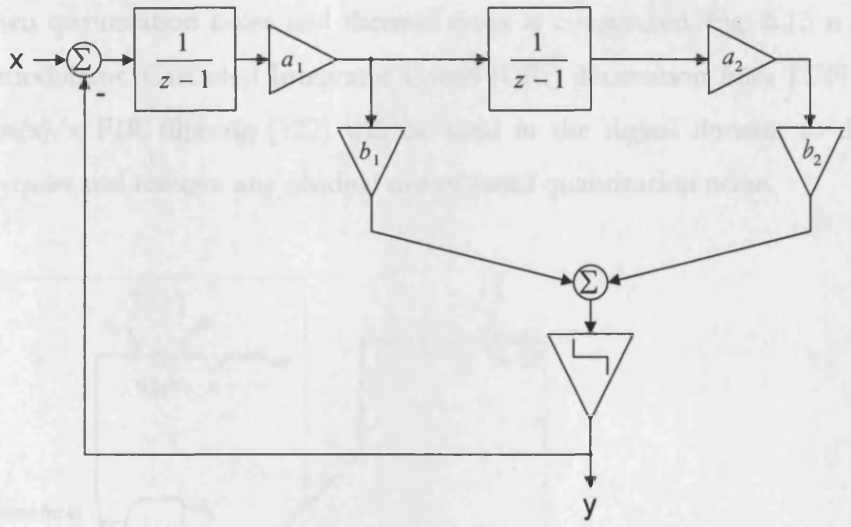

Fig. 6.13 2nd order modulator topology for 14-bit calibration ADC.

A 0.8 pF sampling capacitor was used to exceed kT/C constraints and yield the desired > 84 dB SNR for a 1.5 V_{ppd} input range (i.e. 75% of full-scale to prevent modulator instability but still more than adequate for the application). The transfer function is given below. A scaled-down version of the MDAC amplifier was used for the ΔΣ ADC.

$$NTF_{Butterworth}(z) = \frac{(1-z^{-1})^2}{z^2 - 1.4844z + 0.5924} \tag{6.12}$$

Comparing (6.12) to the generic equation in (6.13) for a 2nd order single-bit topology yields the desired and quantized modulator coefficients in Table 6.3 and Table 6.4 respectively.

$$NTF(z) = \frac{1}{1+L_1(z)} = \frac{(z-1)^2}{(z-1)^2 + a_1 b_1 (z-1)^1 + a_1 a_2 b_2} \tag{6.13}$$

Table 6.3 Modulator loop filter coefficients for 2nd order Butterworth NTF.

I	1	2
a_i	0.5156	0.2095
b_i	1	1

Table 6.4 Quantized modulator loop filter coefficients for 2nd order Butterworth NTF.

I	1	2
a_i	1/2	1/5
b_i	1	1

Fig. 6.14 is the schematic of the 2nd order calibration ΔΣ modulator with approx. 98 dB SNR achieved when quantization noise and thermal noise is considered. Fig. 6.15 is the spectral plot of the modulator. Cascaded Integrator Comb (CIC) decimation filter [220] and further half-band sin(x)/x FIR filtering [122] will be used in the digital domain to decimate the output to Nyquist and remove any residual out-of-band quantization noise.

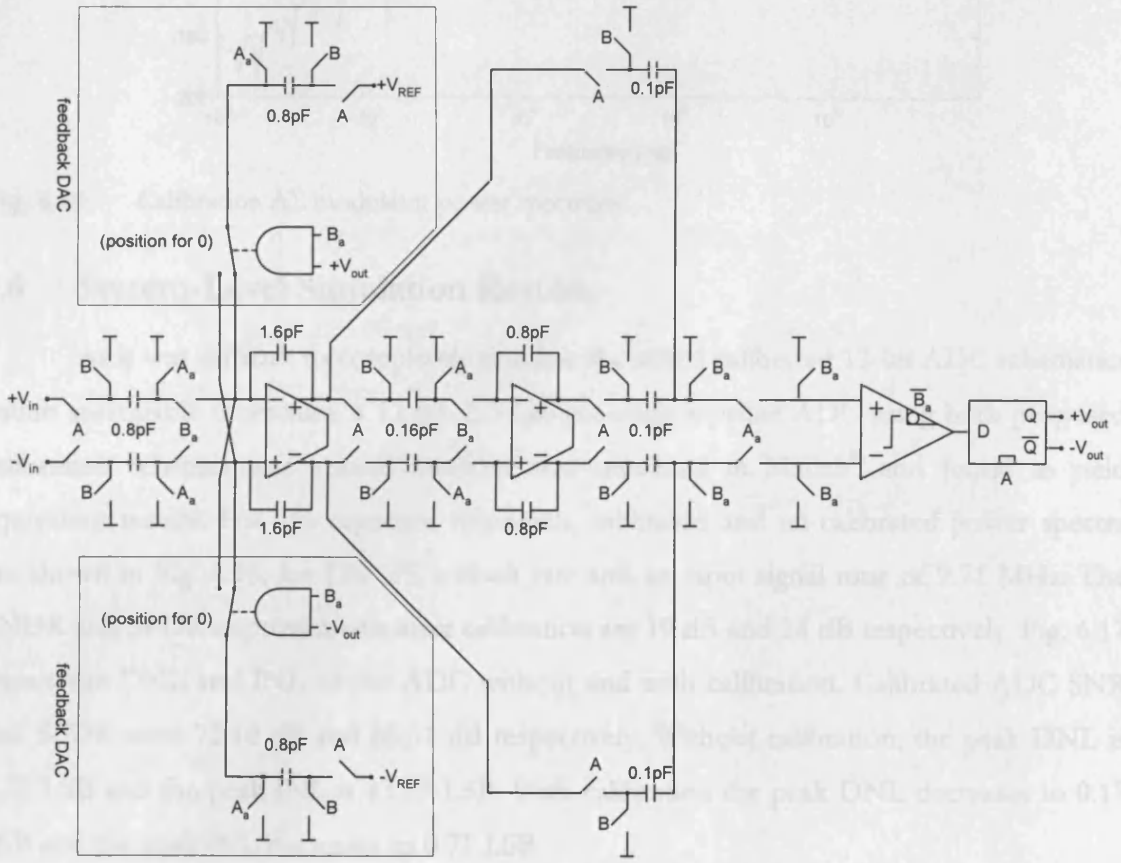

Fig. 6.14 Calibration ΔΣ modulator schematic.

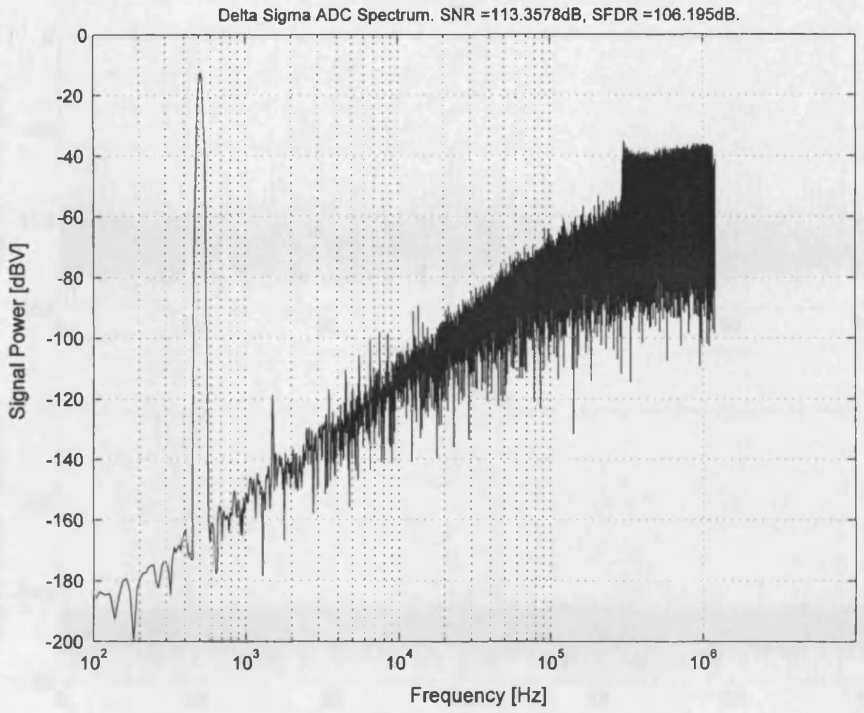

Fig. 6.15 Calibration ΔΣ modulator power spectrum.

6.6 System-Level Simulation Results

As it was difficult to completely simulate the actual calibrated 12-bit ADC schematics within reasonable timescales, a 12-bit, 2.5-bits-per-stage pipeline ADC using both proposed calibration schemes was instead modeled and simulated in Matlab® and found to yield equivalent results. For 1% capacitor mismatch, calibrated and un-calibrated power spectra are shown in Fig. 6.16, for 120 MS/s clock rate and an input signal tone of 9.71 MHz. The SNDR and SFDR improvements after calibration are 19 dB and 24 dB respectively. Fig. 6.17 shows the DNL and INL of the ADC without and with calibration. Calibrated ADC SNR and SFDR were 72.10 dB and 85.51 dB respectively. Without calibration, the peak DNL is 1.22 LSB and the peak INL is 13.29 LSB. With calibration the peak DNL decreases to 0.17 LSB and the peak INL decreases to 0.71 LSB.

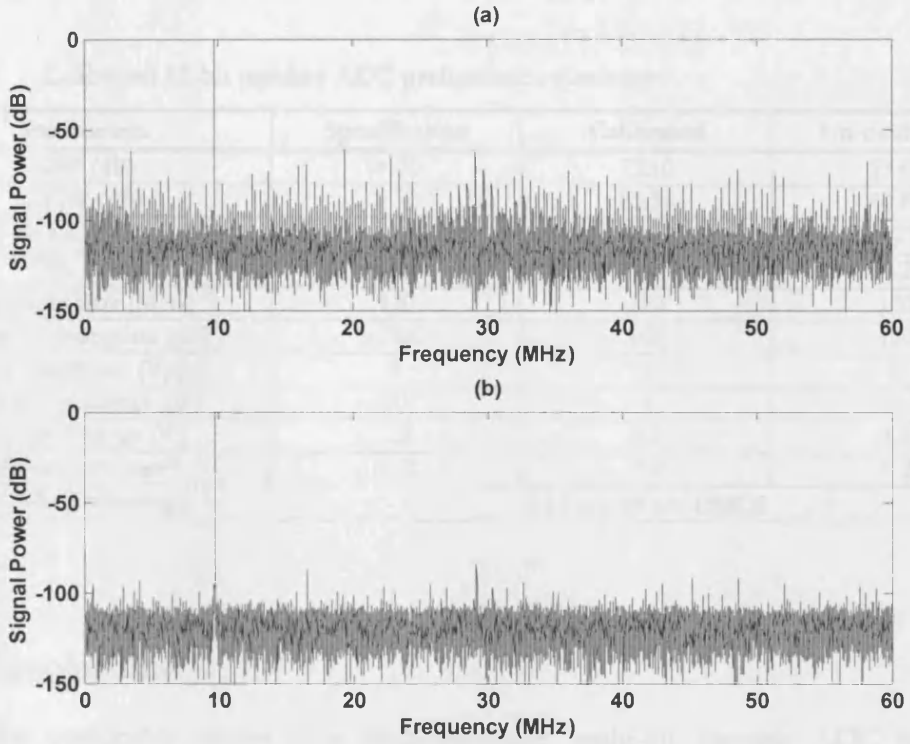

Fig. 6.16 ADC output spectra (a) without and (b) with calibration.

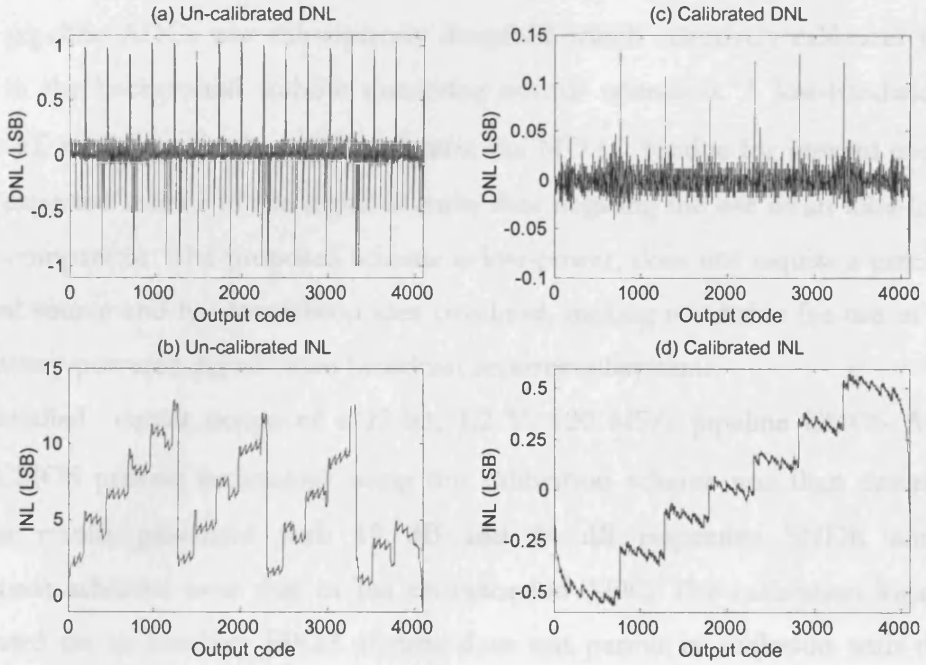

Fig. 6.17 (a) DNL, (b) INL without calibration, (c) DNL, (d) INL with calibration.

Table 6.5 below is the simulated results of the calibrated 12-bit 120MS/s ADC contrasted with the desired specification. The simulated power consumption was estimated by summing the consumption of individual simulated blocks with some margin added for logic overhead since the complete circuits was not simulated.

Table 6.5 Calibrated 12-bit pipeline ADC performance summary.

Parameters	Specification	Calibrated	Un-calibrated
SNR (dB)	> 70	72.10	53.62
SFDR (dB)	> 75	85.51	60.87
DNL (LSB)	± 0.5	0.17	1.22
INL (LSB)	± 1	0.71	13.29
Sampling Rate (MHz)	120	120	120
Power Consumption (mW)	< 120	100	100
Input Amplitude (Vppd)	2	2	2
Input Capacitance (pF)	4	4	4
Supply Voltage (V)	1.2	1.2	1.2
Silicon Area (mm^2)	< 2	< 2	< 2
Process Technology	0.13 μm 1P 6M CMOS		

6.6 Conclusions

The correctible errors in a high-resolution multi-bit pipeline ADC have been showcased. A review was then done on current calibration methods in the literature and their limitations highlighted. A novel segmented analogue background calibration scheme for multi-bit pipeline ADCs was subsequently described which selectively calibrates the ADC MDACs in the background without disrupting normal operation. A low-bandwidth high-precision ΔΣ modulator is also used to digitize the MDAC residue for onward comparison with the expected residue in the digital domain thus negating the use of an ultra-low offset analogue comparator. The proposed scheme is low-power, does not require a precision on-chip signal source and has low silicon area overhead, making it suitable for use in low-cost mobile battery-powered digital video broadcast receiver subsystems.

Detailed circuit design of a 12-bit, 1.2 V, 120 MS/s pipeline CMOS ADC in a 0.13μm CMOS process technology using this calibration scheme was then described and simulation results presented with 19 dB and 24 dB respective SNDR and SFDR improvement achieved over that of the un-calibrated ADC. The calibration logic will be implemented on an auxiliary FPGA if time does not permit its inclusion with the ADC fabrication silicon. Layout design is currently underway and a fabrication run planned for November 2006.

7 Conclusions

"Let us hear the conclusion of the whole matter ..." Ecc.12:13 KJV

With the continued drive towards miniaturization of consumer personal communication devices and with the extreme complexity of such devices as they handle increasing levels of voice, video and data whilst being powered by a rechargeable battery, lower power sub-system design and optimal partitioning between the analogue and digital parts of the system is a key requirements. This work has focused on the optimization of power consumption of one of those key sub-systems, namely the analogue to digital converter with the key contributions to knowledge being:

- The determination of optimal inter-stage resolution partitioning for lowest power dissipation in moderate resolution pipeline ADCs. This enabled the design and fabrication of a video-rate low-power reduced-voltage ADC with the lowest reported measured energy efficiency to date.
- The optimal partitioning of wireless communication receiver baseband with most of the baseband processing pushed into the digital domain to relieve the complexity of the analogue baseband and eliminate the need for post-production trimming or calibration. Since the key to the digitally slanted partitioning is the ΔΣ ADC which now needs significantly higher dynamic range, this motivated the development of a novel switch linearization circuit for the switched capacitor ΔΣ ADC sampling switch. This linearisation circuit allowed for over 12 dB improvement in measured ADC dynamic range in comparison with ADC sampling switch implementation using prior art (transmission gates) and was successfully verified in silicon for both a GSM and WCDMA ΔΣ ADC design.
- The development of novel power efficient calibration schemes for Nyquist-rate pipeline ADCs since video-rate and higher-bandwidth battery-powered receivers on the other hand are difficult to implement using the ΔΣ ADC architecture even for very low over-sampling ratios. They are better implemented using the pipeline ADC architecture with the issue being that some form of calibration is required for higher than 10-bit resolution. Two equivalent low-power background calibration schemes for high-speed high-resolution pipeline ADCs and suitable for implementation in battery-powered mobile devices were then proposed and verified at the system level using Matlab®. Circuit and layout design of a 12-bit ADC was then done to

demonstrate the second reduced analogue complexity calibration scheme with the layout design currently underway and silicon fabrication run planned for November 2006.

Future work in the quest for the minimization of power consumption in high-performance, high-resolution, moderate-to-high-bandwidth ADCs will still continue with the following areas identified for further research:

- Power–efficient calibration schemes for pipeline ADCs
- Ultra-low distortion ADC sampling switch architecture and linearization schemes
- Power-efficient slewing-invariant high-dynamic range OTA topologies for low-power switched capacitor ADC design
- Power-efficient DSP algorithms for correcting impairments erstwhile associated with zero-IF receivers
- The design of low-power high dynamic range continuous time $\Delta\Sigma$ modulator silicon for WCDMA frequencies using clock jitter minimization schemes
- Extension of the pipeline ADC inter-stage resolution optimization routine to cover all process technologies and any n-bit ADC
- Development of power-efficient pipeline ADC calibration schemes that will also address amplifier gain error and thus allow the use of lower-power imprecise amplifiers in the MDACs
- Development of $\Delta\Sigma$ modulator structures that minimize out-of-band tones caused by the interaction between the sampling clock and static signals

Finally, as research on low-power ADC design techniques intensify and efficient low-power low-overhead DSP algorithms are developed to help relax analogue sub-system design complexity and calibrate out analogue component mismatch, it will not be too long before the low-power; reconfigurable software radio nirvana is ultimately reached.

Appendix A ΔΣ Modulation Overview

This overview is abstracted from material already in the literature [122], [145]-[188] and is included as an appendix in the thesis for completeness.

A.1 Continuous-time vs. Discrete-time ΔΣ Modulators

The pioneering ΔΣ ADCs [146] employed only continuous-time loop filters, but with the development of the switched capacitor design methodology in 1977 [150]-[151], most published and commercial ΔΣ ADC designs have been discrete-time switched capacitor implementations. The following table compares and contrasts the two implementation schemes.

Table A.1 Continuous-time vs. Discrete-time ΔΣ modulators

ΔΣ Modulator Scheme	Merits	Demerits
Continuous-time ΔΣ Modulators (Resistor-Capacitor)	Lower bandwidth OTAs required because there is no settling constraints	Loop Filter is sensitive to process variation and tied to a fixed clock frequency
	Loop Filter acts as an implicit anti-alias filter	Calibration may be required for Loop Filter
		Susceptible to clock jitter
	Sampling switch need not be linear as it is inside the loop	Inferior accuracy and linearity
Discrete-time ΔΣ Modulators (Switched Capacitor)	Loop Filter is insensitive to process variation and scales with clock frequency	Moderate bandwidth OTAs required as a result of settling constraints
	Calibration is not required for Loop Filter	Explicit continuous-time anti-alias filter required
	Less susceptible to clock jitter	
	Superior accuracy and linearity	Sampling switch needs to be linear as it is outside the loop

In spite of the lower linearity and accuracy issues with continuous-time designs, they are becoming increasingly popular as a result of their lower power consumption at reasonably high sampling rates in comparison with an equivalent switched-capacitor design [152]. But for extremely high linearity relatively low bandwidth applications, the switched capacitor ΔΣ ADC is still king [153] - [154].

A.2 First-order ΔΣ Modulator

Fig. A.1 is the z-domain diagram of a 1st-order ΔΣ modulator with the quantizer (sub-ADC) represented by an additive noise linear model to simplify the analysis. $U(z)$ is the

discretized analogue input signal, $X(z)$ the modulated signal and $Y(z)$ the quantized digital modulated output.

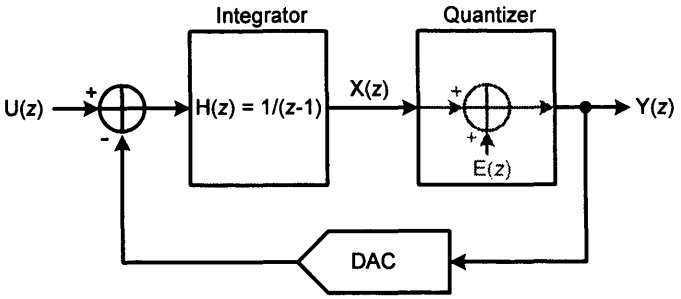

Fig. A.1 First-order ΔΣ modulator.

Simple analysis of the above modulator yields the following equations:

$$Y(z) = X(z) + E(z) \tag{A.1}$$

$$X(z) = \frac{1}{z-1} \cdot [U(z) - Y(z)] \tag{A.2}$$

Combining (A.1) and (A.2) gives:

$$Y(z) - E(z) = \frac{1}{z-1} \cdot [U(z) - Y(z)] \tag{A.3}$$

Manipulating (A.3) slightly yields:

$$Y(z) \cdot (z-1) - E(z) \cdot (z-1) + Y(z) = U(z) \tag{A.4}$$

and

$$Y(z) \cdot z = U(z) + (z-1) \cdot E(z) \tag{A.5}$$

Finally, (A.5) becomes:

$$Y(z) = z^{-1} \cdot U(z) + (1 - z^{-1}) \cdot E(z) \tag{A.6}$$

It can thus be seen that the modulator output is an addition of a delayed version of the original input and the first-order high-pass filtered quantization error $E(z)$. Applying the superposition theorem to (A.6) yields the first-order modulator's signal transfer function (STF) and noise transfer function (NTF) viz.

$$\mathrm{STF}(z) = \frac{Y(z)}{U(z)} = z^{-1} \tag{A.7}$$

$$\mathrm{NTF}(z) = \frac{Y(z)}{E(z)} = (1 - z^{-1}) \tag{A.8}$$

If z is replaced by its sampled frequency domain equivalent $e^{j\omega}$, where ω (angular frequency) is $2 \cdot \pi \cdot f/f_s$, the NTF becomes:

$$\mathrm{NTF}(f) = (1 - e^{-j2\pi\frac{f}{f_s}}) = \frac{e^{j\pi\frac{f}{f_s}} - e^{-j\pi\frac{f}{f_s}}}{2j} \cdot 2j \cdot e^{-j\pi\frac{f}{f_s}} = \sin\left(\frac{\pi f}{f_s}\right) \cdot 2j \cdot e^{-j\pi\frac{f}{f_s}} \tag{A.9}$$

with the magnitude of the NTF being the high-pass function:

$$|\mathrm{NTF}(f)| = 2\sin\left(\frac{\pi f}{f_s}\right) \tag{A.10}$$

In Chapter 2, it was established that the quantization noise voltage of a quantizer or ADC of finite resolution was exactly $\Delta/\sqrt{12}$ (noise power of $\Delta^2/12$), where Δ is the step size or LSB. The power spectral density of the NTF is thus given by:

$$S_Q(f) = \frac{1}{f_s} \cdot \frac{\Delta^2}{12} |\mathrm{NTF(f)}|^2 = \frac{1}{f_s} \cdot \frac{\Delta^2}{12} \cdot 4 \cdot \sin^2\left(\frac{\pi f}{f_s}\right) \tag{A.11}$$

Integrating the quantization noise power over the wanted band (assuming $f_s >> f$ or OSR = $f_s/2 \cdot f >> 1$ and that $\sin(1/\mathrm{OSR}) \cong 1/\mathrm{OSR}$) gives the in-band noise power, i.e.

$$P_E = \int_0^f S_Q(f)df = \int_0^f \frac{1}{f_s} \cdot \frac{\Delta^2}{12} \cdot \left[\frac{2\pi f}{f_s}\right]^2 df = \frac{\Delta^2\pi^2}{36} \cdot \left[\frac{1}{OSR}\right]^3 \tag{A.12}$$

It can thus be seen that doubling the OSR of a 1st-order modulator will increase the SNR by $10 \cdot \log_{10} 2^3$ or 9 dB. If no noise shaping was used, the SNR increase will have been only $10 \cdot \log_{10} 2$ or 3 dB.

A.3 Second-order ΔΣ Modulator

If an additional integrator is added to the loop filter of Fig. A.1, a 2nd-order ΔΣ modulator is realized (Fig. A.2).

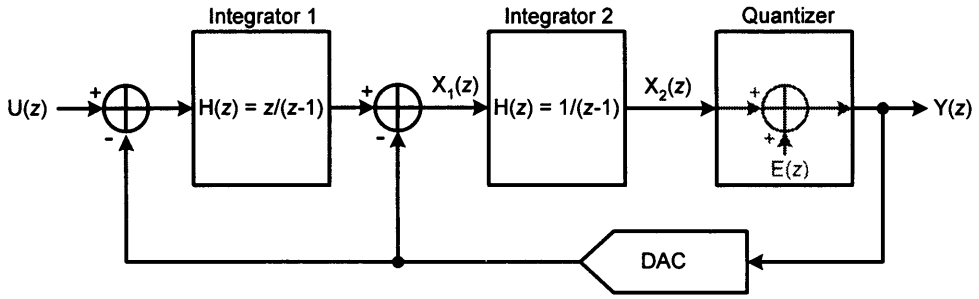

Fig. A.2 Second-order ΔΣ modulator.

Analyzing the above modulator yields the following equations:

$$Y(z) = X_2(z) + E(z) \tag{A.13}$$

$$X_2(z) = \frac{1}{(z-1)} \cdot X_1(z) \tag{A.14}$$

$$X_1(z) = \frac{z}{(z-1)} \cdot [U_1(z) - Y(z)] - Y(z) \tag{A.15}$$

Combining (A.13), (A.14) and (A.15) gives:

$$Y(z) = \frac{1}{(z-1)} \cdot \left[\frac{z}{(z-1)} \cdot [U(z) - Y(z)] - Y(z) \right] + E(z) \tag{A.16}$$

Rearranging (A.16) slightly yields:

$$Y(z) \cdot (z-1)^2 - E(z) \cdot (z-1)^2 + z \cdot Y(z) + (z-1) \cdot Y(z) = z \cdot U(z) \tag{A.17}$$

and

$$Y(z) \cdot z^2 = z \cdot U(z) + (z-1)^2 \cdot E(z) \tag{A.18}$$

Finally, (A.18) becomes:

$$Y(z) = z^{-1} \cdot U(z) + (1 - z^{-1})^2 \cdot E(z) \tag{A.19}$$

It can thus be seen that the modulator output is an addition of a delayed version of the original input and the second-order high-pass filtered quantization error $E(z)$. Applying the superposition theorem to (A.19) yields the second-order modulator's signal transfer function (STF) and noise transfer function (NTF) viz.

$$\mathrm{STF}(z) = \frac{Y(z)}{U(z)} = z^{-1} \tag{A.20}$$

$$\mathrm{NTF}(z)=\frac{Y(z)}{E(z)}=(1-z^{-1})^2 \tag{A.21}$$

If z is again replaced by its sampled frequency domain equivalent $e^{j\omega}$, where ω (angular frequency) is $2\cdot\pi\cdot f/f_s$, the NTF becomes:

$$\mathrm{NTF}(f)=(1-e^{-j2\pi\frac{f}{f_s}})^2=-\left[\frac{e^{j\pi\frac{f}{f_s}}-e^{-j\pi\frac{f}{f_s}}}{2j}\right]^2\cdot 4\cdot e^{-j2\pi\frac{f}{f_s}}=-\sin^2\left(\frac{\pi f}{f_s}\right)\cdot 4\cdot e^{-j2\pi\frac{f}{f_s}} \tag{A.22}$$

with the magnitude of the NTF being the high-pass function:

$$|\mathrm{NTF}(f)|=4\sin^2\left(\frac{\pi f}{f_s}\right) \tag{A.23}$$

The power spectral density of the NTF is thus given by:

$$S_Q(f)=\frac{1}{f_s}\cdot\frac{\Delta^2}{12}|\mathrm{NTF}(f)|^2=\frac{1}{f_s}\cdot\frac{\Delta^2}{12}\cdot 16\cdot\sin^4\left(\frac{\pi f}{f_s}\right) \tag{A.24}$$

Integrating the quantization noise power over the wanted band (assuming $f_s >> f$ or OSR = $f_s/2\cdot f>>1$) gives the in-band noise power, i.e.

$$P_E=\int_0^f S_Q(f)df=\int_0^f\frac{1}{f_s}\cdot\frac{\Delta^2}{12}\cdot\left[\frac{2\pi f}{f_s}\right]^4 df=\frac{\Delta^2\pi^4}{60}\cdot\left[\frac{1}{OSR}\right]^5 \tag{A.25}$$

It can thus be seen that doubling the OSR of a 2nd-order modulator will increase the SNR by $10\cdot\log_{10}2^5$ or 15 dB, 6 dB more than with the first-order modulator.

A.4 Higher-Order ΔΣ Modulators and Stability Issues

Equation (A.25) can be written in its general form for any L-order loop filter viz.

$$P_E=\frac{\Delta^2\pi^{2\cdot L}}{12\cdot(2\cdot L+1)}\cdot\left[\frac{1}{\mathrm{OSR}}\right]^{(2\cdot L+1)} \tag{A.26}$$

The desired theoretical in-band SQNR (signal-to-quantization noise ratio) obtainable using an n-bit quantizer will then be:

$$\mathrm{SQNR}=10\cdot\log_{10}\left[\frac{\Delta^2\cdot 2^{2n}}{8\cdot P_E}\right]\mathrm{dB} \tag{A.27}$$

Stability issues however, prevent the achievement of the theoretical SQNR of (A.27) for higher-order ($L > 2$) $\Delta\Sigma$ modulators with more than 60 dB SQNR lost for a single-bit 5th-order modulator [155]. This is confirmed ($1 \leq L \leq 5$) from actual time-domain simulations in Matlab® and the results tabled below for a 1-bit quantizer OSR = 128 $\Delta\Sigma$ modulator model.

Table A.2 Theoretical and simulated $\Delta\Sigma$ modulator SQNR for OSR = 128.

Modulator Order (*L*)	**1**	**2**	**3**	**4**	**5**
A. SQNR (dB) from (A.27)	65.83	100.25	133.91	167.20	200.27
B. Modulator model SQNR (dB)	61.00	82.36	98.00	107.00	115.36
Difference between **A** and **B**	4.83	17.89	35.91	60.20	84.91

The primary reason for the theoretical vs. simulation deviation observed in Table A.2 is because the linearized models used to extract the equations only consider the stability of the modulator from a pole-zero perspective and does not consider the fact that the quantizer can get over-loaded under dc and sinusoidal excitation thus becoming extremely non-linear leading to undesirable coloration of the frequency spectrum [155]. An over-loaded quantizer makes the loop filter output to become non-monotonic and increase without bounds thus throwing the modulator to the brink of instability. The work-around for modulators of orders higher than 2 is to constrain the input to bounds within which the modulator is guaranteed stable, erstwhile called its *stable input range.*

Under this condition, the full input range of the modulator will be unavailable for use. This stability issue is more prevalent with single-bit quantizer modulators than with multi-bit modulators because of the indeterminate nature of the transfer function slope of the single-bit case (it could easily tend to zero or infinity depending on the input condition). The type of NTF used will also affect the stability of a $\Delta\Sigma$ modulator with Lee's very useful but neither necessary nor sufficient criterion [157] for binary modulators predicting *apriori* that to guarantee stability, the NTF must not exceed an absolute gain of 1.5 (approximately 3.5 dB).

Root locus diagrams are a more reasoned way to ensure the NTF stability with all zeros and poles ideally located inside the unit circle for stability [158]. Ardalan [159] and Risbo [160] have also respectively proposed Gaussian and non-Gaussian probability density techniques for modeling 1-bit modulators which gives theoretical results closely matching simulation. A sufficient but unnecessary criterion for stability of multi-bit quantizer modulators is given in [155] stating that the n-bit quantizer modulator is guaranteed stable if

the maximum input does not exceed $2^n + 2 - |h|$ where $|h|$ is the absolute integral to ∞ of the NTF inverse z-transform.

It can thus be seen that to benefit from the full input range and the unconditional stability of a 2nd-order structure, topological changes will be required. One very popular topology satisfying this requirement is the cascaded $\Delta\Sigma$ modulator.

A.5 Cascaded $\Delta\Sigma$ Modulators

To enjoy the robust stability of 2nd-order modulators at higher orders, a cascade of 2nd-order structures is commonly done with numerous publications on the subject [161]-[172], the drawback being increased sensitivity to circuit imperfection [171]. This strategy relies on the cancellation rather than filtering of the quantization noise and some of the structures are outlined below.

A.5.1 Leslie-Singh Cascade Structure

This structure was proposed by Leslie and Singh [172] and is depicted in Fig. A.3.

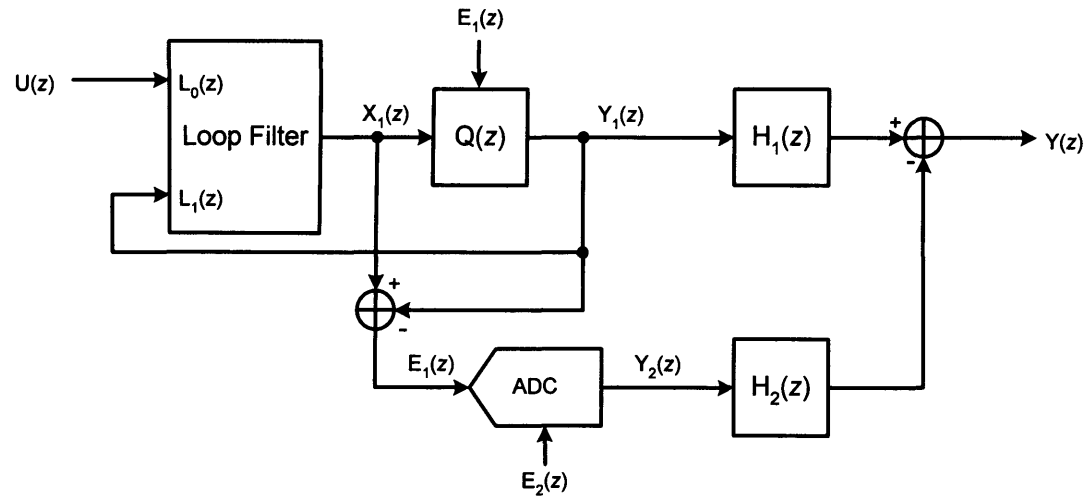

Fig. A.3 Leslie-Singh cascade structure.

It comprises an L order $\Delta\Sigma$ modulator as its first stage and a zero-order ADC as its second stage. The quantization noise $E_1(z)$ is extracted in discrete-time analogue form by subtracting $Y_1(z)$ from $X_1(z)$ and subsequently digitized using a multi-bit ADC, the modulator's second stage. This ADC adds a smaller quantization noise, $E_2(z)$ to $E_1(z)$ to produce $Y_2(z)$ which is then subtracted from $Y_1(z)$ after digital filtering to give the desired output $Y(z)$. Usually, $H_1(z) = z^{-k}$ (k is a unit integer) and $H_2(z)$ is the digital equivalent of the NTF of the first stage. After some analysis [155], the output $Y(z)$ is given by:

$$Y(z) = \frac{z^{-k} \cdot STF_1(z)}{1 - NTF_1(z)} \cdot U(z) + \frac{z^{-1} \cdot NTF_1(z)}{1 - NTF_1(z)} \cdot E(z) \tag{A.28}$$

where

$$\mathrm{STF(z)} = \frac{Y_1(z)}{U(z)} = \frac{L_0(z)}{1 + L_1(z)} \tag{A.29}$$

$$\mathrm{NTF(z)} = \frac{Y(z)}{E(z)} = \frac{1}{1 + L_1(z)} \tag{A.30}$$

Up to 25-30 dB SQNR improvement is obtainable using this structure [155].

A.5.2 Multi-Stage Noise Shaping (MASH) Cascade Structure

In this case [173] – [175], the ADC in Fig. A.3 is replaced with another ΔΣ modulator with the two modulator outputs filtered digitally and subtracted to give the desired output (Fig. A.4).

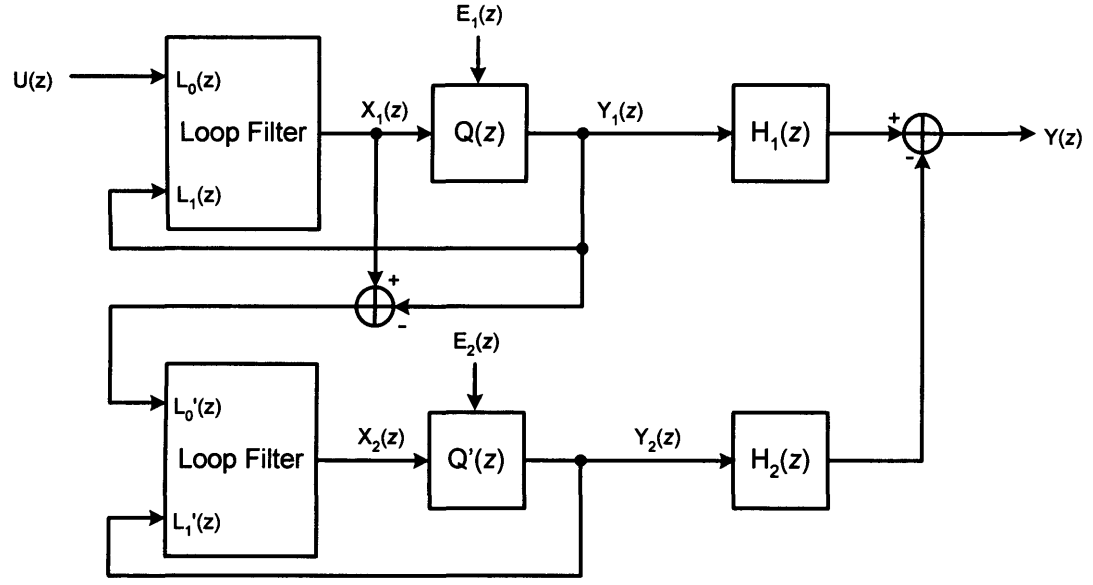

Fig. A.4 MASH cascade structure.

The digital filters are designed in such a way as to allow the complete cancellation of $E_1(z)$ by subtraction. The output of the first stage is given by

$$X_1(z) = STF_1(z) \cdot U(z) + NTF_1(z) \cdot E_1(z) \tag{A.31}$$

The discrete-time analogue quantization noise $E_1(z)$ is now extracted and fed as input into the second modulator with its output given by

$$X_2(z) = STF_2(z) \cdot E_1(z) + NTF_2(z) \cdot E_2(z) \tag{A.32}$$

Hence, $E_1(z)$ will cancel if and $H_2(z)$ are designed such that

$$H_1(z) \cdot \mathrm{NTF}_1(z) - H_2(z) \cdot STF_2(z) = 0 \tag{A.33}$$

This holds if $H_1(z)$ = $\mathrm{STF}_2(z)$ and $H_2(z)$ = $\mathrm{NTF}_1(z)$ and yields for cascade 2nd-order modulators:

$$\mathrm{Y(z)} = z^{-4} \cdot U(z) - (1 - z^{-1})^4 \cdot E_2(z) \tag{A.34}$$

The noise shaping of a 4th order single-loop modulator is thus obtained while the stability is that of a 2nd-order modulator.

A.6 ΔΣ Modulator Loop Filter Architectures

There are a number of commonly used loop filter architectures and the basic ones are described here.

A.6.1 Loop Filter with Distributed Feed-forward and Feedback Paths

This is depicted in Fig. A.5 and consists of cascaded integrators with inputs fed forward and output fed back.

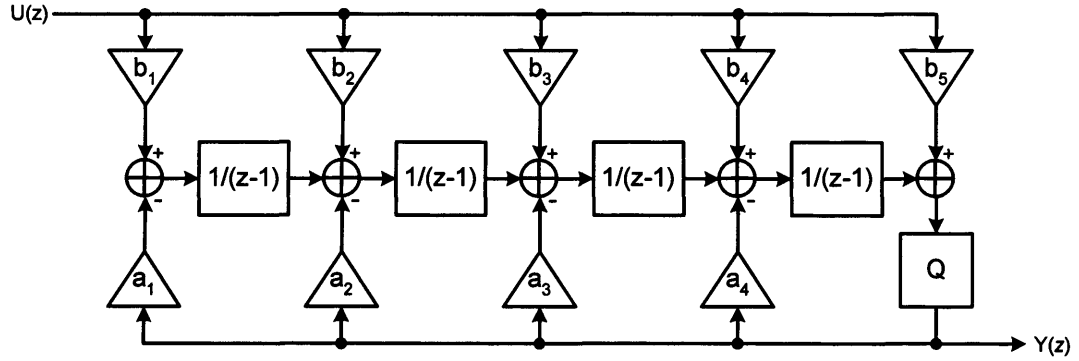

Fig. A.5 4th-order loop filter with distributed feed-forward and feedback paths.

The signal filter transfer function L_0 is given by

$$L_0(z) = \sum_{i=1}^{N+1} \frac{b_i}{(z-1)^{N+1-i}} = \frac{b_1 + b_2(z-1) + \ldots + b_{N+1}(z-1)^N}{(z-1)^N} \tag{A.35}$$

And the noise filter transfer function L_1 by

$$L_1(z) = \sum_{i=1}^{N+1} \frac{-a_i}{(z-1)^{N+1-i}} = -\frac{a_1 + a_2(z-1) + \ldots + a_N(z-1)^{N-1}}{(z-1)^N} \tag{A.36}$$

yielding

$$\mathrm{NTF}(z)=\frac{1}{1-L_1(z)}=\frac{(z-1)^N}{D(z)} \tag{A.37}$$

$$\mathrm{STF}(z)=\frac{L_0(z)}{1-L_1(z)}=\frac{b_1+b_2(z-1)+\ldots+b_{N+1}(z-1)^N}{D(z)} \tag{A.38}$$

where

$$\mathrm{D}(z)=a_1+a_2(z-1)+\ldots+a_{N-1}(z-1)^{N-1}+a_N(z-1)^N \tag{A.39}$$

All zeros of this structure's NTF lie at dc ($z = 1$).

A.6.2 Loop Filter with Feed-forward, Feedback and Resonator Paths

This is depicted in Fig. A.6 and consists of cascaded integrators with inputs fed forward and output fed back in addition to resonators between every other stage (one of integrators in each resonator loop must be delay-free for the poles to remain on the unit circle.

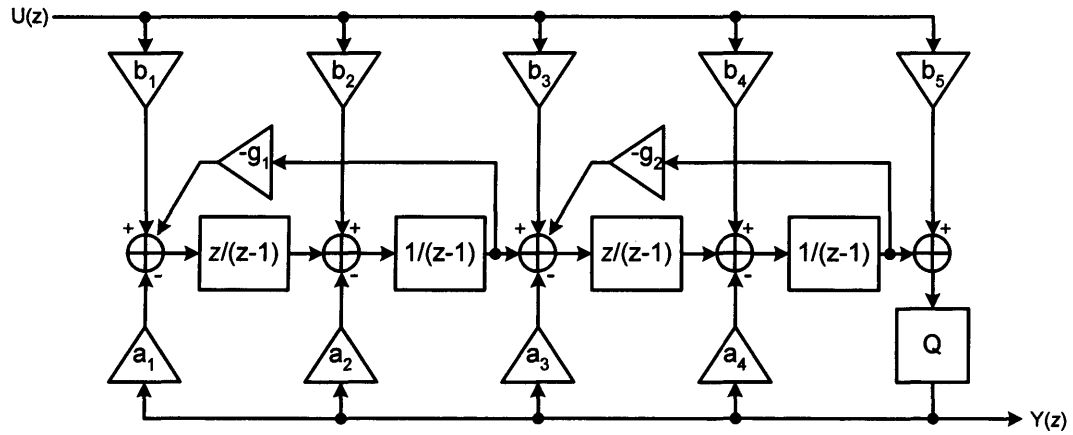

Fig. A.6 4th-order loop filter with feed-forward, feedback and resonator paths.

The signal filter transfer function L_0 is given by

$$L_0(z)=\frac{(b_1z+b_2(z-1))\cdot z+[z^2-(2-g_1)z+1]\cdot(b_3z+b_4(z-1))+b_5}{[z^2-(2-g_1)z+1]\cdot[z^2-(2-g_2)z+1]} \tag{A.40}$$

And the noise filter transfer function L_1 by

$$L_1(z)=\frac{(a_1z+a_2(z-1))\cdot z+[z^2-(2-g_1)z+1]\cdot(a_3z+a_4(z-1))}{[z^2-(2-g_1)z+1]\cdot[z^2-(2-g_2)z+1]} \tag{A.41}$$

A.6.3 Loop Filter with Weighted Feed-forward Summation

This is shown in Fig. A.7 and consists of cascaded integrators with inputs fed forward and summed prior to quantization.

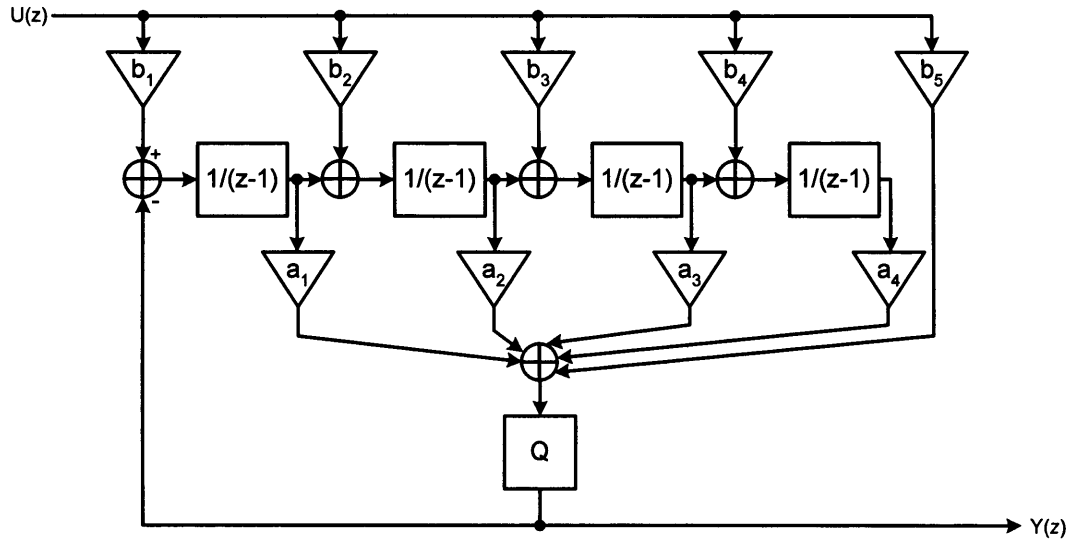

Fig. A.7 4th-order loop filter with weighted feed-forward summation.

The noise filter transfer function L_1 is given by

$$L_1(z) = -a_1 \cdot \frac{1}{(z-1)} - a_2 \cdot \frac{1}{(z-1)^2} + \ldots + a_N \cdot \frac{1}{(z-1)^N} \tag{A.42}$$

And the signal filter transfer function L_0 by

$$L_0(z) = b_1 \cdot \left[\frac{a_1}{(z-1)} + \frac{a_2}{(z-1)^2} + \ldots + \frac{a_N}{(z-1)^N} \right] + b_2 \cdot \left[\frac{a_2}{(z-1)} + \ldots + \frac{a_N}{(z-1)^{N-1}} \right]$$
$$+ b_3 \cdot \left[\frac{a_3}{(z-1)} + \ldots + \frac{a_N}{(z-1)^{N-2}} \right] + \ldots + b_{N-1} \tag{A.43}$$

The zeros at dc can be shifted in order to optimize the NTF by creating resonators using local feedback as in Fig. A.6. The structure in Fig. A.8 below then results.

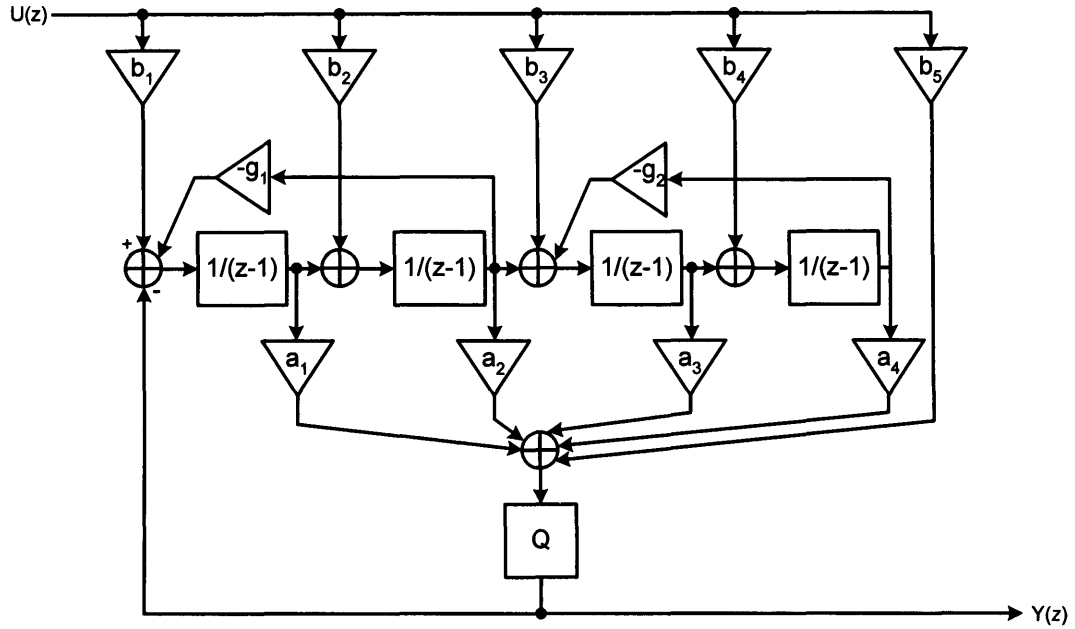

Fig. A.8 4th-order loop filter with weighted feed-forward summation and resonators.

A.7 ΔΣ Modulator Noise Transfer Functions

There are essentially three high-pass NTFs; the pure differentiation NTF (A.44) with zeros at dc ($z = 1$) and infinite poles ($z = 0$), the Butterworth NTF (A.45) with zeros at dc and complex poles and the Inverse Chebyshev NTF (A.46) with complex zeros for optimizing the NTF with up to 34 dB additional SQNR achievable [155] after optimization.

$$\mathrm{NTF}(z) = (1 - z^{-1})^N \tag{A.44}$$

$$\mathrm{NTF}(z) = \frac{(1 - z^{-1})^N}{D(z)} \tag{A.45}$$

$$\mathrm{NTF}(z) = \frac{(1 - g \cdot z^{-1})^N}{D(z)} \tag{A.46}$$

The figures below show the pole/zero positions of the above NTFs and their frequency response. The distributed feed-forward/feedback and weighted feed-forward summation structures yield a Butterworth NTF. The distributed feed-forward/feedback with resonator and weighed feed-forward summation with resonator structures yield an Inverse Chebyshev NTF. Elliptic NTFs have also been used in the literature [157] but are more susceptible to instability for given coefficient perturbation as a result of device impairments.

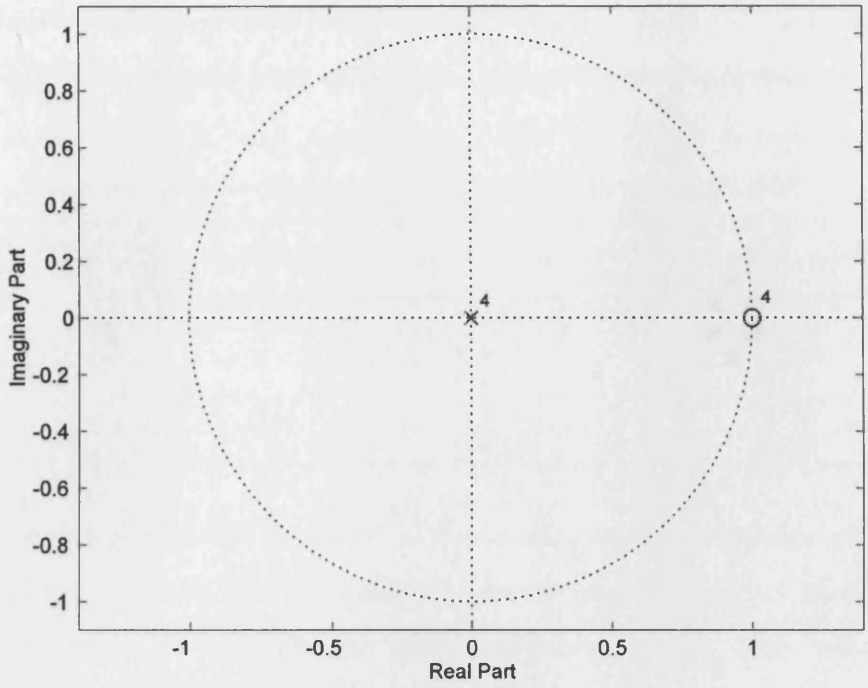

Fig. A.9 Pole-zero plot of a 4th order pure differentiation NTF.

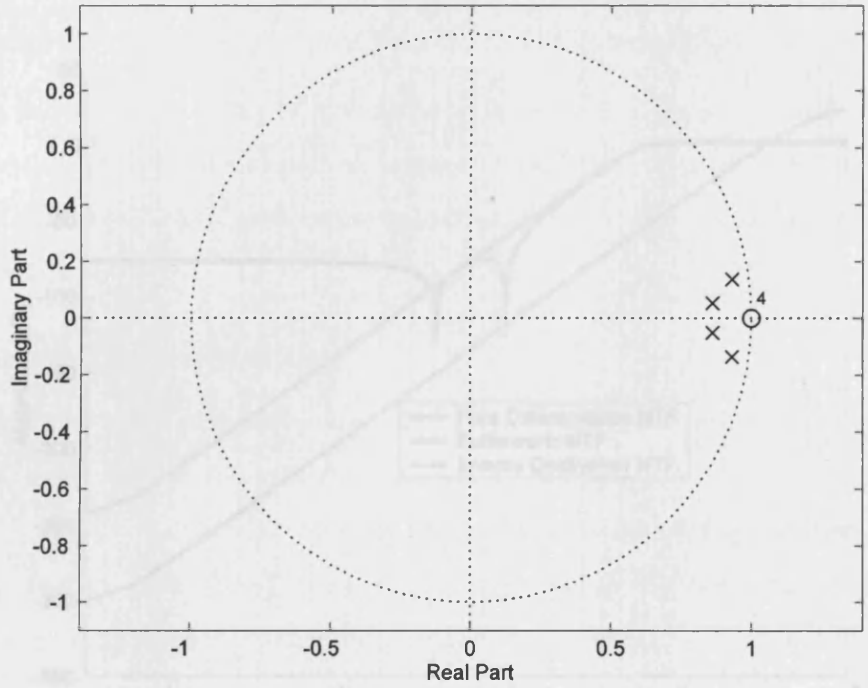

Fig. A.10 Pole-zero plot of a 4th order Butterworth NTF.

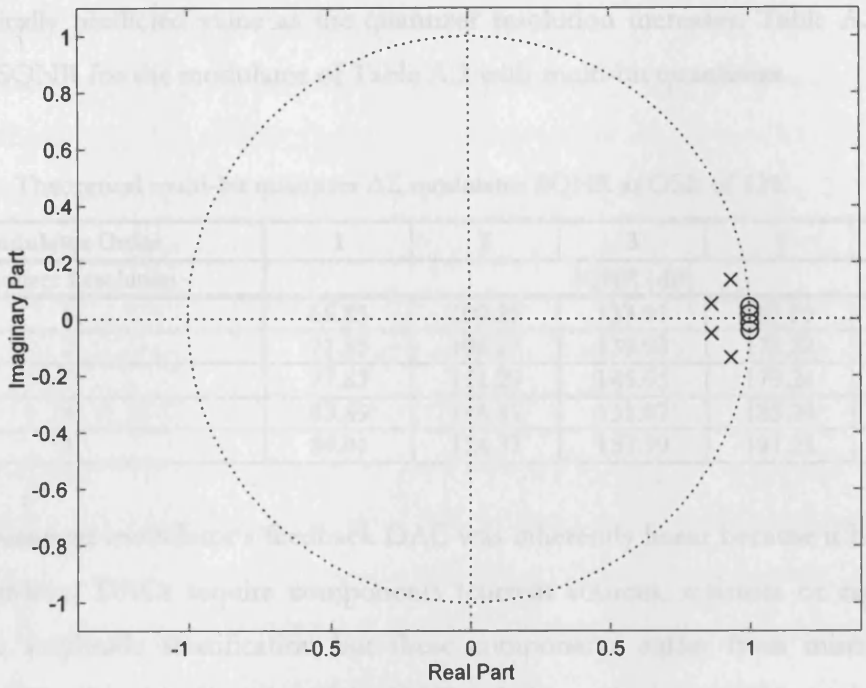

Fig. A.11 Pole-zero plot of a 4th order Inverse Chebyshev NTF.

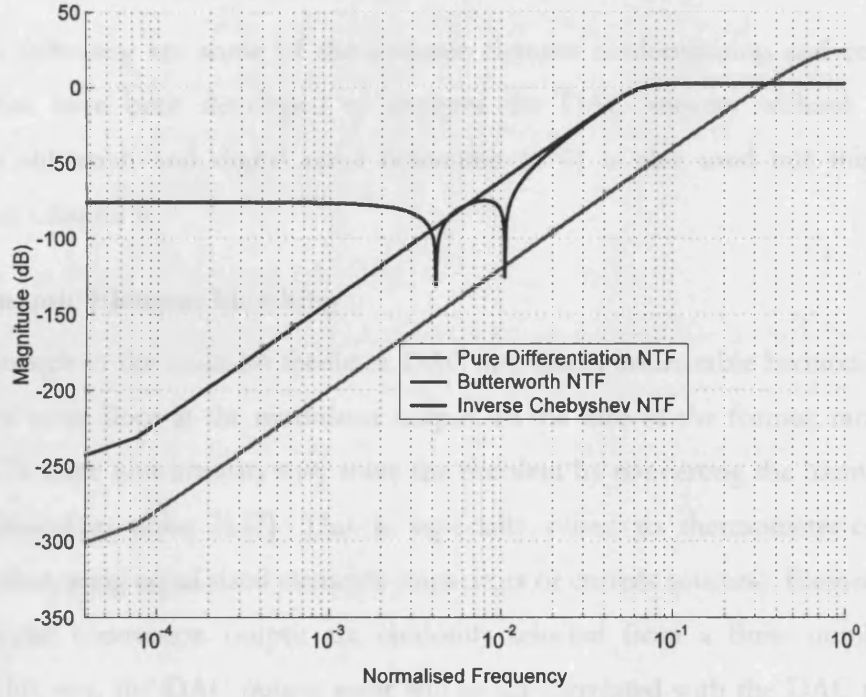

Fig. A.12 Frequency response plots of all three NTFs.

A.8 ΔΣ Modulators with Multi-Bit Quantizers

The employment of multi-bit quantization in ΔΣ modulators yield a 6 dB increase in theoretical SQNR per additional bit and improves overall modulator stability but at the expense of feedback DAC linearity. Overall simulated performance also becomes closer to

the theoretically predicted value as the quantizer resolution increases. Table A.3 gives the theoretical SQNR for the modulator of Table A.2 with multi-bit quantizers.

Table A.3 Theoretical multi-bit quantizer ΔΣ modulator SQNR at OSR of 128.

Modulator Order	1	2	3	4	5
Quantizer Resolution	SQNR (dB)				
1	65.83	100.25	133.91	167.20	200.27
2	71.85	106.27	139.93	173.22	206.29
3	77.87	112.29	145.95	179.24	212.31
4	83.89	118.31	151.97	185.26	218.34
5	89.91	124.33	157.99	191.28	224.36

The 1-bit quantizer modulator's feedback DAC was inherently linear because it had only two levels. Multi-level DACs require components (current sources, resistors or capacitors) to achieve the amplitude stratification but these components suffer from mismatch issues severely compromising the linearity of the DAC and ultimately the multi-bit modulator.

A.9 Correction of ΔΣ Modulator Feedback DAC Imperfections

The following are some of the dynamic element randomization and error shaping methods that have been developed to improve the DAC linearity without component trimming. Calibration and digital error correction [176] is also used but this is further developed in Chapter 6.

A.9.1 Dynamic Element Matching

Device mismatch in the multi-bit feedback DAC introduces undesirable harmonic distortion and elevated noise floor at the modulator output. In the case of the former, randomization of the DAC's static non-linearity may solve the problem by converting the harmonic energy into pseudorandom noise [177]. This is especially suited to thermometer-coded DAC implementation using equal sized elements (capacitors or current sources). Elements required for a particular conversion output are randomly selected from a finite number of unit elements. This way, the DAC output error will be un-correlated with the DAC input and is replaced by random noise.

A.9.2 Mismatch Error Shaping

In this method, the noise shaping property of the ΔΣ modulator is employed in the randomization of the elements. The noise is thus the element mismatch and is shaped out of band. Various methods are employed to achieve mismatch shaping and are described below.

A.9.3 Rotated Data Weighted Averaging

Element rotation [178] or data weighted averaging (DWA) [179] essentially aims to use each unit elements for roughly the same long-term duration, i.e. in a 4-bit DAC with 15 unit elements, elements 1 to 3 will be used for an input code of 3. If the next input code is 9, elements 4 to 12 are used. If subsequently, the input code becomes 5, elements 13, 14, 15, 1 and 2 are then used. All components are thus used sequentially and as frequently as possible and the long-term average of the mismatch error or noise is zero with the noise shaping similar to that of a first-order $\Delta\Sigma$ modulator.

Tonal generation is however a problem with DWA which is addressed using the bi-DWA scheme [180] where the direction of the element rotation is inverted every cycle but with the penalty being a slightly elevated noise floor (9 dB). More recently, an adaptively randomized DWA was proposed [181] that enabled the reduction of in-band tones by more than 10dB whilst maintaining the same noise floor.

A.9.4 Individual Level Averaging

This method [182] also introduces first-order high-pass filtering to the mismatch noise by equalizing the usage of each element for each code over time with the penalty being zero average error convergence latency and a higher noise floor. It is however less likely to generate tones in comparison with legacy DWA.

A.9.5 Vector-Based Mismatch Shaping

This method [183] achieves arbitrarily higher-order mismatch shaping by dedicating a noise shaping loop for each DAC unit element. Significant in-band tonal reduction and spectrally shaped mismatch noise is simultaneously achieved using this method.

A.9.6 Tree Structure Element Selection

This method [184] uses a tree-structured switching blocks or encoder to randomly select the required elements to a first or second order $\Delta\Sigma$ modulator pattern with the resulting in-band residual noise and tones at levels comparable to vector-based mismatch shaping.

Appendix B ΔΣ Modulator Matlab Scripts

The Matlab scripts used for the system-level simulation of the GSM, WCDMA and calibration ΔΣ Modulators are documented in this appendix. The frequencies of input signals used are 4 kHz, 40 kHz and 503 Hz respectively. OSRs are respectively 96, 40 and 512.

B.1 Matlab script for GSM ΔΣ Modulator simulation

```
% Matlab Script to do Systems Simulation of a 4th Order Delta-Sigma ADC
% for GSM Modulator
%Author: Olujide A. Adeniran. 10th July 2006
%
clear all
close all
%********************4th Order GSM Delta-Sigma Code*****************
skew = 1;
% Integrator coefficients
intcoeff1 = skew*0.5;
intcoeff2 = skew*0.25;
intcoeff3 = skew*0.125;
intcoeff4 = skew*0.0625;
feedbcoeff= 0.00625;
ampl = 0.375;
vcm = 1.35;
refp = 1.85;
refn = 0.85;
high = 2.7;
low = 0;
fsample = 26e6; % clock frequency
OSR = 96;
f_signal = 4e3/(fsample/2); % normalized to bandwidth defined by oversampling rate
x=(1:2^18); % Number of data points
x=vcm+ampl*(sin(2*pi*0.5*f_signal*x));
y = zeros(length(x),1); % output data placeholder
%Set 1-bit DAC's initial value to refn
```

```
vd = refn;
%Initialise Integrators to common mode voltages
vint1 = vcm;
vint2 = vcm;
vint3 = vcm;
vint4 = vcm;
% Run modulator for x clock cycles
for i=1:length(x)
%Summing Junction
sum = vcm + (x(i)-vcm) - (vd - vcm) - feedbcoeff*(vint2 - vcm);
%Integrator 1
vint1 = vcm + intcoeff1*(sum - vcm) + (vint1 - vcm);
%Integrator 2
vint2 = vcm + intcoeff2*(vint1 - vcm) + (vint2 - vcm);
%Integrator 3
vint3 = vcm + intcoeff3*(vint2 - vcm) + (vint3 - vcm);
%Integrator 4
vint4 = vcm + intcoeff4*(vint3 - vcm) + (vint4 - vcm);
% Quantizer & D2A
      if ((vcm + (vint1 - vcm) + (vint2 - vcm) + (vint3 - vcm)+ (vint4 - vcm)) > vcm)
            y(i) = high;
            vd = refp;
          else
            y(i) = low;
            vd = refn;
          end
      end
% save results
save('gsmdsadcoutput.dat','y','-ascii');
%************************************************************
```

B.2 Matlab script for WCDMA ΔΣ Modulator simulation

```
% Matlab Script to do Systems Simulation of a 4th Order Delta-Sigma ADC
% for WCDMA Modulator
```

```
%Author: Olujide A. Adeniran. 10th July 2006
%
clear all
close all
%*********************4th Order WCDMA Delta-Sigma Code*****************
skew = 1;
% Integrator coefficients
intcoeff1 = skew*0.5;
intcoeff2 = skew*0.25;
intcoeff3 = skew*0.125;
intcoeff4 = skew*0.0625;
feedbcoeff= 0.035;
ampl = 0.375;
vcm = 1.35;
refp = 1.85;
refn = 0.85;
high = 2.7;
low = 0;
fsample = 153.6e6; % clock frequency
OSR = 40;
f_signal = 40e3/(fsample/2); % normalized to bandwidth defined by oversampling rate
x=(1:2^18); % Number of data points
x=vcm+ampl*(sin(2*pi*0.5*f_signal*x));
y = zeros(length(x),1); % output data placeholder
%Set 1-bit DAC's initial value to refn
vd = refn;
%Initialise Integrators to common mode voltages
vint1 = vcm;
vint2 = vcm;
vint3 = vcm;
vint4 = vcm;
% Run modulator for x clock cycles
for i=1:length(x)
%Summing Junction
```

```
sum = vcm + (x(i)-vcm) - (vd - vcm) - feedbcoeff*(vint2 - vcm);
%Integrator 1
vint1 = vcm + intcoeff1*(sum - vcm) + (vint1 - vcm);
%Integrator 2
vint2 = vcm + intcoeff2*(vint1 - vcm) + (vint2 - vcm);
%Integrator 3
vint3 = vcm + intcoeff3*(vint2 - vcm) + (vint3 - vcm);
%Integrator 4
vint4 = vcm + intcoeff4*(vint3 - vcm) + (vint4 - vcm);
% Quantizer & D2A
        if ((vcm + (vint1 - vcm) + (vint2 - vcm) + (vint3 - vcm)+ (vint4 - vcm)) > vcm)
            y(i) = high;
            vd = refp;
          else
            y(i) = low;
            vd = refn;
          end
    end
% save results
save('wcdmadsadcoutput.dat','y','-ascii');
%*************************************************************
```

B.3 Matlab script for Calibration ΔΣ Modulator simulation

```
% Matlab Script to do Systems Simulation of a 2nd Order Delta-Sigma ADC
% for Calibration ADC Modulator
%Author: Olujide A. Adeniran. 10th July 2006
%
clear all
close all
%*********************2nd Order Calibration Delta-Sigma Code*****************
skew = 1;
% Integrator coefficients
intcoeff1 = skew*0.5;
intcoeff2 = skew*0.2;
```

```
ampl = 0.375;
vcm = 0.6;
refp = 1.1;
refn = 0.1;
high = 1.2;
low = 0;
fsample = 2.4e6; % clock frequency
OSR = 512;
f_signal = 503/(fsample/2); % signal normalized to bandwidth defined by oversampling rate
x=(1:2^18); % Number of data points
x=vcm+ampl*(sin(2*pi*0.5*f_signal*x));
y = zeros(length(x),1); % output data placeholder
%Set 1-bit DAC's initial value to refn
vd = refn;
%Initialise Integrators to common mode voltages
vint1 = vcm;
vint2 = vcm;
% Run modulator for x clock cycles
for i=1:length(x)
 %Summing Junction
sum = vcm + (x(i)-vcm) - (vd - vcm);
%Integrator 1
vint1 = vcm + intcoeff1*(sum - vcm) + (vint1 - vcm);
%Integrator 2
vint2 = vcm + intcoeff2*(vint1 - vcm) + (vint2 - vcm);
% Quantizer & D2A
        if ((vcm + (vint1 - vcm) + (vint2 - vcm)) > vcm)
            y(i) = high;
            vd = refp;
          else
            y(i) = low;
            vd = refn;
          end
```

```
    end
% save results
save('caldsadcoutput.dat','y','-ascii');
%*********************************************************
```

Appendix C Matlab Processing Scripts

The following script was used to load and process the data generated from the above scripts. The FFT of the data is done. Subsequently, SNR, SFDR parameters are extracted from the simulation.

C.1 Matlab script for ΔΣ Modulator FFT Analysis

```
% Matlab Script to do frequency domain analysis on the data from
% GSM, WCDMA and Calibration DS modulator scripts
%Author: Olujide A. Adeniran. 10th July 2006
%
clear all
close all
fsample = 2.4e6; % Clock frequency. Change accordingly
OSR = 512; % Change accordingly
f_signal = 503/(fsample/2); % Change accordingly
my_title = 'Delta Sigma ADC Spectrum';
beta = 20;
x = load('caldsadcoutput.dat'); % Change accordingly
%Normalise input data amplitude
kk = max(x(1:20));
mid = kk/2;
x = x-mid;
x = 4*x;
x = x/max(x);
x = round(x);
N = length(x);
freq=(1:round(N/2))/N*fsample;
window = kaiser(N, beta); % kaiser window is used
window = window/sqrt(mean(window.^2)); % normalize power of window
X = zeros(length(x),1);
for i=1:length(x(1,:))
X = X+(abs(fft(x(:,i).*window))/N).^2; % power spectrum estimation with prior windowing
end
X = X/length(x(1,:));
```

```
X = X(1:(round(N/2))); % consider only one side of the spectrum
subplot(2,1,1); semilogx(freq,10*log10(X),'Color','blue'); xlabel('frequency [Hz]');
ylabel('power [dB]');
X = X(1:(round(N/OSR/2))); % consider in-band spectrum
freq = freq(1:(round(N/OSR/2)));
subplot(2,1,2); plot(freq,10*log10(X),'Color','green'); xlabel('Frequency [Hz]'); ylabel('Power
[dB]');
% Estimate signal and 1st 3 harmonic spectral contents
peak_signal = round(f_signal*N/2);
bins_signal = peak_signal-10 : peak_signal+10;
peak_2ndharmonic = round(2*f_signal*N/2);
bins_2ndharmonic = peak_2ndharmonic-9 : peak_2ndharmonic+9;
peak_3rdharmonic = round(3*f_signal*N/2);
bins_3rdharmonic = peak_3rdharmonic-9 : peak_3rdharmonic+9;
%Integrate Signal
SIGNAL_ENERGY = 0;
for i=bins_signal(1):bins_signal(length(bins_signal))
SIGNAL_ENERGY = SIGNAL_ENERGY + X(i);
end
PEAK_SIG = max(X(bins_signal));
if (f_signal ~= 0.0) % take signal out for noise integration
P = X(peak_signal+11);
X(bins_signal) = [P P P P P P P P P P P P P P P P P P P];
 %Compute SFDR before taking out harmonics
SFDR = 10*log10(PEAK_SIG)-10*log10(max(X))
% Take out 2nd and 3rd harmonic for SNR calculations
P = X(peak_2ndharmonic+10);
X(bins_2ndharmonic) = [P P P P P P P P P P P P P P P P P P P];
P = X(peak_3rdharmonic+10);
X(bins_3rdharmonic) = [P P P P P P P P P P P P P P P P P P P];
 end
hold on;
plot(freq,10*log10(X),'Color','blue'); xlabel('frequency [Hz]'); ylabel('power [dB]');
hold off;
```

```
% Integrate Noise
NOISE = 0;
for i=1:length(X)
NOISE = NOISE + X(i);
end
%Compute SNR and DR
PEAK_NOISE = max(X);
DR = 10*log10(PEAK_SIG)-10*log10(PEAK_NOISE)
N = 10*log10(NOISE)
SNR = 10*log10(SIGNAL_ENERGY/NOISE)
my_title = strcat(my_title,'. SNR = ',num2str(SNR), 'dB, SFDR = ',num2str(SFDR), 'dB.');
subplot(2,1,1);
title(my_title);
zoom on;
```

C.2 Matlab script for Nyquist ADC FFT Analysis

```
% Matlab Script to do frequency domain analysis on the data from
% measured Nyquist ADCs
%Author: Olujide A. Adeniran. 10th July 2006
%
clear
close all
% Sets Number of samples
N=2^16 % change accordingly
NoBits = 10; % change accordingly
out=load('test3_101kHz.csv'); % measured data
out=out(1:N);% Sets Number of samples irrespective of file data length
out=out-(2^NoBits -1)/2;%Removes DC from Data
samp = 20480000; % sampling frequency
infreq = 101000; % signal frequency
nyquist=samp/2;
% Calculating the Power Spectral Density
% using a N length Beta beta Kaiser Window
beta=20;
```

```
kaiser_window=kaiser(N,beta);
out1=out.*kaiser_window; % apply Kaiser window
ps=fft(out1,N); % complex fft
ps=abs(ps(1:(1+N/2)));%Amplitude Spectra
ps=ps.*ps;%convert to Power Spectra
freq=(1:(N/2)+1)/((N/2)+1)*nyquist;
ps=ps/max(ps);
psd=10*log10(ps);
plot(freq,psd,'k');
title('Power Spectrum')
xlabel('Frequency')
ylabel('Power')
zoom on;
% Measuring sidebands of fundamental
a=fix(-8+0.5*N*infreq/nyquist);
b=ceil(8+0.5*N*infreq/nyquist);
sig=sum(ps(a:b))
noi=sum(ps(6:a-1))+sum(ps(b+1:N/2))
snr=10*(log10(sig/noi))
SFDR=0-max(max(psd(6:a-1)),max(psd(b+1:N/2)))
ENOB=(snr-1.76)/6.02
% Analyze input data to find offset and amplitude
N=length(out);
maxin=(max(out));
minin=(min(out));
N1=length(find(out>maxin-1));
N2=length(find(out<minin+1));
C1=cos((pi/360)*180*N1/N);
C2=cos((pi/360)*180*N2/N);
offset=127*(C2-C1)/(C2+C1);
amplitude=(127-offset)/C1;
c=(1:NoBits)/1;
zoom on
x=(1:N)/samp;
```

```
% generate pure sine wave at freq fin with same amplitude as fin
puresine=offset+128+amplitude*(sin(2*pi*infreq*x));
for i=1:(NoBits-1)
if(puresine(i)>(max(out)));
puresine(i)=max(out);
else if(puresine(i)<0);
puresine(i)=0;
end
i=i+1;
end
end
% Calculate DNL
difference=hist(out,2^NoBits)./hist(puresine,2^NoBits);
dnl=difference-1;
% Integrate DNL to find ADC characteristics
dnlmean=dnl-mean(dnl);
k=1;
for i=1:((2^NoBits)-1)
ramp(k)=sum(difference(1:k));
inl(k)=sum(dnlmean(1:k));
k=k+1;
end
% Generate ideal ADC ramp
idealramp=linspace(ramp(1),ramp((2^NoBits)-1),((2^NoBits)-1));
figure(2);
plot(dnl,'k');
title('DNL measurement')
xlabel('Output Code')
ylabel('DNL')
figure (3);
hold on;
plot(ramp,'k');
plot(idealramp,'k')
title('ADC Linearity')
```

```
xlabel('Output Code')
ylabel('Data Output')
zoom on;
figure (4);
plot(inl,'k');
title('INL measurement')
xlabel('Output Code')
ylabel('INL')
zoom on
MaxDNL=max(dnl)
MinDNL=min(dnl)
MaxINL=max(inl)
MinINL=min(inl)
```

Bibliography

[1] http://www.3gpp.org.

[2] http://www.dvb.org.

[3] S. Haykins, *Communication Systems*, (John Wiley & Sons, Inc, 2001).

[4] http://nobelprize.org/physics/laureates/1909/marconi-bio.html.

[5] H. Nyquist, "Certain Topics in Telegraph Transmission Theory," *Transactions of the AIEE*, vol. 47, pp. 617-644, Feb, 1928.

[6] C. E. Shannon, "A mathematical theory of communication," *Bell System Tech. J.*, vol. 27, pp. 379-423, 623-656, 1948.

[7] W. Shockley, "The pathway to the conception of the junction transistor," *IEEE Trans. Electron Devices*, vol. 23, no. 7, pp. 597 – 620, July 1976.

[8] http://www.bbc.co.uk/history/historic_figures/baird_logie.shtml.

[9] http://www.gsmworld.com.

[10] Validating DVB-H - Tests Verify Interoperability Of Specification & Highlight Outstanding Performance. www.dvb.org, Press Release 128, 14/02/2005.

[11] V. Rambeau, H. Brekelmans, M. Notten, K. Boyle, and J. van Sinderen, "Antenna and input stages of a 470-710 MHz silicon TV tuner for portable applications," in *Proc. ESSCIRC 2005*, vol. 1 pp. 239-242, September 2005.

[12] P. Antoine, P. Bauser, H. Beaulaton, M. Buchholz, D. Carey, T. Cassagnes, T. K. Chan, S. Colomines, F. Hurley, D. T. Jobling, N. Kearney, A. C. Murphy, J. Rock, D.Salle, and C.-T. Tu, "A Direct-Conversion Receiver for DVB-H," *IEEE J. Solid State Circuits*, vol. 40, no. 12, pp. 2536-2546, December 2005.

[13] C.-C. Wang, C.-L. Lee, L.-P. Lin, and Y.-L. Tseng, "Wideband 70dB CMOS Digital Variable Gain Amplifier Design for DVB-T Receiver's AGC," in *Proc. ISCAS 2005*, vol. 1 pp. 356 – 359, May 2005.

[14] C.-H. Heng, M. Gupta, S.-H. Lee, D. Kang, and B.-S. Song, "A CMOS TV Tuner/Demodulator IC With Digital Image Rejection," *IEEE J. Solid State Circuits*, vol. 40, no. 12, pp. 2525-2535, December 2005.

[15] L. Jian, Z. Jianyun, S. Bo, Z. Xiaoyang, G. Yawei and T. Ting'ao, "A 10BIT 30MSPS CMOS A/D converter for high performance video applications," in *Proc. ESSCIRC 2005*, vol. 1 pp. 523-526, September 2005.

[16] K-Y. Jheng, T-H. Wu, Y-C. Wang, J-C, Yeo, Y-J. Cho and A-Y. Wu, "A DVB-T baseband demodulator design based on multimode silicon IPs," in *Proc. IEEE VLSI-TSA 2005*, vol. 1, pp. 48-52, April 2005.

[17] L. Gao, S. Liu and Roger A. Dougal, "Dynamic lithium-ion battery model for system simulation." *IEEE Trans. Components and Packaging Technologies*, vol. 25, no. 3, pp. 495 – 505, September. 2002.

[18] David Johns and Ken Martin, *Analog Integrated Circuit Design*, (John Wiley & Sons, Inc, 1997).

[19] B-L, Thomas, W. Rondeau, J. H. Reed and C. W. Bostian, "Analog and Digital Converters" in *IEEE Signal Processing Magazine*, vol. 22, no. 11, pp. 69 – 77, November 2005.

[20] S. Anikhindi, G. Cradockl, R. Makowitz and C. Patzelt, "A commercial DVB-T demodulator chipset," in *Proc. International Broadcasting Convention*, vol. 1, pp. 528 – 533, September 1997.

[21] P. M. Aziz, H. V. Sorensen and J. Van-der-Spiegel, "An overview of sigma-delta converters, in *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp. 61 – 84, January 1996.

[22] B. Widrow and M. E. Hoff, Jr., "Adaptive Switching Circuits", *WESCON Convention Record*, Pt. 4, pp. 96-104, 1960.

[23] M. Bossche, J. Schoukens, and J. Renneboog, "Dynamic testing and diagnostics of ADCs," *IEEE Trans. Circuits Syst.* vol. CAS-33, pp. 775-785, Aug. 1986.

[24] Standard for Digitizing Waveform Recorders, Dec. 1994. IEEE Std. 1057.

[25] Standard for Terminology and Test Methods for Analog-to-Digital Converters, Oct. 2000. IEEE Std. 1241.

[26] C. Clayton, J. A. McClean, and G. J. McCarra, "FFT performance testing of data acquisition systems," *IEEE Trans. Instr. Meas.*, vol. IM-35, pp. 212–215, June 1986.

[27] Blair, J., "Histogram measurement of ADC nonlinearities using sine waves," *IEEE Tran. on Instr. and Meas.*, vol. 43, no. 3, pp. 373–383, 1994.

[28] A. Brandolini and A. Gandelli, "Testing methodologies for analog-todigital converters," *IEEE Trans. Instr. Meas.*, vol. 41, pp. 595–603, Oct. 1992.

[29] T. M. Souders, R. Flach, and T. C. Wong, "An automatic test set for the dynamic characterization of A/D converters," *IEEE Trans. Instr. Meas.*, vol. IM-32, pp. 180–186, Mar. 1983.

[30] C. A. Young, "An enhanced method for characterizing successive approximation converters," *IEEE Trans. Instr. Meas.*, vol. 39, pp. 335–339, Apr. 1990.

[31] E. D. Koltik, G. D. Muginov, and G. P. Tsyvirko, "Calibration of measuring and computational systems for analysis of random signal parameters," in *IMEKO-88, Applications 88-D53*, 1988, pp. 573–580.

[32] G. D. Muginov and A. N. Venetsanopoulos, "A New Approach for Estimating High-Speed Analogue-to-Digital Converter Errors ," *IEEE Trans. Instr. Meas.*, vol. 46, no. 4 pp. 980–985, Aug. 1997.

[33] H. S. Mendonça, J. M. Silva and J. S. Matos, "ADC testing using joint time-frequency analysis," in *Proc. Third International Conference on Advanced A/D and D/A Conversion Techniques and their Applications*, no. 466. pp. 157 – 159, July 1999.

[34] J. Holub, R. Smid and J. Vedral, "Chirp based method for ADC testing: simulation and evaluation," in *Proc. Third International Conference on Advanced A/D and D/A Conversion Techniques and their Applications*, no. 466. pp. 94 – 96, July 1999.

[35] F. Attivissimo, N. Giaquinto, and I. Kale, "INL Reconstruction of A/D Converters via Parametric Spectral Estimation," *IEEE Trans. Instr. Meas.*, vol. 53, no. 4 pp. 940–946, August 2004.

[36] C. Wegener and M. P. Kennedy, "Linear model-based testing of ADC nonlinearities," *IEEE Trans. Circuits and Systems I.*, vol. 51, no. 1, pp. 213–217, Jan. 2004.

[37] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, April 1999.

[38] J. Multer et al., "A 21-mW 8-b 125-MSample/s ADC in 0.09-mm2 in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2116-2125, December 2004.

[39] Y. Chiu, P. R. Gray and B. Nikolić, "A 14-b, 12MS/s, CMOS pipeline ADC with over 100-dB SFDR," *IEEE J. Solid State Circuits*, vol 39, no. 12, pp. 2139-2151, December 2004.

[40] A. Zanchi and F. Tsay, "A 16-bit 65-MS/s 3.3-V pipeline ADC core in SiGe BiCMOS with 78-dB SNR and 180-fs Jitter," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1225–1237, June. 2005.

[41] J. E. Johnston, "A 24-bit delta-sigma ADC with an ultra-low noise chopper-stabilized programmable gain instrumentation amplifier," in *Proc. Conf. Advances A/D and D/A Conversion Techniques and Their Applications*, 1999, pp. 179–182.

[42] K. Poulton, R. Neff, B, Setterberg, B. Wuppermann, T. Kopley, R. Jewett, J. Pernillo, C. Tan and A. Montijo, "A 20 GS/s 8 b ADC with a 1 MB memory in 0.18 /μm CMOS," *IEEE Solid-State Circuits Conference Dig. Tech. Papers.* vol. 1 pp. 318 – 496, February 2003.

[43] P. Scholtens and M. Vertregt, "A 6b 1.6 GSamples/s Flash ADC in 0.18 mm CMOS using Averaging Termination," *IEEE Solid-State Circuits Conference Dig. Tech. Papers*, pp. 128-129, February 2002.

[44] X. Jiang, Z. Wang, M. F. Chang, "A 2 GS/s 6 b ADC in 0.18 μm CMOS," *IEEE Solid-State Circuits Conference Dig. Tech. Papers*, Feb. 2003.

[45] C. Paulus, H.-M. Bluthgen, M. Low, E. Sicheneder, N. Briils, A. Courtois, M. Tiebout, and R. Thewes, "A 4 GS/s 6 b ADC in 0.13 μm CMOS," *IEEE VLSI Symposium Dig. Tech. Papers*, pp. 420 – 423, June 2004.

[46] B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.

[47] I.-I. Pan and A. A. Abidi, "Spatial filtering in flash A/D converters," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 8, pp. 424-4315, August 2003.

[48] H. Okada, Y. Hashimoto, K. Sakata, T. Tsukada, and K. Ishibashi, "Offset calibrating comparator array for 1.2- V, 6-bit, 4-Gsample/s flash ADCs using 0.13-μm CMOS technology," in *Proc. ESSCIRC 2003*, September 2003, pp. 711-714.

[49] Y. Tarnba and K. Yamakido, "A CMOS 6b 500MSamplels ADC for hard disk drive read channel," in *IEEE International Solid-state Circuits Conference Dig. Tech. Papers*, February 1999, pp. 324-325.

[50] M. P, Flynn, C. Donovan, and L. Sattler, "Digiial calibration incorporating redundancy of flash ADCs," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 5, pp. 205-213, May 2003.

[51] C.-C. Huang and J.-T. Wu, "A statistical background calibration technique for flash analog-to-digital converters," in Proc. of *IEEE International Symposium on Circuits and Systems*, vol. 1, May 2004, pp. 125-128.

[52] http://cmp.imag.fr/products/ic/?p=STHCMOS9.

[53] Yoji Yoshii, Minoru Nakamura, Kaoru Hirasawa, Akio Kayanuma and Katsuaki Asano, "An 8-bit 350 MHz Flash ADC," in *IEEE International Solid-state Circuits Conference Dig. Tech. Papers*, February 1987, pp. 96-97.

[54] J. Wu and B. A. Wooley, "A 100-MHz pipelined CMOS comparator," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1379-1385, December. 1988.

[55] S. Kim and M. Song, "An 8-bit 200MSPS CMOS A/D Converter for Analog Interface Module of TFT-LCD Driver," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 528- 531, May 2001.

[56] P. M. Figueiredo and J. C. Vital, "Low kickback noise techniques for CMOS latched comparators," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 537- 540, May 2004.

[57] M. Steyaert et al. "A 100 MHz 8 Bit CMOS Interpolating A/D Converter," in *Proc. IEEE Custom Integrated Circuits Conference*, vol. 1, pp. 28.1.1-28.1.4, May 1993.

[58] Y. Nejirne, M. Hotta, and S. Ueda, "An 8-b ADC with Over-Nyquist Input at 300-Ms/s Conversion Rate," *IEEE J. Solid-State Circuits*, vol. 26, no. 9, pp. 1302-1308, September 1991.

[59] Y.-J. Chuang, H.-H. Ou and B.-D. Liu, "A novel bubble tolerant thermometer-to-binary encoder for flash A/D converter," *IEEE International Symposium on VLSI Design, Automation and Test*, vol. 1, pp. 315 – 518, April 2005.

[60] F. Kaess, R. Kanan, B. Hochet and M. Declercq, "New Encoding Scheme for High-Speed Flash ADC's," in *Proc. IEEE International Symposium on Circuits and Systems.* vol. 1, pp. 5-8, June 1997.

[61] R. Kanan. F. Kaess. M. Declercq, "A 640 mW high accuracy 8-bit 1 GHz flash ADC encoder," in *Proc. IEEE International Symposium on Circuits and Systems.* vol. 2, pp. 420-423, lune 1999.

[62] C. S. Wallace, "A suggestion for a fast multiplier," *IEEE Trans. on Electronics Computers*, pp. 14-17, February 1964.

[63] L. Daegyu, Y. Jinchcol, C. Kyusun, J. Ghaznan, "Fat tree encoder design for ultra-high speed flash A/D converters," in *Proc. Of Midwest Symposium on Circuits and Systems*, vol. 2, pp. 87 - 90, August 2002.

[64] E. Säll, M. Vesterbacka and K. O. Andersson, "A study of digital decoders in flash analog-to-digital converters," in *Proc. IEEE International Symposium on Circuits and Systems.* vol. 2, pp. 129-132, May 2004.

[65] S. Lewis and P. Gray, "A pipelined 5-Msample/s 9-bit analog-to-digital converter," *IEEE J. Solid-state Circuits,* vol. SC-22, pp. 954-961, Dec. 1987.

[66] M. Clara, A. Wiesbauer and F. Kuttner, "A 1.8 V fully embedded 10 b 160MS/s two-step ADC in 0.18μm CMOS," *Proc. Custom Integrated Circuits Conference*, vol. 1, pp. 437 – 440, May 2002.

[67] B. Razavi and B. A. Wooley, "A 12-b 5-Msample/s two-step CMOS A/D Converter," *IEEE J. Solid-state Circuits*, vol. 27, no. 12, pp. 1667 - 1678, December 1990.

[68] A. Zanchi, F. (C.-Y.) Tsay, "A 16-bit 65-MS/s 3.3-V Pipeline ADC Core in SiGe BiCMOS With 78-dB SNR and 180-fs Jitter," *IEEE J. Solid-state Circuits*, vol. 40, no. 6, pp. 1225- 1237, June 2005.

[69] S.-C. Lee, K.i-D. Kim, J.-K. Kwon, J. Kim and S.-H. Lee, "A 10-bit 400-MS/s 160-mW 0.13-μm CMOS Dual-Channel Pipeline ADC Without Channel Mismatch Calibration," in *IEEE J. Solid-state Circuits*, vol. 41, no. 7, pp. 1596-1605, July 2006.

[70] B.-S. Song, S.-H. Lee and M. F. Tompsett, "A 10-b 15-MHz CMOS recycling two-step A/D Converter," *IEEE J. Solid-state Circuits*, vol. 25, no. 6, pp. 1328- 1338, December 1990.

[71] D-Y Chang, "Design techniques for a pipelined ADC without using a front-end sample-and-hold amplifier," *IEEE Trans. Circuits Syst.-I: Regular Papers*, vol. 51, no.11, pp. 2123-2132, Nov. 2004.

[72] J. Goes, J. C. Vital and J. E. Franca, "Systematic Design for Optimization of High-Speed Self-Calibrated Pipelined A/D Converters," *IEEE Trans. Circuits Syst.-II: Analogue and Digital Signal Processing*, vol. 45, no.12, pp. 1513 - 1526, December 1998.

[73] S.H. Lewis, H. S. Fetterman, G. F. Gross Jr., R. Ramachandran and T. R. Viswanathan, "A 10-b 20Msample/s analog-to-digital converter," *IEEE J. Solid State Circuits*, vol. 27, no. 3, pp. 351-358, March 1992.

[74] T. B. Cho and P. R. Gray, "A 10b, 20Msamples/s, 35mW pipeline A/D Converter," *IEEE J. Solid State Circuits*, vol. 30, no. 3, pp. 166-172, March 1995.

[75] W. C. Black, Jr. and D. A. Hodges, "Time-interleaved Converter Arrays," *IEEE J. Solid State Circuits*, vol. 15, no. 12, pp. 1022-1029, December 1980.

[76] K. Poulton, J. J. Corcoran and T. Hornak, "A 1-GHz 6-bit ADC system," *IEEE J. Solid State Circuits*, vol. 22, no. 12, pp. 962-970, December 1987.

[77] K. Kusumoto, A. Matsuzawa, and Kenji Murata, "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," *IEEE J. Solid State Circuits*, vol. 28, no. 12, pp. 1200-1206, December 1993.

[78] F. Vessal and C. A. T. Salama, "An 8-Bit 2-Gsample/s Folding-Interpolating Analog-to-Digital Converter in SiGe Technology," *IEEE J. Solid State Circuits*, vol. 39, no. 1, pp. 238-241, January 2004.

[79] B. M. Gordon, "Linear electronic analog/digital conversion architectures, their origins, parameters, limitations, and applications," *IEEE Trans. Circuits Syst.*, vol. CAS-25, no. 7, pp. 391-418, July 1978.

[80] H. Y. Yang and R.Sarpeshkar, "A Time-Based Energy-Efficient Analog-to-Digital Converter," *IEEE J. Solid State Circuits*, vol. 40, no. 8, pp. 1590-1601, August 2004.

[81] J. Baer and C. Heckler, Jr. "A versatile and sensitive balanced magnetic comparator," *IEEE Trans. Magnetics.*, vol. 2, no. 6, pp. 364-368, September 1966.

[82] J. McCreary and P. Gray, "A high-speed, all-MOS, successive-approximation weighted capacitor A/D conversion technique," in *IEEE International Solid-state Circuits Conference Dig. Tech. Papers*, vol. 18, pp. 38-39, February 1975.

[83] D. Draxelmayr, "A 6b 600 MHz 10mW ADC array in digital 90nm CMOS," *IEEE International Solid-state Circuits Conference Dig. Tech. Papers*, vol. 1, pp. 264-527, February 2004.

[84] P.W. Li, M.J. Chin, P.R. Gray and R. Castello, "A ratio-independent algorithmic analog-to-digital conversion technique," *IEEE J. Solid State Circuits*, vol. 19, no. 6, pp. 828-836, December 1984.

[85] C. Hee-Cheol, Y. Seung-Bin, L. Ho-Young, P. Ho-Jin and K. Jae-Whui, "A calibration-free 3V 16b 500kS/s 6mW 0.5mm^2 ADC with 0.13 μm CMOS," *IEEE Symposium on VLSI Circuits Conference Dig. Tech. Papers*, pp. 76-77, June 2004.

[86] R. J Baker, H. W. Li, D. E. Boyce, CMOS Circuit Design, Layout, and Simulation. Piscataway, NJ, IEEE Press, 1998.

[87] F. Gerfers and Y. Manoli, "A Design Strategy for Low-Voltage Low-Power Continuous-Time ΔΣ A/D Converters," *Pro c. European Design, Automation and Test Conference*, pp. 361 – 368, March 2001.

[88] P. Benabes and I. Kale, "MASH topologies- a means to minimizing sensitivity to clock jitter in higher-order continuous-time sigma-delta modulators," *Proc. IEEE IMTC '03*, vol. 1 pp. 242 – 245, May 2003.

[89] B. Hernes, A. Briskemyr, T. N. Andersen, F. Telste, T. E. Bonnerud, Ø. Moldsvor, " A 1.2V 220MS/s 10b pipeline ADC implemented in 0.13μm digital CMOS," *ISSCC. 2004 Dig. Tech. Papers.* vol. 1, pp. 256 – 526, February 2004.

[90] D. Miyazaki, M. Furuta, S. Kawahito, "A 75mW 10bit 120MSample/s parallel pipeline ADC," *Proc. ESSCIRC '03*, vol. 1, pp. 719 – 722, Sept. 2003.

[91] D.-Y. Chang and Un-Ku Moon, "A 1.4-V 10-bit 25-MS/s pipelined ADC using amplifier-reset switching technique," IEEE J. Solid-State Circuits, vol. 38, pp. 1401-1404, Aug. 2003.

[92] B. Min, P. Kim, F. W. Bowman III, D. M. Boisvert and A. J. Aude, "A 69-mW 10-bit 80-MSample/s pipelined CMOS ADC," IEEE J. Solid-State Circuits, vol. 38, pp. 2031-2038, Dec. 2003.

[93] D. Miyazaki, S. Kawahito and M. Furuta, "A 10-b 30-MS/s low-power pipelined CMOS A/D converter using a pseudodifferential architecture," IEEE J. Solid-State Circuits, vol. 38, pp. 369-373, Feb 2003.

[94] D. Saias, F. Montaudon, E. Andre, F. Bailleul, M. Bely, P. Busson, S. Dedieu, A. Dezzani, A. Moutard, G. Provins, E. Rouat, J. Roux, G. Wagner and F. Paillardet, "A 0.12μm CMOS DVB-T Tuner," *IEEE ISSCC Dig. Tech. Papers*, vol. 1, pp. 430-431, February 2005.

[95] European Industry Association (EICTA) MBRAI-02-16 v1.0 (2004-01): Mobile and Portable DVB –T Radio Access Interface Specification, 2004.

[96] http://www.dvh-h.org.

[97] G. Faria, J.A. Henriksson, E. Stare and P. Talmola, "DVB-H: digital broadcast services to handheld devices," *Proc. IEEE*, vol. 94, no. 1, pp. 194 – 209, January 2006.

[98] A. L. Intini, "Orthogonal Frequency Division Multiplexing for Wireless Networks," Graduate Thesis, University of California, Santa Barbara, December 2000.

[99] R. B. Staszewski, R. Staszewski, J. L. Wallberg, T. Jung, C.-M. Hung, J. Koh, D. Leipold, K. Maggio and P. T. Balsara, "SoC With an Integrated DSP and a 2.4-GHz RF Transmitter," *IEEE Trans. VLSI Syst.*, vol. 13, no. 11, pp. 1253-1265, November 2005.

[100] S. Khorram, H. Darabi, Z. Zhou, Q. Li, B. Marholev, J. Chiu, J. Castaneda, H.-M. Chien, S. B. Anand, S. Wu, M.-A. Pan, R. Roofougaran, H. J. Kim, P. Lettieri, B. Ibrahim, J. J. Rael, L. H. Tran, E. Geronaga, H. Yeh, T. Frost, J. Trachewsky and A. Rofougaran, "A Fully Integrated SOC for 802.11b in 0.18-μm CMOS," *IEEE J. Solid State Circuits*, vol. 40, no.12, pp. 2492-2501, December 2005.

[101] J. Lahteenmaki, J. Miettinen and P. Heino, "The design of miniature 3D RF module," *Proc. IEEE ECTC '05*, vol. 1, pp. 814 – 817, June 2005.

[102] F. Murray, "Silicon based system-in-package: a passive integration technology combined with advanced packaging and system based design tools to allow a breakthrough in miniaturization," *Proc. IEEE Bipolar/BiCMOS Circuit and Technology Meeting*, pp. 169 – 173, October 2005.

[103] W. Krenik, D. D. Buss and P. Rickert, "Cellular Handset Integration—SIP versus SoC" *IEEE J. Solid State Circuits*, vol. 40, no.9, pp. 1839-1846, September 2005.

[104] M. Kornfeld, "DVB-H - the emerging standard for mobile data communication," in Proc. IEEE 2004 Int. Symp. Consumer Electronics, pp. 193-198, Sep. 2004.

[105] European Telecommunication Standards Institute (ETSI) TR 102 377 v1.1.1 (2005-02): Digital Video Broadcasting (DVB); DVB-H Implementation Guidelines, 2005.

[106] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998.

[107] E. Cetin, I. Kale and R.C.S. Morling, "Joint compensation of IQ-imbalance and carrier phase synchronization errors in communication receivers," *Proc. ISCAS'05*, vol. 5, pp. 4481-4484, May 2005.

[108] K. Nagaraj, H. Fetterman, J. Anidjar, S. Lewis, and R. Renninger, "A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers," *IEEE J. Solid State Circuits*, vol. 32, pp. 312–320, Mar. 1997.

[109] P. Bogner, "A 28mW 10b 80MS/s pipelined ADC in 0.13um CMOS," *Proc. ISCAS'04*, vol. 1, pp. 17-20, May 2004.

[110] D. W. Cline and P. R. Gray, "A power optimized 13-b 5-Msamples/s pipelined analog-to-digital converter in 1.2-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, pp. 294–303, March 1996.

[111] B. Murmann and B. Boser "A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification," *IEEE J. of Solid State Circuits*, vol. 38, no. 12, pp. 2040-2050, December 2003.

[112] D-Y Chang, "Design techniques for a pipelined ADC without using a front-end sample-and-hold amplifier," *IEEE Trans. Circuits Syst.-I: Regular Papers*, vol. 51, no.11 pp. 2123-2132, Nov. 2004.

[113] I. Mehr and L. Singer, "A 55-mW, 10-bit 40-MS/s Nyquist-Rate CMOS ADC, *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 318-325, March 2000.

[114] R. Castello, F. Montecchi, F. Reís, and A. Baschirotto, "Low-Voltage Analog Filters," *IEEE Trans. Circuits Syst.-I: Fundamental Theory and Applications*, vol. 42, pp. 827-840, Nov. 1995.

[115] A. M. Abo and P. Gray, "A 1.5-V, 10-bit 14.3 MS/s CMOS pipeline analog-to-digital converter, *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, May 1999.

[116] A-J Annema, "Analog circuit performance and process scaling" *IEEE Trans. Circuits Syst.-II: Analog and Digital Signal Processing*, vol. 46, pp. 711-725, June 1999.

[117] W. Yang, D. Kelly, I. Mehr, M. T. Sayuk and L. Singer, "A 3-V 340mW 14-b 75-Msample/s CMOS ADC with 85 dB SFDR at Nyquist input" *IEEE J. Solid-State Circuits*, vol. 36, pp. 1931-1936, Dec. 2001.

[118] P. T. M. Kwok and H. C. Luong, "Power optimization for pipeline analog-to-digital converters" *IEEE Trans Circuits Syst.-II: Analog and Digital Signal Processing*, vol. 46, pp. 549-553, May 1999.

[119] Kenneth R Laker and Willy M. C. Sansen, Design of Analog Integrated Circuits and Systems, McGraw-Hill Inc, 1994.

[120] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high-resolution comparators," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1916-1926, Dec. 1992.

[121] A. P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low-Power Digital CMOS Design," *IEEE J. Solid-State Circuits*, vol. 27, pp. 473-484, April. 1992.

[122] Steven R. Nosworthy, Richard Schreier, Gabor C. Temes, Delta-Sigma Data Converters: Theory, Design and Simulation, IEEE Press, 1997.

[123] http://www.austriamicrosystems.com

[124] J. Arias, V. Boccuzzi, L. Quintanilla, L. Enríquez, D. Bisbal, M. Banu and J. Barbola, "Low-power pipeline ADC for wireless LANs," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1338-1340, Aug. 2004.

[125] K. Kaviani, O. Oralkan, P. Khuri-Yakub and B. A. Wooley, "A multichannel pipeline analog-to-digital converter for an integrated 3-D ultrasound imaging system," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1266-1270, Jul. 2003.

[126] B. Vaz, J. Goes, R. Piloto, J. Neto, R. Monteiro and N. Paulino, "A Low-voltage 3 mW 10-bit 4MS/s pipeline ADC in digital CMOS for sensor interfacing," *Proc. ISCAS'05*, vol. 1, pp. 4074-4077, May 2005.

[127] B. Vaz, J. Goes and N. Paulino, "A 1.5-V 10-b 50 MS/s time-interleaved switched-opamp pipeline CMOS ADC with high energy efficiency," *2004 VLSI Circuits Symp, Dig. Techn. Papers*, pp. 432-435, June 2004.

[128] J-B. Park, S-M. Yoo, S-W. Kim, Y-J. Cho, and S-H. Lee, "A 10-b 150-MSample/s 1.8-V 123-mW CMOS A/D converter with 400-MHz input bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1335-1337, Aug. 2004.

[129] O. Stroeble, V. Dias and C. Schwoerer, "An 80 MHz 10-b pipeline ADC with dynamic range doubling and dynamic reference selection," *ISSCC' 04 Dig. Tech. Papers*, vol. 1, pp. 462-539, Feb. 2004.

[130] J. Li, J. Chang, B. Shen, X. Leng, Y. Guo, T. Tang, "A 10bit 30MSPS A/D converter for high performance video applications," *Proc. ESSCIRC'05*, pp. 523-526, Sept. 2005.

[131] W. Wolf, "Building the software radio," *IEEE Computer Magazine*, vol. 38, no. 3, pp. 87 – 89, March 2005.

[132] M. R. Yuse, W. Liu, "Alternative Wideband Front-End Architectures for Multi-Standard Software Radios," *Proc. IEEE Vehicular Technology Conference*, vol. 3, pp. 1968 – 1972, September 2004.

[133] T. Salo, S. Lindfors and K. A. I. Halonen, "A 80-MHz Bandpass ΔΣ modulator for a 100-MHz IF Receiver," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 798 - 808, July 2002.

[134] O.Oliaei, P. Clément and P. Gorisse, "A 5-mW Sigma–Delta modulator With 84-dB Dynamic Range for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 37, no. 1, pp. 2 - 10, January 2002.

[135] T. Burger and Q. Huang, "A 13.5-mW 185-Msample/s ΔΣ modulator for UMTS/GSM Dual-Standard IF Reception," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1868 - 1878, December 2001.

[136] L. J. Breems, E. J. van der Zwan and J. H. Huijsing, "A 1.8-mW CMOS modulator with Integrated Mixer for A/D Conversion of IF Signals," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 468 - 475, April 2000.

[137] S. A. Jantzi, K. W. Martin and A. S. Sedra, "Quadrature Bandpass ΔΣ Modulation for Digital Radio," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1935 - 1950, December 1997.

[138] http://www.shoshin.uwaterloo.ca/~jscouria/GSM/index.html.

[139] ETSI TS 100 910 V8.16.0, "Digital cellular telecommunications system (Phase 2+); Radio transmission and reception (3GPP TS 05.05 version 8.16.0 Release 1999)," *European Telecommunications Standards Institute*, August 2003.

[140] http://www.gsacom.com.

[141] WCDMA/UMTS Wireless Networks Technical Brief, http://www.tektronix.com.

[142] ETSI TS 125 101 V7.3.0, "Universal Mobile Telecommunications System (UMTS); User Equipment (UE) radio transmission and reception (FDD) (3GPP TS 25.101 version 7.3.0 Release 7)," *European Telecommunications Standards Institute*, March 2006.

[143] J. C. Rudell, J. A. Weldon, J.-J. Ou, L. Lin, and P. Gray, "An Integrated GSM/DECT Receiver: Design Specifications," *University of California Berkeley Electronics Research Laboratory Memorandum Memo*, no. UCB/ERL M97/82, April 1998.

[144] C. Halijak and J. Tripp, "A deterministic study of delta modulation," *IEEE Trans. Automatic Control*, vol. 8, no. 4, pp. 339 – 347, October 1963.

[145] H. Inose, Y. Yasuda and J. Murakami, "A telemetering system code modulation -- ΔΣ modulation," *IRE Trans. Space Elect. And Telemetry*, vol. SET-8, pp. 204 – 209, September 1962.

[146] H. Inose and Y. Yasuda, "A unity bit coding method by negative feedback," *Proc. IEEE*, vol. 51, no. 11, pp. 1524 – 1535, November 1963.

[147] H. L. Fiedler and B. Hoefflinger, "A CMOS pulse density modulator for high-resolution A/D converters," *IEEE J. Solid State Circuits*, vol. 16, no. 6, pp. 995-996, December 1984.

[148] P. J. Crawley and G. W. Roberts, "Switched-current sigma-delta modulation for A/D conversion," in *Proc. IEEE Int. Symp. On Circuits and Systems*, vol. 3, pp. 1320 - 1323, May 1992.

[149] I. Galton, "Delta-Sigma Data Conversion in Wireless Transceivers," *IEEE Trans. on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 302-316, January 2002.

[150] J. T. Caves, M. A. Copeland, C. F. Rahim and S. D. Rosenbaum, "Sampled analog fiitering using switched capacitors as resistor equivalents," *IEEE J. Solid-State Circuits*, vol. SC-I 2, pp. 592- 599, December 1977.

[151] B. J. Hosticka, R. W. Brodersen and P. R. Gray, "MOS sampled data recursive filters using switched capacitor integrators," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 600-608, December. 1977.

[152] L. Dörrer, F. Kuttner, P. Greco, P. Torta and T. Hartig, "A 3-mW 74-dB SNR 2-MHz Continuous-Time Delta-Sigma ADC With a Tracking ADC Quantizer in 0.13-μm CMOS," *IEEE J. Solid State Circuits*, vol. 40, no. 12, pp. 2416 - 2427, December 2005.

[153] D.A. Kerth, D.B. Kasha, T.G. Mellissinos, D.S. Piasecki and E.J. Swanson, "A 126 dB linear switched-capacitor delta-sigma modulator," *ISSCC' 94 Dig. Tech. Papers*, vol. 1, pp. 196-197, February 1994.

[154] A. Prasad, A. Chokhawala, K. Thompson and J. Melanson, "A 120dB 300mW stereo audio A/D converter with 110dB THD+N," *in Proc. ESSCIRC '04*, vol. 1, pp. 191 – 194, September 2004.

[155] Richard Schreier and Gabor C. Temes, *Understanding Delts-Sigma Data Converters*, (IEEE press and John Wiley & Sons, Inc, 2005).

[156] W. Chou, P. W. Wong and R. M. Gray, "Multistage Sigma-Delta Modulation," *IEEE Trans. Information Theory*, vol. 35, no. 4, pp. 784 – 796, July 1989.

[157] K. C. H. Chao, S. Nadeem, W. L. Lee and C. G. Sodini, "A higher order topology for interpolative modulators for oversampling A/D conversion," *IEEE TCAS*, vol. 37, no. 3, pp. 309 – 318, March 1990.

[158] T. Ritoniemi, T. Karema and H. Tenhunen, "Design of stable high order 1-bit sigma-delta modulators," *Proc. IEEE Int. Symp. On Circuits and Systems*, vol. 4, pp. 3267 - 3270, May 1990.

[159] S. Ardalan and J. Paulos, "An analysis of nonlinear behavior in delta - sigma modulators," *IEEE TCAS*, vol. 34, no. 6, pp. 593 – 603, June 1987.

[160] L. Risbo, "Stability predictions for high-order ΣΔ modulators based on quasilinear modelling," *Proc. IEEE Int. Symp. On Circuits and Systems*, vol. 1, pp. 361 - 364, June 1994.

[161] Y. Matsuya et al., "A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping," *IEEE J. Solid-State Circuits*, vol. 22, pp. 921–929, December 1987.

[162] L. Longo and M. A. Copeland, "A 13-bit ISDN-band ADC using two-stage third-order noise shaping," in *Proc. Custom Integrated Circuit Conf.*, pp. 21.2.1–21.2.4, June 1988.

[163] D. B. Ribner, "A comparison of modulator networks for high-order oversampled ΣΔ analog-to-digital converters," *IEEE Trans. Circuits Systems*, vol. 38, pp. 145–159, February 1991.

[164] G. M. Yin, F. Stubbe, and W. Sansen, "A 16-bit 320 kHz CMOS A/D converter using 2-stage 3rd-order ΣΔ noise-shaping," *IEEE J. Solid-State Circuits*, vol. 28, pp. 640–647, June 1993.

[165] I. Dedic, "A sixth-order triple-loop ΣΔ CMOS ADC with 90 dB SNR and 100 kHz bandwidth," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1994, pp. 188–189, February 1994.

[166] T. Karema, T. Ritoniemi, and H. Tenhunen, "An oversampled sigmadelta A/D converter circuit using two-stage fourth-order modulator," *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 3279–3282, May 1990.

[167] K.-Y. Nam, S.-M. Lee, D. K. Su and B.A. Wooley, "A Low-Voltage Low-Power Sigma-Delta modulator for Broadband Analog-to-Digital Conversion," *IEEE J. Solid State Circuits*, vol. 40, no. 9, pp. 1855-1864, September 2005.

[168] A. Q. Safarian, M. B. Vahidfar, H. Aslanzadeh and S. Mehrmanesh, "A new low power 2-2 cascaded sigma-delta modulator with the reduced number of op-amps for GSM transceiver applications," *in Proc. IEEE ICECS*, vol. 1, pp. 268 – 271, December 2003.

[169] T. L. Brooks, D. H. Robertson, D. F. Kelly, A. D.-Muro and S. W. Harston, "A cascaded sigma–delta pipeline A/D converter with 1.25 MHz signal bandwidth and 89dB SNR," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1896–1906, December 1997.

[170] Y. Geerts, A. M. Marques, M. S. J. Steyaert and W. Sansen, "A 3.3-V, 15-bit, Delta–Sigma ADC with a Signal Bandwidth of 1.1 MHz for ADSL Applications," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 927–936, July 1999.

[171] F. Medeiro, B. P´erez-Verd´u, J. Manuel de la Rosa and A. Rodr´ıguez-V´azquez, "Fourth-Order Cascade SC ΣΔ modulators: A Comparative Study, " *IEEE TCAS-I, Fundamental Theory and Applications*, vol. 45, no. 10, pp. 1041 – 1051, October 1998

[172] T.C.; Leslie and B. Singh, "An improved sigma-delta modulator architecture," *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 372–375, May 1990.

[173] T. Hayashi, Y. Inabe, K. Uchimura and A. Iwata, "A multistage delta-sigma modulator without double integration loop," *ISSCC Dig. Tech. Papers*, vol. 1, pp. 182-183, February 1986.

[174] Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa and T. Yoshitome, "A 16-bit oversampled A-to-D conversion technology using triple integration noise shaping," *IEEE J. Solid-State Circuits*, vol. 22, no. 12, pp. 921–929, December 1987.

[175] J. C. Candy and A. Huynh, "Double integration for digital-to-analog conversion," *IEEE Trans. Communications*, vol. 34, no. 1, pp. 77 – 81, January 1986.

[176] L. E. Larson, T. Cataltepe and G. C. Temes, "Multibit oversampled Σ-Δ A/D convertor with digital error correction," *Electronic Letters*, vol. 24, no. 16, pp. 1051 – 1052, August 1998.

[177] L. R. Carey, "A noise shaping coder topology for 15+ bit converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 4, pp. 267–273, April 1989.

[178] M. J. Story, "Digital to analogue converter adapted to select input sources based on a preselected algorithm once per cycle of a sampling signal," U.S. patent number 5138317, August 11 1992 (filed February 10 1989).

[179] R. T. Baird and T. S. Fiez, "Improved ΣΔ DAC linearity using data weighted averaging," in *Proc. ISCAS*, vol. 1, pp. 13 – 16, May 1995.

[180] I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, C. Jun and S. L. Chan, "A 90-dB SNR 2.5 MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8x oversampling ratio," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820–1828, December 2000.

[181] Y.-In. Park; S. Karthikeyan, W. M. Koe, Z. Jiang and T.-C. Tan, "A 16-bit, 5 MHz multi-bit sigma-delta ADC using adaptively randomized DWA," in *Proc. IEEE CICCI*, vol. 1, pp. 115 – 118, April 1995.

[182] F. Chen and B. H. Leung, "A high resolution multi-bit ΣΔ ADC with digital correction and relaxed amplifier requirements," *IEEE J. Solid-State Circuits*, vol. 30, no. 4, pp. 453–460, December 2000.

[183] R. Schreier and B. Zhang, "Noise-shaped multibit D/A convertor employing unit elements," *Electronic Letters*, vol. 31, no. 20, pp. 1712 – 1713, September 28 1995.

[184] I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," IEEE TCAS-II, vol. 44, pp. 808 – 817, October 1997.

[185] K. Vleugels, S. Rabii, and B. A. Wooley, "A 2.5-V Sigma–Delta modulator for broadband communications applications," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1887–1899, December 2001.

[186] M. de Wit, "Sample and hold circuitry and methods," U.S. Patent 5170075, December 8, 1992.

[187] J. R. Naylor, M. A. Shill, "Bootstrapped FET Sampling Switch," U.S. Patent 5172019, December 15 1992.

[188] H. Pan, M. Segami, M. Choi, J. Cao, and A. A. Abidi, "A 3.3-V 12-b 50-MS/s A/D converter in 0.6μm CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1769–1780, December 2000.

[189] B. Razavi, "*Design of Analog CMOS Integrated Circuits*," McGraw Hill Publishing Company Inc. 2001.

[190] D.G. Haigh and J.T. Taylor, "On switch-induced distortion in switched capacitor circuits," in *Proc. IEEE ISCAS*, vol. 3, pp. 1987 – 1990, June 1988.

[191] Y.-P. Xu, G. Rigby, M. Starr, "Effect of switch charge injection on ΣΔ modulator," *IEEE International Conference on Microelectronics and VLSI*, vol. 1, pp. 131 – 134, November 1995.

[192] S. K. Gupta and V. Fong, "A 64-MHz Clock-Rate ΣΔ ADC With 88-dB SNDR and 105-dB IM3 Distortion at a 1.5-MHz Signal Frequency," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1653 - 1661, December 2002.

[193] W. Yang, D. Kelly, I. Mehr, M.T. Sayuk and L. Singer, "A 3-V 340mW 14-b 75-Msample/s CMOS ADC with 85 dB SFDR at Nyquist input," *IEEE J. Solid State Circuits*, vol. 36, no. 12, pp. 1931-1936, December 2001.

[194] R. Moazzami and C. Hu, "Projecting oxide reliability and optimizing reliability screens," *IEEE Trans. Electron Devices*, vol. 37, no. 7, pp. 1643 - 1650, July 1990.

[195] N. Klemmer and E. Hegazi, "A DLL-Biased, 14-Bit DS Analog-to-Digital Converter for GSM/GPRS/EDGE Handsets," *IEEE J. Solid State Circuits*, vol. 41, no. 2, pp. 330-338, February 2006.

[196] M. Safi-Harb and G. W. Roberts, "Low Power Delta–Sigma Modulator for ADSL Applications in a Low-Voltage CMOS Technology," *IEEE TCAS-I-Regular Papers*, vol. 52, no. 10, pp. 2075 – 2089, October 2005.

[197] R. Gaggl, A. Wiesbauer, G. Fritz, C. Schranz and Peter Pessl, "A 85-dB Dynamic Range Multibit Delta–Sigma ADC for ADSL-CO Applications in 0.18-μm CMOS," *IEEE J. Solid State Circuits*, vol. 38, no. 7, pp. 1105-1114, July 2003.

[198] J. Grilo, Member, I. Galton, K. Wang and R. G. Montemayor, "A 12-mW ADC Delta–Sigma Modulator With 80 dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver," *IEEE J. Solid State Circuits*, vol. 37, no. 3, pp. 271-278, March 2002.

[199] A. Zahabi, O. Shoaei, Y. Koolivand and P. Jabehdar-Maralani, "A Low-Power ΔΣ Modulator with Low Capacitor Spread for Multi-Standard Receiver Applications," in *Proc. ISCAS*, vol. 4 pp. 3107-3110, May 2005.

[200] R. Jiang and T. S. Fiez, "A 1.8V 14b ΔΣ A/D Converter with 4MSamples/s Conversion," *ISSCC Dig. Tech. Papers*, vol. 1, pp. 220-461, February 2002.

[201] L. Yao, M. Steyaert and W. Sansen, "A 1-V, 1-MS/s, 88-dB Sigma-Delta Modulator in 0.13-μm Digital CMOS Technology," in *Proc. IEEE SVLSIC Dig. Tech. Papers*, vol. 1, pp. 180 – 183, June 2005.

[202] R. Del-Rio, F. Medeiro, J.M. de la Rosa, B. Perez-Verdu, A. Rodriguez-Vazquez, "A 2.5-V ΣΔ modulator in 0.25-μm CMOS for ADSL," in *Proc. ISCAS*, vol. 3 pp. 301-304, May 2002.

[203] K.C. Dyer, D. Fu, S.H. Lewis and P. J. Hurst, "An analog background calibration technique for time-interleaved analog-to-digital converters," *IEEE J. Solid State Circuits*, vol. 33, no. 12, pp. 1912-1919, December 1998.

[204] D. Fu, K. C. Dyer, S. H. Lewis and P. J. Hurst, "A digital background calibration technique for time-interleaved analog-to-digital converters," *IEEE J. Solid State Circuits*, vol. 33, no. 12, pp. 1904-1911, December 1998.

[205] D-Y. Chang, J. Li and U-K. Moon, "Radix-Based Digital Calibration Techniques for Multi-Stage Recycling Pipelined ADCs", *IEEE TCAS-I-Regular Papers*, vol. 51, no. 11, November 2004.

[206] J. Li and U-K. Moon, "Background Calibration Techniques for Multistage Pipelined ADCs with Digital Redundancy", *IEEE TCAS-II-Analog and Digital Signal Processing*, vol. 50, no. 9, September 2003.

[207] J. P. Keane, P. J. Hurst and S. H. Lewis, "Background Interstage Gain Calibration Technique for Pipelined ADCs", *IEEE TCAS-I-Regular Papers*, vol. 52, no. 1, January 2005.

[208] R. G. Massolini, G. Cesura and R. Castello, "A Fully Digital Fast Convergence Algorithm for Non-Linearity Correction in Multistage ADC", *IEEE TCAS-II*, 2006.

[209] K. El-Sankary and M. Sawan, "A Background Calibration Technique for Multibit/Stage Pipelined and Time-Interleaved ADCs", *IEEE TCAS-II*, 2006.

[210] C. R. Grace, P. J. Hurst and S. H. Lewis, "A 12-bit 80-Msample/s pipelined ADC with bootstrapped digital calibration," *IEEE J. Solid State Circuits*, vol. 40, no. 5, pp. 1038-1046, May 2005.

[211] K. El-Sankary and M. Sawan, "A Digital Blind Background Capacitor Mismatch Calibration Technique for Pipelined ADC", *IEEE TCAS-II-Express Briefs*, vol. 51, no. 10, October 2004.

[212] A. Shabra and H.-S. Lee, "Oversampled A/D Converters with mismatch shaping," *IEEE J. Solid State Circuits*, vol. 40, no. 5, pp. 1038-1046, May 2005.

[213] I. Galton, "Digital Cancellation of D/A Converter Noise in Pipelined A/D Converter", *IEEE TCAS-II-Analog and Digital Signal Processing*, vol. 47, no. 3, pp. 185 – 196, March 2000.

[214] S-T. Ryu, S. Ray, B-S. Song, G-H. Cho and K. Bacrania, "A 14-b linear capacitor self-trimming pipelined ADC," *IEEE J. Solid State Circuits*, vol. 39, no. 11, pp. 2046-2051, November 2004.

[215] H. S. Lee, D. A. Hodges and P. R. Gray, "A self calibrated 15 bit CMOS A/D converter," *IEEE J. Solid State Circuits*, vol. SC-19, no. 6, pp. 813-819, December 1984.

[216] Y.-M. Lin, B. Kim, P. R. Gray, "A 13-b 2.5-MHz Self-Calibrated Pipelined A/D Converter in 3-μm CMOS", *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 628-636, April 1991.

[217] J. Goes, J. C. Vital, L. Alves, N, Ferreira, P. Ventura, E. Bach, J. E. Franca, R. Koch, "A low-power 14-b 5 MS/s CMOS pipeline ADC with background analog self-calibration", in *Proc. ESSCIRC*, vol. 1 pp. 172-175, September 2000.

[218] O. A. Adeniran and A. Demosthenous, "Optimization of bits-per-stage for low-voltage low-power pipeline ADCs," in *Proc. ECCTD*, vol. 2 pp. 55-58, August 2005.

[219] T. Kuyel and F. Tsay, "Optimal analog trim techniques for improving the linearity of pipeline ADCs," in *Proc. International Test Conference*, vol. 1, pp. 367 – 375, October 2000.

[220] E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Trans. Acoustics, Speech, and Signal Processing*, vol. 29, no. 2, pp. 155 – 162, April 1981.