

A Vestibular Prosthesis With Highly-Isolated Parallel Multichannel Stimulation

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Abstract—This paper presents an implantable vestibular stimulation system capable of providing high flexibility independent parallel stimulation to the semicircular canals in the inner ear for restoring three-dimensional sensation of head movements. To minimize channel interaction during parallel stimulation, the system is implemented with a power isolation method for crosstalk reduction. Experimental results demonstrate that, with this method, electrodes for different stimulation channels located in close proximity (<2 mm) can deliver current pulses simultaneously with minimum inter-channel crosstalk. The design features a memory-based scheme that manages stimulation to the three canals in parallel. A vestibular evoked potential (VEP) recording unit is included for closed-loop adaptive stimulation control. The main components of the prototype vestibular prosthesis are three ASICs, all implemented in a $0.6\text{-}\mu\text{m}$ high-voltage CMOS technology. The measured performance was verified using vestibular electrodes *in vitro*.

Index Terms—Application specific integrated circuit (ASIC), crosstalk, implanted device, parallel stimulation, power isolation, stimulation control, vestibular evoked potential (VEP) recording, vestibular prosthesis.

I. INTRODUCTION

THE vestibular system is a sensory organ located in the inner ear providing cues about head motion for stabilizing vision and keeping balance. People with bilateral vestibular deficiency may suffer from postural instability, chronic disequilibrium, oscillopsia, etc. Physiological research shows that this population could benefit from implantable vestibular prostheses. The early development of sensor-based vestibular prostheses [1], [2] has now progressed to such areas as hardware design [1]–[10], motion signal encoding and processing [11]–[15] and labyrinth modeling [16]. These prototypes have been tested on various animals and vestibulo-ocular reflexes (VORs) by modulated electrical stimuli have been observed. The directions of VOR are correlated with the sensitive axis of the particular semicircular canal afferent being stimulated

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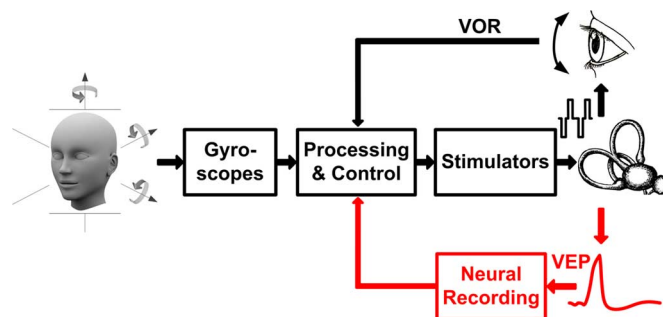


Fig. 1. Conceptual structure of a closed-loop vestibular prosthesis.

[1]–[4], [17]–[20]. Recent trials on humans also showed the same stimulation effects [21], [22]. These results suggest that refining the prototypes into suitable clinical devices for treating severe vestibular disorders is feasible.

The structures of these prototypes are similar. They comprise gyroscopes, processing and control units and stimulator units including electrode arrays, as shown in Fig. 1. The gyroscopes collect head rotation data and the processing and control units transduce this data into modulated current pulses that are generated by the stimulator. The current pulses individually target each of the three semicircular canals via the electrode arrays implanted near the vestibular nerves in order to restore rotational sensation in three-dimensions (3D).

A dynamic feedback path with minimum delay is necessary for evaluating the stimulator performance as well as for optimizing stimulation. Since for decades VOR has been used as a primary metric in clinics for diagnosing vestibular disorders [23], [24], it was naturally adopted in most previous studies for measuring the functional efficacy of stimulation and for optimizing stimulation [11]–[13]. The limitation of VOR in clinical applications, however, is evident. Measurement of VOR is difficult outside a lab or clinical environment. Furthermore, VOR can change because of its adaptive plasticity, changes in the integrity of the electrode arrays or changes in the innervation of the ampullae [25]. Recently investigation has started to characterize the vestibular evoked potential (VEP) in the hope of using it as a more direct metric of vestibular function, which could be used in combination with VOR for a “closed-loop” style adaptive stimulation control [25]–[27].

Results from *in vivo* studies have shown that the performance of vestibular prostheses can be significantly undermined by misalignment between the perception of rotational axes created from stimulation and the actual axes of head rotation [3]. There are three major causes of misalignment: i) mismatch after implantation between the rotational axes of the gyroscopes and

the axes of perception setup from the previously functional canals; ii) current spread from one canal to the others; and iii) errors resulting from signal processing and stimulation control. Several misalignment reduction methods have been proposed, including pre-compensation by feedback recorded VOR into modulation control to compensate measured misalignment [11]–[13], current focusing by using bipolar instead of monopolar electrode arrangements [4] to reduce current spread, and improved techniques in electrode fabrication [4], [28], [29] and surgical placement [21], [22] enabling the stimulation sites to be as close as possible to the targeted nerves. These methods, however, do not address misalignment as a result of limitations in sequential stimulation, as used in most previously reported prototype multichannel vestibular stimulators [3], [4], [6], [30], where the three canals are stimulated one at a time. Sequential stimulation inevitably correlates the stimulating currents in the three canals, whereas the stimulation should ideally be independent with regard to each other in order to create a real 3D sensation. Parallel stimulation is preferable for minimizing misalignment, but two major design challenges exist in its implementation: i) the use of stimulation control where the stimulators are managed sequentially by the processor, especially when the management is via a shared wireless serial data link; and ii) crosstalk between stimulation channels (canals).

The 3-channel stimulation system presented in this paper is part of a collaborative effort to develop an implantable closed-loop vestibular prosthesis.¹ The authors' first generation stimulator design [7] has been enhanced with techniques for implementing parallel stimulation and the incorporation of a recording unit to facilitate closed-loop feedback. The two design challenges previously mentioned are addressed using parallel stimulation management and power isolation for each canal. The implantable stimulation system interfaces with a telemetry unit that provides wireless power and data transmission over an inductive link from an external transmitter [9]. The work is an expansion of [8] and presents comprehensive design details and measured results.

The remaining sections of the paper are organized as follows. Section II discusses considerations for the implementation of parallel stimulation in terms of stimulation control and crosstalk. Section III presents an overview of the developed system, and Section IV explains the method of stimulation and recording control. Section V describes the method of power isolation for crosstalk reduction. The performance of the system is demonstrated with *in vitro* measurements presented in Section VI, followed by concluding remarks in Section VII.

II. CONSIDERATIONS FOR PARALLEL STIMULATION

The ultimate goal of vestibular prostheses is to accurately encode head motion with optimally modulated stimulation, so that sensation of motion can be created with minimum distortion. Pulse rate modulation has been the most favored scheme for encoding head rotation [1]–[4], [17]–[19], sometimes with pulse amplitude modulation as a supplement [15], because it mimics

the natural encoding method where the angular velocity is encoded with the firing rate. *In vivo* experiments in [1] mapped the angular velocity of horizontal head motion ranging between $\pm 500^\circ/\text{s}$ to a pulse rate between 50–250 pps, with a base rate of 150 pps. The base rate was later raised to 200 pps [22] and 250 pps [17] to allow a more symmetrical pulse rate dynamic range between 0–500 pps. Recent research has shown that, in addition to pulse rate, pulse timing may also be an important factor in encoding head motion [31]. When encoding 3D head rotation, the pulse rate and pulse onset timing for one canal should be independent of those of the other canals (the three canals are orthogonally located). However, it is not possible to provide this independence in conventional multichannel stimulators.

In multichannel stimulators used in cochlear implants [32], [33], stimulation of the channels is performed sequentially. Sequential stimulation has been successful in cochlear implants where amplitude modulation is used for encoding audio signals. In vestibular stimulation where pulses overlap between channels, sequential operation results in pulse rate errors, affecting the accuracy of encoding head motion. The natural perception threshold to angular velocity is around $4^\circ/\text{s}$ [31], and the modulation gain of prototype vestibular stimulators is 1–3 pps/($^\circ/\text{s}$) [1], [2]. Therefore, the pulse rate deviation should not exceed 4–12 pps to avoid misalignment. On the other hand, the widths of biphasic pulses commonly used in vestibular stimulation are in the region of 100–200 μs [1]–[4], [7], [8], [17]–[19], [22], [30], yielding a potential delay of 300–600 μs . In sequential stimulation, a delay of such length may greatly alter the pulse rate. For example, where there is a pulse rate of 500 pps (2 ms period), such a delay increases the period to 2.3–2.6 ms (i.e., 384.6–434.8 pps). This is significantly larger than the acceptable frequency error. The accumulative frequency error may be corrected by compensation algorithms, but the demand for accurate encoding imposes a significant challenge in signal processing. Parallel stimulation would avoid these complications.

Parallel stimulation requires that in multiple channels the stimulator be capable of tolerating pulse overlaps. In such a situation, stimulation control and crosstalk present problems when using a conventional sequential system. In most cochlear implants [33] and previously reported vestibular stimulators, the processor directly initiates each pulse to each channel (or canal in case of vestibular stimulators). As illustrated in Fig. 2(a), the processor starts a pulse by sending a command frame containing settings for the pulse profile, while the pulse rate is decided by the interval between frames for the same channel. Despite its advantage in precise control of the pulse onset, sequential stimulation cannot deal with pulse overlaps between channels, especially if the processor connects to the stimulators via a serial data link such as in cochlear implants. A major reason for sequential stimulation is to prevent crosstalk between channels. In Fig. 3(a), when *Canal A* is active for stimulation, *Canal B* is isolated from the power supply and current source via switches S_{B1} and S_{B2} , so that the current is more focused between the stimulation sites in *Canal A*. To achieve better current focusing, a number of electrode topologies have been used, including bipolar, tripolar [4] and hexagonal mosaics as a guard ring [34]. For vestibular stimulators, however,

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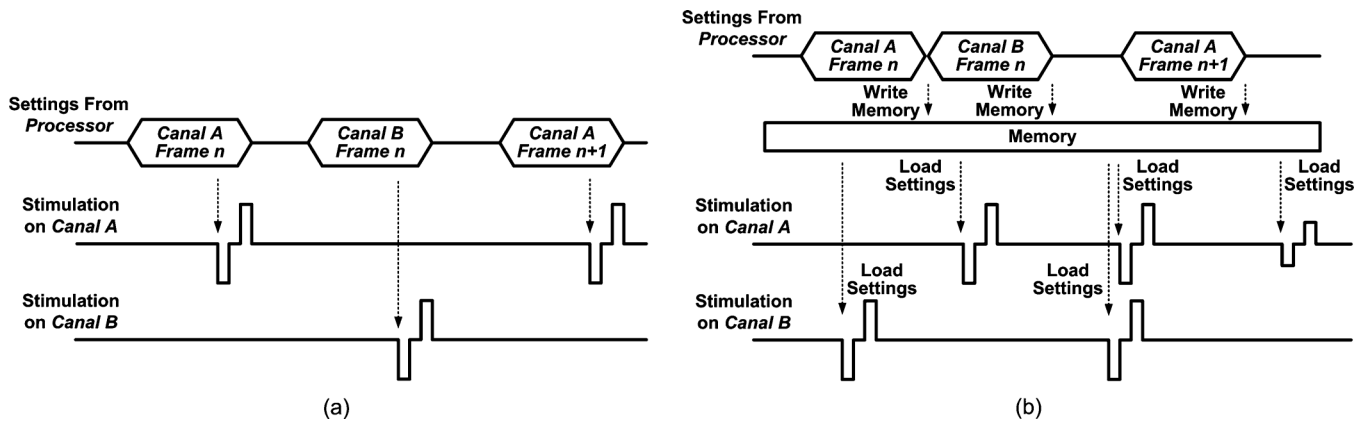


Fig. 2. Stimulation control methods. (a) Sequential arrangement. (b) Parallel arrangement.

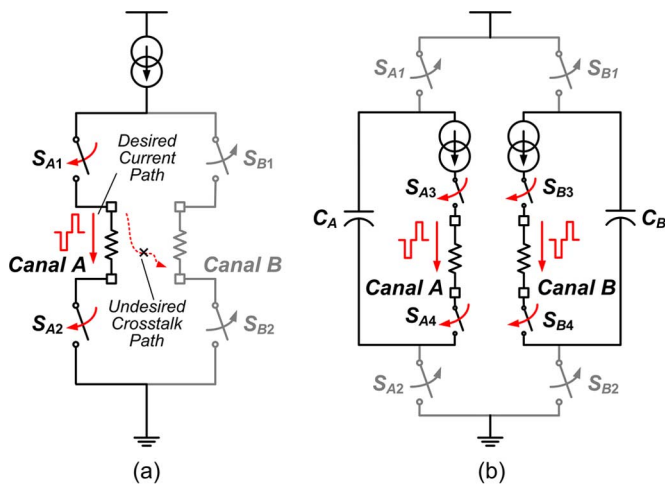


Fig. 3. Methods for crosstalk reduction. (a) Sequential stimulation, where the undesired crosstalk path is removed by stimulating only one canal at a time. (b) Power isolation, where a stimulator is isolated from other stimulators and supplied by stored charge, allowing parallel multichannel stimulation.

the challenge is that the available space for electrode arrays in each canal is very restricted and the distance between the canals where it is suitable for implantation is very small (~ 2 mm). As a result the electrode arrangement does not provide sufficient isolation for parallel stimulation.

For multichannel vestibular stimulation capable of parallel stimulation an alternative system is proposed here with two main features:

- Implementation of a two-stage stimulation control where the operation of real-time stimulation control is split into two parallel units, one in the processor, and the other in a stimulation management unit in the implant. The two units are interfaced with a memory block, as illustrated in Fig. 2(b). All the settings for the pulse profile to one canal, including the pulse rate, are sent to the stimulation management unit where they are stored in memory. For each canal, the corresponding state machine in the management unit repeatedly loads the settings from the memory at the onset of each pulse and generates a pulse accordingly. With this arrangement, the onset of pulses is decoupled from the timing of frames. Instead, they are initiated

by parallel state machines in the management unit. Hence, the stimulation is also parallel. Modulation to one canal is achieved by sending a new frame to update the pulse profile, as in the case of *Canal A* illustrated in Fig. 2(b).

- Implementation of a power isolation stimulation method for crosstalk reduction using capacitors as proposed in [35]. Instead of temporarily separating the stimulation on the canals, the power supply for each canal during stimulation is separated. As illustrated in Fig. 3(b), each canal is assigned a stimulator with its own capacitor for energy storage. When *Canal A* is stimulated, for example, switches S_{A1} and S_{A2} are off so that the current source and the electrodes in *Canal A* are isolated from the rest of the system and are instead supplied by the charge stored in capacitor C_A . During the pulse interval, the storage capacitor is charged while the electrodes are isolated via switches S_{A3} and S_{A4} . As a result the electrodes are always isolated from the power rails, and the canals are floating with respect to each other during stimulation. Thus, parallel stimulation is possible without significant crosstalk.

III. SYSTEM OVERVIEW

The architecture of the developed vestibular prosthesis is shown in Fig. 4. The system consists of a head-mount unit and an implant unit. The head-mount unit detects head rotation with an on-board gyroscope and accordingly calculates the parameters for stimulation in a microprocessor. The gyroscope sensors and the algorithms for processing their outputs are outlined in [36]. The transmitter in the head-mount unit contains a class-*D* amplifier which drives the primary coil in the inductive link with a carrier signal at 13.56 MHz to power the implant. The inductive link also serves as a bi-directional half-duplex communication link. The command frames from the processor to the implant for setting the stimulation characteristics are sent via downlink transmission whose carrier is modulated by amplitude shift keying (ASK) at 400 kbit/s. The uplink transmission uses passive phase shift keying (PPSK) modulation with a data rate of 600 kbit/s. Details of the telemetry design can be found in [9], [37].

The implant has a 12 V supply derived from the secondary coil in the inductive link. In the implementation of the power

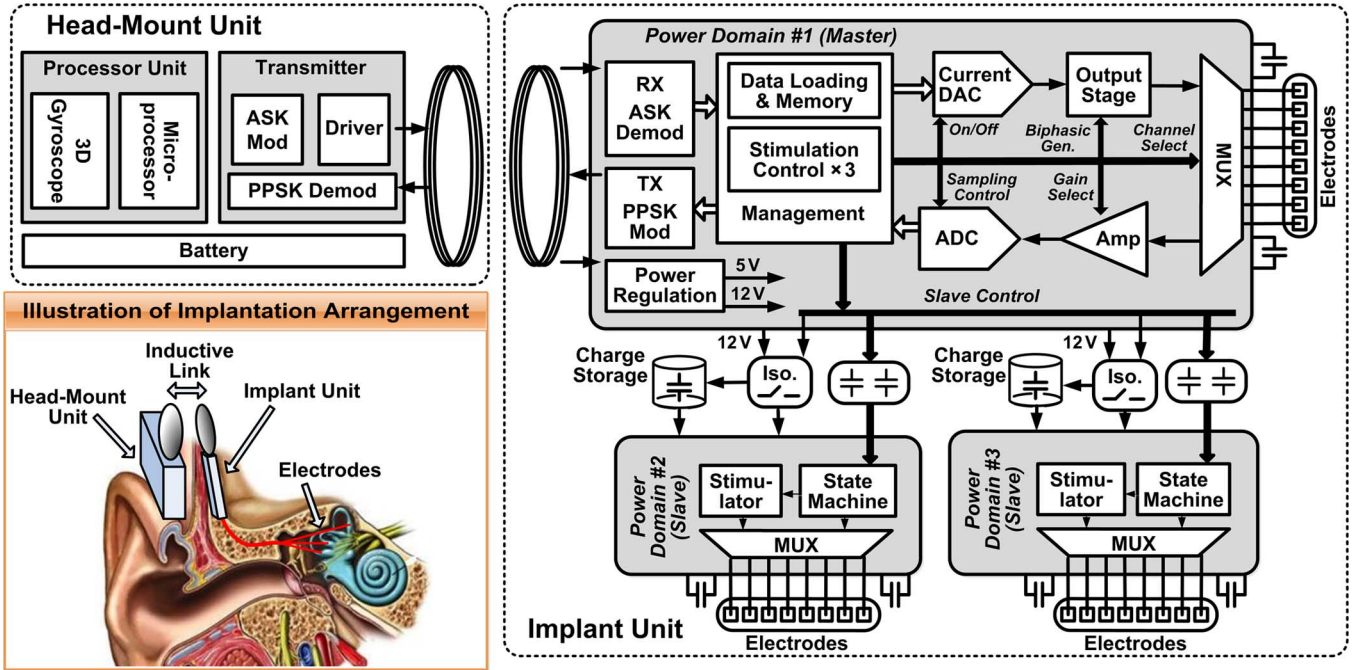


Fig. 4. Architecture of the prototype vestibular prosthesis. The insert illustrates the implantation arrangement.

isolation method, the implant is separated into three power domains as illustrated in Fig. 4. *Power Domain #1* has the 12 V supply and the other two domains (*Power Domain #2*, *Power Domain #3*) are connected to the 12 V supply via isolation switches. There are three stimulators (a master and two slaves), each consisting of an 8-bit current digital-to-analog converter (DAC) and an output stage. Each stimulator is connected to an array of 8 electrodes [28], [29] targeting the three canals. Each slave has its individual power source supplied from a charge storage capacitor. Both the master and slaves have 5 V regulators to supply the low voltage circuits.

The parallel operation of all three stimulators is controlled by the management unit in *Power Domain #1*. The management unit loads demodulated command frames from the processor in the head-mount unit and stores them in the built-in memory. Control of the stimulator in *Power Domain #1* additionally manages the amplifier and analog-to-digital converter (ADC) in the recording unit. Each stimulus pulse from a slave stimulator is initiated by the management unit through capacitive coupled data links. Before the onset of a stimulus pulse, the management unit turns off the isolation switches (Iso.). On the completion of a pulse, the management unit turns on the isolation switches to recharge the storage capacitor.

IV. STIMULATION AND RECORDING MANAGEMENT

The stimulation management unit (an improved version of [7]) comprises three sections, namely, data loading, memory and stimulation control (Fig. 4). Data loading receives command frames from the ASK demodulator [37]. After extracting the compressed pulse interval parameters [7] and verifying the validity of the settings such as maximum charge, the settings are stored in a memory slot according to the address value, including the *Canal ID* and *Packet ID*.

The structure of a command frame is shown in Fig. 5. Unlike the arrangement in [7], the settings for each stimulator (hence each canal) are separated into four 16-bit packets and distributed to four command frames. This allows improvement of the speed of updating stimulation settings. The command frames are sent only when stimulation parameters change. In most cases the pulse modulation does not need to change all the parameters at once. For example, pulse rate modulation only requires *Packet 3* to be updated repeatedly. The external processor can decide which packets to send when an update is needed, distinguished by the *Packet ID*. The *State* indicator informs the data loading unit whether it is a full update with all the four packets needed or a partial update with fewer packets. If the value of *State* is “00”, the data loading unit waits for more command frames to complete the update. If it is “01”, the data loading unit updates the memory after the current command frame. Data verification is always carried out with all the setting parameters. In the case of a partial update, the data loading unit retrieves the unchanged stimulation parameters from the memory to verify the new parameters. With this arrangement, one command frame contains 23 bits. It takes only $57.5 \mu\text{s}$ to transfer the information over the downlink (with a data rate of 400 kbit/s).

Each of the three parallel stimulator control units loads the settings at the onset of a pulse cycle, i.e., the time instant when the pulse interval counter (PIC) reaches zero. At this point, PIC loads the pulse interval setting from the memory and starts to count down. Concurrently the stimulation control state machine programs the pulse profiles and selects stimulating electrodes. If recording is activated by the value of the recording indicator, *Rec*, settings are also loaded for the masker-probe interval (MPI), sampling delay, amplifier gain and length of the recording window. Subsequently the state machine moves to the pulse generation (masker) state. This state consists of a chain

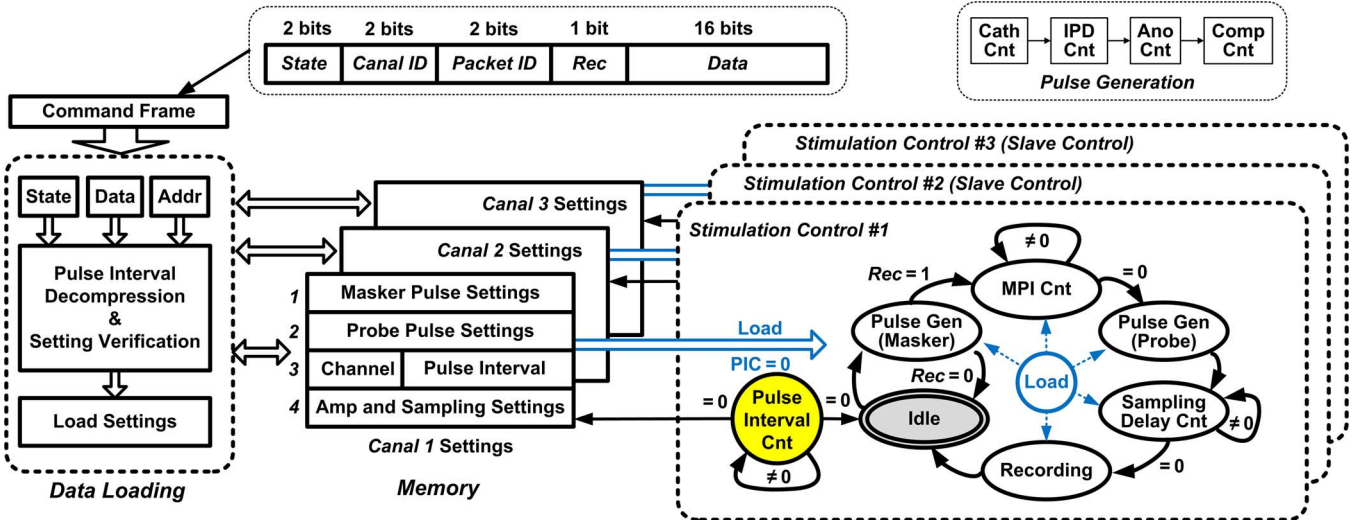


Fig. 5. Stimulation management unit.

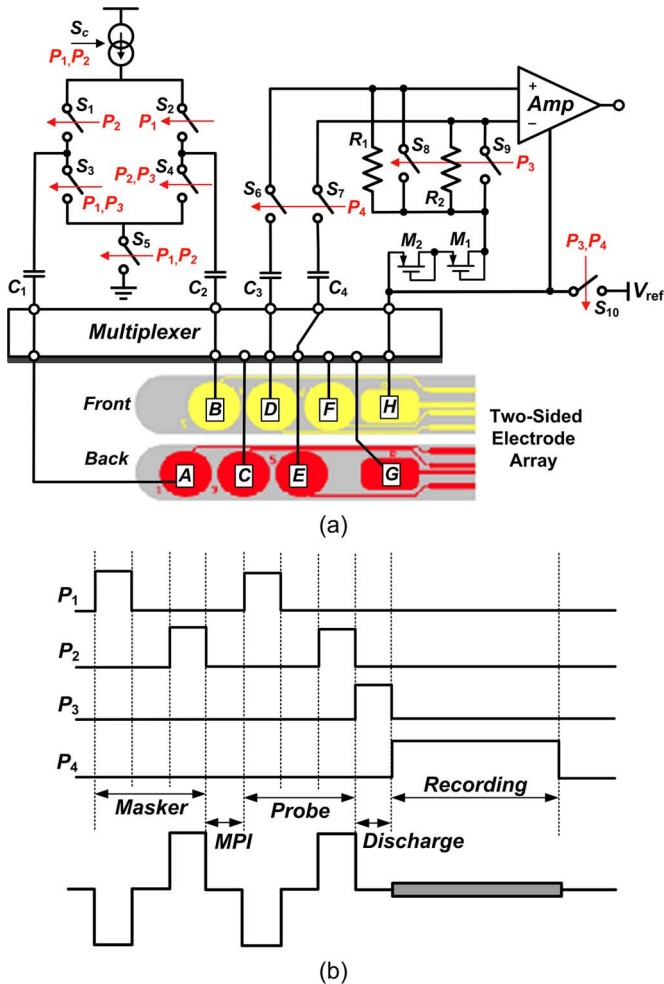


Fig. 6. Operation of stimulation and recording. (a) Circuit of the output stage. (b) Time sequence for stimulation and recording.

of four countdown counters allocated to the cathodic phase, inter-phase delay, anodic phase and active charge compensation phase, as described in [7]. The pulse generation state provides control signals P_1 and P_2 that control the switches in the

output stage, as shown in Fig. 6(a), to generate a biphasic stimulus pulse. After this state, depending on the value of Rec , the state machine either returns to idle waiting for PIC to reach zero again, or enters the recording phase.

The recording unit is designed to acquire the vestibular evoked potential (VEP) after each stimulating pulse. The VEP is digitized and uploaded to the (external) controller. Although the study of characterizing VEP is in its infancy [25]–[27], initial results from *in vivo* tests provide useful information for further refinement of the recording unit specifications. Similar to cochlear implants [33], recording in this prosthesis is implemented with the forward-masking technique for artifact reduction [38], where a probe pulse follows the masker pulse after a short interval. The circuit for the probe pulse generation is identical to the one for masker pulse generation. From the results in [26], [27], the recording unit is designed to accommodate input signals between $2 \mu\text{V}$ and 1mV . Acute response occurs a few hundred microseconds after the onset of a stimulation pulse, while long-latency response can peak later than 10ms after the pulse onset. The *in vivo* study also suggests that a minimum sampling rate of 20kS/s and a 10-bit resolution is necessary. The recording arrangement is shown in Fig. 6(a), and the time sequence of stimulation and recording is shown in Fig. 6(b). In order to avoid saturation of the amplifier, there is a programmable delay of up to $250 \mu\text{s}$ between the completion of the probe pulse and the start of the recording window. During this delay, the control signal P_3 goes high to discharge the stimulating electrodes and short the amplifier inputs to an on-chip 2.5V voltage reference (V_{ref}). After this delay, the amplifier inputs are connected to the selected recording sites by the control signal P_4 and the ADC samples the amplifier output every $50 \mu\text{s}$. The length of the recording window is up to 19.2ms . In the example shown in Fig. 6(a), electrode sites A and B are selected for stimulation, D and E for recording, and with H as reference. The 8-bit current DAC and the output stage are described in detail in [7]. The programmable two-stage amplifier has a bandwidth between 100Hz and 7.5kHz . The amplifier design can be found in [39].

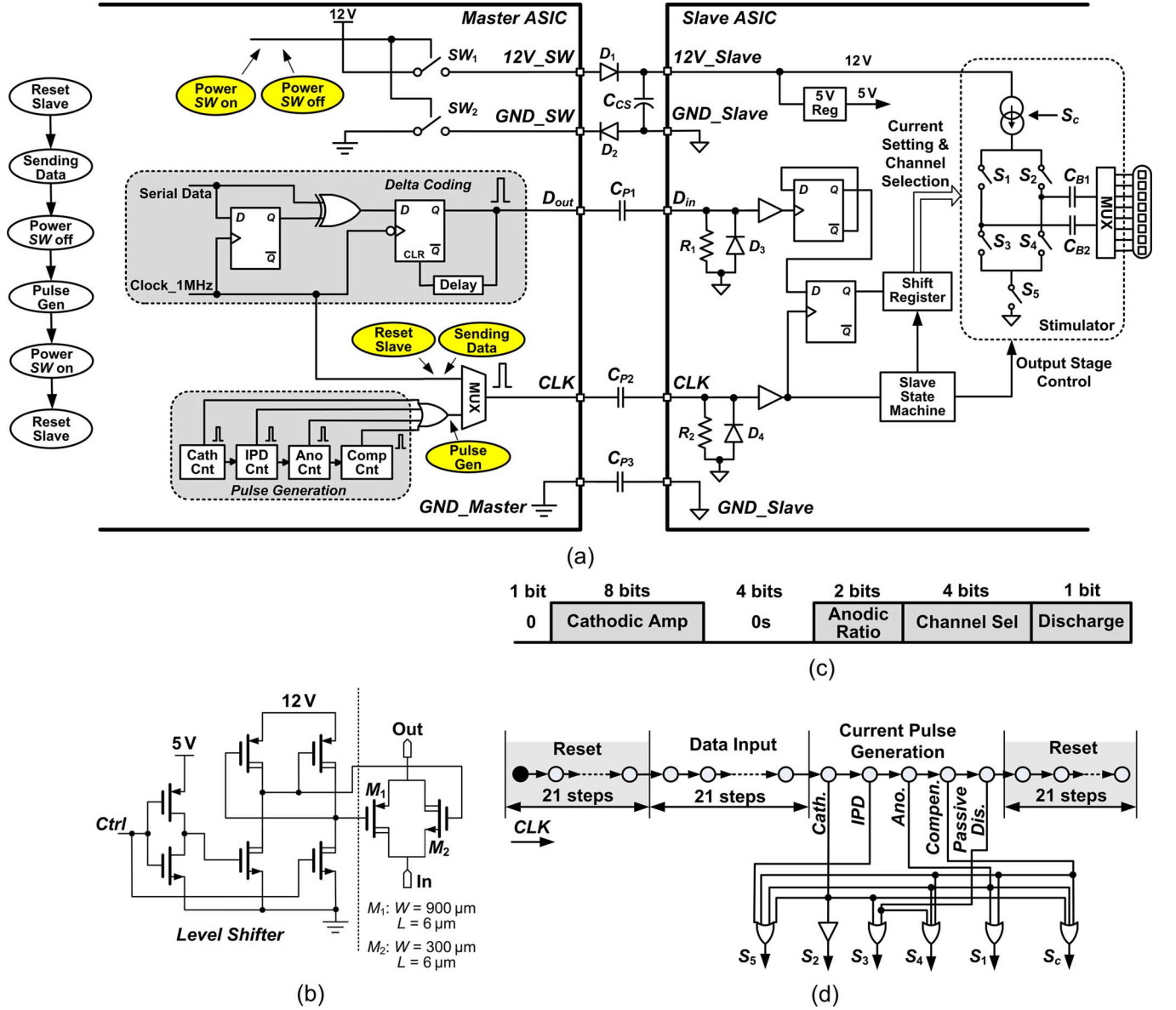


Fig. 7. Power isolation stimulation system. (a) Circuit implementation. (b) Isolation switch schematic. (c) D_{out} data frame to a slave ASIC. (d) Slave state machine.

The stimulation control units of the slave stimulators differ from that of the master unit and have several extra steps before and after the pulse generation state for power isolation control. Details are discussed in the next section.

V. IMPLEMENTATION OF POWER ISOLATED STIMULATION

In order to provide effective power isolation the substrates of each *Power Domain* (Fig. 4) must be separated. This is because the ground voltage of one power domain could go lower than the grounds of the other domains during isolation. This can be achieved by using silicon-on-insulator technology or by implementing the power domains on separate application specific integrated circuits (ASICs). In this design, separate ASICs were chosen for cost reasons. The implant has one master and two slave ASICs. Fig. 7(a) shows the connection between the master and one slave ASIC, and the associated circuits for controlling

the stimulation from the slave ASIC. The connection and circuits to the second slave ASIC is identical.

A. Interconnection

The connection between the master and each slave ASIC has five ports: $12V_SW \rightarrow 12V_Slave$, $GND_SW \rightarrow GND_Slave$, $D_{out} \rightarrow D_{in}$, $CLK \rightarrow CLK$ and $GND_Master \rightarrow GND_Slave$. During pulse intervals in the slave stimulator, the isolation switches SW_1 and SW_2 are on, so the power rails of the slave ASIC are connected to the power rails of the master ASIC and the storage capacitor C_{CS} is charged. SW_1 and SW_2 are implemented in the master ASIC. As shown in Fig. 7(b), they are CMOS switches driven by a level shifter. When SW_1 and SW_2 are turned off, as C_{CS} is considered floating with respect to the master ASIC, the voltage on GND_Slave could go below GND_Master . To prevent forward biasing of the pn junction in the nMOS transistor M_2

in SW_2 , diode D_2 in series with SW_2 is necessary. Similarly, diode D_1 in series with SW_1 is necessary to ensure isolation in the event that $12V_{Slave}$ exceeds $12V_{SW}$. Diodes D_1 and D_2 should be isolated from the substrates of both the master and slave ASICs and therefore must be discrete devices.

The data and clock pulse signals are sent to the slave ASICs through ac coupled capacitive links. Each link consists of a signal coupling capacitor, C_{P1} or C_{P2} , a pull-down resistor, R_1 or R_2 , and a dc restoration diode, D_3 or D_4 . The two signal links are completed by a ground coupling capacitor, C_{P3} , between GND_{Master} and GND_{Slave} . The benefit of this capacitive coupling link is that data transmission is not affected by the relative voltage between the master and slave power rails. The value of the coupling capacitors must be carefully selected so that each link remains high impedance to the stimulation current pulses in order to minimize crosstalk. Selection of the values of C_{P1} , C_{P2} and C_{P3} are discussed in Section V.C.

B. Operation

1) *Flow Control*: The control flow for generating a biphasic stimulus pulse from a slave stimulator is depicted on the left-hand side of Fig. 7(a). Before the onset of a pulse, the management unit in the master ASIC resets the slave state machine (SSM) by sending a 20-bit serial stream via the data link $D_{out} \rightarrow D_{in}$, accompanied by a 1 MHz clock signal on the clock link $CLK \rightarrow CLK$ with one bit per clock pulse. After resetting the SSM, the management unit generates a 20-bit data frame with the delta coding unit and sends it to the slave ASIC. There are 21 clock pulses in both the reset and sending data stages, where the last pulse is for the SSM to load data. A frame consists of the settings for the cathodic pulse amplitude, anodic-cathodic ratio, selection of the stimulating sites, discharge control and five “0” bits as a marker for a data frame, as shown in Fig. 7(c). The slave ASIC demodulates the frame and moves it into a shift register, where the amplitude settings program the current DAC and the channel selection settings configure the multiplexer for the desired electrode sites. After sending the data frame, the management unit turns off SW_1 and SW_2 . From this moment, the slave ASIC is supplied by C_{CS} . The stimulus pulse generation phase follows, operated by a pulse generation unit as described in Section IV. In this phase, a clock pulse is generated at the end of each cathodic and anodic phase (of a biphasic pulse). The clock link to the slave ASIC is now driving the pulse generator unit. These clock pulses are sent to the slave ASIC via the clock link to operate the SSM to generate a biphasic current pulse. The interval between these clock pulses defines the length of each phase. On the completion of a biphasic pulse, the management unit turns SW_1 and SW_2 back on to reconnect the slave ASIC, and a second reset data stream is sent to reset the SSM.

The SSM is a “one-shot” machine driven by clock pulses from the clock link, moving forward by one step per clock pulse, as shown in Fig. 7(d). It directly controls the data shifting in the shift register and the switches in the output stage to generate a biphasic stimulus pulse.

2) *Delta Coding*: The capacitive data link to the slave ASIC can only employ narrow pulses. Because of the capacitor C_{P1} and the pull-down resistor R_1 , the data bits should be coded

with short pulses to guarantee the voltage signals are above the threshold level at the receiving end. Although Manchester coding is commonly used in capacitive data transmission, it requires a complicated decoding circuit.

The aim of the slave ASIC design is to keep the circuit as simple as possible to minimize the demand for energy stored on the storage capacitor and a delta coding method was chosen. A pulse is sent over the data link only when the value in the data stream changes. In operation, every bit in the data stream is compared with the previous bit. If the bit differs from the previous one, a 500 ns pulse is generated; otherwise the output of the modulator remains low. As shown in Fig. 7(a), the modulator circuit requires only two D -flip flops, a XOR gate and a delay cell. At the receiving end, the demodulator is just a D -flip flop. The pulse from the data link drives the D -flip flop at the clock input. Whenever there is a pulse, the output of the D -flip flop changes. Both the modulator and demodulator are synchronized to the 1 MHz clock.

For delta coding an initial condition is required on both sides of the data link, which means the demodulator should be reset before receiving a data frame. An extra reset link between the master and slave ASICs is undesirable because it increases the overall complexity and physical size. A soft reset is implemented in this design. In the reset phase, a 20-bit stream “10101010101010101010” is sent to the slave ASIC. Consequently, the demodulator on the slave ASIC generates a 20-bit stream where every bit changes, regardless of its initial value. Once the SSM detects such a stream, it resets the demodulator output to “0” for the data transmission. The 20-bit data frame, as shown in Fig. 7(c), contains five “0” bits as a marker for a data frame, thus it never falls into the same pattern as the reset stream.

Delta coding is vulnerable to glitches on both the data and clock links. Therefore, a second reset phase after a biphasic pulse is necessary. After reset, switches S_3 , S_4 are closed and S_5 is opened for passive discharge, so that an erroneous pulse will not result in dc current through the electrodes.

C. Considerations on Capacitors

1) *Storage Capacitors*: Each storage capacitor (C_{CS}) should satisfy the requirement that its voltage drop is small while it supplies the slave ASIC. During a biphasic stimulating pulse from a slave ASIC, the maximum charge required for supporting it includes the total charge delivered through the electrodes and the operating current during the pulse. The minimum capacitance is

$$C_{CS} \geq \frac{Q_{\max} \times 2 + T_{\text{pulse}} \times I_{\text{op}}}{V_{\text{drop}}} \quad (1)$$

where Q_{\max} is the maximum allowable charge on the electrode (0.114 μC for this design [29]), T_{pulse} is the duration of the biphasic pulse, I_{op} is the operating current during this pulse, and V_{drop} is the maximum allowed supply voltage drop. The simulated average I_{op} is around 0.3 mA, and T_{pulse} in the most extreme case is 5.5 ms (500 μs in cathodic and compensation phases plus inter-phase delay, as well as an anodic phase 8 times longer than the cathodic phase). For a V_{drop} of less than 1 V, the

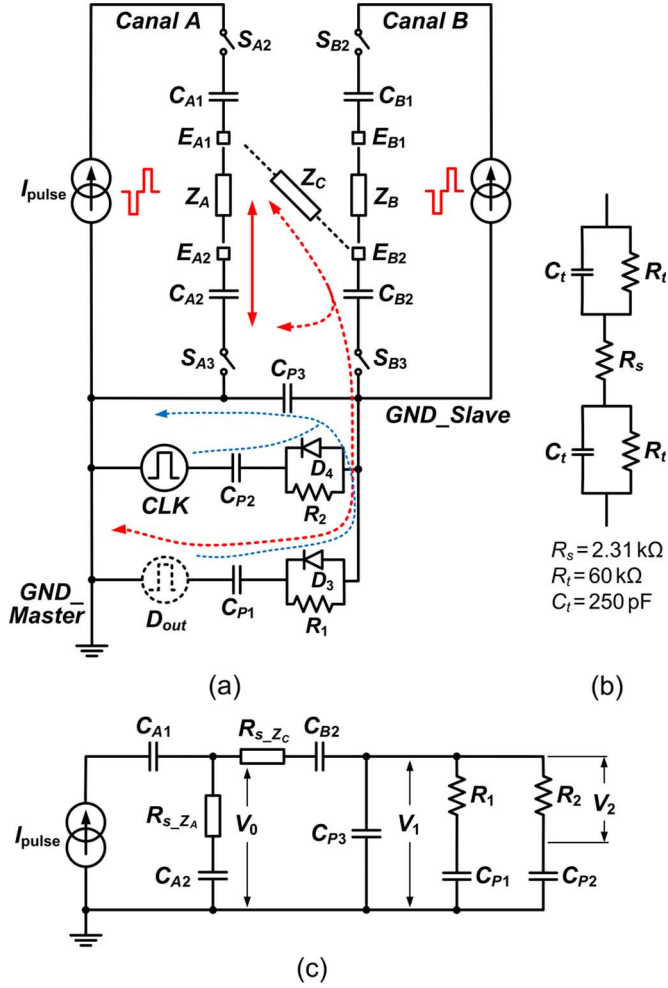


Fig. 8. Analysis of possible channel interaction due to capacitive coupling paths. (a) Indication of possible current paths. (b) Electrode model derived from [28]. (c) Equivalent circuit of the signal and current paths for analyzing crosstalk effect due to I_{pulse} .

minimum capacitance is $1.88 \mu\text{F}$. A $2.2 \mu\text{F}$ was chosen for each storage capacitor.

2) *Coupling Capacitors*: The coupling capacitors C_{P1} , C_{P2} and C_{P3} connect the master and slave ASICs with capacitive links. Fig. 8(a) is a simplified circuit showing the connection of the master ASIC, Canal A, and one of the slave ASICs, Canal B, with crosstalk coupling present. For example, when the two stimulators generate cathodic phase currents at the same time, the switches S_{A2} , S_{A3} , S_{B2} and S_{B3} in the output stage of the stimulators are closed and the electrode arrays are connected (for anodic phase currents switches S_{A1} , S_{A4} , S_{B1} and S_{B4} are closed instead). The normal path of the current from stimulator A through Z_A is shown as a solid red line. E_{A1} and E_{A2} are the stimulating electrodes, Z_A is the electrode-load impedance whose equivalent circuit is shown in Fig. 8(b), and C_{A2} is a blocking capacitor. The crosstalk is through impedance Z_C . Assuming that in the worst instance the distance from E_{A1} to E_{B2} is similar to the distance between E_{A1} and E_{A2} , Z_C has the same equivalent circuit as Z_A and Z_B . The crosstalk path is shown as a dotted red line in Fig. 8(a). The clock signal path [$CLK \rightarrow CLK$, Fig. 7(a)] is the blue dotted line. The data signal circuit [$D_{out} \rightarrow D_{in}$, Fig. 7(a)] is also shown.

The clock or data signal paths contain capacitive elements resulting in a decaying step across resistors R_1 or R_2 . The design target is to provide efficient signal transfer across R_1 or R_2 with minimum crosstalk via Z_C . The time constant in the signal path (clock or data) must allow the voltage across R_1 or R_2 to remain above the logic threshold of the input buffers in the slave ASICs. In Fig. 8(a), when the stimulators are *not* active during the signal transfer, S_{A3} and S_{B3} are open. The time constant τ_s of the decay is then

$$\tau_s = \frac{C_{P2}C_{P3}}{C_{P2}+C_{P3}}R_2. \quad (2)$$

If *both* stimulators are active, S_{A3} and S_{B3} are closed and C_{P3} is in parallel with the series blocking capacitors C_{A2} and C_{B2} (whose values will be shown to be much greater than C_{P3}). Hence, C_{P2} is the dominant capacitor for setting the time constant. The value of $R_1 = R_2 = 65 \text{ k}\Omega$ was chosen to provide an acceptable output load for the buffer logic and to minimise possible crosstalk charge due to the currents in R_1 and R_2 . The input threshold level of the buffers used in the slave ASICs is about 2.5 V. For a 5 V, 500 ns signal pulse the voltage across R_2 is designed to remain above 3.7 V. This requires a time constant τ_s of at least $1.68 \mu\text{s}$. For R_2 (or R_1) of $65 \text{ k}\Omega$, $C_s = 24.9 \text{ pF}$, where C_s is the series capacitance of $2C_t$ and C_{A2} (see Fig. 8).

There are two factors affecting crosstalk coupling due to a stimulating current pulse:

- At the falling edge of a stimulating pulse [I_{pulse} in Fig. 8(a)], any transient voltage generated across resistors R_1 or R_2 must not exceed the logic threshold of the input buffers in the slave ASICs;
- During a stimulating pulse, the total charge through the crosstalk path must not exceed the threshold of neural response. According to [26] this threshold does not exceed 6 nC. A conservative threshold of 1 nC was chosen in this design.

To examine the crosstalk a simplified circuit is shown in Fig. 8(c). The voltage across R_2 as a function of the voltage V_1 is

$$V_2(s) = \frac{s\tau_1}{s\tau_1 + 1}V_1(s) \quad (3)$$

where

$$\tau_1 = R_2 \cdot C_{P2} \quad (4)$$

and s is the Laplace operator. Assuming that C_{P1} , C_{P2} and C_{P3} are much smaller than C_{A2} , C_{B2} and C_t in Z_A and Z_C , the current through R_1 or R_2 does not greatly alter V_1 . Similarly, the current through C_{P3} does not significantly alter the voltage V_0 and can be ignored. Therefore, V_1 can be expressed as

$$V_1(s) = \frac{I_{pulse}}{s} \cdot \frac{s\tau_2 + 1}{sC_s} \cdot \frac{1}{s\tau_3 + 1} \quad (5)$$

where I_{pulse} is the current pulse amplitude

$$\tau_2 = R_{s-Z_A} \cdot C_s \quad (6)$$

$$\tau_3 = (R_{s-Z_A} + R_{s-Z_C}) \cdot C_{P3} \quad (7)$$

and $R_{s_Z_A}$ (or $R_{s_Z_C}$) is defined in Fig. 8(b). For a current pulse width up to a few hundred microseconds, contribution from each R_t is negligible. Combining (3) and (5)

$$V_2(s) = \frac{I_{\text{pulse}}}{s} \cdot \frac{s\tau_2 + 1}{sC_s} \cdot \frac{1}{s\tau_3 + 1} \cdot \frac{s\tau_1}{s\tau_1 + 1}. \quad (8)$$

The inverse Laplace transform of (8) is

$$V_2(t) = I_{\text{pulse}} \cdot R_2 \cdot \frac{C_{P2}}{C_s} \cdot \left\{ 1 + \frac{1}{(\tau_3 - \tau_1)} \cdot \left[(\tau_2 - \tau_3)e^{-t/\tau_3} - (\tau_2 - \tau_1)e^{-t/\tau_1} \right] \right\}. \quad (9)$$

Assuming $\tau_1 \ll \tau_2, \tau_3 \ll \tau_2$ and $C_{P2} \ll C_s$, the term $I_{\text{pulse}} \cdot R_2 \cdot (C_{P2}/C_s)$ can be neglected and (9) may be simplified to

$$V_2(t) \approx I_{\text{pulse}} \cdot R_{s_Z_A} \cdot \frac{\tau_1}{(\tau_3 - \tau_1)} \cdot \left(e^{-t/\tau_3} - e^{-t/\tau_1} \right). \quad (10)$$

Equation (10) shows that a current step due to I_{pulse} results in a spike as a result of the difference between τ_1 and τ_3 , and $V_2(t)$ peaks at a time t_{peak} , where

$$t_{\text{peak}} = \frac{\tau_1\tau_3}{(\tau_3 - \tau_1)} \cdot \ln \left(\frac{\tau_3}{\tau_1} \right). \quad (11)$$

To avoid a false logic pulse at the signal inputs of the slave ASIC, the peak voltage of $V_2(t)$ should be below the logic threshold of 2.5 V. From (10) the peak voltage of $V_2(t)$ reduces with τ_1/τ_3 .

The charge through the crosstalk path [Z_C , Fig. 8(a)] during a stimulating pulse on *Canal A*, is calculated by integrating the current I_{Z_C} through Z_C over the pulse width. From Fig. 8(c) I_{Z_C} is the sum of currents through R_1, R_2 and C_{P3} . Since $R_1 = R_2$ and $C_{P1} = C_{P2}$

$$I_{Z_C}(s) = \frac{V_1(s)}{1/sC_{P3}} + 2 \frac{V_2(s)}{R_2}. \quad (12)$$

Substituting (5) and (8) into (12) the resulting inverse Laplace transform is

$$I_{Z_C}(t) = I_{\text{pulse}} \cdot \left(\frac{C_{P3}}{C_s} + \frac{R_{s_Z_A}}{R_{s_Z_A} + R_{s_Z_C}} e^{-t/\tau_3} \right) + 2 \cdot \frac{V_2(t)}{R_2}. \quad (13)$$

The total charge Q_{Z_C} through Z_C during a cathodic or anodic phase of a stimulating pulse of width PD is

$$Q_{Z_C} = \int_0^{PD} I_{Z_C}(t) dt. \quad (14)$$

When PD is greater than five times the larger of τ_1 or τ_3 , the total charge is approximated to

$$Q_{Z_C} \approx I_{\text{pulse}} \cdot \left[R_{s_Z_A} \cdot (2C_{P2} + C_{P3}) + \frac{2C_{P2} + C_{P3}}{C_s} \cdot PD \right]. \quad (15)$$

For a long pulse, (15) shows two parts contributing to the total coupling charge: a step charge $I_{\text{pulse}} \cdot R_{s_Z_A} \cdot (2C_{P2} + C_{P3})$ at the onset of the current step, and a ramp charge that increases with PD . Both are proportional to $(2C_{P2} + C_{P3})$. The maximum coupling charge (defined by the maximum acceptable threshold of neural response) defines the maximum value of $(2C_{P2} + C_{P3})$.

In this design, based on the compliance limits of the current drivers, C_{A1}, C_{A2}, C_{B1} and C_{B2} are all 200 nF. The values of the components in the equivalent circuit of the electrode arrays used are noted in Fig. 8(b). The maximum amplitude of I_{pulse} is 1 mA. The maximum allowable safe charge into the electrodes [39] is 0.114 μC . When $I_{\text{pulse}} = 1$ mA the maximum available pulse width is then 114 μs . The maximum coupling charge occurs at this pulse width.

The values of C_{P1}, C_{P2} and C_{P3} can now be derived. From (15) the coupling charge threshold is satisfied when $(2C_{P2} + C_{P3})$ is 186 pF. From (10) to minimize the peak voltage of $V_2(t)$ due to the stimulating current, τ_1/τ_3 must be kept to a minimum. Since the maximum value of τ_3 is proscribed by $(2C_{P2} + C_{P3})$, τ_1 must be kept to a minimum. This is set by the minimum acceptable time constant τ_s in (2). $C_{P3} = 120$ pF and $C_{P1} = C_{P2} = 33$ pF satisfy these conditions. From (10) and (11) the resulting peak voltage of $V_2(t)$ is 1.41 V (below the 2.5 V input threshold of the logic).

In this vestibular stimulator design it is important to note that values for C_{P1}, C_{P2} and C_{P3} were chosen for $I_{\text{pulse}} \leq 1$ mA. From (10) and (15) I_{pulse} is one of the factors determining the isolation performance. For higher values of I_{pulse} , in order to maintain the isolation performance, smaller values for C_{P1}, C_{P2} and C_{P3} are necessary, and C_{P2}/C_{P3} must also be smaller to reduce τ_1/τ_3 . However, from (2), if C_{P1}, C_{P2} and C_{P3} are smaller, the pulse widths of CLK and D_{out} must be reduced in proportion to maintain the integrity of the signals. From (10) and (15) lower electrode impedances and shorter pulse widths will improve the isolation performance.

VI. MEASURED RESULTS

The master and slave ASICs were implemented in X-FAB's 0.6- μm HV CMOS technology. Fig. 9 shows the vestibular implant prototype. The implant uses a 55 mm \times 25 mm double-sided printed circuit board, including a 16 mm diameter secondary coil. The master ASIC is placed on the topside, while the two slave ASICs are on the bottom side. Table I lists some of the features and measured performance of the prototype system.

A. Stimulator Outputs

The master and slave ASICs were tested together with three vestibular electrode arrays in physiological saline, with the master ASIC generating pulses on *Canal 1*, slave ASIC 1 on

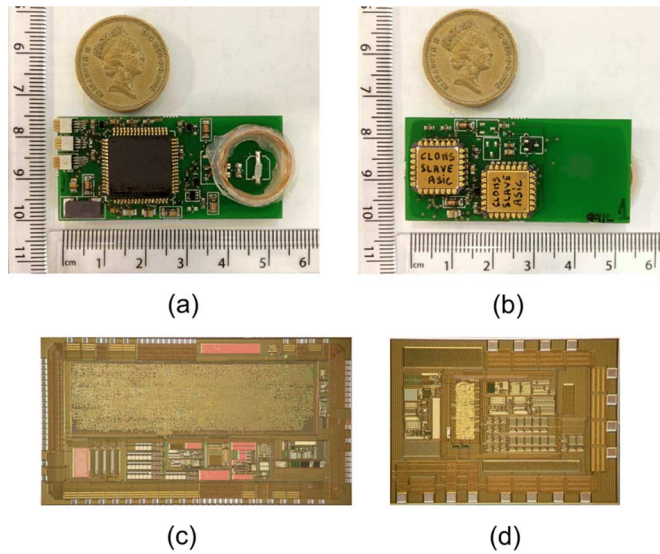


Fig. 9. Photograph of the vestibular implant prototype (electronics) in comparison with a one-pound coin (unit in the photos: cm). (a) Top side with the master ASIC. (b) Bottom side, with the two slave ASICs. The chip microphotographs of the master and slave ASICs are respectively shown in (c) and (d).

TABLE I
SUMMARY OF FEATURES AND PERFORMANCE

Technology	X-FAB 0.6- μm HV CMOS
Die size	Master ASIC: 21.42 mm ² Slave ASIC: 3.90 mm ²
Supply voltage	5 V (digital circuits, DAC, amplifier) 12 V (stimulator output stage)
Stimulation:	
Stimulation type	Biphasic
Stimulation current	≤ 1 mA
Pulse rate	1–500 pps
Pulse rate resolution	≤ 0.5 pps
Pulse duration	Cathodic phase: 0–500 μs Anodic phase: 1–8 times cathodic width
Recording:	
Amplifier gain	70 dB, 57 dB, 43 dB, 26 dB
Bandwidth	70 Hz – 8.2 kHz
Input-referred noise	2.16 μV_{rms}
CMRR	77.3 dB @ 1 kHz
Sampling rate	20 kSample/s
Power consumption	29.7 mW (with 1 mA stimulus on all three canals and 40 pps, 19.2 ms recording window on the master ASIC, 500 pps on the slave ASICs)

Canal 2 and slave ASIC 2 on *Canal 3*. A series 5 k Ω resistor was connected to each electrode array to monitor the electrode current.

1) *Pulse Modulation*: In the results shown in Fig. 10(a), current pulses to the three canals are modulated by a 2 Hz sinusoid in different schemes. On *Canal 1*, pulse amplitude modulation with a swing of 400 μA was applied to pulses with a base rate of 90 pps (the natural baseline firing rate) and base amplitude of 300 μA , while on *Canal 2*, pulse rate modulation with a swing of 400 pps to pulses with a base rate of 250 pps (the elevated baseline rate used in [17], [18]) and base amplitude of

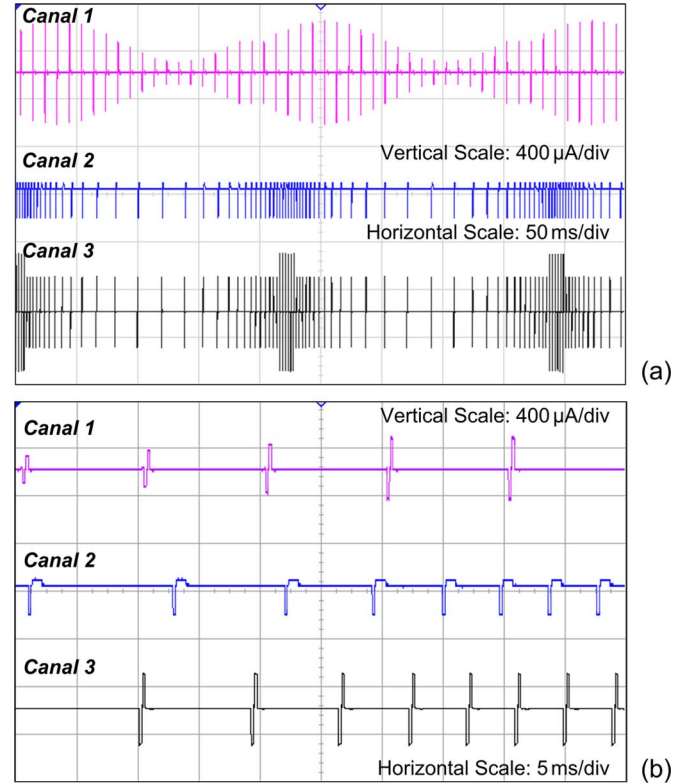


Fig. 10. Oscillograms showing current pulses from the master and slave ASICs. (a) With pulse amplitude modulation on *Canal 1*, pulse width modulation on *Canal 2* and co-modulation on *Canal 3*. (b) Zoom-in view.

300 μA . Co-modulation was applied on *Canal 3* according to the *in vivo* tests in [15] to account for the excitation-inhibition asymmetry. It was based on the same pulse rate modulation on *Canal 2*, but the pulse amplitude was increased to 500 μA for pulse rates in the range of 400–500 pps in order to elicit a larger eye response to stimulation. Details of the pulses are shown in a zoom-in display in Fig. 10(b). The pulses on *Canal 1* and *Canal 3* are symmetrical biphasic pulses with a pulse width of 200 μs and an inter-phase delay of 100 μs . Pulses on *Canal 2* are asymmetrical pseudo-monophasic pulses with a cathodic width of 200 μs and an anodic width of 400 μs .

2) *Recording*: Fig. 11 shows results of a recording test. The master stimulator was set to generate 192 μA pulses with 128 μs pulse width per phase and 50 μs inter-phase delay. The pulse interval was 14.432 ms to allow a 3.2 ms recording window. No masker pulse was activated. In Fig. 6(a) electrodes (*B* and *G*) and (*A* and *D*) were chosen for stimulation and recording, respectively. A 1 V peak-peak, 4 kHz sinusoidal signal was applied to two metal plates in saline, 5 cm apart. This signal was sensed via electrodes *A* and *D* and amplified during the recording window.

B. Parallel Stimulation

Two electrode arrays were placed in saline solution to test parallel stimulation as shown in Fig. 12. Each array was connected to a slave ASIC. They were separated by a 1.5 mm gap with a silicone rubber spacer to simulate the estimated distance

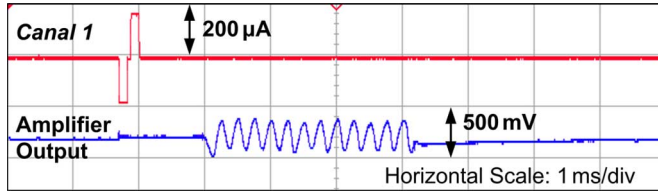


Fig. 11. Oscilloscope showing stimulation current pulses from the master ASIC and the amplifier output during the recording window.

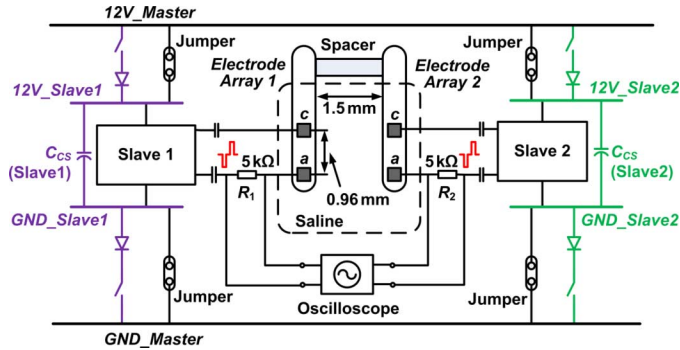


Fig. 12. Setup for parallel stimulation tests. The two slave stimulators are powered and controlled by the master ASIC as shown in Fig. 7(a). The master ASIC and the communication links are not shown in this figure for clarity.

between electrode arrays in the inner ear after implantation. Currents from the two slave ASICs are labelled *Canal 2* and *Canal 3* in the oscillograms (*Canal 2* from slave 1, and *Canal 3* from slave 2). The anode (labelled *a*) and cathode (labelled *c*) on each array are 0.96 mm apart. Each array was connected to a slave stimulator via a 5 k Ω sensing resistor in series with the anode electrode. Current pulses through the electrodes were monitored on an oscilloscope by measuring the voltage across the resistor. Current pulses from both stimulators were pseudo-monophasic pulses, as shown in Fig. 13(a), with a cathodic phase (labelled *A*) of 1 mA amplitude and 114 μ s width (the maximum allowed charge), a 100 μ s inter-phase delay (labelled *B*), an anodic phase (labelled *C*) with width eight times longer than the cathodic phase and a compensation phase (labelled *D*) of equal width to the cathodic phase. The pulse rate was 517 pps on *Canal 2* and 250 pps on *Canal 3*. The stimulation pulses occasionally overlap in time. The normally isolated power supplies can be connected by jumpers in Fig. 12 to compare the crosstalk reduction performance with and without power isolation. When the jumpers are shorted, power isolation is cancelled and all the three stimulators effectively share the same power supply. Crosstalk with and without isolation can then be compared.

Fig. 13(a) shows the measured supply voltage on the storage capacitor and the control waveforms when generating a biphasic pulse from one of the slave stimulators. The pulses measured at the D_{in} and CLK ports of the slave ASIC show the control flow of generating a biphasic pulse (see Section V.B). At the onset of the 1.24 ms pulse, the isolation switches are turned off, and the storage capacitor starts discharging. The supply voltage drop is less than 500 mV. At the end of the pulse the storage capacitor is connected back to the power rails to recharge. The time for voltage recovery is less than 500 μ s. Fig. 13(b) shows the waveforms on both the data and clock links during the “slave reset” and “sending data” states. After the reset stream, a number of

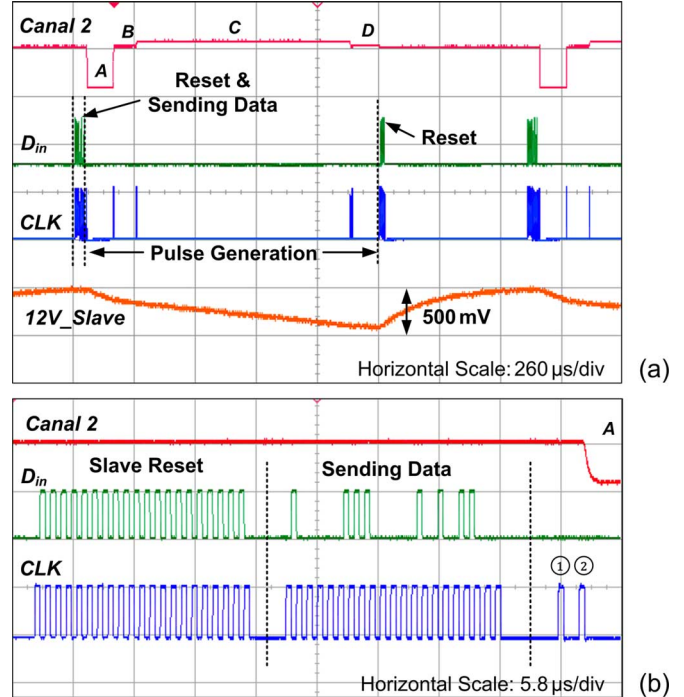


Fig. 13. Oscilloscope showing the control flow of power isolation stimulation. (a) The supply voltage on the storage capacitor and the control waveforms on the data and clock links to generate a biphasic pulse from a slave stimulator. (b) Details of the data and clock links during slave reset and sending data states. The amplitude of the digital D_{in} and CLK signals is 5 V.

pulses representing command frame “0111110100001100100” are sent to set the pulse amplitude at 1 mA and select electrode sites *D* and *H* for stimulation. The value switched eight times in this frame, so that there are 8 pulses on D_{in} in the “sending data” section. After the “sending data” section, the slave state machine enters the pulse generation state, where the first CLK pulse ① sets the “H-bridge” as cathodic-first, and the second CLK pulse ② activates the current DAC. The cathodic phase of the current pulse, *A*, starts after ②. By switching on the output stage before the current DAC switching spikes on the current pulses can be minimized.

C. Crosstalk Reduction

For comparison, two tests were conducted, one with both stimulators connected to a common power supply and the other with power isolation. Fig. 14 shows the moment when pulses from the two stimulators overlap in both scenarios. Part of *Pulse 1* on *Canal 2* overlaps with *Pulse A* on *Canal 3*. In Fig. 14(a) the stimulators effectively share the same power rails by shorting the jumpers. When overlapping, part of the current from *Canal 2* can flow to the electrode array connected to *Canal 3* through a crosstalk path, and hence cause current collapse through the sensing resistor R_1 . The same is true for pulses from *Canal 3*. Pulse collapse is shown on both *Pulse 1* at ① and *Pulse B* at ②. Crosstalk from *Canal 2* to *Canal 3* is evident. At ①, during the cathodic phase of *Pulse 1* on *Canal 2*, current is from cathode (*c*) to anode (*a*) on *Electrode Array 1* then to GND_Slave1 . Concurrently *Pulse A* on *Canal 3* is in the compensation phase [7], where the cathode (*c*) on *Electrode Array 2* is connected to GND_Slave2 . Since GND_Slave1 and GND_Slave2 are both shorted to GND_Master via the jumpers, a crosstalk path

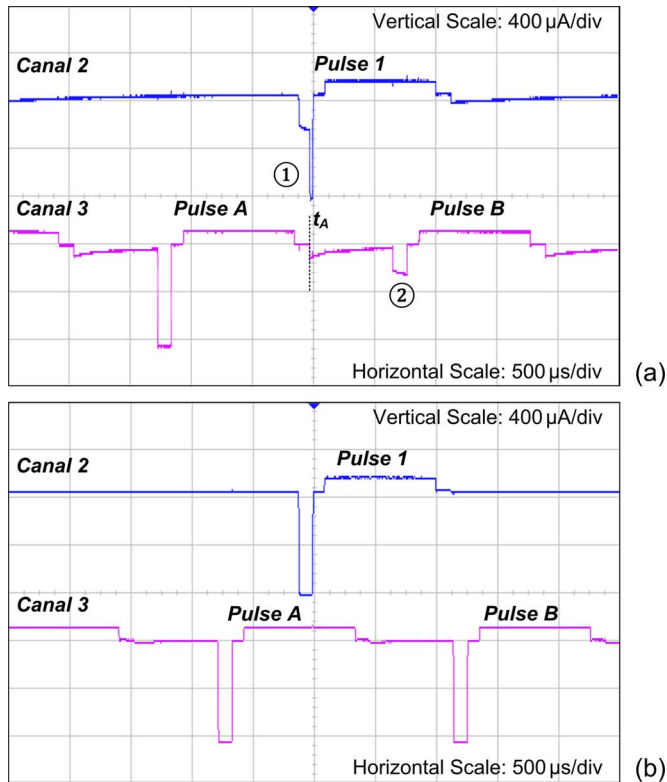


Fig. 14. Oscilloscopes showing current pulses from the two slave stimulators to demonstrate the effects of crosstalk. (a) Common power supply. (b) Isolated power supplies.

occurs through which part of the current from *Canal 2* flows from *c* on *Electrode Array 1* to *c* on *Electrode Array 2* and then to *GND_Master*, resulting in less current return to the anode (*a*) on *Electrode Array 1*. Hence, *Pulse 1* measured through R_1 collapses. This crosstalk exists until time t_A , when the compensation phase of *Pulse A* finishes and *Electrode Array 2* is isolated from slave 2. At this point the current in *Pulse 1* recovers. Similarly, the entire cathodic phase of *Pulse B* collapses at ② where it overlaps with the anodic phase of *Pulse 1*, during which period a crosstalk path exists from *c* on *Electrode Array 2* to *c* on *Electrode Array 1* and then to *GND_Master*. The collapse significantly reduces the overall charge in the cathodic phase, normally the stimulating phase, which may cause insufficient stimulating current through the anode and thus “missing a beat” in pulse rate modulation. In contrast, in Fig. 14(b) where the jumpers are disconnected and power isolation is restored, the effectiveness of the power isolation is demonstrated as both pulses remain intact during the overlaps.

Similar tests were conducted when slave 2 was replaced by the master stimulator. The results are shown in Fig. 15. In these tests the master stimulator was connected to *Electrode Array 1*, labelled *Canal 1* in Fig. 15, and slave 1 to *Electrode Array 2*, labelled *Canal 2*. Similar to the results in Fig. 14, power isolation affords minimal crosstalk during pulse overlaps between canals. In Fig. 15(a), when there is no power isolation, pulse distortion is evident during the cathodic phase of *Pulse 1* and *Pulse B*. The distortion disappears when power isolation is restored.

VII. CONCLUSION

This paper has presented the design of a prototype vestibular prosthesis with 3D parallel stimulation. A power isolation

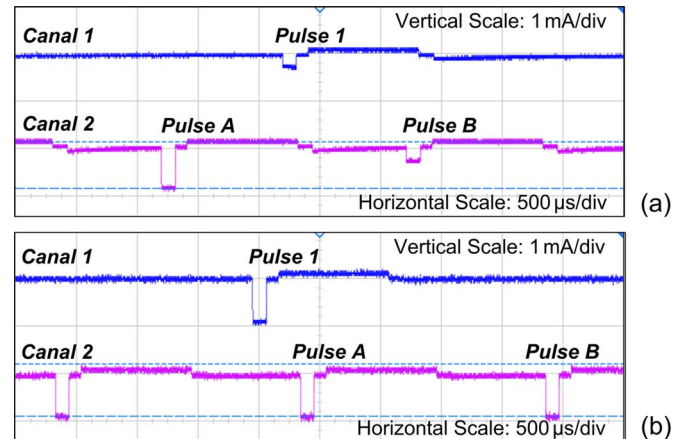


Fig. 15. Oscilloscopes showing current pulses from the master stimulator and one of the slave stimulators to demonstrate the effects of crosstalk. (a) Common power supply. (b) Isolated power supply.

method has been implemented which provides separate sources of power supply to the three stimulators for the semicircular canals during stimulation. Crosstalk between canals during parallel stimulation can then be minimized, and has been successfully demonstrated with *in vitro* experiments. A memory-based stimulation control has been designed to independently manage parallel stimulation of the three canals, providing a wide variety of stimulation patterns. Information from head rotation can be encoded flexibly with pulse rate modulation, pulse amplitude modulation and hybrid modulation methods. A recording unit has been implemented to record the VEP for adaptive stimulation control. The stimulation system has been implemented with three ASICs in a 0.6- μm high-voltage CMOS technology.

The prototype vestibular prosthesis is an intermediate step in the progress towards developing a clinical implant for treating severe vestibular disorders. Compared with state-of-art designs in the literature, including specifically designed vestibular prostheses [1]–[4], [6], [10] and modified commercial cochlear implants [30], [40], the system presented in this paper enables independent parallel stimulation to the three canals with minimal crosstalk. In addition, it features a versatile stimulation management and neural recording for feedback, which potentially provides additional information for development of algorithms, offering more precise sensation of head rotation.

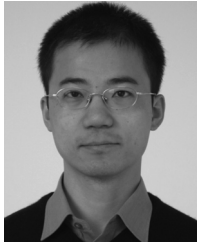
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