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UCL Electronic and Electrical Engineering: Profile

A. J. Seeds

Information

- Information **Sensing**
- Information **Processing**
- Information **Transmission**
- Information **Output**

Including the Energy and Manufacturing technologies to make this possible

Department Scale

- **38 Academic Staff**, including 6 Royal Society/Royal Academy of Engineering/EPSRC Fellowship Holders

- **52 Research and Technical Staff**

- **10.4 FTE Administrative Staff**

- **538 Students**
  - 340 Undergraduate (Intake 110 AAA min. AAA* ave.)
  - 80 MSc
  - 120 Research (MRes/PhD/EngD)

Turnover and Contribution (2012/13 FY)

- **Total Income £14.6m (15% of Faculty total)**
  - Teaching £8.6m
  - Research £5.2m (Direct £4m, Indirect £1.2m)
  - Other £772k

- **Expenditure £9.4m**
  - Staff £5.2m
  - Operating expenses £4.2m

- **Contribution £5.2m (19% of Faculty total)**

Major Research Initiatives

- **3 EPSRC Programme Grants**
  - UNLocking the capacity of Optical Communications (UNLOC)- £4.8 m (PI P. Bayvel)
  - Nano-electronic Based Quantum Physics- £6.6 m (PI M. Pepper)
  - Coherent TeraHertz Systems (COTS)- £6.8 m (PI A. J. Seeds)

- **CDT** in Photonic Systems Development- £7.1 m (PI A. J. Seeds)

- National Dark Fibre Infrastructure Service- £2.5 m (PI A. J. Seeds)

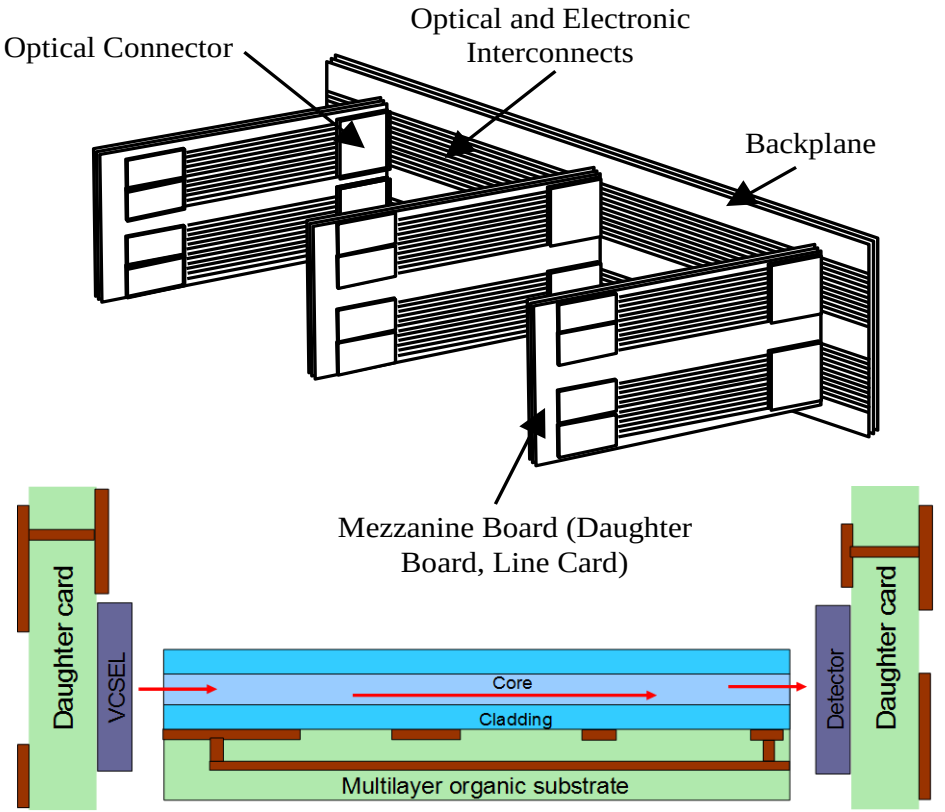
- Other current Grants/Contracts total £15.1 m

£38.1 m of awarded Grants/Contracts (> £1 m/acad.)

Space

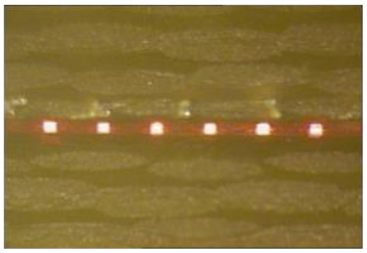
Optical Interconnects

- Advanced Interconnect Backplanes for Cloud Computing and Data Centres
- Passive backplane into which plugs and unplugs: Blade servers, Hard disc drive cards, Multiway switch fabrics
- Bottleneck at the backplane

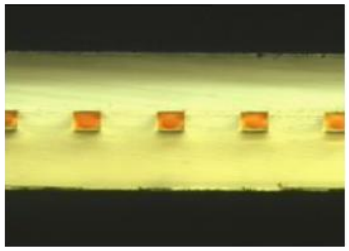


- Challenge to develop low cost high speed scalable interconnect technology compatible with Printed Circuit Board design and fabrication
- Challenge to develop a low cost passively alignable pluggable optical connector

Polymer waveguides laminated in and on PCBs



Source: Exxelis Ltd

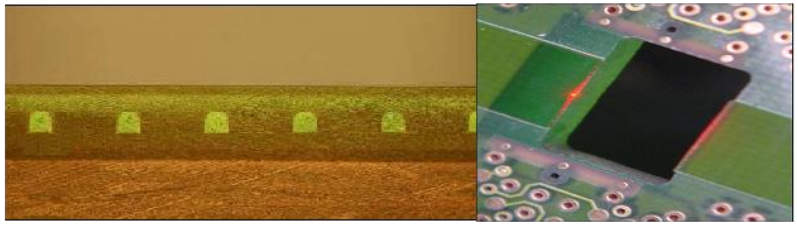


Source: Fraunhofer IZM

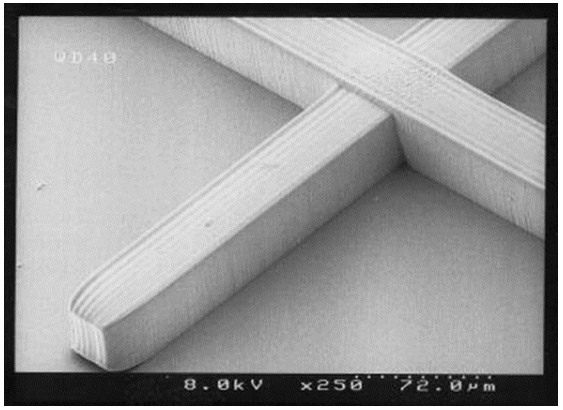
Source: UCL/Exxelis

Source: UCL/Exxelis

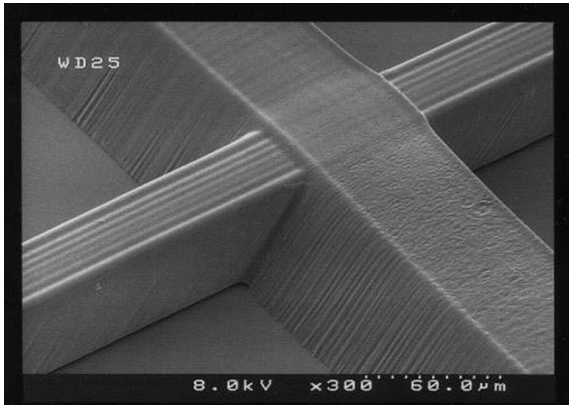
Source: Varioprint AG



Source: IBM Zürich



Source: Heriot Watt



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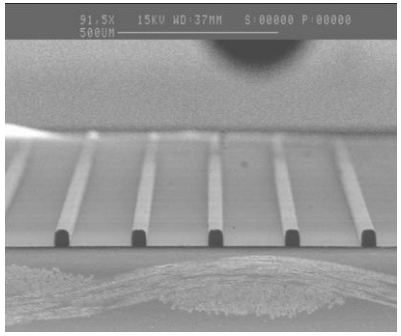
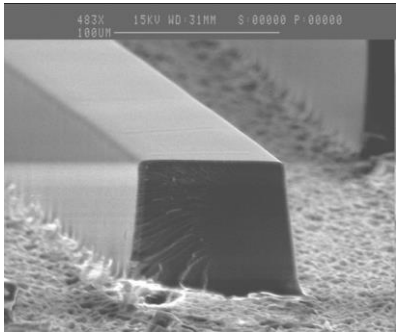


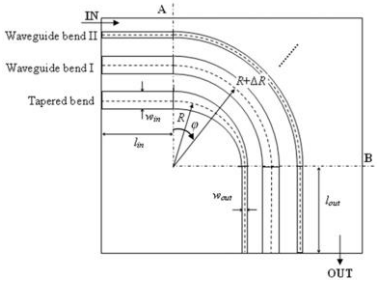


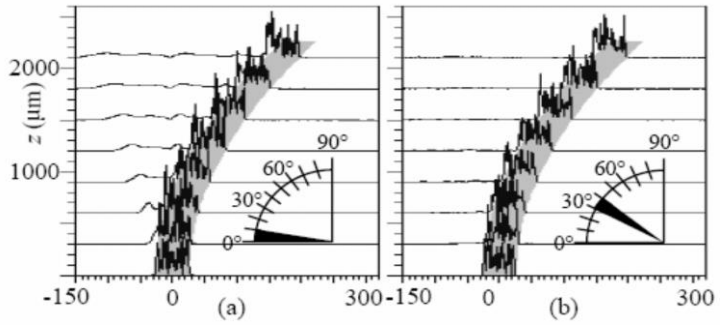
Source: Exxelis

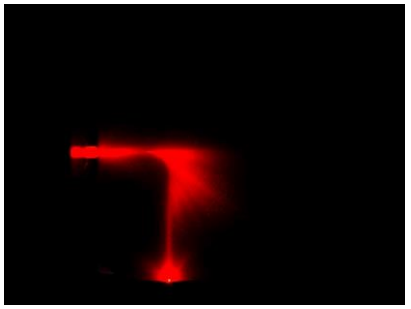
Photolithography, Laser Direct Write, Laser Ablation, Ink Jet Printing and Embossing Fabrication

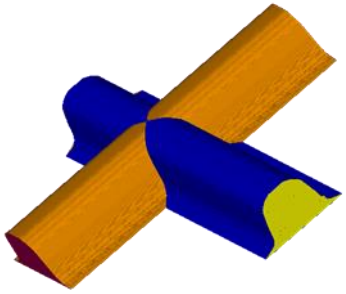
Waveguide Design Rules

- Aim to establish waveguide design rules and to incorporate them into PCB layout software
- Design rules established by comparing modelled with experimental results
- Modelling: Wide angle Beam Propagation Method, Raytracing, Overlap integrals of Mode expansions
- Experimental measurements: loss, crosstalk, misalignment tolerance, near field and far field output light patterns, sidewall roughness and end facet roughness

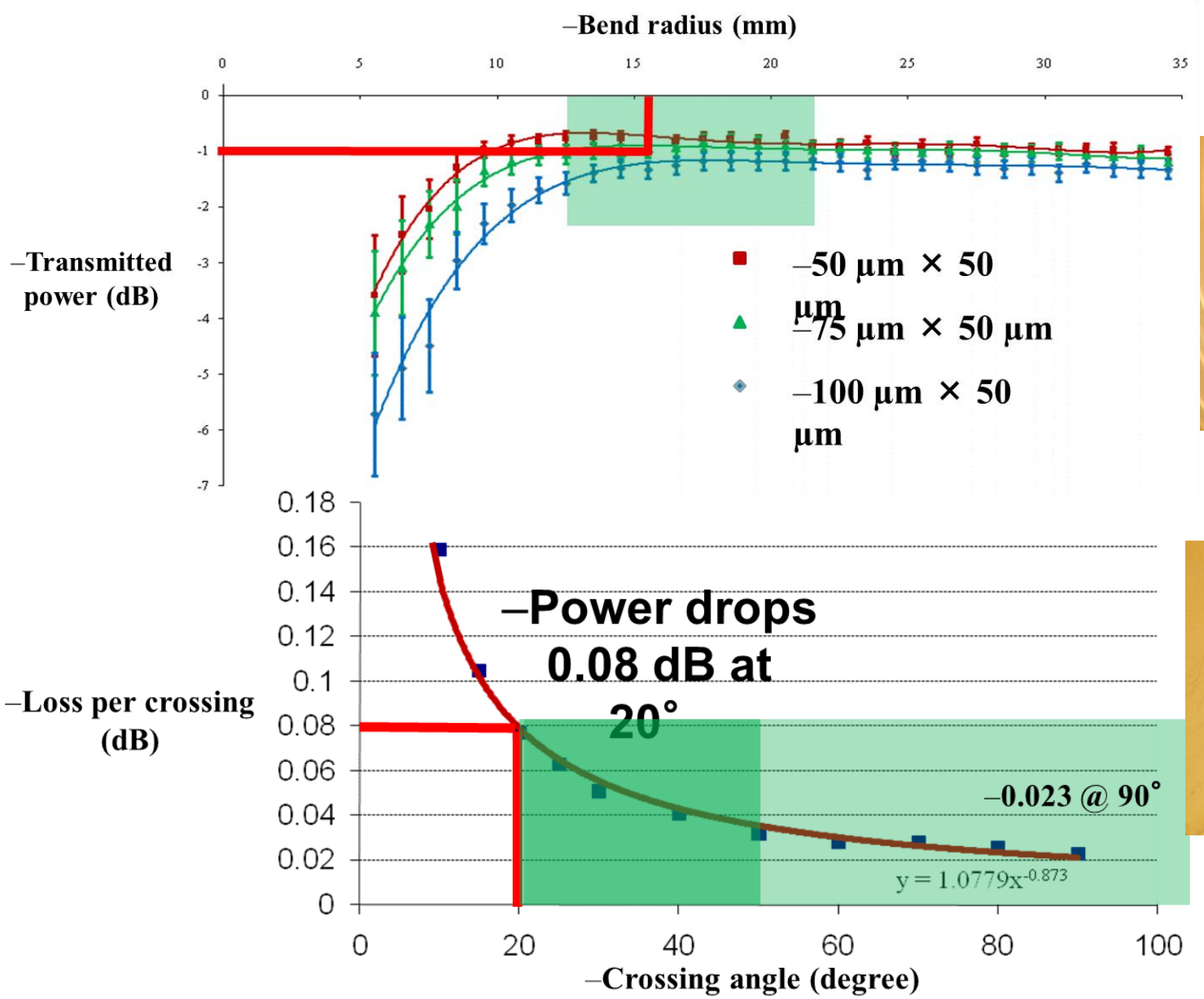




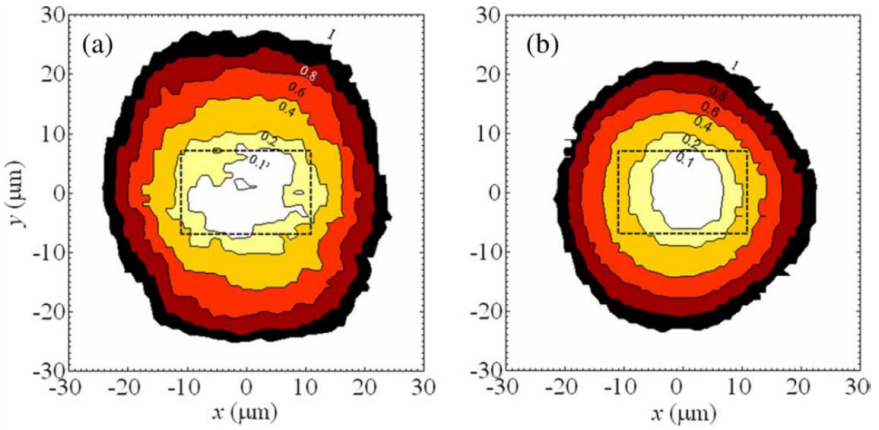




Waveguide Layout Design Rules

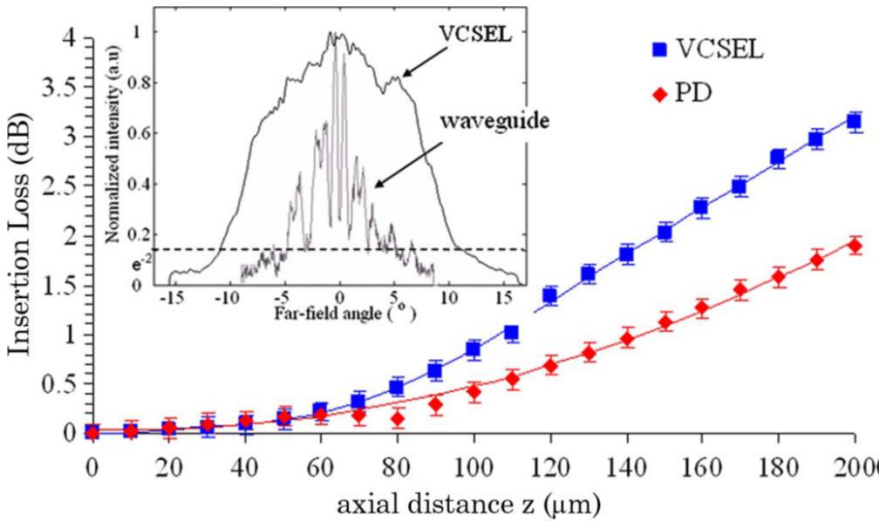


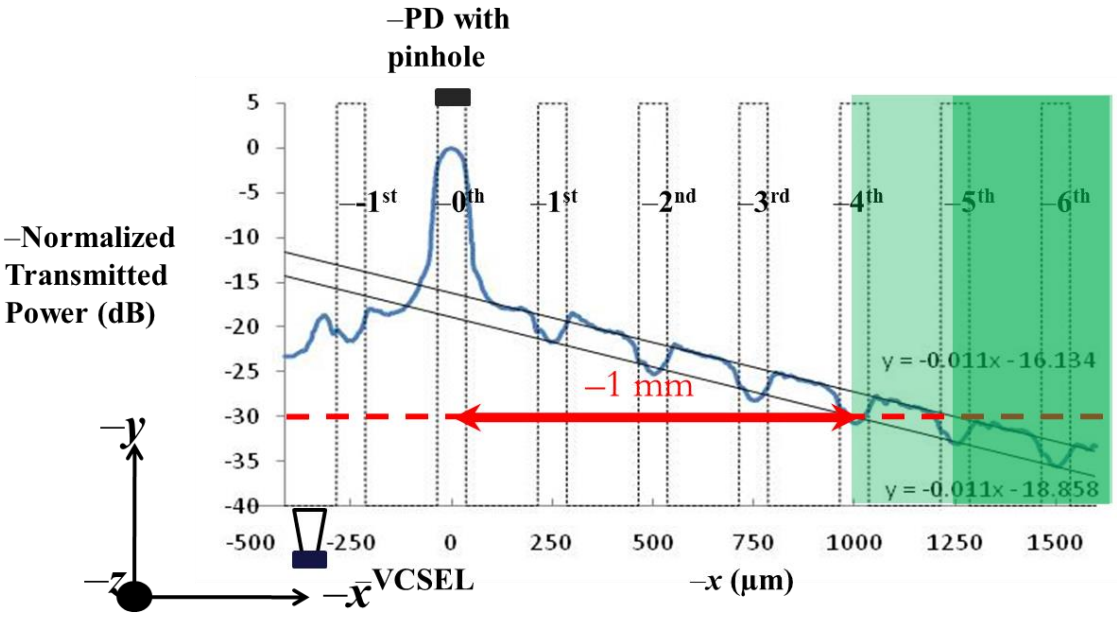
Misalignment and Crosstalk Integration Design Rules

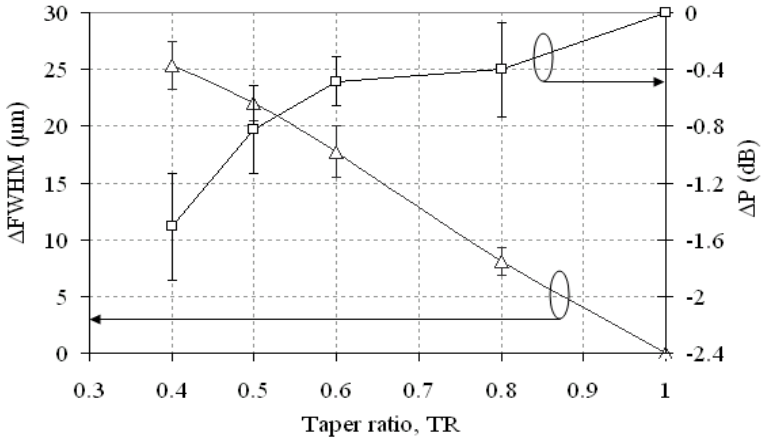


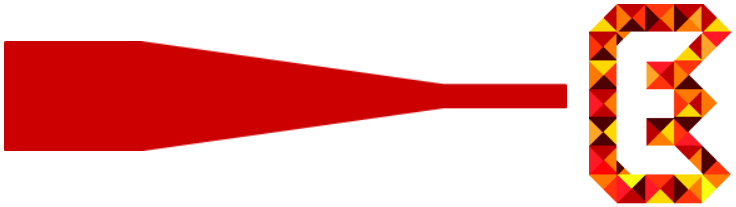
(a) Contour map of relative insertion loss compared to the maximum coupling position for VCSEL misalignment at z = 0.

– (b) Same for PD misalignment at $z = 0$. Resolution step was $\Delta x = \Delta y = 1$ μm.

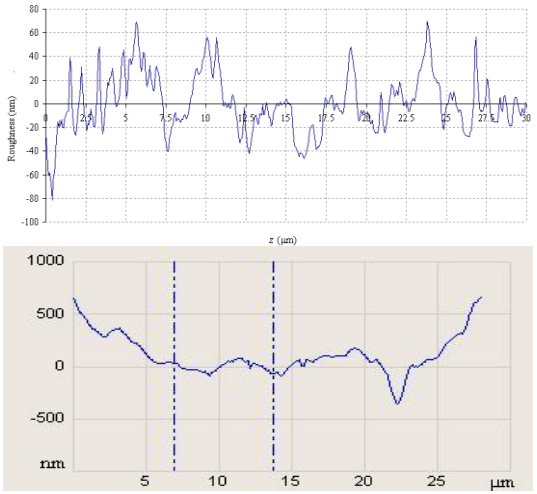






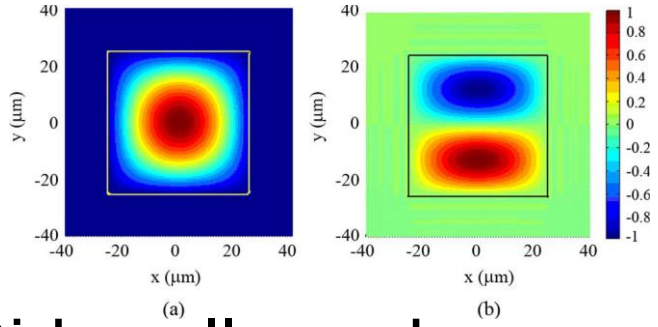


Waveguide Side and End Roughness Design Rules

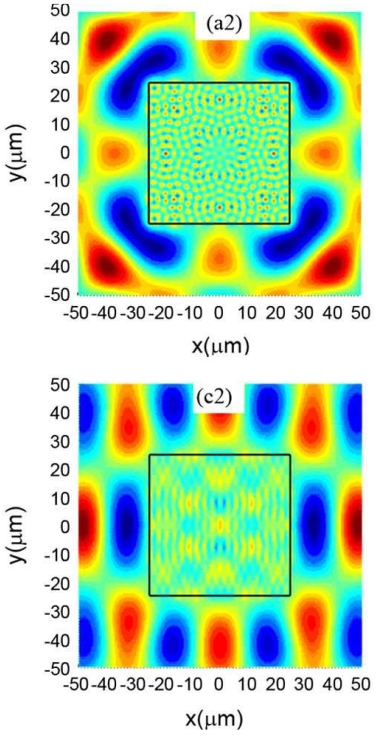


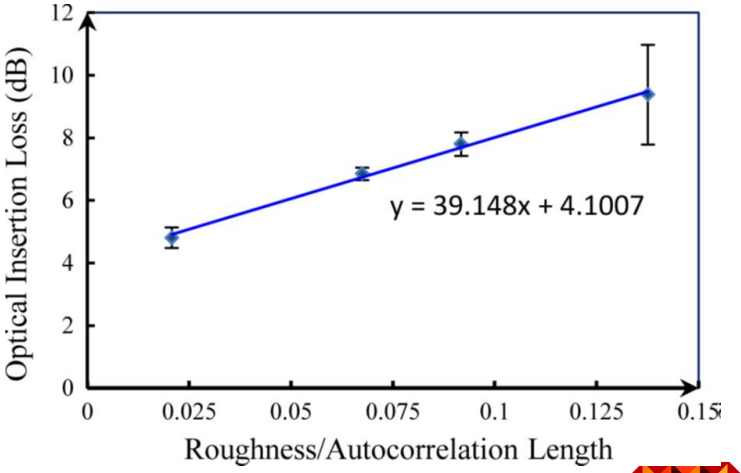
- RMS side wall roughness: 9 nm to 74 nm
- RMS polished end facet roughness: 26 nm to 192 nm.

End Facet roughness causes optical input and output coupling loss



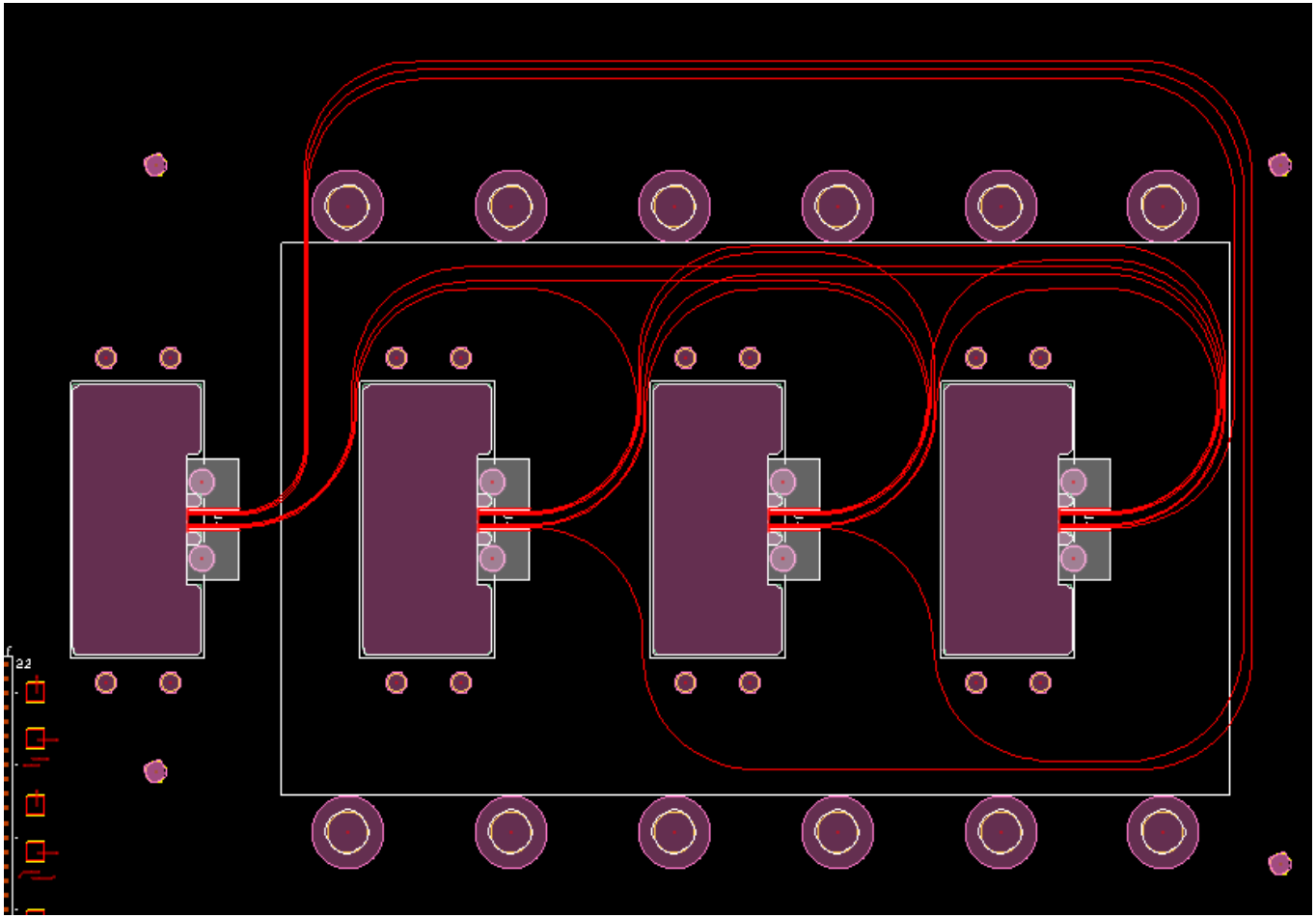
Sidewall roughness couples bound modes to each other and to radiation modes

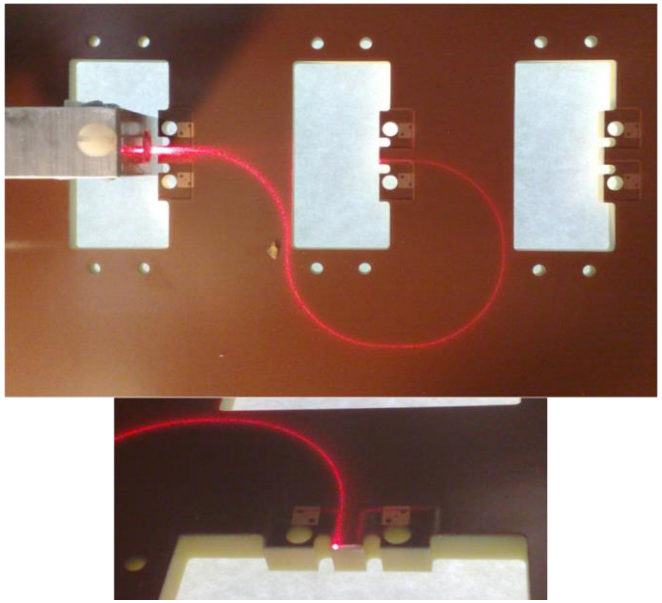




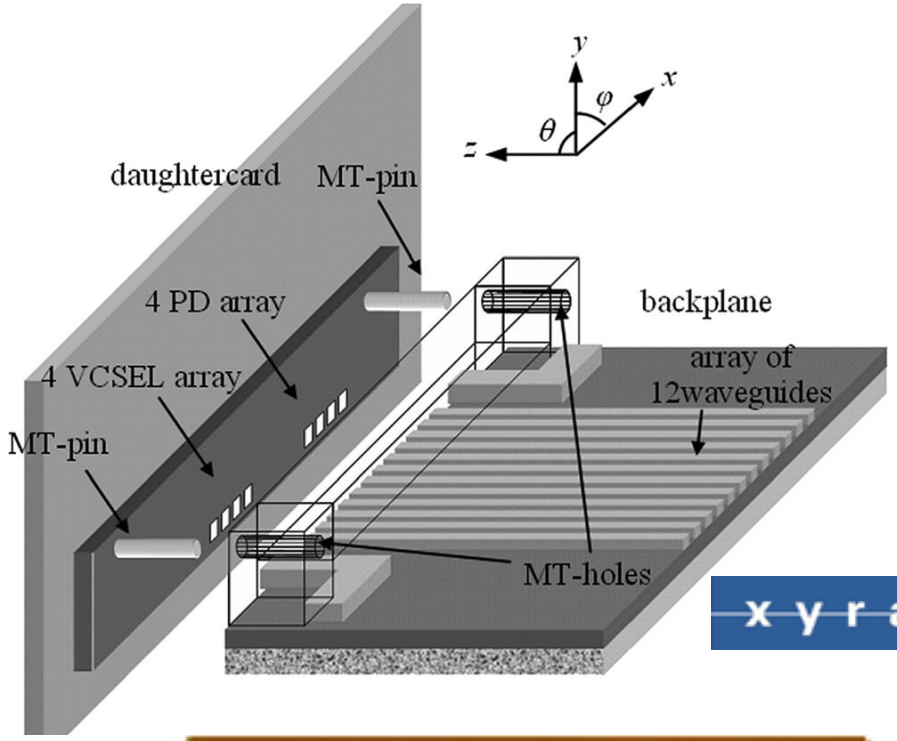
4 x 4 Duplex Waveguide Interconnection Fabric

Our waveguide design rules were incorporated into Cadence PCB layout software and used to design the most complex optical and electronic multilayer PCB

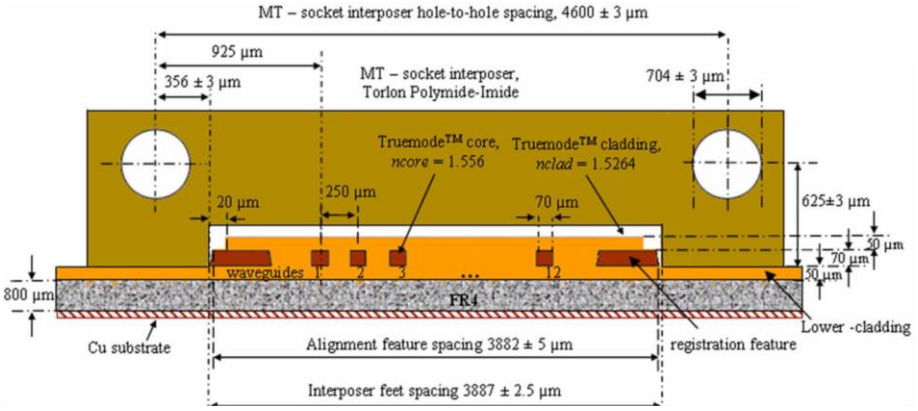


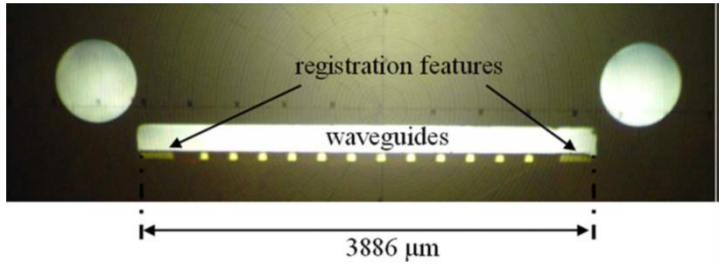


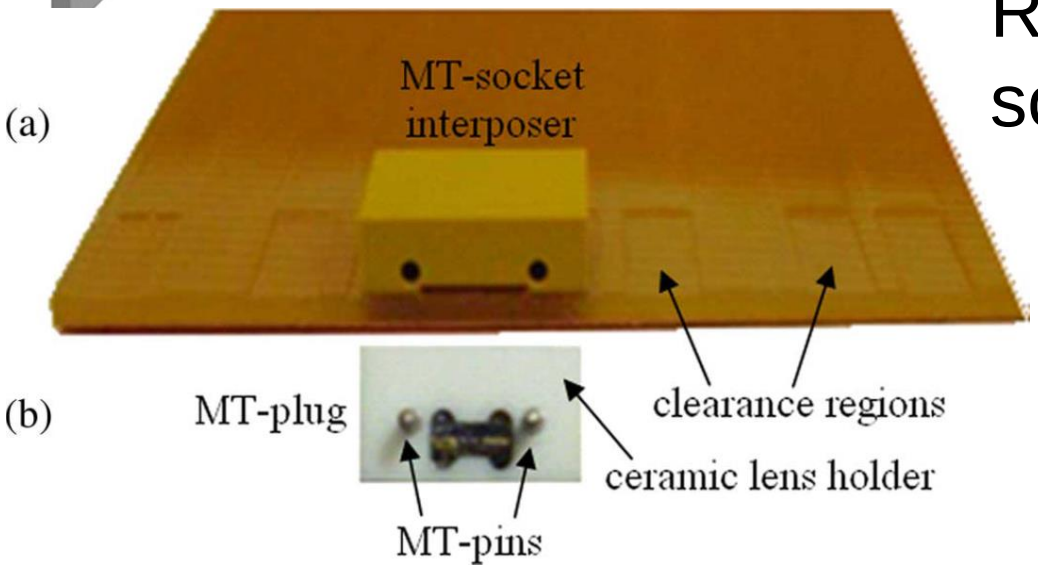
Low Cost Passive Precise connector alignment



xyratex







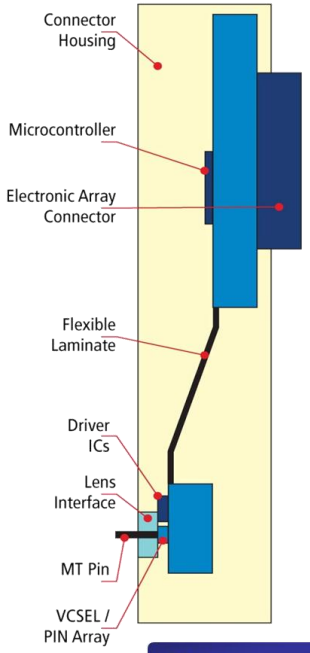
Repeatable alignment accuracy socket to waveguides

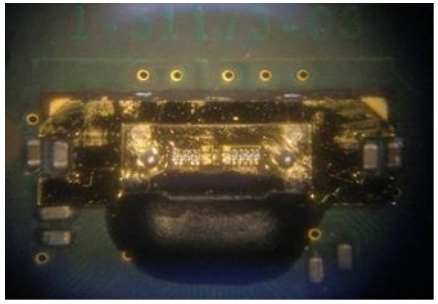
X ±3 microns

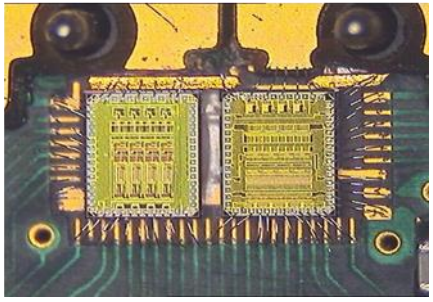
Y ±4 microns

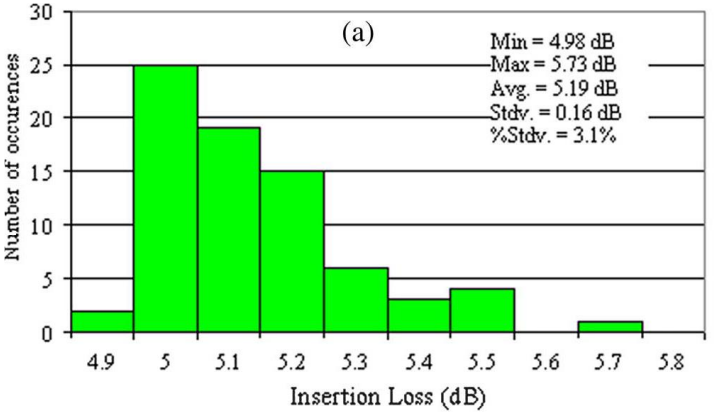
Z ±10 microns

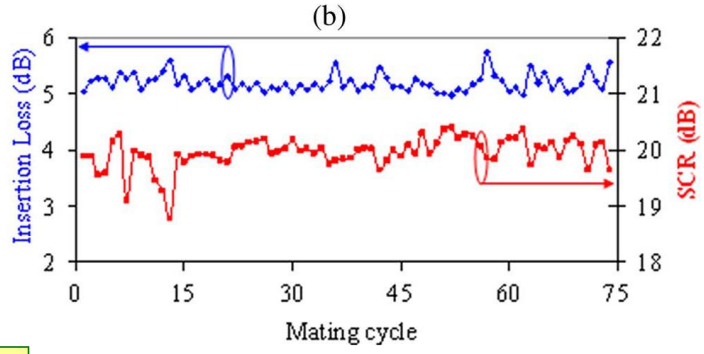
80 Gb/s Aggregate Connector Design and Performance

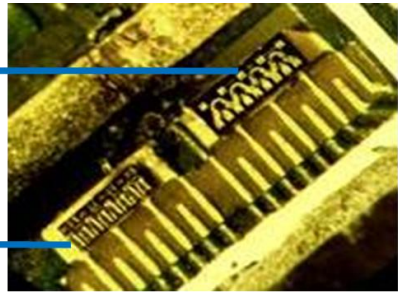


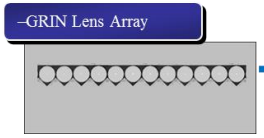


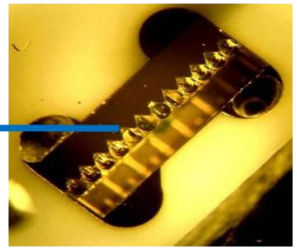


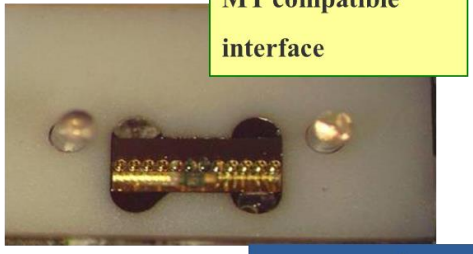






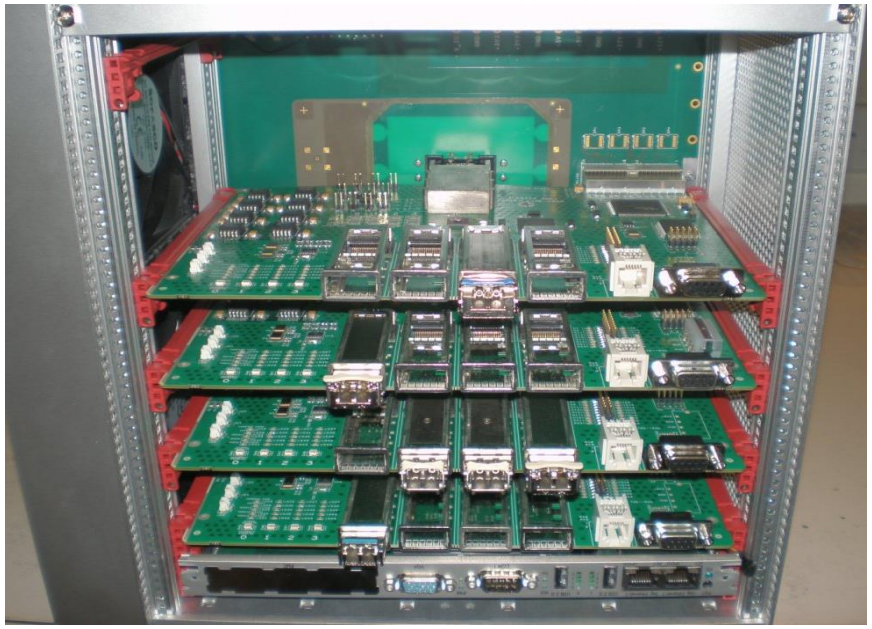


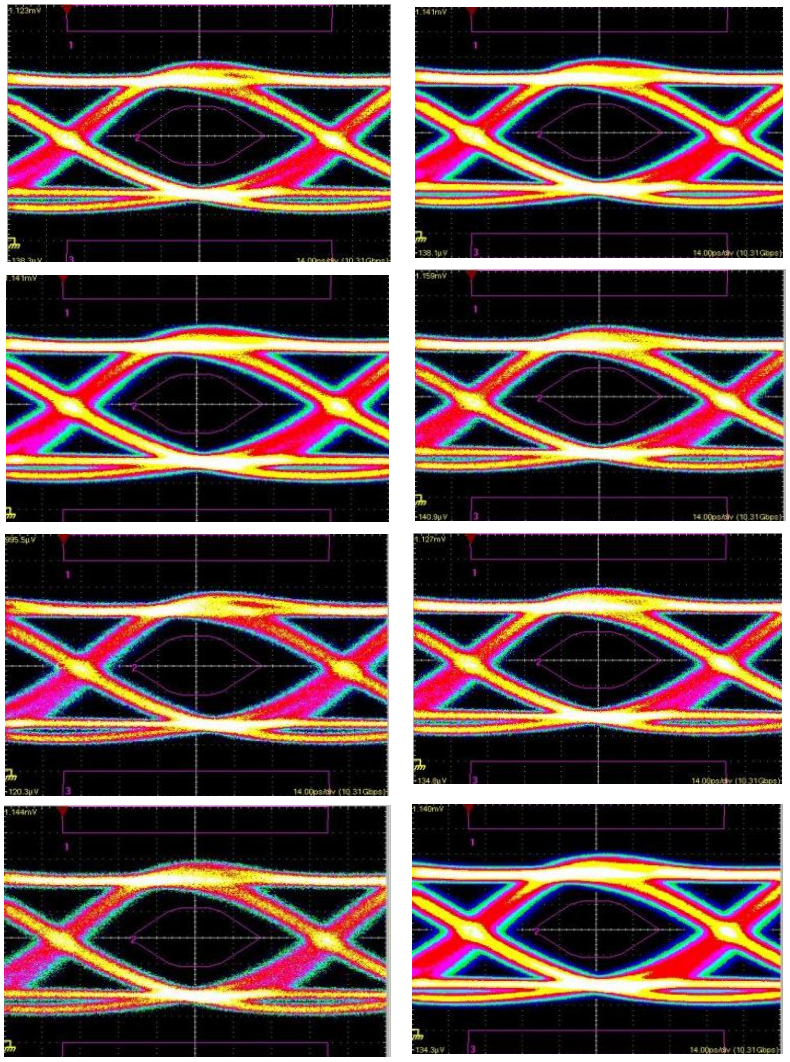




xyratex

Rack based optical backplane system performance





Test data measured on 8 waveguides

- Data rate: 10.3 Gb/s
- Typical Pk to Pk jitter: 26 ps

BERT on all waveguides

- Measured by UCL and Xyratex on all waveguides
- BER less than 10^{-12} measured