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Xueying Yu,^{1,a)} Hui Jia,^{1,a)} Wenyu Hu,² Chong Chen,¹ Haotian Zeng,¹ Mateus G. Masteghin,³ Makhayeni Mtunzi,¹ Huiwen Deng,¹ Yutong Zhang,¹ Suguo Huo,⁴ Mingchu Tang,¹ Xiaoyi Wang,⁵ Yang Qiu,⁶ Alwyn Seeds,¹ and Huiyun Liu¹

AFFILIATIONS

¹ Department of Electronic and Electrical Engineering, University College London, Torrington Place, London WC1E 7JE, United Kingdom

² Department of Physics, Southern University of Science and Technology, Shenzhen 518055, China

³ DTU Nanolab, Technical University of Denmark, Fysikvej, Kongens Lyngby 2800, Denmark

⁴ London Centre for Nanotechnology, 17-19 Gordon Street, London WC1H 0AH, United Kingdom

⁵ Southwest Minzu University, State Ethnic Affairs Commission, Chengdu 610041, China

⁶ Core Research Facilities, Southern University of Science and Technology, Shenzhen 518055, China

^{a)} Authors to whom correspondence should be addressed: zceexyu@ucl.ac.uk and huijia@ucl.ac.uk

ABSTRACT

Thermal cyclic annealing (TCA) is recognized as the key process in improving Ge film quality during epitaxial growth on Si substrates. In Ge-on-Si systems, annealing temperatures rarely exceed 900 °C due to the limitation of the Ge melting point (938 °C). In this study, ultra-high temperature TCA is performed on a series of 500 nm Ge buffer layers grown on Si (001), with the upper limit ranging from 900 to 950 °C. The structural properties of the Ge thin films are investigated, indicating that an optimized TCA profile occurs with the upper annealing temperature just below the melting point of Ge. Higher annealing temperature above the melting temperature of Ge results in homogeneous alloying of Ge and Si, induced by enhanced Si diffusion into Ge. This process produces a Ge_{0.75}Si_{0.25} layer with a threading dislocation density of $3.5 \times 10^8 \text{ cm}^{-2}$ and a surface roughness of 3 nm. These findings inspire a novel approach for creating Ge-rich GeSi layers on Si, which potentially benefits the Ge/GeSi/Si (001) heterostructures and their applications in advanced Si-based semiconductor devices.

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I. INTRODUCTION

The monolithic growth of Ge and GeSi thin films on Si (001) substrates has been appealing in semiconductor research due to its great potential in advanced Si-based electronic and optoelectronic applications. Ge is particularly attractive for its high carrier mobility, making it a promising material for p-channel transistors in complementary metal-oxide-semiconductor (CMOS) technology.¹ The high absorption of Ge material over a wide spectral range makes Ge an ideal candidate for realizing Si-integrated photodetectors.^{2–4} These demands have driven the development of complex Ge/Si

heterostructures, with monolithic Ge(Si)-on-Si systems being of particular interest for integrating photonic and electronic components on a single Si-based chip.^{5–7} In addition, high-quality Ge-on-Si platforms also serve as virtual substrates for the integration of III-Vs and Si, leveraging the lattice similarity between Ge and GaAs.⁸

However, the heteroepitaxy growth of Ge on Si is challenged by the 4.2% lattice mismatch, which leads to massive threading dislocation (TD) generation. The propagation of TDs through the epitaxial layer significantly degrades the structural and optoelectronic quality of Ge films. TDs penetrating the active regions act as non-radiative recombination centers, where electrons and holes

recombine with short lifetimes without emitting photons, limiting the performance of Ge-on-Si systems in device applications. Efforts have been devoted to optimizing the growth designs and techniques of the Ge(Si) on Si to enhance the structural quality, including two-step growth, doping, and high-temperature (HT) annealing.^{9–11} In particular, a wide range of annealing methods, such as continuous annealing,¹² thermal cyclic annealing (TCA),^{13,14} and rapid thermal annealing (RTA),¹⁵ have been demonstrated to improve the Ge(Si) film quality. Although the impact of annealing temperature on defect reduction has been extensively studied, most research has focused on temperatures well below the deformation point of Ge, as long-period continuous annealing above 900 °C might lead to structural damage in the Ge film.¹⁶ The high and low temperature limits in TCA are chosen arbitrarily in the existing studies, despite having a major influence on the Si–Ge interdiffusion and TD gliding velocity.

In this study, we explore the effect of increasing the high temperature limit of TCA treatment, especially on the structural and defect behavior of Ge thin films grown on Si. Five 500-nm Ge samples grown on Si (001) by molecular beam epitaxy (MBE) are subjected to *in situ* TCA with brief high-temperature holds to prevent structural damage. The high temperature limit is set to 900, 910, 920, 930, and 950 °C, respectively, which is designed to approach and exceed the melting point of Ge material to locate the highest possible temperature in TCA while preserving the structural properties. The five TCA configurations were separated into two groups for distinct research purposes. The 900–930 °C group was designed to examine how increments in TCA temperature affect the Ge epilayer quality. The optimized TCA temperature is determined accordingly, at which TDs are enabled with maximum acceleration to trigger self-annihilation, presenting the lowest TD density (TDD). This observation confirms that an optimized TCA temperature limit exists at ~10 °C below the deformation point of the Ge epilayer, which needs to be calibrated in epilayer growth design. The 950 °C TCA condition was set to assess the crystalline response of the Ge epilayer when processed at a TCA temperature just above the melting point of Ge ($T_m \approx 938$ °C). At an extreme annealing temperature above the Ge melting point, the structural and compositional properties of the Ge epilayer demonstrate significant modifications. An unexpected formation of a homogeneous Ge-rich GeSi alloy layer has been observed, which provides insights into the Si diffusion behavior within the Ge epilayer. This finding inspires a novel approach for producing high-quality homogeneous Ge-rich GeSi alloy layers on Si. This advancement holds potential for GeSi-on-Si applications, particularly in scenarios where low-defect, high-performance GeSi materials are essential.

II. EXPERIMENTAL

A. Material epitaxy growth

All samples were grown on 3-inch n-type Si (100) substrates with a 4° offcut toward (110) using a Veeco Gen-930 solid-source MBE system. The samples were preliminarily prepared by applying argon plasma for three minutes, which interacts with the oxide layer and sputters away the oxides before loading into the MBE systems.¹⁷ The Ar plasma was generated using a Diener Plasma Asher, with a chamber working pressure of 0.4 mbar, Ar fluxes of 30 SCCM, and an RF power of 300 W. An *in situ* thermal deoxidization process was performed at 1130 °C for 45 min prior to the growth to completely

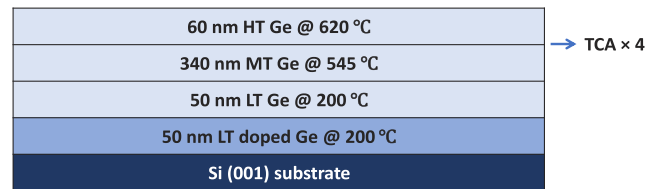


FIG. 1. Schematics of the Ge layer structure with various TCA temperatures.

remove the oxides on the substrates. The growth of Ge buffer layers followed the previously developed co-doping technique, starting with the co-doping of P and Sb in the initial 50-nm Ge nucleation layer (NL) at low temperatures (LT) by MBE,¹⁸ followed by a 50-nm LT dopants-capping layer. The growth rate of the LT layers was set to 0.5 Å/s to ensure nucleation quality. Then, the growth temperature was increased to 545 °C for the deposition of the following 340 nm Ge layer at a high growth rate at 1.5 Å/s. An *in situ* four-cycle TCA was carried out at different temperatures for each of the five samples, with the high annealing temperature (T_{high}) being 900, 910, 920, 930, and 950 °C and the low (T_{low}) being 600, 610, 620, 630, and 650 °C, respectively, as illustrated in Fig. 1. The growth and annealing temperatures were controlled by the Veeco MBE system's thermocouple setting and directly monitored using the thermocouple readings. The temperature difference between T_{high} and T_{low} was set consistently to 300 °C for all samples. After annealing, a HT Ge layer is grown at 620 °C with a growth rate of 1.5 Å/s. The total thickness of all Ge samples was 500 nm.

B. Temperature measurement and uncertainty

Temperatures reported in this study refer to the thermocouple-based readings. Standard infrared pyrometers were not used because Ge and Si are partially transparent at typical pyrometer wavelengths, making direct surface temperature measurements inaccurate without additional surface coatings or emissivity corrections. Given the limitations in the precision of thermocouple-based readings, the relative consistency of the temperature steps is maintained across samples. Prior to the experiments, the temperature reading was calibrated against the Ge melting point to minimize the uncertainty.

C. Characterization

The surface morphologies of the samples were revealed by Bruker atomic force microscopy (AFM), and the estimation of dislocation density was performed by the electron channeling contrast imaging (ECCI) technique in scanning electron microscopy (SEM). The crystallography of the Ge sample was analyzed via high-resolution x-ray diffraction (HR-XRD). The Raman spectra were obtained using a Renishaw inViaTM Raman spectrometer at room temperature with an excitation wavelength of 633 nm, allowing access to the structural and compositional properties of the samples. To investigate the local structure and chemistry of the Ge epilayer grown on the 950 °C TCA buffer, a cross-sectional transmission electron microscopy (TEM) specimen was prepared by focused ion beam (FIB) thinning using Thermo Fisher Helios 600i, and the bright field imaging was carried out in a Thermo Fisher Talos F200X

G2 scanning transmission electron microscope. The energy dispersive x-ray (EDX) elemental maps were recorded from Super-X silicon drift detectors, where the energy resolution and collection angle were 136 eV and 0.9 sr, respectively.

III. RESULTS

A. TCA temperature optimization for the Ge epilayer

The large lattice mismatch between Ge and Si creates strain in the epitaxial layer, which is initially accommodated elastically and accumulates as the Ge layer thickness increases. When the Ge layer reaches a critical thickness, the strain relaxes elastically by inducing a rough surface or plastically by generating high-density TDs.¹⁹ TCA is a widely used technique to improve the quality of Ge epilayers grown on Si substrates by repeatedly heating and cooling the sample to promote strain relaxation and TD annihilation.^{13,14} In this study, TCA is applied to five samples with annealing profiles shown in Fig. 2, ranging from 600–900 to 650–950 °C. During the temperature increment in each annealing cycle, the gliding of TDs is thermally

motivated,^{20,21} increasing the probability of self-annihilation and escaping from the sample edge during the holding period at T_{high} . Inserting a cooling step between high temperature holds allows thermal stress to reaccumulate due to the thermal expansion mismatch between Ge and Si. This renewed thermal stress provides a driving force for dislocation gliding in the subsequent heating cycle and stimulates the formation of dislocation loops, contributing to sustained surface TD reduction.

The structural defects in 500 nm Ge layers with different annealing temperatures are studied to address the impact of TCA on TDD and surface quality. To determine the temperature-dependent surface roughness and TDD, Fig. 3(a) compares the root mean squared (RMS) values of the surface roughness and TDD of the Ge samples annealed at various temperatures. The RMS roughness is a statistical measure of the height variations of a surface, which can be calculated by the given function²²

$$S_q = \sqrt{\frac{1}{A} \iint_0^A Z^2(x, y) dx dy}, \quad (1)$$

where $Z(x, y)$ is the surface height function at coordinates (x, y) , A is the area over which the roughness is being measured, and the integral computes the mean of the squared deviations of the surface height over the area. The TDD is estimated by taking the pits count in each ECCI scan over the corresponding scan area. The average RMS roughness and TDD values are measured across multiple surface areas via AFM and ECCI, with error bars calculated from standard error. The as-grown Ge layer exhibits the smoothest surface, with an RMS roughness of about 0.53 nm, but suffers the highest TDD ($\sim 8 \times 10^8 \text{ cm}^{-2}$), as illustrated in Figs. 3(b) and 3(c). The strain accumulated in the Ge epilayer due to lattice mismatch is mainly released via plastic relaxation (i.e., TD generation) when annealing is not performed.²³ According to Fig. 3(a), a considerable reduction in TDD occurs when TCA is employed, whereas the surface roughness of these samples significantly increases. The TDD declines as the annealing temperature increases up to 920 °C, where the TDD reaches a minimum. The reduction can be attributed to the increased TD mobility at a higher temperature, promoting TD annihilations. The gliding of TDs can be activated by thermal stress, which is

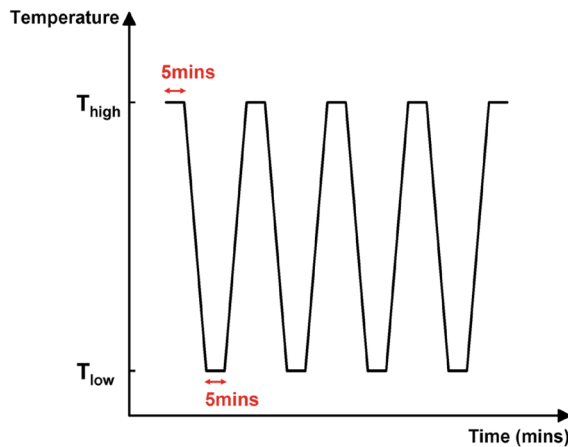


FIG. 2. Annealing profile of the Ge samples, where T_{high} is equal to 900, 910, 920, 930, and 950 °C and T_{low} is equal to 600, 610, 620, 630, and 650 °C, respectively.

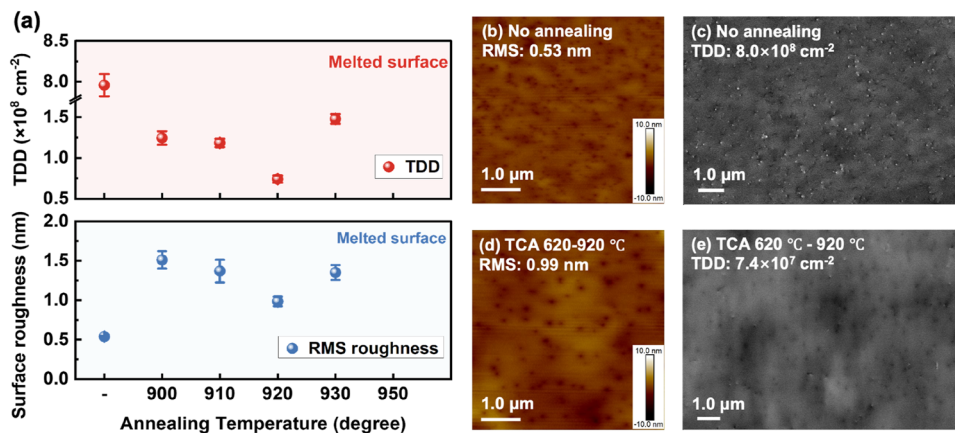


FIG. 3. (a) Upper: Threading dislocation density and lower: surface RMS roughness with respect to increasing annealing temperature, indicating the optimized annealing window is between 620 and 920 °C. (b) Representative $5 \times 5 \mu\text{m}^2$ AFM scan and (c) $7.13 \times 10.8 \mu\text{m}^2$ ECCI scan of the Ge sample without annealing treatment. (d) $5 \times 5 \mu\text{m}^2$ AFM scan and (e) $7.13 \times 10.8 \mu\text{m}^2$ ECCI scan of the Ge sample with TCA treatment between 620 and 920 °C.

introduced by the coefficient of thermal expansion (CTE) mismatch between Si and Ge during heating and cooling, with expression of a function of T_{high} and T_{low} . Values of thermal strain accumulated in the Ge layers during TCAs have been obtained by theoretical calculations and experiments.^{24,25} The thermal strain accumulation strongly depends on the temperature difference between T_{high} and T_{low} . A temperature rise of 300 °C from T_{low} to T_{high} is set to be consistent in our experiment to allow comparable thermal strain (γ) accumulation for each Ge sample. TD velocity can be described as a function of thermal stress (τ) and annealing temperature (T),

$$v = v_0 \left(\frac{\tau}{\tau_0} \right)^m \exp \left(-\frac{Q}{kT} \right), \quad (2)$$

where v_0 , τ_0 , m , and Q for Ge are $2.93 \times 10^2 \text{ ms}^{-1}$, 1 MPa, 1.7, and 1.62 eV, respectively, with k being the Boltzmann constant.^{26,27} Accordingly, TDs are expected to be accelerated when the annealing temperature increases, potentially leading to boosted TD eliminations. The TDD in the sample annealed with T_{high} at 920 °C is significantly reduced by nearly an order of magnitude to $\sim 6.2 (\pm 0.6) \times 10^7 \text{ cm}^{-2}$, as measured by ECCI in Fig. 3(e). However, further increasing T_{high} to 930 °C does not further reduce TDD, according to Fig. 3(a), although the TD mobility is expected to be exaggerated. The surface roughness of the Ge samples, on the other hand, rises when TCA is applied. The unannealed Ge layer reveals a rather smooth surface with an average roughness of 0.53 nm in a $5 \times 5 \mu\text{m}^2$ AFM scan, as shown in Fig. 3(b). For all TCA-treated samples, the surface is about the same roughness level, with only a slight decrease to 0.99 (± 0.1) nm at T_{high} of 920 °C, as shown in Fig. 3(d). Once the annealing temperature (950 °C) exceeds the melting point of Ge (938 °C), significant changes in surface morphology are observed. The sample morphology investigated by AFM and ECCI scans

is given in Figs. 4(a) and 4(b), respectively, where pronounced Ge ridges and islands are observed on the sample surface. The island growth of the Ge layer is generally due to the strain-driven Stranski–Krastanov (SK) growth mode, which is distinct from other samples with layered growth mode. This observation suggests that annealing at 950 °C leads to a structural and compositional modification to the Ge layer. This observation suggests that the compositional modification could trigger the formation of interface strain between the Ge buffer and the capping epilayer, resulting in the structural distortion of the Ge cap layer. Another sample without the HT-grown Ge cap layer is prepared to examine the effect of the 950 °C annealing on the Ge epilayer structural properties, whose surface morphologies are presented in Figs. 4(c) and 4(d). The AFM scan in (c) describes a sample surface without the Ge islanding, giving an RMS surface roughness of 3.2 nm. The ECCI image in (d) estimates the surface TDD to be $3 \times 10^8 \text{ cm}^{-2}$. A detailed structural investigation of the Ge sample under 950 °C annealing is necessary and will be presented in detail in Secs. III B and III C.

B. Compositional evolution of Ge layers under HT TCA

To evaluate the strain and crystalline quality of Ge layers grown on Si (001) upon TCA with increasing temperatures, high-resolution x-ray diffraction (HR-XRD) analysis has been conducted on the group of Ge samples. Figure 5 illustrates the strain evolution with increasing annealing temperature by taking the omega-2theta scans on the (004) plane of the Ge-on-Si samples. The inserts on the right present the peak positions and the full width at half maximum (FWHM) of the Ge reflections. Note that the legend labels in the XRD plots represent the T_{high} in the TCA profiles.

The symmetric Ge peak with strong intensity of the as-grown sample suggests good crystallinity of the Ge film. This peak appears

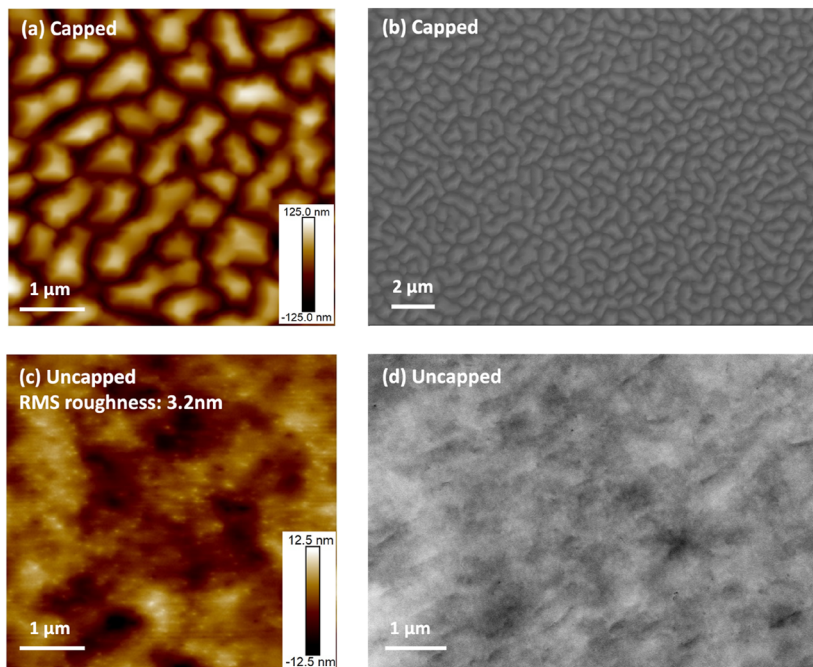


FIG. 4. Ge sample surface with TCA between 650 and 950 °C. (a) Representative $5 \times 5 \mu\text{m}^2$ AFM scan, (b) $7.13 \times 10.8 \mu\text{m}^2$ ECCI scan of the HT Ge capped sample, demonstrating Ge ridges and islands due to SK growth mode. (c) Representative $5 \times 5 \mu\text{m}^2$ AFM scan and (d) $7.13 \times 10.8 \mu\text{m}^2$ ECCI scan of the uncapped sample.

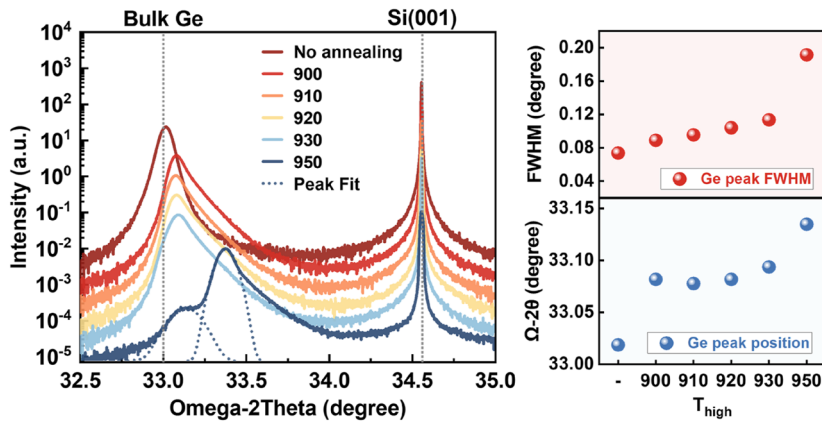


FIG. 5. HR-XRD measurements of samples without annealing and with TCA with T_{high} of 900, 910, 920, 930, and 950 °C, respectively. The insert illustrates the full widths at half maximum and the omega-2theta positions of the Ge reflections, where the values for the 950 °C curve are estimated from the peak fitting indicated as the dotted lines.

at a slightly higher angle than that of bulk Ge, indicating slight tensile stress remaining in the as-grown Ge layer after cooling from HT growth due to the larger CTE of Ge compared to Si. When the TCA is employed, the peak position shifts toward a larger angle, suggesting that a higher tensile strain of about 0.22% is accumulated during the TCA. For T_{high} of 900, 910, and 920 °C, the Ge peak positions remain consistent, indicating comparable strain accumulations—supporting the previous discussion on the consistent strain accumulation with the same temperature difference between T_{high} and T_{low} . On the other hand, the asymmetry of the Ge peaks for the annealed samples is attributed to the strong Ge-Si intermixing upon annealing. The Ge peaks broaden with higher TCA temperatures, as shown in the inset FWHM plot, indicating enhanced intermixing of Ge and Si as the TCA temperature increases. Note that the values of peak position and FWHM of the 950 °C annealed sample are estimated from the peak fitting indicated as the dotted lines in Fig. 5. At T_{high} of 930 °C, the peak broadening and sign of splitting on the left side of the Ge peak imply a degradation in the crystalline quality of the Ge layer. This aligns with the previous observations of higher TDD and surface roughness in the Ge layer annealed at T_{high} of 930 °C. As the annealing temperature exceeds the melting point of Ge and initiates the Ge melting behavior, a peak corresponding to the formation of a GeSi layer appears between the Ge and Si peaks. A simultaneous intensity drop and peak broadening of the Ge reflection also suggest substantial changes in the structure and composition of the Ge epilayer. The Ge content in this GeSi alloy layer can be estimated based on Bragg's law: $\lambda = 2d \sin \theta$, where $\lambda = 1.5406 \text{ \AA}$ for Cu K α radiation, and θ is derived from the GeSi peak position. The calculated perpendicular lattice constant of the GeSi layer is $\sim 5.60 \text{ \AA}$, suggesting a Ge content of roughly 75%.

Raman spectroscopy has been carried out to further investigate the compositional properties of the Ge samples. An incident wavelength of 633 nm has been used in the measurement of all Ge samples. Figure 6(a) shows Raman spectra from 100–600 cm^{-1} for all samples with different TCA profiles, with the Ge-Ge optical vibration mode highlighted in Fig. 6(b). The Ge layer annealed at 950 °C has a main Ge peak at 300–301 cm^{-1} associated with a separate and less-intensive peak at a lower wavenumber, while other samples have consistent peak positions slightly below 300 cm^{-1} . The relation between the peak shift and the in-plane strain has

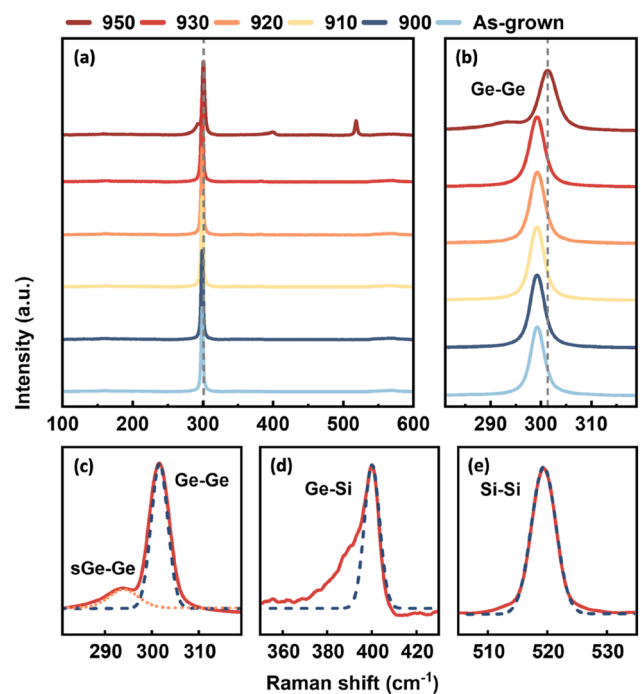


FIG. 6. (a) Raman spectra using 633 nm excitation wavelength of the Ge layers annealed at different temperatures. (b) Zooming in at the Ge-Ge vibration modes. (c)–(e) Amplified peaks of the Ge-Ge, Ge-Si, and Si-Si vibration modes of the Ge sample treated with TCA between 650 and 950 °C, respectively. The dotted lines are the Gaussian fittings of the peaks.

been well established by equations reported in Ref. 28. Compared to the known position of the Ge-Ge mode for bulk Ge material ($\sim 301 \text{ cm}^{-1}$), the Ge layers with T_{high} below 930 °C suggest slight tensile strain in the in-plane direction.²⁹ The residual in-plane tensile strain in the Ge layer is induced by the cooling down from HT growth under the influence of the larger CTE of Ge compared to the Si substrate, which agrees well with the XRD results demonstrated earlier.

Significant changes are observed in the Raman spectra for the sample annealed at 950 °C, including the emergence of additional vibrational bonds and the upshifting and splitting of the Ge–Ge mode, indicating substantial structural and compositional modifications in the Ge layer. Figures 6(c)–6(e) magnify the additional vibrational modes and present the Gaussian fittings of Ge–Ge, Ge–Si, and Si–Si bonds, respectively. The composition of the Ge sample can be deduced from the peak positions of the vibration modes. As shown in Fig. 6(d), the Ge–Si vibration mode is detected at $\sim 401 \text{ cm}^{-1}$, corresponding to a Ge content of 75%,³⁰ which is in good agreement with the XRD result. The Ge–Ge mode of the 950 °C annealed Ge sample shifts to a larger wavenumber, along with the appearance of a secondary Ge–Ge mode at 290–295 cm^{-1} , as shown in Figs. 6(b) and 6(c). The high-frequency phonon peak at 301 cm^{-1} is attributed to bulk Ge, while the low-frequency mode is attributed to the Ge content in the formed GeSi alloy. The Ge peak corresponding to the Ge content in the GeSi alloy shifts $\sim 7 \text{ cm}^{-1}$ from the bulk Ge mode, also corresponding to a Ge content of 75%.³¹ The Si–Si vibration mode at 520 cm^{-1} matches with unstrained Si, which corresponds to the detection of the Si substrate. The penetration depth of the 633 nm laser is $\sim 30 \text{ nm}$ in bulk Ge and $\sim 3000 \text{ nm}$ in bulk Si.³² Therefore, a penetration depth of over 500 nm supports the formation of the GeSi film upon the exaggerated intermixing of Ge and Si. Note that a Si–Si mode that should have been attributed to the GeSi alloy has not been observed in the Raman spectrum. The absence of the Si–Si peak has been reported for the Ge-rich thick GeSi alloy in other studies.³¹ The distinct detection of Ge and GeSi peaks in both HR-XRD and Raman measurements suggests that the grown Ge layer may be separated into two regions of structures with different compositional properties upon annealing at 950 °C.

Raman spectroscopy is also carried out to evaluate the compositional property of the 950 °C annealed sample without the HT cap Ge, as shown in Fig. 7, where (b)–(d) are the magnified vibration modes of Ge–Ge, Ge–Si, and Si–Si, respectively. With the absence of the Ge cap layer, the Ge–Ge mode corresponding to the Ge layer at $\sim 301 \text{ cm}^{-1}$ vanishes, while the Ge–Ge mode at 290–295 cm^{-1}

representing the Ge content in the $\text{Ge}_{0.75}\text{Si}_{0.25}$ becomes more pronounced in comparison with the Raman spectrum demonstrated in Fig. 6. The Ge–Si mode at $\sim 401 \text{ cm}^{-1}$ verifies that a homogeneous $\text{Ge}_{0.75}\text{Si}_{0.25}$ alloy layer has been produced due to the significant diffusion of Si into Ge. Removing the Ge cap layer enhances the detection of the Si substrate, as indicated by the increased Si–Si peak intensity.

C. Homogeneous GeSi alloying under TCA above Ge melting temperature

To confirm the presence of two distinct layers during the growth of a Ge epilayer on Si, TEM was used to examine the structure of the annealed Ge epilayer beyond the Ge melting temperature. As shown in Fig. 8(a), the high-angle annular dark field (HAADF) image reveals two separate structural regions: a flat layer followed by an island formation, divided by a sharp interface. Since HAADF contrast is proportional to the atomic number squared (Z^2), the darker region near the structural interface may indicate the presence of a lighter material (e.g., Si) rather than a thickness variation, whereas no obvious thickness contours were observed between the structural regions.

Elemental maps of Si and Ge in Figs. 8(b) and 8(c) indicate the co-existence of Ge and Si in the flat layer region, resembling a possible formation of GeSi binary alloy. To confirm this, valence electron energy loss spectroscopy (VEELS) was applied to analyze the local chemical composition across the Ge/SiGe heterostructure, as shown in Fig. 8(d).³³ The plasmon loss spectrum from the island region exhibits a peak at 15.61 eV, confirming the presence of pure Ge. The VEEL spectrum in the flat layer shows a single plasmon peak, where the peak energy (15.72 eV) was located between pure Si (16.7 eV) and Ge (15.6 eV), suggesting the formation of a GeSi alloy.³⁴

Si has a high diffusion coefficient in Ge as a result of the vacancy-assisted diffusion mechanism, which allows Si to diffuse a length of hundreds of nm in Ge.³⁵ The diffusivity of Si upon annealing is strongly related to the annealing temperature, which can be expressed as an Arrhenius expression

$$D = D_0 \exp\left(-\frac{E_a}{kT}\right), \quad (3)$$

where E_a is the activation energy, D_0 is the exponential factor, T is the annealing temperature, and k is the Boltzmann constant. An increase in thermal budget increases Si diffusivity, extending the diffusion tail and the thickness of the graded GeSi interface.^{36,37} While Ge–Si interdiffusion is well-documented, our findings show that an even GeSi alloy layer was formed with a sharp interface between the GeSi layer and the Si substrate. This contradicts the typical graded GeSi interface formed through typical Ge–Si interdiffusion.^{38,39} Our result implies that Si concentration tends to saturate at 25% in the alloy layer formed by Si diffusion into Ge, which may be explained by the concentration-dependency of the Si diffusivity in Ge. The Boltzmann–Matano method suggested that the Si diffusion coefficient in Ge can be given as a function of the Ge concentration.⁴⁰ Previous studies show that the Si concentration consistently reaches $\sim 75\%$ at the original hetero-interface in the Ge–Si interdiffusion profiles, regardless of the annealing thermal budget.⁴¹ In addition, Si diffusivity decreases exponentially as Ge content decreases until it reaches $\sim 75\%$, where the rate of decline slows.^{41,42} Therefore, the Si

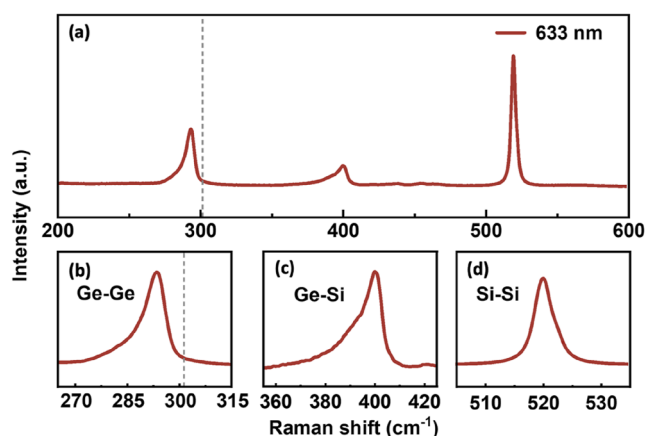


FIG. 7. (a) Raman spectra using 633 nm excitation wavelength of the Ge layers annealed with T_{high} of 950 °C, without top Ge layer. (b)–(d) Zooming in at the (b) Ge–Ge, (c) Ge–Si, and (d) Si–Si vibration modes of the Ge sample treated with TCA between 650 and 950 °C, respectively.

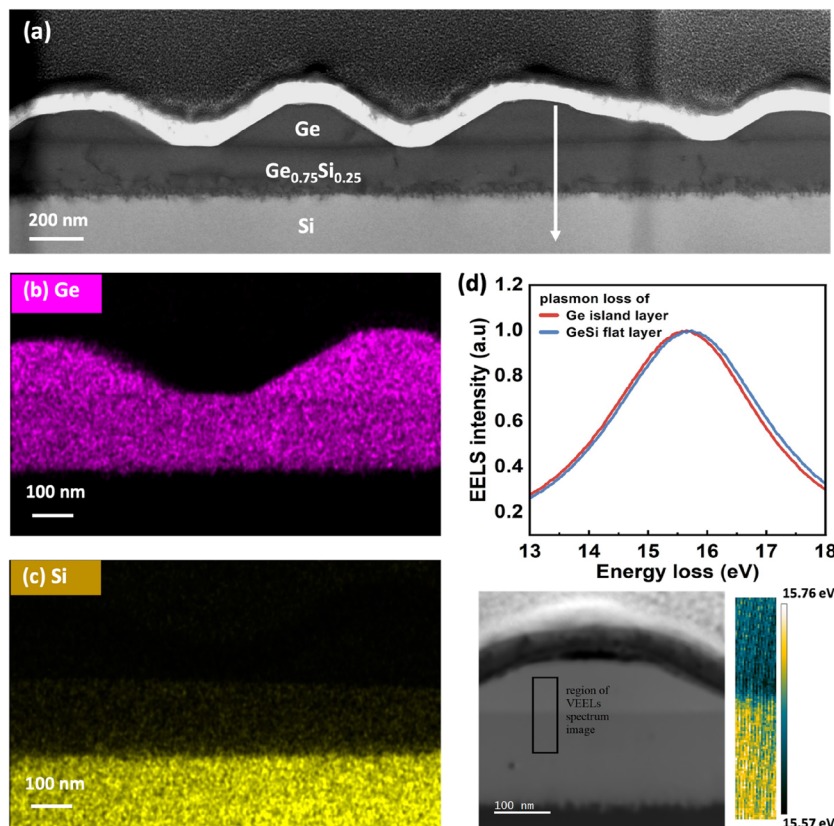


FIG. 8. (a) High angle annular dark field (HAADF) image of the Ge epilayer with TCA between 650 and 950 °C, presenting a flat layer with a subsequent island formation. (b) and (c) The energy dispersive x-ray (EDX) spectroscopy describing the elemental distribution of Ge and Si, respectively. (d) Spectrum of plasmon loss in valence electron energy loss spectroscopy (VEELS).

diffusion is likely to be retarded when the Si concentration reaches 25%. When the diffusion of Si is initiated, one can consider it diffusing into pure Ge with the largest diffusion coefficient at a given annealing thermal budget. Subsequently, the Ge content near the Ge/Si interface starts to decrease as the Si atoms incorporate, leading to a reduction in the diffusion coefficient of Si. Considering suppressed Si diffusion at the interface and exaggerated diffusion at the Ge-rich diffusion front, uniform alloying could be achieved by initiating Si diffusion repeatedly with multiple cycles of annealing. As a result, a compositionally uniform $\text{Ge}_{0.75}\text{Si}_{0.25}$ layer with a thickness of over 100 nm is produced. TCA instead of continuous annealing is selected to limit the peak-temperature exposure during the annealing treatment, which improves reproducibility and mitigates the risk of melt-mediated structural modifications and potential chamber contamination when operating above the melting point of Ge. While a single 950 °C/20 min annealing may produce similar alloying in principle, TCA is chosen here as it permits thermal-strain reaccumulation between cycles and offers a more controlled *in situ* annealing above the Ge melting point.

Figure 9 gives an EDX intensity line profile across the white arrow in Fig. 8(a), which confirms the uniformity of the GeSi alloy layer over a thickness of ~100 nm. HT annealing above the Ge melting point would also cause segregation and sublimation of the Ge atoms, evidenced by the dramatic reduction in thickness from 440 nm deposition to a produced GeSi layer of just over 100 nm. It is also worth noticing that an accumulation of Si atoms is detected

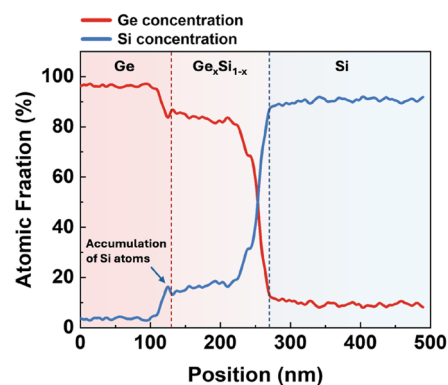


FIG. 9. EDX measurement of the concentration profile in the Ge sample with TCA between 650 and 950 °C. The $\text{Ge}_x\text{Si}_{1-x}$ alloy layer has a uniform Ge content, along with abrupt interfaces with the Si substrate and Ge islands. A mild accumulation of Si atoms is observed at the interface of GeSi and Ge.

at the diffusion front of the $\text{Ge}_{0.75}\text{Si}_{0.25}$ layer, which suggests that the diffused Si atoms would rather accumulate at the surface of the alloy layer instead of incorporating into the alloy layer. TDs can move in two ways—climb and glide. TD encounter and escape primarily occur through gliding on {111} planes. Climbing, on the other hand, involves point defects moving toward or away from the TD

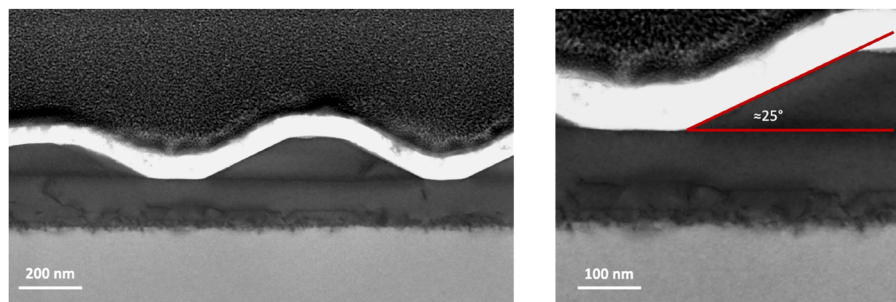


FIG. 10. Cross-sectional TEM image of the Ge domes with {113} facets upon Ge growth of 630 °C on a $\text{Ge}_{0.75}\text{Si}_{0.25}$ layer.

core, resulting in movement of the dislocation, which is limited to extreme conditions, such as temperatures near the melting point.¹⁹ Ultra HT annealing is therefore likely to facilitate additional TD movement, resulting in a low TDD. As a result, applying HT cyclic annealing slightly above the melting point of Ge has led to the production of a thin Ge-rich homogeneous GeSi layer with TDD of $3 \times 10^8 \text{ cm}^{-2}$ and surface roughness of around 3 nm, which may potentially benefit applications requiring Ge-rich GeSi-on-Si systems, such as strained GeSi/Ge quantum wells for transport studies and high-mobility devices,⁴³ and modulators and photodetectors.⁴

According to the structural design in Fig. 1, 60-nm HT Ge is deposited following the TCA process, resulting in the SK growth of Ge on the $\text{Ge}_{0.75}\text{Si}_{0.25}$ layer with a $\sim 1\%$ lattice mismatch, forming the Ge islands and ridges. The Ge ridges induced by the HT SK growth mode exhibit a single-faceted nature highlighted by TEM images in Fig. 10. The facets indicate an inclination of $\sim 25^\circ$ with respect to the (001) substrate, corresponding to {113} facets, as described in Fig. 10(b). The observed Ge ridges are bounded by multiple {113} facets plus a (001) facet on top, which agrees with the trend in surface energies for relaxed Ge facets, where {113} is the most and {001} is the second most energy favorable facet.⁴⁴ The TEM images also reveal the low-defect feature of the Ge islands due to the mild lattice mismatch with the underlying Ge-rich GeSi film. These self-assembled {113} faceted Ge nanostructures present great potential for the integration of III-V on Si, where adjacent facets play the role of antiphase domain annihilation.^{45,46} In addition, high-quality Ge nanocrystals can possibly be achieved by adjusting the deposition rate and thickness of the HT Ge, presenting opportunities for Ge/GeSi on Si applications, particularly light-emitting devices such as Ge quantum dots embedded in a (Ge)Si matrix.⁴⁷

IV. CONCLUSION

The study explores the upper temperature limit of TCA for Ge thin films grown on Si (001) substrates, aiming to maximize annealing efficiency while preserving the structural integrity of the Ge epilayer. By examining TCA with upper intervals between 900 and 950 °C, an optimized TCA temperature was identified, 10–20 °C below the deformation point of the Ge film. In addition, the study reveals that annealing above the Ge melting point significantly enhances Si diffusion into the Ge epilayer, with Si concentration saturating at 25%. Instead of a typical Si diffusion tail in the Ge epilayer, the TCA between 650 and 950 °C has resulted in the formation of a homogeneous $\text{Ge}_{0.75}\text{Si}_{0.25}$ alloy layer on the Si substrate. The uniformity of the alloy layer is attributed to the Ge

concentration-dependency of Si diffusion in the Ge epilayer and the re-established diffusion process enabled by the cyclic annealing. These findings introduce a novel method for fabricating Ge-rich GeSi layers on Si, offering potential for advancing Ge/GeSi/Si (001) heterostructures in Si-based optoelectronic applications.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Xueying Yu: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Writing – original draft (equal). **Hui Jia:** Data curation (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Wenyu Hu:** Data curation (equal); Methodology (equal); Validation (equal); Writing – review & editing (equal). **Chong Chen:** Data curation (equal); Methodology (equal). **Haotian Zeng:** Methodology (equal). **Mateus G. Masteghini:** Methodology (supporting); Validation (supporting). **Makhayeni Mtunzi:** Methodology (equal). **Huiwen Deng:** Methodology (equal). **Yutong Zhang:** Methodology (supporting). **Suguo Huo:** Methodology (equal); Resources (equal). **Mingchu Tang:** Supervision (equal); Validation (equal); Writing – review & editing (supporting). **Xiaoyi Wang:** Investigation (supporting); Resources (equal); Supervision (supporting); Validation (equal); Writing – review & editing (equal). **Yang Qiu:** Resources (supporting); Supervision (supporting). **Alwyn Seeds:** Resources (supporting); Supervision (supporting). **Huiyun Liu:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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