An Area-Efficient, Differential Resonant Ultrasound Pulser with 69% fCV^2 Dynamic Power Reduction

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Abstract—This paper presents a scalable, differential resonant pulser for wearable/portable ultrasound applications, such as hand gesture recognition for prosthesis control and gaming. Presently, the mainstream pulser topologies include the class-D amplifier, multi-level pulse shaping, charge-recycling, and LC-resonant. A resonant pulser topology is adopted because theoretical analysis has shown that the resonant pulser has an inherent power advantage over other types of pulsers. The current state-of-the-art resonant pulser, while achieving excellent fCV^2 power dissipation reduction, lacks scalability. This work aims to tackle this shortcoming by using high-voltage DMOS transistors in a more area-efficient manner. On average, the proposed circuit uses three DMOS transistors per single-ended transducer or six DMOS transistors per differential transducer, making the proposed circuit attractive for multi-channel systems. Post-layout simulation results show that the proposed differential resonant pulser can achieve 69% fCV^2 dynamic power reduction, which is comparable to the state-of-the-art. To the best of the authors' knowledge, the proposed differential resonant pulser for ultrasound applications is the first of its kind.

Keywords—CMOS integrated circuit, dynamic power reduction, high-voltage pulser, LC resonance, ultrasound sensing, ultrasound transducer.

I. Introduction

Ultrasound's many useful properties have made it a mainstay in today's medical technology [1]. Ultrasound is generated by driving a piezoelectric transducer with voltage pulses (typically square waves). The pulser circuit is a fundamental building block in ultrasound systems. When designing an ultrasound pulser circuit, a crucial specification to consider is its power dissipation. This is because the transducer contains an enormous parasitic capacitance, as detailed in its Butterworth-Van Dyke equivalent model. When using a conventional 2-level pulser [Fig. 1(a)], the charging and discharging of this parasitic capacitance can incur prohibitively large fCV^2 dynamic power dissipation. Conventional 2-level pulsers have been implemented using level shifters and a class-D output stage in [2], [3].

To reduce the unacceptably large fCV^2 power dissipation, three different categories of pulsers have been proposed – multi-level [Fig. 1(b)), charge recycling [Fig. 1(c)], and resonant pulsers [Fig. 1(d)]. Multi-level pulsers [4], [5] aim to decrease power dissipation by reducing the *average* voltage step. By breaking down the overall voltage swing into multiple steps, the capacitance only needs to be charged up a fraction of the overall voltage swing in each step. With N steps, it has been shown that the power dissipation will be reduced to P/N, where P is the conventional 2-level pulser power dissipation [4].

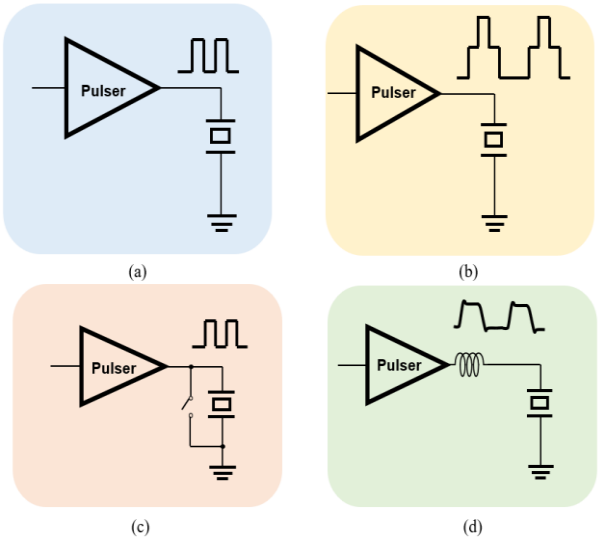
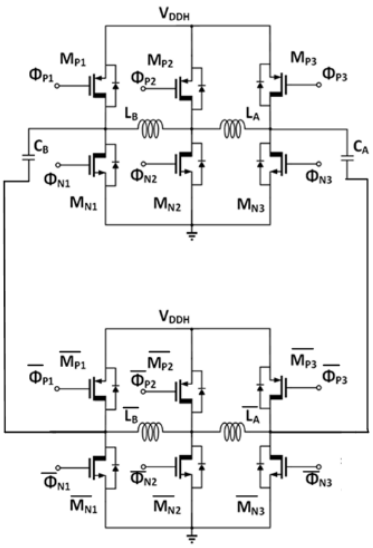


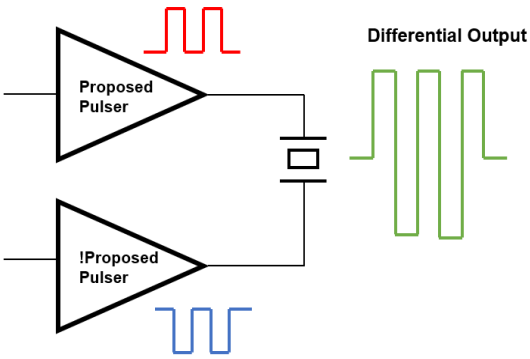
Fig. 1. Various types of pulsers. Note that the transducer is normally modelled by a large parasitic capacitance. (a) Conventional 2-level pulser [2], [3]. (b) Multi-level pulser [4], [5]. (c) Charge-recycling pulser [6-8]. (d) Resonant pulser [9].

Charge recycling pulsers [6-8] are designed with the idea that during the recycling phase, the top and bottom electrodes will be shorted together, and the capacitor charge will be evenly distributed such that the potential on each electrode will be V_{DDH}. Therefore, in the next charge/discharge phase, each electrode voltage only needs to change by $V_{DDH}/2$. Theoretically, this can result in 50% reduction of fCV^2.

In a resonant pulser [9] an external inductor forms a resonant tank with the transducer's parasitic capacitance such that the energy associated with charging and discharging the capacitance can be stored in the inductor and returned to the power supply instead of dumping it wastefully to ground. The resonant pulser has an inherent, matchless advantage over other types of pulsers because it can theoretically achieve 100% fCV^2 saving by returning energy to the power supply. The fCV^2 saving that the other two types of pulsers offer are limited in theory. Multi-level pulsers would require an infinite number of steps to fully eliminate fCV^2, and charge recycling pulsers can at most have 50% fCV^2 reduction. The major disadvantage of resonant pulsers is that due to the relatively bulky off-chip inductor they cannot be deployed in ultrasound applications with stringent area constraints such as intravascular imaging required. Resonant pulsers are better suited for area-relaxed, portable ultrasound applications such as fingerprint scanners [2], hand gesture recognition [10] and even in robots/drones [6], [7].



(a)



(b)

Fig. 2. (a) Proposed pulser circuit, high voltage DMOS devices were used. L_A=L_B=2.1 µH; C_A=C_B=40 pF. (b) Differential pulser configuration. "!" symbolises antiphase operation.

This paper presents the design of an area-efficient, scalable, differential resonant pulser with 69% fCV^2 reduction for portable/wearable ultrasound applications. The rest of the paper is organised as follows. Section II discusses the proposed pulser circuit, Section III presents post-layout simulation results and Section IV concludes the paper.

II. Proposed Pulser Circuit

The proposed pulser [Fig. 2(a)] is intended to interface with differential ultrasound transducers such as bimorph piezoelectric micromachined ultrasonic transducers (PMUTs) [11], [12]. It can be reconfigured to interface with single-ended transducers. An advantage of using a differential transducer is that during the transmit phase, its top and bottom electrodes can accept two antiphase driving pulses operating at $V_{DDH}/2$ each to achieve the same overall differential swing of V_{DDH} [Fig. 2(b)]. Although differential operation requires two pulser circuits dissipating power, the quadratic dependence on V in fCV^2 means that reducing V by two times can still lead to overall fCV^2 reduction i.e. $2 \times fC(V_{DDH}/2)^2 < fCV_{DDH}{}^2$. From a system-level perspective, differential pulser operation offers a significantly smaller burden on the on-chip power management block. To elaborate

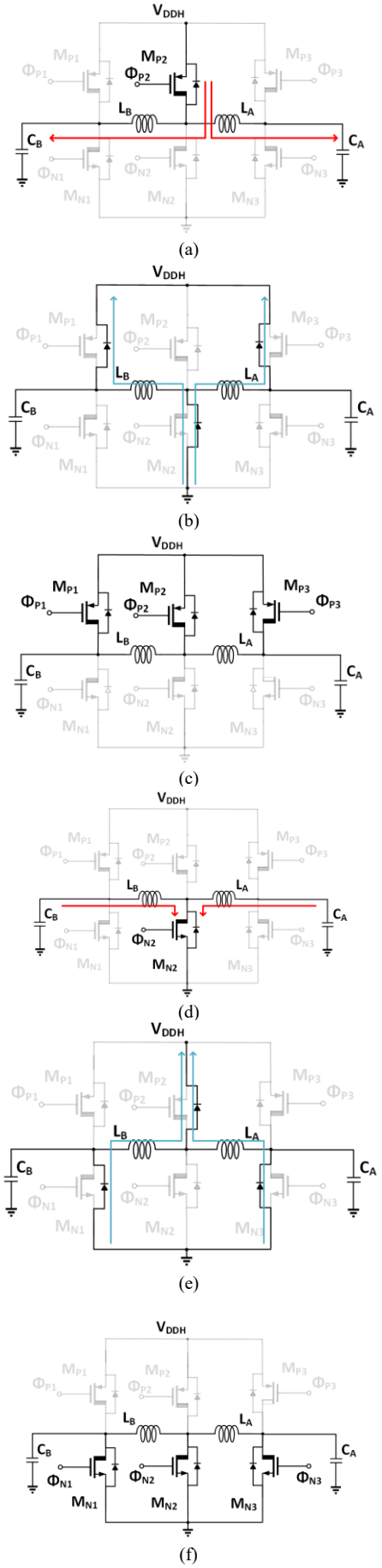


Fig. 3. Operation of the pulser in six phases.

further, if the pulser driving voltage V_{DDH} is generated on-chip using charge pumps [6] or hybrid dc-dc converters [7], then the burden on the power management block to generate 15 V rather than 30 V is very different.

A key shortcoming of the state-of-the-art resonant pulsers is that they are not scalable for differential transducers and multi-channel systems because they require four or more high-voltage DMOS transistors per single-ended transducer [9], [14]. By virtue of their construction, DMOS transistors occupy a massive amount of precious silicon die area, and where possible, the number of DMOS transistors should be minimised. The proposed pulser is designed to be scalable and area-efficient by making two circuit blocks capable of driving two differential transducers. More specifically, this means that on average, the proposed circuit requires three DMOS transistors per single-ended transducer or six DMOS transistors per differential transducer instead of at least four/eight DMOS transistors in [9], [14]. For multi-channel systems with N differential transducers, the number of DMOS transistors grows according to $6N$ for the proposed pulser, in contrast to at least $8N$ for the current state-of-the-art pulsers [9], [14]. As N increases, the area-saving benefits of the proposed pulser becomes more evident.

In this work, the transducer is modelled as a 40-pF capacitive load (C_A and C_B) as shown in Fig. 3. The resonant LC charging/discharging concept was adapted from [9]. The operation of the pulser circuit (one block) can be explained in six phases [Fig. 3]. In phase 1 [Fig. 3(a)], only M_{P2} is turned on, which charges up the inductors and capacitors from the power supply. In phase 2 [Fig. 3(b)], when the capacitor voltage reaches V_{DDH} (15 V), all DMOS transistors are turned off. With this abrupt change in inductor current, an electromotive force will be developed across the inductors to oppose this change (Lenz's law) and a current will flow back to the voltage supply in the direction indicated with blue arrows. This can be interpreted as the inductor returning its stored energy from phase 1 back to the power supply. Therefore, in phase 2, the output voltages across the capacitors C_A and C_B will be momentarily greater than V_{DDH}. This overshoot behaviour is not surprising given that this is a second-order RLC system. In phase 3, M_{P1}, M_{P2}, M_{P3} turn on to charge the capacitors to V_{DDH} and to ensure that no energy is stored in the inductors. In phase 4, the capacitors are discharged by turning on M_{N2}. Note that in this phase, the capacitor is transferring its energy into the inductor's magnetic field, charging the inductor instead of dumping the energy to ground. When the capacitor voltage reaches zero, phase 5 turns off all DMOS transistors. The change in inductor current will cause a current to flow in the direction indicated with blue arrows. Once again, the inductor will return its energy back to the power supply and a voltage undershoot will be expected at the output. Phase 5 is similar to phase 2. In phase 6, M_{N1}, M_{N2}, M_{N3} are all turned on to discharge capacitor voltages to ground and to fully discharge the inductors.

The actual sizing of transistors and inductors in this circuit is guided by fine-tuning the most important parameter for a second-order system, the damping ratio for a series resonant RLC circuit $\zeta = \frac{R}{2}\sqrt{\frac{C}{L}}$. ζ will influence the transient response of the circuit, especially the over/undershoot and rise/fall times. From [13], the approximation (1) can be used to tune the value

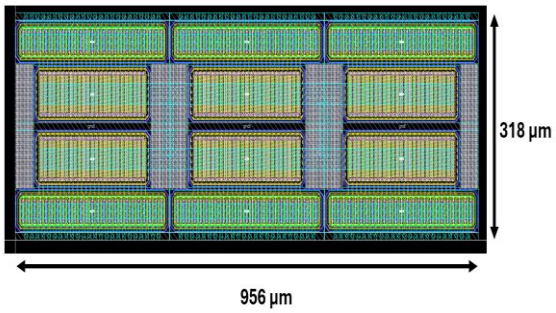


Fig. 4. Layout of the proposed pulser. 12 DMOS to drive two differential transducers.

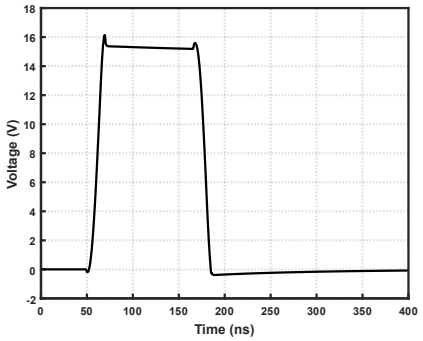


Fig. 5. Pulser output waveform for a single-ended 40-pF transducer at 3.33 MHz.

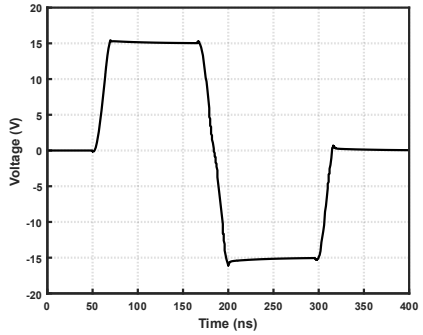


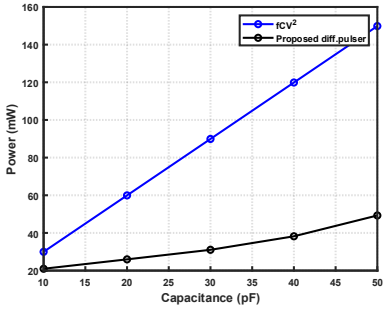
Fig. 6. Pulser output waveform for a differential 40-pF transducer at 3.33 MHz. where V_{DDH} = 15 V. The overall voltage swing is 30 V_{pp}. Note that a small over/undershoot.

$$T_r = \frac{2.16\zeta + 0.60}{\omega_n}. \quad (1)$$

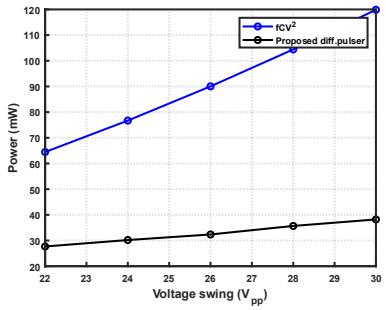
of ζ to optimize the rise/fall times of the circuit. T_r is the rise time and ω_n is the natural frequency of the resonant circuit.

III. Simulation Results

The circuit was developed in a 0.18 µm HV BCD technology. The layout is shown in Fig. 4. Fig. 5 shows the pulser operation when driving a single-ended transducer. Fig. 6 shows the differential pulser operation. In both Fig. 5 and Fig. 6 there are small over/undershoots which quickly decay so their impact on the pulser's acoustic performance is minimal. Fig. 7 shows the power performance of the proposed differential pulser against varying capacitive loads and voltage swings. It is evident that the proposed differential pulser



(a)



(b)

Fig. 7. (a) Power dissipation against capacitance at 3.33 MHz and 30 V_{pp}. (b) Power dissipation against voltage swing at 3.33 MHz and 40-pF capacitive load.

TABLE I. COMPARISON WITH STATE-OF-THE-ART DESIGNS

	This work (post-layout simulation)	[7]	[9]	[14]
Technology	**0.18 µm HV BCD**	0.18 µm CMOS	0.18 µm HV BCD	0.18 µm HV BCD
Cap. (pF)	**40**	1900	820	120
Freq. (MHz)	**3.33**	0.04	0.005	2.5
DMOS/SE transducer	**3**	N/A	4	≥ 4
TX Voltage (V_{pp})	**30**	28	30	30
Theoretical fCV^2 (mW)	**120**	59.6	3.69	270
Power (mW)	**38**	75[a]	0.993[a]	99.9
fCV^2 Reduction?	✓ **69%**	×	✓ 73%	✓ 63%
Differential?	✓	✓	×	×

[a]Estimated from paper.

dissipates a much smaller power than the theoretical fCV^2 level.

Table I summarises the performance of the proposed differential pulser and compares it against the state-of-the-art. The proposed differential pulser operating from 15 V is able to save 69% fCV^2 power dissipation as compared to a conventional 2-level 30 V single-ended pulser. The fCV^2 dynamic power reduction of the proposed differential pulser is comparable to the state-of-the-art, however, the proposed circuit is a more scalable solution.

IV. CONCLUSION

Present ultrasound pulser designs have been discussed and compared. A novel differential resonant pulser for wearable or portable ultrasound applications has been presented. It operates at 3.33 MHz and uses only three DMOS transistors per single-ended transducer or six DMOS transistors per differential transducer with 69% fCV^2 reduction of power dissipation. While matching the degree of power saving in present pulsers, the new resonant pulser is particularly advantageous in the use of chip area when multiple transducers are required. To the best of the authors' knowledge, the proposed differential resonant pulser for ultrasound applications is the first of its kind.

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