A 2.43 mW Multi-frequency Electrical Impedance Tomography ASIC with Dual-Mode Impedance Readout

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***Abstract*— This paper presents a multi-frequency time-variance-based Electrical Impedance Tomography (EIT) ASIC, designed to balance high-speed performance with low power consumption for biomedical applications. The ASIC leverages a dual-mode impedance readout architecture, incorporating time-to-digital demodulation at high frequencies and digital I-Q demodulation at low frequencies, which together address limitations in conventional EIT systems regarding data acquisition speed and power efficiency. The proposed system includes a current generator with an integrated auto-calibration scheme and a flexible clock generator with multiple PLLs, supporting a wide frequency range from 15.6 kHz to 1 MHz. Fabricated in a 65 nm CMOS process, the ASIC achieves a total power consumption of 2.43 mW and enables detailed multi-frequency impedance analysis while maintaining compactness and cost-effectiveness. In-vitro measurements with water tank validate its efficacy in different frequency-dependent impedance changes.**

***Keywords*— EIT, multi-frequency, time-to-digital**

I. INTRODUCTION

In recent years, Electrical Impedance Tomography (EIT) has emerged as a highly promising technique in lung imaging, human-machine interfaces, and cancer diagnosis, due to its capability of providing real-time, low-cost, and radiation-free monitoring [1-3]. Fig. 1 shows a common operating principle of EIT systems. It operates by injecting a known ac current through a pair of electrodes at a specific position on the target, while the resulting voltages are measured by other electrode pairs at different positions. By varying the electrode pairs for current injection and voltage measurement, a comprehensive set of impedance data is collected. This data is then used to reconstruct detailed images of the target area.

EIT image reconstruction can be performed using either time-variance or frequency-variance methods, each suited to different clinical and imaging requirements. In time-variance-based EIT systems, images are reconstructed from impedance changes measured over time at a single fixed frequency [1][3]. This single-frequency approach provides high temporal resolution, making it suitable for tracking rapid physiological processes. However, it suffers from limited tissue differentiation, reduced sensitivity to frequency-dependent physiological changes, and lower spatial resolution, which can restrict its effectiveness in applications requiring detailed tissue characterization [4][5].

In contrast, frequency-variation-based EIT systems continuously sweep across a range of frequencies, and the images come out from the impedance variation over different frequencies. This frequency sweeping approach allows for high sensitivity to frequency-dependent tissue properties, enhancing tissue characterization and making it valuable for

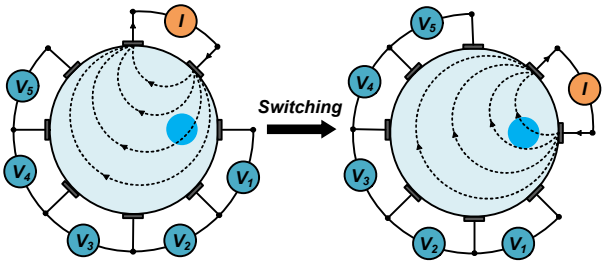


Fig. 1. Operating principle of a common EIT system.

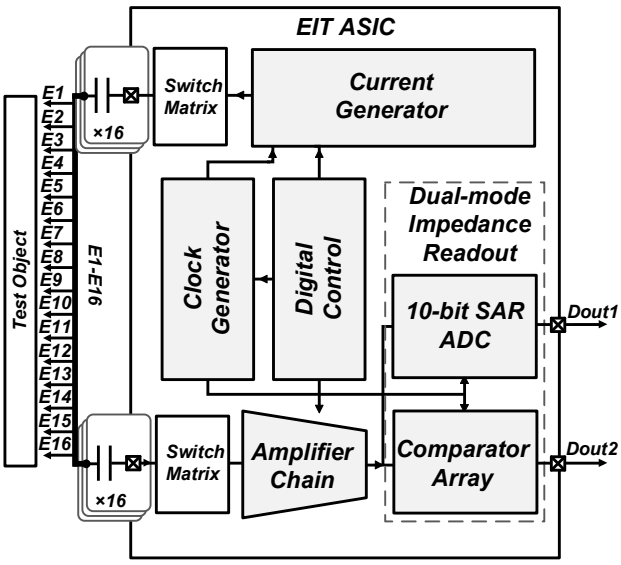


Fig. 2. Simplified block diagram of the proposed EIT ASIC.

applications where detailed tissue information is essential [2]. However, frequency-variation-based EIT struggles to capture dynamic changes due to the lack of time variance data and low data acquisition speed.

Multi-frequency time-variance-based EIT is a possible solution to solve the above issues [6-7]. By measuring the time variated impedance at multiple discrete frequencies, it combines the strengths of both time-variance and frequency-variance methods, allowing it to capture both the temporal changes and the frequency-dependent impedance characteristics of tissues. However, this approach also introduces challenges to temporal resolution and power consumption due to the intensive data acquisition demands.

In this paper, a multi-frequency time-variance-based EIT ASIC is proposed, featuring high speed and low power consumption. It features a dual-mode impedance readout architecture, combining a time-to-digital impedance readout

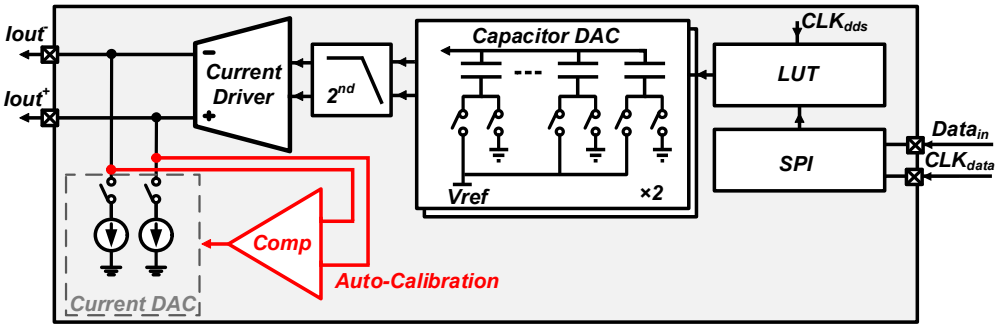


Fig. 3. Detailed block diagram of the current generator

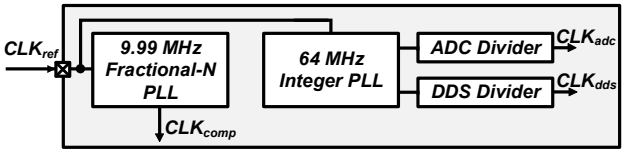


Fig. 4. Detailed block diagram of the clock generator

for high frequency impedance readout and a digital I-Q demodulation for low frequency readout, which effectively address the limitation of data acquisition speed and power consumption in conventional architectures. On the other hand, the highly integrated system further reduces power consumption. This EIT ASIC is designed and fabricated in a 65 nm CMOS process. The rest of the paper is organized as follows. Section II shows the detailed circuit implementation and working principles. Section III presents simulation results. Section IV concludes the paper.

II. Circuit Implementation

A. Top Level Block Diagram

The Simplified top level block diagram of this EIT ASIC is shown in Fig. 2. It has a current generator for injecting the required current, an amplifier chain for recording and amplifying the induced voltage. Both the current generator and the amplifier chain are multiplexed into 16 electrodes by the switch matrix. A clock generator is used to generate the required clock for both impedance readout and current generating. The recorded voltage can be digitized by the 10-bit SAR ADC for digital I-Q demodulation [1] or by the comparator array for a time-to-digital demodulation [3].

B. Current Generator

A detailed block diagram of the current generator is shown in Fig. 3. Direct Digital Synthesis (DDS) is used to generate the required current. It includes a 128-address, 8-bit Look-Up Table (LUT) that generates the required signal pattern, with patterns programmed externally via the Serial Peripheral Interface (SPI). Two 8-bit capacitor digital-to-analog converters (DACs) quantize the digital signal from the LUT into an analog voltage, followed by a second-order low-pass filter to eliminate high-order harmonics. A current driver then converts this voltage signal into current for injection into the test object. A current feedback structure is implemented in the current driver due to its superior linearity [8].

For clinical EIT systems, blocking capacitors are essential to prevent DC current from passing through electrodes and tissues. However, this setup can introduce significant DC offset voltages at the output nodes when using a current

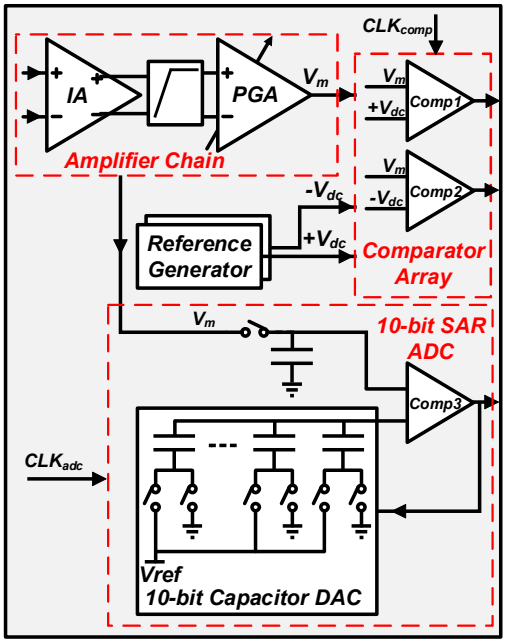


Fig. 5. Detailed block diagram of the amplifier chain and the dual-mode impedance readout.

feedback structure. To address this, an auto-calibration scheme is proposed. Before the current injection, the output DC voltage is sensed and compared via a comparator. Based on the comparison results, the calibration current DACs adjust the current to reduce the DC offset voltage. This method effectively decreases the dc offset voltage at the output nodes with minimum cost.

C. Clock Generator

The detailed block diagram of the clock generator is shown in Fig. 4. It consists of a 10-phase fractional-N phase-locked loop (PLL) with a 9.99 MHz output, used to generate the clock signal required by the comparator array, and an integer PLL with a 64 MHz output, which provides the frequency required by the ADC and DDS. Two frequency dividers are placed after the 64 MHz PLL to enable flexible clock selection for both the DDS and ADC.

The choice of a 10-phase, 9.99 MHz clock for the comparator and a 64 MHz clock for the DDS follows the least common multiple coherent sampling principle, which significantly improves temporal resolution for time-to-digital demodulation [3].

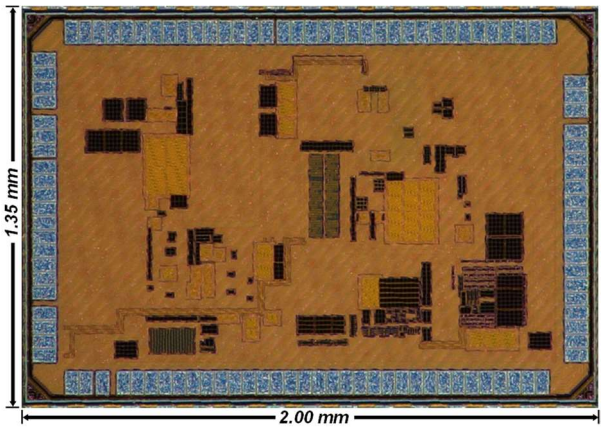


Fig. 6. Chip micrograph of the EIT ASIC.

TABLE I
PERFORMANCE SUMMARY

Technology	65 nm CMOS	
Die Size	2.00 mm × 1.35 mm	
Total Power Consumption	2.43 mW	
Frequency Range	15.6 kHz – 1 MHz	
Current Generator	Supply	1.8 V
	Operating Frequency	64 MHz
	Power consumption	2.01 mW
	Output Current	0.125 mA – 1 mA
	THD	< 0.3 %
Amplifier Chain	Supply	1.2 V/1.8 V
	Power Consumption	204 µW
	Input Referred Noise	6.7 μV_{rms} (dc-2 MHz)
	Gain	20 V/V – 300 V/V
Clock Generator	Power Consumption	102 µW
	Frequency	10-phase 9.99 MHz, 64 MHz
Dual-Mode Impedance Readout	Operating Frequency	10-phase 9.99 MHz for comparators
		16 MHz for ADC
	Power consumption	18µW for comparators
		27µW for ADC

D. Amplifier Chain and Dual Mode Impedance readout

The detailed block diagram of the dual-mode impedance readout is presented in Fig. 5. The amplifier chain contains an instrumentation amplifier (IA) and a programmable gain amplifier (PGA). It provides a gain from 20 V/V to 300 V/V in 5 steps. A high pass filter (HPF) is implemented between the IA and PGA to remove the offset.

To achieve both low power and high data acquisition speed, a dual-mode impedance readout is implemented. At high frequencies, the impedance is digitized by time-to-digital demodulation method. In this approach, two comparators controlled by the clock CLK_{comp} detects the cross points between the measured voltage, V_m, and the two complementary dc reference voltage, $\pm Vdc$. The impedance can then be digitized by counting the pulses from the comparators' output [3]. For low-frequency measurements, the current generator injects multi-frequency sinewaves into the test object, and the measured voltage, V_m, is directly digitized by a 10-bit SAR ADC. The digitized signal is then used for digital I-Q demodulation, which allows simultaneous readout of multi-frequency signals. This arrangement offers two key advantages. Firstly, by employing power-efficient time-to-digital demodulation at high frequencies, it avoids the need for power-intensive high-speed ADCs typically required in conventional digital I-Q demodulation, thus reducing overall power consumption. Secondly, by simultaneously reading out multi-frequency signals at low frequencies via digital I-Q demodulation, it effectively overcomes the speed limitations associated with the long signal periods at these frequencies.

Fig. 7. The image of the water tank with a copper tube, a nylon tube and a banana.

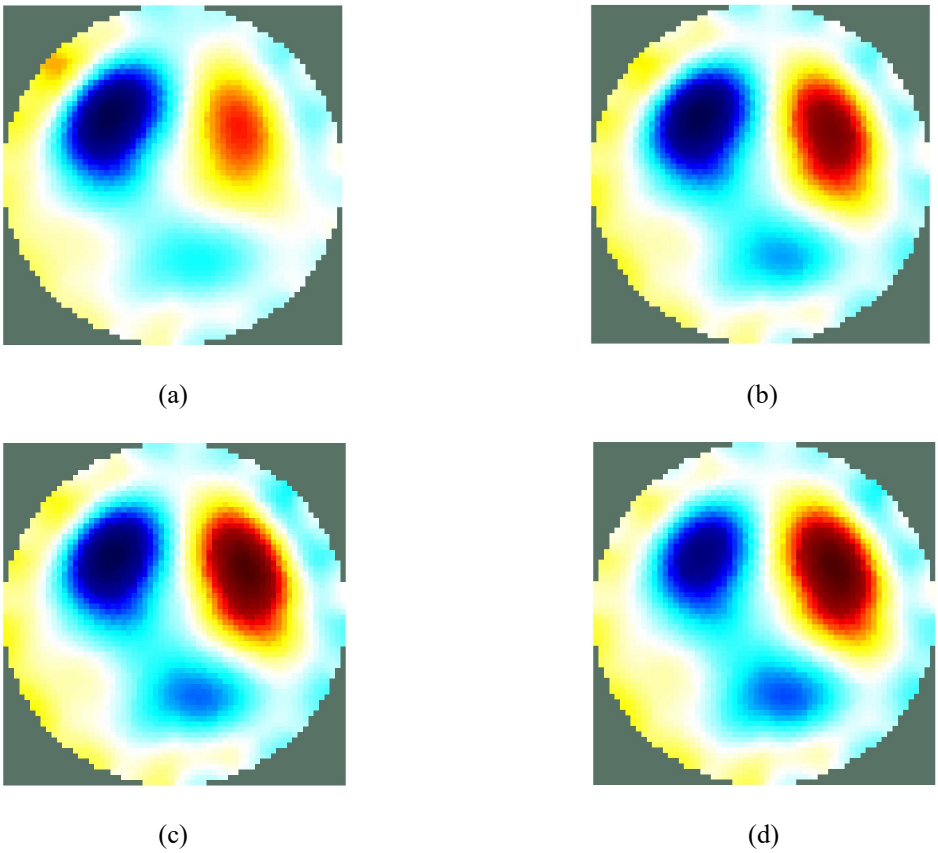
III. MEASUREMENT RESULTS

A. Overview

The EIT ASIC is designed and fabricated in a 65 nm CMOS process. The chip micrograph is shown in Fig. 6. It has a die size of 2.7 mm^2. The supply voltage for the current driver and IA is 1.8 V, while all other blocks are under 1.2 V supply. It has a total power consumption of 2.43 mW. It has a frequency range from 15.6 kHz to 1 MHz. By reading out the impedance through digital I-Q demodulation at frequencies of 15.6 kHz. 31.2 kHz and 62.5 kHz simultaneously measuring impedance at other frequencies above 62.5 kHz with time-to-digital demodulation, this ASIC can provide a maximum multi-frequency frame rate of 22 fps. A summary of the performance of the chip presented in TABLE I.

B. Images with In-Vitro Measurements

To verify the performance of the EIT ASIC, a water tank filled with 0.5 S/m saline solution containing a copper tube, a nylon tube and a banana was measured. The test setup is shown in Fig. 7. EIDORS was used for image reconstruction with Gauss-Newton algorithm [9]. Fig. 8 shows the image of the tested water tank at the frequency of 62.5 kHz. 125 kHz. 250 kHz and 500 kHz. As shown in the figure, this EIT ASIC effectively measured the frequency-dependent impedance change of the banana inside the water tank.



(a) (b) (c) (d)

Fig. 8. The reconstructed image of the water at the frequency of (a) 62.5 kHz, (b) 125 kHz, (c) 250 kHz and (d) 500 kHz.

TABLE 2
COMPARISON WITH PRIOR WORK

Parameters	[3]	[10]	[11]	**This Work**
CMOS Process (nm)	65 nm	350 nm	180 nm	65 nm
Supply (V)	1/1.8	±9	1.8	1.2 /1.8
Power Consumption (mW)	1.76	250	4.84	2.43
Bandwidth (kHz)	100-500	45-1000	1-18	15-1000
Maximum Output Current (μA_{pp})	700	6000	50	1000
Multi-frequency	No	No	No	**Yes**

IV. CONCLUSION

This paper presents the first fully integrated multi-frequency time-variance based EIT ASIC. It has a frequency range of 15 kHz to 1 MHz, with a total power consumption of 2.43 mW. The dual-mode impedance readout architecture effectively addresses the limitations on the data acquisition speed and power consumption in conventional multi-frequency EIT systems. A comparison with prior work is presented in TABLE II.

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