Voiding in Parylene-C Encapsulation of Surface Mount LEDs for an Optogenetic Epilepsy Neuroprosthesis

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***Abstract*—It is often assumed that Parylene-C encapsulation films are void-free & conformal by nature of their vapour deposition. We present a case study in an optrode device where voiding occurs; we argue the voids originate from the geometry of the substrate and from the use of surface mount components. The segment under study consists of a commercial LED bonded with Au/Au thermosonic bonding onto a custom silicon substrate. We demonstrate via micro-sectioning that there is polymer voiding behaviour (1) in sub-LED surfaces; and (2) within through-hole vias in the silicon substrate (channels designed to allow polymer vapour ingress during deposition). By making a comparison to the solutions found in the IC industry around tungsten vapour filling of blind vias, we present geometric solutions for failure mitigation.**

Keywords—optrodes, neuroprostheses, Parylene-C, voids, encapsulation, micropackaging

I. Introduction

The CANDO (Controlling Abnormal Neural Dynamics with Optogenetics) project aimed to treat focal epilepsy with an optogenetic brain implant and its associated gene therapy [1]. The brain implant consisted of an array of 16 optrodes which was to be implanted in the epileptic focus. Each optrode was made of silicon and was designed to penetrate cortical tissue. Discrete surface mount commercial LEDs were chosen as the light source due to their high efficiency (~40%), low cost, and low form factor (50µm thick). Prior investigations into custom "super thin" LEDs (3-5µm thick) with an outer seal ring cathode had inadequate efficiency (~3%) (Fig. 1). Monolithic LEDs built into the substrate such as those in [2] were outside the scope of our manufacturing capability.

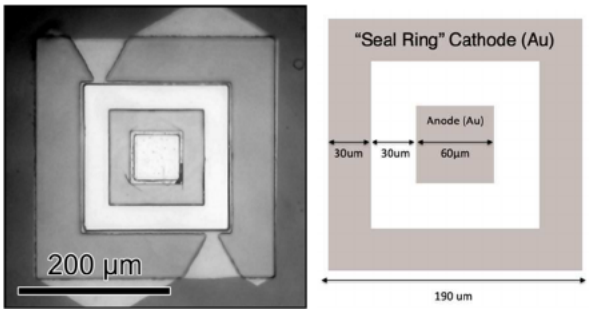

Fig. 1. Custom LEDs from our collaborator at the University of Strathclyde (not used in final implant due to low efficiency); note the "seal ring" cathode, intended to seal out moisture from diffusing in and shorting the anode and cathode.

The commercial LEDs chosen had only a spacing of 50µm between the two bond pads, and were any moisture present, device failure could occur. Thus, a method of encapsulating not only the surface mount LED, but also more importantly its anode and cathode would be required in the wet, corrosive environment of the human body. The device was protected by Parylene-C encapsulation, an established method of protecting electronics intended for use in implanted devices, such as neuroprostheses. The polymer is used due to its properties of chemical stability, non-toxicity & its ability to create low stress conformal films [3].

For polymer encapsulants applied in liquid phase, such as liquid silicone rubber, techniques such as vacuum centrifuging have been developed to ensure the encapsulant covers all surfaces and is void-free [4]. For encapsulants applied in vapour phase, such as Parylene-C, the conformal films are often assumed to be void-free; this paper examines this assumption and examines its consequences. A comparison is made to the voiding behaviour of tungsten films in blind silicon vias to form an understanding of the phenomenon [5].

II. Theory

A. Water Permeability in Polymers & Diffusion in Voids

While gravimetrically measured water uptake (as a function of immersion time & temperature) is often used as a measure of a polymer's moisture sensitivity, a more useful and thorough measure is its water permeability. A polymer's water permeability is a function of its: (1) diffusion coefficient; and its (2) solubility (or 'partition') coefficient. Both parameters are temperature & pressure dependent. From [7] the formula for water permeability (P) is:

$$P = \frac{q\tau}{At(VP_1 - VP_2)} = Q_f\tau \quad (1)$$

where q is the quantity of gas diffusing through a film of thickness τ, area A, in time t, and with a partial pressure difference between the diffusing gas on either side of the membrane as ($VP_1 - VP_2$).

If we take the human cortex, or any implant environment generally, we may globally assume 100% humidity, constant temperature (37°C), and constant pressure (1 atm).

Locally, we may find minimal variations in temperature originating from (1) natural body fluctuations; and (2) from

heat generated from a device. The latter is limited to 1°C increase in the cortex by regulation. Thus, we may assume the temperature-dependency to be constant and ignore.

On the other hand, a local pressure gradient across a polymer encapsulation, i.e. ($VP_1 - VP_2$) from Eq. 1, may be developed by the following phenomena: (1) osmotic pressure from ionic contaminants on the surface of the device, which would form a concentration gradient, drawing in water; (2) applied external pressure; and (3) a polymer void formed under vacuum creating a negative pressure gradient when the device is then exposed to atmosphere.

Regarding (1): the osmotic pressure of various surface contaminants has been explored in [6]; this is controlled for by rigorous surface cleansing. Regarding (2): this would be an unusual situation for a neuroprosthesis to experience. The third case (3) is of most significance to us – a void formed under vacuum will, due to the pressure difference across the encapsulation (the membrane), cause water vapour to diffuse through the membrane, which will then condense into liquid water, through which current leakage may occur.

Table 1 below taken from [7] lists the water permeability constants of various common polymers. Parylene-C is often referred to as a "moisture barrier" [8]; while it is an order of magnitude less permeable than silicone, it is still water permeable, as all polymers are, due to their network structure.

TABLE I. WATER PERMEABILITY CONSTANTS[1] [7]

Polymer	Permeability Constant
Silicones	$2.4 - 4.3 \times 10^{-8}$
Poly(chloro-p-xylylene) (Parylene-C)	2.0×10^{-9}
Cellulose acetate	$1.2 - 3.1 \times 10^{-6}$
Polystyrene	1.2×10^{-7}
Polyurethanes	$1.3 - 4.7 \times 10^{-8}$
Low-density polyethylene	$1.1 - 1.8 \times 10^{-8}$
High-density polyethylene	$1.6 - 1.8 \times 10^{-9}$
Epoxies	$1.0 - 1.3 \times 10^{-8}$
Poly(ethylene terephthalate) (Mylar)	1.0×10^{-8}
Polypropylene	$3.8 - 4.0 \times 10^{-9}$
Poly(tetrafluoroethylene) (Teflon)	3.5×10^{-9}
Poly(vinylidene chloride) (Saran)	3.1×10^{-9}

The unit of permeability here is defined as $P = \frac{cm^3_{STP} \cdot cm}{cm^2 \cdot s \cdot cmHg}$ where cm^3_{STP} is the 'standard cubic centimeter' (a unit of amount of gas rather than a unit of volume). The equivalent SI unit would be the GPU (gas permeance unit) where $1\ GPU = 3.35 \frac{10^{-10} mol}{m^2 \cdot s \cdot Pa}$.

In dimensional analysis, permeability is an L^2/T unit, and thus theoretically, it would take 10 times longer for a void in Parylene-C to fill with water than one in silicone, all other factors equal.

B. Chemical Vapour Deposition of Parylene-C

Parylene-C, or poly(chloro-para-xylylene) is formed from the reaction of chloro-para-xylylene monomers into a polymer with a backbone chain of chloro-para-benzenediyl rings (–C_6ClH_3–) connected by 1,2-ethanediyl bridges (–CH_2–CH_2–). The process of deposition is called the Gorham process, a chemical vapour deposition (CVD) process involving 3 steps: sublimation, pyrolysis & deposition. Firstly, the precursor Parylene-C dimer is sublimed; the dimer is then pyrolised into 2 monomers at high temperature; finally, the monomers polymerise onto contact surfaces of the device at room temperature into linear polymer chains [9].

C. The Sub-LED Through-Hole Via

The creation of a through-hole via underneath the LED between the anode & cathode pads was introduced (1) to prevent shorts between the anode/cathode; and (2) as a technique for enhancing the Parylene-C's encapsulation by allowing a pathway for flow of the monomer vapour.

Because the LED sits on top of this through-hole via, it effectively turns into a blind via; thus we may make a comparison to the work in [5] which is on voiding in tungsten-filled blind vias for IC manufacture.

D. Step Coverage

Step coverage is the parameter that describes the conformality of a set of deposition conditions, where at 100% step coverage every surface exposed to the gas phase experiences identical deposition rates and is thus ideally conformal and voidless [5]. Voidless deposition requires sufficient mass transport of reactants into contact surfaces, and removal of reactants away from surfaces. For a blind via, step coverage can be defined in two ways:

$$step\ coverage = 1 - A(L_0/R_0) \quad (2)$$

where A is a function of the deposition conditions (which for Parylene-C deposition are a function of temperature and pressure of Parylene-C monomer vapour); R_0 & L_0 are the initial radius and depth of the via respectively. Alternatively, step coverage can be experimentally determined by cross sections, via the formula:

$$step\ coverage = (x/y)*100\% \quad (3)$$

where x is the wall thickness of the void, and y is the maximum thickness of the deposited film inside the void (see Fig. 2 below).

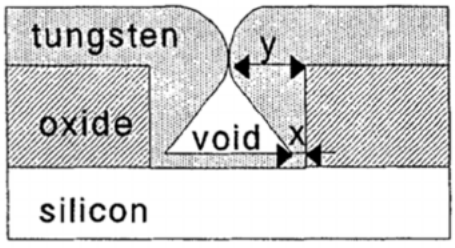

Fig. 2. Definition of step coverage of a film in a blind via using the example of metallic tungsten films in silicon [5].

[1] *Measured at 23°C on 3-8×10^{-3} cm thick films.*

Parylene-C deposition produces no by-products, and thus in terms of mass transport considerations, the accumulation of depleted reaction products is not a consideration. In comparison, the vapour deposition of tungsten relies on the reduction of tungsten hexafluoride (WF_6) with hydrogen gas (H_2) yielding metallic tungsten with a by-product of hydrogen fluoride vapour (HF) which must be continuously exhausted in order for film deposition to proceed forward [10].

III. Method

A. Device Fabrication

Optrode devices were fabricated in-house in the Newcastle University cleanrooms on a silicon substrate (see Fig 3). The LEDs used were Cree® TR2227™ (CreeLED, USA). There were 2 LEDs & 2 recording electrodes on each optrode tine. Appropriate design of photoresist layer (SPR 220) allowed the growth of a 5-8um pillar of gold over the anode and cathode pads using electroplating. A thermosonic fine-placer tool was then used (150°C, 1.5N) to bond each LED to its pads (300mW, 1s). The sub-LED via was created using DRIE during the same step as device singulation. The gap between the anode and the cathode pads was 50µm. The via was ⌀50µm in diameter.

B. Parylene-C Encapsulation

Device encapsulation was carried out in a Labcoater Parylene deposition system (PDS Labcoater 2010, Speciality Coating Systems Inc, USA). 17.5g of Parylene-C precursor powder was used per deposition run; this was repeated twice for a goal film thickness of 20µm. Adhesion promoter (A-174 silane) was added to the chamber before each deposition. The dimer powder was sublimated (175°C, 1.0 torr) and passed through a furnace stage for monomerisation (690°C, 0.5 torr) before low-vacuum deposition (20 min, 25°C, 0.1 torr).

C. Micro-Sectioning

Device micro-sectioning was performed via a commercial service called Perfect Edge™ (MCS Ltd, UK). It is a non-mechanical technique that uses an inert gas plasma. Images were produced with SEM. Devices were micro-sectioned along the longitudinal axis of the optrode (see Fig 3).

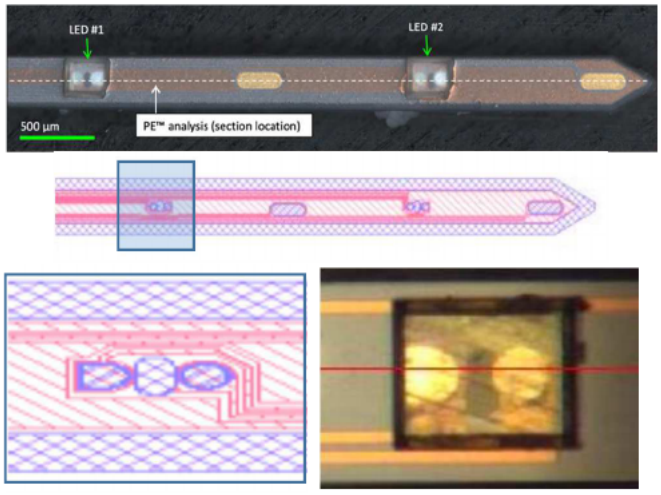

Fig. 3. TOP: photograph of one Parylene-C coated optrode tine with 2 LEDs & 2 oval recording electrodes visible; MIDDLE: KLayout view of same optrode tine with box around detail view; BOTTOM-LEFT: KLayout detail view of the anode & cathode bonding pads, and the sub-LED through-via; BOTTOM-RIGHT: microscope image of LED #1 on the device shaft, with the red line the direction of the micro-section cut.

IV. Results

We present results for the micro-sections of two LEDs: LED #1 and LED #2 (see Fig. 5-10).

For LED #1, the Parylene-C encapsulation was observed to be conformal and coated all surfaces, though unequally. Two kinds of voids were observed: (1) a larger void in the via underneath the LED, approximately 12.5µm wide and 30µm deep (see Fig. 5); and (2) a thin void underneath the LED approximately 0.8µm thick and 10µm long (see Fig. 6). Additionally, around voids were visible around the gold bond pads (see Fig. 7).

For LED #2, the Parylene-C encapsulation was observed to be conformal on the top surfaces, and the through-hole via was void-free (see Fig. 8). However, on the underside of the LED, and around the gold bond pillars large voids were observed: voids 1.8µm thick and 60µm long (see Fig. 9, 10).

V. Discussion

A. Void Formation

The failure of the Parylene-C vapour to continue polymerising in volumes narrower than ~1-2µm suggests that the reaction is preferentially occurring elsewhere. As there are no reaction products that need to be evacuated, it is likely that the monomer is simply depleted in those spaces where we can observe voids. We can deduce that the vapour pressure in the chamber is inadequate to supply new reactants. Thus, for our deposition parameters a geometric limit (~1-2µm) exists.

Furthermore, the void in the sub-LED through-hole via is similar to that reported in silicon vias filled using tungsten chemical vapour deposition as described in [5]. Figure 4 is intentionally reproduced from [5] upside-down; this is to draw a comparison to Figure 5, whereby in the former, a blind via in silicon is incompletely filled with metallic tungsten, and in the latter, a through-hole via becomes a blind via as a result of being blocked by an LED, and this pseudo-blind via is similarly incompletely filled with Parylene-C.

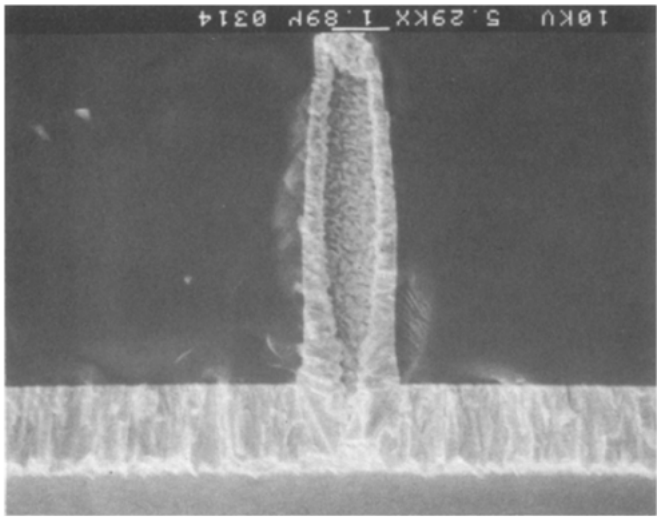

Fig. 4. A large void in metallic tungsten film for via filling of a blind via in silicon. (Intentionally presented upside-down by the author.) [5]

In LED #1, the aspect ratio of the via was 50/200µm = 0.25 (i.e., R_0 = 25µm & L_0 = 200µm). The void in the via had a maximum width of 12.5µm; thus, the step coverage = (50-12.5)/50 = 75% (using Eq. 3). Substituting this into Eq. 2 resulted in A = 0.03125.

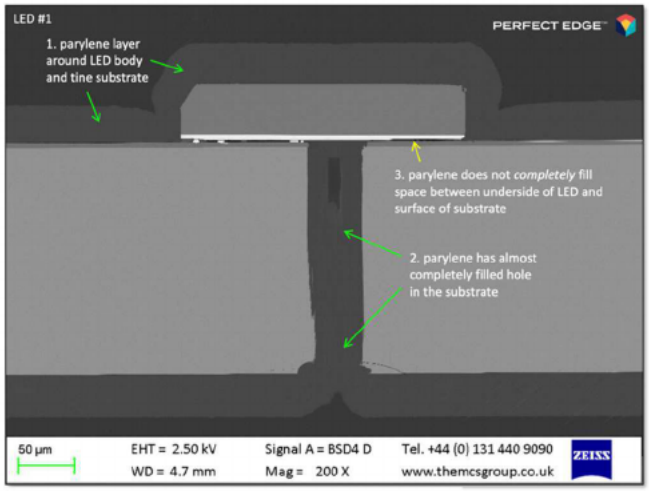

Fig. 5. LED #1 (overall view) – A void in the sub-LED through-hole via approximately 12.5µm wide and 30µm deep.

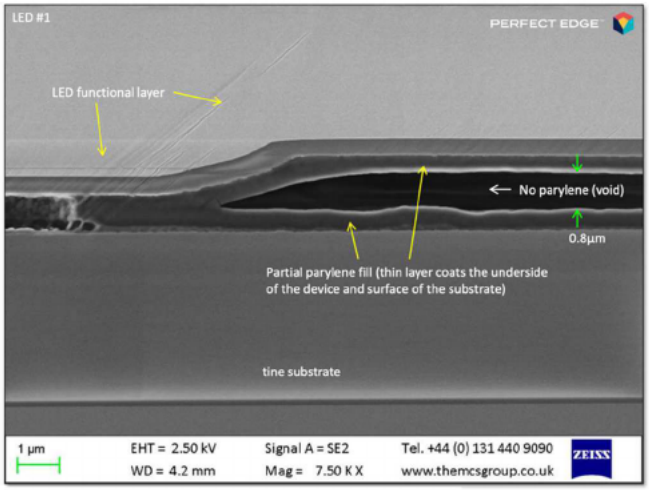

Fig. 6. LED #1 (underside view) – a thin void on the underside of the LED ("sub-LED") 0.8µm thick and approximate 10µm long.

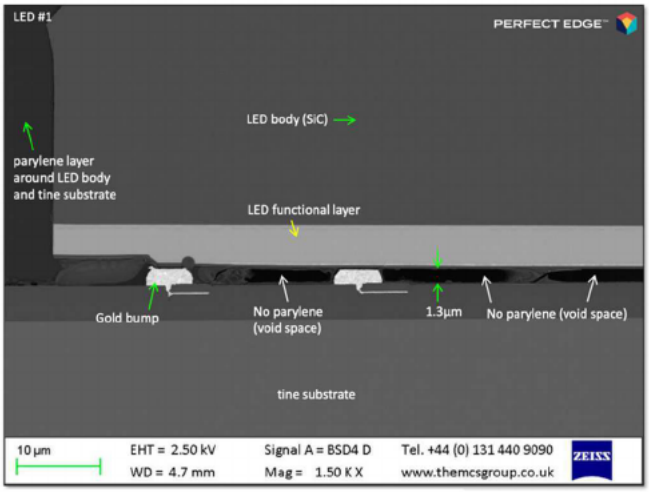

Fig. 7. LED #1 (gold pad view) – Around the critical areas of the gold pads, voids are present and the metal is not fully encapsulated.

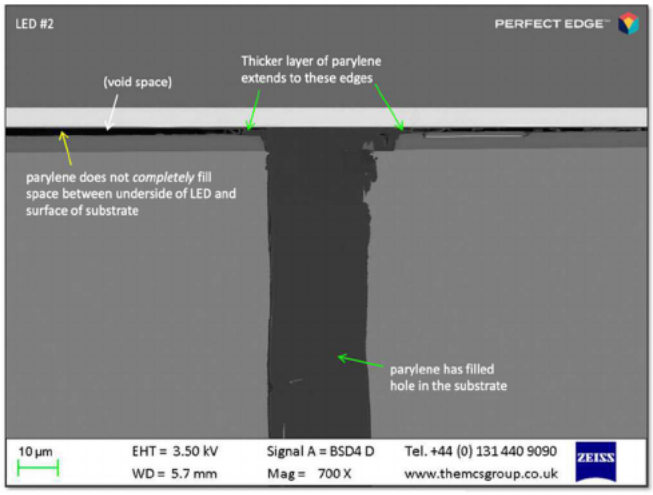

Fig. 8. LED #2 (overall view) – The sub-LED through-hole via is void-free; compare to Fig. 5 where there is a void.

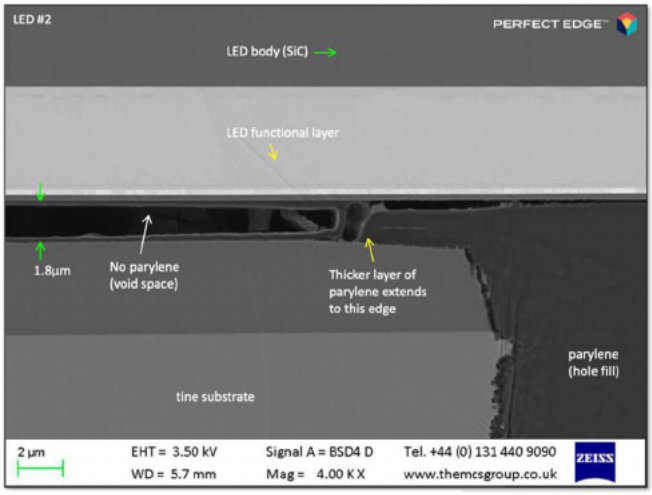

Fig. 9. LED #2 (underside view) – a thin void on the underside of the LED ("sub-LED") 1.8µm thick and approximate 60µm long.

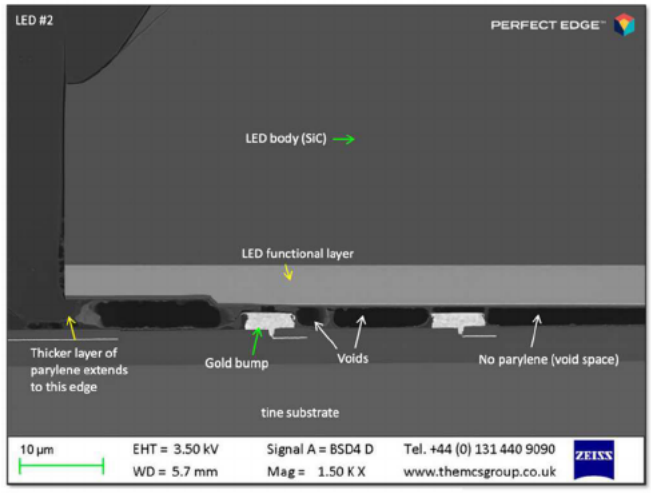

Fig. 10. LED #2 (gold pad view) – Around the critical areas of the gold pads, voids are present and the metal is not fully encapsulated.

By utilising the concept of step coverage introduced in [5] we can offer some geometric solutions to this problem.

B. *Geometric Solutions*

For applications that require surface mount components with adjacent bond pads, where designers would like to use sub-component through-hole vias between pads to aid in encapsulation, where deposition parameters are fixed, we present some solutions to the voiding problem in and Figure 11 & Table 2 below:

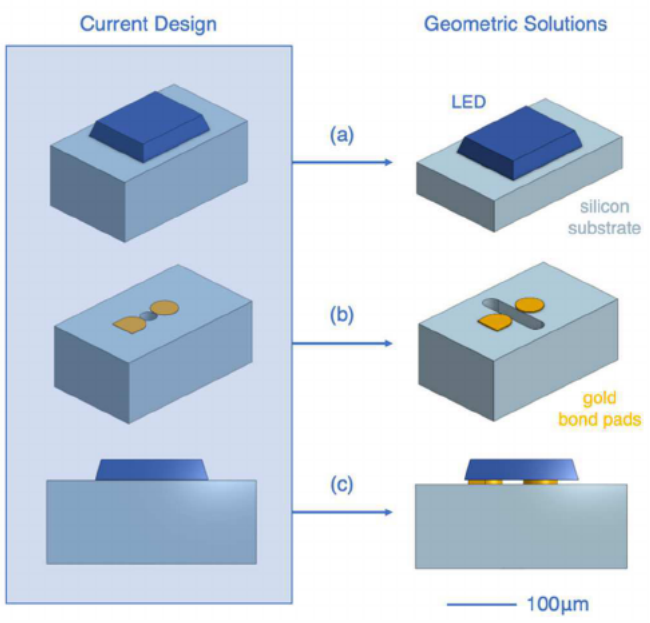

Fig. 11. Hypothetical 300µm long segments of the optrode; 3 geometric solutions to voids in Parylene-C film: (a) substrate thinning; (b) via-widening; and (c) gold bond pad heightening.

TABLE II. GEOMETRIC SOLUTIONS TO VOIDS

Solution	Advantages	Disadvantages
substrate thinning	reduces overall device profile; increases step coverage by decreasing L_0	additional wafer level process; weakens the device for insertion
via-widening	increases step coverage by increasing effective R_0; no longer blind-via, acts as through-hole for gas flow	large stress concentrations at thin edges of shank; much weaker for buckling during insertion
gold bond pad heightening	no longer blind via, larger path for vapour to flow; void-free sub-LED encapsulation	increases overall device profile; difficult to electroplate multiple microns of gold

With substrate thinning we can increase the aspect ratio of vias (e.g., thinning the substrate by half to 100µm would increase aspect ratio from 0.25 to 0.5); for the calculated value of A (0.03125) the step coverage would increase from 75% to 93.75% and thus the maximum void width would theoretically decrease from 12.5 to 1.6µm. The disadvantage of substrate thinning is the technical difficulty of the process, and the weakening of the device mechanically.

Via-widening beyond the edges of the surface mount component is intended to allow the via to behave as a true through-hole via, rather than as a pseudo-blind via. Theoretically, the Parylene-C vapour would have more of a pathway to flow. The weakness of this is that it would induce large stress concentrates in the shank.

Lastly, gold pad heightening is intended to overcome the ~1-2µm geometric limit of the deposition process, by lifting the component higher off the substrate (10µm in Fig. 11). The main disadvantage is the increase in the device profile, which is not desirable for an implantable device.

A technical solution may require one or multiple of these modifications to an existing design.

VI. CONCLUSION

We cannot assume that Parylene-C vapour will form conformal, void-free encapsulations over all surfaces in surface mount components. Specific geometries and deposition parameters may lead to voids in vias and in the undersides of surface mount components. For devices used in harsh environments, such as implanted devices, these voids may lead to device failure in the event of moisture ingress. For polymer encapsulation to be successful in these applications, we must predict such voiding and mitigate with geometric solutions, such as those suggested in this paper.

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REFERENCES

[1] Zaaimi, B., Turnbull, M., Hazra, A., Wang, Y., Gandara, C., McLeod, F., ... & Jackson, A. (2022). Closed-loop optogenetic control of the dynamics of neural activity in non-human primates. Nature Biomedical Engineering, 1-17.

[2] Wu, F., Stark, E., Ku, P. C., Wise, K. D., Buzsáki, G., & Yoon, E. (2015). Monolithically integrated µLEDs on silicon neural probes for high-resolution optogenetic studies in behaving animals. Neuron, 88(6), 1136-1148.

[3] Von Metzen, R. P., & Stieglitz, T. (2013). The effects of annealing on mechanical, chemical, and physical properties and structural stability of Parylene C. Biomedical microdevices, 15, 727-735.

[4] Donaldson, P. E. K., & Sayer, E. (1975). A vacuum centrifuge for void-free potting of implantable hybrid microcircuits in silicone. Medical and biological engineering, 13, 595-596.

[5] Schmitz, J. E. J., & Hasper, A. (1993). On the mechanism of the step coverage of blanket tungsten chemical vapor deposition. Journal of the Electrochemical Society, 140(7), 2112.

[6] Donaldson, N., Baviskar, P., Cunningham, J., & Wilson, D. (2012). The permeability of silicone rubber to metal compounds: relevance to implanted devices. Journal of Biomedical Materials Research Part A, 100(3), 588-598.

[7] Spivack, M. A., & Ferrante, G. (1969). Determination of the water vapor permeability and continuity of ultrathin Parylene membranes. Journal of The Electrochemical Society, 116(11), 1592.

[8] Li, W., Rodger, D., Menon, P., & Tai, Y. C. (2008). Corrosion behavior of parylene-metal-parylene thin films in saline. ECS Transactions, 11(18), 1.

[9] Marszalek, T., Gazicki-Lipman, M., & Ulanski, J. (2017). Parylene C as a versatile dielectric material for organic field-effect transistors. Beilstein Journal of Nanotechnology, 8(1), 1532-1545.

[10] Korolev, Y. M. (2015). Deposition of tungsten by reduction of its hexafluoride with hydrogen under the stoichiometric component ratio: an environmentally pure production process. Russian Journal of Non-Ferrous Metals, 56, 149-154.