Applied Physics
Express

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To cite this article before publication: Henry Montagu *et al* 2025 *Appl. Phys. Express* in press https://doi.org/10.35848/1882-0786/adac27

Spin polarised quantum conductance in 1D channels

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We report the experimental observation of a spin-polarised conductance plateau at e^2/h in a clean one-dimensional (1D) quantum wire defined by back-gated, split gate devices on a GaAs/AlGaAs heterostructure in the absence of a magnetic field. The 1D devices were fabricated using standard lithography techniques consisting of split gates, and a custom-designed back gate allows for the modulation of carrier density within the 1D channel. The differential conductance shows regular quantised plateaus in units of $2e^2/h$ as a function of back gate voltage, including the observation of the $0.7(2e^2/h)$ conductance anomaly. The 0.7 anomaly, on reducing the charge carrier concentration, gradually converts into a $0.5(2e^2/h)$ structure, indicating the lifting of spin degeneracy in the absence of a magnetic field. Our results suggest the potential of low-density 1D devices for applications in spintronics and quantum electronics.

In solid-state systems, electrons play a crucial role as the fundamental units, and their transport properties have been extensively studied, particularly as dimensionality changes. When electrons are confined to lower dimensions, they transition into a two-dimensional electron gas (2DEG), resulting from variations in the density of states. The electrical transport characteristics of the 2DEG have been well-documented, especially through investigations of the Quantum Hall Effect (QHE).[1,2] This remarkable phenomenon emerges when a perpendicular magnetic field is applied to the 2DEG, leading to the formation of Landau Levels and the subsequent manifestation of QHE. The 2DEG provides an excellent platform for developing one-dimensional (1D) channels.[3] In these channels, electrons can move freely in one direction while confined in the other two dimensions. A notable example of a 1D system is the quantum wire formed using the 2DEG within a GaAs/AlGaAs heterostructure. As we manipulate the width of the 1D constriction using split gate voltages, the differential conductance of these channels reveals a rich spectrum of 1D modes. In a 1D quantum wire, conductance takes on quantised values, with each 1D subband contributing a spin-degenerate conductance of $2e^2/h$. The total conductance is expressed as $N2e^2/h$, where N = 1, 2, 3, 4...are 1D subbands.[4-8] In this setting, non-interacting electrons can only change momentum in one dimension, leading to a progressive filling of the subbands. The ground state of this system behaves like a true Fermi liquid, displaying a conductance plateau at $2e^2/h$.[9] Additionally, a plateau at $0.7(2e^2/h)$ often appears alongside the usual integer plateaus.[10] This 0.7 conductance anomaly provides an intriguing area of exploration, as it is often linked to intrinsic spin polarisation within disorder-free 1D channels.[4,7,10] There are also proposals suggesting the involvement of a Kondo impurity in explaining the 0.7 anomaly.[11]

Reducing the carrier concentration can significantly influence the correlation effects within 1D channels.[12-18] This is effectively achieved by implementing either a top gate over the split gates or a mid-line gate.[4,14-18] By leveraging the interaction effects, we can configure a line of 1D electrons into new phases, determined by the low density of these electrons and the weaker confinement potential. As the density of electrons in the 1D quantum wire decreases, the kinetic energy of the electrons becomes comparable to the Coulomb energy, resulting in various spin phases, including the Wigner lattice.[14-16,18-24] A single row of 1D electrons in this lattice distinctly splits into a zigzag pattern or organises into two rows.

The zigzag phase and the two-row configuration represent a complex interplay where spin and charge phases coexist.[19,20] Recent investigations into zigzag and 1D Wigner lattice systems have demonstrated the emergence of fractional quantisation of conductance in 1D channels formed in n-GaAs and p-germanium-based systems without any magnetic field. In low-density 1D channels in n-GaAs, fractional quantised conductance at values 2/5, 1/2, 1/5 and other exotic quantum states (measured in units of e^2/h) have been observed in addition to a plateau at $1(e^2/h)$.[24-27] A plateau at e^2/h signifies the system is spin-polarised in the absence of a magnetic field. Thus, a system like this demonstrates potential for spintronics and quantum electronics applications.

The observation of the e^2/h plateau is significant as it suggests the possibility of exchange correlations affecting spin in the 1D system. There is the suggestion that in a 1D system, the spin aligns in a preferred direction, creating a ferromagnetic order, resulting in a quantised plateau at e^2/h.[22,23] This may be derived from the intrinsic spin polarisation and exchange-correlation with the 1D channel.[28-30] Also, a spin mode emerges alongside the charge mode when considering electron-electron interactions.[31,32] The general Luttinger liquid (LL) model cannot effectively explain this phenomenon, as the electrons' spin is incoherent in the low-density regime. Spin-incoherent transport is theorised to show a quantum conductance of e^2/h[22,23], which was experimentally shown in top-gated and split-gated devices in GaAs/AlGaAs heterostructures.[33] A plateau was reported at approximately e^2/h in midline-gated, split-gate devices utilising high-quality coupled bilayer electron systems.[34,35] There are reports of observing the e^2/h plateau, which is suggested to form due to lateral spin-orbit interactions in materials that have relatively lower quality compared to GaAs.[36] In this article, we deal with investigations of the e^2/h plateau in clean 1D channels formed in GaAs-based heterostructures with different confinement gates, aiming to address the knowledge gap in the literature through device fabrication and measurements.

While midline-gated split-gate devices are capable of tailoring the confinement potential, they could also potentially divide a 1D channel into two, which brings challenges in probing interaction effects. The advantages of top-gated devices lie in their ability to fine-tune parabolic confinement in 1D quantum wires.[14-18] However, the use of large negative voltages inherently limits them, which could screen the underlying 2DEG and obscure interaction effects. Maintaining greater separation between the top gate and the 2DEG can mitigate

screening, but existing technical challenges restrict this distance to a few hundred nanometres due to difficulties in appropriately cross-linking the polymer (PPMA) insulating layer separating the top gate from the split gate.[15,16] Moreover, the production of top-gated, split-gate devices involves two essential e-beam lithography stages—one for the split gate and another for the top gate.

To effectively tackle these challenges, we propose a solution that preserves interaction effects in 1D channels and allows for fine control over confinement strength. This is achieved by introducing a back gate on a thinned semi-insulating GaAs wafer, ensuring that it is sufficiently distanced from the 2DEG. Importantly, the fabrication of this back gate does not necessitate an additional e-beam lithography stage, rendering the process more economical. The back-gated, split-gate device is strategically advantageous, as the gate will be positioned tens of micrometres away from the 2DEG, resulting in minimal screening effects. This configuration enables uniform tuning of confinement, facilitating thorough investigations into electron-electron interactions and advancing our understanding of electron transport in 1D channels.

In the present Letter, we report the observation of a spin polarised conductance plateau of e^2/h in transport measurements of 1D quantum wires. The quantum wire is defined using split gates on the top of a GaAs/AlGaAs heterostructure, and a specially designed Schottky back-gate has been used to tune the density of 1D electrons.

The devices used in the present work were fabricated from a delta-doped GaAs/AlGaAs heterostructure grown using molecular beam epitaxy (MBE), where the 2DEG formed ~ 300 nm beneath the surface had mobility in the dark (light) of 1.2×10^6 cm^2/Vs (3.0×10^6 cm^2/Vs) and an electron density of 9.0×10^{10} cm^{-2} (1.2×10^{11} cm^{-2}). A pair of split gates of length (width) of 0.4 μm (0.5 μm), were patterned by a standard e-beam lithographic technique.[15,16] The back gate fabrication process involves several key steps detailed in Ref. 16, with an overview presented in Figure 1. The GaAs chip's initial thickness was approximately 500 μm. After completing the topside fabrication of the Ohmic and Schottky split gates, a 10 μm layer of photoresist, (SPR-220), was spun-coated on the chip to protect the devices during wet etching. The chip was then mounted upside down on a glass slide and baked at 115°C for 3 minutes to harden the photoresist, as shown in Fig. 1(a). This photoresist is resistant to the

acid peroxide etching solution and can be removed by soaking the chip in acetone, illustrated in Fig. 1(b). To thin the GaAs chip, a sulfuric acid/peroxide solution in a 1:1:9 ratio of H_2SO_4:H_2O:H_2O_2 was used. With an optimised etching rate of 15μm/min, this process effectively reduced the chip's thickness to between 50 and 100 μm, with an average thickness of approximately 50 μm, as measured by a Dektak thickness profilometer [Fig. 1c)]. Following thinning, the chip was subjected to e-beam evaporation to deposit a Ti/Au layer (30 nm/120 nm) for the back gate metallisation. After metallisation, the chip was immersed in acetone to dissolve the photoresist, as shown in Fig. 1(d). Finally, the chip was mounted with the Ti/Au side down onto a non-magnetic leadless chip carrier (LCC) using silver epoxy for electrical contact and mechanical support, Fig. 1(e). Gold wire bonds were then made to connect the contact pads on the topside and back gate via the silver conducting epoxy using a conventional ultrasonic bonder.

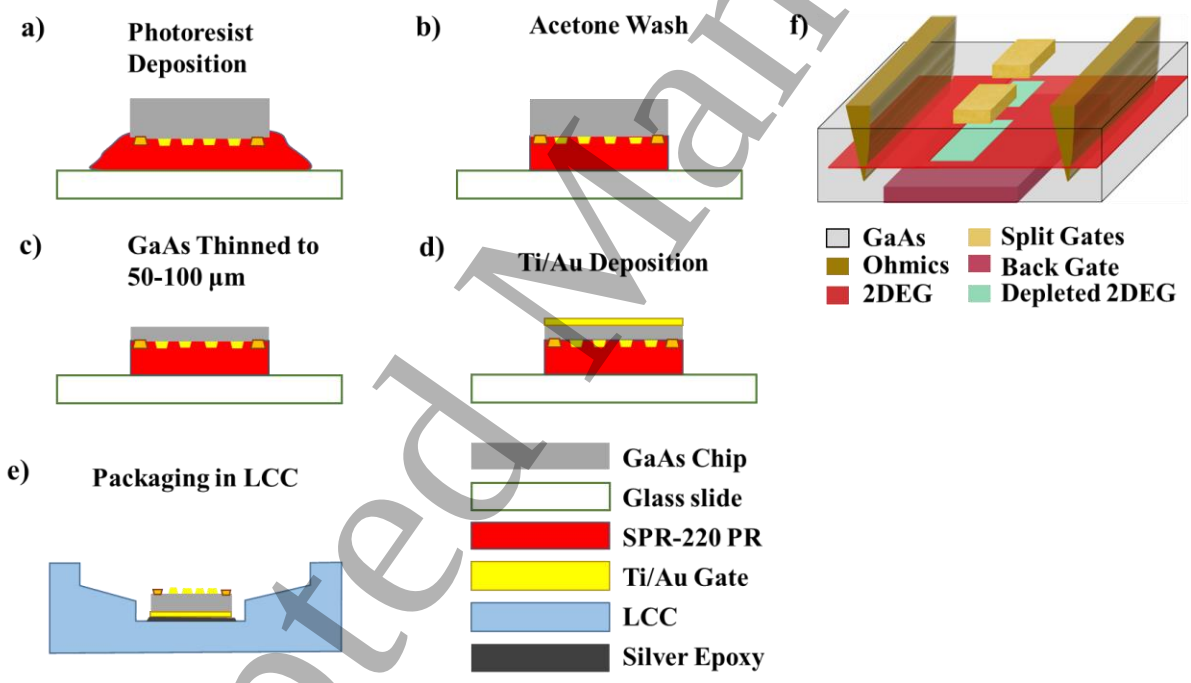

Fig. 1. The schematic diagram outlines the procedure for incorporating a back gate into a GaAs sample. a) A positive photoresist is applied to the top surface of the GaAs chip, which features a fabricated 1D device. The chip is then positioned with the photoresist-coated side facing downward onto a thin glass slide. b) Acetone is used to remove any excess photoresist from the backside and corners. c) The chip is thinned to a thickness of 50-100 µm through a wet-etching process. d) A metal layer of Ti/Au is deposited to form the back gate. e) The processed chip, now equipped with a back gate, is packaged in an LCC using conductive silver epoxy.

f) A schematic representation of the 1D device is included, showing a pair of split gates, ohmic contacts for the source and drain, and a back gate used to adjust the carrier density in the 1D quantum wire.

The results presented in this Letter are based on two cooldowns. During the first cooldown, the sample was illuminated with a red LED at a current of 200 µA for one second resulting in 2D carrier density ~ 1.2×10^{11} cm^{-2}. In the second cooldown, the sample was illuminated with the same red LED, but at a reduced current of 100 µA for one second (2D carrier density ~ 1×10^{11} cm^{-2}).

Figure 2 shows scanning electron microscopy images: (a) a comparison between un-etched (~500 μm thick chip) and an etched chip (~50 μm thick) with a back gate; (b) the two packaged chips: (top) wire-bonded thinned chip with a back gate; (bottom) wire-bonded device without a back-gate. The two-terminal differential conductance (G) measurements were performed using an excitation voltage of 10 µV at 73 Hz in a cryofree dilution refrigerator with an electron temperature of 70 mK.

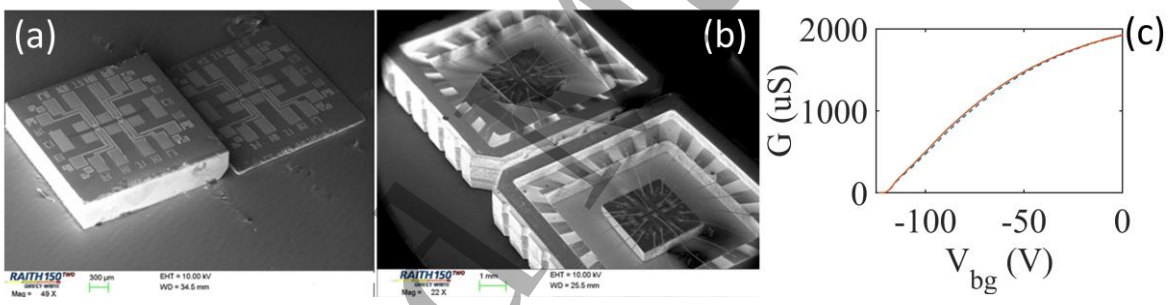

Fig. 2. The scanning electron microscopy images of the fabricated and etched GaAs chips and the final devices packaged in LCCs. a) shows a chip before etching (left) with a thickness of ~ 500 µm and after etching to a thickness of ~ 50 µm (right), b) final devices packaged in LCCs for comparison, the top image is for packaged etched-chip with a back gate using conducting silver epoxy, and the bottom image is for un-etched chip without a back gate. In the latter case, non-conductive Ge-varnish was used to glue the chip to the base of LCC. (c) The differential conductance measurement of the 2DEG by sweeping the back gate voltage without any voltage being applied to the split gate. The conductance decreases as the back gate is made negative until the channel is fully pinched off at -120 V.

Figure 1(f) shows the schematic diagram of the back-gated, split gate device fabricated on a GaAs/AlGaAs heterostructure. Figure 2(c) shows the reverse and forward sweeps of the differential conductance of the 2DEG as a function of the voltage applied to the back gate without any bias applied to the split gate. As the back gate is made more negative, the conductance drops, and the channel gets fully pinched off at $V_{bg} \sim$ -120 V. It may be noted that there is hardly any hysteresis between the forward and backward voltage sweeps, indicating a good quality fabricated back gate. The 2DEG density of electrons, n_{2D}, was estimated to be ~ 9.0×10^{10}cm^{-2} using low-magnetic field magnetoresistance measurements without illuminating the sample. We also estimated the approximate n_{2D} using the back gate voltage required to deplete the 2D electrons in the two terminal conductance measurement [Fig. 2(c)]. The back gated device containing the 2DEG may be considered as a parallel plate capacitor, with D~50 μm, the distance between the back gate and the 2DEG. Therefore, using V_P= -120 V in the relation $V_P = 4\pi e n_{2D} D/\varepsilon\varepsilon_0$, where e is the charge of electron, n_{2D} is the 2DEG density, ε is the dielectric constant of GaAs (12.5), and ε_0 is the permittivity of free space, we estimated n_{2D} ~1.3×10^{10} cm^{-2}, which is relatively low density, indicating limitations of density estimation using a simple capacitor model.[37,38)]

Figure 3 shows the conductance plot as the split-gate voltage is swept for various back-gate voltages in the first cooldown. The back gate voltage for the left-most trace is 0 V which is incremented by -4.0 V so that the right-most trace is taken for $V_{bg} \sim$ -120 V. The regular quantised plateaus in units of $2e^2/h$ are resolved showing upto seven 1D modes [see Fig. 3 (a) and (b)]. As the conductance traces progress from left to right, the confinement potential transitions from a strongly-confined regime to a weakly-confined regime. Moving from stronger to weaker confinement, the plateaus become shorter, indicating a reduction in the 1D subband spacing. As the back gate voltage is made more negative, the pinch-off voltage of the split gate, V_{sg}, moves to lower negative voltages, which indicates a lower carrier density. It is important to note that the back gate voltage controls the density of electrons between the split gate and the entire 2DEG. Therefore, the series resistance was removed individually for each trace where the series resistance was 370(3700) Ω for Vbg at 0(-120) V. Figure 3(b) is the colourplot of the data shown in Fig. 3(a), showing the emergence of quantised conductance clearly, the 0.7 conductance anomaly is also present for the entire confinement regime. However, it gets strengthened in the low-density regime with a weaker confinement

potential, which agrees with previous findings, indicating that its origin is linked to correlation effects.[4,6,10,11)]

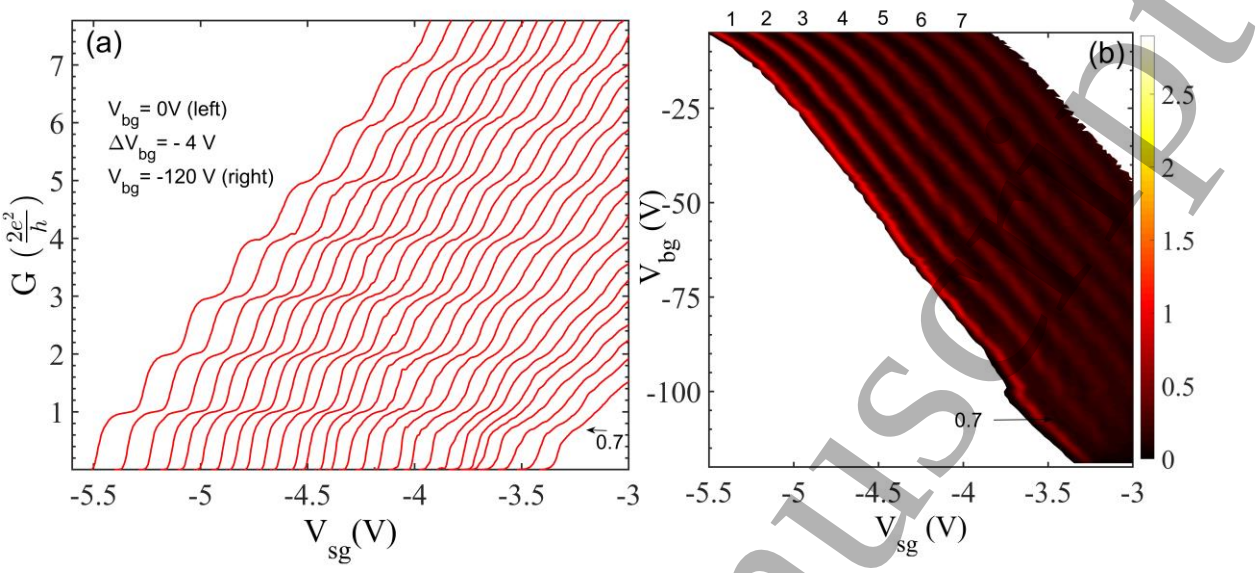

Fig. 3. The differential conductance measurements of a split gate device with a back gate in the first cooldown. For each trace, the conductance is measured as a function of split gate voltage (V_{sg}) at a fixed value of back gate voltage, V_{bg}. V_{bg} is incremented in steps of -4 V from 0 V on the left to ~ -120 V on the right. The conductance traces from left to right means that the confinement of 1D wire is changing from strong to weak depending on the applied back gate voltage. a) The ground state plateau represented by $2e^2/h$ becomes shorter and less defined as the confinement (and the density of 1D electrons) is reduced, and in the weaker confinement, the 0.7 structure strengthens. (b) The colourplot of the transconductance of data in Fig. 3(a), dG/dV_{sg} , as a function of V_{sg} and V_{bg}. Regions of high transconductance are shown in red and low transconductance (plateaus) in black, showing the indexing of seven 1D subbands. The colour bar is in units of $2e^2/h$.

Figure 4 shows the differential conductance plot of the device with a lower 2D carrier density measured in the second cooldown. The split gate voltage was swept for various back gate voltages from 0 V (left) to -32 V (right) in steps of -2.0 V. The quantised plateaus in units of $2e^2/h$ are observed, in addition to a well-defined shoulder representing the 0.7($2e^2/h$) structure, shown by a (+) symbol on the first trace on the left of Fig. 4(a). On further making the back gate voltage more negative, which in turn makes the confinement weaker, the 0.7 structure goes through a gradual weakening process and on a few occasions, signatures of regaining the strength (shown by a (*) symbol) were observed before finally forming the

0.5($2e^2/h$) structure, [see the colourplot as the upper inset in Fig. 4(a)]. This dynamic process is shown within the dotted rectangle in Fig. 4(a). Also, we have included a lower inset in the main plot of Fig. 4, which shows selected traces from the main plot, where the transition from 0.7 to 0.5 features may be clearly seen. It appears that the system was trying to stabilise between the 0.7 and 0.5 structures; it may indicate ferromagnetic ordering due to the reduced carrier density, which increased exchange correlation.[28,29] The result is presented differently in Fig. 4 (b) by differentiating data in Fig. 4(a). In this plot, a valley represents a plateau, so 0.7, 1 and 2 are labelled at the bottom trace. The re-strengthening of the 0.7 structure is shown by the (*) symbol. The traces between the (*) symbols show a regime where instability of the 0.7—0.5 states was noted. The higher traces show the regime when the system has entered into a fully spin-polarised state, represented by a plateau at the 0.5($2e^2/h$) structure.

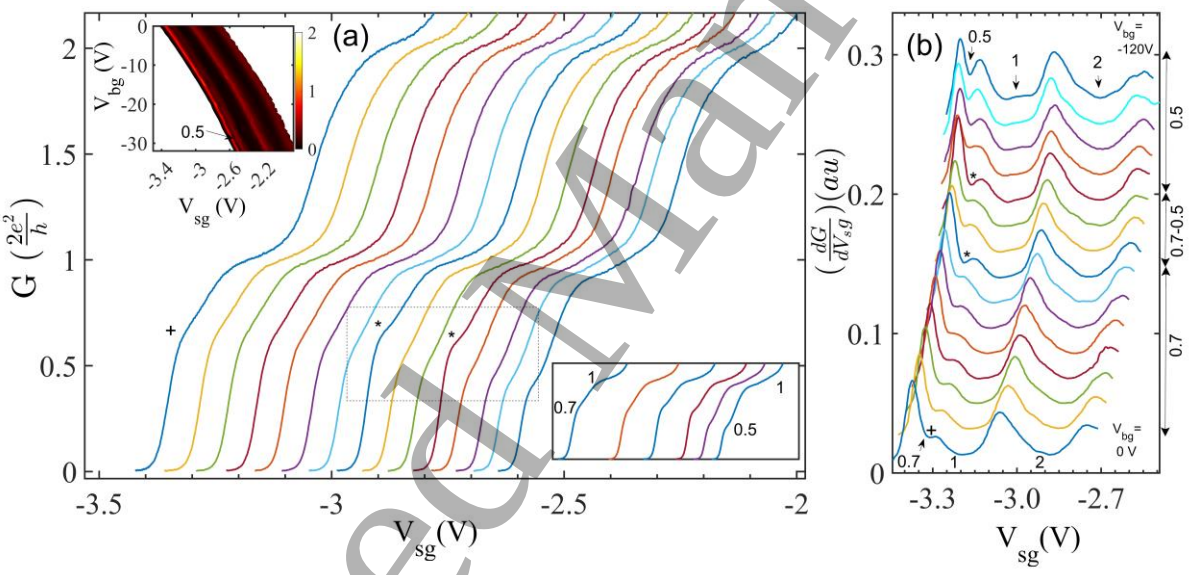

Fig. 4. (a). The differential conductance measurements of a split gate device with a back gate in the second cooldown. For each trace, the conductance is measured as a function of V_{sg} at a fixed V_{bg}. V_{bg} is incremented in steps of -2 V from 0 V on the left to ~ -32 V on the right. a) The 0.7 structure loses strength as the back gate becomes more negative, resulting in a regime, indicated by a dotted rectangle, where the 0.7 and 0.5 structures appear to compete due to exchange correlation. Finally, the 0.7 structure settles at a value close to the 0.5 ($2e^2/h$) structure. The upper inset shows a colourplot of the transconductance of data in Fig. 4(a), dG/dV_{sg} ,as a function of V_{sg} and V_{bg}. Regions of high transconductance are shown in red and low transconductance (plateaus) in black. The colour bar is in units of $2e^2/h$. The lower inset

shows selected traces from the main plot, where the transition from 0.7 to 0.5 features may be clearly seen (b). The transconductance (dG/dV_{sg}) plots of data in Fig. 4 (a) is shown. Here, dG/dV_{sg} is plotted as a function of V_{sg} and V_{bg}, the bottom trace is taken at V_{bg}=0 V, and subsequent traces were taken at increments of -2.0 V so that the top trace was taken at V_{bg}~ -32 V. The plots have been offset vertically (0.1 (a.u.)) and horizontally (-0.021 V) for clarity.

In the second cooldown, the spin-polarized 0.5 feature was observed in a low-density 1D wire, where the density of 2DEG was estimated to be lower than in the first cooldown. Figure 3 presented the differential conductance results obtained during the first cooldown. As the carrier density decreased, the 0.7 structure became more pronounced, while the first plateau at $2e^2/h$ diminished and ultimately disappeared. This left only the 0.7 structure visible at an applied back gate voltage of ~ -120 V. However, in these results, we could not detect the transition of the 0.7 structure into the 0.5 feature, possibly due to resolution issues in the measurements or confinement potential in the extremely low-density regime. It is important to note that the back gate affects the entire 2DEG, not just the 1D channel, which may restrict our access to very low-density areas. Figure 4 shows the results on the device measured in the second cooldown with a lower, starting 2D carrier density. In this plot, we noticed the observations of the 0.7 structure and, subsequently, the spin polarised 0.5 feature as the local density within the 1D channel was reduced with the help of a back gate (with a maximum negative voltage of ~ -32 V).

We should look at a few differences between the two plots. The plateau width in Fig. 4 for the left trace is narrower than in Fig. 3, left trace. This suggests that the starting 2D density in Fig. 3 was higher, while in Fig. 4, it was lower. When there are more carriers in a 1D channel, the likelihood of many-body effects diminishes because the electrons are strongly confined. However, as we reduce the number of carriers and the confinement potential, interaction effects begin to dominate over kinetic energy, leading to the observed 0.5 anomaly. This scenario appears to be more relevant to the conditions illustrated in Fig. 4. Therefore, it is crucial not only to achieve a lower starting density for the 2DEG but also to effectively reduce both the confinement and the local 1D density within the 1D channel.

The two kinds of controlled illumination were done in the present work to produce the conditions for observing the spin-polarised effect within the 1D channel. Moreover, the illumination has a significant effect on the 2DEG density; it is generally linked to the persistent

photoconductivity of DX and other charged centres, which release electrons when illuminated. The illumination also affects the background potential and homogeneity in the 2DEG. In our view, the observed spin-polarized and other many-body effects are influenced by a delicate balance between the 2D density and the precise adjustment of the 1D density, along with the confinement potential that defines the 1D constriction or channel. It may be noted that we have replicated this effect in several cooldowns and across three different wafers.

It is recognised that electrons' spin is unstable at low densities due to decreased kinetic energy compared to the exchange energy between interacting electrons.[28,30] In a strictly 1D system where a single mode ($2e^2/h$) is occupied, sweeping the split gate towards pinching off the channel reduces carriers in the system which increases exchange energy resulting in spontaneous spin polarisation. This introduces a separation of bands based on spin orientation, which eventually affects the transmission through the system. The spontaneously polarised spins, so created, aligned in a preferred direction, called parallel spins, occupy the lowest subband. This results in a conductance plateau appearing at e^2/h and a plateau at $2e^2/h$, represented by antiparallel spins.[28] The degree of spin polarisation can be substantial for systems where an additional gate is utilised to effectively reduce carriers and weaken the confinement potential. In our case, when the back gate is made more negative, the exchange potential dominates the transport with current carried by aligned spins, resulting in a spin polarised conductance plateau.

We estimated the density of electrons in the weaker confinement to be n_{2D}~ 5.5 x 10^{10} cm^{-2} ($n_{2D} = \varepsilon\varepsilon_0 V_P/2\pi eW$, here W=500 nm is the separation between the split gate) at V_{sg}= -2.5 V, where the e^2/h plateau was observed [Fig. 4]. For the estimation of density of 1D electrons n_{1D} per unit length, we calculated the depletion length, $l \sim 159\ nm$ of the 2DEG created by the split gate[37,38] using the relation $l = \varepsilon\varepsilon_0 V_P/2\pi^2 n_{2D} e$, where n_{2D} ~ 5.5 x 10^{10} cm^{-2} (estimated above), and $V_P = V_{sg} = -2.5\ V$. Using the value of l, n_{1D} was estimated to be ~8.7 x10^5 cm^{-1} such that $n_{1D} a_B < 1$, where $a_B = 10\ nm$, is the effective Bohr radius of GaAs ($a_B = \varepsilon\hbar^2/m^* e^2$, here $\hbar$ is the reduced Planck constant and $m^* = 0.067$ is the effective mass of electron in GaAs), which suggests the system has possibly formed the 1D Wigner lattice, in agreement with previous reports.[14,19-25] In the case of a low-density quantum wire, the kinetic energy is small compared to the electron-electron interaction energy $e^2 n_{2D}/\varepsilon$. Therefore, the electrons will reorganise themselves placed at equidistant locations forming a

zigzag to minimise the Coulomb repulsion. Such rearrangement of electrons in 1D is called the Wigner lattice.[22,23] The 1D electrons forming a Wigner lattice can also be viewed as an antiferromagnetic Heisenberg spin chain with small exchange coupling, *J*, between the nearest neighbours.[19-23] Such spin modes propagate independently to the charge modes, therefore their combined effect can affect the conductance in the ground state of a quantum wire. The results in Fig. 4, where the 0.7-0.5 structures fluctuate in the moderate density regime and later the 0.5 structure strengthens in the low-density regime, perhaps suggest spin modes propagate with different velocities affecting the transmission or conductance in the ground state. The exchange coupling, *J* may be expressed as $J{\sim}E_E(n_{1D}a_B)^{-3/4}\exp\left(-\eta(n_{1D}a_B)^{-\frac{1}{2}}\right)$, where E_F is Fermi energy of the 2DEG, and $\eta{\sim}2.82$.[22,23] It may be noted that *J* varies exponentially with n_{1D}, therefore the former becomes very significant at very low densities. Also, for a similar reason, the estimation of *J* is very difficult due to inaccuracies in the estimation of n_{1D}. Furthermore, the spin excitations contribution to conductance becomes effective when $J \ll T \ll E_F$, our measurement temperature of 70 mK is well within this regime when J/k_B~ 2mK from[23,33], and E_F/k_B~1.7 K. Further detailed measurements, including the estimation of spin coupling constant J, are in progress and will be published elsewhere.

In conclusion, we have shown spin transport in a weakly confined, low-density quantum wire defined using a back-gated, split gate device. Our results show the presence of a strong exchange-driven spin polarised conductance plateau at e^2/h in a low-density 1D quantum wire in agreement with the theoretical prediction. A low density 1D system shows potential for applications in spintronics and quantum electronics.

The work is funded by the United Kingdom Research and Innovation (UKRI), Future Leaders Fellowship (References: MR/S015728/1; MR/X006077/1), the Engineering and Physical Sciences Research Council (EPSRC), the Royal Society and the Science and Technology Facilities Council, STFC (Reference: ST/Y005147/1).

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