A High-Voltage Differential SPDT T/R Switch for Ultrasound Systems

Yaohua Zhang, *Student Member, IEEE*, Dai Jiang, *Senior Member, IEEE*, and Andreas Demosthenous, *Fellow, IEEE*

***Abstract*—An improved bootstrapped circuit topology is proposed for the design of a high-voltage, differential, single-pole double-throw transmit/receive switch for an ultrasound hand gesture recognition system. The differential transmit/receive switch is designed in a 0.18 µm HV BCD technology. It is intended to interface with bimorph piezoelectric micromachined ultrasonic transducer electrodes, although a single-ended version can also interface with conventional ultrasound transducers. A comprehensive analysis has produced useful insights, namely the dependence of off-isolation on high-voltage input slew rate, and the dependence of common-mode rejection ratio on threshold mismatch and timing misalignment. In addition, an extended model has been developed to predict harmonic distortion through a DMOS transistor. Measured results verify the effectiveness of the design guidelines and switch operation. The switch circuit exhibits 67 Ω on-resistance and −63 dB off-isolation while occupying a modest area of 289 µm × 295 µm. The switch achieved a figure-of-merit with 74% improvement over the state-of-the-art. To the best of the authors' knowledge, this differential switch is the first of its kind reported for piezoelectric micromachined ultrasonic transducer biomedical ultrasound systems.**

***Index Terms*— Bipolar-CMOS-DMOS (BCD), MOSFET switch, high-voltage analog switch, single-pole double-throw switch, transmit/receive switch, ultrasound hand gesture recognition.**

I. INTRODUCTION

HIGH-VOLTAGE semiconductor switches form an integral and indispensable component in many modern applications, such as MEMS drivers [1], neurostimulators [2], [3], power management SoC [4], RF front-ends [5], and ultrasound imaging [6]-[13]. The use of high-voltage switches is especially prevalent in ultrasound applications, which typically drive the transducers with several tens of Volt [14]. For ultrasound applications a high-voltage switch can be employed to deliver high-voltage pulses to the transducers in place of an integrated pulser circuit [9], [10] or more commonly, as a transmit/receive (T/R) switch to protect the low-voltage circuits [15-17]. In a typical ultrasound system (Fig. 1), the receive-side (RX) circuits such as the low-noise amplifier, filters, and analog-to-digital-converter (ADC) are constructed using low-voltage transistors [18], [19]. On the other hand, the transmit (TX) pulses are high-voltage signals. Therefore, it is necessary to use a T/R switch to isolate and protect the RX circuits from any high-voltage pulses that may couple through unintentionally. Prior to the 1980s and even to some extent in modern times, the diode-bridge limiter circuit constructed using discrete components was a popular choice for the T/R switch in ultrasound systems [20]. However, the diode-bridge limiter is not suitable for on-chip integration because the forward bias current required makes it power hungry. The advent of Bipolar-CMOS-DMOS (BCD) technology enables high-voltage and low-voltage circuits to be fabricated on the same die. As a result, on-chip T/R switch topologies are feasible and the circuits in an ultrasound system are progressing toward

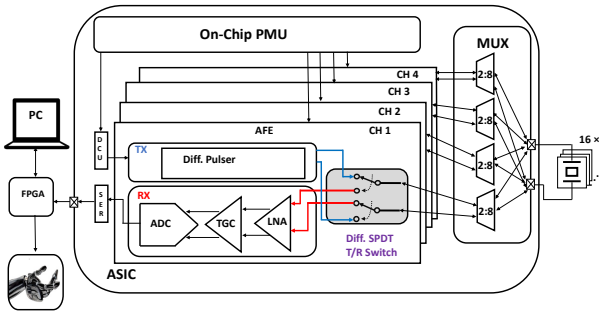


Fig. 1. Proposed architecture of an ultrasound hand gesture recognition system, with the role of the differential T/R switch highlighted in grey. Note that four differential transducers share one differential analog front-end.

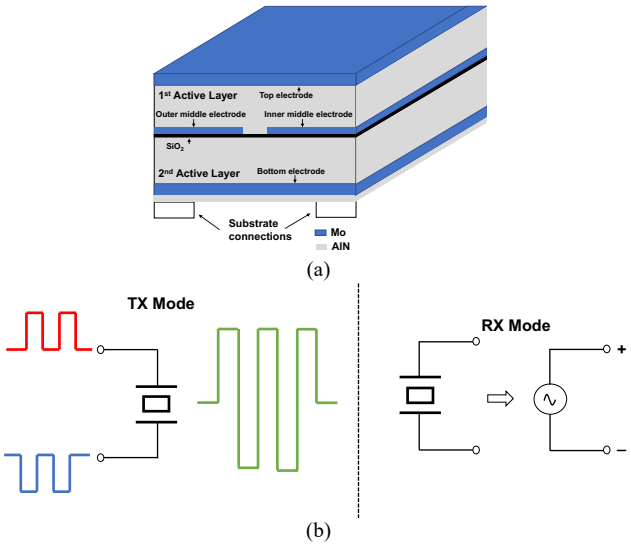


Fig. 2. (a) Bimorph PMUT structure [17]. (b) Operation of the bimorph PMUT in TX and RX modes.

Manuscript submitted 28 April, 2024; revised 16 June, 2024. This work was supported by the European Union's Horizon 2020 Research and Innovation Program under Grant 899822. *(Corresponding author: Andreas Demosthenous).*

Yaohua Zhang, Dai Jiang, and Andreas Demosthenous are with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, United Kingdom (e-mail: yaohua.zhang@ucl.ac.uk; a.demosthenous@ucl.ac.uk).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org

full on-chip integration.

Presently, the trend in ultrasound ASIC design is to interface with an increasing number of transducers. For instance, in medical ultrasound imaging, the ASICs designed in the early 2000s tended to interface with a small number of transducers (16 transducers in [21]). They now target more than a hundred transducers [22], [23]. When interfacing with a small number of transducers, the circuits can be designed to be single-ended and relatively simple with acceptable performance [24]. Unfortunately, the shift toward a higher transducer count has exacerbated the complexity and challenges associated with the ASIC design. With more than a hundred transducers available in catheter-based ultrasound imaging, it is impractical to connect wires to every individual transducer. Consequently, cable-reduction techniques must be adopted, and various techniques have been proposed such as sub-array beamforming [22], time-division multiplexing [25], and frequency-division multiplexing [26]. However, these cable-reduction techniques have worsened the distortion, crosstalk, and power supply rejection [27], which necessitate either system-level mitigation [28] or more complex on-chip power rail regulation [29]. Due to their inherent drawbacks with regard to distortion and crosstalk, single-ended interface circuits [21], [24] are no longer viable. Without a more effective solution, the trend toward an increasing transducer count will only cause more severe performance deterioration.

On a related note, a new type of ultrasound transducer, the piezoelectric micromachined ultrasonic transducer (PMUT) in Fig. 2(a) has seen remarkable advances and has been successfully demonstrated in applications such as drone/robot vision [16]. The advent of PMUT is game-changing because it is CMOS-compatible (advantage over piezoelectric crystals) and does not require a high-voltage dc bias (advantage over capacitive micromachined ultrasonic transducers) [14]. Recently, bimorph PMUTs [Fig. 2(a)] made from an AlN/Mo/AlN stack have been proposed [30], [31]. From a circuit design perspective, an important advantage that bimorph PMUTs offer is that they allow for *fully differential* interface circuits. Due to its physical structure, a bimorph PMUT can act as a differential load (TX mode) or differential signal source (RX mode), as illustrated in Fig. 2(b).

Considering the severe performance challenges that ultrasound ASICs face and the availability of a differential transducer, a fully differential architecture is becoming a more attractive and superior choice, especially when interfacing to a large number of transducers. A fully differential architecture is a natural choice when interfacing with bimorph PMUTs, and can reap benefits including reduced crosstalk, higher linearity, and greater immunity to power supply noise, at a moderate increase in area and power. A fully differential architecture naturally calls for a differential T/R switch.

To the best of the authors' knowledge, a differential T/R switch for ultrasound applications has not been published to date. This paper aims to fill this gap and presents the design of a high-voltage differential single-pole double-throw (SPDT) T/R switch. The proposed switch introduces new features to the well-established single-ended, single-pole single-throw (SPST) ultrasound T/R switch and can stimulate new applications that require a differential architecture. The switch is intended for use in a fully differential ASIC (both TX and RX circuits are differential) for next generation ultrasound hand gesture recognition applications such as prosthetic/robotic hand control, interactive gaming, and virtual/augmented reality [32], [33]. A preliminary version of this paper has been reported in a conference paper [32]. The rest of the paper is organised as follows. Section II reviews the state-of-the-art, Section III discusses and analyses the proposed switch circuit, Section IV presents the measured results and Section V concludes the paper.

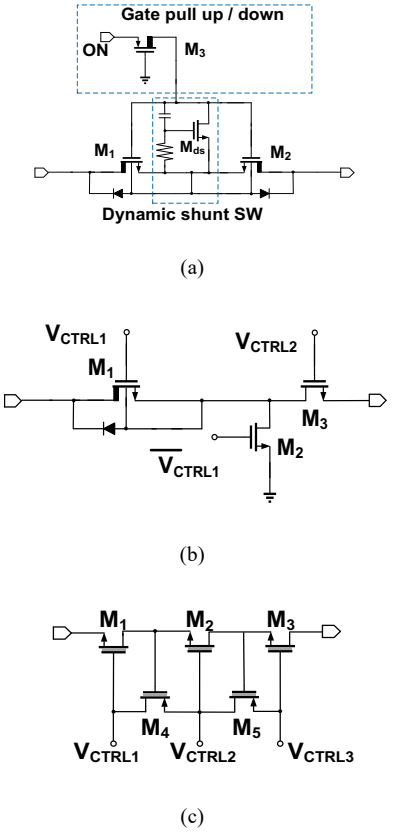


Fig. 3. State-of-the-art ultrasound T/R switches. Thick drain devices refer to DMOS, thick gate devices refer to thick-oxide, nominal 3.3 V devices (a) Bipolar T/R switch with dynamic shunt control [12]. (b) Series-shunt unipolar T/R switch [34]. (c) Unipolar, stacked-transistor T/R switch [17].

II. State-of-the-art Analysis

In ultrasound applications, high-voltage switches may sometimes be confused with T/R switches. To avoid this confusion, this paper adopts a nomenclature similar to that proposed in [12]. A high-voltage switch is defined as a switch that only passes high-voltage transmit pulses to the transducers, whereas a T/R switch is defined as a switch that is capable of passing high-voltage transmit pulses during the TX mode (optional), and of passing small receive signals and isolating high-voltage pulses simultaneously during the RX mode. A T/R switch should have mutually exclusive TX and RX paths. The T/R switch proposed in this paper is similar to T/R switches commonly used in RF front-ends [35], [36].

The performance of a T/R switch can be measured by the

following specifications:

- On-resistance (R_{on}): the dc resistance of the switch when turned on. R_{on} is an important parameter to minimize because it directly influences the bandwidth, distortion, thermal noise, and switching time of the switch.
- Off-isolation: how well the T/R switch is able to prevent high-voltage TX pulses being coupled to an undesired port. Without adequate off-isolation, there is a risk that the low-voltage transistors will be permanently damaged by high-voltage pulses that leak through.
- Linearity: the harmonic distortion introduced by the switch when turned on. The required distortion level is directly influenced by the subsequent ADC in the RX signal chain.
- Switching time: the delay introduced by the switch between a signal at the input port and the same signal at the output port.

Ultrasound T/R switches can be split into two broad categories, bipolar and unipolar. Bipolar T/R switches [Fig. 3(a)] are designed to block out both positive and negative high-voltage pulses. By virtue of its construction, there exists a parasitic drain-source diode in a DMOS. A single DMOS cannot block out negative voltage pulses because this parasitic diode will be forward biased. Therefore, bipolar T/R switches have at least two DMOS arranged in a back-to-back configuration. The main reason why both positive and negative voltages are used is to increase the peak-to-peak TX voltage and generate stronger ultrasound waves. Note that the T/R switch proposed in this paper is a unipolar design because another advantage of a differential design is that a large peak-to-peak TX voltage [Fig. 2(b)] can be generated using positive voltages only, which greatly simplifies circuit design and testing.

Among the unipolar ultrasound T/R switches published, a popular design is a series-shunt circuit, as illustrated in Fig. 3(b) [34]. On top of a series DMOS transistor which withstands most of the high-voltage TX pulse, a low-voltage shunt transistor is included to provide a low impedance path to ground. In the authors' experience, this shunt device presents only a small area penalty but can provide several tens of dB improvement in off-isolation.

Another category of unipolar ultrasound T/R switches uses standard CMOS transistors [Fig. 3(c)], instead of high-voltage DMOS because of system-level considerations, i.e. with standard CMOS, there could be more intellectual properties (IPs) accessible [17]. In such a scenario, the T/R switch can be made high-voltage tolerant using a stack of deep N-well, thick-oxide CMOS transistors [17]. For instance, the design in [17] stacks five 3.3 V nominal transistors to form a switch capable of blocking out a TX voltage of 13.2 V with some margin. Although stacked-transistor T/R switches have been demonstrated successfully, the disadvantage is that these switches require complex gate control signals.

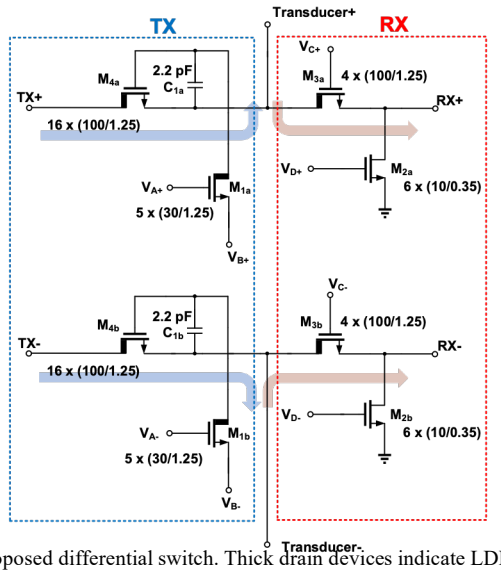
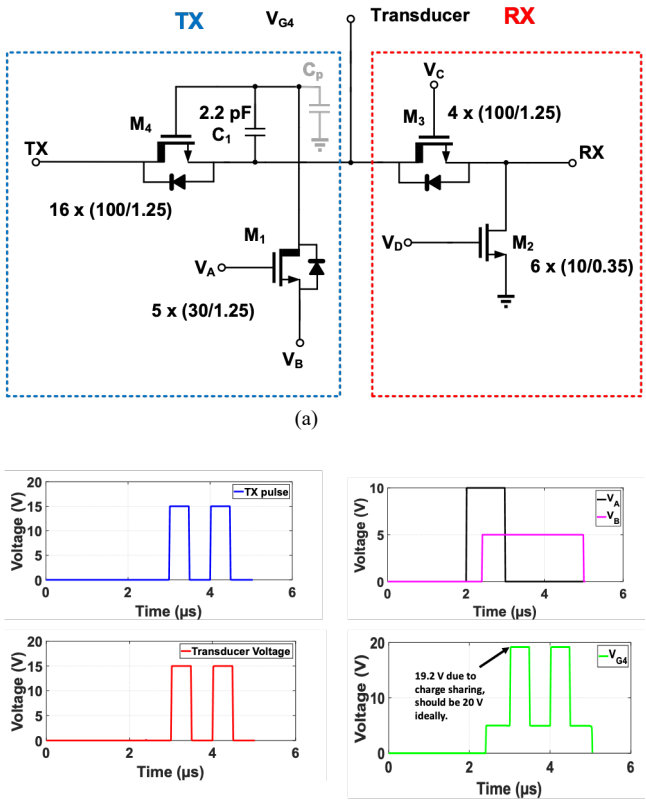


Fig. 4. Proposed differential switch. Thick drain devices indicate LDMOS, whereas standard NMOS symbols refer to a 3.3 V low-voltage transistor. Dimensions in µm.



(a)

(b)

Fig. 5. (a) Single-ended half-circuit with DMOS body diode and parasitic capacitance explicitly drawn. Dimensions in µm. (b) Simulated control waveforms.

III. Proposed Switch Circuit

The proposed differential SPDT T/R switch is shown in Fig. 4. As mentioned previously, this switch is intended for use in a next generation wearable ultrasound hand gesture recognition system. In this hand gesture recognition system (Fig. 1), there

are 16 transducers distributed evenly around the forearm. However, the hand gesture recognition ASIC only contains 4 analog front-end channels and employs a multiplexing strategy to access the 16 transducers. Preliminary studies conducted by the authors and project partners have revealed that ultrasound interrogation of more positions around the forearm is more important than activating a greater number of transducers simultaneously. It is beneficial to distribute more transducers around the forearm. On the other hand, dedicating an analog front-end per transducer will only bring diminishing marginal returns as the transducer count increases. This contrasts with ultrasound catheter/probe-based imaging applications which prioritize a large number of transducers activated simultaneously for better image quality, i.e. *n* transducers require *n* analog front-ends. In these imaging applications, it is possible to use an SPST T/R switch connected to the RX circuit input because the pulser circuit is directly connected to the transducer. For ultrasound hand gesture recognition purposes, the use of multiplexing means that the pulsers cannot be directly connected to the transducers and SPST T/R switches cannot be used. Therefore, the T/R switch in this paper is designed to be SPDT to support multiplexing.

A. T/R Switch Circuit Operation

The operation of the proposed differential SPDT switch can be best explained by considering its half-circuit as shown in Fig. 5(a). In RX mode, the series transistor M_3 is turned on, the shunt transistor M_2 is turned off and the TX side is disabled. The switch is sized to have a low R_{on}. A low R_{on} minimizes thermal noise and will not degrade the signal-to-noise ratio of the RX circuits. Although a single high-voltage DMOS M_3 can be used, a shunt transistor M_2 is included to improve off-isolation by providing a low-impedance path to ground.

In the TX mode, M_3 is turned off and M_2 is turned on to isolate the RX circuit from high-voltage pulses. In order to transfer high-voltage pulses while obeying a reasonable area constraint, the TX switch is designed as a bootstrapped switch, adapted from [10]. The bootstrapping action is an area-efficient technique compared to designing a separate high-voltage latch circuit to control the switch. In contrast to that in [10], the proposed switch has a simpler structure and is more area-efficient as it cuts down on redundant diodes and transistors. The proposed TX switch consists of only two high-voltage DMOS (M_1, M_4) and one capacitor (C_1), unlike that in [10] which contains three high-voltage DMOS, two diodes and two capacitors. Another crucial difference is that the proposed switch does not require forward biased diodes to operate. Note that in most p-substrate CMOS technologies, a forward biased pn junction (typically implemented using a Schottky diode or npn/pnp BJT) is considered risky as it requires additional processes to guarantee that substrate leakage current does not damage the die. The use of a forward biased pn junction is either forbidden or discouraged.

The TX side is designed to transfer a 0 V to 15 V, 1 MHz square pulse to the transducer (modelled as a 20-pF load). To do so, M_4 is turned on and the high-voltage pulses pass from its drain to its source, which is also connected to the transducers. Comprehensive simulations showed that a V_{GS4} of around 5 V is required to turn on M_4 to an acceptable R_{on}. Hence, the V_{G4} is required to be as high as 20 V when passing the 15 V pulses to the transducers. The maximum V_{GS} for the DMOS transistor in the chosen BCD technology is 18 V. This implies that a simple 0 V (low) / 20 V (high) signal cannot be used to control V_{G4}. Instead, a bootstrapped switch has been designed that ensures a 5 V offset between the gate and source of M_4 even when passing the 15 V pulses. As seen from Fig. 5(b), when V_A goes high to 10 V first, V_{GS1} is 10 V, and M_1 is turned on. This pulls the top plate of V_1 down to V_B which is at 0 V. Subsequently, when V_A and V_B are both high, V_{GS1} is equal to 5 V, M_1 is still turned on and charges the top plate of C_1 (V_{G4}) to 5 V which also turns M_4 on. When the high-voltage pulses arrive, M_4 is bootstrapped and C_1 maintains the required overdrive voltage to keep M_4 on.

Note that DMOS break down could be an issue in bootstrap circuits if not properly considered. The maximum V_{DS} of the DMOS used in this work is 40 V. The maximum V_{DS} will never be exceeded because there are no signals that are higher than 20 V. There is a safe margin of 20 V for V_{DS}. In addition, because of the way the bootstrapping action works, V_{GS4} never exceeds 5 V. The DMOS transistor is always working within its safe operating region, so DMOS break down is not an issue to be concerned within this work.

B. RX Distortion Analysis

Since the shunt transistor M_2 is turned off in the RX mode, the overall distortion performance is primarily determined by M_3. Although well-known bootstrapped and complementary switch structures can minimize distortion, the associated area penalty and increased design complexity do not make them attractive options in ultrasound T/R switch design. Through rigorous analysis and careful optimization, the use of a single N-type DMOS (M_3) can be designed for acceptable distortion levels.

During the RX mode, M_3 effectively serves as a sampling switch. The main source of distortion is the input-dependent R_{on}, which causes an input-dependent delay across M_3 [37]. Note that M_3 is turned on during the entire period of the RX mode and not turned on/off according to a sampling clock as in ADC track/hold stages. Therefore, the other sources of distortion such as charge injection and turn-off timing that are applicable to ADC track/hold stages are not relevant to this application. In the RX mode, M_3 forms an *RC* low-pass filter with the input capacitance of the subsequent gain stage and the off-capacitance of the shunt transistor M_1. Assuming, without loss of generality that R_{on} is constant, the bandwidth of the switch is much larger than the input signal bandwidth and the input signal $v_{in}(t)$ is an ac signal with zero dc offset. With appropriate Laplace and inverse Laplace transforms, it can be shown that the output voltage $v_{out}(t)$ is a delayed version of the input signal as in (2).

$$\tau \triangleq R_{on}C_{out}. \tag{1}$$

$$v_{out}(t) \approx v_{in}(t-\tau). \tag{2}$$

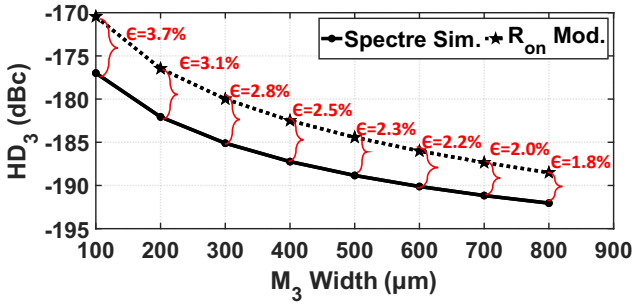


Fig. 6. HD_3 versus widths of M_3.

Next, the assumption of a constant R_{on} is revisited. In practice, the R_{on} of M_3 is not a constant value but a non-linear, multi-variable function that does not have a well-defined, explicit expression, unlike that for a standard CMOS transistor. The presence of the drift region in a DMOS introduces quasi-saturation, which causes the velocity saturation of carries to occur before actual saturation via pinch-off [38]. This complicates the modelling of DMOS drain current significantly. A precise model of DMOS drain current must rely on computer simulations that solve Poisson's equation iteratively as done in the HiSIM-HV model [39] adopted by the process design kit of this BCD process.

In response to the unwieldy HiSIM-HV model, an approximate model for DMOS drain current using the hyperbolic tangent function has been proposed in [38] that is more intuitive and friendlier for hand calculations. The advantage of a hyperbolic tangent function is that its shape approximates the typical shape of I_{DS}/V_{DS} curve, and its higher order derivatives are also continuous. In [38], I_{DS} is defined as

$$I_{DS}(V_{DS}) = I_{Dsat}\tanh\left(\frac{g_{d0}V_{DS}}{I_{Dsat}}\right)(1+\lambda V_{DS}), \tag{3}$$

$$g_{on}(V_{DS}) = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{g_{d0}}{\cosh^2\left(\frac{g_{d0}V_{DS}}{I_{Dsat}}\right)}, \tag{4}$$

where I_{Dsat} is the drain saturation current, λ is the channel length modulation parameter, and g_{d0} is the small signal drain conductance at zero V_{DS}. The asymptotic behavior of (3) at extreme values of V_{DS} can be easily verified by inspection. The advantage of (3) is the small number of dependent parameters, which can all be easily extracted from simulations.

In this paper, the authors present an extension to the hyperbolic tangent model (3) specifically for the triode region, which is more suitable for modelling switch operation. The authors present a linear model for $g_{on}(V_{DS})$ that is dependent on two easily extractable parameters. The value of g_{d0} is extracted from the simulated I_{DS}/V_{DS} curve. g_{d0} represents the maximum slope of the I_{DS}/V_{DS} curve. The valid range ($V_{DS,valid}$) for linear modelling is determined next. The valid range is defined as the maximum V_{DS} beyond which g_{on} drops below 90% of g_{d0}. This valid range can be tightened for greater accuracy. The linear slope (h) of g_{on} from g_{d0} to the value of g_{on} at $V_{DS,valid}$ is finally computed. The linear model of g_{on} across the valid range is defined as

$$g_{on}(v_{in}) \triangleq \frac{1}{R_{on}(v_{in})} = g_{d0} - hv_{in}. \tag{5}$$

Equation (5) is substituted into the output signal (2) and approximated by the first three terms of the Taylor series expansion in (8).

$$v_{out}(t) \approx v_{in}(t-\tau) \approx v_{in}(t) - \tau_0\frac{dv_{in}(t)}{dt}. \tag{6}$$

$$\tau(v_{in}) = R_{on}(v_{in})C_{out} \tag{7}$$

$$\approx C_{out}\left(R_{on}(0) + v_{in}\frac{dR_{on}}{dv_{in}}(0) + \frac{1}{2}v^2{}_{in}\frac{d^2R_{on}}{dv_{in}^2}(0)\right). \tag{8}$$

Substituting the input signal $v_{in}(t) = A\sin\omega_0 t$ into (8) and (7) into (6) and taking the amplitudes of the harmonics, the harmonic distortion equations (up to third order) can be found. Given the differential operation of the T/R-switch, it is more meaningful to look at HD_3 because even-order distortion will be suppressed. HD_3 is given by

$$\mathrm{HD}_3\left(W/L\right) \approx \frac{A^2C_{out}\omega_0h^2}{4g_{d0}^3}. \tag{9}$$

The HD_3 values predicted by (9) and those obtained from Spectre simulations are plotted against the widths of M_3 in Fig. 6. Although increasing the width of M_3 can improve HD_3 as predicted in (9), Fig. 6 shows diminishing marginal returns beyond 400 µm. Fig. 6 shows that the linear model can predict HD_3 to a surprisingly high accuracy, with a maximum error of only 3.7%. However, the limitation is that neither (9) nor the corresponding Spectre simulations include the effects of circuit noise. In practice, the harmonic distortion performance of the proposed switch will be noise-limited.

C. TX Speed Analysis

In Fig. 5 the speed or the rise/fall time of the TX branch is determined primarily by the R_{on} of M_4, which to a first-order, is inversely proportional to i) the voltage V_{G4} held on the bootstrap capacitance, and ii) the width of M_4. In order to hold a sufficiently large voltage V_{G4} for a certain rise/fall time, the bootstrap capacitance needs to be sized carefully by accounting for the non-trivial parasitic capacitance at the drain node of M_1. This parasitic capacitance (labelled as C_p in Fig. 5) includes the drain capacitance of M_1 and the gate capacitance of M_3. Charge sharing with C_p causes the bootstrapped voltage to be lower than expected, resulting in an increased R_{on} and propagation delay across the drain/source terminals of M_4.

An often-neglected impact of the increased propagation delay is the higher risk of violating the maximum allowed forward bias voltage of the parasitic pn junction between the drain (cathode) and source (anode) of M_4. This diode is typically designed to withstand a large reverse bias voltage but a small

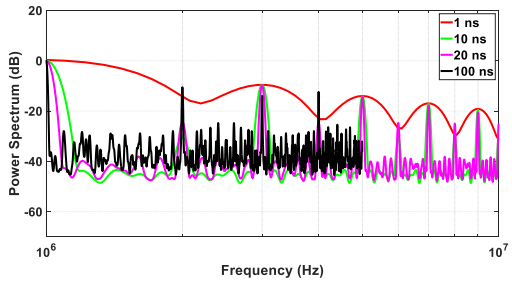


Fig. 7. Power spectra for trapezoidal waves with 1 MHz frequency, 50% duty cycle, and 15 V amplitude (normalized) but varying rise/fall times are plotted.

forward bias voltage (maximum of 0.5 V in this technology). If there were no propagation delay through a DMOS transistor, then with a square wave passing from its drain to its source, the pn body diode would never be forward biased. However, due to a non-zero propagation delay in practice, it is unavoidable that its source voltage will be higher than its drain voltage for a short time instant when transferring a square wave. Naturally, a smaller propagation delay will lead to a smaller forward bias voltage in the pn junction. Extensive simulations across different corners revealed that C_1 must be sufficiently large (2.2 pF, MIM) to provide enough overdrive for a sufficiently low R_{on}, an acceptable rise/fall time, and a forward pn bias voltage that is well within the safety limits of the technology.

In addition to a sufficiently high overdrive voltage, the width of M_4 must be increased to achieve a faster rise/fall time, incurring a significant area penalty. Before a decision on the optimal width of M_4 is made, it is important to explore the impact of rise/fall time on the TX pulse distortion performance. Assuming a trapezoidal wave is used to approximate a square wave, its Fourier series expansion $f(t)$ is:

$$f(t) = C_0 + \sum_{n=1}^{\infty} C_n \cos(n\omega_0 t + \Phi_{cn}), \tag{10}$$

$$C_n = \frac{1}{T}\int_{t_0}^{t_0+T} f(t)e^{-jn\omega_0 t}dt, \tag{11}$$

$$C_0 = \frac{AT_0}{T} - \frac{A}{2}. \tag{12}$$

For $n \neq 0$ and $t_r = t_f$, the magnitude of the coefficients C_n [40] is:

$$C_n = \frac{2AT_{on}}{T}\left|\text{sinc}\frac{n\pi T_{on}}{T}\right|\left|\text{sinc}\frac{n\pi t_r}{T}\right|. \tag{13}$$

By taking the envelope of the amplitudes of the Fourier coefficients C_n, an upper bound or worst-case magnitude spectrum can be obtained. It has been proved in [40] that this envelope function exhibits two poles. On the other hand, for a square wave with zero rise/fall times, its magnitude spectrum envelope exhibits only one pole. From a distortion perspective, it is desirable to have non-zero rise/fall times because the harmonic content at higher frequencies will be suppressed to a greater extent. The power spectra of trapezoidal waves with 1

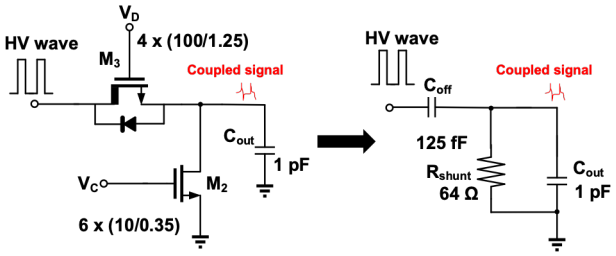


Fig. 8. Proposed first-order *CRC* circuit for off-isolation modelling. Source resistance of the TX circuit can be ignored.

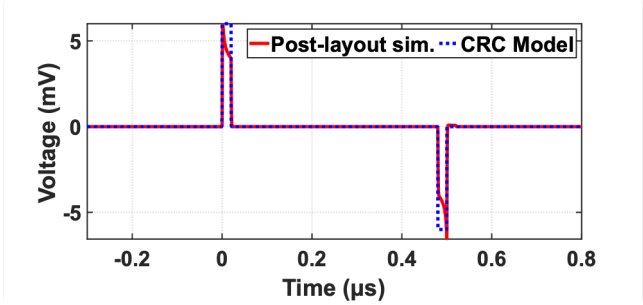


Fig. 9. Post-layout simulation of the coupled spike waveform at the RX output port vs the spike waveform predicted by the proposed model.

MHz frequency, 50% duty cycle, and 15 V amplitude (normalized) but varying rise/fall times are plotted in Fig. 7. The harmonic content with a rise/fall time of 1 ns is larger than that with a 100 ns rise/fall time. Although a slow rise/fall time is advantageous for harmonic distortion, it results in less acoustic power being generated by the transducer. A rise/fall time of 20 ns yields a second harmonic that is around 40 dB lower than the fundamental, which is sufficient for a TX pulse in most ultrasound applications [41]. To support 20 ns, M_4 needs to be sized as 1600 μm, which is an acceptable dimension. A rise/fall time of around 20 ns is selected as the optimal design target. Targeting a rise/fall time faster than 20 ns brings diminishing marginal returns because the width of M_4 will have to be increased disproportionately. Note that it is unavoidable for the TX distortion to be worse than RX distortion, considering the large TX voltage swing and the square pulse shape. It is known that distortion tends to worsen with large voltage amplitudes and a square pulse contains more harmonics inherently.

D. Off-isolation Analysis

The off-isolation performance is a crucial aspect of a T/R switch that warrants a thorough investigation into its root causes and dependent factors. However, the many complex and non-linear capacitances associated with the extra drift region in DMOS transistors have complicated greatly the exact modelling of off-isolation. To arrive at a practical off-isolation circuit model, a bold but effective approximation was made to reduce the entire DMOS M_3 from at least nine nodal capacitances in the off-mode to a single lumped capacitance, C_{off} from its drain to source terminals (extracted from simulations). M_2 is approximated as a shunt resistance R_{shunt}, which models the R_{on} of M_2. In combination with C_{out}, a first-order *CRC* circuit (Fig. 8) is proposed which models off-isolation to a high level of accuracy.

The transfer function of the first-order *CRC* model $H(s)$ is:

$$H(s) = \frac{Y(s)}{X(s)} = \frac{sR_{shunt}C_{off}}{1+sR_{shunt}(C_{off}+C_{out})} = \frac{sR_{shunt}C_{off}}{1+s\tau}, \quad (14)$$

where $\tau = R_{shunt}(C_{off} + C_{out})$ is the time constant. Note that the input signal $x(t)$ is the high-voltage square wave coming from the TX side. $x(t)$ can be expressed as

$$x(t) = \begin{cases} 0, t < 0 & (15) \\ mt, 0 \le t < t_r & (16) \\ \frac{A}{t_r}, t_r \le t < t_r + T_{on} & (17) \\ -m(t - t_r - T_{on} - t_f), t_r + T_{on} \le t < t_r + T_{on} + t_f & (18) \\ 0, t_r + T_{on} + t_f \le t < T_{period} & (19) \end{cases}$$

where A is the amplitude, t_r and t_f are rise and fall times respectively, T_{on} is the on-time, and T_{period} is the period of the TX high-voltage wave. The proposed first-order *CRC* circuit's output response to $x(t)$ will be analysed individually.

The response to (15) is 0. The response $y(t)$ to the rising edge (16) in the time domain is given by

$$y(t) = \frac{AR_{shunt}C_{off}}{t_r}\left\{u(t) - u(t)e^{-t/\tau}\right\}, \quad (20)$$

where $u(t)$ is the unit step function. Equation (20) reveals important insights into off-isolation. Firstly, off-isolation improves with a smaller $R_{shunt}C_{off}$ product, which can be accomplished by increasing the dimensions of M_2 and/or decreasing the dimensions of M_3. However, decreasing the dimensions of M_3 will increase R_{on}, and a trade-off must be made. Secondly, an unexpected insight from (20) is that off-isolation is dependent on the *slew rate* of the incoming high-voltage square wave, and not on frequency as is common in RF systems. From an off-isolation perspective, it is beneficial for the high-voltage TX wave to have a smaller slew rate. Equation (20) shows that the amplitude of the coupled spike due to the high voltage rising edge is $AR_{shunt}C_{off}/t_r$. By substituting $A = 15$ V, $R_{shunt} = 64\,\Omega$, $C_{off} = 125$ fF, $t_r = 20$ ns into (20), the result is 6 mV, which is very close to the post-layout simulated value of 5.9 mV as seen in Fig. 9.

The response to (17) in the time domain is given by

$$y(t) = \frac{AR_{shunt}C_{off}}{\tau}e^{\frac{-(t-t_r)}{\tau}}, \quad (21)$$

which describes an exponential decay from the peak value. As seen in Fig. 9, the predicted exponential decay follows the simulated waveform closely. The decay rate and to a large extent the "shape" of the coupled spike, are mainly determined by the ratio of t_r to τ, which can be tuned easily. The responses to (18) and (19) follow (15) and (16) analogously and will not be elaborated further.

E. Differential-Mode Analysis

The proposed T/R switch's differential-mode response is analyzed separately according to its RX and TX sides. On the RX side (on-mode), the threshold voltage mismatch (ΔV_{TH}) in the DMOS transistors (M_{3a} and M_{3b}, Fig. 4) is identified as the leading cause of differential performance degradation. This is because the layout strategy prioritizes minimal coupling/crosstalk over matching intentionally, which means that there is a greater risk of threshold voltage mismatch. Additional information on the layout strategy is explained further in Section IV. ΔV_{TH} manifests itself as a R_{on} mismatch (ΔR_{on}) between M_{3a} and M_{3b}. As a result of ΔV_{TH}, the degradation in differential performance is reflected in a lower common-mode rejection and finite, non-zero even-order distortion.

Assume that the input-output relationship through the differential RX switch in the Laplace domain is:

$$V_{OUT,P}(s) = \frac{V_{IN,CM}(s) + V_{IN,DIFF}(s)}{1 + sR_{on}C_{out}}, \quad (22)$$

$$V_{OUT,N}(s) = \frac{V_{IN,CM}(s) - V_{IN,DIFF}(s)}{1 + s(R_{on} + \Delta R_{on})C_{out}}, \quad (23)$$

which use a first-order *RC* approximation that shows explicitly the dependence on ΔR_{on}. The differential output voltage $V_{OUT,DIFF}(s) = V_{OUT,P}(s) - V_{OUT,N}(s)$ is:

$$V_{OUT,DIFF}(s) = \frac{V_{IN,DIFF}(s)\left(2 + sC_{out}(2R_{on} + \Delta R_{on})\right)}{(1 + sR_{on}C_{out})(1 + s(R_{on} + \Delta R_{on})C_{out})} + \frac{V_{IN,CM}(s)(sC_{out}\Delta R_{on})}{(1 + sR_{on}C_{out})(1 + s(R_{on} + \Delta R_{on})C_{out})}, \quad (24)$$

which shows the differential output voltage as a superposition of differential (desired) and common-mode (undesired) components. The common-mode rejection ratio (CMRR) is given by the ratio of the differential gain to the common-mode to differential-mode conversion. The CMRR is derived as a function of complex frequency s in (25).

$$CMRR(s) = \frac{2 + sC_{out}(2R_{on} + \Delta R_{on})}{2sC_{out}\Delta R_{on}}. \quad (25)$$

By taking asymptotic approximations, it can be seen from (25) that at low frequencies, CMRR is very large (approaches infinity asymptotically), whereas at very high frequencies, CMRR decreases to $(2R_{on} + \Delta R_{on})/2\Delta R_{on}$. It is beneficial to reduce ΔV_{TH} for a better CMRR. Thus, M_{3a} and M_{3b} are sized to a large area to reduce ΔV_{TH} without relying on layout techniques (common-centroiding). The estimated ΔV_{TH} is 0.1%. Comprehensive post-layout simulations show that the CMRR of the proposed switch is very large at the intended operating frequency, which validates its ability to support differential operation.

On the other hand, the TX side's differential-mode response is much less dependent on ΔV_{TH}, given its large transistor area. Its differential-mode response is largely determined by the

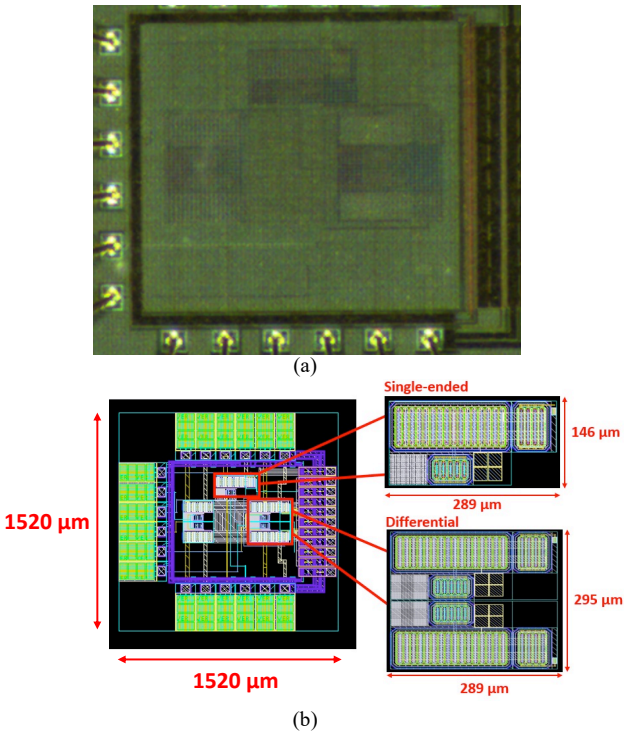


Fig. 10. (a) Chip microphotograph. (b) Complete chip-level layout, with zoomed-in views of the single-ended and differential switches. Unlabeled blocks are test structures.

relative timing misalignment between the positive and negative TX high-voltage pulses. Comprehensive simulations performed at the slowest corner have shown that the relative timing misalignment is of the order of a few nanoseconds. The impact of such a small timing misalignment on the differential-mode response can be safely neglected, considering that the intended TX operating period is much larger at 1 µs.

IV. Measured Results

The T/R switch circuit was implemented in a 1P6M (one polysilicon layer, 6 metal layers), 0.18 µm HV BCD technology. It was chosen because it offers a range of DMOS transistors with different voltage options. The die microphotograph is shown in Fig. 10(a). The single-ended half-circuit and differential circuit occupy 289 µm × 146 µm and 289 µm × 295 µm respectively as illustrated in Fig. 10(b).

An important trade-off to consider in the layout of the differential switch is between transistor matching and cross-coupling. For instance, to achieve good transistor matching, the transistors are placed very closely to each other using techniques such as inter-digitisation and common-centroiding. However, a close proximity between transistors will inevitably lead to an increase in cross-coupling and a worsening in off-isolation. Mismatch between transistors is generally manifested as a dc offset, which is not signal-dependent and can be relatively simple to mitigate. On the other hand, cross-coupling is signal-dependent and introduces distortion in the output signal, which is a much more difficult error to rectify. Therefore, the layout strategy of the proposed switch prioritises low cross-coupling over transistor matching. To that end, the low-voltage RX transistor M_2 is placed far away from the high-voltage TX transistor M_4 with M_3 in between for further

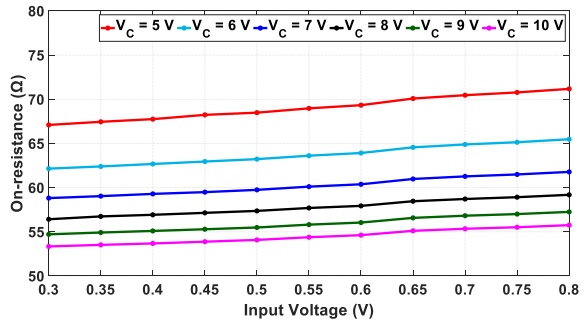


Fig. 11. R_{on} plotted against input voltage for different gate control voltages.

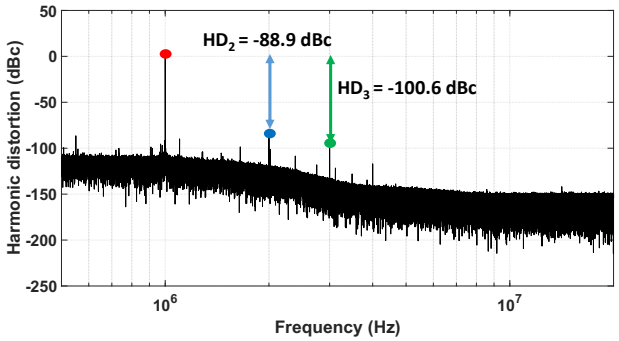


Fig. 12. Harmonic distortion for the RX output (differential). Input signal is a 100 mV_{pp}, 1 MHz sinewave.

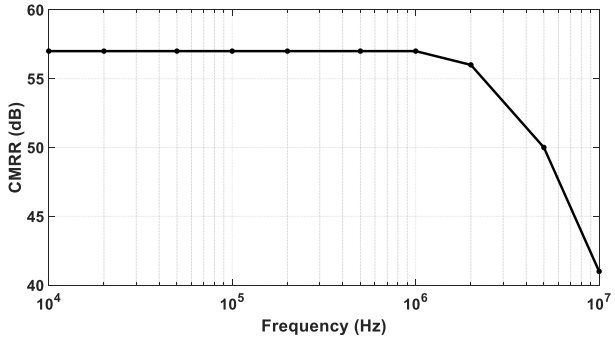


Fig. 13. CMRR plotted against frequency.

shielding. In addition, the wiring between TX and RX is kept minimal and substrate vias are placed abundantly where possible to create a low-impedance path to ground for any stray pick-up. Techniques for matching layout such as common-centroid and dummy devices were not adopted intentionally. The proposed differential switch was laid out to maximise symmetry along a horizontal axis.

Fig. 11 shows R_{on} of M_3 plotted against input voltage for varying control voltages. For V_C set to 5 V and an input voltage ranging from 0.3 V to 0.8 V, R_{on} only changes from 67 Ω to 71 Ω. This means that R_{on} is relatively flat, which is desirable for a T/R switch. R_{on} flatness improves with an increasing V_C. Fig. 12 illustrates the harmonic distortion of the RX output (differential), which shows excellent HD_2 and HD_3 performance. Nevertheless, the measured HD_2 and HD_3 results are worse than that predicted in Section III because the presence of noise and other nonlinearities are not included in the modelling. The total harmonic distortion (THD) is −88.6 dBc.

Fig. 12 shows that HD_2 is poorer than HD_3. Due to systematic and random mismatch in the switch circuit and possible imbalance in the differential signal generator instrument, the differential cancelling of even-order harmonics will not be perfect in practice. Even-order harmonics will persist, albeit attenuated greatly. Thus, it is likely that imperfect differential cancelling of a relatively strong second-order harmonic resulted in a final HD_2 that is worse than HD_3.

Fig. 13 shows the CMRR plotted against frequency. The CMRR rolls off at higher frequencies. However, the CMRR is sufficiently high at 57 dB up to the intended frequency of operation.

Fig. 14 shows the differential high-voltage pulses being transferred to the transducer port and a very small signal being coupled through to the RX output port. This shows that the proposed circuit is effective in acting as an SPDT switch. The transducer is modelled as a 20-pF capacitive load. Note that the single-ended voltage swing in Fig. 14(a) is 8.5 V instead of 15 V. This discrepancy is due to laboratory instrument limitations. The maximum voltage output from the signal generator (Keysight 33600A) is limited to 10 V_{pp}. The voltage output from the signal generator is buffered by a commercial buffer (Texas Instruments BUF634AIDR) before being sent to the chip's input. This buffer reduces the voltage swing slightly. The dotted line in Fig. 14(a) represents the output of this commercial buffer, i.e. the input signal directly connected to the chip. It can be seen from Figs. 14(a) and (b) that the chip input and output high-voltage signals match very closely with minimal delay, validating the TX operation in both differential and single-ended modes. The measured amplitude of the coupled spikes at the RX output port [Fig. 14(c)] is in close agreement with that predicted by the *CRC* model and post-layout simulations in Section III.

Fig. 15. shows the off-isolation of the T/R switch plotted against high-voltage input rise time for different frequencies. To measure the off-isolation, the RX side is turned off and a high-voltage square wave is applied to the TX side (turned on). The coupled output signal at the RX port is measured. Subsequently, the off-isolation is obtained from the measured peak-to-peak values as in (26).

$$\mathrm{ISO_{off}} = 20\log_{10}\frac{V_{outRX,pp}}{V_{inTX,pp}}. \qquad (26)$$

As predicted in Section III, increasing the rise time (decreasing slew rate), improves the off-isolation. Fig. 15 supports the argument made in Section III that in the case of ultrasound T/R switches working with high-voltage square waves, the slew rate of the incoming high-voltage square wave affects the off-isolation to a much greater extent than its frequency.

Table I summarises the performance of the proposed circuit and compares it to the state-of-the-art. The proposed switch circuit is suitable for low-power designs because it does not consume any static power, unlike the designs in [2], [3], and [12]. The area comparison is rather subjective and arbitrary because the occupied area is directly influenced by the chosen technology. Older process nodes and technologies that use junction isolation for high-voltage isolation (this work) tend to occupy a larger area than high-voltage SOI technology used in [42]. Furthermore, it is inevitable for a differential design to take up more area than a single-ended design. A more balanced comparison is the number of high-voltage transistors used in the design as a proxy for area. It can be seen from Table I that the proposed circuit is comparable to the state-of-the-art in this regard.

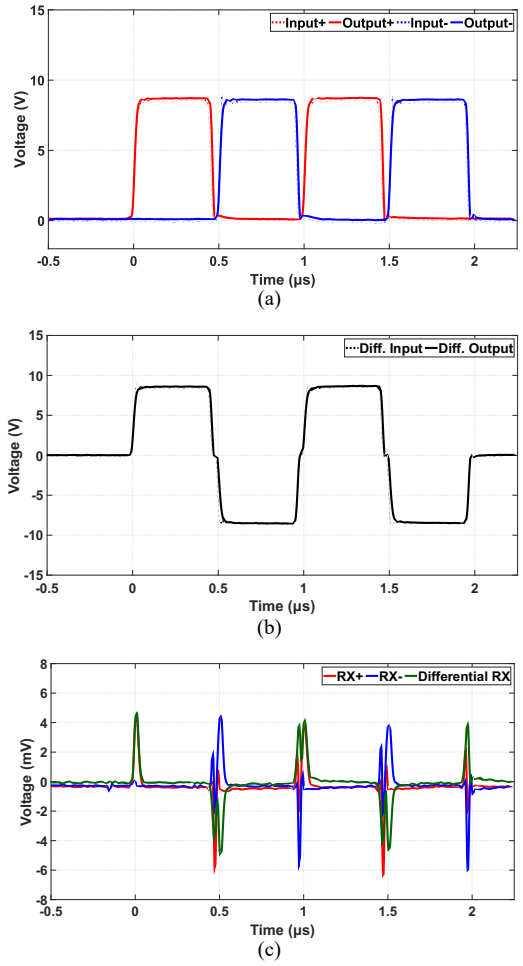


Fig. 14. Operation of the switch in TX mode. (a) High voltage waveforms at the TX input and output ports. (b) Differential high voltage waveforms at the TX input and output ports. (c) Very small voltage spikes coupled to the RX output ports.

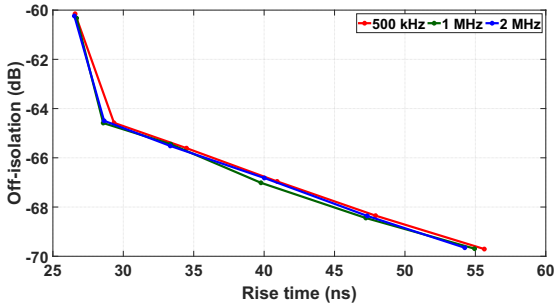


Fig. 15. Off-isolation plotted against rise time for different high-voltage input frequencies. Fall time is nominally equal to rise time. The high-voltage input amplitude is 8.5 V for all cases.

TABLE I. COMPARISON WITH STATE-OF-THE-ART DESIGNS

	This work	[8]	[12]	[6]	[7]	[2]	[3]	[5]	[43]
Technology	0.18 µm HV BCD	0.18 µm HV CMOS	0.18 µm HV SOI	0.35 µm HV CMOS	LV + 200 V HV CMOS	0.18 µm HV CMOS	0.35 µm HV CMOS	65 nm SOI-CMOS	65 nm SOI-CMOS
R_{on} (Ω)	67	N.A.	290	180	N.A.	100	700	2.32	2
Off-isolation (dB)	−63[b]	−53	−64@10 MHz	−17.52	N.A.	−92@10 kHz	−34	22@100 MHz	17@1 GHz
FoM	0.31[a], 0.16[b]	N.A.	0.074	0.019	N.A.	0.092	0.0054	N.A.	N.A.
Area/ch (μm^2)	42190[a], 85260[b]	5525	9920	48320	70312	18000	260000	N.A.	N.A.
Area×R_{on} ($mm^2.\Omega$)	2.70[a], 5.46[b]	N.A.	2.88	8.70	N.A.	1.8	182	N.A.	N.A.
Number of HV MOS/ch	3[a], 6[b]	17	3	⩾ 5	5	10	9	0[c]	0[c]
Voltage swing (V_{pp})	17[b]	40	138	10	200	20	120	24	20
Switching time (ns)	28	N.A.	N.A.	260/280	N.A.	80	4000	3200	10000
Static current/ch (µA)	0	0	0 (TX) 2.42 (RX)	N.A.	N.A.	0.3	90	N.A.	N.A.
Type of switch	Differential, SPDT	Single-ended, SPST	Single-ended, SPST	Single-ended, SPST	Single-ended, SPST	Single-ended, SPST	Single-ended, SPST	Single-ended, SPST	Single-ended, SPST
Application	Ultrasound	Ultrasound	Ultrasound	Ultrasound	Ultrasound	Neural stimulator	Neural stimulator	RF/analog	RF/analog

[a]Single-ended.
[b]Differential.
[c]Standard CMOS transistors were stacked to support high voltage.

The two most important specifications for a T/R switch in ultrasound applications are its R_{on}, and off-isolation (ISO_{off}). These two specifications are integral to the function of the switch, and it is logical to construct a figure-of-merit (FoM) from these two specifications. In this paper, a simple but insightful FoM to compare ultrasound T/R switches is proposed and given by (27), where n is the number of high-voltage transistors, a fairer proxy for area comparison.

$$\text{FoM} = \frac{|\text{ISO}_{\text{off}}(\text{dB})|}{n \times \text{R}_{\text{on}}(\Omega)}. \tag{27}$$

Since the ideal T/R switch should have large off-isolation, low R_{on}, and small n, a higher FoM is desirable. The proposed switch achieves an FoM of 0.16, which is a 74% improvement over the state-of-the-art [2].

V. CONCLUSION

This paper presented a high-voltage, differential T/R SPDT switch, designed in a 0.18 µm HV BCD technology for PMUT-based ultrasound hand gesture recognition applications. The T/R switch is also suitable for applications that can employ differential ultrasound transducers such as robot vision in dark conditions [16], range finding [44], and drone navigation [45]. To the best of the authors' knowledge, this is the first differential SPDT T/R switch reported for ultrasound systems. The need and benefits of a differential ultrasound T/R switch were elaborated. The T/R switch incorporated a bootstrapping technique to pass high-voltage pulses and a shunt branch for improved isolation. The reliability of this switch, i.e. safe operating condition had been addressed. A comprehensive analysis into the design and optimisation of this T/R switch was carried out. The hyperbolic tangent model for the triode region had been extended to predict HD_3 for optimizing the RX circuit design. A method to examine the rise/fall time for optimizing the TX circuit was introduced. A *CRC* equivalent circuit was developed to model off-isolation effectively. It was found that off-isolation is dependent on the slew rate of the incoming high-voltage square wave, and not on operation frequency as commonly assumed. The CMRR was derived to characterize the differential performance. Threshold voltage mismatch in the switching transistors and the relative timing misalignment between the positive and negative transmit high-voltage pulses were found to be the leading causes of differential performance degradation in RX and TX operations respectively. Measured results validated the differential operation of the switch. The switch circuit showed 67 Ω on-resistance and −63 dB off-isolation while employing a small number of high-voltage transistors. The switch achieved an FoM with 74% improvement over the state-of-the-art.

ACKNOWLEDGMENT

The authors would like to thank Mr. Martin Scott and Mr. Noordeen Marikkar for the support offered during chip testing.

REFERENCES

[1] S. Dai, R. W. Knepper and M. N. Horenstein, "A 300-V LDMOS analog-multiplexed driver for MEMS devices," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 62, no. 12, pp. 2806-2816, Dec. 2015.

[2] A. Safarpour, F. Dehnavi, M. Saberi, R. Lotfi and W. A. Serdijn, "Speed-power improvement in high-voltage switches employed in multielectrode arrays," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 7, pp. 3139-3143, July 2022.

[3] D. Osipov et al., "Current driver with read-out HV protection for neural stimulation," in *Proc. IEEE Nordic Circuits Syst. Conf. (NORCAS)*, 2016, pp. 1-4.

[4] D. Y. Aksin and I. Ozkaya, "25V sampling switch for power management data converters in 0.35μm CMOS with DNMOS," in *2009 Proc. IEEE Eur. Solid State Circuits Conf.*, 2009, pp. 136-139.

[5] V. Solomko, S. Syroiezhin and R. Weigel, "High-voltage analog switch inspired by stacked MOSFET-based RF switches," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 11, pp. 4008-4012, Nov. 2023.

[6] H. Jung et al., "CMOS high-voltage analog 1–64 multiplexer/demultiplexer for integrated ultrasound guided breast needle biopsy," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 65, no. 8, pp. 1334-1345, Aug. 2018.

[7] G. Ricotti and V. Bottarel, "HV floating switch matrix with parachute safety driving for 3D echography systems," in *Proc. IEEE 44th Eur. Solid State Circuits Conf.*, 2018, pp. 271-273.

[8] S.-J. Jung, S.-K. Hong, and O.-K. Kwon, "Area-efficient high-voltage switch using floating control circuit for 3D ultrasound imaging systems," *Electron. Lett*., vol. 50, no. 25, pp. 1900–1902, 2014.

[9] M. Tan et al., "A front-end ASIC with high-voltage transmit switching and receive digitization for 3-D forward-looking intravascular ultrasound imaging," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2284-2297, Aug. 2018.

[10] E. Kang et al., "A reconfigurable ultrasound transceiver ASIC with 24 × 40 elements for 3-D carotid artery imaging," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 2065-2075, July 2018.

[11] F. Yamashita, J. Aizawa and H. Honda, "A new compact, low on resistance and high off isolation high voltage analog switch IC without using high voltage power supplies for ultrasound imaging system," in *Proc. 28th Int. Symp. Power Semiconductor Devices ICs (ISPD)*, Jun. 2016, pp. 415-418.

[12] S. Kajiyama et al., "T/R switch composed of three HV-MOSFETs with 12.1-μW consumption that enables per-channel self-loopback AC tests and −18.1-dB switching noise suppression for 3-D ultrasound imaging with 3072-ch transceiver," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 2, pp. 153-165, Feb. 2022.

[13] L. Novaresi, P. Malcovati, A. Mazzanti and E. Bonizzoni, "A bipolar 3-level high-voltage pulser for highly integrated ultrasound imaging systems," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 70, no. 5, pp. 1709-1713, May 2023.

[14] Y. Zhang and A. Demosthenous, "Integrated circuits for medical ultrasound applications: imaging and beyond," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 5, pp. 838-858, Oct. 2021.

[15] Y. Zhang et al., "A four-channel analog front-end ASIC for wearable a-mode ultrasound hand kinematic tracking applications," in *Proc. IEEE Biomed. Circuits Syst. Conf*., 2023, pp. 1-4, 2023.

[16] H. Wu et al., "An ultrasound ASIC with universal energy recycling for >7-m all-weather metamorphic robotic vision," *IEEE J. Solid-State Circuits*, vol. 57, no. 10, pp. 3036-3047, Oct. 2022.

[17] J. Lee et al., "A 36-channel auto-calibrated front-end ASIC for a pMUT-based miniaturized 3-D ultrasound system," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1910-1923, Jun. 2021.

[18] X. Yu, Y. Wang, F. Ye and J. Ren, "Low-noise low-power ultrasound AFE with continuous TGC built in both TIA and beamformer," *IEEE Trans. Biomed. Circuits Syst*., vol. 17, no. 5, pp. 1062-1073, Oct. 2023.

[19] X. Yu et al., "28-nm CMOS ultrasound AFE with split attenuation for optimizing gain-range, noise, and area," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 70, no. 12, pp. 4742-4754, Dec. 2023.

[20] TX-810: 8-channel, programmable T/R switch for ultrasound. Accessed Jan. 9, 2024. [Online]. Available: https://www.ti.com/lit/ds/symlink/tx810.pdf?ts=1704562703580&ref_url=https%253A%252F%252Fwww.google.com%252F.

[21] I. O. Wygant et al., "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 55, no. 2, pp. 327-342, Feb. 2008.

[22] C. Chen et al., "A pitch-matched front-end ASIC with integrated subarray beamforming ADC for miniature 3-D ultrasound probes," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3050-3064, Nov. 2018.

[23] Y. M. Hopf et al., "A pitch-matched high-frame-rate ultrasound imaging ASIC for catheter-based 3-D probes," *IEEE J. Solid-State Circuits*, vol. 59, no. 2, pp. 476-491, Feb. 2024.

[24] I. O. Wygant et al., "An integrated circuit with transmit beamforming flip-chip bonded to a 2-D CMUT array for 3-D ultrasound imaging," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 56, no. 10, pp. 2145-2156, Oct. 2009.

[25] G. Jung et al., "A reduced-wire ICE catheter ASIC with Tx beamforming and Rx time-division multiplexing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 6, pp. 1246-1255, Dec. 2018.

[26] M. W. Rashid, C. Tekes, M. Ghovanloo and F. L. Degertekin, "Design of frequency-division multiplexing front-end receiver electronics for CMUT-on-CMOS based intracardiac echocardiography," in *Proc. IEEE Int. Ultrason. Symp.*, 2014, pp. 1540-1543.

[27] Y. M. Hopf et al., "A compact integrated high-voltage pulser insensitive to supply transients for 3-D miniature ultrasound probes," *IEEE Solid-State Circuits Lett.*, vol. 5, pp. 166-169, 2022.

[28] Qilong Liu, Chao Chen, Z. -y. Chang, C. Prins and M. A. P. Pertijs, "A mixed-signal multiplexing system for cable-count reduction in ultrasound probes," in *Proc. IEEE Int. Ultrason. Symp*, 2015, pp. 1-4.

[29] C. Chen, Z. Chen, Z. -y. Chang and M. A. P. Pertijs, "A compact 0.135-mW/channel LNA array for piezoelectric ultrasound transducers," in *Proc. IEEE 41st Eur. Solid State Circuits Conf.*, 2015, pp. 404-407.

[30] S. Akhbari, F. Sammoura, B. Eovino, C. Yang and L. Lin, "Bimorph piezoelectric micromachined ultrasonic transducers," *J. Microelectromech. Syst.*, vol. 25, no. 2, pp. 326-336, April 2016.

[31] Z. Shao, S. Pala, Y. Peng and L. Lin, "Bimorph pinned piezoelectric micromachined ultrasonic transducers for space imaging applications," *J. Microelectromech. Syst.*, vol. 30, no. 4, pp. 650-658, Aug. 2021.

[32] Y. Zhang, D. Jiang and A. Demosthenous, "A differential SPDT T/R switch for PMUT biomedical ultrasound systems," *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, Singapore, 2024, pp. 1-4.

[33] Y. Zhang et al., "Live demonstration: a wearable eight-channel a-mode ultrasound system for hand gesture recognition and interactive gaming," *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, Singapore, 2024, pp. 1-1.

[34] M. Sautto et al., "A CMUT transceiver front-end with 100-V TX driver and 1-mW low-noise capacitive feedback RX amplifier in BCD-SOI technology," in *Proc. IEEE 40th Eur. Solid State Circuits Conf.*, 2014, pp. 407-410.

[35] Q. Li and Y. P. Zhang, "CMOS T/R switch design: towards ultra-wideband and higher frequency," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 563-570, March 2007.

[36] L. Chen, L. Chen, Z. Ge, Y. Sun, T. J. Hamilton and X. Zhu, "A 90-GHz asymmetrical single-pole double-throw switch with >19.5-dBm 1-dB compression point in transmission mode using 55-nm bulk CMOS technology," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 68, no. 11, pp. 4616-4625, Nov. 2021.

[37] T. Iizuka, T. Ito and A. A. Abidi, "Comprehensive analysis of distortion in the passive FET sample-and-hold circuit," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 65, no. 4, pp. 1157-1173, April 2018.

[38] C. W. Tang and K. Y. Tong, "A compact large signal model of LDMOS," *Solid-State Electron*., vol. 46, no. 12, pp. 2111–2115, 2002.

[39] Y. Oritsuki *et al*., "HiSIM-HV: A compact model for simulation of high-voltage MOSFET circuits," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2671-2678, Oct. 2010.

[40] Paul, Clayton R., Robert C. Scully, and Mark A. Steffka, *Introduction to electromagnetic compatibility*, 3rd ed., Hoboken, NJ, USA: John Wiley & Sons, 2022.

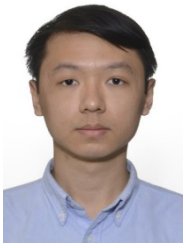
[41] Hsia C, Hsiao Y-C and Huang Y-C, "A single-chip high-voltage integrated actuator for biomedical ultrasound scanners," *Sensors*, vol. 19, no.23, 2019.

[42] M. Tan et al., "An integrated programmable high-voltage bipolar pulser with embedded transmit/receive switch for miniature ultrasound probes," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 79-82, Sept. 2019.

[43] S. Syroiezhin, R. Weigel and V. Solomko, "High-voltage MOSFET-based stacked RF switch with extended bandwidth down to DC," *IEEE Solid-State Circuits Lett*., vol. 6, pp. 129-132, 2023.

[44] G. Berkol, P. G. M. Baltus, P. J. A. Harpe and E. Cantatore, "A 1.25 μJ per measurement ultrasound rangefinder system in 65 nm CMOS for explorations with a swarm of sensor nodes," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 68, no. 4, pp. 1409-1420, April 2021.

[45] J. Guo et al., "A 0.5° - resolution hybrid dual-band ultrasound imaging SoC for UAV applications," in *Proc. IEEE Int. Solid-State Circuits Conf*., 2024, pp. 108-110.



Yaohua Zhang (Student Member, IEEE) received the MEng degree in Electrical and Electronic Engineering from Imperial College London, UK with First Class Honours in 2020. He is a Research Assistant in the Bioelectronics Group, Department of Electronic and Electrical Engineering, University College London, UK, and he is also pursuing a PhD in the same department. He was awarded the IEEE Circuits and Systems Society 2024 Pre-Doctoral Grant and a Best Live Demo award at IEEE ISCAS 2024. His research is concerned primarily with ultrasound integrated circuit design for neuroprosthetics. His research interests include analog/biomedical IC design, mixed-signal IC design, bioelectronics, neuromorphic circuits, computer-aided design of integrated circuits, signal processing and ultrasound transducers.

Dai Jiang (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees from Beihang Unviersity (formerly the Beijing University of Aeronautics and Astronautics), China, in 1998 and 2001, respectively, and the Ph.D. degree from University College London (UCL), U.K., in 2009. He is currently a lecturer with the Department of Electronic and Electrical Engineering at UCL. His research interests include CMOS analog and mixed-signal integrated circuit design for biomedical applications. He is an Associate Editor of the IEEE Transactions on Circuits and Systems II: Express Briefs, and a member of the Biomedical and Life Science Circuits and Systems Technical Committee of the IEEE Circuits and Systems Society.

Andreas Demosthenous (Fellow, IEEE) received the B.Eng. degree in electrical and electronic engineering from the University of Leicester, Leicester, U.K., the M.Sc. degree in telecommunications technology from Aston University, Birmingham, U.K., and the Ph.D. degree in electronic and electrical engineering from University College London (UCL), London, U.K., in 1992, 1994, and 1998, respectively. He is currently a Professor with the Department of Electronic and Electrical Engineering, UCL, where he leads the Bioelectronics Group. He has made outstanding contributions to improving safety and performance in integrated circuit design for active medical devices, such as spinal cord and brain stimulators. He has numerous collaborations for cross-disciplinary research, both within the U.K. and internationally. He has authored over 350 articles in journals and international conference proceedings, several book chapters, and holds several patents. His research interests include analog and mixed-signal integrated circuits for biomedical, sensor, and signal processing applications.

Dr Demosthenous is a fellow of the Institution of Engineering and Technology (IET), a fellow of the European Alliance for Medical and Biological Engineering Sciences (EAMBES), and a Chartered Engineer (CEng). He was a co-recipient of a number of best paper awards and has graduated many Ph.D. students. He was an Associate Editor, from 2006 to 2007 and the Deputy Editor-in-Chief, from 2014 to 2015 of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS; and an Associate Editor, from 2008 to 2009 and the Editor-in-Chief, from 2016 to 2019 of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS. He was an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS from 2013 to 2023, and currently serves on its steering committee. He serves on the Editorial Boards of Physiological Measurement and Neuroelectronics journals. He has served on the Technical Programme Committee of numerous conferences including ISCAS, BIOCAS, ICECS, ESSCIRC and NER. He was the Chair of the IEEE Circuits and Systems Society (CASS) Fellows Evaluation Committee, 2022-2023 and has served on many CASS committees including the Board of Editors, John Choma Education Award Evaluation Committee, and Mac Van Valkenburg Award Evaluation Committee. He is the Chair of the UK and Ireland IEEE CASS Chapter and the General Co-Chair of ISCAS 2025.