A 199 µW, 82.9% Efficiency Current Driver with Active Common-Mode Reduction for Impedance-Based Tactile Sensors

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***Abstract*—This paper presents a differential current driver based on a current feedback structure, designed to drive hydrogel sensors. It achieves low power consumption, low common-mode signal on the load, and high current efficiency. The use of a negative unit gain buffer reduces the common-mode signal on the load arising from process variations. The current driver was designed in a 65-nm CMOS technology with a 3.3 V supply. Simulation results demonstrate a THD of 0.4% at 125 kHz, for 40 μA_{p-p} output current. The common-mode voltage on the load is reduced by 98.96% compared to a conventional topology using two independent drivers. The total current consumption is 60.3 µA, resulting in a current efficiency of 82.9%. The simulated output impedance is 2.76 MΩ at 125 kHz and 1.47 MΩ at 300 kHz.**

Keywords—Current driver, common-mode reduction, current feedback, impedance measurement, low power.

I. Introduction

Over the last two decades, there has been significant progress and increased development of tactile sensors, that are frequently composed of hydrogel-based materials [1]. Hydrogel sensors are soft and resilient. They efficiently contact human skin, making them attractive for artificial intelligence, wearable devices, and robotic skin applications. Hydrogel-based sensors can detect various physical parameters including humidity, temperature, biochemical reactions, and pressure, among which the pressure is measured by the impedance of hydrogel [2]. A typical hydrogel sensor system is illustrated in Fig. 1(a), where an impedance measurement system injects an ac current. The readout circuit measures the voltage developed on different electrode positions via a switch network to extract the desired physiological information.

Fig. 1(b) shows the basic circuit where a differential current driver injects a current, and a differential amplifier measures the generated voltage. The performance of the differential current driver is critical in determining the system's measurement accuracy. Differential drivers can be implemented with two independent current drivers, such as the differential difference transconductance amplifier (DDTA) topology reported in [4]-[6]. Another popular design is the transconductance and transimpedance implementations reported in [7]-[10].

The challenge in implementing a differential current driver is the matching of the currents as shown in Fig. 1(b). Any unbalanced current ΔI, due to mismatch and process variations, results in an ac common-mode voltage on the load, which must be accommodated by the common-mode rejection ratio (CMRR) of the instrumentation amplifier (IA). The existence of switching networks between the current driver and the IA,

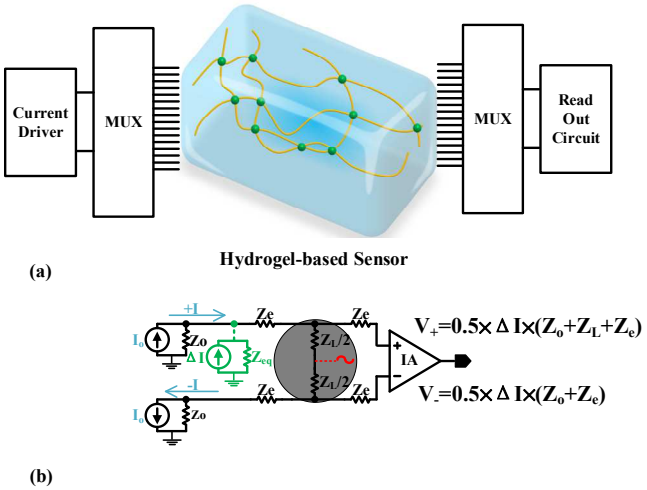

Fig. 1. (a) Illustration of an impedance measurement system for hydrogel sensor. (b) Differential current driver with a ΔI mismatch current.

as shown in Fig. 1(a), causes further imbalance and increased common mode voltages.

In addition, a hydrogel-based tactile sensor has a high load impedance of about 100 kΩ compared to other bio-impedance sensors of about 1 kΩ [3]. Hence, it requires the current driver output resistance to be relatively large to ensure good output current accuracy.

To overcome these challenges, this paper proposes a low power differential driver using a master-slave topology designed in CMOS technology. The design reduces the common-mode voltage while maintaining other important circuit performance parameters. It consumes 199 µW of power from a 3.3V supply, can output a maximum current of 50 μA_{p-p}, and has an output impedance of 2.76 MΩ at 125kHz.

The rest of the paper is organised as follows. Section II presents the current driver structure, and Section III describes the circuit details of its sub-blocks. Section IV shows the simulated results of the current driver. Conclusions are drawn in Section V.

II. System Structure

The proposed current driver with a master-slave topology is shown in Fig. 2. It uses a negative unity gain amplifier, shown by the orange triangle in Fig. 2. Instead of a copy of the master driver to sink the current, it inverts the voltage of the source side at point P, and applies the inverted voltage to the sink side at point Q, ideally eliminating the common-mode signal on the load. This slave inverter provides a current return path that automatically mirrors the master driver.

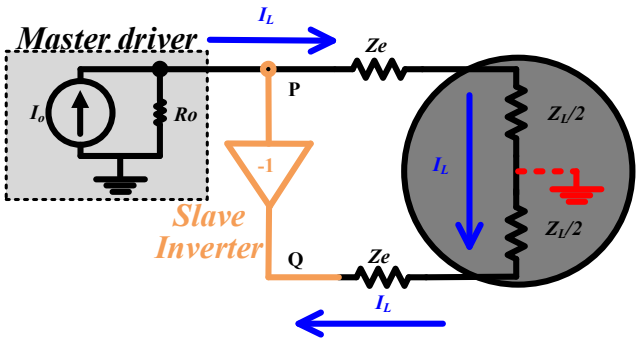

Fig. 2. Proposed current driver with negative unity gain amplifier.

For this topology, the relationship between the current from the master driver, I_o, and the current flowing through the load, I_L, can be expressed as:

$$I_L = \frac{V_+ - A_{CL}V_+}{Z_L} = I_o \frac{R_o}{R_o + \frac{Z_L}{1-A_{CL}}}. \quad (1)$$

The output impedance of the overall current driver is:

$$R_{out} = \frac{V_+ - A_{CL}V_+}{\frac{V_+}{R_o}} = (1-A_{CL})R_o \quad (2)$$

where V_+ is the voltage at node P, Z_L is the load impedance, R_o is the master driver output impedance, I_o is the output current of the master driver, and A_{CL} is the closed-loop gain of the slave inverter. The closer A_{CL} is to -1, the closer the output current delivered to the load is controlled by the master driver (Z_L<<R_o). The overall differential driver output impedance is doubled from R_o when A_{CL}=-1.

For common mode voltage, KCL at point P yields:

$$\frac{V_+ - A_{CL}V_+}{Z_L} + \frac{V_+}{R_o} - I_o = 0. \quad (3)$$

Based on (3), V_+ can be expressed as:

$$V_+ = \frac{I_o R_o Z_L}{Z_L + (1-A_{CL})R_o}. \quad (4)$$

According to (4), the common-mode voltage on the load thus can be written as :

$$V_{cm} = \frac{V_+ + V_-}{2} = \frac{1}{2}\frac{I_o R_o Z_L (1+A_{CL})}{Z_L + (1-A_{CL})R_o}. \quad (5)$$

Hence ideally, when A_{CL}=-1, this topology can actively eliminate the unwanted common mode signal and achieve a fully differential current injection.

III. Circuit Implementation

A. Master Driver Design

The master driver is a DDTA-based topology using a feedback resistor R_f as shown in Fig. 3. The relationship between input and output for the DDTA is:

$$Gm_{DDTA}[(V_{1P} - V_{1N}) - I_O R_f] = I_O. \quad (6)$$

From (6), the transfer function of the master driver is:

$$Gm_M = \frac{I_O}{V_{1P} - V_{1N}} = \frac{Gm_{DDTA}}{1 + Gm_{DDTA} \times R_f} \approx \frac{1}{R_f} \quad (7)$$

where the Gm_M is the closed-loop transconductance of the DDTA when configured as the master driver, Gm_{DDTA} is the open-loop transconductance of the DDTA, and I_O is the current flowing through R_f.

To define Gm_M by $1/R_f$ with 99% accuracy:

$$\frac{Gm_{DDTA}}{1 + Gm_{DDTA} \times R_f} = 0.99\frac{1}{R_f} \quad (8)$$

R_f is set to 1 kΩ, and from (8), the minimum Gm_{DDTA} required is 100mA/V. In a previous design [6], two cascaded differential OTA stages were used to enhance the overall transconductance Gm_M. Its circuit design is complex and power-demanding. In the proposed design, the master driver is in the form of a two-stage rail-to-rail DDTA. The required level of Gm_{DDTA} is achieved by boosting the transconductance of M17 with a high gain folded cascade input stage as shown below:

$$Gm_{DDTA} = gm_{17} \times (gm_n + gm_p) \times \left\{ \frac{1}{\frac{1}{(gm_{14} \times \frac{1}{g_{o13}} \times \frac{1}{g_{o14}})} + \frac{1}{(gm_{15} \times \frac{1}{g_{o15}} \times \frac{1}{g_{o16}})}} \right\} \quad (9)$$

where gm_n, gm_p, and gm_{17} are transconductances of the transistors in two input n-differential pairs, p-differential pairs, and M17 respectively. g_{o13},g_{o14},g_{o15} and g_{o16} are respectively the admittance of M13, M14, M15 and M16. Based on (9), to achieve Gm_{DDTA}=100 mA/V using a gm_{17} smaller than 20 μA/V, the open-loop gain of the folded cascade input stage should be larger than 5 kV/V which is achieved by the cascade stage.

The power is mostly consumed by the input differential pairs and M17 where their transconductance is proportional to the bias current. The input differential pairs operate in the sub-threshold region with a higher width-to-length ratio, leading to lower current consumption for the same transconductance requirement. The current consumption is less than 2 μA for each differential pair, significantly reducing power.

The first stage of the DDTA adopts rail-to-rail input differential pairs. This ensures the transconductance of differential pairs remains constant when the voltage signal across resistor R_f has a large amplitude, which is fed back to the input of DDTA. This results in improved current linearity, hence better THD performance.

B. Slave Inverter Design

The schematic of the slave inverter is shown in the right upper part of Fig. 3. It is based on a differential difference amplifier (DDA) unity gain inverter.

The first stage adopts rail-to-rail input differential pairs and converts four differential inputs into two single-ended outputs for the next stage.

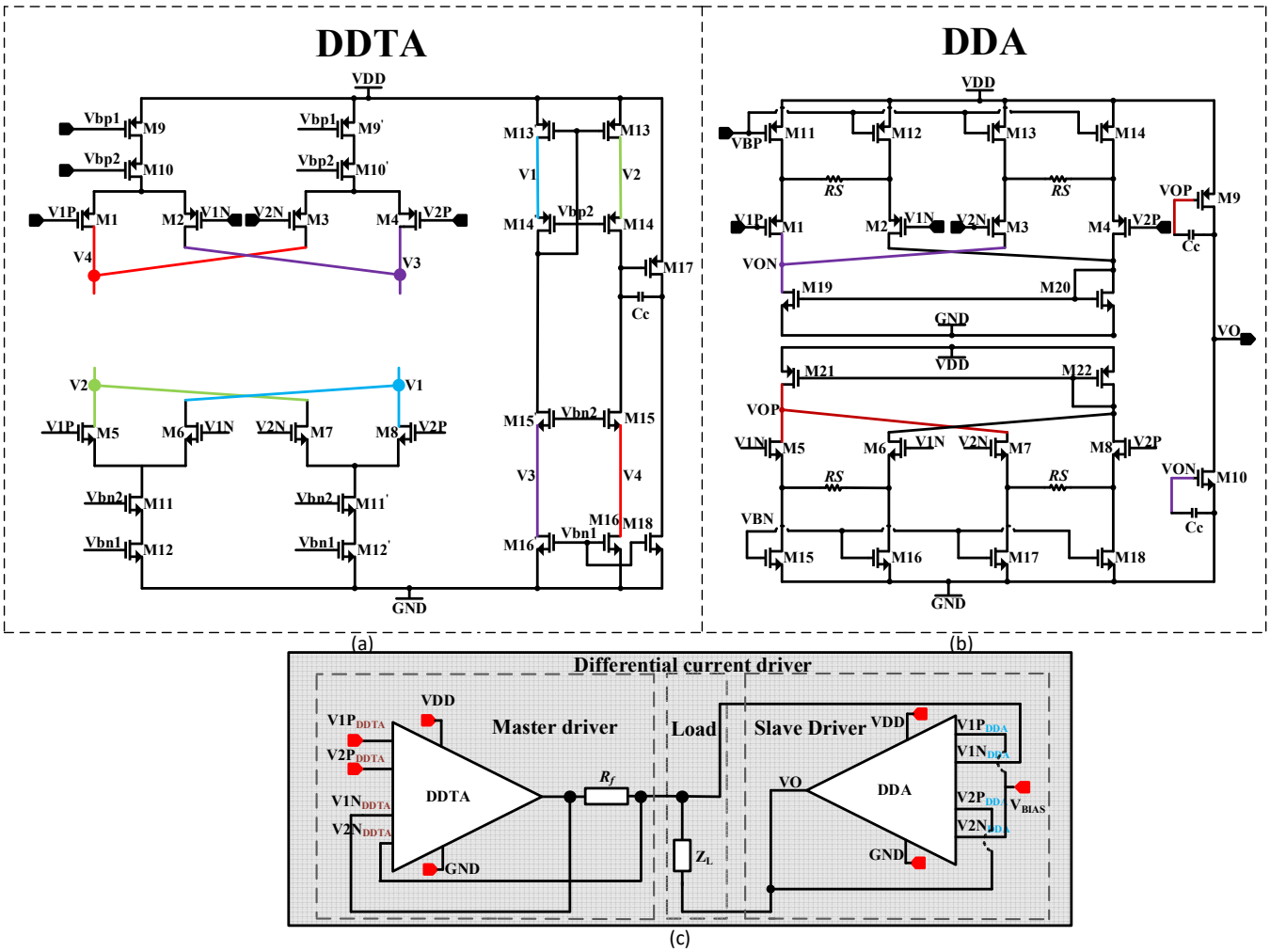

Fig. 3. Detailed transistor level and symbol level circuit of the current driver. (a) Circuit details of DDTA. (b) Transistor level circuit of DDA. (c) Symbol level design of current driver.

Four resistors *RS* are added to the sources of the input differential pairs to enhance the linearity and compensate for the inherent nonlinearity of the second stage, a class-AB amplifier. The transfer function of the circuit is:

$$A_{OL} = \left(\frac{gm_1 \times ro_{19}}{1 + gm_1 \times \frac{RS}{2}} \times gm_{10} + \frac{gm_5 \times ro_{21}}{1 + gm_5 \times \frac{RS}{2}} \times gm_9\right) \times rout \,. \quad (10)$$

The transfer function for a closed-loop DDA is:

$$A_{OL}(V_{1N} + V_O) = V_O \,. \quad (11)$$

From (11):

$$A_{CL} = \frac{V_O}{V_{1N}} = \frac{A_{OL}}{1 - A_{OL}} \approx -1 \quad (12)$$

where A_{OL} is the open-loop gain of the DDA, A_{CL} is the gain of the negative unity gain buffer, gm_1, gm_5, gm_9, gm_{10} refer to the transconductance of M1, M5, M9, M10, ro_{19}, ro_{21} are intrinsic impedances of M19 and M21 respectively, and V_{BIAS} is ac ground.

Based on (1), (2), (5), A_{CL} should be -1 ideally. The implemented DDA has an A_{OL} larger than 8 kV/V; from (12), this leads to more than 99.98% accuracy for the desired A_{CL}.

The class-AB output stage in the DDA provides the sink current. The quiescent current in M9 and M10 is much smaller than that in the output stage in the DDTA, by using a class-AB stage rather than a class-A stage. The quiescent current of the class-AB stage is about one-tenth of the output current of the current driver.

IV. Simulations

The current driver was designed in 65 nm TSMC CMOS process technology with a 3.3 V supply. As shown in Fig. 4, the current driver occupies a layoutarea of 100 µm × 220 µm. The performance of the common-mode reduction circuit was simulated by measuring the common-mode voltage across a 1 kΩ load at 125kHz. The comparison was made between using two identical DDTA master drivers in source and sink configuration and the proposed topology. Monte Carlo results of common-mode signals are shown in Fig. 5. The common-mode signal is reduced from 211 mV_{pp} to 2.2 mV_{pp}, a 98.96% common-mode noise reduction.

The output impedance as a function of frequency is shown in Fig. 6. The current driver has an output impedance of 4 MΩ at 10 kHz, 2.76 MΩ at 125 kHz and 1.47 MΩ at 300 kHz. The Monte Carlo THD performance tested with a 1 kΩ load at 125 kHz with an output current of 40 $\mu A_{p\text{-}p}$ is shown in Fig. 7. The mean THD is 0.4 % and the output impedance was simulated with an output current of 40 $\mu A_{p\text{-}p}$.

Table I summarises the performance of the differential current driver and provides a comparison with the state-of-the-art. The current driver in this paper has a larger output impedance, higher current efficiency and better common-

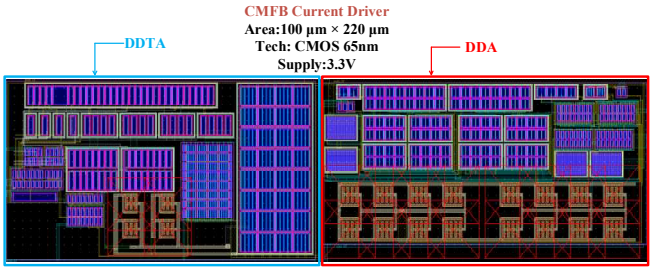

Fig. 4. Layout of the current driver.

mode reduction performance while maintaining other important circuit performance parameters.

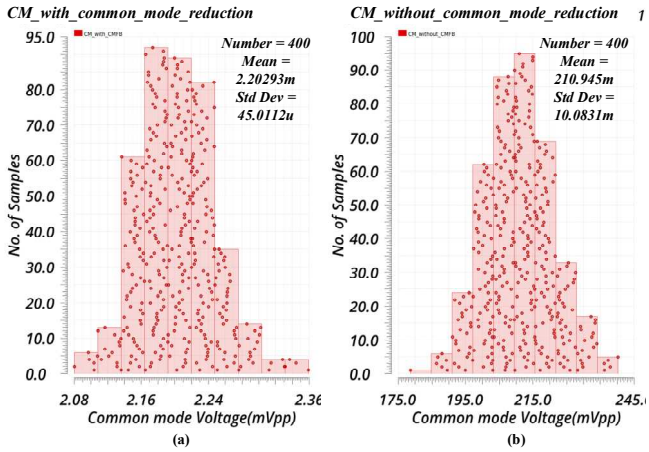

Fig. 5. Monte Carlo simulations. (a) Common-mode voltage with the proposed current driver on 1kΩ load at 125kHz. (b) Common-mode voltage on 1kΩ load at 125kHz using two identical differential master drivers.

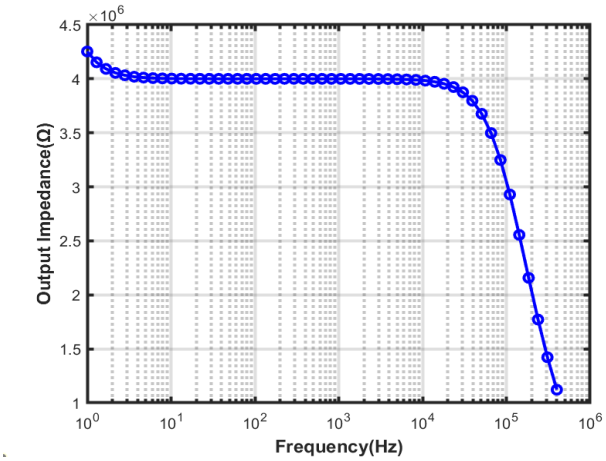

Fig. 6. Output impedance of differential current driver.

TABLE I. COMPARISON OF CURRENT DRIVERS

	[5]	[8]	[9]	[10]	This work
Topology	V-I	V-I	V-I	Current DAC	V-I
CMOS Process	350 nm	65 nm	65 nm	180 nm	65 nm
Supply	±2.5 V	0.5 V	1.2 V	1.2 V	3.3 V
Output Impedance	1MΩ @3MHz	331kΩ @20kHz	1MΩ @1MHz	55kΩ @20kHz	2.76MΩ @125kHz
Power Consumption	15 mW	6.2 µW	2.424 mW	249.4 µW	199 µW
Max Output Current	1.8mA$_{pp}$	2 µA$_{pp}$	400µA$_{pp}$	160µA$_{pp}$	50µA$_{pp}$
THD	0.4% @1mA$_{pp}$	0.088% @2µA$_{pp}$	0.5% @400µA$_{pp}$	<0.4% @160µA$_{pp}$	0.4% @40µA$_{pp}$
Current Efficiency	60%	22.8%	19.8%	76.9%	82.9%
CM Reduction	NO	NO	NO	Manual calibration	Automatic calibration

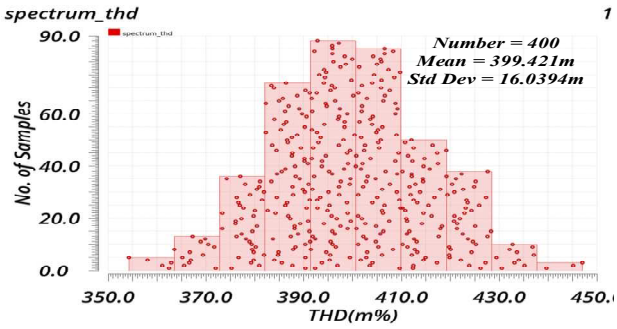

Fig. 7. THD performance of the current driver in Monte Carlo simulations.

V. CONCLUSION

A new fully integrated, high performance current driver has been desined in CMOS 65 nm. The current driver comprises a DDTA and a DDA for hydrogel impedance measurement. Simulations have demonstrated the merits of the current driver; the measured common-mode signal has been reduced by 98.96% using the common-mode reduction technique compared to using two identical differential drivers. At an output current of 40 µA$_{p-p}$, the THD is 0.4%, and the power consumption of the current driver is 199 µW at a maximum output current 50 µA$_{p-p}$.

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