A Current DAC Based Current Generator with Fourth-Order Current-Mode Filter for Electrical Impedance Tomography

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***Abstract*—The current generator is one of the most essential parts in electrical impedance tomography (EIT) systems. State-of-art current generators suffer from the trade-off between current efficiency, linearity, output impedance and well-controlled output current level. To address these challenges, a current DAC based current generator with a fourth-order current-mode filter is proposed. The current generator was designed and simulated in a 65 nm CMOS process. By utilizing the proposed current-mode filter and the master and slave current DAC, the current generator achieves a well-controlled output current leveling with 255 tunning steps, 83.9% current efficiency, 0.11% THD at 1 mA_{pp} output current and 2 MΩ output impedance at 500 kHz.**

Keywords—EIT, current generator, direct digital synthesis, impedance.

I. INTRODUCTION

Over the years, electrical impedance tomography (EIT) has seen growing popularity in biomedical applications including continuous respiratory monitoring, human machine interface, cancer detection and brain imaging [1]. The principle of EIT is measuring the impedance of an object (organ or tissue) at different locations and forming an image. By injecting a known ac current and measuring the induced voltage at different locations, a group of impedance data can be obtained and an image based on conductivity distribution of the measured object can be reconstructed.

The current generator (CG), also known as current driver, is one of the most important parts of EIT systems. It plays the role of injecting an accurate ac current with well-defined amplitude and frequency to object under test. For EIT applications such as lung imaging, the current amplitude range typically varies from 200 μA to 6 mA, with frequencies varying from 10 kHz to 1 MHz [2]-[5]. To guarantee the impedance measurement accuracy, there are four general requirements for a CG: a) low total harmonic distortion (THD); b) well-controlled output current amplitude; c) high current efficiency; d) high output impedance. A low THD can reduce the systematic error during impedance calculation, and a well-controlled output current amplitude can make it easy for impedance calculation and adapting for wide range of loads, while a high output impedance can avoid current amplitude variations due to load changes. Also, a high current efficiency is also critical since the CG could consume more than 80 % of the total power in state-of-art EIT systems [2]-[6].

State-of-art CGs may be classified into two categories: a) current DAC based CG, and b) voltage-to-current converter (V-I) based CG. The simplified diagrams are shown in Fig. 1. For current DAC based CG, the sinusoidal current can be directly generated by switching between different branches of current mirror DAC with different aspect ratios. Due to the simplicity of implementation and intrinsic property of current DAC, it has high current efficiency and well-controlled output current amplitude. However, it suffers from high THD due to direct digital synthesized pseudo sine wave and low output impedance due to undefined drain voltage. In addition, the fully open loop operation requires regular resetting to remove the unbalanced charge due to source and sink current mismatch. For V-I based current generator, the V-I converter converts the sinusoidal voltage signal into current, where the sinusoidal voltage can be generated by a voltage DAC with low pass filters removing high order harmonics or a RC oscillator [8]-[9]. Thanks to the pure sinusoidal input voltage, V-I based CG can achieve superior THD performance. Also, due to the well-define common mode voltage controlled by feedback, it can achieve high output impedance. However, the current efficiency is usually limited by the power-hungry feedback structure and the required high open loop gain and bandwidth. A V-I based CG with current feedback has been proposed in [10] - it simultaneously achieves high current efficiency, low THD, high output impedance and well-defined output current level. However, an external sinusoidal voltage was used without any on-chip implementation method. The transconductance of all the reported V-I based CGs are defined by the input sinusoidal voltage over a feedback resistor, where the tuning of the output current amplitude requires the change of input voltage value or the feedback resistor value. Such tuning scheme has poor resolution and significantly increases design complexity.

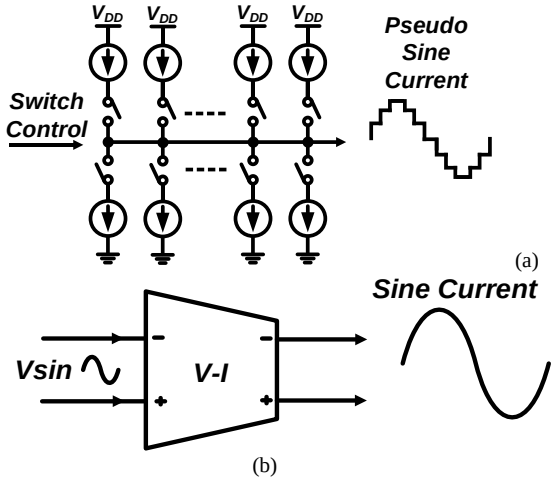

Fig. 1. Simplified diagram of (a) current DAC based CG and (b) V-I based CG.

To address these challenges, a current DAC based current generator is proposed featuring: 1) an embedded on-chip

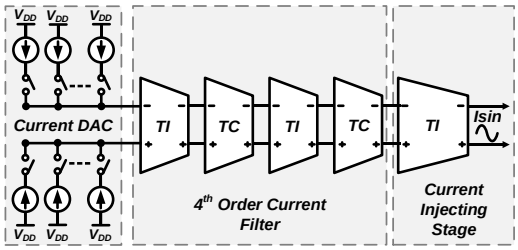

Fig. 2. Top-level block diagram of the proposed CG.

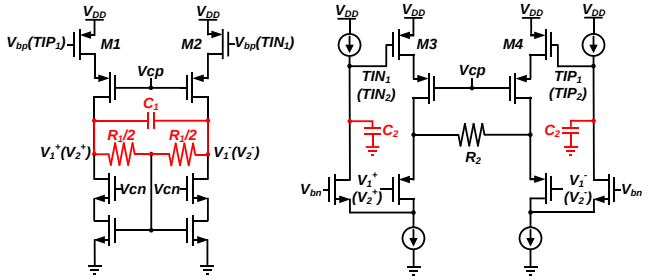

Fig. 3. Proposed current-mode filter. (a) TI based active RC filter and (b) TC based active GmC filter.

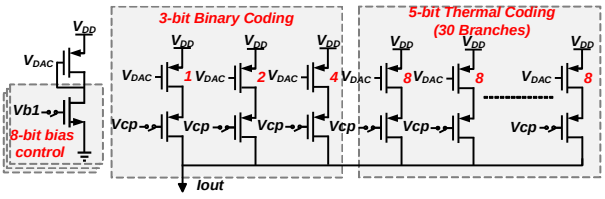

Fig. 4. Detailed schematic of the current DAC.

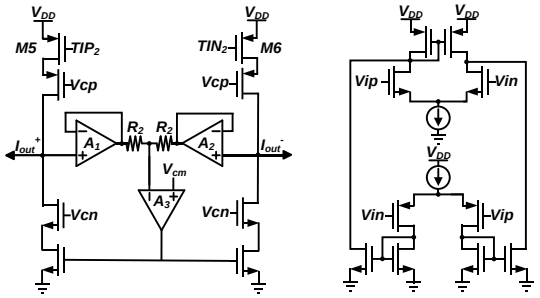

Fig. 5. Detailed schematic of (a) output stage and (b) complementary.

sinusoidal signal generator with fourth-order current filter achieving pure sinusoidal current injection; 2) well-defined output common-mode voltage achieving high output impedance; 3) well-controlled output current amplitude with large and high-resolution tuning range; 4) high current efficiency to reduce the total power budget. The rest of the paper is organized as follows. Section II shows the detailed circuit implementation and working principles. Section III presents simulation results. Section IV concludes the paper.

II. Circuit Implementation

A. Top Level Block Diagram

The simplified top-level block diagram of the proposed CG is shown in Fig. 2. It is composed of three parts: a) a current DAC for pseudo-sine current generating; b) a fourth-order current filter for removing high order harmonics in pseudo-sine current; c) an output stage for current injection. During the operating of the CG, the pseudo-sine current will be generated by the current DAC and then filtered by the fourth-order current-mode filter for pure sine current injection. The fourth-order current-mode filter is composed of two transimpedance (TI) amplifier based active RC filters and two transconductance (TC) amplifier based GmC filters.

B. Proposed Current-Mode Filter

Linearity is the most important design challenge for active filters. To address this issue, a new high linearity active filter structure with current input and current output utilizing the intrinsic high linearity of passive components is proposed. A complete current filtering process is achieved by a pair of TI based active RC filters and a TC based active GmC filter; their schematics are shown in Fig. 3. For the first stage TI filter, the two top transistors M1 and M2 are biased by a dc voltage, and the pseudo-sine current will be injected into the filter at the nodes of V_1^+ and V_1^-. The injected current will go through the parallel resistor R_1 and capacitor C_1, which create a dominant pole $1/(2\pi \times R_1 \times C_1)$ during the V-I conversion and thus the high frequency components can be attenuated. Such V-I conversion has high linearity and well-defined conversion ratio for in-band signals due to the high linearity of passive components. For the second stage TI filter, the two top transistors are controlled by the previous TC filter to perform the current input.

The TC filter is based on flipped voltage follower, where the source voltages of the input transistors will follow the input voltages and create a voltage drop at each node of R_2 and achieve a high-linearity V-I conversion. The converted current is copied by the top transistors M3 and M4 and used for the control of the second stage TI filter or the output stage. It would be intuitive that the same RC pair can be used to filter the high frequency harmonics. However, such implementation would create a dominant zero instead of a pole during the V-I conversion and thus the high order harmonics would be amplified. To overcome this issue, extra capacitors are added at the gates of the M3 and M4, where the converted current is sensed and copied for current injection at the second stage TI filter or the output stage.

In the proposed active order filter design, the current signal is conditioned by two pairs of TI and TC filters, achieving a current input and output with fourth-order low pass filtering function. For a complete current to voltage, and then back to current conversion process achieved by a pair of TI filter and TC filter, the current conversion ratio between the in-band output current and input current equals to $(R_1/R_2) \times K$, where K is the aspect ratio between M3/4 and M1/2. Consequently, the proposed fourth-order current mode filter chain has a well-defined output current.

C. Current DAC

The current DAC for generating the input pseudo-sine current should satisfy the following two requirements: 1) large tuning range with high resolution to adapt for a large load impedance range, and 2) high linearity to reduce the intrinsic THD during direct digital synthesis (DDS). A current DAC composed of a 8-bit master current DAC and another 8-bit slave current DAC are employed, where the master DAC is used for controlling the bias current and the slave DAC is used for pseudo-sine current generating. Compared with the capacitor based voltage DAC counterparts, it achieves easy

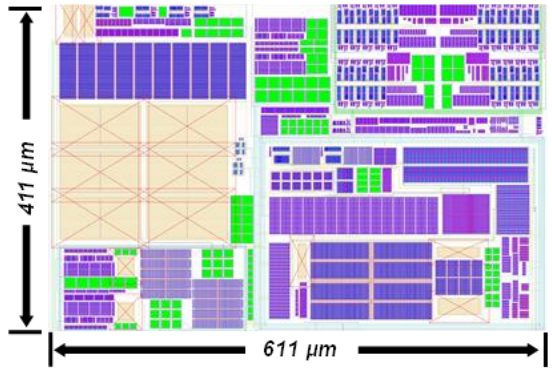

Fig. 6. Layout of the proposed CG.

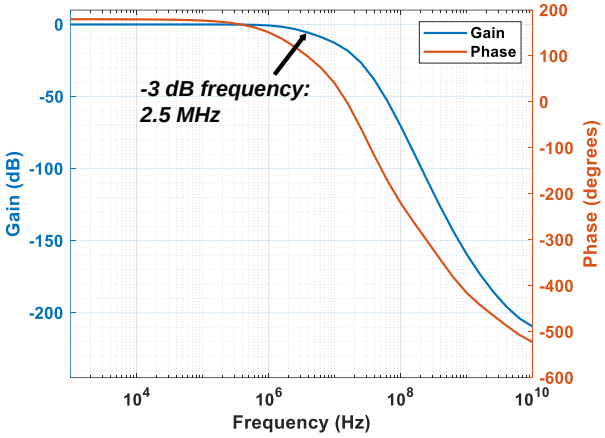

Fig. 7. ac response of the proposed fourth-order current-mode filter.

tunning, simplicity of implementation and high area efficiency. The detailed schematic of the proposed current DAC is shown in Fig. 4. By utilizing an 8-bit master DAC, the proposed CG can achieve a large tuning range with 255 linear tuning steps, which makes it adaptive for more than two orders of load impedance change. To address the requirement on linearity, a PMOS only, 8-bit slave DAC with 3-bit binary coding and 5 bit thermal coding is used. The PMOS only current DAC achieves better matching property compared with traditional current DAC structures with both PMOS and NMOS. To further decrease the integral nonlinearity (INL) and differential nonlinearity (DNL), the top 5 most significant bits (MSB) are based on thermal coding, while the binary coding 3 least significant bits (LSB) are used to reduce the complexity of the switches. To relax the bandwidth requirement of the active filter, an oversampling ratio of 128 is used for the DDS in this design.

D. Output Stage

The output stage should have a high output impedance and large output voltage range to guarantee current injection accuracy. The detailed schematic of the output stage is shown in Fig. 5. The working principle of the output stage is similar to the second TI filter, where the filtered sine current is copied by the top transistors M5 and M6. The two resistors for common-mode feedback (CMFB) are isolated by the unit-gain buffers to avoid reducing the output impedance. In addition, to avoid reduction of output voltage range, a complementary input amplifier which has rail to rail input range is used for the CMFB buffers.

The current conversion ratio between the output stage and the second stage TC filter is determined by the aspect ratio

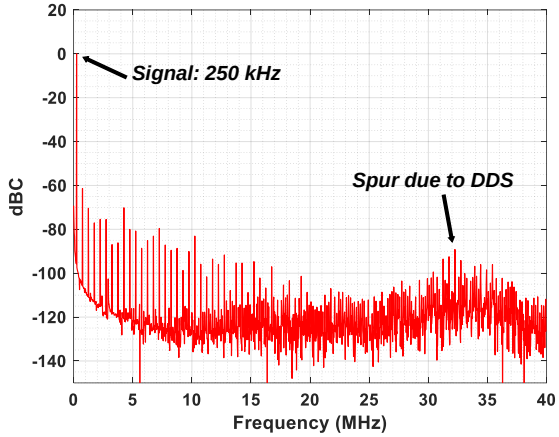

Fig. 8. FFT of the CG output current at a current magnitude of 1 mA_{pp} and frequency of 250 kHz with a 1 kΩ load resistor.

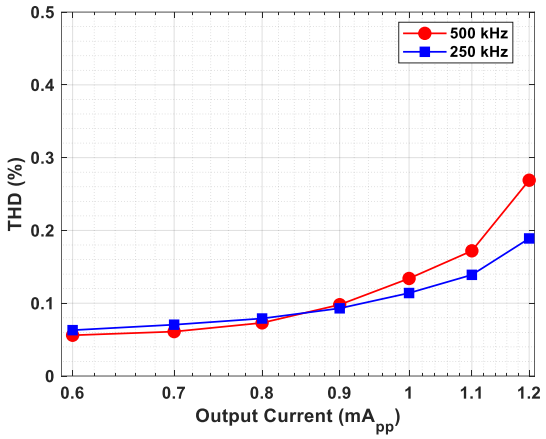

Fig. 9. THD versus different output current magnitude at signal frequencies of 250 kHz and 500 kHz.

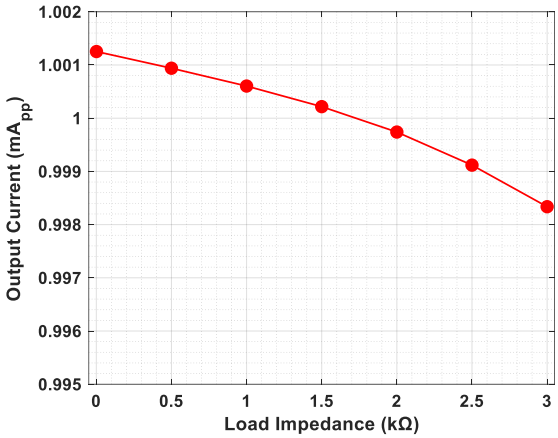

Fig. 10. The output current magnitude at 500 kHz with different load impedance values.

between M5/6 in the output stage and M3/4 in the second stage TC filter. To maximize current efficiency, the current conversion ratio between the first and second TI and TC filter pairs and the output stage are 1:5:60, respectively. The output current is 60 times the value of the initial input pseudo-sine current.

III. Simulated Results

The proposed CG was designed and simulated in a 65 nm CMOS process in Cadence Virtuoso under a 3.3 V supply with a total current consumption of 1.43 mA. The layout is shown

TABLE I
COMPARISON OF CURRENT GENERATORS

Parameters	[6]	[7]	[9]	[10]	**This work**
CMOS Process	180 nm	55 nm	65 nm	65 nm	65 nm
Supply (V)	1.2	1.2	0.5	3.3	3.3
Topology	Current DAC	Current DAC	V-I	V-I	Current DAC
On-chip Sine-wave Generation	Yes	Yes	Yes	No	Yes
Output Current Range (μA_{pp})	40-160 (4 steps)	1-100 (100 steps)	2 (fixed)	0-1375 (fixed)	0-1200 (255 steps)
THD	0.4% at 160μA_{pp}	0.7% at 100 μA_{pp}	0.088% at 2μA_{pp}	0.1% at 1.375 mA_{pp}	0.11% at 1 mA_{pp}
Current Efficiency	76.9%	84.7%	22.8 %	89.3 %	83.9%
Output Impedance	55 kΩ at 20 kHz	72 kΩ	331 kΩ at 20 kHz	1 MΩ at 500 kHz	2 MΩ at 500 kHz

in Fig. 6. The CG occupies a chip area of 0.25 mm^2 and has a bandwidth up to 1 MHz, with output current level from 0 to 1.2 mA in 255 linear steps, resulting in a maximum current efficiency of 83.9%.

The ac simulation of the current-mode filter is shown in Fig. 7. The proposed active filter has a cut-off frequency of 2.5 MHz. The CG was simulated with a 1 kΩ load resistor at an oversampling ratio of 128. The fast-Fourier-transform of the output current with a 1 mA_{pp} magnitude at 250 kHz signal frequency is shown in Fig. 8. The high frequency spur due to DDS is significantly attenuated, achieving a THD of 0.11 % in this condition.

The simulation results of THD versus different output current magnitude at signal frequency of 250 kHz and 500 kHz are shown in Fig. 9. For current magnitude lower than 0.9 mA_{pp}, the THD with signal frequency of 250 kHz is larger than that at 500 kHz due to the reduced DDS frequency (32 MHz for 250 kHz signal and 64 MHz for 500 kHz signal). For current magnitude larger than 0.9 mA_{pp}, the THD is dominated by the distortion during filtering and current injection resulting from the decreased loop gain and bandwidth when it reaches the boundary condition. Consequently, the 250 kHz signal has lower THD due to its lower bandwidth requirements. The THD at the maximum output current of 1.2 mA is 0.18 and 0.27 at 250 kHz and 500 kHz, respectively.

The output current magnitude at 500 kHz versus different load impedance is shown in Fig. 10. The proposed CG achieves an output impedance higher than 2 MΩ, which is sufficient for most EIT applications.

IV. CONCLUSION

A current DAC based current generator with current-mode filter has been proposed, achieving a maximum current efficiency of 83.9%, with a THD of 0.11% for an output current magnitude of 1 mA_{pp} and 0.19% for an output current of 1.2 mA at 250 kHz frequency. The circuit has a large current tunning range from 0-1.2 mA_{pp} with 255 linear tunning steps making the current generator adaptive for a large load impedance range. In addition, an output impedance of 2 MΩ at 500 kHz is also achieved, providing an accurate current injecting with different load impedances. Table I provides a comparison with the state-of-the-art showing the superior performance of the new CG.

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