Spatially Resolved Dielectric Loss at the Si/SiO₂ Interface

Megan Cowie^(a),^{1,*} Taylor J. Z. Stock,^{2,3} Procopios C. Constantinou^(a),² Neil J. Curson^(a),^{2,3} and Peter Grütter^(a)

²London Centre for Nanotechnology, University College London, London, United Kingdom

³Department of Electronic and Electrical Engineering, University College London, London, United Kingdom

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The Si/SiO₂ interface is populated by isolated trap states that modify its electronic properties. These traps are of critical interest for the development of semiconductor-based quantum sensors and computers, as well as nanoelectronic devices. Here, we study the electric susceptibility of the Si/SiO₂ interface with nm spatial resolution using frequency-modulated atomic force microscopy. The sample measured here is a patterned dopant delta layer buried 2 nm beneath the silicon native oxide interface. We show that charge organization timescales of the Si/SiO₂ interface range from 1–150 ns, and increase significantly around interfacial traps. We conclude that under time-varying gate biases, dielectric loss in metal-insulatorsemiconductor capacitor devices is in the frequency range of MHz to sub-MHz, and is highly spatially heterogeneous over nm length scales.

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Semiconductors are emerging as a promising platform for spin-based quantum sensing and computation, with a clear path to scalability and long coherence times. In one widely adopted architecture, single dopant atoms are buried some nanometers beneath the semiconductor surface, where they are electronically accessed by means of an applied gate voltage [1–4]. Silicon is a promising host lattice, in large part because existing Si microfabrication technologies are unparalleled for any other material [2,4]. However, it is impossible to fabricate a Si surface that is entirely homogeneous: In particular, if the surface has a SiO₂ overlayer, a variety of defects such as interfacial traps (ITs such as P_{b0} and P_{b1} centers [5]) populate the Si/SiO₂ interface, modifying the surface electronic environment and resulting in, for example, random telegraph fluctuations (1/f noise) [6–9] and threshold voltage shifts [10].

ITs in silicon devices have been studied using a wide range of techniques [11,12], including transport measurements [9,13], capacitance [14], and admittance spectroscopy [15-22], deep level transient spectroscopy [14], photoemission spectroscopy [23], and electron spin resonance spectroscopy [24-26]. With these techniques, average IT densities, and their combined effect on the global electronic properties of the device, are characterized. However, for both quantum and classical computation, it is increasingly important to understand how individual ITs modify the local electronic environment at the nanoscale.

The coherence of spin qubits in silicon, which are laterally spaced nanometers apart [1,4] is determined in part by their electronic bath [27,28] (i.e., the silicon electronic landscape). So, nanoscale inhomogeneities of the silicon susceptibility (due to, e.g., the presence of ITs) compromise qubit performance, which will become increasingly significant as qubit numbers continue to increase. Classical computation is also not immune to defect states at the Si surface. Indeed, as circuit components shrink to nanometer dimensions, surface and interface effects play an increasingly dominant role in device function [29]. It is thus important to understand the origin of inhomogeneity in the electronic properties of nanoscale silicon-based devices.

Scanning probe microscopy techniques allow for the characterization of trap densities and charge states in silicon with micron-scale [30,31] and nanoscale [32-35] spatial resolution. However, trap charging and discharging timescales, which are nonzero and associated with energy loss under the influence of a time-varying electric field, have so far not been measured for individual ITs. In this Letter, we present the first spatially resolved measurements of dielectric loss associated with individual ITs at the Si/SiO₂ interface, characterized with nanometer spatial resolution using frequency-modulated atomic force microscopy (fm-AFM) [36,37]. We find that dielectric loss is spatially heterogeneous over nanometer length scales, and that the charge relaxation times at the Si/SiO₂ interface range between 1-150 ns, where there is a significant increase in this timescale around isolated trap states.

The sample studied here is a patterned n-type Si surface buried beneath 1 nm of epitaxial silicon and terminated with 1 nm of native oxide. Figure 1 shows the spatial variability of the fm-AFM driving force F_d , which is an indirect measure of the dielectric loss, near two different trap sites observed at the Si/SiO₂ interface at variable tipsubstrate gate bias V_q . The dielectric loss is bias-dependent and highly sensitive to spatially localized ITs. The measurement methodology will now be briefly discussed, before being applied to study the sample described above.



FIG. 1. ITs at the Si/SiO₂ interface. fm-AFM F_d measurement corresponding to dielectric loss at a donorlike (a)–(c) and acceptorlike (d)–(f) interfacial trap, measured at variable bias at room temperature in ultrahigh vacuum. The color scale is $F_d = 0.550 \text{ meV/cycle.}$

At large (> 10 nm) tip-sample separations in nonmagnetic systems, where the tip-sample force is predominantly electrostatic, the fm-AFM tip-sample junction can be described as a metal-insulator-semiconductor (MIS) capacitor [33,38–43]. In this work, the MIS capacitor is composed of a metallic tip, an insulating gap of thickness z_{ins} (composed of the ~10 nm tip-sample vacuum gap plus 1 nm of SiO_2), and an n-type Si(100) substrate. The total capacitance of this system is made up of the insulator (oxide and vacuum) and interfacial (C_{int}) capacitances in series, where C_{int} describes the space-charge organization (i.e., band bending) at the silicon-oxide interface. For the low-frequency MIS capacitor, loss can be described as an equivalent series resistance, which introduces a phase shift in the circuit response corresponding to the Debye charging or discharging timescale τ of the Si/SiO₂ interface. In other words, τ is the time required to establish a surface potential V_{S} , which is nonzero due to the finite carrier mobility.

fm-AFM is a dynamic microscopy, which is why it can be used to characterize dielectric loss [44–48]. In fm-AFM, a cantilever-mounted tip is driven on the cantilever resonance ω at a constant oscillation amplitude A above a sample surface. This means that over every oscillation cycle, the insulator thickness z_{ins} varies in time. Consequently, the surface charge organization (i.e., band bending V_S) and tip-sample force (\vec{F}_{ts} [49]) also vary in time. See the Supplemental Material [50] for animations of this dynamic sample response. \vec{F}_{ts} leads to a shift in ω with respect to the free natural resonance ω_o . Assuming harmonic oscillation where $z_{ins}(t) = A \cos(\omega t)$, the frequency shift $\Delta \omega$ and drive amplitude F_d are [48,51,52]

$$\Delta \omega = \omega - \omega_o = \frac{-\omega_o}{2kA} \frac{\omega_o}{\pi} \int_0^{2\pi/\omega} \partial t F_{\rm ts}(t) \cos(\omega t) \quad (1a)$$

$$F_d = \frac{kA}{Q} - \frac{\omega_o}{\pi} \int_0^{2\pi/\omega} \partial t \, F_{\rm ts}(t) \sin(\omega t), \qquad (1b)$$

where k and Q are the spring constant and Q factor of the cantilever. In the derivation of Eq. (1) (see Refs. [38,48,51–53]), Eq. (1b) contains the phase information of the Fourier series expansion of $F_{ts}(t)$, such that $\Delta \omega$ is related to the components of $\vec{F}_{ts}(t)$ which are in phase with $z_{ins}(t)$ and F_d depends on the out-of-phase $\vec{F}_{ts}(t)$ components. A nonzero surface charge organization timescale τ therefore manifests as in increase in F_d [38]. fm-AFM, then, can be thought of as spatially localized admittance spectroscopy [12,15,19] in which the MIS capacitance and conductance are measured by modulating the MIS potential. Typically in admittance spectroscopy, the MIS potential is modulated by applying an ac bias. In fm-AFM, the MIS potential modulation occurs inherently due to the oscillating cantilever.

The results shown in this Letter were measured in the low-frequency (quasistatic) regime ($f = 2\pi\omega \approx 310$ kHz), such that an increase in τ means that more energy is dissipated by Ohmic loss [44,54]. In other words, τ is the resistor-capacitor (RC) time constant of the MIS capacitor. In the small-angle regime where $\tau \ll 1/f$, as in this experiment, the surface charge reorganization can be approximated as a constant phase offset δ between $F_{\rm ts}(t)$ and $z_{\rm ins}(t)$:

$$\delta = \tau \omega, \tag{2}$$

where $\omega = 2\pi f$. Consequently, an increase in τ corresponds to an increase in the out-of-phase force component, and in the measured F_d . Since in the small-angle regime $\tan(\delta) \approx \delta$, Eq. (2) shows that an increase in τ corresponds to an increase in the equivalent series resistance or loss tangent $\tan(\delta)$.

In this Letter, F_d is measured using fm-AFM to determine the spatial inhomogeneity of τ . The experimental τ is calculated by comparing experimental F_d bias spectra to modeled F_d bias spectra at variable τ . The modeled F_d spectra are calculated by solving the MIS capacitor model as a function of time over an entire cantilever oscillation cycle (by varying the insulator thickness z_{ins}). See the Supplemental Material for a description of the MIS model used in this work. The MIS force $F_{ts}(t)$ is then calculated and integrated according to Eq. (1), to solve for Δf and F_d . This series of calculations is repeated for ~10 000 values of τ . For each measured bias, the experimental F_d is compared to all of the modeled results at that bias. The model that minimizes the difference between the experimental and modeled F_d spectra is taken as the best fit τ .

Results.—The sample measured here contains patterned squares of variable two-dimensional dopant density, up to a maximum of 1.6×10^{14} /cm² [55], on a background substrate doping of 9.0×10^{14} /cm³. The unpatterned

background is bulk doped with phosphorous, while the patterned squares are delta-doped with arsenic with a dopant layer thickness of approximately 2 nm. The entire wafer is capped by 3 nm of epitaxial Si, the surface of which has subsequently formed 1 nm of native SiO_2 , as determined by secondary mass ion spectroscopy [55]. The results shown in Figs. 1 and 2 were measured in the background (lowest dopant density) region.

Spatial inhomogeneity: The Si/SiO₂ interface is prone to trap states that modify the electronic properties of the MIS capacitor [6,12,56]. In particular, ITs (such as P_{b0} and $P_{\rm b1}$ centers) that have energy levels within the band gap interact significantly with the Si/SiO₂ interface charge [12,57]. Donorlike traps [e.g., Figs. 1(a)-1(c)], which have energies in the lower half of the band gap, can become positively charged via emission of an electron to the valence band. Acceptorlike traps [e.g., Figs. 1(d)-1(f)], which have energies in the upper half of the band gap, can become negatively charged via capture of an electron from the conduction band [56,57]. The interface state occupancy depends on V_S (and therefore V_q), since capture or emission into a trap depends on its energy with respect to the Fermi level E_f [6]. This section shows that when the fm-AFM tip is positioned near an IT, the surface charging timescale τ increases. This is measured as an increase in the applied fm-AFM drive amplitude F_d .

Figures 2(a)–2(f) show modeled band diagrams including a donorlike trap and an acceptorlike trap at the bottom and top of the fm-AFM cantilever oscillation. The donorlike trap is unoccupied at high negative voltage, but as $|V_g|$ decreases and the bands flatten and bend downward, the donorlike trap energy lowers below E_f , and it becomes occupied. The acceptorlike trap is unoccupied from negative biases up to positive biases, where the trap energy lowers below E_f and it becomes occupied. The trap state energies found here (0.17 eV above the valence band for the donorlike trap and 0.65 eV above the valence band for the acceptorlike trap) are in agreement with accepted levels for P_{b0} states [26,58]. Animations of the IT charge states as the cantilever oscillates are shown for variable bias V_a in the Supplemental Material.

Figure 2(g) shows the bias-dependent energy of each trap. At biases between the crossing points, the trap energy shifts above and below E_f during every oscillation cycle [Figs. 2(b) and 2(e)] and there is a significant increase in $tan(\delta)$ as compared to the trap-free spectrum [Fig. 2(h)]. This is because, upon electron capture and re-emission as the cantilever oscillates, loss occurs as the system relaxes to its ground state in a mechanism attributed to cascade phonon scattering [15,19,59,60]. The magnitude of $tan(\delta)$ measured here is consistent with previously reported biasdependent loss peaks attributed to interface states in silicon [21,22]. The gray spectrum in Fig. 2(h) corresponds to the intrinsic relaxation timescale of the Si/SiO₂ interface. The orange and blue spectra show the increase in the surface relaxation timescale near Si/SiO₂ ITs. Note that the gray spectrum in Fig. 2(h) is nonzero and also varies with bias. An explanation of the origin of this background bias dependence (i.e., why τ is nonzero even in the absence of ITs) will follow.

The bias-dependent spatial inhomogeneity of $tan(\delta)$ manifests as the ringlike F_d features in Figs. 1 and 3 [35]. Any spatially localized process that exhibits a peak in a bias spectrum in fm-AFM manifests as a ring when imaged



FIG. 2. Interfacial state occupancy and loss. As the cantilever oscillates, the potential at the sample surface varies. (a)–(f) Modeled silicon band bending near the Si/SiO₂ interface (z = 0) at the bottom ("bot," closest z_{ins} , solid) and top ("top," farthest z_{ins} , dashed) of the cantilever oscillation at different biases (V_g). (The dashed and solid curves nearly overlap at positive biases.) The tip and insulating gap are not shown. Donorlike (orange) and acceptorlike (blue) states are shown at the bottom and top of the cantilever oscillation. The state occupancy is indicated by full (occupied) or empty (unoccupied) circles. (g) Modeled V_g -dependent energy of the donorlike and acceptorlike states relative to E_f at the bottom (solid) and top (dashed) of the 6 nm cantilever oscillation. The corresponding modeled crossing points, where the trap energy equals E_f , are indicated by vertical lines. (h) RC time constant τ and loss tangent tan(δ) measured above a donorlike trap (orange), acceptorlike trap (blue), and far from either trap (gray). Ten curves are shown for each trap, with their average overlaid. In (h), the uncertainty diverges to infinity as V_g approaches the flatband voltage V_{fb} , so this region is omitted.



FIG. 3. Spatial inhomogeneity of Si/SiO₂. fm-AFM F_d measurement of the patterned surface at variable bias: (a) $V_g = -4$ V; (b) $V_g = -6$ V; and (c) $V_g = -8$ V. The dopant density is highest in the two leftmost squares, intermediate in the right square, and lowest in the background. The color scale bar for (a)–(c) is $F_d = 0.500$ meV/cycle.

spatially at constant height [61] due to the spatial localization of the top gate (tip), which introduces circularly symmetric equipotential lines at the sample surface. As the tip moves in x, y, or z away from a trap, the peak shifts to more extreme biases. This is demonstrated in the Supplemental Material.

Dopant density dependence: Three "delta-doped" patterned squares of this sample can be seen in Fig. 3. Almost no rings appear in the highly doped (square-patterned) regions. This is due to the increased Si metallicity within the patterned squares: as the dopant density increases, the change in band bending over every fm-AFM oscillation cycle (ΔV_S) decreases, meaning that defects are not electronically accessed according to the process shown in Figs. 2(a)-2(f) (that is, the crossing points would occur at $V_q < -10$ V). By similar reasoning, acceptorlike rings are much sparser: measurements at positive bias-not shown-exhibited fewer than five rings over the area shown in Fig. 3. This is because at positive biases (in the accumulation regime), ΔV_S is small as the cantilever oscillates, so only states very close to the conduction band edge have crossing points at $V_q < 10$ V. The donorlike IT density in Fig. 3 is approximately 10 traps/100 nm².

Bias dependence: Even in the absence of ITs, the surface charge density continually reorganizes over every cantilever oscillation cycle. The nature of the surface charge reorganization is bias-dependent, and can be understood in terms of the bias regimes of the MIS capacitor at



FIG. 4. Bias dependencies of an MIS capacitor. (a) Measured drive amplitude F_d with the tip close to the surface (color) and far from the surface (black, $z_{ins} \sim 1 \mu m$). Modeled F_d for various τ (indicated) are also shown. Six regimes (ss, sw, ww, wd, dd, and aa) are identified, indicating the bias regime (s, strong inversion; w, weak inversion; d, depletion; or a, accumulation) at the bottom and top of the oscillation. (For example, in the wd regime, the capacitor is under weak inversion at the closest tip-sample separation, and depletion at the farthest tip-sample separation.) (b) Corresponding RC time constant τ and loss tangent $\tan(\delta)$. At the flatband voltage $V_{\rm fb}$, indicated by a dashed line, the F_d curves all overlap and the τ and $\tan(\delta)$ uncertainties diverge to infinity, so this region was omitted.

the bottom and top of the cantilever oscillation, as defined in the Fig. 4 caption. Animations of the MIS bias regimes as the cantilever oscillates are shown in the Supplemental Material.

The dielectric loss measured here depends in part on the number of carriers moving within the depletion region as the cantilever oscillates. (See the Supplemental Material for a more detailed explanation.) When the cantilever oscillates within the depletion and weak inversion regimes, ΔV_S is large over every oscillation cycle. Correspondingly, the number of holes moving within the depletion region as the cantilever oscillates is large, so τ and tan(δ) [Fig. 4(b)] are large. When the cantilever oscillates within the strong inversion and accumulation regimes, ΔV_S is small and the number of carriers moving as the cantilever oscillates is small, so τ and tan(δ) decrease. This signifies that dielectric loss corresponding to the surface charge reorganization in response to a time-varying MIS potential is inherently bias-dependent.

Conclusions.—We show that the magnitude of dielectric loss at the Si/SiO₂ interface is highly inhomogeneous [28,35,43], dopant-density-dependent, and gate-bias-dependent. In particular, ITs lead to a dramatic increase in dielectric loss at biases corresponding to the trap state energy. This result is directly applicable to fixed-geometry field-effect devices. In such devices, where the MIS

potential is modulated by applying an ac gate bias, increasing the ac bias amplitude will increase the width of this bias-dependent loss peak. Increasing the distance between the gate and the trap (or, if a qubit is acting as a spectrometer of the trap state [27], the distance between the qubit and the trap) will shift the peak toward more extreme voltages.

The surface charge organization timescale τ measured here is spatially variable and ranges between 1 and 150 ns, which encompasses typical Rabi frequencies of buried spin qubits (which are between 1 and 10 MHz) [62,63]. This indicates that the amplitude and phase of the potential at qubit locations will be a function of the temporal structure of the applied bias pulse sequence and the local position and energy level of defect states.

The values of V_g in this work are much greater than the typical $\mu V - mV$ values used for spin qubit readout. However, the bias-dependent MIS surface potential is highly sensitive to the capacitor geometry, specifically the insulator thickness. Here, the closest tip-sample separation is 12 nm, but for the same capacitor with a 1 nm insulator thickness, the peak that occurs at ~ -4 V in Fig. 2(h) can be expected to occur closer to -500 mV.

Finally, the tan(δ) ~ 0.1 measured here (which is similar to other room temperature findings [64–67]) is several orders of magnitude smaller at cryogenic temperatures [68,69], as carrier concentrations decrease and various phonon scattering mechanisms are reduced [67]. Still, these dielectric losses can occur under any time-varying electric field, and so should be taken into consideration for the continued development of nano- and atomic-scale semiconductor devices, quantum sensors, and quantum computers.

Methods.—Experimental setup: Nanosensors platinum-iridium coated silicon tips (PPP-NCHPt) with ~310 kHz resonant frequency, spring constant 42 N/m, and a *Q* factor of approximately 18 000 were used for all measurements. The oscillation amplitude was 6 nm. Experiments were conducted at room temperature (assumed to be 300 k) in ultrahigh vacuum (~10⁻¹⁰ mbar).

Bias spectroscopy: Each bias spectrum includes the forward (positive to negative V_g) and backward curve superimposed, showing that there is negligible hysteresis with bias. Each sweep was acquired over ~30 s.

Multipass imaging: Figures 1 and 3 were measured by electrostatic force microscopy multipass imaging. In the first pass, the tip tracked the topography defined by $V_g = 0$ V at a set point $\Delta f = -3$ Hz. In subsequent passes, the tip followed this same topography, but V_g was set to the displayed values. The rings shown here were stable over several weeks of measurement.

Sample fabrication: The Si(001) substrate is phosphorous-doped $(9.15 \times 10^{14}/\text{cm}^3)$ and 300 µm thick. The variably arsenic delta-doped regions were fabricated by hydrogen resist lithography [55].

MIS model: The MIS model [38,49,56] parameters were closest, $z_{ins} = 12$ nm; tip radius, 5 nm; $\epsilon = 11.7$; electron affinity, 4.05 eV; tip work function, 4.75 eV; electron and hole effective masses, 1.08 and 0.56; n-type dopant density, $5 \times 10^{17}/\text{cm}^3$; and band gap, 0.7 eV. This band gap is smaller than the ~1.1 eV expected for bulk Si; the discrepancy could be due to surface band gap narrowing due to the presence of the large surface state density, as in [70,71]. For details of the MIS model, see the Supplemental Material.

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^{*}Corresponding author: megan.cowie@mail.mcgill.ca

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