A High-Voltage, Implantable ASIC for Active Interfaces of the Vagus Nerve

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Abstract—**Versatility of neural interfaces is a key factor in the efficacy of bioelectronic solutions for treating neurological and cardiac disorders. High-density and highly selective interfaces demand a small form factor, resulting in very high electrode impedances that require a large compliance voltage. This paper presents the design of a low-noise, electrode-driving ASIC in 180-nm high-voltage CMOS technology to achieve concurrent stimulation and recording for vagus nerve interfaces. Inter-channel crosstalk is minimized using pole-shifting. The ASIC has a variable recording gain of 60 to 74 dB and programmable, stimulating currents of 4 to 124 µA, which account for variations in the electrode characteristics. The ASIC occupies an area of 2.31 mm^2. Measured results show clear biphasic stimulus pulses ranging in widths from 10 to 500 µs. To address the impact of artifacts on biopotential recording, the recording amplifier has a very low input-referred noise of 2.92 µV$_{rms}$ over a variable bandwidth that ranges from 300 Hz to 1.4 kHz or 6.6 kHz with or without pole shifting, respectively.**

Keywords—Active electrodes, bioelectronics, implantable neural interface, microchannel electrodes

I. INTRODUCTION

Disorders of the nervous system are a major cause of disability across the globe, with around one in nine deaths of a nervous system disorder and over 28% of years lived with disability [1]. Therapeutic strategies to restore motor and sensory functions have been developed to achieve monitoring and artificial control of the nervous system. Bioelectronic solutions employ a wide range of neural electrodes to interface the nervous tissues, enabling direct communication with the fibres in the central or peripheral nervous system by providing the pathways for neural modulation, recording, and regeneration [2]. A typical implementation of neuroprosthetic devices used to address symptoms of the peripheral nerves involves an implantable passive interface that contacts the neural tissue and communicates with separate circuitry for electrical stimulation and biopotential recording. Though electrode types vary in shape and level of invasiveness, a common shortcoming of passive interfaces is in the quality of measured signals in the presence of noise and reliable scaling of channel density within a regenerative system.

A solution to address the challenges of passive interfaces, integrates microfabricated electronics into the electrode site using an application-specific integrated circuit (ASIC) as a substrate for the electrodes, as shown in the conceptual diagram of Fig. 1. In-situ recording amplifiers result in a higher signal-to-noise ratio, and the use of multiplexing
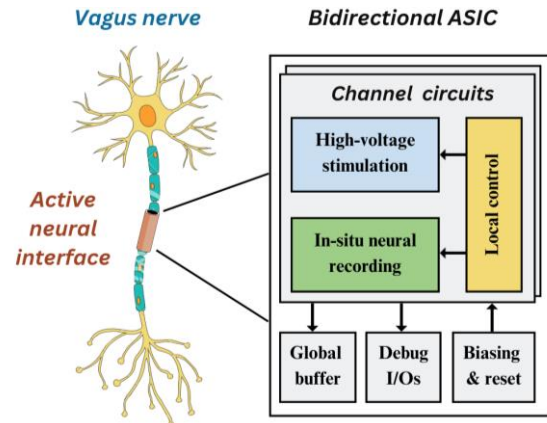
Fig. 1. Active interface conceptual diagram.

circuits minimise the number of external connectors, improving device reliability [3]. Careful attention to device materials and fabrication processes, such as silicon post-processing and interface encapsulation, can ensure the safety, efficacy, and longevity of the electrode for both stimulation and recording. This is of particular importance in the development of implantable devices due to the impact of foreign body response on both the host and the interface system, though its primary aim is to assist with healing damaged tissue [4]. It is, therefore, desirable to interface the nervous tissue in an environment that fosters regeneration and supports neural growth while operating as an active interface.

The design of active neural probes that incorporates CMOS microfabrication has been widely developed for interfacing the central nervous system over the past few decades, achieving high degrees of selectivity and channel density [5]. Interfaces aimed at the peripheral nervous system have been considered more recently, for applications such as retinal prosthesis [6], bladder control [7], and regenerative interfaces [8] that modulate the vagal fibres [9] to encourage growth and achieve artificial control of the severed vagus nerve following a heart transplant. Concurrent operation of electrical stimulation and neural recording in adjacent channels suffers from stimulus artifacts. To overcome the challenges imposed by the high-voltage stimulation pulses on the microvolt-level biopotential measurements, methods have been developed to minimize artifacts, improve front-end immunity, and reconstruct neural data [10].

This paper presents an implantable ASIC designed in a high-voltage CMOS technology for concurrent electrical stimulation and neural recording. Section II outlines the system architecture including the control, stimulating, and recording circuits. Section III presents performance results of the ASIC. Concluding remarks are drawn in Section IV.

II. DEVICE ARCHITECTURE

A. ASIC Overview

The active electrode-driving ASIC comprises three main blocks responsible for electrical stimulation, neural recording, and local digital control of the channels. Additional circuits that supply biases, generate reset signals, switch between the channels, and buffer the measured neural signals are present in a small global area (outside channels) of the chip. The architecture of the system design is shown Fig. 2. There are two channels located longitudinally across the ASIC, each consisting of a tripolar high-voltage (HV) electrode structure. The corresponding pads ($E_{A,B,C}$) are surrounded by the digital and analog circuits of varying voltage capabilities. Low voltage transistors are used for digital control and biopotential recording, to minimize power consumption and design area. To achieve safe and efficacious stimulation despite the high-impedance electrode sites, high-voltage transistors compliant up to 45 V were employed at the output stage of the stimulating current drivers, ensuring a high voltage compliance. The circuits for generating the currents, including the digital to analog converter (DAC) and those used for calibration, operate at low voltages.

B. Control Logic

A two-line communication link is used to transfer the command bits for the desired function from an external control unit. Pull-up/down resistors are used to set channel ID values on-chip, and additional input/output (I/O) pins are available for global ID setting. This enables channel scaling by parallelising multiple ASICs to form a high-density or a distributed neural interface. Upon detection of the control signal with a matching ID under a 1 MHz clock, one of seven operating modes is identified; idle, neural recording, stimulation with low-frequency, high-frequency and chopped pulse profiles [11], calibration, and electroplating. The parameters are stored in shift registers to provide analog switch control at the appropriate times. Switch control is achieved via a finite-state machine (FSM) during stimulation, which cycles through anodic, cathodic, and discharge phases ($\Phi_{A,C,D}$, respectively) with controlled pulse widths to ensure charge balance [12]. The timing parameters are stored in 7-bit pulse-width, 4-bit delay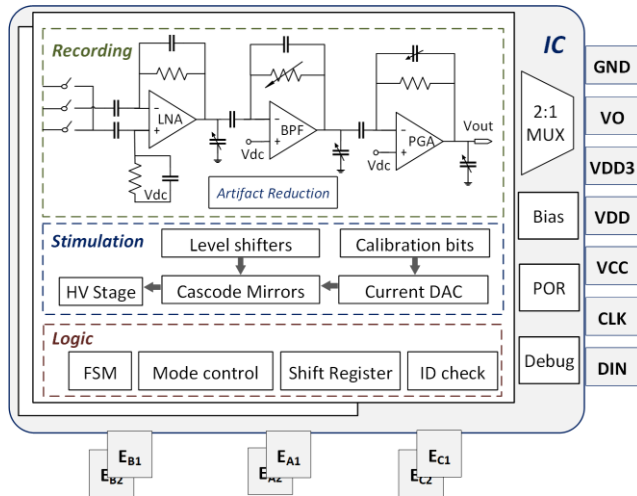, and 4-bit period registers, which enables a fine resolution of 8 µs for low-frequency, and 1 µs for high-frequency stimulation. Recording is enabled by connecting the high-voltage electrode sites to the low-voltage, ac-coupled analog front-end, with additional control over the amplifier gain and signal bandwidth. A selected mode will continue to operate until the next mode has been accepted and the shift registers are replaced as long as the device remains powered on, limiting the delay imposed by mode switching. Furthermore, adjacent channels and parallel ASICs can operate in different modes with varying parameters completely independently.

C. Simulating Drivers

A high-voltage current source is implemented to provide biphasic, square stimulating current waveforms from a high-impedance output stage. Fig. 3 shows the schematic of the current driver structure, which comprises a 5-bit binary-weighted transistors current DAC, high-voltage cascode current mirrors and transistor switches at the electrode nodes (controlled through level shifters), as well as low-voltage calibration current mirrors. The 9-bit calibration mirrors enable fine adjustments in the scaled outputs to account for process variations that otherwise result in mismatch between the anodic and cathodic phases, or the currents injected through each electrode pad. The stimulating driver provides a wide range of currents, suitable for eliciting or blocking neural activity within a microchannel neural interface [8]. The high-voltage output mirrors at each outer electrode node ($E_{B,C}$) accept a 3-bit calibration command that can increase the stimulating current by a factor of 10% to 17.5% of the scaled output relative to each phase. The remaining 6 bits can vary the currents at each node with respect to one another, thus matching the currents at E_B and E_C from 6.25% to 43.75%. The output current I_A at the center node E_A is the sum of the currents I_B (at node E_B) and I_C (at node E_C), which can be expressed as

$$\begin{cases} I_B = (10 \times (cal[5:3]/16 + A[4:0]) \\ \qquad + cal[8:6]/4) \times 200 \text{ nA} \\ \\ I_C = (10 \times (cal[2:0]/16 + A[4:0]) \\ \qquad + cal[8:6]/4) \times 200 \text{ nA} \end{cases} \quad (1)$$

where $A[4:0]$ is the 5-bit current DAC control setting and *cal[8:0]* is the 9-bit calibration bus stored locally in each

Fig. 2. Interface IC functional block diagram illustrating the three-stage neural recording amplifier circuit schematic.
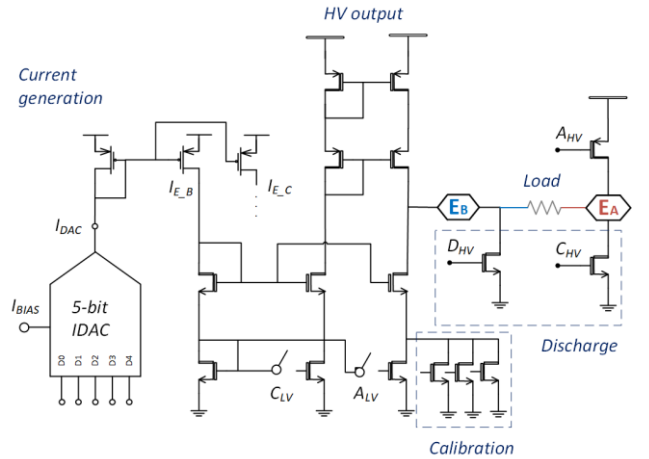

Fig. 3. Stimulator current driver circuit schematic including the 5-bit IDAC, cascode current mirrors, and discharge switches.

channel. All high voltage devices of the output stage supplied by *VCC* are compliant up to 45 V, while the current DAC and low-voltage mirrors operate at a 3.3 V supply.

D. Recording Amplifiers

Neural activity in the form of action potentials is measured by the analog front-end supplied by 1.8 V. This consists of a three-stage amplifier, as shown in the recording section of Fig. 2. This circuit is designed to capture µV-level biopotential signals that range in the frequencies of 300 Hz to 5 kHz. A low-noise amplifier (LNA) with a gain of 100 V/V (40 dB) is used in the first stage, following a set of blanking switches that protect the low-voltage recording circuits from the high-voltage electrode sites. The next stage constricts signal bandwidth using a bandpass filter (BPF) with a gain of 5 V/V (14 dB), and optional high-pass corner adjustment by the feedback pseudo-resistor. The final stage uses a programmable gain amplifier (PGA), that uses a 2-bit control signal to determine a gain of 2 to 10 V/V (6 to 20 dB), thus resulting in a wide front-end gain ranging around 1000 to 5000 V/V (60 to 74 dB).

E. Artifact Reduction

In order to limit the impact of artifacts during concurrent electrical stimulation and neural recording in adjacent channels, continuous monitoring of the biopotential signals is carried out to automatically detect the presence of artifacts [13]. This enables adjustment of the amplifiers' low-pass corner, which in turn attenuates a wider range of frequencies in the recording channel, including those of the stimulus pulses. A differential comparator is placed in parallel to the LNA, the output of which controls the variable load capacitors at each amplifier stage.

III. RESULTS

The active electrode ASIC was implemented in the XFAB 0.18 µm HV CMOS technology. Fig. 4 shows a micrograph
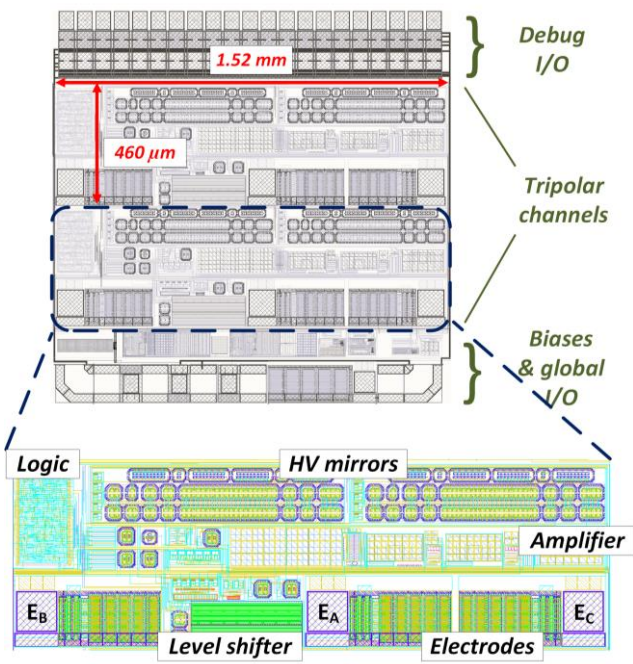

Fig. 4. Micrograph of the interface ASIC and the channel layout illustrating the electrodes, current mirrors, logic, and recording amplifier.

of the ASIC with a labelled layout view of the tripolar channel including the control logic, stimulating drivers (high-voltage mirrors), level shifters, analog front-end (AFE), and the high-voltage electrode pads. Each channel occupies 0.61 mm^2 within a total chip area of 2.31 mm^2.

A. Electrical Stimulation

Measured results of the channel stimulator are shown in Fig. 5. These include the transient waveforms at different stimulating modes of varying frequency settings with pulse widths ranging from 10 µs to 500 µs and packet widths of 2 µs during the chopped setting. The voltage measurements were obtained using a Keysight MSO-X 3024T oscilloscope across a 10-kΩ resistive load. The digital control pulses generated by the FSM for driving the phase switches are displayed as Φ_A, Φ_C, and Φ_D for reference. The discharge phase is enabled by default outside of the anodic and cathodic phases to avoid the build-up of charge on the tissue.

In post-layout simulations, the current DAC showed an average integrated non-linearity (INL) of 0.138 of the least-significant bit (LSB), and the differential non-linearity (DNL) was 0.017 LSB, which is scaled by a factor of 10 from a bias supply of 200 nA. A maximum variation of 40% in the output current was observed in Monte Carlo simulation, which can be adjusted to meet demands using the calibration mode.
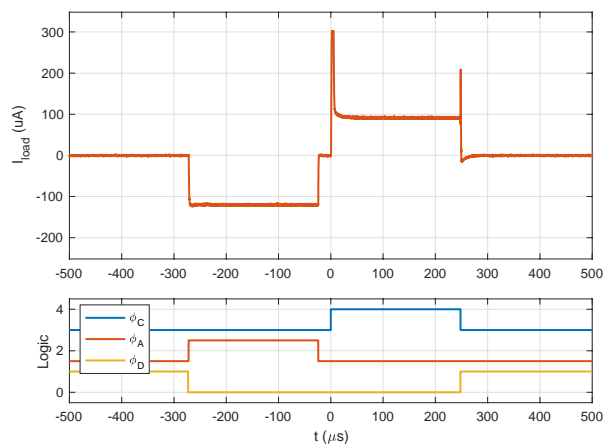
(a)
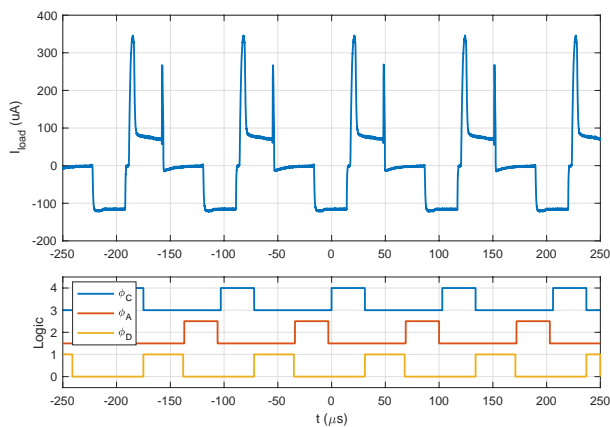
(b)

Fig. 5. Transient measurements of stimulus pulses for (a) low-frequency, and (b) high-frequency settings.

B. Neural Recording

The three-stage amplifier in each channel aims to limit the noise contribution of the device via appropriate design of the LNA, achieving a total input-referred noise (IRN) of 2.92 μV_{rms}, as obtained in post-layout simulations. An overall gain of 74.8 dB can be obtained from the analog front-end over the frequencies ranging from 335 Hz – 6.6 kHz at the nominal setting, and 330 Hz – 1.4 kHz during pole shifting. Measurements of the recording unit are ongoing to verify the simulated performance.

IV. CONCLUSION

A high-voltage, implantable ASIC for active neural interfaces has been presented. The stimulator provides a wide range of modes and parameters for evoking or blocking neural activity. The recording front-end has a low-noise performance (IRN of 2.92 μV_{rms}), with variable gain (up to 74.8 dB) and bandwidth (330 Hz to 1.4 kHz or 6.6 kHz) settings. A comparative overview of the circuit performance with respect to the state-of-the-art in active electrodes is outlined in Table I. This work provides a large voltage compliance for stimulation and a programmable gain and bandwidth for recording. The ASIC employs artifact reduction for concurrent recording and stimulation.

TABLE I.   COMPARATIVE PERFORMANCE REVIEW

	[7]	[14]	[15]	This work
Technology	0.18 µm	65 nm	0.35 µm	0.18 µm
Supply (V)	1.8, 3.3	±11	3, 5	1.8, 3.3, 40
Die area	-	4 mm²	2.15 mm²	2.31 mm²
Application	Bladder	Brain-computer interface	Retinal	Vagus nerve
Stimulation Compliance Max current Frequency	3.3 V 2.48 mA 1–40 Hz	±11 V 10.2 mA 10 Hz	5 V 1.1 mA 50 kHz	45 V 124 µA 7.4 Hz – 20 kHz
Recording Gain Bandwidth IRN (μV_{rms})	61.6 dB 300 Hz–5.3 kHz 3.62	- 10 Hz – 1 kHz 2.9	50 dB 0.1–300 Hz 2.08	60–74 dB 330 Hz–6.6/1.4 kHz 2.93
Artifact reduction	Yes	Yes	No	Yes

REFERENCES

[1] D. C. Bergen and D. Silberberg, "Nervous system disorders: A global epidemic," *Neurology and Public Health,* vol. 59, no. 7, pp. 1194-1196, 2002.

[2] V. Paggi, O. Akouissi, S. Micera and S. P. Lacour, "Compliant peripheral nerve interfaces," *J. Neural Eng.,* vol. 18, no. 3, pp. 1-26, 2021.

[3] R. Verplancke, M. Cauwe, D. Schaubroeck and e. al., "Development of an active high-density transverse intrafascicular micro-electrode probe," *J. Micromech. Microeng.,* vol. 30, no. 1, 2020.

[4] C. E. Larson and E. Meng, "A review for the peripheral nerve interface designer," *J. Neuroscience Methods,* vol. 32, 2020.

[5] N. A. Steinmetz, C. Koch, K. D. Harris and M. Carandini, "Challenges and opportunities for large-scale electrophysiology with Neuropixels probes," *Current Opinion in Neurobiology,* vol. 50, pp. 92-100, 2018.

[6] T. Noda, K. Sasagawa, T. Tokuda and e. al., "Smart electrode array device with CMOS multi-chip architecture for neural interface," *Electronics Letters,* vol. 48, no. 21, pp. 1328-1329, 2012.

[7] W. Tao, F. Li, C. Wang, G. Tu, Z. Wang and X. Lü, "Design of integrated neural stimulating and recording frontend for bladded control prosthesis," *Analog Integrated Circuits and Signal Processing,* vol. 91, pp. 403-416, 2017.

[8] H. T. Lancashire, D. Jiang, A. Demosthenous and N. Donaldson, "An ASIC for recording and stimulation in stacked microchannel neural interfaces," *IEEE Trans. Biomed. Circuits Syst.,* vol. 13, no. 2, pp. 259 - 270, 2019.

[9] M. Habibollahi, D. Jiang, H. Lancashire and A. Demosthenous, "A bidirectional ASIC for active microchannel," in *Int. Conf. Electronics Circuits Syst. (ICECS)*, Glasgow, 2022.

[10] A. Zhou, B. C. Johnson and R. Muller, "Toward true closed-loop neuromodulation: artifact-free recording during stimulation," *Current Opinion in Neurobiology,* vol. 50, pp. 119-127, 2018.

[11] D. Jiang and A. Demosthenous, "A multichannel high-frequency power-isolated neural stimulator with crosstalk reduction," *IEEE Trans. Biomed. Circuits Syst.,* vol. 12, no. 4, pp. 940-953, 2018.

[12] D. Jiang, Y. Wu, N. Almarri and e. al., "An integrated multi-channel opto-electro arbitrary waveform stimulator for treating motor neurone disease," in *IEEE Int. Symp. Circuits Syst. (ISCAS)*, Daegu, 2021.

[13] M. Habibollahi, F. F. Hanzaee, D. Jiang, H. Lancashire and A. Demosthenous, "An active microchannel neural interface with Artifact Reduction," in *IEEE Int. Symp. Circuits Syst. (ISCAS)*, Daegu, 2021.

[14] J. P. Uehlin, W. A. Smith, C. R. Pamula and e. al., "A single-chip bidirectional neural interface with high-voltage stimulation and adaptive artifact cancellation in standard CMOS," *IEEE J. Solid-State Circuits,* vol. 55, no. 7, pp. 1749-1761, 2020.

[15] R. Ramezani, Y. Liu, F. Dehkhoda and e. al., "On-probe neural interface ASIC for combined electrical recording and optogenetic stimulation," *IEEE Trans. Biomed. Circuits Syst.,* vol. 12, no. 3, pp. 576-588, 2018.