A Four-Channel Analog Front-End ASIC for Wearable A-Mode Ultrasound Hand Kinematic Tracking Applications

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Abstract—This paper presents the design of a four-channel analog front-end ASIC for a wearable A-mode ultrasound hand kinematic tracking system. The system uses ultrasound to record and decode forearm muscle morphology for controlling a prosthetic hand. The design of the wearable system will be in the form of a custom-built bracelet with eight analog front-end/piezoelectric transducer pairs embedded throughout its circumference. The ASIC has four analog front-end channels, each comprising a pulser for driving the transducers, a transmit/receive switch for isolation/protection and a programmable gain amplifier. The ASIC was implemented in a 0.18 µm HV BCD process. Measurements show that the pulser can drive a 130-pF capacitive load with 30 Vpp square pulses at 1 MHz. The programmable gain amplifier can support three gain levels (9.54 dB, 15.56 dB, 21.58 dB) and consume 1.74 mW. Acoustic experiments demonstrate successful ASIC operation in both the transmit and receive modes.

Keywords—Assistive/rehabilitation technology, hand gesture recognition, human-machine interface, ultrasound ASIC, wearable health device.

I. INTRODUCTION

Hand kinematics is the movement of mechanical points and systems within the human hand, taking into consideration time and space but not the acting forces [1]. Hand kinematic tracking is a dynamic process, aiming to closely follow and predict hand movements. Hand kinematic tracking is also evaluated dynamically, for instance, by controlling a moving object [2]. Hand kinematic tracking is a major and rapidly advancing research area in human-machine interfaces (HMI) with applications ranging from robotic manipulation, prosthetic control to gaming/virtual reality. These applications typically require HMI systems that are portable/wearable, robust and easy to use.

Technological advancements in transducer, front-end electronics and machine learning algorithms have made it possible to decode hand motion from forearm muscular signals and hence, control prosthetic hands [3]. Among the diverse range of sensing modalities (EIT [4], surface electromyography (sEMG) [5], ultrasound [6]) used to decode human hand motion, sEMG is the most common approach. In addition, hand gestures have been reported to be decoded from sEMG signals to a good level of accuracy [6].

However, there are many challenges and limitations associated with using sEMG. For example, sEMG signal quality can be significantly affected by external factors such as poor skin contact, environmental electronic interference, and motion artifacts [6]. Moreover, the shallow depth of recording (~1 cm below skin surface) is a fundamental limit-

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the cumbersome instruments reported in the literature severely degrade the user experience.

In this paper, a miniaturised solution is proposed in which a custom-built wearable bracelet (Fig. 1) houses eight analog front-end/transducer pairs distributed at different locations to target different sections of the forearm. The rest of the paper is organised as follows. Section II describes the overall system architecture, Section III discusses the analog front-end (AFE) ASIC, Section IV presents the experimental results and Section V concludes the paper.

II. OVERALL SYSTEM ARCHITECTURE

The system architecture is shown in Fig. 2. It consists of custom-built 1 MHz piezoelectric transducers (PZTs), AFE ASICs, battery and power management unit, analog-to-digital converters (ADCs), FPGA, and machine learning algorithms running on a laptop. The AFE ASIC consists of a transmit (TX) branch and a receive (RX) branch. In the TX branch, the pulser is controlled by the external FPGA to drive the PZTs with high-voltage (HV) square waves to generate sufficient acoustic pressure for penetrating 3 - 5 cm below the skin surface. In the RX branch, there is a transmit/receive (T/R) switch for the protection of the RX circuits which are designed with low-voltage (LV) transistors that are susceptible to damage by HV pulses coupled from the pulser. The RX branch also contains a programmable gain amplifier (PGA) with 3 equally spaced gain levels for time-gain compensation. After the PGA, the amplified signals are digitised off-chip for the subsequent digital processing.

The digitised data from the ADC is first pre-processed before being fed into a machine learning algorithm. Specifically, the raw data must be i) trimmed to remove noisy and non-useful samples, ii) Gaussian filtered and applied to a Hilbert transform function (envelope detection), iii) windowed for RMS calculation, and iv) first 100 principal components extracted and sent to linear regressor for hand kinematic tracking [2].

III. ANALOG FRONT-END DESIGN

A. Pulser

The pulser circuit is designed to drive the PZT with 1 MHz, 30 V_{pp} square waves. The architecture of the pulser circuit is shown in Fig. 3(a). The pulser contains a floating level shifter, tapered buffers, and a class D output stage (M_1 and M_2). By turning on M_1 or M_2 at the class D output stage, the output swings from the HV rail (30 V) to ground, generating a 30 V_{pp} square wave signal. As the pulser is designed to drive a large capacitive load, M_1 and M_2 in the class D output stage must be sized sufficiently large. M_1 and M_2 will generally dominate the area of the pulser. Tapered buffers are used to drive the large M_1 and M_2. M_3 is an N-type LDMOS and can be driven by a 0 – 3.3 V input signal from the external FPGA. However, to drive the P-type LDMOS M_4, the 0 – 3.3 V input signal is level shifted to 26.7 V – 30 V, implemented by the floating level shifter.

The floating level shifter shown in Fig. 3(b) is adapted from [10]. The floating level shifter consists of two complementary branches; its operation can be analysed easily from its half-circuit. When V_{in} goes high, M_7 conducts, whereas M_8 is turned off. With M_7 turned on, the source voltage of M_5 is pulled down toward V_{SSP}. The source volta-

\[ V_{SSP} = \text{Floating Level Shifter} \]

\[ V_{out} = \text{Level Shifter to drive high side output PMOS. Thick drain devices refer to 45 LDMOS whereas standard NMOS symbol refers to a deep N-well 3.3 V transistor.} \]

\[ V_{in} = \text{Pulser to drive the PZT. (a) Floating level shifter-based pulser to drive the PZT. (b) Level shifter to drive high side output PMOS. Thick drain devices refer to 45 LDMOS whereas standard NMOS symbol refers to a deep N-well 3.3 V transistor.} \]

\[ V_{ds} = \text{Folded-cascode amplifier.} \]
The PGA amplifies the received ultrasound signals with three programmable gain levels for processing by the ADC. The PGA is a single-ended voltage amplifier, unlike transimpedance amplifiers commonly reported in the literature. This is because the custom-built PZTs have a relatively low impedance value of ~ 2 kΩ at 1 MHz. Considering the low transducer impedance, it is desirable to design a voltage amplifier with an input impedance several orders of magnitude larger than 2 kΩ to read out a signal with minimal loading.

Differential amplifiers have the advantages of lower harmonic distortion and better power supply rejection. However, harmonic distortion and power supply rejection are not the most critical specifications in this application and their design requirements can be relaxed. Therefore, in this design, a single-ended implementation has been chosen considering the inherently single-ended nature of the PZT (all transducers share a common ground). In addition, a single-ended amplifier is less expensive in terms of both power and die area.

The PGA schematic in Fig. 2 has a switchable capacitor network to realise different gain levels. Switch S3 is turned on during the TX phase to place the amplifier in unity-gain feedback and force the common-mode voltage at the inverting input to be equal to 0.9 V. In the RX phase, S3 is turned off but the common-mode voltage is retained at the inverting input and the PGA’s operating conditions are well established. The core voltage amplifier in the PGA is a folded-cascode op-amp shown in Fig. 4.

C. Transmit/Receive Switch

In this application, the transducers are driven with unipolar pulses and the T/R switch only needs to provide unidirectional isolation. This greatly reduces the design complexity of the T/R switch. The series-shunt topology [11] in Fig. 5 is adopted. During the TX phase, the PGA circuit should be isolated from the TX pulses. Therefore, M1 and M2 will be turned off and M3 turned on to shunt the PGA input to ground. During the RX phase, M1 and M2 conduct, whereas M3 is turned off.

The two most important performance parameters of the T/R switch are on-resistance ($R_{on}$) and off-state isolation. It is desirable to have a low $R_{on}$ to minimize the impact of noise impact on the PGA side. In general, in order to achieve a low $R_{on}$, wide devices should be used. However, this would lead to significant parasitic capacitances, which would degrade the off-state isolation since there would be more signal leakage through these parasitic capacitances [11]. As a balanced trade-off, $R_{on}$ was designed to be smaller than 100 Ω. The measured $R_{on}$ of the T/R switch is 96 Ω.
The ASIC occupies 2.3 mm × 4.3 mm in a 0.18 μm HV-BCD process as seen in Fig. 6. The pulser circuit was electrically characterised with a 130-pF capacitive load mimicking the transducer capacitance. The pulser circuit was configured to drive this load with a 1 MHz, 30 Vpp square wave. The measured output voltage waveform of the pulser is shown in Fig. 7(a). The pulser circuit dissipates a power of 174.5 mW and has a rise/fall time of 86.4/74.4 ns. The measured frequency response of the PGA at different gain settings is shown in Fig. 7(b). It exhibits a bandwidth of 2.74 MHz and an input-referred noise of 23.6 μVrms integrated from 0.5 MHz to 1.5 MHz.

The performance of the ASIC has also been characterised in the acoustic domain, as summarised in Fig. 8 and Fig. 9. Fig. 8(a) depicts the acoustic experimental setup for the pulser, in which a hydrophone is placed at a very close distance (several mm) from the transducer to measure the transmitted acoustic pressure. The measured pressure values in Fig. 8(b) and Fig. 8(c) agree well with expectations. Fig. 9(a) shows the acoustic experimental setup for the PGA, in which one PZT is driven externally and the other PZT is connected to the ASIC. The amplified signal output in the voltage domain with the PGA set to maximum gain is shown in Fig. 9(b) and demonstrate successful receive functionality.

A performance summary and comparison against the state-of-the-art (SoA) is provided in Table I. The PGA power and noise performance is comparable to the SoA, although it must be stressed that this ASIC was developed for a novel application with its own unique design targets. The pulser’s power consumption is higher compared to the SoA. This is to be expected given that for this application, the transducer is a much higher capacitive load. From an overall system point of view, the operation of the pulser is heavily duty-cycled. The pulser’s contribution to the average power dissipation is actually small and acceptable.

### Table I. Comparison with State-of-the-Art Designs

<table>
<thead>
<tr>
<th>Technology</th>
<th>This work</th>
<th>[12]</th>
<th>[13]</th>
<th>[14]</th>
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</thead>
<tbody>
<tr>
<td>0.18 μm HV BCD</td>
<td>0.18 μm HV</td>
<td>0.16 μm BCD-SOI</td>
<td>0.18 μm CMOS</td>
<td></td>
</tr>
<tr>
<td>Pulser output voltage</td>
<td>30 Vpp</td>
<td>30 Vpp</td>
<td>60 Vpp&lt;sup&gt;1&lt;/sup&gt;</td>
<td>13.2 Vpp&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td>Pulser frequency</td>
<td>1 MHz</td>
<td>3.3 MHz</td>
<td>2.5 MHz</td>
<td>5 MHz</td>
</tr>
<tr>
<td>Pulser power</td>
<td>174.5 mW</td>
<td>52.4 mW&lt;sup&gt;2&lt;/sup&gt;</td>
<td>-</td>
<td>12.8 mW</td>
</tr>
<tr>
<td>Rise/fall time</td>
<td>86.4/74.4 ns</td>
<td>-</td>
<td>72/72 ns&lt;sup&gt;3&lt;/sup&gt;</td>
<td>-</td>
</tr>
<tr>
<td>Transducer load</td>
<td>130 pF</td>
<td>40 pF // 80 kΩ</td>
<td>1.8 nF // 240 Ω</td>
<td>(3.87 kΩ + 0.7 MHz + 1.93 pF) // 25.2 pF</td>
</tr>
<tr>
<td>PGA gain</td>
<td>9.54 - 21.58 dB</td>
<td>96.6 dBΩ</td>
<td>23 - 33 dB</td>
<td>19 - 73 dB</td>
</tr>
<tr>
<td>PGA BW</td>
<td>2.74 MHz</td>
<td>5.2 MHz</td>
<td>2 - 4 MHz</td>
<td>13 MHz</td>
</tr>
<tr>
<td>PGA power</td>
<td>1.74 mW</td>
<td>14.3 mW (active power)</td>
<td>5.4 mW</td>
<td>0.93 mW&lt;sup&gt;4&lt;/sup&gt;</td>
</tr>
<tr>
<td>PGA input-referred noise</td>
<td>11.3 nV/√Hz @ 1 MHz</td>
<td>0.56 mA/v/√Hz @ 3 MHz</td>
<td>13 nV/√Hz @ 3 MHz</td>
<td>19.3 nV/√Hz @ 5 MHz</td>
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<sup>1</sup> Actual measured value. <sup>2</sup> Estimated from paper. <sup>3</sup> Including ADC.

### V. Conclusion

A four-channel AFE ASIC for wearable A-mode ultrasound hand kinematic tracking has been presented. The ASIC occupies 2.3 mm × 4.3 mm in a 0.18 μm HV-BCD process. Preliminary electrical and acoustic experimental results have successfully validated the functionalities of the ASIC. Future work would involve human testing of the entire system (after implementation of the system in Fig. 1) to evaluate the effectiveness of A-mode ultrasound hand kinematic tracking.

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### References


