Energy Efficiency Bounds for Photonic Analog to Digital Converters

Callum Deakin, *Member, IEEE,* and Zhixin Liu, *Senior Member, IEEE*

***Abstract*—Many efforts have examined the prospect of photonic based analog to digital converters (ADCs) and shown that they can substantially outperform their electronic counterparts in terms of speed and resolution. In this paper we analyse the power consumption of photonic ADCs, which has not been meaningfully examined in previous literature yet is a critical figure of merit for analog to digital conversion. Firstly, we show that in a quantum noise limited regime photonic based converters cannot exceed the efficiency of conventional electronic designs in any reasonable operating environment. However, we further show that the exceptional performance of photonic ADCs at high frequencies may allow them to outperform high sampling rate electronic ADCs on a Schreier figure of merit basis, whose performance is limited by technological constraints such as clock jitter and the switching speed of the integrated circuit technology.**

***Index Terms*—analog-to-digital conversion, photonic analog-to-digital conversion, power consumption.**

I. Introduction

ANALOG to digital converters (ADCs) are ubiquitous devices that link our analog world to the vast digital infrastructure that underpins modern society. The speed, accuracy and efficiency of ADCs can profoundly impact system architectures and overall performance across a huge variety of applications, including optical and wireless communications, electronic warfare, medical imaging, and instrumentation [1].

Modern optical communications in particular typically use high speed ADCs with bandwidths of 10s of GHz and recently higher than 100 GHz [2], and are increasingly demanding higher resolutions to enable high order modulation formats and maximise channel spectral efficiency [3]. On the other hand, wireless communications systems typically operate at much lower baudrates but with higher order modulation in the crowded radio spectrum, where using high speed ADCs has enabled software defined radio (SDR). SDR shifts much of the traditional front end analog processing, such as filtering, mixing and (de)modulation into the digital domain. Such an approach dramatically increases the flexibility and performance of wireless communications systems [4].

Both of these applications rely on ADCs that can digitise high bandwidth signals accurately (i.e. with high resolution), yet ADCs exhibit a well known speed-resolution tradeoff. Historically, the main limitation on the accuracy of high speed converters was the switching speed of the integrated circuit technology, such as InP or GaAs, while lower speed converters were typically limited by thermal noise [5]. However, progress in converter design has meant that for high speed ADCs the sampling clock jitter or comparator ambiguity is often the main culprit for this tradeoff [5], [6].

As ADC technology has approached these fundamental limits, many have suggested photonic based designs as a more radical change to ADC architecture [7]. The exceptionally low jitter of optical sources, along with the ability of photonic integrated circuits to handle extremely high bandwidth signals, would seemingly make optics the natural next step in ADC evolution. Indeed, a wide variety of published photonic ADC architectures have demonsrated performance well in excess of state of the art electronic ADCs (e.g. 7 bits effective number of bits (ENOB) at 40 GHz [8], [9]).

Despite this impressive performance there has been, to the best of our knowledge, little to no discussion of the power efficiency of photonic ADCs. Power dissipation and efficiency are important factors in determining the performance of ADCs [10], [11], especially in communications systems where power consumption is critical [12]. Indeed, the energy per bit transmitted is often considered the main determinant for the future growth of communications networks [13], [14], [15]. Within this paradigm, photonic ADCs will only thrive if they can, at a minimum, match the power efficiency of electronic ADCs. Therefore, assessing the power consumption and efficiency is essential to determining whether the impressive speed-resolution performance afforded by photonic ADCs can translate into real-world improvements in network capacity and efficiency in energy sensitive applications [16].

In this paper we estimate bounds for the energy consumption of a generalised class of photonic analog to digital converters, and compare the power efficiency with their thermal noise limited electronic counterparts. We further develop a practical model of power consumption in photonic ADCs, based on the main active components required, and show that photonic ADCs may outperform electronic designs at high frequencies due to their superior jitter performance.

The rest of the paper is organised as follows. Section II reviews the power consumption limits in electronic ADCs and typically used figure of merits to form a basis of comparison. Section III estimates a generic lower bound on the power consumption of photonic ADCs based on shot and thermal noise limits, while Section IV attempts a more realistic estimation based on a component-by-component analysis. Finally, we consider several case studies of published photonic ADC designs in Section V and estimate their achievable energy efficiency. A portion of this work was originally presented

C. Deakin was with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, UK. He is now with Nokia Bell Labs, Murray Hill, NJ 07974, USA. (e-mail: callum.deakin@nokia-bell-labs.com).

Z. Liu is with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, UK. (e-mail: zhixin.liu@ucl.ac.uk).

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as a conference presentation in [17].

II. Energy consumption in electronic ADCs

As ADC power consumption varies significantly with the resolution and bandwidth, it is only fair to make the comparison under the same bandwidth and resolution performance. To this end, we always relate power consumption to a specific bandwidth and SNR performance throughout this paper. The ultimate lower bound for ADC power consumption is often considered to be the minimum sampling power which is set by the thermal noise of the sampling capacitor [18], [19], [12]. For a sampling capacitor of capacitance C, the mean square voltage noise (power of the thermal noise) is

$$\overline{v_C^2} = \frac{k_B T}{C} \tag{1}$$

at temperature T, where k_B is the Boltzmann constant. A sine wave switching the sampling capacitor across the full scale voltage of V_{FS} will have RMS voltage $V_{\text{FS}}/2\sqrt{2}$, leading to a thermal noise limited SNR of

$$\text{SNR} = \frac{C V_{\text{FS}}^2}{8 k_B T} \tag{2}$$

This signal input to the ADC must charge the capacitor within a single sampling period, requiring a charge of CV_{FS} to be delivered every sampling period, and therefore a current of

$$I \geq f_s C V_{\text{FS}} \tag{3}$$

and a power of

$$P = I V_{\text{FS}} \geq f_s C V_{\text{FS}}^2 \tag{4}$$

$$\geq 8 f_s k_B T \times \text{SNR}. \tag{5}$$

by plugging in (2). This sets the minimum power dissipated to achieve a particular SNR at sampling rate f_s if the ADC is limited purely by thermal noise at the sampling capacitor. Equivalently, this also sets the effective number of bits (ENOB) or resolution of the ADC, which is directly defined by the SNR through the well known expression [20]

$$\text{SNR} = \frac{3}{2} \cdot 2^{2\times \text{ENOB}} \tag{6}$$

for a given power consumption and sampling rate. Clearly, choosing a higher value of capacitance will lead to lower noise contribution in (1) but also drive up the power consumption as defined by (3). Note that the bound of (5) is a general bound for analog circuits first noted in [21].

Throughout this paper we will consider only the fundamental stochastic noise sources and use the term SNR, although real ADCs often contain nonlinear distortions and so are characterised by the signal to noise and distortion ratio (SINAD or SNDR). In the absence of nonlinear distortions these terms are equivalent.

A. Figures of merit

Given that (5) suggests that power consumption in an ADC should be directly proportional to sample rate and SNR, a natural figure of merit for ADCs is

$$\text{FOM}_S = \frac{\Delta f \times \text{SNR}}{P} = \frac{f_s \times \text{SNR}}{2P} \tag{7}$$

which is known as the Schreier figure of merit [22], [10]. Δf is the Nyquist bandwidth, $2\Delta f = f_s$, which represents the maximum bandwidth that can be digitised by the ADC as per the Nyquist-Shannon sampling theorem. Strictly speaking the unit of FOM_S is per Joule (or dB/J in decibels) but it is the convention in ADC literature to drop the 'J' and simply write dB. We will follow this convention throughout this paper. Another commonly used figure of merit combining power dissipation, bandwidth and resolution is the Walden figure of merit

$$\text{FOM}_W = \frac{P}{f_s 2^{\text{ENOB}}} \tag{8}$$

which was chosen empirically based on experimental outcomes [1] and suggested that the power doubles for every effective bit (or $4\times$ increase in SNR). While this matched experimental outcomes for many years, the relation suggested by FOM_S is more consistent with higher SNR results and is better justified theoretically by the thermal noise limit in (5) [23], [10]. We will therefore focus on FOM_S throughout this paper.

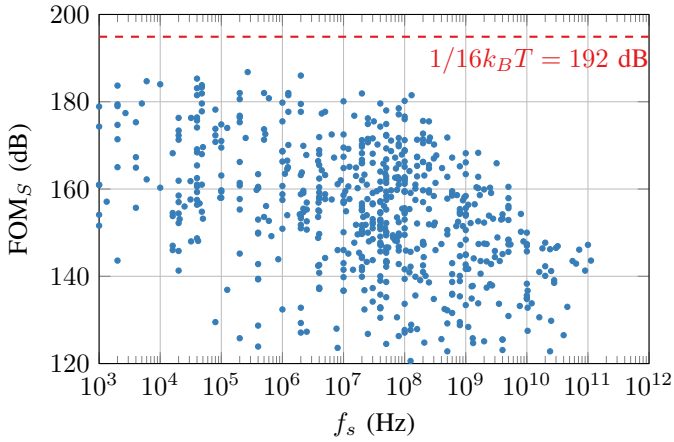

Fig. 1. FOM_S for ADC designs presented at the VLSI and ISSCC conferences 1997-2022, reproduced from [24]. The thermal noise limit, $1/16 f_s k_B T =$ 192 dB is calculated for T = 293 K.

As shown in Fig. 1, state of the art electronic ADCs can achieve $\text{FOM}_S > 185$ dB, irrespective of sampling rate, for $f_s < 10^8$ Hz (e.g. 186.8 dB [25]). This is about 7 dB below the thermal noise limited power efficiency of $\text{FOM}_S = 192$ dB set by (5). However for $f_s > 10^8$ Hz, the FOM_S declines at a rate of approximately 10 dB per decade for leading designs, where technological limitations such as jitter and comparator ambiguity begin to limit performance [5].

Many high speed ADC designs are interleaving designs [11], [26], [6]. A modification of FOM_S to M sub-ADCs

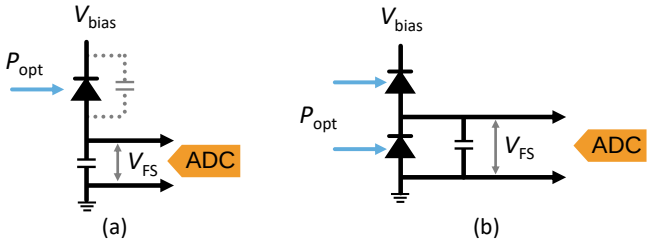

Fig. 2. Sub-receiver model: the illuminated photodiode switches an ADC input, represented as a capacitive load, to the full scale voltage V_{FS} [28]. This model can be applied to both (a) single and (b) balanced photodiode configurations.

with the same V_{FS} suggests that, in principle, interleaving allows for an arbitrary increase in bandwidth (sampling rate) without any corresponding penalty in power efficiency. For an interleaving ADC with M channels, we have an M times increase in f_s and an M times increase in power consumption, leading to

$$\text{FOM}_{S,\text{IL}} = \frac{Mf_s \times \text{SNR}}{2MP} \tag{9}$$

$$\text{FOM}_{S,\text{IL}} = \text{FOM}_{\text{S,sub-ADC}}. \tag{10}$$

Referring to Fig. 1, this suggests that we could simply take any ADC design from $< 10^8$ Hz as a sub-ADC in an interleaving design to achieve comparable power efficiencies at $> 10^8$ Hz. Clearly however, (9) does not account for any overhead associated with the interleaving structure, i.e.: signal buffering, routing, references, clocking and controls, the front-end interface to the input signal source, the digital back-end de-multiplexing, the power supplies for the different sections, and calibration circuitry [27]. Accounting for this overhead as P_0 instead gives

$$\text{FOM}_{S,\text{IL}} = \frac{Mf_s \times \text{SNR}}{P_0 + 2MP} < \text{FOM}_{\text{S,sub-ADC}} \tag{11}$$

Practically, as M increases, the analog input buffer must drive more sub-ADCs, thereby increasing front-end loading, which degrades input bandwidth (BW) and linearity, and increases power consumption [11], [26]. This means that in a practical system, P_0 is not strictly independent of M as (11) suggests and so M cannot be increased arbitrarily to minimise the impact of P_0. Besides, a large M introduces other issues such as the need for more complex digital signal processing and calibration, and an increase in footprint.

III. Fundamental Limits on Photonic ADC Efficiency

To estimate an equivalent lower bound to (5) for photonic ADCs we could consider the minimum optical power P_{opt}, typically from a pulsed laser source or a frequency comb, that we must generate in order to implement a photonic ADC. The signal to noise ratio of this optical source is fundamentally set by shot noise, which leads to an optical power

$$P_{\text{opt,sh}} \geq h\nu\Delta f \times \text{SNR} \tag{12}$$

required to achieve a certain SNR. For optical frequency ν, Planck constant h and bandwidth $\Delta f = f_s/2$.

In analogy to (2), where we derived a minimum ADC input capacitance required to achieve a certain resolution, we can also consider the thermal noise on a simple photodiode capacitor circuit used to detect the optical signal, as shown in Fig. 2(a). Note that the circuit in Fig. 2(a) is not strictly practical since the charged capacitor would be unable to discharge the accumulated charge without a load resistor, but it is useful model to consider fundamental limits [28]. Considering a capacitor driven by a photodiode, then the optical energy required to induce a voltage change, V_{FS}, equal to the full scale voltage of the ADC across this capacitor is

$$E_{\text{opt,th}} = CV_{\text{FS}}\frac{h\nu}{q\eta_q} \tag{13}$$

where q is the charge of an electron and η_q is quantum efficiency of the photodiode. Note this equation can also be expressed in terms of the photodiode responsivity, which is defined as $R = \frac{q\eta_q}{h\nu}$. This capacitance includes, at a minimum, the ADC load capacitance and the junction capacitance of the photodiode itself. To sufficiently charge this capacitor for a sampling rate of f_s requires optical power

$$P_{\text{opt,th}} = f_s CV_{\text{FS}}\frac{h\nu}{q\eta_q}. \tag{14}$$

We can then plug in (2) to relate the minimum optical power required to achieve a particular SNR for an ADC limited by the thermal noise of the photodiode-capacitor circuit shown in Fig. 2(a). By eliminating V_{FS}, we obtain

$$P_{\text{opt,th}} \geq f_s\frac{h\nu}{q\eta_q}\sqrt{8Ck_BT \times \text{SNR}}. \tag{15}$$

and by summing (12) and (15) a total optical power

$$P_{\text{opt}} \geq \frac{h\nu f_s}{2} \times \text{SNR} + f_s\frac{h\nu}{q\eta_q}\sqrt{8Ck_BT \times \text{SNR}}. \tag{16}$$

that is required to achieve a particular SNR at a sampling rate f_s, where the first term on the right is the shot noise limited power and the second term is the thermal noise limited power. Under the extremely generous assumption that we can generate this optical power with perfect efficiency and without any loss in the passive components[1], i.e. $P_{\text{opt}} = P$, the bound (16) can be compared directly to the thermal noise bound for electronic ADCs presented in (5).

Firstly, even if the receiver capacitance in (16) can be made arbitrarily small (i.e the limit $C \to 0$), the photonic ADC power consumption will still be shot noise limited, as we derived in (12). Under this scenario, we can obtain the condition under which the power consumption of a photonic ADC can be lower than the thermal noise-defined power consumption of an electronic ADC by combining (12) and (5)

$$h\nu < 16k_BT \tag{17}$$

[1]In reality impossible due to, among other things, non-radiative transition(s) in the laser source.

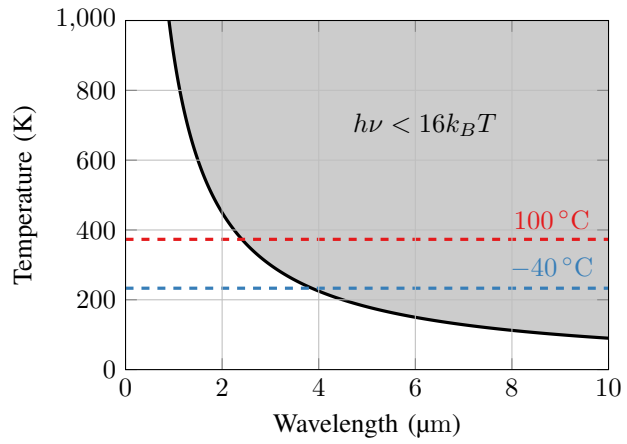

Fig. 3. Temperature-wavelength map with (17) plotted. The grey shaded region indicates the temperature-wavelength combinations under which a shot noise limited photonic ADC can be more energy efficient than a thermal noise limited electronic ADC.

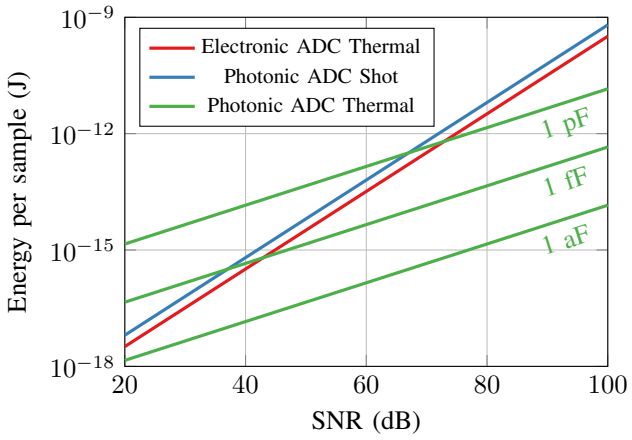

Fig. 4. Energy per sample for thermal noise limited electronic ADCs, shot noise limited photonic ADCs, and thermal noise limited photonic ADCs. This plot assumes $\eta_q = 1$, $\nu = 192$ THz, $T = 293$ K, and that the optical power is generated with perfect efficiency, .

where we have taken care to consider the factor of 2 difference between (12) and (5) due to the relation between sampling rate and bandwidth, $2\Delta f = f_s$. At $T = 300$ K this requires an optical frequency $\nu < 10^{14}$ Hz ($\lambda > 3\,\mu$m), far lower than the typical telecom operating frequencies of photonic devices. This is indicated in Fig. 3, where the grey shaded region indicates the temperature-wavelength combinations under which the condition (17) is satisfied and the shot noise limited photonic ADC can outperform a thermal noise limited electronic ADC. For any typical operating optical wavelength ($\lambda < 2\,\mu$m), this only occurs for unreasonably high operating temperatures (> 500 K). From this simple analysis it is clear that the high photon energy compared to the average kinetic energy imparted by the thermal noise, i.e. $h\nu \gg k_BT$, guarantees that electronic designs will be more power efficient than their photonic counterparts in quantum noise limited regimes.

Secondly, Fig. 4 highlights that the thermal noise contribution of the receiver will play a significant contribution in limiting the energy efficiency of photonic ADCs. For $\eta_q = 1$ and a commonly achievable photodiode junction capacitance of 1 pF, thermal noise dominates the energy consumption at SNR < 70 dB. Given that most photonic ADCs demonstrated so far operate with SNR < 50 dB, thermal noise likely places the fundamental limit on photonic ADC power efficiency and produces a much higher energy cost per sample at 1 pF than the equivalent thermal noise limited electronic ADC. Ensuring the photonic ADC power efficiency is purely shot noise limited for SNR > 20 dB requires a photodiode capacitance of 1 aF, which is several orders of magnitude beyond the current state of the art. While ~ 1 fF capacitance photodiodes are achievable [29], [30], [31], note as an example that in [30] the measured 8 fF photodiode capacitance is degraded by the parasitic capacitance of the wire bond (25 fF), which highlights how implementing such low capacitance photodiode in real circuits faces significant technical challenges.

IV. Practical Energy Consumption in Photonic ADCs

Photonic ADCs have been demonstrated with a wide variety of architectures [7]. Therefore, in order to estimate more practical bounds on the power consumption of photonic ADCs we consider two main classes of photonic ADCs, that we will label as type A and type B shown in Fig. 5:

1) **Type A** photonic ADCs use a pulse train from a mode locked laser, whose repetition rate is scaled up using wavelength demux/mux and delay line device. This pulse train is modulated with the signal of interest and then demuxed for parallel detection by sub-ADCs. Examples in this class are time-interleaving designs such as photonic sampling [8] and time stretch ADCs [32], [33].
2) **Type B** photonic ADCs take a continuous wave (CW) optical source which is split into signal and reference paths. The reference path generates a comb which is used as a reference against the input signal, while the input signal is modulated either directly onto the CW optical source [34] or onto another comb [9], [35]. The combined signals are demuxed and detected by parallel photodiode and sub-ADCs. Such designs are typically frequency interleaving.

Despite the apparent architectural differences between these two classes of photonic ADCs, in terms of power consumption they are quite similar when considering the minimum active components required to implement a photonic ADC. These components include a pulsed laser source (or a pulsed source generated from a CW source) as the optical sampling device, an electro-optic modulator to map the input signal onto the optical pulse train, followed by a bank of N channels containing a photoreceiver and electronic sub-ADC that detect subsets (either in the time [32], [8] or frequency [9], [34] domains) of the incoming signal in parallel at a fraction of the aggregate sampling rate. The signal is then reconstructed digitally to obtain the full rate signal at the much higher resolution offered by such optical techniques. The power consumption contribution of the required restitching digital

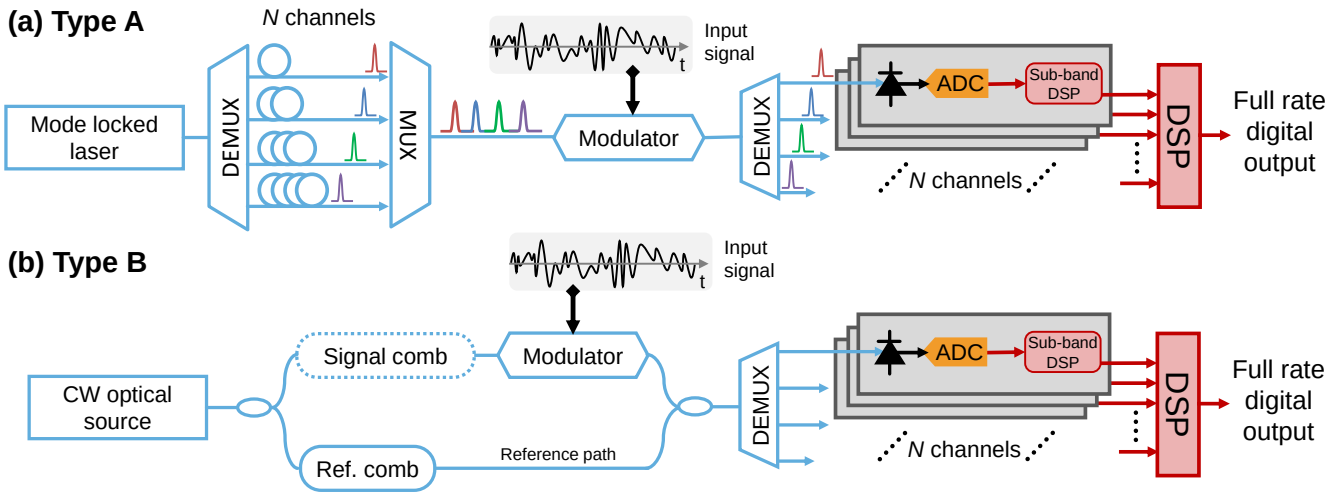

Fig. 5. Two generalised models of a photonic ADC. Despite their architectural differences, the main active active components between the two are essentially the same. ADC, analog to digital converter; DSP, digital signal processing.

signal processing (DSP) is not considered here since it is the same for interleaving electronic ADCs, which are the most common designs at high sampling rates, so is not relevant for comparison.

With this in mind, we first consider the power consumption of the essential active components required to implement a photonic ADC, which will form the basis of our power consumption estimates. Implications for power consumption arising from the architectural differences between type A and type B will be discussed later.

A. Power consumption by component

1) Optical source: For a optical source, the power consumption can be defined by the wall plug efficiency η_{WPE}, which describes the electrical power P_{src} required to generate an optical power P_{opt}

$$P_{\text{src}} = \frac{P_{\text{opt}}}{\eta_{\text{WPE}}} \tag{18}$$

CW semiconductor optical lasers often have wall plug efficiencies of around 30% and state of the art devices can achieve in excess of 50% [36], [37], [38]. The efficiency of pulsed sources is typically lower, with conventional micro-combs achieving up to 3.4% [39] and suitable mode locked laser sources achieving 1-2% [40]. However, recent novel micro-comb designs have shown pump conversion efficiencies of up to 86% [41], suggesting that suitable pulsed sources can be generated from pump diodes with little loss in system wall plug efficiency.

2) Electrical to optical conversion: Most high speed electro-optic modulators are travelling wave designs in which the electrode acts a transmission line [42], [16]. In this configuration, the modulator is designed as a transmission line with characteristic impedance Z_0, and so dissipates power [43], [44]

$$P_{\text{mod}} = \frac{V_{\text{RMS}}^2}{Z_0} \tag{19}$$

for driving signal with root mean square voltage V_{RMS}. Typically, the modulator used in a photonic ADC is a Mach Zehnder modulator (MZM) biased at the null which has optical field transfer function

$$M(x(t)) = \sin\left(\frac{\pi x(t)}{2V_\pi}\right) \tag{20}$$

for input zero-mean RF signal $x(t)$, assuming no insertion loss. For maximally efficient EO conversion, the power of $x(t)$ is adjusted such that $\max(|x(t)|) = V_\pi$, giving $V_{\text{RMS}} = \frac{V_\pi}{\sqrt{\text{PAPR}}}$ for a signal input with peak to average power ratio (PAPR).

The action of the modulator has two effects in terms of power consumption. Firstly, the power required to drive the modulator is directly related to the V_π through (19) to give

$$P_{\text{mod}} = \frac{V_\pi^2}{Z_0 \text{PAPR}}. \tag{21}$$

Secondly, it reduces the optical power (i.e. modulation loss) by a factor determined by the transfer function (20), which increases the optical power we need to generate in a shot or thermal noise limited scenario.

It is important to note that V_π and modulator bandwidth typically operate in a tradeoff, and so are often compared using the bandwidth/volt (or volt/bandwidth) metric. 10 GHz/V is typical for commercial bulk lithium niobate, with 30 GHz/V achievable for state of the art thin film lithium niobate [43]. We can therefore modify (21) to a function of this tradeoff

$$P_{\text{mod}} = \frac{(\Delta f V_{\Delta f})^2}{Z_0 \text{PAPR}} \tag{22}$$

for $V_{\Delta f}$ volts per Hz and a bandwidth of Δf. Assuming that V_π scales linearly with modulator bandwidth is generally a valid assumption if velocity mismatch is the limiting factor in the modulator bandwidth, as is typical for short electrode lengths (high bandwidth/V_π) [45].

3) Optical to electrical conversion: If the responsivity of the photodiodes is $R = \eta_q \frac{q}{h\nu}$ for quantum efficiency η_q, then the power supplied by the bias current is [16]

$$P_{\text{PD}} = \eta_q \frac{q}{h\nu} V_{\text{bias}} P_{\text{opt}} \tag{23}$$

which is the minimum power consumption of the OE conversion stage for optical power P_{opt} incident on the photodiode. This excludes the contribution of any TIAs in the signal path. Note that if the total optical power is P_{opt}, then the optical power per photoreceiver is P_{opt}/N and the total power consumption by the N photoreceivers (whether balanced, single ended or otherwise) will simply be

$$NP_{\text{PD}} = \eta_q \frac{q}{h\nu} V_{\text{bias}} P_{\text{opt}} \tag{24}$$

Note here that responsivity often operates in a tradeoff with the bandwidth of the photodiode, with typical maximum gain bandwidth products of 10^9 HzA/W [46].

4) Sub-ADCs: The contribution of sub-ADCs to the overall power consumption of the photonic ADCs can be considered in the same way their interleaving electronic counterparts. As described in (11), an interleaving ADC with M channels will have a total power consumption from sub-ADCs of MP along with additional interleaving overhead P_0. For photonic ADCs this additional overhead results from the optical source and EO/OE conversions described in the previous sections. The power consumption of the sub-ADCs used in any design can therefore be estimated from published electronic ADC results, such as those presented in Fig. 1, provided the sub-ADC results meets the sampling rate and resolution requirements defined by the photonic ADC architecture. As Fig. 1 shows, lower sampling rate ADCs are more efficient in FOM_S terms for $f_s > 10^8$ Hz, which may allow photonic ADCs to outperform the power efficiency of electronic ADCs if the photonic interleaving overhead P_0 is sufficiently small.

B. Overall power efficiency

Considering the aforementioned active components, we can derive an overall an expression for the energy per sample of a photonic ADC digitising an input signal defined only by its peak to average power ratio (PAPR)

$$P/f_s = \frac{P_{\text{opt}}}{f_s}\left[\underbrace{RV_{\text{bias}}\sin^2\left(\frac{\pi}{2\sqrt{\text{PAPR}}}\right)}_{\text{sub-receiver}} + \underbrace{\frac{1}{\eta_{\text{WPE}}}}_{\text{laser source}}\right] + \underbrace{\frac{f_s V_{\Delta f}^2}{4Z_0 \times \text{PAPR}}}_{\text{modulator}} \tag{25}$$

Note that the modulator nonlinearity, as represented by the sin function in (25), can be compensated through simple digital compensation [47], [48]. For a lower bound, the optical power P_{opt} can be obtained through the combined shot and thermal noise limits we obtained in (16).

Fig. 6 shows how the modulator limited energy per sample increases linearly with sampling rate for a fixed GHz/V and PAPR, under the assumption that the modulator V_π increases linearly with bandwidth. Furthermore, while Fig. 6 shows a higher PAPR signal reduces the modulator power consumption, this increases the optical loss and therefore the required optical power.

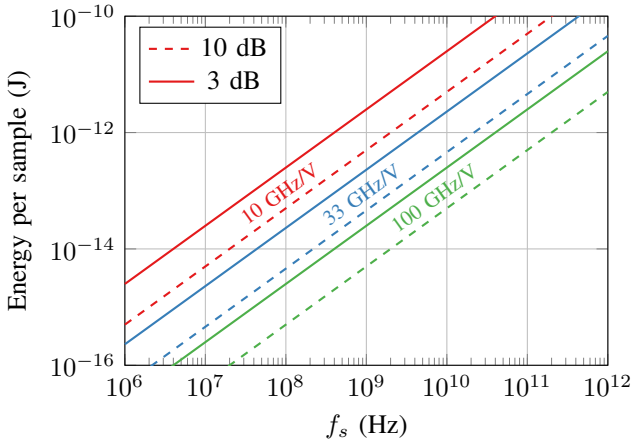

Fig. 6. Energy per sample scaling with sampling rate for photonic ADCs for modulator limited scenarios, for different PAPR values: 10 dB, and 3 dB are plotted with dashed and solid lines respectively. Nyquist rate sampling is assumed, with $Z_0 = 50\ \Omega$.

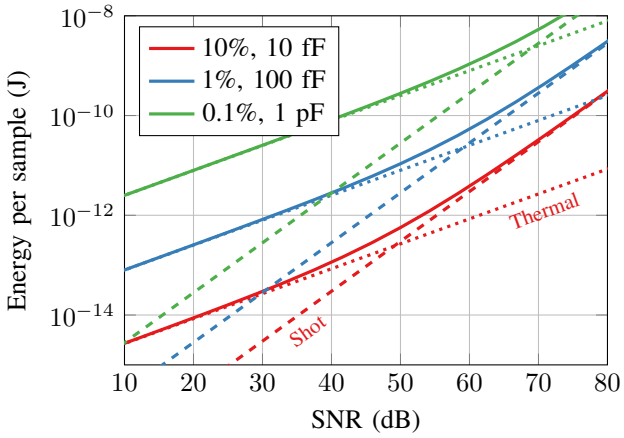

Fig. 7. Optical power limited energy per sample scaling with SNR: dashed and dotted lines indicate the shot and thermal noise limits respectively for each case. Nyquist rate sampling is assumed, with $Z_0 = 50\ \Omega$, $V_{\text{bias}} = 3$ V, $R = 1$ A/W, $\nu = 192$ THz, $T = 293$ K, PAPR = 10 dB.

Fig. 7 plots how the energy per sample changes with the shot and thermal noise limited SNR of the photonic ADC. A higher SNR increases the energy per sample due to the increase in optical power needed to overcome shot and thermal noise, as per (12) and (15). Three cases are plotted: $\{\eta_{\text{WPE}} = 0.1\ \%$, $C_{\text{Rx}} = 1$ pF$\}$ (green), $\{\eta_{\text{WPE}} = 1\ \%$, $C_{\text{Rx}} = 100$ fF$\}$ (blue) and$\{\eta_{\text{WPE}} = 10\ \%$, $C_{\text{Rx}} = 10$ fF$\}$ (red) with the limits imposed by shot and thermal noise indicated for each case. Clearly, shot and thermal noise limit are the dominant contributions to the energy per sample for high and low SNR respectively, with the cross over point between shot and thermal noise shifting to lower SNR as the wall plug efficiency improves. If wall plug efficiencies of $> 10\%$ can be achieved, then Fig. 7 shows that shot noise will limit the energy per sample at SNRs typically achieved for the best performing photonic ADCs (40-50 dB).

C. Differences between type A and type B

The differences in power efficiency between type A and type B photonic ADCs as sketched in Fig. 5 becomes apparent once the optical to electrical conversion method is considered. Almost all successful demonstrations of photonic ADCs use balanced detection as shown in Fig. 2(b). In a type A photonic ADC, balanced detectors are typically use to detect the complimentary outputs of the modulator [8] to reject common mode noise, cancel even order nonlinearity and, importantly for power consumption, enable efficient use of the optical power.

For type B photonic ADCs however, balanced detectors are used to detect the amplitude (or a coherent receiver to detect both in-phase and quadrature amplitude components) of the modulated signal and enable the shifting of spectral slices required for frequency interleaving designs [35], [34]. Since now only the fraction of the total optical power sent through the signal branch is modulated with the input signal, the shot and thermal noise limits in (12) and (15) respectively must be modified. Assume that a fraction α of the total generated optical power is sent to the signal branch, such that

$$P_{\text{sig}} = \alpha P_{\text{opt}} \tag{26}$$

$$P_{\text{ref}} = (1-\alpha) P_{\text{opt}} \tag{27}$$

for the optical power in the reference branch P_{ref}, optical power in signal branch P_{sig} and where $0 < \alpha < 1$. This modifies the shot noise limit (12) to

$$P_{\text{opt,sh}} \geq \frac{h\nu\Delta f}{4\alpha(1-\alpha)} \times \text{SNR} \tag{28}$$

since the current on the balanced receiver is proportional to $2\sqrt{P_{\text{ref}}P_{\text{sig}}}$ rather than simply the overall optical power [49]. On the other hand, the thermal noise limit (15) is also modified to

$$P_{\text{opt,th}} \geq f_s \eta_q \frac{h\nu}{q} \sqrt{\frac{2Ck_BT}{\alpha(1-\alpha)} \times \text{SNR}}. \tag{29}$$

It is clear that for type B photonic ADCs, minimising the fundamental bound on power consumption requires maximising the value of $\alpha(1-\alpha)$, which occurs for $\alpha = 0.5$, i.e. when optical power is split evenly between the two branches. In this case the type B limits reduce back to the originally derived limits (12) and (15).

D. Impact of jitter

Many photonic ADCs are designed to exploit the extremely low jitter of optical sources, and the impact of jitter on photonic and electronic ADCs has been extensively discussed in previously [1], [10], [7], [8], [50], [51]. However, it is also interesting to consider how jitter interacts with energy consumption. In a jitter limited ADC, the SNR follows the well known upper bound of [52], [53]

$$\text{SNR} = \frac{1}{(2\pi\sigma f_{\text{in}})^2} \tag{30}$$

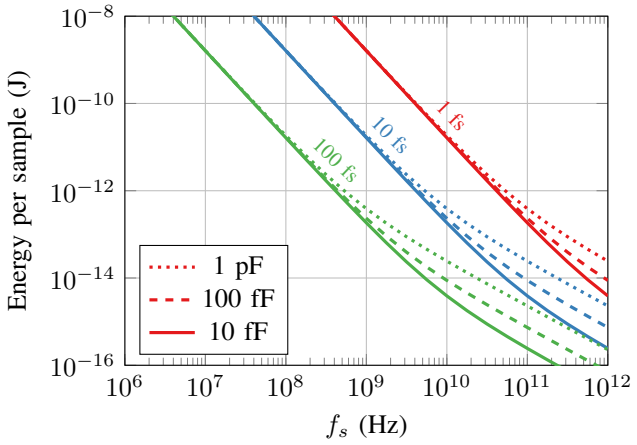

Fig. 8. Energy per sample scaling with sampling rate for photonic ADCs for jitter limited scenarios, for different photodiode capacitances: 1 pF, 100 fF, and 10 fF are plotted with dotted, dashed and solid lines respectively. Nyquist rate sampling is assumed, with $\eta_q = 1$, $\nu = 192$ THz, $T = 293$ K.

for root-mean-square jitter σ and input frequency f_{in}. The frequency f_{in} is typically assumed to be $f_s/2$, the highest frequency an ADC can unambiguously digitise. A decrease in jitter causes a corresponding increase in power consumption since more accurate sub-ADC digitisation is needed and therefore an increase in the optical power required to overcome shot and thermal limits on SNR. Note that this jitter trend is also true for high speed electronic ADCs, where the more accurate digitisation enabled by lower jitter also leads to an increase in power consumption [18]. The degradation of SNR caused by jitter can also cause a drop in FOM_S at higher frequencies, as illustrated by Fig. 1.

This is plotted in Fig. 8, which plots the jitter limited energy per sample as a function of sampling rate. Specifically, the jitter limited energy per sample is derived by substituting the value of SNR from (30) into (16), obtaining the shot and thermal noise limited energy consumption required for an ADC to be jitter limited. Energy per sample actually decreases with increasing frequency for a fixed jitter since the jitter limited SNR is lower, requiring less optical power to reach the required SNR. At low frequencies, the energy per sample is shot noise limited and so the different values of capacitance converge for a given jitter.

The physical origin of this jitter in any specific photonic ADC implementation can arise from a number of different sources, which may be optical or electronic in origin. For example, pulse to pulse timing variations of a mode locked laser [8], the jitter of an electronic oscillator used to create a frequency comb [35] or the thermo-refractive fluctuations of a microring resonator used to generate a frequency comb [34].

V. Case Studies: Comparison between Electronic and Photonic ADCs

We can use (25) to estimate, for photonic ADCs in general, a range for the achievable FOM_S given the sources of power consumption we described in the previous section. In Fig. 9 we plot FOM_S for varying sampling rate f_s, as in Fig. 1, but add estimations for photonic ADCs. The red shaded

region indicates a generalised estimation of the achievable FOM$_S$ for photonic ADCs calculated from (25), with optical power defined by (16), based on the best and the worst case parameters listed in Table I.

Red circles indicate the estimated FOM$_S$ for four specific photonic ADCs [8], [9], [32], [34], based on the published frequency/SNR result and best estimates of the power consumption of the components used. The parameters used for the component power consumption are listed in Table II. Where available, we have used the actual parameters from the published reference but in absence of the required data, we have used a reasonable estimate for the componenet parameter: where this is the case, the value is *italicised*. These particular papers were chosen as case studies for two reasons. Firstly, they are to the best of our knowledge the best performing photonic ADCs in terms of effective jitter and represent cases where photonic ADCs have outperformed electronic ADCs in terms of SNR (ENOB) at the target frequency. Secondly, they represent a diverse range of architectures including: photonic time-stetch (time-interleaving) [32], mode locked laser based photonic sampling (time-interleaving) [8], single frequency comb based broadband frequency interleaving [34], and dual frequency comb narrowband frequency interleaving [48].

In this exercise it is our goal to effectively estimate the overhead of the optical processing front end, i.e. P_0 in (11), and so the power consumption of the sub-ADCs is in each case inferred from the best reported electronic ADC research results at the requisite bandwidth and resolution. As opposed to using the power consumption of the commercially available ADCs used in the actual experiments, this also ensures a fair comparison with the plotted electronic ADC data from [24] (blue crosses). Specifically, for [8], [9], [32] this is FOM$_S$ = 168.2 dB at 1 GHz [54] (extrapolated to 5 GHz for [32]), and for [34] this is FOM$_S$ = 147.2 dB at 100 GHz [55] (extrapolated to 80 GHz).

Since these published photonic ADCs results were likely designed without regard for power consumption, we have also estimated the maximum achievable FOM$_S$ based on the minimum estimated power (i.e. using the 'best' parameters in Table I) required to achieve the presented result, which is indicated using an arrow for each result, and labelled as FOM$_S$ (potential) in Table II.

While even in the best scenario our estimates for photonic ADCs FOM$_S$ do not exceed the best published electronic ADC results for $f_s < 10^8$ Hz, the red shaded area in Fig. 9(a) clearly indicates that photonic ADCs may outperform their electronic ADC counterparts on an FOM$_S$ basis at higher frequencies. This can mainly be attributed to the outstanding jitter performance of the photonic ADCs. Maintaining however the power efficiency implied by (25) at high frequencies via low jitter sources may include significant technical challenges, although recent developments in integrated photonics have demonstrated microcomb sources with wall plug efficiencies up to 3.4% [39] on a hybrid III–V/Si$_3$N$_4$ platform along with highly efficient modulators exceeding 100 GHz/V in thin film lithium niobate [56], [43]. Indeed, recent fabrication of micro-comb sources with near unity pump conversion efficiency [41] and highly customisable spectral shapes [57] suggests that in the future the efficiency of comb sources may approach that of a CW laser source. The co- or hybrid integration of these technologies along with the required electronics and CMOS digital circuitry is essential for achieving the efficiencies speculated here, which may be enabled by the promising recent progress in integration of photonic components on silicon platforms [58].

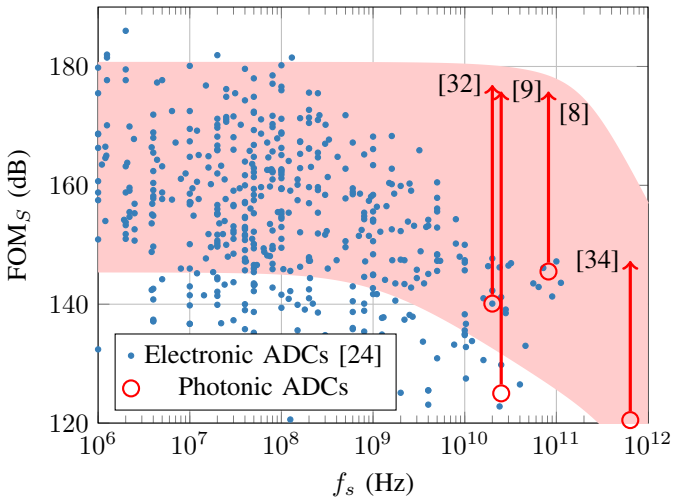

Fig. 9. FOM$_S$ estimation for photonic ADCs (red circles) compared to published results from electronic ADCs [24]. The red shaded area indicates the achievable FOM$_S$ for generalised photonic ADCs based on (25) and the parameters in Table I. The red arrows extending from the photonic ADC results indicate the maximum estimated FOM$_S$ for each architecture.

Parameter	Worst	Best
$1/V_{\Delta f}$	10 GHz/V	100 GHz/V
Jitter	1 ps	1 fs
Optical loss	20 dB	0 dB
PAPR	10 dB	3 dB
Z_0	50	50
η_{WPE}	1%	10%
R	0.5 A/W	1.25 A/W
V_{bias}	3 V	1 V
C_{Rx}	1 pF	100 fF

TABLE I
PARAMETERS USED TO PLOT RED SHADED AREA IN FIG.9

One additional observation from Table II is that the optical amplifiers consume a large fraction of the overall power. In these published experiments, the optical amplifiers are typically being used to compensate optical insertion losses from the discrete components used, which can often approach 30 dB. This is particularly acute in [34] where a large number of EDFAs are used, presumably to compensate chip coupling losses and filter insertion losses. On the other hand, [9] uses a single high power EDFA in order to generate two frequency combs via electro optic modulation using discrete modulators. Full system on chip integration or use of a more efficient comb generation can eliminate the need for optical amplifiers, and allow these systems to approach the efficiency indicated by the FOM$_S$ (potential).

Parameter	Time stretch [32]	TI [8]	FI, single comb [34]	FI, dual comb [9]
V_π	*3 V*	*4.2 V*	-	-
Modulation index	0.7	0.23	-	-
RMS drive voltage	*1.48 V*	*0.68 V*	*0.59 V*	2.2 V
Input drive power	**44 mW**	**9.3 mW**	**456 mW**	**100 mW**
Laser output power	*10 mW*	10 mW	*10 mW*	50 mW
Wall plug efficiency	*1%*	0.81%	*1%*	*1%*
Laser power consumption	**1 W**	**1.23 W**	**1 W**	**5 W**
Total optical amplifier output power	*200 mW*	*100 mW*	*800 mW*	5 W
EDFA wall plug efficiency [59]	*10%*	*10%*	*10%*	*5%*
Optical amplifier power consumption	**2 W**	**1 W**	**8 W**	**100 W**
R	*1 A/W*	0.6 A/W	*0.5 A/W*	1 A/W
V_{bias}	*3 V*	2.25 V	*2 V*	3 V
Optical power per receiver	-3 dBm	-8.8 dBm	*10 dBm*	0 dBm
Channels	2	157	4	25
Receiver power consumption	**3 mW**	**27 mW**	**40 mW**	**75 mW**
Sub-ADC bandwidth	5 GHz	524 MHz	80 GHz	500 MHz
Sub-ADC power consumption	*23.6 mW*	*3.98 mW*	*249 mW*	*3.8 mW*
No. of sub-ADCs	2	157	4	25
Total sub-ADC power	**47.1 mW**	**625 mW**	**996 mW**	**95 mW**
Total power consumption	**3.1 W**	**2.89 W**	**10.5 W**	**105.27 W**
SNR	45.1 dB	44 dB	15.7 dB	44 dB
f_s (full bandwidth)	20 GSa/s	82 GSa/s	640 GSa/s	25 GSa/s
Analog bandwidth	10 GHz	41 GHz	320 GHz	40 GHz
FOM$_S$	**140.1 dB**	**145.5 dB**	**120.5 dB**	**125.0 dB**
FOM$_S$ (potential)	**176.9 dB**	**175.8 dB**	**147.3 dB**	**175.8 dB**

TABLE II
ESTIMATED POWER CONSUMPTION FOR PUBLISHED PHOTONIC ADC EXPERIMENTS. ESTIMATED VALUES ARE ITALICISED.

VI. CONCLUSION

We model and estimate the theoretical power dissipation bounds for photonic ADCs. In analogy to the thermal noise bound for electronic ADCs, we showed that the shot noise and photodiode thermal noise provide equivalent bounds for photonic ADCs and suggest that in a quantisation noise limited regime they cannot exceed the power efficiency of electronic ADCs in any reasonable operating environment. We also derived a model for practical energy consumption by examining the power consumption of the minimum active components required to implement a photonic ADC, and applied this model to photonic ADC experiments reported in the literature. Although our power consumption estimations of the considered case studies are not favourable, estimating the best case power consumption using state of the art components suggests that photonic ADCs may outperform their electronic ADC counterparts in high frequency regimes due to their exceptional jitter performance.

It is important to emphasise that the power consumption estimates provided here do not claim to be definitive or highly accurate estimations of the photonic ADCs referenced here, nor that the models presented can be used to calculated the actual power consumption of a fully realised photonic ADC. Instead, the goal of this paper is provide a power consumption benchmark against which to measure future photonic ADCs, as well as a fundamental comparison between photonic and electronic ADCs on an energy efficiency basis, which should be considered when designing photonic ADCs going forward in addition to the frequently referenced speed and resolution metrics.

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