This article has been accepted for publication in IEEE Transactions on Nanotechnology. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2023.3284144

Unipolar potentiation and depression in memristive devices utilising the subthreshold regime

Daniel J. Mannion[1*], Viet Cuong Vu[1], Wing H Ng[1], Adnan Mehonic[1], Anthony J. Kenyon[1]
[1]*Department of Electronic & Electrical Engineering*
Univeristy College London (UCL)
London, United Kingdom
[*]Correspondance Address: daniel.mannion.13@ucl.ac.uk

***Abstract*— We present a resistance switching device that exhibits analogue potentiation and depression of conductance under the same voltage polarity. This contrasts with previously studied devices that potentiate and depress under opposite polarities. We refer to this mode of operation as the subthreshold regime due to it occurring at voltage or current biases that are insufficient to produce discrete or non-volatile switching. This behaviour has the potential to reduce the complexity of neuronal and synaptic circuitry in neuromorphic computing by removing the need for voltage pulses of both positive and negative polarities. The characteristically long timescales may also help replicate bio-realistic timings. In this paper, we detail how to induce this unique behaviour, how to tune its properties to a desired response, and finally, we demonstrate one potential application.**

Keywords*— neuromorphic, synapse, resistance switching, memristor, ReRAM, current transient, silicon oxide, subthreshold regime.

I. Introduction

We are increasingly taking inspiration from biological examples in pursuit of lower power consumption for machine learning hardware [1]. Nanoscale devices with nonlinear conductance and hysteretic effects, such as memristors [2], [3] and more general resistance switching devices, have played a significant role in this pursuit. One example is their use as artificial synapses, where they replicate the learning rules observed in biological synapses and enable computation when integrated within biologically-inspired networks such as spiking neural networks.

Potentiation and depression are two fundamental processes that occur within synapses and are the foundations of more complex learning rules. During potentiation a synapse's conductivity increases and during depression decreases. Changes caused during potentiation or depression can also vary in volatility: they may persist and be long-term (Long Term Potentiation (LTP) and Long Term Depression (LTD)) or their effects can reverse over time and be considered short-term (Short Term Potentiation (STP) and Short Term Depression (STD)).

These fundamental synaptic behaviours have been replicated in a wide variety of electronic devices, predominantly memristors or ReRAM devices [4] which have been shown to exhibit potentiation and depression over both long and short timescales. However, in these examples, potentiation and depression often occur in opposite polarities. This imposes the requirement that potentiating and depressing inputs must be able to source spikes of different polarities, potentially increasing the complexity of the neuron circuits driving the synapses. It would be preferable to build networks that can operate on single rail power supplies, in line with the majority of today's digital electronics. This would require devices in which potentiation and depression can occur due to a single polarity of voltage pulse. There are examples of devices exhibiting potentiation and depression within the same voltage polarity such as complementary ReRAM [5] or unipolar ReRAM devices [6]. However, these exhibit discrete binary switching behaviours as opposed to the more biologically analogous analogue changes in resistance.

Here, we introduce a device capable of exhibiting both analogue potentiation and depression under the same voltage polarity and amplitude. It is based on a behaviour previously referred to as the *current transient phenomenon* that has historically been used to estimate the mobilities and activation energies of defects within oxides [7], [8] where a Space-Charge-Limited-Current (SCLC) model is employed to explain the behaviour [9][10].

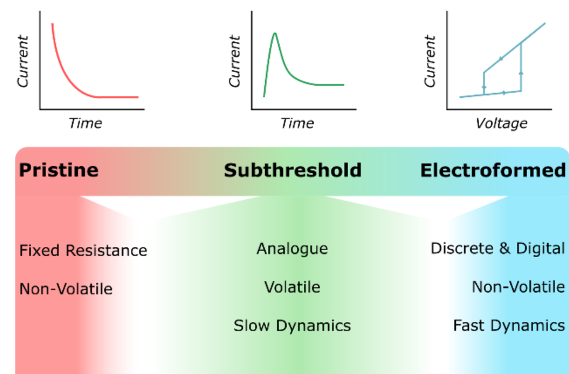

Fig. 1. **Inducing a spectrum of behaviours in metal-oxide MIM devices.** Metal-Insulator-Metal devices demonstrate a range of behaviours based on the way in which they have been electrically stressed. In this paper, we document a state found inbetween the extremes of the pristine and electroformed states. This intermediate state reveals qualitatively different behaviours compared to what is observed at either of the two extremes. We refer to this as the subthreshold regime.

The Space Charge Limited Current (SCLC) model describes a generic space charge within an ideal insulator. This model was later linked to oxygen vacancy migration in thin films [8] where the space charge in question is assumed to be charged oxygen vacancies. It is argued the drift of charged defects under an applied bias causes an ionic current in addition to any electronic current. The migrating oxygen vacancies are blocked by the electrical contact at one side and accumulate. This accumulation forms a Coulombic repulsion impeding further migration in turn reducing the ionic current as it begins to work against itself. However, there is not yet a consensus on the validity of the SCLC model in this context.

Authorized licensed use limited to: University College London. Downloaded on June 12,2023 at 10:05:38 UTC from IEEE Xplore. Restrictions apply.
© 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

This article has been accepted for publication in IEEE Transactions on Nanotechnology. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2023.3284144

An alternative explanation involves migrating oxygen vacancies modulating the electronic conduction via changes in interfacial electrostatic barriers [11]. Other studies have found evidence to support this alternative explanation albeit for changes in bulk conduction as opposed to at the interface. For example, electronic traps with activation energies of 0.18-0.3eV have been detected in titanium oxide films exhibiting the current transient phenomenon [12]. This led the authors to conclude oxygen vacancy migration caused changes in electron/hole concentrations in turn modulating bulk conductivity. A further extension to these existing arguments is that changes in conductivity are occurring at both the interface and bulk simultaneously [13].

To summarise, there are a number of physical explanations for the current transient phenomenon. All consider there to be some charged defect migrating within the oxide (often oxygen vacancies), where they differ is on the effect this migration has. The general trend has been towards an electronic explanation whereby the migrating defects modulate the electronic conductivity at either a metal-oxide interface, within the bulk of the oxide thin film, or at both simultaneously.

However, we present this behaviour, which we refer to as the subthreshold regime, in a new context: as a useful computational device, rather than a method of characterisation. In previous work, we employed this behaviour to carry out computation - for example, to detect edges within spike-encoded images [14]. But there are other uses for this regime. For example, the long timescales (seconds to minutes) of the current transients will have uses when biological timescales are important, such as in replicating eligibility traces [15], [16], or in habituation and homeostasis applications which we discuss in a later section. This current transient behaviour has been observed in a range of oxides such as barium strontium titanite systems [8], [7], [11], [17], hafnium oxide [18], tantalum oxide [19]. Here we present it in silicon oxide.

The subthreshold regime appears to be a generic behaviour of metal-insulator-metal (MIM) devices. This suggests that the behaviour may be reproducible in devices already in wide use today, leading to the concept of a single device capable of producing a wide range of behaviours based on the manner and degree to which it is stressed, as illustrated in Fig. 1.

In this paper, we document the subthreshold regime under a DC step potential and then replicate the response with spike trains, suggesting its suitability for spiking neural networks. We then show how the balance between potentiation and depression can be tuned by two means: varying the amplitude of voltage spikes and by electrically stressing the sample. Finally, we demonstrate one potential application which uses the subthreshold regime to replicate habituation and homeostatic behaviours.

II. Methods & Device Fabrication

A. Device Fabrication

The device has a metal-insulator-metal structure as illustrated in Fig. 2 and was originally developed for binary resistance switching applications [20]. The bottom metal contact is a molybdenum film of 280nm thickness deposited via magnetron sputtering. The insulator layer is a slightly sub-stochiometric and amorphous layer of silicon oxide with a thickness of 35nm, deposited via RF magnetron sputtering. The top metal contact is a 115nm thick gold film deposited via e-beam evaporation through a contact mask. The shape of the top contact is a square of $200 \times 200\mu m$ defining the active area of the device. To improve adhesion of the gold contact, a 3nm layer of titanium was deposited prior to the gold evaporation. This also serves as a gettering layer to seed the oxide layer with oxygen vacancies.

Fig. 2. **Device Structure.** The device studied in this paper has a metal-insulator-metal structure. The two electrical constacts are the molybdenum bottom contact and the gold top contact. A 3nm titanium buffer layer is depostited prior to the depostion of the gold, to improve the adhesion of the top contact and to serve as an oxygen getter.

B. Electrical Stressing

After fabrication the device must go through an electrical stressing process in order to enter the subthreshold regime. While this is may appear similar to the electroforming process typical of resistance switching and memristor devices [21], it involves driving a constant current through the device as opposed to the more common approach of voltage sweeping., and does not lead to an abrupt change in device conductance.

Devices are stressed by grounding the molybdenum contact and applying negative currents to the gold contact, implying electron injection at the gold contact and hole injection at the molybdenum contact. The magnitude of the constant current is varied depending on the desired behaviour, but in this work is between $-0.1\mu A$ to $-100\mu A$ and is applied for 100 seconds. During stressing, the voltage induced across the device gradually reduces, eventually approaching a steady state value, as shown in Fig. 3.

The behaviours presented in the following sections are not immediately present after undergoing this stressing procedure. Instead, the stressed devices are left to rest for approximately 24 hours before such behaviours emerge. We assume this is due to a significant redistribution of charged defects occurring during the stressing process, which must be allowed to return to a resting distribution.

Although this stressing procedure provides a degree of tunability to the devices, which is discussed in Section IIB, it does also bring limitations. For example, integrating the circuitry required for stressing could potentially negate our claimed benefits of requiring only single rail power supplies. Equally, the resting period after stressing introduces an additional step to fabricating the circuit.

Crucially, however, the stressing process is not a necessity. Most studies of the current transient phenomenon described in this paper undergo no electrical stressing but exhibit the behavior immediately after fabrication [7]. This suggests that a desired response could be achieved through fabrication. That said, the stressing procedure presented in this paper has benefits during the development and testing of novel circuits as it enables researchers to tune behavior electronically without the need to refabricate devices. This is discussed later in the paper.

III. Results & Discussion

A. Combined Potentiation and Depression

The presence of both potentiation and depression is best demonstrated by applying a step potential to the device.

Authorized licensed use limited to: University College London. Downloaded on June 12,2023 at 10:05:38 UTC from IEEE Xplore. Restrictions apply.
© 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

This article has been accepted for publication in IEEE Transactions on Nanotechnology. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2023.3284144

Applying a negative step potential to the device's top gold electrode results in transient current as shown in Fig. 4. Initially a fast potentiation is observed occurring on the order of seconds; however, this very quickly reaches a peak beyond which the competition with depression begins to dominate the device conductance, eventually pushing the conductance beneath its initial value. This is a slower process that continues for tens of seconds. Changes in conductance persist for tens of minutes.

The transient current response of the device to a range of DC voltages is plotted in Fig. 4. For each voltage the mean of 3 trials is plotted, with error bars indicating the maximum and minimum of all trials. At lower voltages, i.e. -1V, negligible depression is observed, but it becomes progressively more prominent at larger voltages. Potentiation is observed for all voltages, including -1V, and appears to accelerate with increasing voltage.

It is interesting to note the repeatability of the device's response as shown in Fig. 5 where 132 current transients which were induced by applying a step potential of -0.8V to the gold electrical contact are collated. While resistance switching devices often exhibit variable and stochastic responses [22] we can see from the range (light grey), and the 5% and 95% percentiles (dark grey), that the device's behaviour is repeatable and predictable. Note this is only true if the device is allowed to fully relax between trials. This is evident in Fig. 5 from the range having a larger spread than that of the 5% and 95% percentiles which is caused by the first three trials exhibiting larger currents due to a settling which occurs across the many trials.

Relaxation is achieved by grounding both electrical contacts and leaving the device to rest. The reset process is slow, and a rest time of 1 hour is needed to ensure complete relaxation. However, relaxation can be accelerated by applying a positive potential to the gold contact instead of grounding it.

While this behaviour is evident during step potentials, neuromorphic synapses are often operated using pulse trains [23]. It is therefore important to establish if the same behaviour can be replicated when a series of voltage pulses are applied to the device. We show this is indeed the case by applying a series of gaussian pulses to the device. The pulses have a full width half maximum (FWHM) of 20ms, an amplitude of -3V, a period of 300ms and are again applied to the gold contact. Note, while the pulses have a negative amplitude the device current has been inverted in the following figures for clarity.

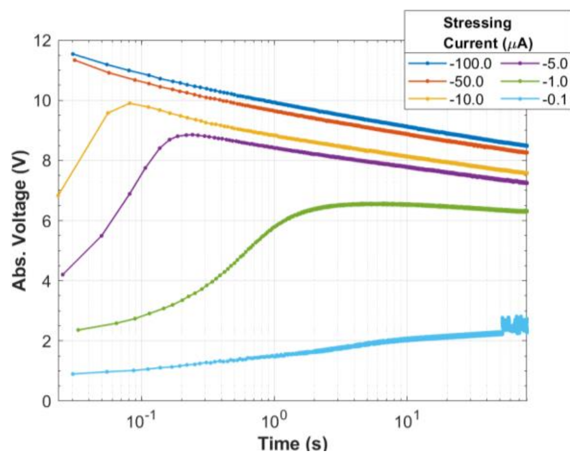

Fig. 3. **Response of devices to different magnitudes of stressing currents.** The voltage across the device is plotted during the initial constant current stressing for six separate devices, each with a different magnitude of current. The stressing lasts 100 seconds.

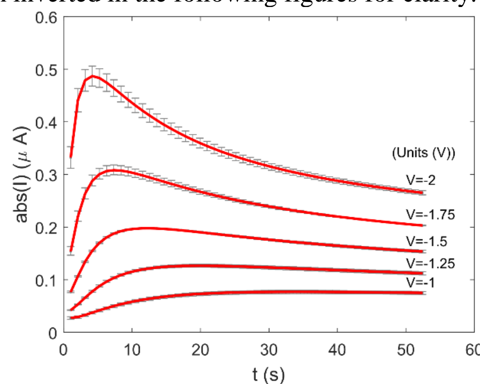

Fig. 4. **The current transient of the subthrehold regime and its voltage dependence**. The current transients of amorphous silicon dioxide thin films for a range of voltages. The voltage is applied to the gold electrical contact while the molybdenum contact is grounded. For each voltage, the average of three trials is plotted, with error bars depicting the maximum and minimum of the three trials.

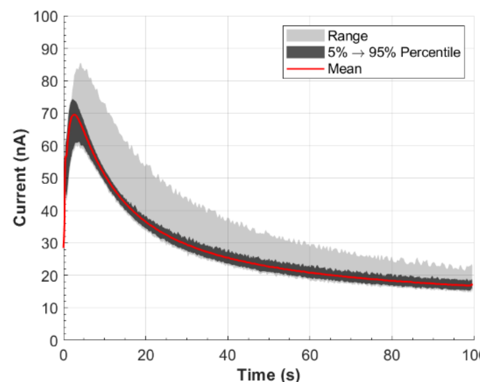

Fig. 5. **Repeatability of the current transients within the subthreshold regime.** The mean, range and 5%/95% percentiles are plotted for 132 current transients induced by a -0.8V step potential applied to the gold electrical contact while the molybdenum contacted was electrically grounded. The data has been low pass filtered using a single order filter with a cutoff frequency of 10kHz to remove noise which otherwise obscurres variability between trials.

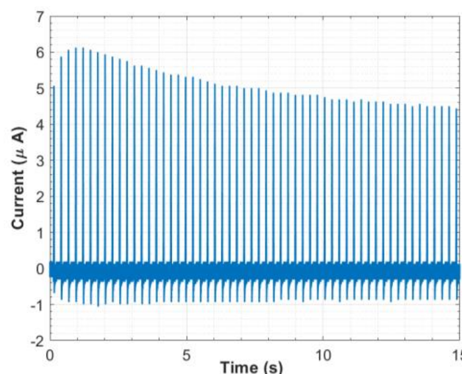

Fig. 6. **Device response to a spike train.** The current flowing through the device while a spike train is applied. The pulses are applied to the gold electrical contact while the molybdenum contact is grounded. Each pulse has a Gaussian form with a FWHM of 20ms, an amplitude of -3V and period of 300ms. The magnitude of the current thas been inverted for clarity. The device had been electrically stressed with a constant current of $-100\mu A\ for\ 100\ seconds$.

Authorized licensed use limited to: University College London. Downloaded on June 12,2023 at 10:05:38 UTC from IEEE Xplore. Restrictions apply.
© 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

This article has been accepted for publication in IEEE Transactions on Nanotechnology. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2023.3284144

The current response to the train of Gaussian pulses is plotted in Fig. 6, demonstrating behaviour like that observed in the DC measurements. An initial potentiation lasting approximately four pulses, is followed by a longer depression period. This shows that the combination of potentiation and depression are achievable in both DC and spike train operation. This is promising as it suggests the device is suitable for use in spiking neural networks.

One potential advantage of the subthreshold regime is its high resistance value (approx. 10MΩ). The resistance switching devices used in neuromorphic computing typically switch between high resistance states (approx. 100k Ω) and low resistance states (approx. 1k Ω) [21]. However, within the subthreshold regime, our device stays within a range of resistances similar to, or greater, than the high resistance state of binary resistance switching devices. This suggests the device could operate with lower current draws than that of a typical resistance switching device. However, this does have its limitations. The wide resistance range of switching devices allows systems to be less sensitive to noise or voltage fluctuations and also provides a greater range in which devices can be programmed. There is therefore a trade-off between current draw and resilience to noise. Another challenge of the subthreshold regime of the voltage driven depression. From Figure 4 it is clear little depression occurs beneath -1V. This potentially limits the operating voltage of a circuit wishing to make use of depression dynamics within the subthreshold regime.

B. *Selecting for Potentiation or Depression*

The ability to select/tune between potentiation and depression is important for circuit designers wanting to use the device in neuromorphic circuits. In this section we will demonstrate two approaches to tuning the balance between potentiation and depression.

The more flexible approach is to adjust the amplitude of the applied pulses. As shown in Fig. 4, smaller voltages, such as -1V, exhibit some degree of potentiation but not depression. This is also the case for low voltage spike trains. Fig. 7 shows the current response to spike trains with different pulse amplitudes. Lower voltages do not exhibit depression. We believe the absence of depression at lower voltages may indicate that the process requires a minimum electric field to induce the change from potentiation. This suggests the need to overcome an activation barrier to induce defect drift.

On the other hand, depression may be the desired behaviour. In this case, the amplitude of pulses can be increased to the point at which the initial potentiation is overcome. In Fig. 8. we plot the percentage change in device conductance from its initial value. This is repeated for spike trains of various amplitudes. We find spike trains with an amplitude $< -3.75V$ are largely potentiating, with the change in conductance remaining positive. However, when the amplitude is increased to $-4.5V$, the spike train causes the change in conductance to go negative and causes depression.

An alternative and more permanent approach to select for a specific behaviour is to adjust the electrical stressing the device undergoes following fabrication.

As described above, the devices are initially stressed by forcing a constant current through the device. By adjusting the magnitude of current being applied to the device, we can modify how aggressively the device is stressed and in tune adjust the current transient response. In Fig. 3 the response to stressing is plotted for six different devices, each stressed with a different current, from -0.1 μA to -100μA, applied to each device for 100 seconds.

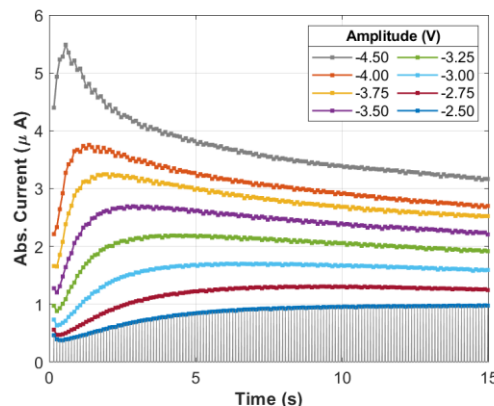

Fig. 7. **Dependence of potentiation and depression on the amplitude of applied voltage pulses.** Device current is plotted for Gaussian spike trains of increasing amplitude. The Gaussian current pulses are plotted in grey for the smallest amplitude (-2.5V). However, for clarity, only the peaks of each pulse are plotted for the remaining amplitudes. The pulses have a FWHM of 20ms and a period of 100ms. The device had previously been electrically stressed with a constant current of $-50\mu A$ for 100 seconds.

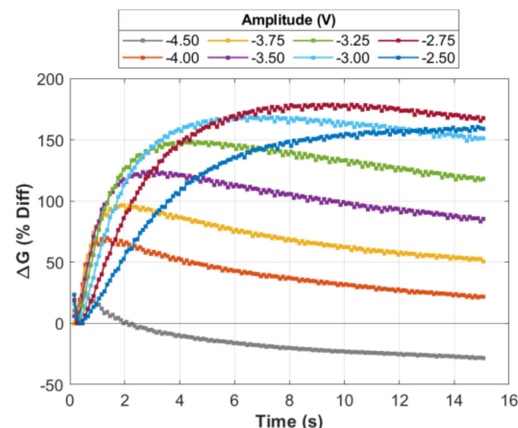

Fig. 8. **Selecting for depression with spike trains of larger amplitudes.** The change in conductance induced by each pulse of the spike train is plotted as the percentage difference from its original value. Larger amplitudes have a predominantly depressing effect whereas smaller amplitudes have a potentiating effect. The device had initially been electrically stressed with a constant current of $-50\mu A$ for 100 seconds.

The resultant current transients, plotted in Fig. 9, exhibit progressively more prominent potentiation for higher stressing currents. This is combined with an increasing conductance. At the extremes, the device stressed with the smallest current, -0.1μA, exhibits no potentiation only depression and the device stressed the most, -100μA, potentiates to almost 10× its initial conductance.

These techniques provide the opportunity to adjust the degree of potentiation occurring in the device, from barely present to prominent. It is important to note that this tuning is irreversible and would most likely be decided at the point of circuit fabrication. In contrast, the approach of varying spike amplitude is flexible and can be adjusted during operation.

Authorized licensed use limited to: University College London. Downloaded on June 12,2023 at 10:05:38 UTC from IEEE Xplore. Restrictions apply.
© 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

This article has been accepted for publication in IEEE Transactions on Nanotechnology. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2023.3284144

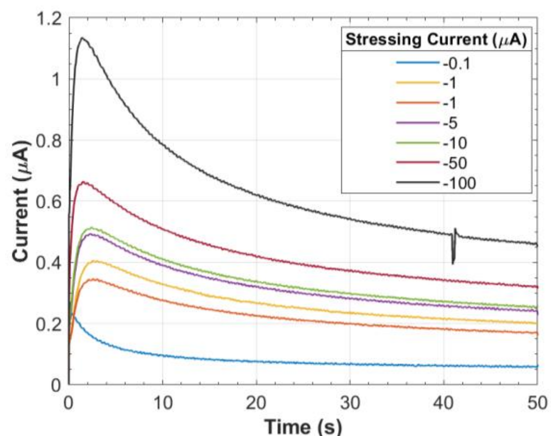

Fig. 9. **Device current dependence on stressing magnitudes.** The device current is plotted in response to a step potential of -1.25V for devices initially stressed to different degrees. Devices stressed to a lesser extent exhibit no potentiation while devices heavily stressed exhibit both greater potentiation and depression. The absolute value of the device current has been plotted for clarity.

C. *Steady State Analysis*

With the device able to exhibit both an increase and decrease in conductance, and with each of these occurring at different rates and with different relaxation rates, it is inevitable that the steady state conductance for different spike train periods will differ. Before investigating the computational potential of this behaviour, we will confirm this is the case.

In Fig. 10, the device current is plotted for spike trains with a range of inter-spike time periods. Each spike train causes the device to eventually settle to a steady state conductance for which changes in conductance caused by the applied spikes are balanced with the relaxation dynamics of the device. We find the steady state conductance depends on the period of the pulses applied to the devices, as expected – higher frequency pulses cause the device to become less conductive.

These results suggest that we could potentially use this behaviour to modify device resistance in response to spike trains of different frequencies. We will show in the following section how this has potential applications in implementing homeostatic behaviours.

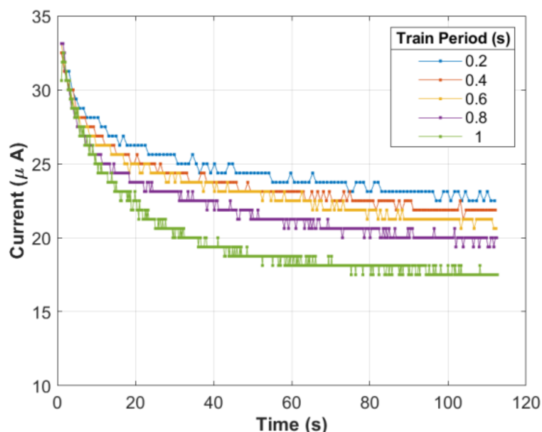

Fig. 10. **Device current for trains of voltage spikes of varying inter-spike time periods.** The maximum device current is plotted for each pulse applied to a $400 \times 400\mu m$ device. The pulses are Gaussian in shape with a FWHM of 50ms and an amplitude of -2.25V. The absolute value of the device current has been plotted for clarity.

IV. Applications

In this section we highlight selected potential applications of this behaviour to novel computing architectures. It is not an exhaustive list; however, we hope it demonstrates there is some utility to this behaviour and that it inspires readers to consider whether it could have uses in their own computational tasks.

A. *Homeostasis*

In biological systems homeostasis refers to a system maintaining preferred operating conditions or particular states. The regulation of body temperature is one example of a homeostatic process. When applied to spiking neural networks, homeostasis can act to maintain a certain spiking activity to avoid excessive power consumption via unnecessary spike events, or it could protect against faulty neurons entering a chaotic, high activity state. Without homeostasis, such events could cause the entire network to erupt into a chaotic state.

Homeostasis in memristor-based synapses has repeatedly been implemented by applying pulses of opposite polarities to the presynaptic spikes - typically applied at the post neuron side of the synapse [24], [25]. This approach is applied globally to all input synapses and is a way to indirectly increase the neuron's firing threshold [25]–[27]. The homeostasis is therefore a response to the postsynaptic neuron's firing rate rather than individual presynaptic neurons.

One example of homeostatic behaviour implemented with memristors follows from the approach usually taken in CMOS circuits by adapting the firing threshold of the neuron. The conductance change of a phase change memory (PCM) memristor is used to modulate the threshold of a CMOS neuron [28]. The PCM device is connected to the output of the post-synaptic neuron, with each pulse increasing the conductance of the device. This in turn this causes the reference voltage generated from the PCM device to increase with time. Such homeostatic neurons have been used in recurrent neural networks [29] and demonstrate the advantage of introducing homeostasis by comparing the accuracy of performance of a network on the MNIST dataset both with and without homeostasis. An average improvement of 20% is achieved [30].

But homeostasis can also be applied at the level of individual synapses, rather than by modulating the threshold of the post-synaptic neuron. For example, one form of homeostasis is habituation, where a step change in input only results in a temporary step change in the output which eventually decays to steady-state value. An example of this has been demonstrated in copper phthalocyanine (CuPc)-based memristors [31]. However, this is achieved in a specific operating regime, in which the memristor is exposed to alternating excitatory and inhibitory pulses. As is common in such work, pulses are of opposite polarities, a requirement which seems to be the result of the memristor's bipolar behaviour.

An alternative approach to implementing synaptic-level homeostasis with memristors is to exploit the temperature dependence of device conductance [32]. Increasing the temperature of the memristor reduces the device's resistance and can therefore be used to modulate the conductance of the device. If the input exhibits a step change, a feedback loop acts to heat the synapses and reduce their weight. Using the thermal properties of the memristor is a unique approach to modulating

Authorized licensed use limited to: University College London. Downloaded on June 12,2023 at 10:05:38 UTC from IEEE Xplore. Restrictions apply.
© 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

This article has been accepted for publication in IEEE Transactions on Nanotechnology. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2023.3284144

the weight of the synapse in parallel to the spiking inputs and is advantageous from a timescale perspective as the cooling/heating times are inherently much slower than any electronic processes. However, it has a cost; heating elements generate higher power consumption.

The challenge of applying homeostasis at the individual synaptic level, in which a specific synapse's weight is reduced due to an overactive presynaptic neuron, is interesting to note. This may be because a memristor's direction of change in conductance, i.e. depression or potentiation, is typically dependent on the spike's polarity and not on the firing rate. This is a result of the memristor having a monotonic response to a single polarity regardless of spike frequency. Depression is therefore only achieved by applying a spike of opposite polarity or to the opposite electrode. This makes implementation of homeostasis easiest when potentiation is carried out by neurons on one side of the memristor (presynaptic) whilst depression is driven by the neuron on the opposite side (postsynaptic) [24], [25].

To apply an habituation form of homeostasis to an attached input neuron, the synapse needs a non-monotonic response to the input firing rate; at low frequencies the conductance should be higher but beyond a threshold the gain should reduce enabling depression. Fortunately, a device in the subthreshold regime is able to implement this thanks to the steady state behaviour studied in the previous section.

As shown in the previous section, the steady state conductance of the device depends on the firing rate of the attached neuron. For higher frequency pulse trains, the device conductance is depressed; while at lower frequencies, the device conductance has a higher steady state. This behaviour can be used to supress the effect of a faulty input neuron that has entered a high frequency overactive state. This enables homeostasis to be applied individually to each incoming synapse, in response to their driving neuron's activity, rather than to all input synapses. An advantage of this approach is there being no need for the presynaptic neuron to apply pulses of opposite polarities or of requiring access to the postsynaptic side of the synapse – simplifying circuit construction in comparison to other studies [24], [25], [31], [32].

This concept is demonstrated in Fig. 11. The device is connected to a signal generator producing Gaussian pulses at a slow rate of 1Hz. We define this as the normal background activity of that neuron. We select for depression by choosing a relatively large pulse amplitude of –3V. The device reaches a steady state conductance under these conditions. At $t = 1.8$ minutes, we simulate the input neuron entering a faulty higher activity state which could have been caused by, for example, circuit damage. The frequency of the spike train is increased to 10Hz. Without homeostasis this faulty input could cause the attached output neuron to enter a similar state, which could propagate through subsequent layers of the neural network. Fortunately, due to the steady state behaviour of a device in the subthreshold regime, the device conductance reduces when exposed to a high frequency spike train. This reduces the total current that is injected into the attached output neuron and so reduces the chance of this high frequency input triggering similar behaviour in subsequent neurons.

While this suppression is useful in protecting the network from overactivity, the suppression should ideally not be permanent. If the input neuron returns to its normal operating conditions, the suppression should be reversed, and the neuron allowed to contribute to the network once again. From $t = 2.8$ minutes we demonstrate this concept. The signal generator returns to the background level of activity with a spike train of frequency 1Hz. The device conductance responds by returning to its original steady state value prior to the neuron's faulty phase, which is possible due to the volatility of the conductance changes within the subthreshold regime. This is an important feature of homeostatic mechanisms: the ability of protection mechanisms to reverse if normal operating conditions return.

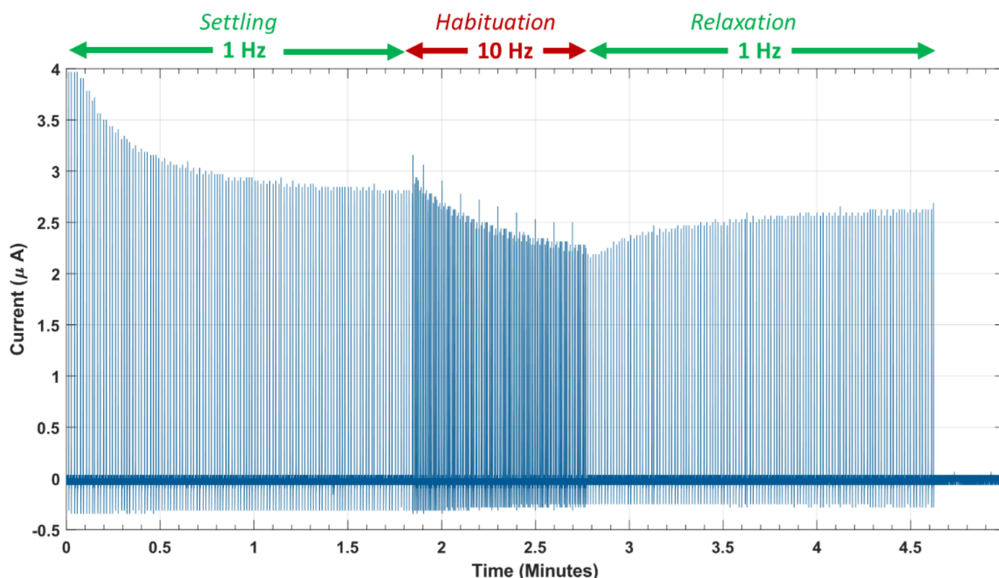

Fig. 11. **Demonstration of habituation using the subthreshold regime.** The device current is plotted in response to a series of Gaussian pulses with a full width half maximum of 50ms and an amplitude of -3V. The frequency of the pulses switches from 1Hz to 10Hz and back to 1Hz to simulate a connected neuron entering a overactive or broken state are then returning to its normal background activity. Habituation is demonstrated during the 10Hz overactive phase which is then shown to relax when the input returns to its background rate.

Authorized licensed use limited to: University College London. Downloaded on June 12,2023 at 10:05:38 UTC from IEEE Xplore. Restrictions apply.
© 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

This article has been accepted for publication in IEEE Transactions on Nanotechnology. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2023.3284144

While we have shown the basic principle of homeostatic habituation is possible using the subthreshold regime there are limitations. For example, it is not possible to program a specific and fixed conductance value when the device has entered this subthreshold regime. In contrast, if the device is electroformed like a typical memristor, the weight can be programmed to a range of analogue values. Implementing this homeostatic behaviour in a physical system could require the device to be placed in series with a device in a programmable operating regime. Fortunately, both devices - the programmable device and the subthreshold device - are structurally the same, being produced by the same fabrication process; the only difference being how the device is electrically stressed. This means integrating both types of devices onto a single wafer is feasible.

V. Future Work and Limitations

How and where this behaviour should be used in neuromorphic computing is an open question. We have previously employed the device to detect edges within images by way of a novel circuit, [14] but the device may also have potential as a synapse within spiking neural networks. The slow dynamics of the conductance depression could prove useful for implementing long term homeostasis or habituation while its volatile potentiation may better suit short term memory. Equally, the combination of these two behaviours in a single device could have unknown benefits.

With regards to spiking neural networks, the subthreshold regime could be used to implement synapse weight update rules such as spike-rate-dependent plasticity (SRDP) [33]. In SRDP, the frequency of the input signal is used to update the synaptic weights. This is in contrast to spike-timing-dependent plasticity rules which adjust the weight based on the time intervals between spikes from the presynaptic and postsynaptic neurons. The homeostasis behaviour here is a direct function of the spike train frequency and has an immediate impact on the weight update process between neural network layers. Additionally, the volatile nature of the changes in conductance which occur in the subthreshold regime are akin to a forgetting process. Such forgetting processes have been used to decrease synaptic weights without the need to trigger inhibiting pulses [34]. This can simplify circuit complexity. However, the forgetting phenomenon has not been fully studied in the of context of SNNs directly so we cannot gauge accurately its impact on network performance.

However, we must also acknowledge that the slow dynamics of this behaviour could also prove a disadvantage when speed is a priority limiting the behaviours use to circuits with slower dynamics.

Equally, if the behaviour is to be used by circuit designers, then we must also address the physics underpinning this behaviour. Existing models such as the SCLC model and other electronic explanations need further verification in order for accurate simulations/models to be developed and the fundamental limitations of the behaviour to be identified.

VI. Conclusion

In this paper we have demonstrated a device that can be made to exhibit potentiation and depression of conductance under the same voltage polarity in an operating regime that we refer to as the subthreshold regime. We have documented how to induce this behaviour within standard resistance switching devices and how to select for particular dynamics. The methodologies we have presented will not only enable researchers to replicate the behaviour in their own devices, but also instruct circuit designers on how to tune the behaviour to their specific application.

The subthreshold regime's ability to produce potentiation and depression under the same polarity of voltage pulses is a unique behaviour which directly addresses the ongoing issues of circuits needing to source pulses of both polarities, or, of neurons having access to both sides of a synapse – leading to complex signal routing. This operating regime will have applications in the field of neuromorphic computing where circuits exploiting the behaviour could operate using single rail power supplies, simplifying circuit construction and layout. Equally, the more complex dynamics may present the opportunity for new types of neuromorphic circuits as discussed in the context of homeostasis in individual synapses.

From a broader perspective, this operating regime also strengthens the notion of entirely memristive circuits. Having identified and presented an intermediate regime found between the two extremes of the pristine and electroformed states of MIM devices, with qualitatively different characteristics, it leads us to question how these different behaviours could be combined and what new computations could this lead to in the future.

Acknowledgments

DJM acknowledges the EPSRC for financially supporting the project [EP/T517793/1]. VCV acknowledges the EPSRC for funding via project [2576207].

References

[1] A. Mehonic and A. J. Kenyon, "Brain-inspired computing needs a master plan," *Nature 2022 604:7905*, vol. 604, no. 7905, pp. 255–260, Apr. 2022, doi: 10.1038/s41586-021-04362-w.

[2] L. O. Chua, "Memristor—The Missing Circuit Element," *IEEE Transactions on Circuit Theory*, 1971, doi: 10.1109/TCT.1971.1083337.

[3] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008, doi: 10.1038/nature06932.

[4] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett*, 2010, doi: 10.1021/nl904092h.

[5] S. A. Khan and S. Kim, "Comparison of diverse resistive switching characteristics and demonstration of transitions among them in Al-incorporated HfO2-based resistive switching memory for neuromorphic applications," *RSC Adv*, vol. 10, no. 52, pp. 31342–31347, Aug. 2020, doi: 10.1039/D0RA06389D.

[6] A. Mehonic *et al.*, "Electrically tailored resistance switching in silicon oxide," *Nanotechnology*, vol. 23, no. 45, p. 455201, Nov. 2012, doi: 10.1088/0957-4484/23/45/455201.

[7] F. El Kamel, P. Gonon, L. Ortega, F. Jomni, and B. Yangui, "Space charge limited transient currents and oxygen vacancy mobility in amorphous BaTiO3 thin films," *J Appl Phys*, vol. 99, no. 9, p. 094107, May 2006, doi: 10.1063/1.2196112.

[8] S. Zafar *et al.*, "Oxygen vacancy mobility determined from current measurements in thin Ba0.5Sr0.5TiO3 films," *Appl Phys Lett*, vol. 73, no. 2, p. 175, Jul. 1998, doi: 10.1063/1.121746.

[9] A. Many and G. Rakavy, "Theory of Transient Space-Charge-Limited Currents in Solids in the Presence of Trapping," *Physical Review*, vol. 126, no. 6, pp. 1980–1988, Jun. 1962, doi: 10.1103/PhysRev.126.1980.

[10] M. A. Lampert and P. Mark, "Current injection in solids." Academic Press, 1970.

[11] R. Meyer, R. Liedtke, and R. Waser, "Oxygen vacancy migration and time-dependent leakage current behavior of Ba0.3Sr0.7TiO3 thin

Authorized licensed use limited to: University College London. Downloaded on June 12,2023 at 10:05:38 UTC from IEEE Xplore. Restrictions apply.
© 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

This article has been accepted for publication in IEEE Transactions on Nanotechnology. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2023.3284144

films," *Appl Phys Lett*, vol. 86, no. 11, p. 112904, Mar. 2005, doi: 10.1063/1.1874313.

[12] N. Zhong, H. Shima, and H. Akinaga, "Transient Current Study on Pt/TiO $_{2-x}$/Pt Capacitor," *Jpn J Appl Phys*, vol. 49, no. 4, p. 04DJ15, Apr. 2010, doi: 10.1143/JJAP.49.04DJ15.

[13] D. J. Mannion, "Current transient phenomena in silicon oxide resistance switching oxides: characterisation and computational applications," *Doctoral thesis, UCL (University College London).* , Apr. 2022.

[14] D. J. Mannion, A. Mehonic, W. H. Ng, and A. J. Kenyon, "Memristor-Based Edge Detection for Spike Encoded Pixels," *Front Neurosci*, vol. 13, p. 1386, Jan. 2020, doi: 10.3389/fnins.2019.01386.

[15] Y. Demirag *et al.*, "PCM-trace: Scalable synaptic eligibility traces with resistivity drift of phase-change materials," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2021-May, 2021, doi: 10.1109/ISCAS51556.2021.9401446.

[16] R. A. John *et al.*, "Reconfigurable halide perovskite nanocrystal memristors for neuromorphic computing," *Nature Communications 2022 13:1*, vol. 13, no. 1, pp. 1–10, Apr. 2022, doi: 10.1038/s41467-022-29727-1.

[17] J. Wang and S. Trolier-McKinstry, "Oxygen vacancy motion in Er-doped barium strontium titanate thin films," *Appl Phys Lett*, vol. 89, no. 17, p. 172906, Oct. 2006, doi: 10.1063/1.2364127.

[18] S. Zafar, H. Jagannathan, L. F. Edge, and D. Gupta, "Measurement of oxygen diffusion in nanometer scale HfO2 gate dielectric films," *Appl Phys Lett*, vol. 98, no. 15, p. 152903, Apr. 2011, doi: 10.1063/1.3579256.

[19] L. Chen, "Study On The Leakage Current Behavior And Conduction Mechanism Of Porous Low-k In Cu/porous Low-k Interconnects: The Influence Of Extrinsic Factors," University of Texas Arlington, Arlington, 2010.

[20] A. Mehonic *et al.*, "Intrinsic resistance switching in amorphous silicon oxide for high performance SiOx ReRAM devices," *Microelectron Eng*, vol. 178, pp. 98–103, Jun. 2017, doi: 10.1016/j.mee.2017.04.033.

[21] D. S. Jeong, B. J. Choi, and C. S. Hwang, "Electroforming Processes in Metal Oxide Resistive-Switching Cells," in *Resistive Switching*, Weinheim, Germany: Wiley-VCH Verlag GmbH & Co. KGaA, 2016, pp. 289–316. doi: 10.1002/9783527680870.ch10.

[22] Y. Li, Z. Wang, R. Midya, Q. Xia, and J. Joshua Yang, "Review of memristor devices in neuromorphic computing: Materials sciences and device challenges," *Journal of Physics D: Applied Physics*. 2018. doi: 10.1088/1361-6463/aade3f.

[23] M. Prezioso, F. Merrikh Bayat, B. Hoskins, K. Likharev, and D. Strukov, "Self-Adaptive Spike-Time-Dependent Plasticity of Metal-Oxide Memristors," *Sci Rep*, 2016, doi: 10.1038/srep21331.

[24] L. Wang *et al.*, "Long-Term Homeostatic Properties Complementary to Hebbian Rules in CuPc-Based Multifunctional Memristor," *Sci Rep*, 2016, doi: 10.1038/srep35273.

[25] Z. Zhao *et al.*, "A Memristor-Based Spiking Neural Network with High Scalability and Learning Efficiency," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2020, doi: 10.1109/TCSII.2020.2980054.

[26] X. Shi, Z. Zeng, L. Le Yang, and Y. Huang, "Memristor-Based Circuit Design for Neuron with Homeostatic Plasticity," *IEEE Trans Emerg Top Comput Intell*, 2018, doi: 10.1109/TETCI.2018.2829914.

[27] C. Bartolozzi, O. Nikolayeva, and G. Indiveri, "Implementing homeostatic plasticity in VLSI networks of spiking neurons," in *Proceedings of the 15th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2008*, 2008. doi: 10.1109/ICECS.2008.4674945.

[28] I. Muñoz-Martin, S. Bianchi, S. Hashemkhani, G. Pedretti, O. Melnic, and D. Ielmini, "A Brain-Inspired Homeostatic Neuron Based on Phase-Change Memories for Efficient Neuromorphic Computing," *Front Neurosci*, vol. 15, p. 1054, Aug. 2021, doi: 10.3389/FNINS.2021.709053/BIBTEX.

[29] S. Bianchi, I. Muñoz-Martín, S. Hashemkhani, G. Pedretti, and D. Ielmini, "A bio-inspired recurrent neural network with self-adaptive neurons and PCM synapses for solving reinforcement learning tasks," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2020-October, 2020, doi: 10.1109/ISCAS45731.2020.9181103/VIDEO.

[30] I. Muñoz-Martín, S. Bianchi, S. Hashemkhani, G. Pedretti, and D. Ielmini, "Hardware implementation of PCM-based neurons with self-regulating threshold for homeostatic scaling in unsupervised learning," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2020-October, 2020, doi: 10.1109/ISCAS45731.2020.9181033/VIDEO.

[31] L. Wang *et al.*, "Long-Term Homeostatic Properties Complementary to Hebbian Rules in CuPc-Based Multifunctional Memristor," *Sci Rep*, 2016, doi: 10.1038/srep35273.

[32] T. Abbey, A. Serb, S. Stathopoulos, L. Michalas, and T. Prodromakis, "Emulating homoeostatic effects with metal-oxide memristors T-dependence," Oct. 2021.

[33] P. Huang *et al.*, "Binary Resistive-Switching-Device-Based Electronic Synapse with Spike-Rate-Dependent Plasticity for Online Learning," *ACS Appl Electron Mater*, 2019, doi: 10.1021/acsaelm.9b00011.

[34] J. Li *et al.*, "Enhanced Spiking Neural Network with forgetting phenomenon based on electronic synaptic devices," *Neurocomputing*, 2020, doi: 10.1016/j.neucom.2019.09.030.

Authorized licensed use limited to: University College London. Downloaded on June 12,2023 at 10:05:38 UTC from IEEE Xplore. Restrictions apply.
© 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.