Modular Multi-Channel RFSoC System Expansion and Array Design

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***Abstract*—Radio Frequency (RF) sensors are often designed to operate in a single mode or configuration. Demands coming from operating in future challenging Electromagnetic Environment (EM) conditions require innovative solutions and significant changes from current radar architectures. This paper provides a system level review of a modular multi-function RF sensor solution which allows for a N node solution which can be either used to drive a singular powerful array solution OR deployed as N multistatic RF sensor nodes. Both solutions use a common digital solution which is based on the Xilinx Radio Frequency System on a Chip (RFSoC) technology. An antenna array operating at C-band has been designed for the project, along with daughter-boards which facilitate access to all 8 receive channels from the Xilinx ZCU111 RFSoC development board. A solution to the challenges of synchronising the ADC channels (including across multiple ZCU111 boards) is also presented, with results showing the synchronisation performance.**

***Index Terms*—RFSoC, Array Antenna, Beamforming, Multi-static**

I. Introduction

The Xilinx Radio Frequency System on a Chip (RFSoC) [1] concept has in recent years provided significant potential benefit for RF sensors and communication devices. The RFSoC is a commercial off the shelf (COTS) device containing a large Field Programmable Gate Array (FPGA) integrated on-chip with multi-gigasample per second analogue to digital converters (ADC) and digital to analogue converters (DAC). Different variants of the RFSoC device contain 8 or 16 ADC and DAC channels. Each ADC/DAC also includes digital down-/up-conversion, and decimation/interpolation which may optionally be included in the signal chain providing direct digital sampling of RF signals and conversion to baseband. The performance of the ADCs on the RFSoC has been characterised in [2]. This close integration of programmable logic and high speed analogue conversion components enables more accessible creation of systems which would previously have required the complex integration of multiple devices to achieve similar functionality.

The ARESTOR system [3] developed in the Department of Electronic and Electrical Engineering at UCL is a multi-role RF sensor based on the Xilinx ZCU111 RFSoC evaluation board [4]. The initial premise for the overall ARESTOR concept was a modular system where multiple sub-systems consisting of an RFSoC based ARESTOR platform plus an array antenna could be stacked to create a larger array antenna with associated backend processing provided by the multiple ARESTOR systems, Fig. 1(a). As operational requirements change precisely the same hardware systems might be separated to provide a multistatic distributed sensor, Fig. 1(b).

Previous studies have used ARESTOR for performing a diverse range of experimental campaigns including multi-band active radar measurements of drones [5], simultaneous active and passive radar measurements of human targets [6], integrated sensing and communications (ISAC) [7], [8] and real-time detection and classification of internet of things (IoT) signals [9].

The possible benefits provided by the use of RFSoC devices to phased array radar digitisation and processing is starting to be recognised. Fagan *et al* [10] report on a project which had early access to RFSoC and paired it with a 64 element S-band phased array antenna. The S-band antenna outputs were down-mixed due to the pre-production RFSoC having much lower sample rates than are available in the current commercial versions. The structure of our system is similar in that we use an RF downconverter to translate from C-band to a 1 GHz baseband. This work illustrates the cost and size reductions enabled by the use of integrated devices, but also warns that high level language implementation of algorithms is necessary or the complexity will result in excessively long development timescales. Fosberry and Livadaru [11] have implemented a beamforming system using 8 ADC channels from 16 channels available in a later version of the RFSoC. The authors use Matlab to create the FPGA based system. Matlab is further used to calibrate the system and provide the beam steering vectors. Pulipati *et al* [12] describe a four element array operating at 28 GHz with 800 MHz of bandwidth which uses RFSoC for back-end processing. This array system is aimed at future communication systems. The paper describes the system as 'direct-conversion' however a down conversion stage is still required to place the received signals within the sampling range of the RFSoC. The work in [13] implements a C-band phased array using an 8x8 array of Vivaldi antenna elements for radio astronomy applications and two 16 channel RFSoC boards to produce a four beam system each with 1.25 GHZ of instantaneous bandwidth. The RFSoC will be used to implement channelisation by polyphase filters and beamforming. Another work aimed at communications applications is described in [14]. This system multiplexes multiple input channels onto a single RFSoC ADC channel so only exploits a limited part of the RFSoC ADC/DAC capability. However, it makes extensive use of the FPGA to calculate factors required for multiplexing the input channels.

Fig. 1: Concept of modular RFSoC based monostatic array solution (a) which can be re-deployed as a distributed coherent multistatic solution (b).

Schweizer *et al* [15] address the design of a 4x4 MIMO radar highlighting the massive dataflow issues which multiple multi-gigabit per second ADCs and DACs impose on the processing stages which follow. The radar consists of a 77 GHz front end feeding an 8 element patch antenna array.

Although ARESTOR is already very capable and has been employed successfully in various radar and communications based projects, the ZCU111 board that it is based on does have certain limitations which preclude it from use in systems requiring coherency across all 8 input or output channels. This is mostly due to the configuration of the XM500 daughter-board supplied with the ZCU111. The XM500 provides SMA connector interfaces to all input/output channels. The issue with the XM500 is that for flexibility 2 input and 2 output channels are provided with high frequency balans, 2 with low frequency balans, and the remaining 4 channels of inputs and outputs, as differential pairs directly accessing the RFSoC chip pins.

The project described in this work aims to upgrade the ARESTOR system by replacing the XM500 with a custom designed daughter-board with identical paths for all channels to the outside world. The concept is extended to provide modular access to pairs of input/output channels such that different characteristics might be applied to each pair if required, Section II.

The second aspect of this project is to develop a 16 channel C-band array antenna for which the upgraded ARESTOR platform will provide the digital backend, implementing beam-forming and radar signal processing.

The structure of this paper is as follows. Section II describes the details of the custom designed daughter-board to replace the XM500. A critical consideration for successful array antenna processing is the timing and coherency of the data maintained across all channels, both within a single ARESTOR platform as well as across multiple ARESTOR platforms, Section III addresses the challenges associated with this requirement in the use of the RFSoC, and specifically the ZCU111 development board, and the results we have achieved. Section IV describes the C-band array antenna and the down-converter board which brings the outputs from the array into the ZCU111 frequency range designed for this project. Finally we summarise the work and draw conclusions in Section V.

II. Modular Daughter-board Design

The differential inputs/outputs from the ADCs/DACs on the RFSoC chip along with clocking inputs and a number of digital pins are made available on the ZCU111 through two high pin-count headers referred to as the RFMC connectors. Xilinx provide a separate daughter-board, the XM500, which mates with the RFMC connectors and provides SMA connections for all the RF and clock signals. The XM500 splits both the ADC and DAC channels into two low-frequency and two high-frequency single ended connections and four differential connections. Although this makes the XM500 useful for testing a variety of operational modes of the ZCU111, it is not suitable for larger scale multi-channel applications such as the C-band phased-array work presented here, which requires all eight receive channels to operate at the same frequency and interface with single-ended signals from the RF front-end. To overcome this limitation we have developed our own daughter-board which provides a common interface to all 8 receive channels and 8 transmit channels of the ZCU111.

The ARESTOR platform was primarily developed as a multi-role RF sensor [3]. This makes design of a common RF front-end challenging, since each operational mode of the system likely requires different analogue signal conditioning. Rather than attempt to develop a single design which could address all these needs, we instead opted for a flexible and modular design which could be easily modified to suit any sensing needs. Our concept is shown in Fig. 2. A daughter-board which mates with the RFMC connectors on the ZCU111 provides RF signal conditioning which is common to all possible sensing modes. Separate granddaughter-boards plug into the daughter-board and provide the specialisations required for each different sensing mode. The daughter-board additionally provides power distribution and digital control signals to

each of the granddaughter-boards. An EEPROM chip on each granddaughter board identifies it, allowing software running on the ZCU111 to query what hardware is present and load the required drivers. Our high-level Python API allows a common command and control interface regardless of the combination of granddaughter-boards that are connected.

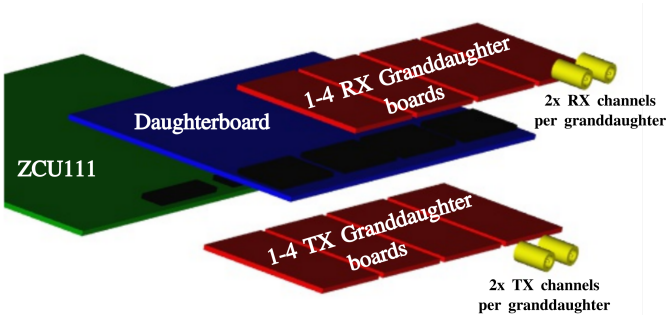

Fig. 2: Visualisation of the modular daughter-board and granddaughter-board design.

Our daughter-board design was implemented as a 6-layer PCB, with receive paths routed on the top side and transmit paths routed on the bottom side to provide the best possible isolation between them. The RF traces are length-matched so as to facilitate phase-coherent measurements across all channels. A set of simple granddaughter-boards which just provide an SMA connection to the RX or TX channels have also been created. The complete assembly is shown in Fig. 3. Wide band up- and down-mixing granddaughter-boards will be created in the near future based on the prototype RF front-end which we previously developed [6].

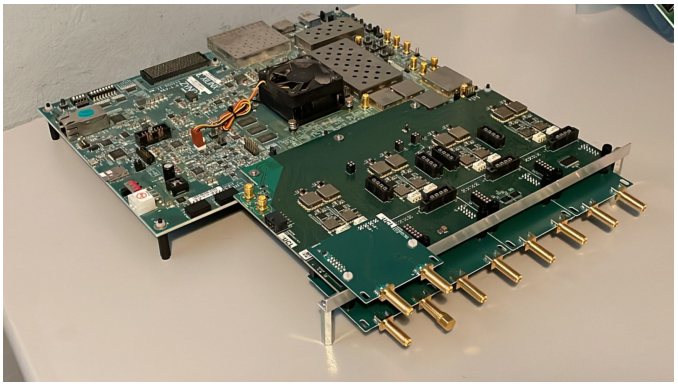

Fig. 3: Photograph of a ZCU111 with our new daughter-board installed. One RX, and four TX granddaughter-boards are installed.

Figure 4 shows the components used in the receive channels on our daughter-board. The incoming RF signal from the granddaughter-board is low-pass filtered to remove any frequencies that are beyond the operating range of the subsequent RF limiter component. A RLM-33+ RF limiter is then used to keep the RF power level below the maximum level for the LNA. Because the limiter is less effective at low frequencies, there is a high-pass filter placed after the limiter to further attenuate any low frequency components. A variable gain DVGA2-33A+ LNA is then used to tune the signal level to within the linear range (< -10 dBm) of the subsequent power limiter, which in turn limits the power level to 0 dBm (within the safe operating range of the ADCs on the RFSoC). The output level of the LNA must be set by the control software. A balun is then used to convert the single-ended signal to differential before it is routed to the ADC. Note that this design throws away a lot of dynamic range of the ADC in order to be within the linear range of the RLM-23-1WL+ power limiter. However, we believe that this is a reasonable compromise in order to protect the ADCs from being overloaded and possibly damaged. The transmit channels are much simpler and only consist of a balun.

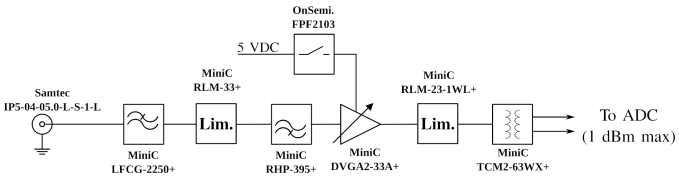

Fig. 4: Block diagram of the RX chain on our daughter-board. Each daughter-board has eight copies of this (one for each receive channel).

III. Timing and Synchronisation - Multi-Tile & Multi-Board

Within the RFSoC chip the ADCs and DACs are grouped onto tiles, with four tiles each containing two ADCs and two tiles each containing four DACs. Each tile has its own PLL, used to generate the sampling clocks for all its ADCs/DACs. In order to perform coherent measurements from ADCs/DACs across multiple tiles Xilinx provide a "multi-tile synchronisation" (MTS) mechanism. This synchronises the PLLs on separate tiles and also matches the latency of data through the FIFOs which cross the clock domain as data is moved off of the tile. MTS requires that two coherent copies of a low frequency (<10 MHz) clock be supplied to the RFSoC, the so called SYSREF and PL_SYSREF clocks. On the ZCU111 these are generated by a Texas Instruments LMK0408 device as shown in Fig. 5.

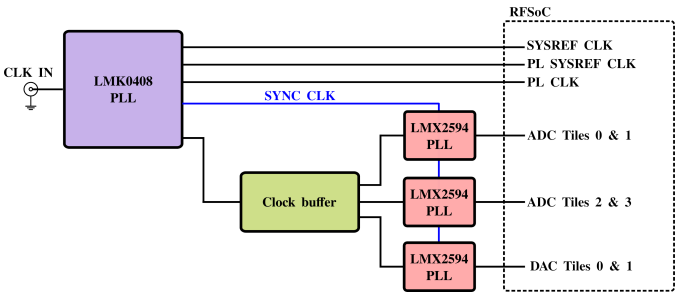

Fig. 5: Simplified block diagram of the ZCU111's clocking infrastructure.

The MTS mechanism is also suitable for synchronising measurements across multiple devices. However, this requires that all devices are supplied with coherent SYSREF and PL_SYSREF clocks. A limitation of the ZCU111 is that these signals cannot be supplied from an external source, since the board does not provide connections for the PL_SYSREF. ARESTOR circumvents this limitation by supplying the LMK0408 with a 5 MHz clock as its input (CLK IN) and configuring it in zero-delay mode such that its SYSREF and PL_SYSREF outputs are coherent copies of this input clock. Hence, by supplying multiple ARESTOR devices with in-phase 5 MHz clocks they may be synchronised using MTS.

This method of producing in-phase SYSREF signals on separate ZCU111 boards was tested by configuring the spare output of the LMK0408 to also produce a 5 MHz SYSREF signal. This output is routed to an SMA connector on the ZCU111 allowing easy measurement of the signal. The phase error between these SYSREF signals from two separate ZCU111 boards (clocked with a common 5 MHz input clock) was measured using a Rohde and Schwarz 2024 oscilloscope, sampling at 10 GSPS. A 1 PPS (pulse per second) signal from a Rubidium GPSDO was used as a trigger signal. Figure 6 shows the phase error between the two SYSREF signals over a period of 2.5 hours. The mean offset is 155 ps with a standard deviation of 4.5 ps (this is better than the 5 MHz input clocks used, which showed a standard deviation of 9.5 ps). The relatively large mean offset is consistent across system restarts and could be negated either in post-processing of multi-node data or by using the analog delay function of the LMK0408 to match the phases across devices.

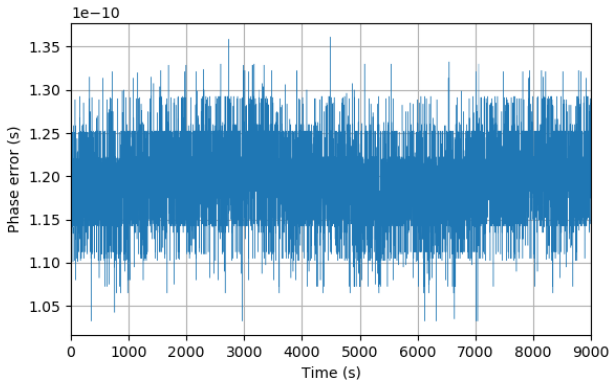

Fig. 6: Plot of phase error between the 5 MHz SYSREF signals on two separate ZCU111s. Measurements were made each second. The mean offset is 155 ps with a standard deviation of 4.5 ps.

An added complexity of synchronising all the ADCs on the ZCU111 is that tiles 0 and 1 are clocked by a different external LMX2594 PLL chip from tiles 2 and 3, as shown in Fig. 5. In order for MTS to be effective across these two groups of ADC tiles, the two LMX2594s must be synchronised with each other. This can be achieved by programming their VCO_PHASE_SYNC registers. If an external SYNC signal is required (which depends on the exact configuration of the chip) it can be applied using the SYNC CLK output from the LMK0408. This same procedure applies when synchronising multiple boards.

Figure 7 shows the experimental setup used to assess the performance of the MTS procedure across ADC tiles on a single ARESTOR node (single ZCU111). A 1 GHz tone from a signal generator is passed through a splitter and into one ADC on each tile. The ADCs are configured to sample at 3.84 GHz, and this data is then digitally down mixed by 900 MHz before being decimated by a factor of 8. This results in a 100 MHz signal sampled at a rate of 480 MHz. Thirty repeats of a 1 ms capture are performed, with all clocks being reset and MTS performed between each repeat.

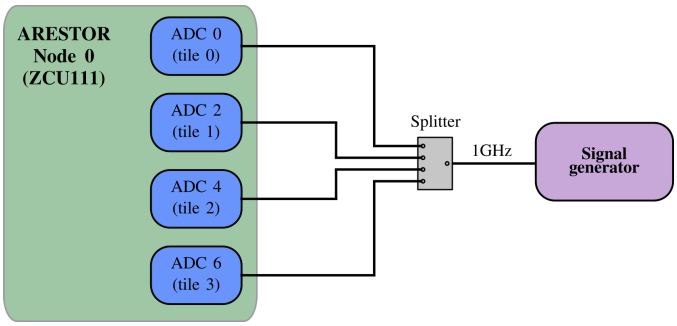

Fig. 7: Experimental setup for measuring MTS performance across ADC tiles on a single ZCU111.

To determine the phase variation between ADCs, each 1 ms capture is split into blocks of 100 samples. Each block is then fitted to a simulated 100 MHz signal using a Levenburg-Marquardt least-squares optimisation. The amplitude, phase and DC offset are left as free parameters in the fitting. The phase difference between any pair of ADCs is then computed by comparing the optimal phase value from the fitting on corresponding blocks from them. Figure 8 shows the results from applying this technique to ADC0 and ADC4.

It should be noted that it is not the absolute phase difference values shown in Fig. 8 that are of interest, since these include differences due to external cables etc., but rather it is the variation in phase difference between repeats that is indicative of the MTS performance. Our results show that a deterministic phase synchronisation of different ADC channels can be achieved to within ± 0.018 radians. We have only presented results for ADC0 and ADC4, however, this is a worst-case pairing since both tiles are clocked by separate LMX2594 devices. Comparison of other pairs of ADCs shows comparable or better results.

IV. Antenna Array Design

In this section, the design and analysis of a 16 channel planar antenna array and RF front-end, capable of operating from 5 - 6 GHz for use with ARESTOR is presented. The array aperture is comprised of 16 individual antenna elements arranged linearly along a horizontal axis. This is designed to be a receive-only array, with beam steering being performed

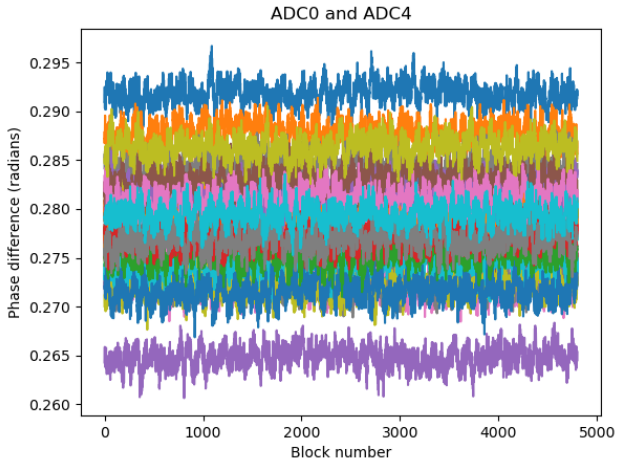

Fig. 8: Phase difference between ADC0 and ADC4 measuring a 1 GHz tone. Each line represents a single repeat with all clocks being reset and MTS being performed for each repeat.

digitally by the ARESTOR system. The RF front-end of the array ensures the signals are appropriately down converted to a suitable frequency range that can then be sampled by the RFSoC. This is limited by the frequency range of the new daughter-board, which operates from 400 - 2500 MHz.

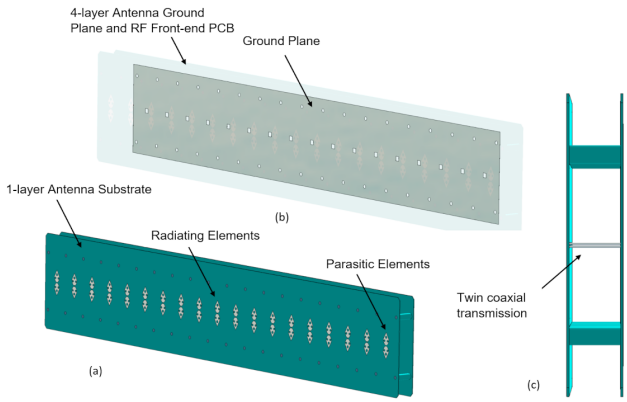

Fig. 9: 16 channel, C-band antenna array design.

Figure 9 shows the antenna array design, which is comprised of two main layers. The first layer (Fig. 9 (a)) accommodates the radiating elements of the antenna array. The second layer (Fig. 9 (b)) consists of a typical four layer PCB stack. One side of the board acts as a ground plane for the radiating elements while the other side provides an area for all the front-end circuitry. This integrated transition between the RF front-end board and the antenna array board, negates the need for additional interfacing cables, which at high frequencies can introduce significant losses.

The radiating elements in the array are based on dipole antennas. In order to achieve a wide bandwidth, several standard design techniques have been employed. Each element consists of a pair of patches, with semi-elliptical bases and inverted-cone tops, above a ground plane. The pair of patches are excited in anti phase and have an input impedance of 100 Ohms. The size of the ground plane below the antenna element affects the radiation pattern, particularly in the azimuthal plane. The antenna element is arranged vertically to provide a broader beam pattern and, as a result, the antenna is vertically polarised. This modified dipole shape design provides a wide bandwidth and radiation pattern, without increasing the complexity of the antenna. The performance of planar dipole antennas is not sensitive to small parameter variations, giving good robustness to PCB manufacturing tolerances. The antenna elements are supported on a 0.78 mm thick Taconic TLX-9 dielectric substrate.

The antenna elements are connected to the RF PCB board using a balanced twin coaxial transmission line (Fig. 9 (c)) with a balun of ratio 1:2 used to match the impedances. In order to achieve a good impedance match over the wide bandwidth, the gap between radiating patches and the ground plane was optimised to 17 mm. The antenna board is supported by nylon spacers, mounted to the RF PCB board. All the RF circuitry and the signal SMA interface were carefully laid out to minimise signal degradation. Figure 10 shows the measured return loss of an individual antenna element in the array. As seen from the figure, frequencies from 4 to 6 GHz, exhibit a return loss of better than -10 dB.

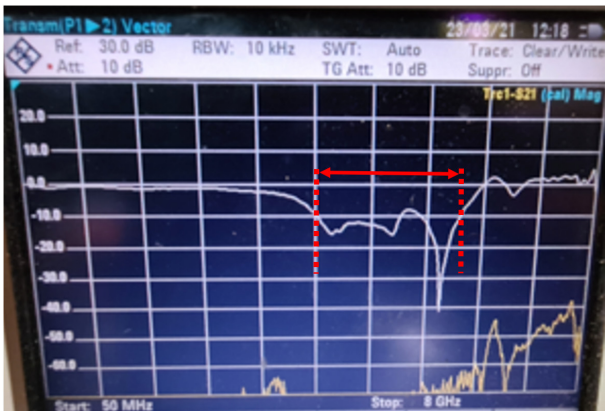

Fig. 10: Anechoic chamber measurements of antenna element return loss.

The simulated radiation pattern at 5.8 GHz of a single element within the array is shown in Figure 11. As shown, the 3 dB beam-width of a single element $\sim$ 99 degrees in azimuth and $\sim$ 96 degrees in elevation. This provides a wide coverage for the array and beam steering scanning angles.

The RF PCB board contains 16 identical channels that take the 5-6 GHz signals from each antenna element and through a single stage superheterodyne down-conversion, produce IF signals of 400-1400 MHz, which can be digitised by ARESTOR. The RF design also provides a flexible option to introduce a filtering stage if narrower bandwidth (up to 40 MHz) IF signals are preferred.

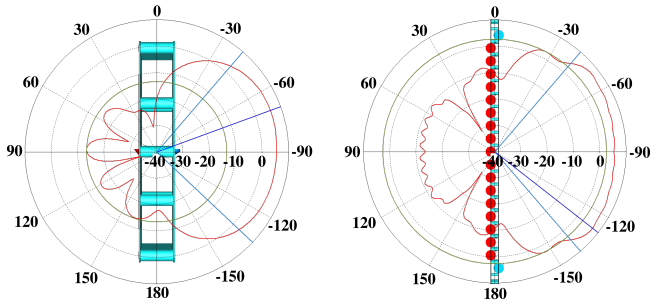

Fig. 11: Single antenna element far-field radiation pattern at 5.8 GHz at $\phi = 90°$ (left) and $\theta = 90°$ (right), simulated in CST Studio Suite. Plots show angle in degrees vs gain in dBi.

A fully assembled prototype of the array unit is shown in Fig. 12. The 16 output channels are provided by 2m coaxial cables, which will be connected to the granddaughter-boards of the upgraded ARESTOR system. Multiple arrays may be used with individual ARESTOR nodes (only making use of 8 channels) to perform multi-static measurements, or two co-located ARESTOR nodes may be used to receive all channels from a single array.

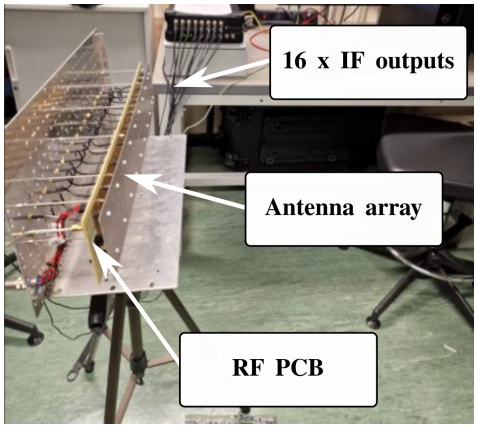

Fig. 12: Fully assembled 16 channel integrated antenna and RF array.

V. Conclusion

In this paper we have described the enhancements being made to the UCL ARESTOR platform replacing the original Xilinx daughter-board with our own modular design to provide flexible access to all 8 ADC and DAC channels. We have further introduced the 16 channel C-band array antenna and associated RF PCB designed at UCL which will be paired with the updated ARESTOR platform to provide a beam steerable RF sensing solution capable of operating as a 16-channel monostatic node or as several spatially separated 8-channel multi-static nodes.

Future work will include testing of the complete system, and development of real-time beamforming within the RFSoC. Following this field trials of the integrated system will take place.

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