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Review

A Comprehensive Review on Planar Magnetics and the Structures to Reduce the Parasitic Elements and Improve Efficiency

Pouya Kolahian *, Ferdinand Grimm and Mehdi Baghdadi

UCL Mechanical Engineering, University College London (UCL), London WC1E 6BT, UK
* Correspondence: pouya.kolahian.19@ucl.ac.uk

Abstract: Due to the need for highly efficient and compact power electronic converters to operate at higher frequencies, traditional wire-wound magnetics are not suitable. This paper provides a comprehensive review of planar magnetic technologies, discussing their advantages as well as associated disadvantages. An extensive review of the research literature is presented with the aim of suggesting models for planar magnetics. Several strategies are proposed to overcome the limitations of planar magnetics, including winding conduction loss, leakage inductance, and winding capacitance. The goal of this study is to provide engineers and researchers with a clear roadmap for designing planar magnetic devices.

Keywords: magnetics; parasitic capacitance; leakage inductance; proximity effect; eddy current loss

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1. Introduction

High-power density and high-efficiency power converters have become popular in a wide range of industrial applications including telecommunications, automotive, aerospace, and data processing. When it comes to achieving high power density, it is inevitable that switch-mode power converters will need to be utilized. Semiconductor devices, magnetics, and capacitors are all components of a switch-mode converter. The sizes of all these elements must be optimized in order to achieve the minimum possible total volume [1].

Magnetic components, such as inductors and transformers, are prominent elements in every switch-mode converter. Despite the other elements, the only solution to decrease the sizes of these elements is to increase the switching frequency [2]. Due to the emergence of wide bandgap (WBG) devices in the past decade, reaching higher frequencies has become possible. This necessitates improvements in the design of magnetic devices to make use of high-frequency switching and build even smaller devices.

According to their geometric properties, magnetic devices can be divided into two classes: wire-wound magnetic devices and planar magnetic devices. Wire-wound magnetic devices differ from planar magnetic devices primarily in their core structures and winding methods [3]. Wire-wound magnetics are wound with round wires, while planar magnetics use thin copper foils manufactured as flat conductors on printed circuit boards (PCBs) or lead frames (LFs). Using PCBs and LFs allows for reliable repeatability in the manufacturing of magnetic components.

High-frequency power-conversion applications are increasingly using planar magnetic devices to replace traditional transformers and inductors. The main features that make planar magnetics particularly attractive [4] for industrial applications include (i) low profiles, (ii) effective heat dissipation, (iii) ease of manufacturing, (iv) repeatability, (v) modularity, (vi) more straightforward implementation of winding interleaving, and (vii) predictable parasitics. As opposed to wire-wound magnetics, planar magnetics have some limitations, such as large interwinding capacitance [5], where there are methods to overcome these

limitations. Compared to traditional transformers, planar magnetic devices are increasingly preferred due to their superior performances at higher frequencies used in power conversion applications.

A deeper understanding of passive components and integrated circuit behavior is necessary with new technologies and higher frequencies. To account for the physical phenomena of planar magnetics, a systematic modeling approach is essential [6]. An overview of planar magnetics is presented in Section 2, including the equivalent circuits, parasitic capacitance modeling, and leakage inductance modeling. As a road map for designing planar magnetics, Section 3 discusses the structures used to optimize and overcome parasitic elements associated with planar magnetics. The concluding section of the report provides a summary of the findings and suggests future directions.

2. Magnetic Characterization of Planar Magnetics

For modeling planar magnetics, the equivalent circuit has been discussed at the outset as it can be used to analyze the complex circuitry of planar magnetics mathematically and to retain all of their electrical properties. These models are expressed with different combinations of parasitic components and the analytical results can be verified through the finite element method (FEM).

2.1. Equivalent Circuits for Planar Magnetics

Several equivalent circuits have been used to describe planar magnetics [7–15]. The simplest description involves using only one impedance, as shown in Figure 1a. In [7], a more detailed model was suggested, as shown in Figure 1b. This model consists of two resistors, one inductance, and one capacitance. The parameters for this model are computed from a series of measurements outlined in [7]. The authors, by using a comparison with FEM and experiment results, show that the model can reliably predict the total capacitance of the transformer, especially in the case of a higher number of inner layers in a PCB.

In [8], an equivalent circuit with two interwinding capacitances and one intra-winding capacitance (shown in Figure 1c) was examined. In addition, the model uses winding resistances and inductances as well as a magnetization inductance. It was stated that this model is especially accurate if the transformer windings possess strong magnetic coupling [8]. This model requires fewer experiments to characterize compared to the traditional six-capacitor model. Using experimental evaluation, it has been demonstrated that this model can predict the behavior of the circuit over a wide range of frequencies. However, its prediction performance decreases as the operating frequency becomes too high.

A model with three parasitic capacitances, which is shown in Figure 1d, was proposed in [9]. This model also provides generally good accuracy for the examined operating frequencies.

An equivalent circuit with six parasitic capacitances was proposed in [10], as shown in Figure 1e. Using an energy-based approach, a model that uses six-parasitic capacitances was derived to describe the dynamic behavior of the model. While the six-capacitor model provides more accurate results compared to the lumped versions, it requires a higher number of tests and has a higher dynamic order. This leads to more complicated controllers and more computationally intensive simulations.

A different modeling approach was suggested by [11–15]. Contrary to the previous approaches, the authors obtained a circuit model by approximating the electromagnetic phenomena inside the transformer with a one-dimensional standing wave and solving the Maxwell equations for this case. The resulting equivalent circuit is shown in Figure 1f. It consists of a number of nonlinear impedances and, thus, is difficult to control. Furthermore, it can be seen that this model does not include parasitic capacitances. Compared to the experiment, the proposed model showed good performance, and each impedance has a direct physical interpretation. The parameters of the circuit model can be derived from the transformer datasheet using a one-dimensional wave propagation approach, as introduced in [11].

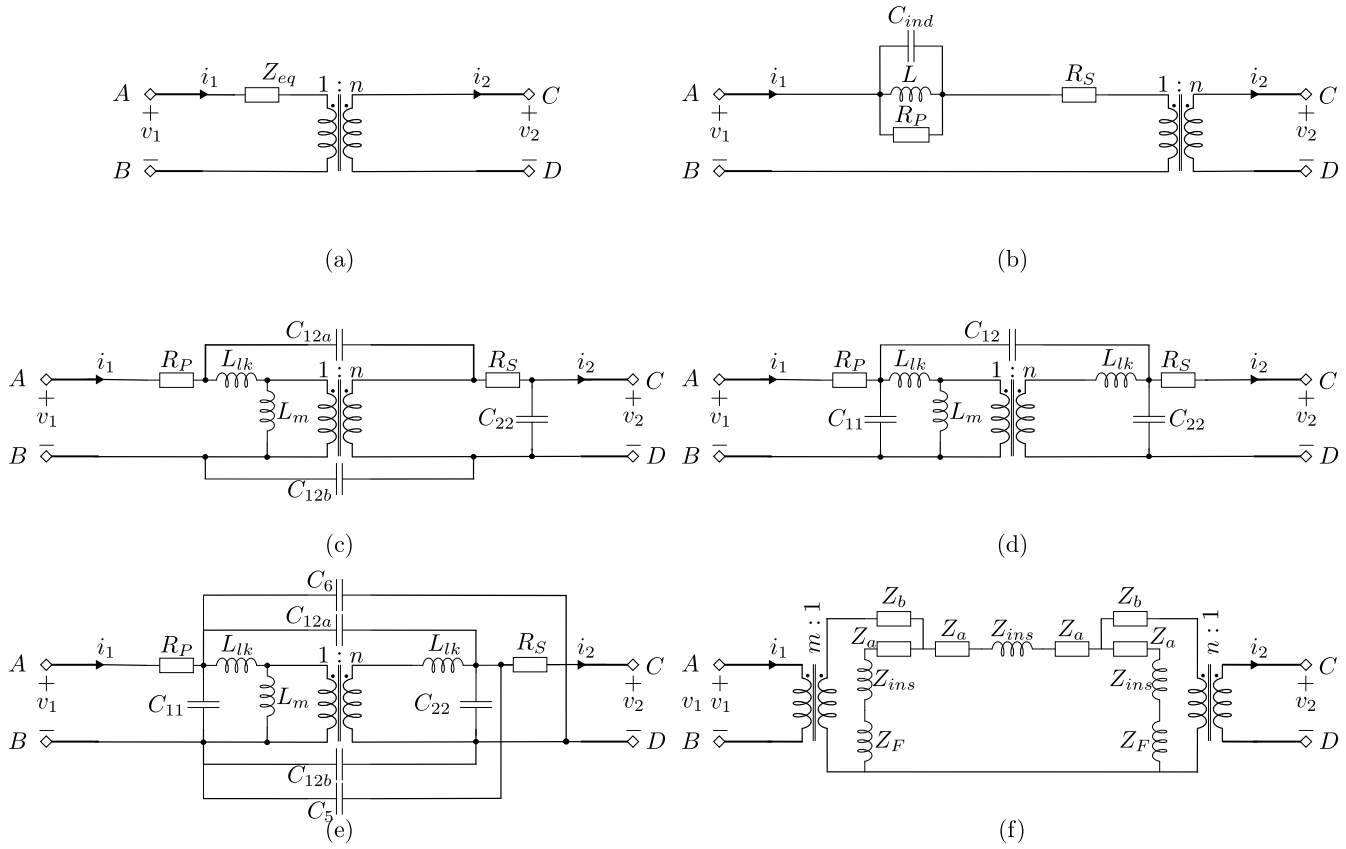


Figure 1. Transformer modeling overview. (**a**) Equivalent circuit with one equivalent AC resistance. (**b**) Equivalent circuit of the model proposed by [7]. (**c**) Equivalent circuit of the model proposed by [8]. (**d**) Equivalent circuit of the lumped model proposed by [9]. (**e**) Equivalent circuit of the six-capacitor model [10]. (**f**) Equivalent circuit of the lumped model proposed by [11].

2.2. Parasitic Capacitance

With regard to different equivalent circuits for planar magnetics, numerous capacitances are present, and the behaviors of these capacitances should be deeply studied. This section discusses the parasitic capacitances that arise in planar magnetics. Initially, parasitic capacitances are discussed in terms of their types, where they occur within the circuits, and what mechanisms cause them. Following that, formulas and experiments are presented that can help estimate parasitic capacitances, as well as how to avoid them. Lastly, their effects on planar transformer-based converters and their interactions with other components are discussed.

In terms of electrical theory, a capacitor can be defined as any pair of conductive objects coupled together. Thus, numerous capacitances will be associated with magnetic devices between different parts of the device and with the surrounding environment. These capacitances are called parasitic capacitances and must be carefully considered during the design stage. At higher frequencies, a capacitor will behave more like a resistor on the verge of shorting out. Thus, parasitic capacitance poses a real problem at high frequencies, while it does not have a significant effect at lower frequencies [16]. With reference to Figure 2, parasitic capacitances can manifest themselves in the transformer in several ways, including (i) turn-to-turn capacitance between two turns in the same winding or different windings (C_{P-S}), (ii) the capacitance between the windings and the magnetic cores (C_{P-C}, C_{S-C}), (iii) the capacitance between the windings/core and the ground (C_{C-G}). The distribution is dependent heavily on the geometry and spatially distributed in nature [17].

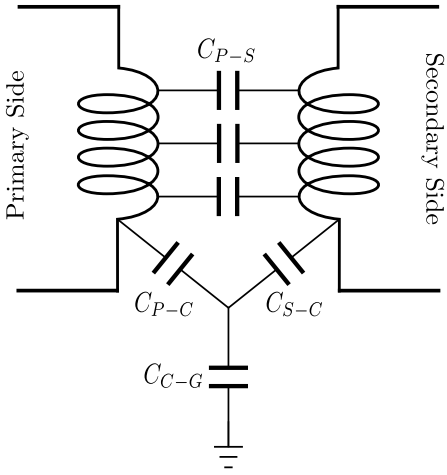


Figure 2. Parasitic capacitance sources in planar transformers. There are four kinds of parasitic capacitances in transformers. Parasitic capacitance between the primary and secondary (C_{P-S}), which is between the windings. Parasitic capacitance between the primary side and the core (C_{P-C}). Parasitic capacitance between the secondary side and the core (C_{S-C}). Parasitic capacitance between the windings/core and the ground (C_{C-G}).

Due to the considerable overlaps between the tracks in different layers of the windings of a planar transformer, there is a large parasitic capacitance between the layers of the primary winding and the secondary winding. The transformer is affected by an undesirable electrostatic coupling between the primary and secondary windings or between the windings and the core which is called common mode (CM) noise. A parasitic capacitance also results between the core and the layers of windings that are exposed to the core. Since the voltages of overlapping layers change rapidly as a result of high-frequency switching, the parasitic capacitances experience a high *dv/dt* value. The CM noise is the result of these oscillating currents that circulate through the circuit at high frequencies and causes EMI problems [18]. Previous studies [7,19] have developed analytical methods to estimate parasitic capacitance values in the design process. This model has also been used to design and optimize DC–DC isolated converters [20,21].

The design of planar transformers in LLC topologies has been the subject of several studies [22,23]. Topologies based on resonance studies suggest that the couplings between the oscillators and the transformer do not adversely affect gain or modulation when the power levels and frequencies are high. Whereas, in dual active bridge (DAB)-based topologies, they amplify the effect of the parasitics in the switches and can degrade the converter performance [24].

With the high-frequency operation, the parasitic capacitance in transformers and inductors has become an issue due to the fact that the impedance is affected considerably by parasitic capacitances. Thus, the operation frequency of these magnetics will be limited [24]. EMI and reduced efficiency are also caused by a high charge inrush current and high-frequency oscillations in the circuit [5]. It is also necessary to provide a reasonable amount of the switching current during the dead time in order to achieve zero-voltage switching for MOSFETs [25]. This causes parasitic capacitances to cause high-frequency current oscillations, so understanding how these oscillations occur is essential to minimizing parasitic effects in devices. It is, therefore, necessary to develop a parasitic capacitance model for planar magnetics in order to account for these effects.

In [24], guidelines for defining acceptable values for parasitic capacitances in transformers were provided, which matched the soft switching of a converter. Two examples were presented to illustrate the effects of winding geometries on transformer parameters. The first design used a PCB, and the thickness was minimized. The second design adjusted different leg heights to study different geometries. In both transformers, the

inductances were minimized through interleaved windings to reduce losses. Layers were built parallel to the turns of the primary winding throughout the primary winding to reduce current density. The first transformer was designed to limit core and winding losses in the transformer without accounting for the constraint of interwinding capacitance. The second configuration was designed to optimize the trade-off between transformer losses and interwinding capacitance.

It is possible to estimate the parasitic capacitances in transformers of interleaved primary/secondary windings, with large copper conductors, using the classical plane capacitor equation [24]:

$$C_{\mathrm{p}} = N_{face} \cdot \epsilon_0 \cdot \epsilon_r \cdot \frac{S_{face}}{e_{\mathrm{FR4}}}. \quad (1)$$

where geometric parameters that affect the capacitance include the number of parallel surfaces N_{face}, the surface area of each S_{face}, and the insulation spacing e_{FR4}. ϵ_0 is the permittivity and ϵ_r is the relative permittivity.

An electrostatic FEM model, to evaluate the parasitic capacitance of a two-turn transformer, was also carried out, which verifies the C_{p} value. The interwinding capacitance rises hyperbolically with the decreasing insulation thickness [24] as shown in Figure 3.

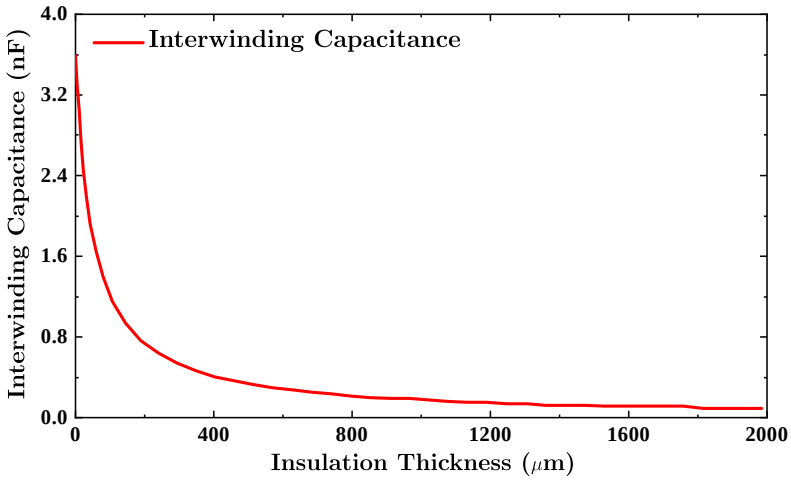


Figure 3. Hyperbolic change of Inter-winding Capacitance Based on the changes in the Insulation Thickness which proves the relation of the parasitic capacitances to the geometry of the magnetics. Reproduced with permission from [24], IEEE, 2019.

2.3. Leakage Inductance

The purpose of this section is to discuss leakage inductances in planar magnetics. Identifying their locations in the circuit and the mechanisms responsible for their occurrences is the first step. Following this, a set of formulas that can be used to estimate leakage inductances will be presented. Lastly, inductance is examined as a function of the distance between the layers and the core.

Leakage inductance is the imperfect coupling of the windings in the circuital model of a high-frequency transformer, and it represents an inductive element in the model [26], as can be seen in Figure 4. In [27], the leakage inductance of transformers is discussed in detail. The energy stored in the leakage inductance results in the generation of voltage spikes in the switches, which leads to lower efficiency and increased losses on the switches [28]. Energy in a low-leakage construction is mostly stored in the windings and the gaps between them. Moreover, the amount of stored energy in the leakage inductance is intrinsically independent of the core geometry and is mostly determined by the geometry of the windings themselves. There is, however, a particular difference in winding geometry caused by different core geometries that may impact the leakage inductance.

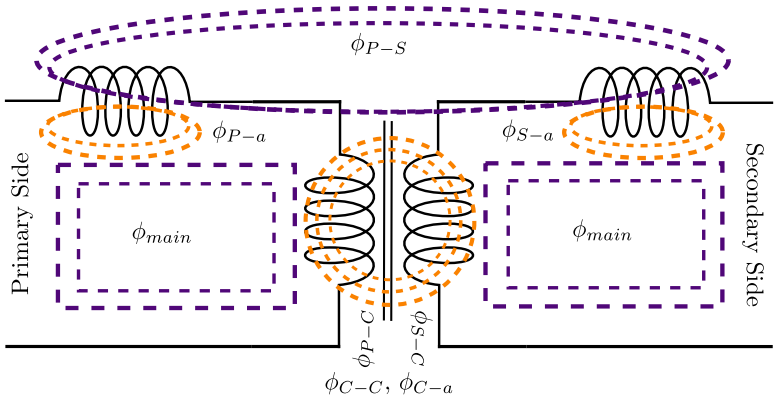


Figure 4. Flux leakage from core to air (ϕ_{C-a}), core to core (ϕ_{C-C}), primary winding to the core (ϕ_{P-C}), secondary winding to the core (ϕ_{S-C}), primary winding to air (ϕ_{P-a}), secondary winding to air (ϕ_{S-a}), primary winding to secondary winding (ϕ_{P-S}), and main flux (ϕ_{main}).

Contrary to popular belief, the leakage inductance of a planar transformer is higher than that of a conventional transformer as an intrinsic property [29]. In [28], a comparison was conducted on the leakage inductance of a planar and a conventional structure, in which the leakage inductance of the planar structure is almost twice that of the conventional one. For the fairness of the experiment, the cross-section of the core, volume of the core, number of turns, and thickness of the conductors were kept the same. With increased core dimensions, the difference in leakage inductances between the two structures will increase. This is mainly due to the fact that the mean turn length (MTL) of planar magnetics is longer. Reference [29] compares the planar structure with other core structures, leading to the conclusion that planar structures do not have a low inductance by design; thus, the use of other methods, such as interleaving, should be considered to reduce the leakage inductance.

In addition, a planar winding with a higher aspect ratio of the conductor width to conductor thickness will naturally have a "radial effect", which reduces leakage inductance [30]. There is a need to find accurate leakage inductance predictions for planar transformers since the winding width in a traditional transformer is much smaller than the winding height. Therefore, maximizing efficiency would require an optimized design. The leakage inductance for a nicely matched resonant frequency has also been investigated in planar transformers, such as LLC converters [31–35].

Research on the properties of planar transformers has focused on obtaining winding losses, largely using Dowell's formula [36]. This formula may also be used to measure leakage inductance in conventional transformers. Accordingly, [37] proposed a novel set of formulas to calculate the self- and mutual inductances of a planar coil on a homogeneous ferromagnetic substrate. It should be noted that these formulas are not suitable for PCB windings with cores and are designed for air core planar windings and thick-film transformers.

As previously mentioned, a common misconception is that planar transformers have low leakage inductance intrinsically, compared to conventional counterparts. A planar transformer has an intrinsically longer MTL than a vertical structure [3]; leakage inductance is, therefore, increased. Dowell's method has been extensively used in order to determine the leakage inductance of wire-wound transformers, whereas significant errors have been observed when applied to planar transformers. The main causes of these errors are as follows:

1. Traditional analysis has only taken account of the leakage inductance at low frequency (frequency-independent), while high-frequency eddy currents have been ignored.
2. The insulators between layers do not figure in traditional analytical expressions due to their small thickness. However, the copper thickness of a PCB winding (35–70 µm) is usually much smaller than its dielectric layer thickness, which is typically 200 µm. As a consequence of this, the analytical error can range up to ≈30%, or even higher [27], with regard to the layout dimensions.

3. Conventional transformers were not affected by the "radial effect".

The currents that are conducted along the inner edge of planar transformer windings concentrate towards the center of conductors. This affects the amplitude of the magnetic field adjacent to the center of the conductors. A novel analytical method was proposed in [30] for leakage inductances in planar transformers that combine all three factors discussed above, especially for "radial effects". This approach separates the eddy current effect and the radial effect of leakage inductance by decomposing the leakage flux into longitudinal and transversal flux fields. With the proposed formula incorporating both high-frequency eddy current effects and radial effects, the accurate prediction of leakage inductance is available in transformers. Total leakage energy takes into account the stored energy from each elementary layer, which can be expressed using the following formula [30]:

$$E_{\text{total}} = E_{\text{p}} + E_{\text{s}} + E_{\text{d}}. \tag{2}$$

where E_{p}, E_{s}, and E_{p} are the energy stored in the primary winding, the energy stored in the secondary winding, and the energy stored in the dielectric layer, respectively. With the same layer thickness in every layer and defined turn, a total leakage inductance can be calculated by the following method:

$$\begin{aligned} L_{lk} &= \frac{\mu_0 \cdot \pi \cdot n_p}{3\ln\left(\frac{r_2}{r_1}\right)} \cdot \left[\frac{(n_p)^2(k_1+2k_2)(n+1)}{\gamma \sinh^2(\gamma h_{\text{p}})}\right] + \\ &\quad \frac{\mu_0 \cdot \pi \cdot n_p}{3\ln\left(\frac{r_2}{r_1}\right)} \cdot \left[\frac{(k_1-4k_2)(n+1)}{2n\gamma \sinh^2(\gamma h_{\text{p}})}\right] + \\ &\quad \frac{\mu_0 \cdot \pi \cdot n_p \cdot h_{\text{i}}}{3\ln\left(\frac{r_2}{r_1}\right)} \cdot \left[2(1+n)\cdot (n_p)^2 + \frac{1}{n} + 1\right]. \end{aligned} \tag{3}$$

$$k_1 = sinh(2\gamma h_p) - 2\gamma h_p. \tag{4}$$

$$k_2 = \gamma h_p cosh(\gamma.h_p) - sinh(\gamma.h_p). \tag{5}$$

$$n = \frac{n_s}{n_p} \tag{6}$$

where n_p and n_s represent the number of turns in the primary and secondary. r_1 and r_2 are the distances between the center and the inner and outer edges of the core, respectively. h_p is equal to h_s, i.e., the thicknesses of the primary and secondary windings. h_i is the thickness of the dielectric. γ and μ_0 are the propagation constant and permeability of air, respectively.

In [30], leakage inductance is compared between Dowell's calculation [36] and a previous work presented in [38]. Along with the proposed calculation, an FEA simulation and experimental measurements are reported in the paper. The "radial effect" was neglected in the mentioned works, which led to over-estimations of the leakage inductance. Overall, the experimental measurement closely matches the proposed method.

Effect of PCB Layer Distance on Inductance

A structure of a planar transformer with an adjustable air gap (l_{g}) and gaps between different layers (l_{b}) is shown in Figure 5. By changing the air gap l_{g}, the magnetizing inductance of the transformer can be adjusted. This method uses two separate boards for the primary and secondary windings, providing an additional degree of freedom (l_{b}). As a result, l_{b} can be controlled to achieve precise leakage inductance values, which is a key design criterion for resonant converters. It is important to design the air gap length

accurately to obtain the correct transformer parameters. The air gap length is calculated as follows: [1]:

$$l_g = \left(\frac{N^2}{L_m} - \frac{l_e}{\mu_0 \mu_r A_e}\right) \mu_0 A_e. \quad (7)$$

where N is the number of primary side windings. L_m is the magnetizing inductance. l_e and Ae are the core's effective length and area, respectively. μ_0 and μ_r are the air permeability and relative permeability.

Having established the transformer parameters, the leakage inductance can then be determined by tuning l_b. In order to calculate the l_b, the length of the core's leg, the air gap, and the thickness of the board must be taken into consideration.

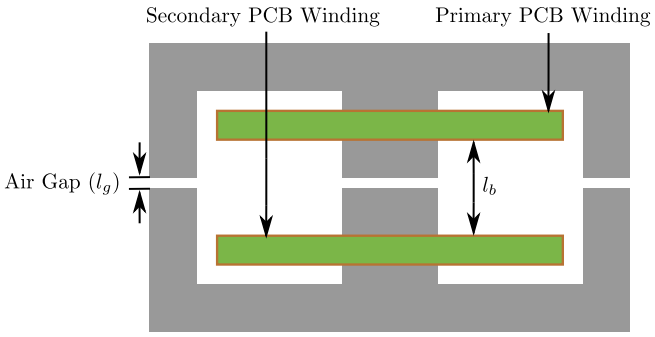


Figure 5. Structure of the planar transformer with adjustable leakage and magnetizing inductance. L_g (for adjusting the magnetizing inductance and leakage inductance) is the air gap and L_b (for adjusting the leakage inductance precisely) is the distance between the primary and secondary windings. Reproduced with permission from [1], IEEE, 2019.

2.4. Finite Element Analysis

Several different approaches have been introduced to model the behaviors of planar transformers. For electromagnetic analysis, FEA models [11,39–48] of the device provide accurate results compared to experiments [39,47] and reveal the detailed distributions of magnetic fields produced by the transformer. Another use of FEA is to obtain the parameters that are used in circuit models introduced in the previous section. In this way, it is possible to obtain the leakage inductance [44], or the entire impedance matrix [45] of the planar inductor. Due to the quasi-2D structure, the model can be reduced to a 2D one to reduce the computational complexity [40]. Moreover, a set of FEM models can be formulated for parameter variations and serve as the basis for the design and optimization of the transformer [42,43]. It is possible to extend the FEA to other physical domains in the FEA to obtain a more accurate picture of the situation. In [46], the authors built a numerical thermal model of a planar inductor based on FEA computations. When the behavior of the transformer with a core is of interest, the core can be included in the FEA. The core can be modeled as homogenous and the effects of lamination can be included by setting an anisotropic permeability [48]. Furthermore, the authors showed that any clamping can be neglected in the modeling without major decreases in accuracy. Even though FEA is an excellent tool, a 3D model is necessary for some arrangements, such as Litz structures, since 2D simulations cannot provide accurate results. A three-dimensional analysis of a planar magnetic device with a Litz structure faces two major challenges: the power and time required to simulate the model, as well as the requirement to provide accurate geometric representations of the structure [49].

3. Optimization of Planar Magnetics

As mentioned previously, a planar transformer is composed of flat foil patterns on a printed circuit board, which limits the number of turns possible. Meanwhile, fewer turns are required due to the larger magnetic cross-sectional area. Additionally, the flat form of the magnetic core material maximizes the surface area for heat dissipation. Due to

the printed circuit nature of the winding, the spacing between turns and layers is highly consistent. As a result, interwinding capacitance is invariant, and the winding interleaving facilitates reduced AC losses. In light of all of these factors, planar transformers are efficient and have excellent repeatability.

Optimizing planar windings is a complicated procedure as a vast number of winding techniques and geometries are possible. Planar windings can be modeled in many ways, requiring optimization based on application-specific factors. These include efficiency, power density, and other physical constraints, such as maximum footprint, design complexity, and fabrication capability. As a result, optimization of planar windings requires a comprehensive approach that considers multiple objectives, including performance, manufacturability, and reliability. By evaluating the trade-offs between these objectives, an optimal design can be achieved that meets the application requirements.

Manufacturing even a simple planar winding involves making a large number of complex decisions. The winding shape, inner and outer dimensions, number of turns, spacing between conductors, number of layers, conductor thickness, and conductor width are just a few critical decisions. Each of these decisions can have a significant impact on the performance of the product. For instance, the number of turns and the spacing between conductors can affect the efficiency and power density of the final product. Similarly, the number of layers and the conductor width and thickness can influence the maximum footprint and fabrication complexity.

Different design techniques have been employed to enhance planar magnetics, such as interleaving, track-width reduction, removing inner turns, shifting, changing the winding arrangement, and Litzing methods, as shown in Figure 6. These methods enable engineers to identify the most suitable design parameters and configurations to optimize planar magnetics for a given application, resulting in a reduction of leakage inductance, parasitic capacitance, and AC resistance. Taking into account the various factors that influence the performance of planar magnetics, these techniques can be utilized to decrease the total power loss. For instance, interleaving can reduce leakage inductance by stacking multiple layers of windings together and reducing the MMF, while track-width reduction can shorten the total length of the traces, thereby reducing AC resistance. Removing inner turns, shifting, and changing the winding arrangement can help minimize the leakage inductance and parasitic capacitance of the magnetics. Finally, Litzing methods can improve the efficiency of planar magnetics by decreasing AC resistance. Here is a summary of the methods that have been used to optimize planar magnetics.

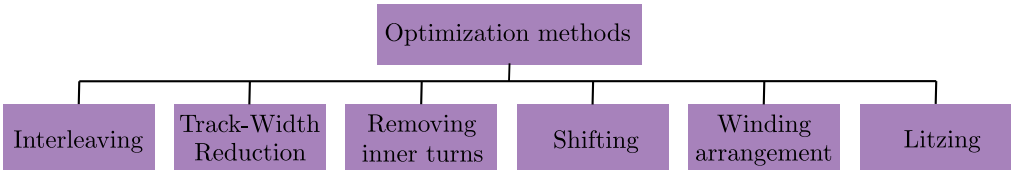


Figure 6. An overview of the optimization methods discussed in this paper. The following methods are described here: interleaving [50–53], track-width reduction [54–58], removing inner turns [59], shifting [17], changing the winding arrangement [17], and Litzing [60–64].

3.1. Interleaving

Interleaving involves dividing the windings into several portions and alternating between the primary and secondary side windings to reduce the MMF (magnetomotive force), as depicted in Figure 7.

3.1.1. Fully Interleaved

The losses in the windings of transformers increase dramatically at high frequencies due to eddy currents, making a detailed model of winding losses necessary for designing or optimizing transformers for a range of frequencies and winding arrangements. AC losses, such as proximity effect losses and skin effect losses, have a negative impact on

transformer performance in high-frequency power conversion applications. Eddy currents are generated within a conductor by the alternating field generated by the current, which tends to cancel the field produced by the original current. The current in a conductor tends to have a higher density near the surface than at the center, resulting in increased resistance, known as the skin effect. The proximity effect occurs when an adjacent conductor carries a current, causing a circulating current within the conductor due to the time-varying field generated by the current in the adjacent conductor. The proximity effect and the skin effect cause non-uniform cross-sectional current density, resulting in greater resistance in the winding at higher frequencies. As shown in [65], the skin effect of an infinite foil conductor can be illustrated using the relative resistance of AC to DC:

$$\frac{R_{ac}}{R_{dc}} = \frac{\xi}{2}.\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi}. \tag{8}$$

where $\xi = h/\delta$, δ and h are the skin depth and thickness of the conductor. The expression for the AC resistance of the n^{th} layer is derived based on Dowell's assumptions and the solution for the general field of the distribution of current density in an infinite foil conductor [65,66].

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\xi}{2} \cdot \left[\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + (2m-1)^2.\frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}\right]. \tag{9}$$

where $R_{ac,m}$ and $R_{dc,m}$ are the AC and DC resistances of the windings, respectively. m can be defined as:

$$m = \frac{F(h)}{F(h) - F(0)}. \tag{10}$$

where $F(0)$ and $F(h)$ are the MMFs at the layer's boundary. The first term in (9) is the same as (8), which represents the skin effect. The proximity effect is represented by the second term. When the winding is multilayered, the proximity effect loss may systematically outweigh the skin effect loss, depending on m, which is a function of the winding arrangement. If the excitation voltages of the primary and secondary windings are in phase, transformer windings that are interleaved can minimize proximity loss significantly. MMF distributions can be seen in Figure 7 for interleaving and non-interleaving winding arrangements. Different results can be achieved m for fully interleaved and non-interleaved structures, as shown in Figure 7, based on the calculation done in (10).

The current distribution inside conductors can be explored using an FEA tool to explain the eddy current effect in two different arrangements. Figure 8a,b show the current distributions for windings with and without interleaving, respectively, when the excitation frequency is 50 kHz. Two-dimensional planar transformer models with cylindrical symmetry around the Z-axis have been constructed, and all conditions in both models are the same except for the winding arrangement. From the figures, it is evident that the current density decreases as we move away from the Z-axis due to the DC "spirality" effect (the non-uniform distribution of the DC along the spiral). The increased current density is further amplified by the skin and proximity effects when the frequency is high. Hence, the color division of the current distribution is a result of the DC spirality effect, proximity effects, and skin effects. The DC spirality effect will not contribute to AC resistance. Figure 8a indicates that the current density on the non-interleaved arrangement tends to be elevated due to the proximity effect. There is a tendency toward the conductor surface in the layer close to the interface between the primary and secondary layers; therefore, the color division area decreases, which results in a higher AC resistance.

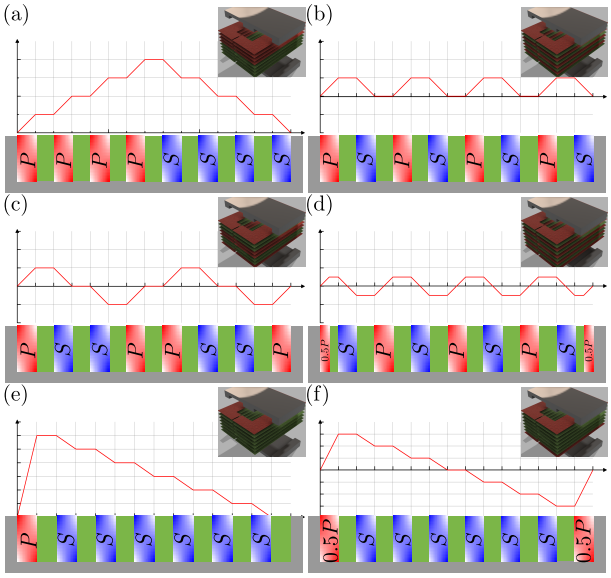
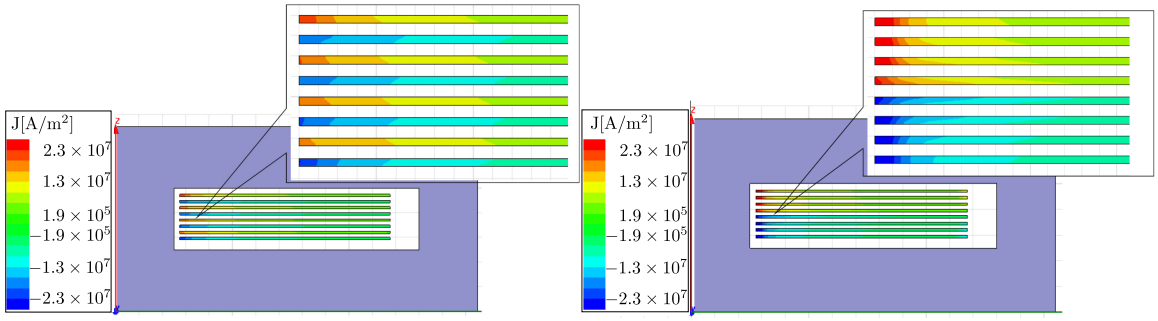


Figure 7. MMF distributions; (**a**) non-interleaved arrangement (P-P-P-P-S-S-S-S), (**b**) fully interleaved arrangement (P-S-P-S-P-S-P-S), (**c**) alternative interleaved arrangement (P-S-S-P-P-S-S-P), and (**d**) improved interleaved arrangement (0.5P-S-P-S-P-S-P-S-0.5P), (**e**) non-interleaved arrangement for insulation requirements while having higher voltages (P-S-S-S-S-S-S), (**f**) partially interleaved arrangement for insulation requirements while having higher voltages (0.5P-S-S-S-S-S-S-0.5P).



(**a**) (**b**)

Figure 8. Comparison of current distribution in the (**a**) fully interleaving arrangement, and (**b**) non-interleaving arrangement. The color division of the current distribution result from the DC spirality effect, proximity effect, and skin effects. Reproduced with permission from [50], IEEE, 2010.

The leakage inductance in total can be calculated as follows:

$$L_{lk} = \mu_0 \cdot \frac{l_w}{b_w} \cdot \left[\frac{46(h_1 + h_2)}{3} + 44h_\Delta \right]. \tag{11}$$

where h_1 and h_2 are the layer-thickness of the primary and the secondary respectively, and h_Δ is the height of the insulator layer. l_w is the length of each turn, and b_w is the width of each turn. Applying the same procedure, for a fully interleaved arrangement, the leakage inductance can be deduced in the following manner:

$$L_{lk} = \mu_0 \cdot \frac{l_w}{b_w} \cdot 4 \left[\frac{(h_1 + h_2)}{3} + h_\Delta \right]. \tag{12}$$

The leakage inductance can be significantly reduced with a fully interleaved system. In addition to winding structures, certain physical parameters, such as conductor thickness and width, insulator thickness, and number of turns, can also affect leakage inductance in planar transformers [49]. Parasitic elements in transformers cause leakage inductance,

limiting the slope of the main switch current between zero and the rated value, which reduces the rate of commutation between output diodes. Furthermore, the energy stored in the leakage inductance is released, generating voltage spikes that can cause EMI problems on the main switch and increase switching losses, thus lowering its efficiency [67].

General full interleaving significantly reduces leakage inductance. The lower MMF ratio (m) reduces the AC resistance by weakening the proximity effect among adjacent layers. In each layer, the MMF is reduced (as shown in Figure 7b), which reduces the energy associated with leakage inductance. However, a higher parasitic capacitance can be found at seven intersections between the secondary and primary windings. A new interleaving method, shown in Figure 7c, has been introduced in [24]. In this layout, the interwinding capacitance is lower than in the fully interleaved arrangement, at the cost of a negligible increase in intra-winding capacitance.

An improved interleaving method compared to the methods mentioned before was proposed in the [50], which is shown in Figure 7d. Different winding arrangements are compared for the purpose of evaluating both their pros and cons.

The comparison of the three main models of interleaving and non-interleaving methods is shown in Figure 9. The non-interleaved model (Figure 7a) has the highest leakage inductance, but due to only one intersection between the primary and secondary windings, it achieves minimal parasitic capacitance. In the P-S-P-S-P-S-P-S interleaving model (Figure 7b), the AC resistance and leakage inductance are dramatically reduced as it is fully interleaved. With a fully interleaved model, the overall MMF is reduced throughout, but there are more intersections between the primary and secondary windings, resulting in higher parasitic capacitance. In the P-S-S-P-P-S-S-P interleaving model, also known as alternative interleaving (Figure 7c), the MMF distribution is similar to that of the fully interleaved model, while the number of intersections is smaller, and as a result, the parasitic capacitance is lower.

A better interleaving arrangement is the 0.5P-S-P-S-P-S-P-S-0.5P interleaving model that accommodates top and bottom turns together as a layer so that the MMF ratio m is further reduced. The analytical MMF distribution of this model is illustrated in Figure 7d. The MMF ratios (m) on each branch may not be 0.5 due to the probable errors in impedances on the top and bottom layers. However, this ratio (m) can be lowered below 1. Thus, as shown in Figure 9, a lower AC resistance can be observed in the higher frequencies, and a gradual rising trend can be seen above the 100 kHz frequency point. A significant advantage of this arrangement is that it reduces AC resistance and leakage inductance while also reducing parasitic capacitance compared with the alternative interleaving arrangements. Adding quadruple interleaving will also result in $m = 0.5$ by splitting the secondary [50].

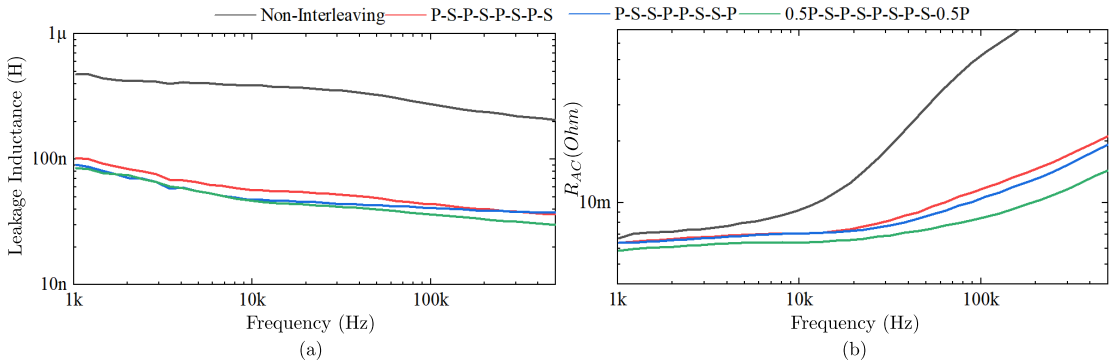


Figure 9. Comparison of the (**a**) leakage inductance and (**b**) AC resistance measurements for non-interleaved, fully interleaved (P-S-P-S-P-S-P-S), reduced intersection-interleaving (P-S-S-P-P-S-S-P), and improved-interleaved configurations (0.5P-S-P-S-P-S-0.5P). Reproduced with permission from [50], IEEE, 2010.

Table 1 compares the different interleaving models with the non-interleaving method as the reference model. The improved method reduces parasitic capacitance while also decreasing inductance and AC resistance.

Table 1. Comparison of AC to DC resistance, leakage inductance, and parasitic inductance of non-interleaved and three different interleaving structures. The results are normalized based on the non-interleaved configuration.

	Rac*/*Rdc	**Leakage**	**Parasitic**
	(pu)	**Inductance (pu)**	**Capacitance (pu)**
non-interleaved	1/1	1	1
fully interleaved	0.28/0.94	0.135	8.18
P-S-S-P-P-S-S-P	0.31/0.95	0.146	3.69
0.5P-S-P-S-P-S-0.5P	0.24/0.87	0.125	3.38

3.1.2. Partially Interleaved

Transformers with isolation requirements (such as those working with higher voltages) would not benefit from a full interleaving of windings. Consequently, leakage inductance can be reduced by using partial interleaving. A partially interleaved structure is presented in [51]. According to MMF calculations, partial interleaving (Figure 7f) reduces leakage inductance compared to the non-interleaved (Figure 7e) structure. Primary and secondary windings of these structures differ primarily in their insulation thicknesses, while the other parameters are identical. With the partially interleaved structure, there are two parallel primary windings and larger insulation between primary and secondary windings, while non-interleaved structures have single primary windings and thinner insulation between the primary and secondary windings. MMF primarily occurs in the magnetic core window because the magnetic reluctance in the inner core is so small.

The proposed method was tested using a planar transformer for a traveling-wave tube amplifier with both a partially interleaved and non-interleaved structure. Results from data collected on both the partially interleaved and non-interleaved structures are presented in Figure 10, showing an approximately 30% decrease in the leakage inductance.

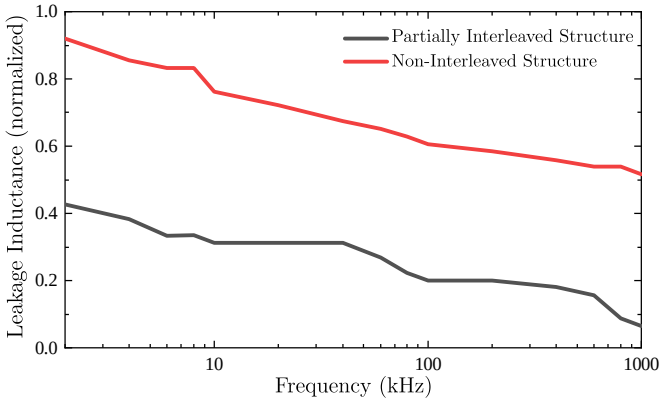


Figure 10. Normalized leakage inductance in partially interleaved and non-interleaved structures. It is visible that leakage inductance was reduced by around 30% for the partially interleaved structure. Reproduced with permission from [51], IEEE, 2010.

In addition, the transformer had an additional primary winding and thicker insulation layer, increasing its complexity. After analyzing the simulation results, it can be stated that the proposed partially interleaved structure is acceptable for high-voltage high-frequency applications.

In [52], the authors worked with high-voltage fields using planar transformers and accounted for the parasitic elements. An improved interleaved structure was proposed for a multi-output transformer in high-voltage and high-frequency applications. The proposed method was compared with several other methods with and without interleaved design, as can be seen in Figure 11.

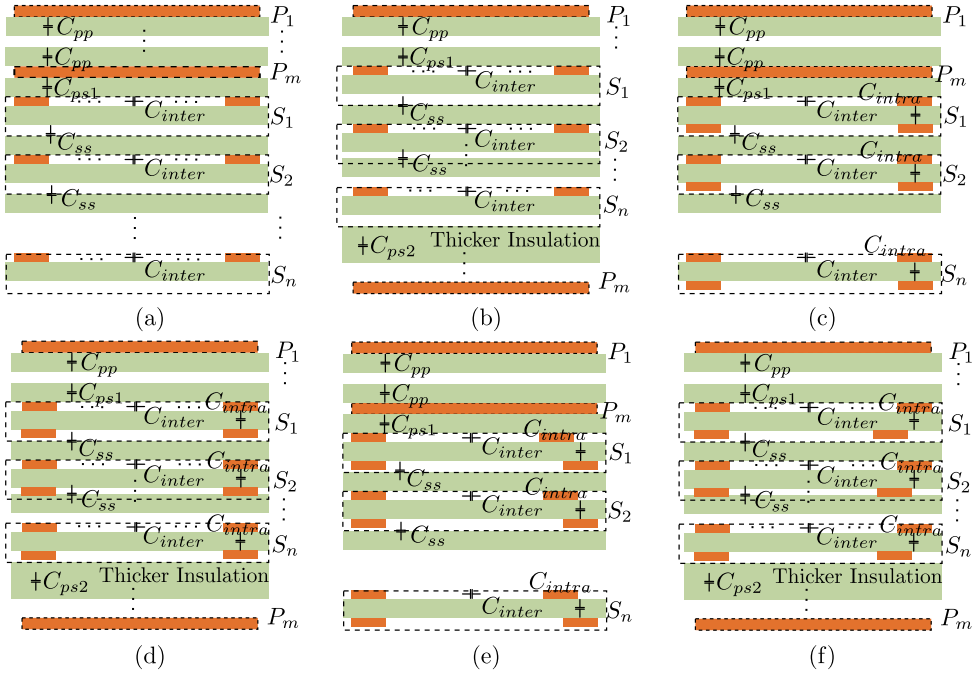


Figure 11. Multi-output transformer structures for high-voltage high-frequency applications: (**a**) W_1 (non-interleaved, single layer), (**b**) W_2 (partially-interleaved, single layer), (**c**) W_3 (non-interleaved, two-layered), (**d**) W_4 (partially-interleaved, two-layered), (**e**) W_5 (non-interleaved, non-overlapped), (**f**) W_6 (partially-interleaved, non-overlapped) [52].

A comparative analysis of the proposed structure and other typical structures was carried out with leakage inductance, AC resistance (R_{AC}), R_{AC}/R_{DC}, as well as AC capacitance (Cp). The leakage inductance was reduced by half with the partially interleaved structures (W2, W4, and W6) compared with non-interleaved structures (W1, W3, and W5).

The R_{AC}/R_{DC} can be used to reflect characteristics associated with high frequencies. The degree of interleaving of the products (W2, W4, and W6) affected the results regarding the R_{AC}/R_{DC}. Even though it has been proven that W2 has the lowest ratio of AC and DC resistances, W4 has a lower DC resistance than W2, meaning that its AC resistance is still lower than W2.

Compared to their non-interleaved counterparts (W1, W3, and W5), partially interleaved structures (W2, W4, and W6) exhibit superior high-frequency characteristics. At a low frequency (below 500 kHz), the R_{ac} of W4 is the lowest, mainly as a result of a lower DC resistance. With the frequency increased to 500 kHz, the R_{ac} of W4 will equal that of W2. Conversely, with a higher switching frequency, the R_{ac} of W4 will be greater than that of W2, which results in lower losses at higher frequencies.

While operating at higher frequencies, it can be concluded that the partially interleaved, single-layer structure, W2, exhibits better high-frequency properties and lower copper loss. Additionally, the partially interleaved structure has a 50% reduction in the R_{ac} compared to the non-interleaved structure. It is, however, possible that the critical frequency differs depending on the application.

In partially interleaved structures, C_p is larger than that of the corresponding non-interleaved structure because of the extra capacitance created between its primary and secondary windings. Among the three partially interleaved structures, W4 has the highest C_p due to its high intra-winding capacitance (C_{intra}) as well as the largest overlapped

winding area. On the other hand, W6 has a lower C_p due to its smaller overlapped area compared with W4, but there exists a significant intra-winding capacitance (C_{intra}) responsible for the AC capacitance of W6. W2 is the least capacitive structure among all partially interleaved structures. The turns are stacked into one layer and the opposite layer is only used for the outgoing line. By doing this, the C_{intra} is greatly reduced, and therefore the C_p of a single-layered structure is significantly lowered.

Based on Table 2, it is evident that W1 and W2, with low C_p, are desirable. Accordingly, in order to optimally design the planar transformer from different perspectives, trade-offs must be made. Taking everything into consideration, W2 appears to be the most suitable option for high-voltage and high-frequency applications with multiple outputs, due to its low R_{ac}, low L_r, and low C_p.

Table 2. Comparison of leakage inductance, AC resistance, and parasitic capacitance of winding arrangements W1–W6 (partially interleaved and non-interleaved structures), normalized according to W1.

Winding	L_{lk} (pu) (500 kHz)	R_{ac} (pu) (500 kHz)	C_p (pu)
W1	1	1	1
W2	0.48	0.52	0.145
W3	1.08	1.09	0.590
W4	0.47	0.50	0.594
W5	1.10	1.01	0.333
W6	0.52	0.51	0.359

3.1.3. Paired-Layers Interleaving

CM noise is propagated by large parasitic capacitances between the primary and secondary layers of the PTs, thereby causing EMI problems. The improved winding method in [53] is designed to overcome CM noise and unwanted resonant frequency in LLC PTs. The proposed method would help make LLC converters slim and flat (with high-power density) by eliminating the need for bulky CM chokes. In addition, the novel winding method offers low inductance and AC resistivity, which are also crucial characteristics for high-efficiency transformers. The main causes for CM noise in LLC transformers and a comprehensive approach that targets all sources of CM noise in a transformer were discussed in [53].

The goal of this approach is to eliminate CM noise to almost zero by identifying where it originates. CM noise can be attributed to three principal causes: (i) IP-S is caused by the overlapping of primary and secondary layers, (ii) IP-C is caused by the interaction between primary layers and core, and (iii) IP-C-S is caused by the coupling between primary and secondary layers through the core.

By using the paired-layers interleaving method, turns with high *dv/dt* will be shielded, and turns with the same *dv/dt* will be overlapped. Thus, the elimination of the circulating current between the primary and secondary (known as CM noise) is possible. Experimental results from the proposed winding method show 11–20 dBμV of CM noise reduction compared to the traditional winding method with the same parasitic capacitance.

The IP-S effect is generated by the intersection of the primary and secondary layers of the transformer, and it is the most significant part of the CM noise. A typical scenario is depicted in Figure 12a, where two layers that operate separately (from the primary and secondary) cross one another. A model of electrostatic behavior can be constructed based on six capacitors, as shown in Figure 12b (with each terminal having a capacitor between them) [53]. The total generated CM noise between these layers can be determined by summing up the currents in capacitors C_{ac}, C_{ad}, C_{bc}, and C_{bd} (CM noise is not contributed

by capacitors C_{ab} and C_{cd} because they are in the same winding). The currents flowing through the capacitors are as follows: [53]:

$$i_{ac} = C_{ac}\left(\frac{dv_a}{dt} - \frac{dv_c}{dt}\right), \tag{13a}$$

$$i_{ad} = C_{ad}\left(\frac{dv_a}{dt} - \frac{dv_d}{dt}\right), \tag{13b}$$

$$i_{bc} = C_{bc}\left(\frac{dv_b}{dt} - \frac{dv_c}{dt}\right), \tag{13c}$$

$$i_{bd} = C_{bd}\left(\frac{dv_b}{dt} - \frac{dv_d}{dt}\right). \tag{13d}$$

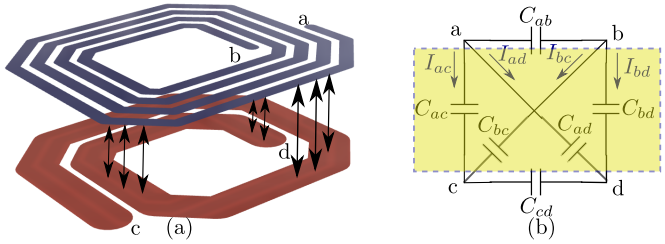


Figure 12. CM noise generation when primary and secondary layers overlap. (**a**) Physical presentation of the overlapping. (**b**) Equivalent parasitic capacitance model that shows how CM noise is generated.

By summarizing the above equations, we can derive the total amount of CM noise. To achieve zero CM noise from overlapping layers, there needs to be a condition in which this sums to zero [53]. The first requirement concerns the *dv/dt* between the overlapping layers:

$$\frac{dv_a}{dt} = \frac{dv_c}{dt}, \frac{dv_b}{dt} = \frac{dv_d}{dt}. \tag{14}$$

The achievement of these equalities requires the fulfillment of two conditions. It is imperative that the overlapping layers have the same number of turns as well as a similar *dv/dt* at the ports of the overlapping layers. The overlap of specific primary and secondary turns is the only way this can be achieved. By taking (11) into consideration, two variables can be eliminated, resulting in the following equation:

$$i_{CM} = i_{ad} + i_{bc} \tag{15}$$

$$= C_{ad}\left(\frac{dv_a}{dt} - \frac{dv_d}{dt}\right) + C_{bc}\left(\frac{dv_b}{dt} - \frac{dv_c}{dt}\right) \tag{16}$$

$$= (C_{ad} - C_{bc})\left(\frac{dv_a}{dt} - \frac{dv_b}{dt}\right) \tag{17}$$

Neither dv_a/dt nor dv_b/dt can be equal because they belong to the same winding. In order to make (14) equal to zero, C_{bc} and C_{ad} need to be equal. By means of symmetry, it is possible to ensure that C_{ad} and C_{bc} are equal, as the value does not matter. As long as the overlapping layers are symmetrical, there will be the same number of turns and the PCB layout, and the windings will be rotated by 180°. The following equations can be valid due to symmetry:

$$C_{ad} = C_{bc}, \quad C_{ab} = C_{cd}. \tag{18}$$

Under these conditions, the CM noise equals zero.

There is also the possibility of CM noise propagating through the core. The amount of CM noise produced by the core overlap is much less than that generated by the primary and secondary layers. However, in order to reduce the amount even further, it is necessary to prevent the production of CM noise in the core. In addition, the portion of the CM noise that is generated from capacitive coupling between the primary and secondary windings

through the core is called the IP-C-S, which can be reduced further by protecting the primary layers against interferences [53]. As a result, both the top layer and bottom layer should belong to the secondary, and the primary layers should encapsulate the secondary layers.

With the proposed method, the noise generated by the core is minimized regardless of the structure of a transformer. The performances of traditional interleaved planar transformers have been reduced at the expense of CM noise. By integrating this feature into planar transformer design, a well-known trade-off between minimizing AC resistance and minimizing CM noise can be resolved.

3.2. Track-Width Reduction (TWR) and Inverted TWR

The TWR technique has been shown to decrease the leakage inductance as the track width is decreased from unity, reaching a minimum before increasing the resistance as further reductions are made [68]. To improve the design of spiral windings in planar systems, several approaches have been proposed [54]. An analytical method has also been developed for calculating the resistance of spiral windings, whether circular or rectangular, with varying track widths [55]. Inductors incorporating square spirals for radio frequency applications have also demonstrated the benefits of track width variations. Different dimensioning methods, resistance models, and width-varying procedures are used in these important contributions to improve some particular cases of the more common spiral winding construction [69].

There have been extensive discussions addressing the drawbacks of planar transformer designs, including variable capacitance caused by the additional layers, turns, and windings combined [3]. The high parasitic capacitance produced by an array of planar conductors with high voltage differences stacked on top of each other can alter waveforms and reduce self-resonance frequencies, resulting in high shoot-through currents.

The planar spiral with inverse TWR was proposed in [56], where the next layer has a TWR less than unity, followed by a TWR greater than unity for less copper overlapping between the layers, as shown in Figure 13. With this technique, overlapping conductors are reduced as well as the overall voltage gradient between layers, resulting in a reduction in the general capacitive energy of the spiral winding. The design of a prototype planar coil winding and analysis of its *R*, *L*, and *C* characteristics indicate that the proposed technique reduces the parasitic capacitance by the same amount on par with a control coil winding; it also significantly reduces the resistance.

(**a**) (**b**)

Figure 13. Planar spiral winding of two adjacent layers without turn connections for (**a**) traditional TWR (top layer) and (**b**) inverted TWR (bottom layer). This type of winding allows for less leakage inductance in the transformer as the track width is decreased from unity, dropping to a minimum before increasing the resistance as further decreases are made. Reproduced with permission from [56], IEEE, 2010.

The inverted TWR spiral winding structure with a planar spiral is also able to reduce the interlayer capacitance in order to reduce heat loss [56]. In this approach, one layer of turns is reduced uniformly from the outside to the inside by a constant ratio, and on the next layer, the reverse is done. This results in a greatly reduced amount of copper

overlapping and a much smaller voltage drop between the largest overlapped areas. Based on the winding dimensions and layer separation shown in Figure 14, it was demonstrated that capacitance could decrease by 50% while AC resistance could drop by up to 20% [56].

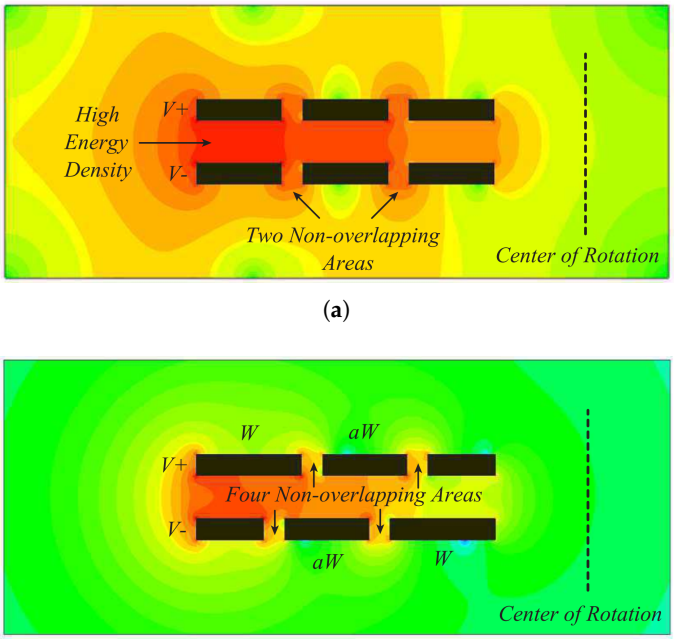


Figure 14. FEA capacitive energy cross-section of (**a**) a traditional planar spiral winding and (**b**) the proposed inverse TWR planar spiral winding. An extremely high capacitive energy area can be found at the input terminals of the traditional winding due to its overlapping conductors. With the proposed winding, much less energy is trapped at the input terminal since the winding provides double the areas without overlap. Reproduced with permission from [56], IEEE, 2010.

3.3. Removing Inner Turns (Hollow Effect)

In the presence of higher frequencies, the eddy current phenomenon is strongly influenced, resulting in a reduced effective current area of the coil and, thus, the AC loss cannot be avoided [57]. This effect is either caused by high-frequency currents in the conductor, skin effect, or it can be a result of external conductors (proximity effect). Figure 15 shows selected flux lines in a typical three-turn planar spiral winding, illustrating the flux lines that cause the skin and proximity effects [58]. The figure also illustrates a special phenomenon occurring in the center of the winding, where the flux lines all point in the same direction. Consequently, planar conductors will suffer increased eddy current losses under this additive flux. In order to evaluate the impact of this issue qualitatively, FEM simulation was used. In Figure 16a, a top-down view of the magnetic field strength simulation indicates that a high-frequency loss was induced on the inner turns, as the field was strongest in the center of the spiral. A cross-sectional view of the flux vectors in Figure 16a is shown in Figure 16b. In the center of the winding, there are distinct patterns of the increased magnetic flux, without much extensions (vertically). Magnetic flux vectors have decreasing radial strength until they reach their weakest point outside the windings, where they repel each other.

When the internal turns in a spiral winding are too wide, they contribute the most resistive losses, thereby reducing the overall inductance and, as this winding is relatively small compared with the outer winding, this poses a critical problem. To resolve this problem traditionally, inner turns were removed to decrease inductance in exchange for much lower resistance (the hollow effect) [59], which is unacceptable in wireless power transfer, considering a resonant application, the resonant frequency will change significantly even with a change of 5% or 10% in inductance.

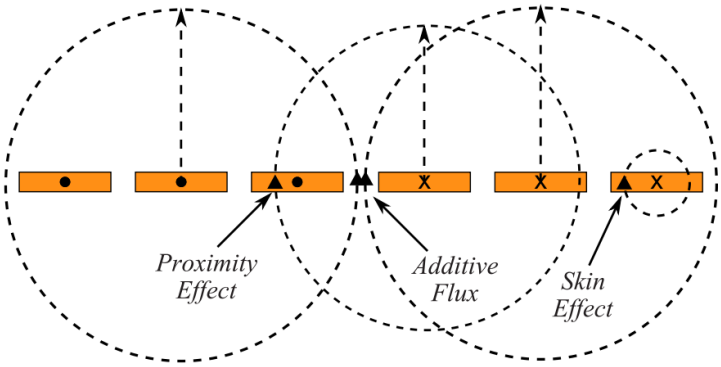
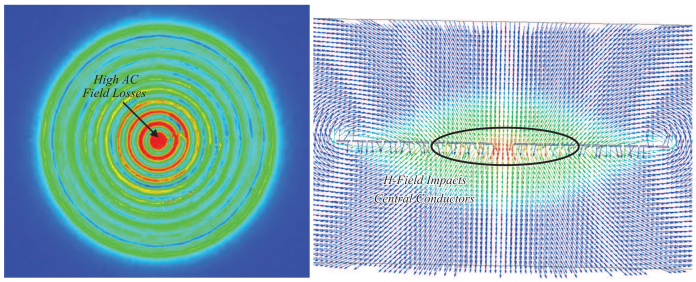


Figure 15. Idealized flux lines in a 3-turn planar spiral winding demonstrate the skin effects, proximity effects, and additive flux in the center of the winding. The direction of the current is shown by the dot and cross notation [58].



(**a**) (**b**)

Figure 16. (**a**) Magnetic field strength, H, for a horizontal cross-section of a circular planar spiral winding. (**b**) Magnetic field intensity vector, $\tilde{H}$, for a vertical cross-section of a circular planar spiral winding [58].

Two algorithms were used in [58] to reduce the resistance in the interior turns: increasing the internal radius and applying a non-unity TWR. By doing so, the internal turns will prevent more of the flux, and the winding will have less surface for the flux to touch. Furthermore, the proposed method achieved a 100% improvement in the quality factor (Q), compared to a 20% improvement for inductance and a 50% increase in Q for the technique of removing turns. Without changing the footprint of the winding, the inductance cannot be tuned by removing turns. An evaluation of the proposed winding was conducted by comparing it with a traditional spiral winding and one in which turns were removed in a 5 W, 110–200 kHz wireless power transfer system. The efficiency of the traditional planar spiral winding was 70% at the rated load, while the winding with removed turns had an efficiency of 80%. Meanwhile, the hollow planar spiral winding with TWR had an efficiency of 90%.

3.4. Shifting

The capacitive coupling between planar layers changes with the physical structure. Shifting involves changing the structure to reduce parasitic capacitances. In reference [17], the authors extensively investigated the possibility of relative shifts between the planar layer positions. The shared surface area of these planar tracks, as shown in Figure 17, can be reduced if these tracks are shifted relative to one another. As a result, they have a reduced capacitive coupling. As long as shifting the layers does not significantly affect the volume of the planar element, layer shifting is desirable. Shifting in the structure refers to the position of the middle layer relative to the upper- and lower-fixed structures.

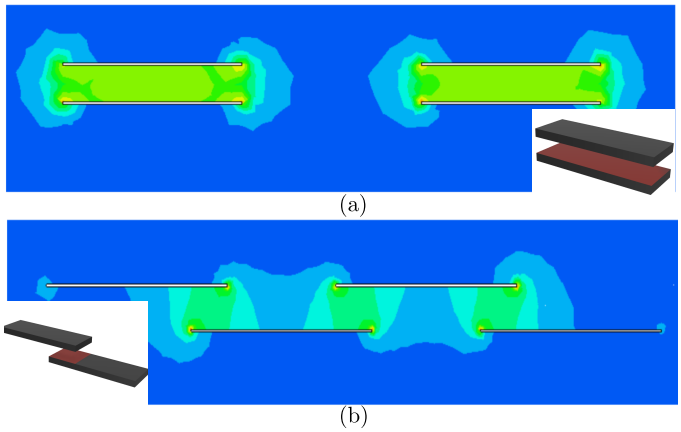


Figure 17. Effective common surface area between two tracks and comparison of FEM results for (**a**) non-shifted, and (**b**) two-layer-shifted structures. The shifting of layers reduces the trapped energy between them [17].

The first aspect to investigate when considering shifting is the capacitance coupling between tracks in the same layer, which is generally small due to a smaller area facing each other. Not only the distance between two tracks, but also the area influences their capacitances, and the shielding effect of the middle layer needs to be taken into account. With shifting, the capacitance in the first aspect may increase or decrease, but this effect is small. The second aspect is the capacitance between tracks of two adjacent layers, which have the largest values. With an increase in shifting, a significant reduction in capacitive coupling can be achieved between these layers. As the shifting rate increases, the level of coupling between tracks of non-adjacent layers, considered the third aspect, may increase since the extent of their facing is likely to increase.

The results from the 2D simulation, 3D simulation, and calculation are presented in Figure 18, indicating that shifting can reduce the capacitive coupling between tracks by up to 50%. If the layer is shifted by more than 50%, the occurrence of repeated cases will increase as well.

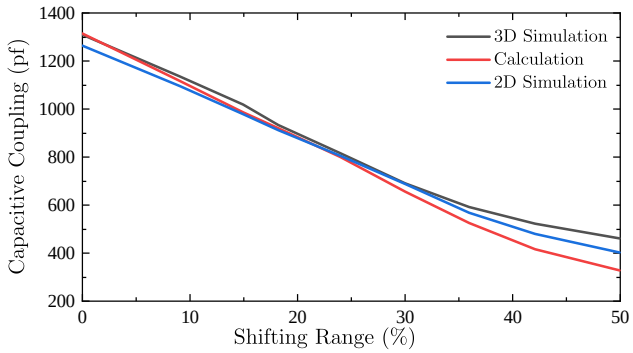


Figure 18. Capacitive coupling simulations and calculation results for different shifting ranges between layers. Since capacitive coupling also depends on the distance between the tracks, shifting can only be effective within a limited range in each design, as there may be repeated cases [17].

3.5. Winding Arrangement within the Layers

The winding structure should be designed in a way to minimize capacitive coupling between adjacent layers while maximizing the shielding effect of each layer.

A magnetic core connected to more than one winding affects the value of the equivalent capacitance directly. Table 3 illustrates some possible series connections for a four-layer inductor and addresses the various connections within the layers described in Figure 19.

Table 3. Comparison of equivalent capacitances for different winding arrangements within the layers. Figure 19 illustrates the various configurations mentioned here.

Winding Arrangement Sequence	Equivalent Capacitance [Percent of Case (1, 2, 3, 4)]
(1,2,3,4)	100
(1,3,4,2)	142
(1,3,2,4)	135
(2,3,1,4)	138
(1,2,4,3)	110
Split Winding Method	77

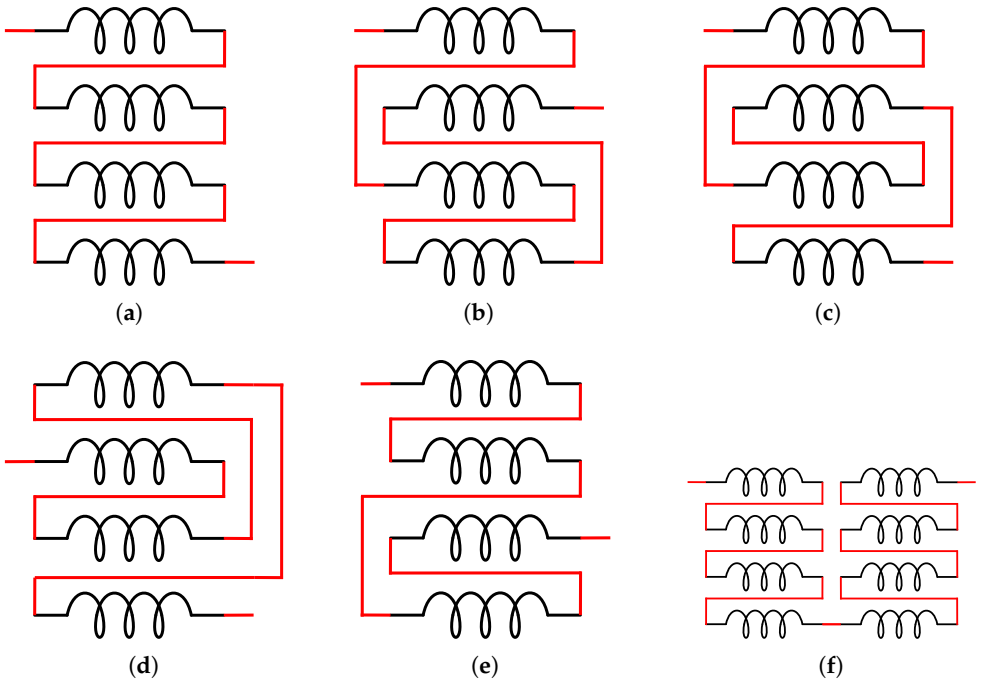


Figure 19. Various series connections of PCB layers as windings to reduce capacitive coupling. This allows for the inductors to be wound in a way that allows them to be split into multiple layers, which reduces the amount of capacitive coupling between the layers. This leads to a more efficient inductor and better performance. (**a**) (1,2,3,4), (**b**) (1,3,4,2), (**c**) (1,3,2,4), (**d**) (2,3,1,4), (**e**) (1,2,4,3), and (**f**) split winding connections [17].

According to Table 3, series connections between adjacent layers have a lower equivalent capacitance. This can be explained by the fact that as a result of each connection, some stray capacitors are short-circuited. The stray capacitance between adjacent windings is the most significant. Due to this, a larger capacitor is shorted when windings are connected closer together, thereby decreasing the equivalent capacitor more than other connections.

Besides the number of layers in parallel, another parameter that influences the equivalent capacitance is how many layers are connected in series. With more layers, there are more parasitic capacitances that are connected and, therefore, the parasitic capacitance is reduced. The concept of a split circuit was presented in [17], where each layer contains two windings. Table 3 indicates that the parasitic capacitance decreases for the split winding structures. However, as the number of turns increases, the difference between the stray capacitances of simple series connections and the split winding method decreases.

3.6. Litzing

Due to the proximity and skin effects, high-frequency currents in solid conductors tend to concentrate on the edges. In order to combat skin and proximity effects, a round Litz wire is commonly used as a solution. A Litz structure is a conductor constructed to a particular pattern. Different examples of planar Litz structures are shown in Figure 20. Thus, the width of the conductor is divided into many lengthwise strands and these strands are then woven together in the same way a Litz wire is constructed. If these isolated strands of wire are woven together into one thicker conductor, the high-frequency resistance of the conductor can be reduced.

A planar Litz wire was previously proposed as an alternative to the round Litz wire in [60]. From the outset, it would seem that a Litzing would be able to reduce the AC resistance in planar magnetics as well [61].

In [62], some guidelines and definitions are given in order to define the design of a Litz conductor. There are four main components of a Litz structure in a planar configuration: strands, conductors, strand angles, and Litz lines (Figure 20). Strands are narrow conductors used to construct Litz structures (Figure 20a). The strand angle is measured relative to the current direction and the Litz conductor direction (Figure 20a). Planar Litz lines are parallel lines equidistant along the width of the planar Litz conductor (Figure 20c). In planar Litz structures, many isolated strands of wire are woven together in a manner that produces one large current-carrying conductor, also called a planar Litz conductor (Figure 20d). The spacing between the lines and the spacing between the strands will determine the maximum width of the strands.

Based on [62], the following statements describe the design process of the planar Litz conductor:

1. Compared to a solid planar conductor, an improvement (even in only small frequency intervals) is positive in terms of leakage and loss reduction.
2. A minimum of two layers will be needed.
3. A Litz conductor with more strands will be more efficient.
4. To achieve equal resistances and equal current divisions, all Litz strands must have equal lengths and widths.
5. In a winding window, the Litz filament may be wound in a zigzag pattern so that it is subjected to the magnetic field all over.
6. Connecting the top and bottom layers requires the use of the appropriate technique.

Depending on the construction of the planar Litz wire structure, the design may not be as physically flexible as that of a traditional model. The first disadvantage of using at least two insulating layers is that they lower the fill factor. However, this becomes less important with relatively thick conductor substrates. Additionally, the copper fill factor is reduced when the conduction path is divided into individual strands. Finally, the angle of the strands introduces increased resistance by lengthening the current path. However, round Litz wire also exhibits the latter two drawbacks. Therefore, planar Litz wire may perform poorly at low frequencies. The proximity effect, on the other hand, can eventually mask all the benefits of the Litz winding compared to a solid conductor winding if the frequency is high enough [62]. Therefore, the benefits are only apparent if the design is optimized for the appropriate frequency.

For instance, in [62], at the frequency of 100 kHz, a 0.51 mm (20 mil) track size was selected for the copper strand width, which is equivalent to twice the skin depth. The DC resistance is directly affected by the filling factor, which decreases as the spacing increases. Therefore, optimal selection will depend on the application. As an example, it is better to have a larger spacing when the frequency loss is significant. Manufacturing technologies also limit the strand width and spacing choices [70].

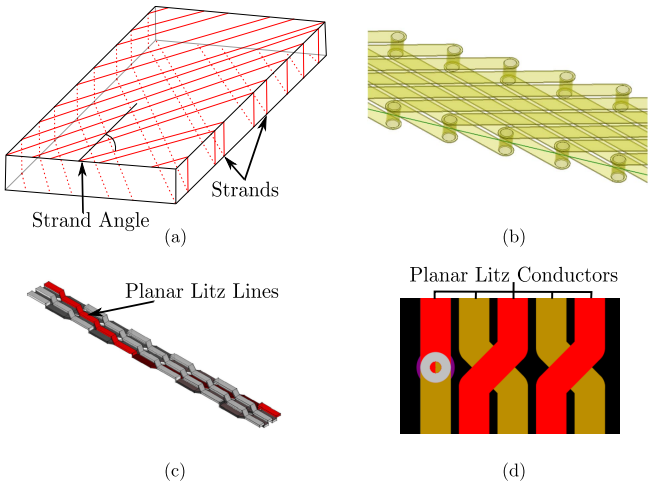


Figure 20. PCB-based Litzing involves winding conductors in a specific pattern on a printed circuit board. This provides a higher level of electromagnetic shielding and reduces the AC resistance of the conductor. This effect is more pronounced at higher frequencies, resulting in lower AC resistance. The following structures have been proposed for Litzing. (**a**) [62], (**b**) [63], (**c**) [63], (**d**) layer changes for Litzing in [63]. Reproduced with permission from [63], IEEE, 2010.

It was demonstrated that the Litz winding, either with or without a core, outperforms the solid conductor winding over a wide frequency range. In this particular Litz design, the AC resistance can be lower between 20 and 700 kHz when this specific winding is used. Utilizing Litz windings instead of solid conductors at 200 kHz can reduce AC resistance by as much as 30%. In the case of a gapped core, the AC resistance of the winding increases rapidly with frequency due to the fringing effect around the air gap. However, the gap length hardly impacts the Litz winding performance.

A novel Litz wire planar transformer and two designs of Litz wire air-core inductors were presented in [63], which save a lot of space and exhibit lower resistance compared to conventional wiring methods. To achieve the Litz structure on a PCB base, at least two layers of PCB must be used [49]. Each of the two layers can have one Litz layer. As illustrated in Figure 20b,c, there are two ways of arranging track transposition. It appears that the first arrangement involves substantial extra moving tracks but is inflexible when the trace has many corners or is circular, which is quite common when designing air-core planar inductors. In contrast, the latter can be fitted by reducing the number of transitions in the circular planar inductor trace. Every track can change positions by passing through vias or by shifting aside using the structure shown in Figure 20d. Although the frequency is critical, the number of changes required should be limited because too many changes can increase the number of vias and hence resistance.

The Litz structure may be compromised by insufficient changes leaving proximity effects between tracks on the same strand. Based on [64], it has been determined that all of the tracks must occupy each possible location at least three to four times around the coil. However, in some cases, fewer changes resulted in similar characteristics.

The electrical simulation and testing results confirm that the Litz wire has much better performance regarding resistance, although it has higher DC resistance because of various changes, including vias. The experiments show that electromagnetic radiation has been significantly reduced by adding a 1mm thick aluminum shield [63]. These changes are also reflected in the experimental settings. During testing of the core, the induced voltage dropped sharply from 2.39 V to 0.09 V. While a shielded air-core inductor has lower inductance due to the distance between its circuit board and its shield, the resistance is virtually the same as that of an air-core inductor without a shield. Hence, with proper gap adjustment, inductance can be set properly while avoiding radiation.

The shield material saturation, which significantly reduces its effectiveness, is a greater concern, which is not discussed in this paper. Due to the small skin depth of

high-permeability materials, the resultant flux is concentrated in a smaller area, thereby magnifying the effects of saturation. It is, therefore, possible to obtain saturation flux density with relatively low amounts of the applied field. This can easily be avoided by ensuring the shield is thick enough to prevent saturation because the flux would extend around the saturated areas and still be effective [71].

By examining various conductor arrangements, [49] offers an applicable guideline for conductors in a planar inductor. Four structures were examined in order to obtain a thorough examination (solid, multi-track, in-layer twisted, and Litzing). Several case studies were conducted using both ferrite-core and air-core inductors by varying different parameters. Three factors—AC resistance, RAC/RDC, and inductance—were taken into consideration when evaluating each structure. When choosing the best structure for the conductors, it has been said that taking into account all three qualities in accordance with the intended operating frequency is crucial. Studies were conducted using measurement data for experimental prototypes in the 10 Hz–1 MHz frequency band. In order to attain the needed qualities, a set of guidelines for designing planar inductors has been offered.

4. Conclusions

An overview of planar magnetic technologies was presented here, emphasizing their parasitic element modeling. The significant advantages of planar magnetics were summarized. Planar magnetics provide more efficient use of space, higher power density, and improved thermal management compared to conventional magnetics. They also have the potential to reduce the size and weight of power electronics systems. These advantages make planar magnetics an attractive option for many power electronics applications.

This paper discusses the inherent properties of planar magnetics by examining winding conduction loss, leakage inductance, and winding capacitance. Several methods have been studied to overcome the shortcomings of planar magnetics. These methods involve either modifying the geometry of the windings or PCB arrangement to reduce parasitic elements and improve the efficiency of the device. Other techniques, such as shielding, also help to reduce losses. Interleaving, CM noise-cancellation methods, track-width reduction, hollow effect methods, shifting, and Litzing were discussed throughout this article. Furthermore, these methods were evaluated, showing that they are effective ways to improve the performance of planar magnetics. The following is a summary of the methods discussed.

Studies show that a planar transformer does not inherently have low leakage inductance, but it does have a higher leakage inductance compared to other transformer types. However, a planar transformer has the advantage that the windings of its primary and secondary can be relatively easily interleaved. Interleaving the windings can reduce AC resistance and leakage inductance to a considerable extent. The primary and secondary windings in a planar transformer are typically flat and printed on a single board, which makes the interleaving process easier. Increasing the magnetic coupling between the windings reduces AC resistance and leakage inductance, making planar transformers more efficient and reliable. These sandwiched planar structures and their extensions have been widely used in embedded electronics, power supply on a chip, and microscale or nanoscale integrated systems. Due to the non-uniform flux distribution caused by this design, as well as the large amount of external flux passing through the conductors, the standard analytical approach cannot be applied.

Planar winding transformers also have a high winding capacitance that cannot be ignored. There is always a balance to be struck between the winding capacitance and the leakage inductance. These parasitic elements arise from voltage potentials between turns, layers of the winding, and between the winding and core. Consequently, it is essential to account for these parasitic elements in order to achieve an optimal design for planar winding transformers. The use of planar magnetic components entails many trade-offs for designers. An approach to cancel common-mode noise nearly to zero was proposed without affecting leakage inductance. This is accomplished by using paired-layer interleaving, a

technique that reduces voltage potentials between turns, layers, and core by interleaving adjacent turns of the winding layers.

Track-width reduction (TWR) is a process used to reduce the size of a printed circuit board (PCB) trace, which in turn reduces its inductance and improves the performance of the system. Using TWR has confirmed that leakage inductance drops as the track width decreases from unity to a minimum, at which point, the resistance increases as the track width decreases further. There are several approaches to improving the spiral winding design in a planar system, for example, by reducing the interlayer capacitance by using an inverted TWR spiral winding structure. Consequently, the copper overlap is greatly reduced and the voltage drops between the largest overlapped areas are normally much smaller. This suggests that the inverted TWR structure is able to achieve better performance than traditional spiral winding structures, leading to improved system efficiency and reliability. There can be a 50% decrease in capacitance and a 20% reduction in AC resistance.

The hollow effect planar magnetics technique is used to design spiral windings that reduce resistive losses in the system. It involves removing the inner turns of the winding to reduce the inductance, thereby decreasing resistance and increasing system efficiency. This technique is useful because it reduces eddy current losses in the system, which occur when the current in the winding induces a magnetic flux in the core, causing a current to flow in the same direction. This current generates a resistive force that reduces system efficiency. Since most eddy current losses pass through the inner turns, eliminating them can significantly reduce eddy current losses.

Depending on the physical structure, capacitive coupling can vary between planar layers. Shifting is the process of reducing parasitic capacitances by changing the structure. By increasing the shifting, it is possible to reduce the capacitive coupling between these layers by a significant amount. This is due to the fact that capacitive coupling is proportional to the overlap between two conductive layers, so increasing the distance between them decreases the coupling. In addition, changing the structure of the layers can affect capacitive coupling by changing the electric field distribution between them.

In solid conductors, a high-frequency current tends to concentrate at the edges due to the proximity effects and skin exposure. This is due to the fact that the skin depth of a solid conductor is dependent on the frequency of the current. At higher frequencies, the skin depth decreases, meaning that more of the current is concentrated at the edges of the conductor. The use of a round Litz wire is a common solution to combat skin and proximity effects in conventional magnetics. As an alternative to round Litz wires, planar Litz wires were previously proposed. Litzing PCB traces are also suitable for reducing the AC resistance in planar magnetics as well.

A great deal of the existing magnetic design literature focuses on only one aspect of design, often leading to excellent solutions for that aspect but ignoring others. Despite the trade-offs, an excellent design must consider all aspects and make allowances for them. Combining these methods and utilizing their benefits can be effective ways to develop designs for the future. As such, it is important to consider a holistic approach to design, one that brings multiple aspects together in an integrated and comprehensive manner.

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