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Low Power Analog Processing for Ultra-High-Speed Receivers with RF Correlation

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ABSTRACT Ultra-high-speed data communication receivers (Rxs) conventionally require analog digital converters (ADC)s with high sampling rates which have design challenges in terms of adequate resolution and power. This leads to ultra-high-speed Rxs utilising expensive and bulky high-speed oscilloscopes which are extremely inefficient for demodulation, in terms of power and size. Designing energy-efficient mixed-signal and baseband units for ultra-high-speed Rxs requires a paradigm approach detailed in this paper that circumvents the use of power-hungry ADCs by employing low-power analog processing. The low-power analog Rx employs direct-demodulation with RF correlation using low-power comparators. The Rx is able to support multiple modulations with highest modulation of 16-QAM reported so far for direct-demodulation with RF correlation. Simulations using Matlab, Simulink R2020a® indicate sufficient symbol-error rate (SER) performance at a symbol rate of 8 GS/s for the 71 GHz Urban Micro Cell and 140 GHz indoor channels. Power analysis undertaken with current analog, hybrid and digital beamforming approaches requiring ADCs indicates considerable power savings. This novel approach can be adopted for ultra-high-speed Rxs envisaged for beyond fifth generation (B5G)/sixth generation (6G)/ terahertz (THz) communication without the power-hungry ADCs, leading to low-power integrated design solutions.

INDEX TERMS Analog-processing, beyond fifth-generation (B5G), RF-correlation, THz, ultra-high-speed

I. INTRODUCTION

Tera hertz (THz) electromagnetic spectrum applications such as imaging have been extensively used in radio astronomy, with the first astronomical THz images dating back to the 1960s. Since 1990 there has been much progress in THz time-domain spectroscopy for tissue characterisation and cancer detection due to advances in femtosecond optoelectronics. New antenna and CMOS integrated-chip technologies are fast emerging as an alternative for realizing affordable THz systems. This together with the availability of wider bandwidths in the THz spectrum motivates more innovative applications e.g. novel cognition, sensing, imaging, communications, and positioning capabilities that may be employed by automated machinery, autonomous cars, and new human interfaces [1].

Policy and research communities have yet to agree on the range of frequencies that would form the THz communication band. However, the Federal Communications Commission (FCC) in November 2019 formally opened up the spectrum between 95 GHz-3 THz [2] for experimental purposes termed as THz communication, beyond fifth-generation (B5G) and sixth-generation (6G) communication. This spectrum has many challenges such as narrow or pencil beam antennae demanding accurate line-of-sight (LOS) communication with frequent beam alignment for the mobile users. Mitigating such challenges will require research on topics such as channel modelling, antenna design, fast antenna beam alignment, radio resource management, and protocol design.

The spectrum has ultra-high-speed data in Gb/s requiring low-power and compact integrated-chips that are challenging to design. Due to the degradation of active device performance

at frequencies close to its maximum operating frequency, the operating frequency cannot be arbitrarily high. Current state-of-the-art CMOS technologies enable circuits operating up to 1.3 THz, to detect both the amplitude and phase of signals up to 1.2 THz, and signal amplitudes up to 10 THz. [3]. Other CMOS implementations include a 240-GHz QPSK transceiver with a data rate of 16- Gb/s and a 300-GHz radio-frequency (RF) transmitter (Tx) that can support 105-Gb/s with 32-QAM [4],[5].

To cater for the high path loss that occurs in signal transmission the ultra-high-speed receiver (Rx) antenna front-end (AFE) will require beamforming to increase antenna directivity. As frequency increases the beamforming directional antennas incur a lower path loss for the same aperture area [6]. Beamforming can be employed in the analog and/or digital domains. Analog beamforming (ABF) is performed at either RF or at an intermediate frequency (IF) through a phase shifter (PS) and a low noise amplifier (LNA) per antenna element as shown in Fig.1, where N_{RX} is the number of antenna elements and N_S is the number of baseband chains. The antenna elements can be employed as uniform linear arrays or uniform rectangular arrays (URA). This reduces power consumption as only one down-conversion chain is required with a variable gain amplifier (VGA) and an analog-to-digital converter (ADC) per digital stream. The VGA ensures that the signal power is adequate to drive the ADC. Certain applications require a high beamforming gain which is done by increasing N_{RX} to 64, 128 or 256. For these hybrid beamforming (HBF) is preferred in order to reduce the number of PS, down-conversion chains and ADCs as N_{RX} is high. HBF with two RF chains as shown in Fig. 1 where each RF chain has its down-conversion chain, VGA and ADC. Partial beamforming is done by PS in the RF domain and by digitally in baseband. For digital beamforming (DBF) shown in Fig. 1, beamforming is performed digitally in baseband. This overcomes the limitation of being able to transmit/receive at few or only fixed directions in ABF and HBF. Since each antenna element requires its own down-conversion stage along with a VGA and ADC, DBF becomes very power-hungry for large numbers of antenna elements. Even for a lower number power requirements remain high in the case of high-speed data due to power-hungry high-speed ADCs and VGAs, requiring higher sampling rates and larger gain ranges respectively to compensate for the reduced beamforming gain

ABF utilizing one RF chain has significant advantage in energy efficiency. PSs can be employed with low resolution which are easier to realize and are more energy-efficient. To circumvent the restriction of limited beamforming directions, the optimal continuous phase ABF can be obtained, and quantize the phase of PS to a finite set [7]–[9], employ codebooks [10]-[14], or machine learning [15]. Recent novel approaches indicate the similar performance of ABF PSs with low and high resolutions in mmWave downlink multicast systems [16]. Similar approaches in ABF and HBF have been proposed for THz communication [17]-[20]. The choice of

beamforming and the associated transceiver depends on the application, but in most cases, HBF and DBF architectures require multiple energy-intensive RF chains and have relatively high-power consumption.
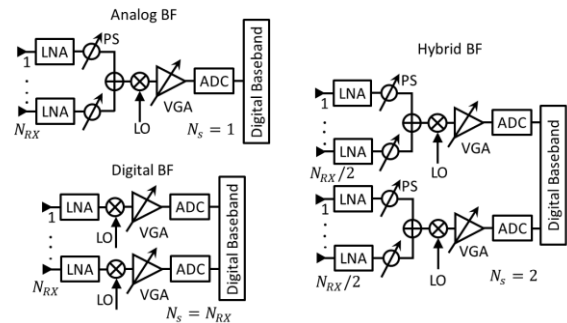

Fig. 1. Analog, hybrid and digital beamforming.

Post AFE Rxs are either employed as direct-conversion i.e. direct-demodulation [21], [22] or IF conversion [23], [24] architectures for demodulating data. To demodulate the raw bit information, the Rxs with ultra-high-speed data will require high-resolution ADCs with sampling rates at least 2-4 times the symbol rate T_S of the modulated baseband or IF signals to avoid aliasing [25]. However, signal-to-noise-distortion ratio (SNDR) and spurious-free-dynamic range (SFDR) both degrade with an increase in the ADC sampling rate leading to poor resolution. Current state-of-the-art high-speed Rxs therefore employ expensive and bulky high-speed oscilloscopes to demodulate data [26], [27]. This leads to ultra-high-speed Rxs being extremely energy inefficient for demodulation. Channel bonding is an alternative solution but requires several parallel data converters with a high level of calibration [21]. Accordingly designing energy-efficient mixed-signal and baseband units for ultra-high-speed Rxs is challenging and requires a paradigm approach. One such approach is to design high-speed Rxs with direct-demodulation requiring no ADCs. Such architectures are reported but support only single and low-order OOK, BPSK, QPSK modulations and have large latency, or have architectures that are not suitable for ultra-high-speed data Rxs.

We detail further the design challenges in ultra-high-speed ADCs, direct-demodulation without ADCs and motivations for adopting the approach in this paper.

A. Ultra-High-Speed ADC

ADC is one of the most power-hungry blocks for Rxs. The effective number of bits (ENOB) of an ADC is its dynamic range above the noise levels (quantization and thermal) that is available for measuring the signal input amplitude. ENOB can be increased by increasing quantization levels for Nyquist ADCs or its sampling frequency (f_s) to above the Nyquist frequency as in oversampling ADCs. A trade-off however exists between power dissipation P_d, ENOB and f_s determined in a figure-of-merit FOM_{ADC} [28]:

$$FOM_{ADC} = \frac{P_d}{(f_s 2^{ENOB})} \quad (1)$$

Sampling data is fundamental to an ADC and hence the power required for it acts as a lower bound to P_d. The thermal sampling noise $N_{TS} = kT/C_s$, where C_s is the sampling capacitor of the ADC, k Boltzmann's Constant, and T the temperature in Kelvin [29]. Typically, C_s is chosen large enough such that N_{TS} of the same order as the ADC's quantization noise N_Q. Assuming that an n-bit ADC is designed such that N_{TS}, N_Q leads to the following minimum value of C_s [29]:

$$C_s = \frac{12kT2^{2n}}{V_{in}^2} \quad (2)$$

where, V_{in} is the full-scale voltage at the ADC input. For an ideal n-bit ADC [29]:

$$ENOB = n - 0.5 \quad (3)$$

For high-resolution ADCs $n > 10$, P_d is dominated by sampling thermal noise and grows proportionally as 2^{2n}. For low-resolution ADCs $n < 6$, P_d is dominated by component mismatch and capacitor size, proportionate to 2^n [29]. As technology and supply voltages scale to lower values, the permissible noise levels reduce further requiring larger values of C_s for a given resolution [29], and for low- resolution ADCs, the energy efficiency becomes limited by thermal noise.

For high-speed demodulation a minimum resolution is required across the entire bandwidth. Due to parasitic capacitances the ADC power and speed becomes a nonlinear relation leading to a lower FOM_{ADC}. ADCs operating above a certain FOM_{ADC} thus degrade performance of resolution and speed [30]. To increase the sampling speed without degrading the FOM_{ADC}, time interleaving ADCs are used which run at lower sampling speed. However, these require power-hungry front-end drivers and are prone to timing and gain mismatches [31], [32]. Hence they have limited ENOB and require high power e.g. 950mW [33].

B. Direct-demodulation without ADC

High-speed Rxs with direct-modulation and requiring no ADCs are reported in [21], [22], [34]-[36]. However, these are either architecture specific such as for spread spectrum systems, or support only single low-order modulations such as OOK, BPSK and QPSK. Ultra-high-speed Rxs will require higher modulation formats for increased data rates and should be adaptive to be able to support multiple modulations depending on channel conditions. Direct-modulation for 8-PSK and higher-order modulations become challenging as the boundary decisions for symbols reduce hence becoming more susceptible to noise. An 8-PSK direct-demodulation based on the arctangent technique in parallel with a digital phased-locked loop (PLL) is presented in [37]. This however requires large lookup tables and memory increasing latency which becomes extremely challenging to implement at ultra-high-speeds. A technique that overcomes this limitation is described in [38], which however is limited to 8-PSK. This paper

proposes a novel low-power analog processing (LPAP) Rx with ABF, employing direct-demodulation and RF correlation without the power-hungry high-speed ADCs. Below are the main contributions of the paper not reported so far in the available literature:

- The Rx design is able to support multiple modulations of BPSK, 4-QAM, along with the highest modulation of 16-QAM reported so far for direct-demodulation with RF correlation and with a single architecture.
- Simulations of the Rx employed with ABF indicate sufficient symbol of error (SER) performance with a symbol rate of 8 GS/s for 71 GHz Urban Micro (UMi) Cell and 140 GHz indoor (InH) channels.
- Power and linearity analysis are undertaken with the current ABF, BHF and DBF configurations requiring ADCs, indicating considerable power savings and SFDR.

Section II details the LPAP Rx architecture, channel model, RF signal power at AFE, phase noise model, comparator and digital decoder design. Simulation results in section III provide for the BER curves, equalizer performance, blocking and interference analysis. The circuit component values, linearity and power comparison analysis for various Rx architectures, are detailed in section IV with conclusions in section V.

II. LOW POWER ANALOG PROCESSING

A. Receiver Architecture

The LPAP Rx consists of 32 antenna elements each followed by LNA and PS as shown in Fig. 2. The input signal is a BPSK/QPSK/16-QAM RF signal with a symbol rate of 8 GS/s. The signal is converted to in phase (V_{in}) and quadrature phase (V_q) components by two LOs at RF, one in-phase with the RF signal, and other with a 90° phase difference. For direct-demodulation Rxs there are widely employed techniques available for synchronization such as pilots/training sequences; and for mitigating the I/Q imbalances which can be employed. The low pass filters (LPF) are employed to filter out any interference signals in the proximity of the RF signal. Since V_{in}, V_q are low pass baseband signals this overcomes any sharp roll-off requirements for the LPF, hence lowering the power requirements. The LPF is a single pole RC filter with a 3dB cut-off at 12 GHz. The VGAs provide sufficient amplification for a stable signal reference value in the subsequent stages.
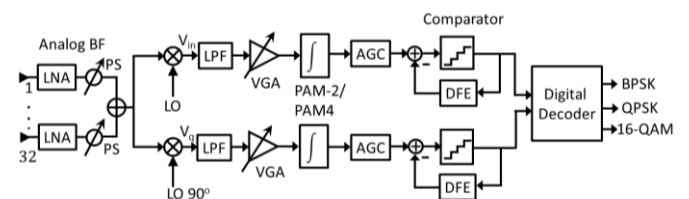

Fig. 2. LPAP Rx architecture.

At the integrator outputs V_{in}, V_q are pulse amplitude modulated (PAM) signals with two-levels (PAM-2) for BPSK/QPSK modulation. For 16-QAM V_{in}, V_q are four-level PAM signals (PAM-4). The automatic gain controls (AGC) ensure a certain voltage level at the comparator. Decision feedback equalizers (DFE) remove any inter-symbol interference (ISI) and channel distortion. The equalized signals are then decoded by the digital decoder that enables demodulation of the BPSK/QPSK/16-QAM signal.

B. Channel Model and RF Signal Power

Based on the 3D statistical channel model in [39], [40], an open-source MATLAB-based statistical simulator NYUSim v3.1, has been developed by New York University (NYU) [41]. The simulator generates 3D angle-of-departure (AOD) and angle-of-arrival (AOA) power spectra and power delay profiles (PDPs) that match measured field results from 0.1-148 GHz RF frequencies. This is based on over 15,000 PDPs that were measured and used to derive directional and omnidirectional path loss models and extract small-scale channel statistics such as the number of time clusters, cluster delays, and cluster powers. In the 3GPP TR 38.901 outdoor channel model for frequencies above 0.5 GHz [42], the number of clusters is unrealistically large which is not supported by the real-world measurements at mmWave bands [39], [40], [43]. In contrast, in the outdoor statistical model implemented in NYUSim v3.1, the number of time clusters ranges from 1 to 6, and the mean number of spatial lobes is about 2 which is upper-bounded by 5. These are obtained from field observations and are much smaller than those in the 3GPP channel model [44], [45]. To realistically quantify the signal power received P_r at AFE, NYUSIM v3.1 is employed in this paper for simulating the 71 GHz and 140 GHz channels, as the simulator is built from field data which gives more realistic results.

Input values for NYUSim v3.1 are given in TABLE I indicated as channel parameters which include atmospheric conditions, spatial consistency and antenna parameters, where HPBW is the half power beamwidth and N_{TX} number of antenna elements in the Tx array. Spatial consistency mode is applicable in outdoor channels, where the Rx moves along a specific path generating correlated and consecutive channel impulse responses for successive sampling points on the path. The path can be selected as linear or hexagonal. Spatially correlated large-scale parameters such as shadow fading, and time-variant small-scale parameters such as angles, power, delay and phase of each multipath component are generated [46], [47]. In addition the effects of human blockage causing temporal shadowing for both indoor and outdoor channels are modelled. For this the default setting option is used in this paper where an average mean attenuation for human blockage is implemented based on a linear fit applicable to the Tx/Rx antenna HPBW [48].

The PDPs generated are weighted by the Tx and Rx antenna directivity given as [39]:

$$G(\theta, \phi) = max\left(G_0 e^{-\alpha\theta^2 - \beta\phi^2}, \frac{G_0}{100}\right) \qquad (4)$$

$$\alpha = \frac{4\log_e 2}{\theta_{3dB}^2}, \beta = \frac{4\log_e 2}{\phi_{3dB}^2}, G_0 = \frac{41253\eta}{\theta_{3dB}\phi_{3dB}} \qquad (5)$$

where, (θ, ϕ) are the azimuth and elevation angle offsets from the boresight direction in degrees, G_0 is the maximum directive boresight gain in linear units, $(\theta_{3dB}, \phi_{3dB})$ are the azimuth and elevation HPBW in degrees, α, β are parameters that depend on the HPBW values, and $\eta = 0.7$ is the typical average antenna efficiency. Conventionally, the HPBW of an antenna array is a function of the number of antenna elements and the antenna spacing, but here in the simulator three parameters i.e., the HPBW, number of antenna elements, and antenna spacing can be independently specified, since there may be a wide range of beamforming approaches as in Fig. 1, in all of which different individual antenna element types (e.g., patch antennas, vertical antennas, horns) can be used.

TABLE I
NYUSIMv3 PARAMETER SETTINGS

Channel Parameters

Frequency (0.1-148 GHz) Channel	71 GHz, 140 GHz. UMi, InH	As allocated by FCC. 71 GHz Urban micro outdoor, 148 GHz Indoor.
Tx Rx Separation	50 m, 25 m	Normal UMi outdoor, InH indoor values.
Tx Power	35 dBm, 30 dBm	Normal UMi, InH base station power.
Base station height	15 m, 3 m	Normal UMi, InH base station heights.
Rx height	1.5 m	Normal height.
Number of Rx locations	200	Mean of 200 simulations.
Barometric Pressure	1013.25 mbar	Standard atmospheric condition.
Humidity	50 %	Standard atmospheric condition.
Rain Rate	0 mm/hr	Standard atmospheric condition.
Polarisation	Co-polarization	Co-polarization of Tx and Rx antenna URAs are considered.

Spatial Consistency Parameters

Correlation Distance	10 m	Standard simulator setting.
Rx Track Type	Linear	To ensure realistic path profile.
Rx Moving Direction	45°	Standard simulator setting.
Rx Velocity	10 m/s	Velocity assumed in UMi channel.
Rx Moving Distance	10 m	Distance in Tx-Rx separation.

Antenna Parameters

Tx Array Type	URA	URA is considered in this paper.
Rx Array Type	URA	URA is considered in this paper.
No. of Tx elements	N_{TX}	256
No. of Tx elements	N_{RX}	32
Tx/Rx Antenna Azimuth/Elevation HPBW	$7° - 360°$	$7°, 7°$ lower limit for NYU.

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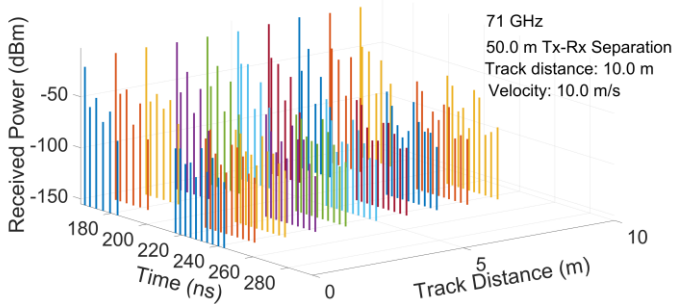The PDP profile generated for 71 GHz channel is shown in Fig. 3.

Fig. 3. PDP 71 GHz channel.

The variation in PDP due to shadow fading for the mobile Rx is shown in Fig. 4 for a Rx track at 45°. The PDP profile for the 140 GHz channel is shown in Fig. 5.
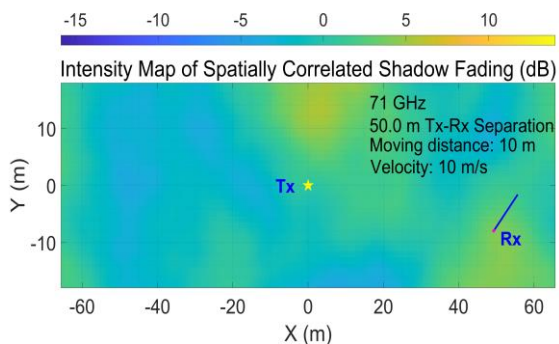

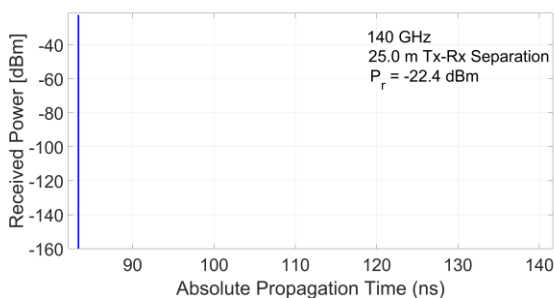Fig. 4. 71 GHz channel variation in PDP due to Rx mobility.

Fig. 5. PDP 140 GHz channel.

The cumulative distribution function $F(.)$ of P_r for 200 simulations is shown in Fig. 6. More than 200 simulations show no change in statistical values. The mean power values obtained are -14.44 dBm and -15.55 dBm for the 71 GHz and 140 GHz channels respectively. The mean value of PDP variation obtained is $\pm$ 6 dB accounting for user mobility in the 71 GHz channel. Accordingly, P_r at the input to AFE assumed are -21 dBm and -16 dBm for the 71 GHz and 140 GHz respectively.
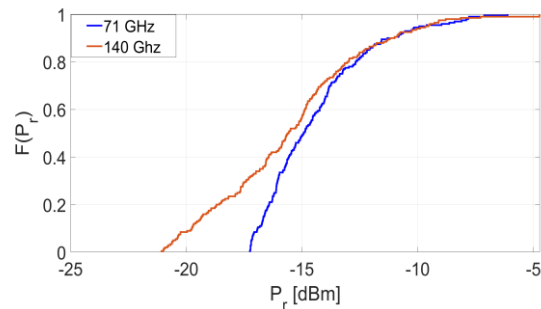

Fig. 6. Cumulative density function of power received.

The thermal noise power for a bandwidth (B) of 8 GHz is calculated as -75.09 dBm using

$$N_T = 10log\left[\frac{kTB}{10^{-3}}\right] \quad (6)$$

where, $k = 1.380648 \times 10^{-23}$ J/K is the Boltzmann's constant and $T = 280$ the noise temperature in Kelvin.

C. Local Oscillator Phase Noise

A common circuit solution for LO is frequency generation with a voltage controlled oscillator (VCO). Several parameters that can be employed in VCO design and the performance is well captured by a Figure-of-Merit (FOM_{VCO}) which accounts for power, different semiconductor technologies and circuitry topologies where:

$$FOM_{VCO} = L\ (f) - 20\log\left(\frac{f_o}{f}\right) + 10\log\ (P_{VCO}\ /1mW)\ (7)$$

where, $L\ (f)$ is the phase noise in dBc/Hz at a frequency offset f, f_o is the oscillation frequency, and P_{VCO} the power consumption in mW. On a linear scale both $L\ (f)$ and P_{VCO} are $\propto f_o^2$. In order to maintain the phase noise level at a certain offset when increasing f_o by a factor α requires the power to be increased by α^2, assuming a fixed FOM_{VCO}. Conversely, for a fixed power consumption and FOM_{VCO} the phase noise will increase by α^2, or 6dB per every doubling of f_o. A common way to suppress LO phase noise is to apply a PLL, where the VCO which is locked to a highly stable reference, normally a low frequency crystal oscillator, by use of a phase frequency detector, filter and counter. The PLL compares the phase of a reference signal to the phase of an adjustable feedback signal to ensure a steady higher frequency output.

Different strategies can be employed for implementation of signal generation and distribution such as centralized PLL generation (one PLL for all baseband chains), distributed PLL generation (one PLL per baseband chain) and semi-distributed PLL generation (baseband chains within a group sharing a common PLL). The different strategies have not yet been investigated. A comparison could lead to some potential advantages/disadvantages for implementation in mmWave or higher frequencies, forming a basis for future study. The total phase noise of a PLL is composed of contributions from the VCO outside the loop bandwidth and the reference oscillator inside the loop. A significant noise contribution is also added by the phase detector and the divider. This poses significant challenges when employing higher frequencies with phase sensitive modulation such as 16-QAM in ultra-high-speed

Rxs. As the VCO phase noise increases by 6dB per doubling of the frequency, an increase in VCO frequency from 3 GHz to 30 GHz would result in phase noise degradation of 20 dB for a given offset frequency.

Another contributing factor that increases phase noise at higher frequencies is the degradation in quality factor (Q)-value and low signal power. In order to achieve low phase noise, the Q-value and signal power need to be maximized while minimizing the noise figure of the active device, which is challenging to achieve when the signal frequency increases. For monolithic circuits, the Q-value of the on-chip resonator decreases as frequency increases due to an increase of parasitic losses due to substrate effects and resistance of metal tracks. The fundamental VCO frequency is therefore generally limited to ~15 GHz while employing frequency multipliers for higher frequency requirements. In addition, the up-conversion of the $\frac{1}{f}$ noise creates an added slope in the vicinity of the carrier frequency. The $\frac{1}{f}$ noise depends on technology, where planar devices such as FET, PHEMT and CMOS are seen to have a higher noise level than vertical bipolar devices like Si bipolar, SiGe HBT and GaAs HBTs.

Existing phase noise models include Leeson's model [49] and those developed by Hijimira and Lee [50], Rael and Abidi [51], and Razavi [52]. A phase noise model that gives accurate results when compared with actual prototypes is the single-sideband (SSB) pole-zero model developed by the IEEE 802.15.3c task group [53]. The phase noise at offset frequency f in dBc/Hz is given by:

$$L(f) = L(0). \frac{1+\left(\frac{f}{f_z}\right)^2}{1+\left(\frac{f}{f_p}\right)^2} \qquad (8)$$

where f_z and f_p are the pole and zero frequencies respectively. The model was extended and employed by 3GPP for mmWave circuits which is a generalization of the multi-pole/zero model extended to fractional orders in [54] where:

$$L(f) = L(0) \frac{\prod_{n=1}^{N} 1+(\frac{f}{f_{z,n}})^{\alpha_{z,n}}}{\prod_{m=1}^{M} 1+(\frac{f}{f_{p,m}})^{\alpha_{p,m}}} \qquad (9)$$

In [54] the modelled phase noise obtained by (9) is compared with a research prototype PLL designed in a 28nm FD-SOI CMOS process indicating accurate results. This is for distributed PLL generation at 29.55 GHz. The model is used by 3GPP to estimate PLL phase noise at higher frequencies of 45 GHz and 70 GHz [53]. The same method is followed in this paper to estimate the PLL phase noise at 71 GHz and 140 GHz. When the PLL phase noise profile is given at frequency f_o with phase noise $L(f_o)$, the correct phase noise $L(f)$ at any other oscillation frequency f according to Lesson's equation is [49]:

$$L(f) = L(f_o) 20log_{10}\left(\frac{f}{f_o}\right) \qquad (10)$$

Here f_o= 29.55 GHz is the carrier frequency with a known phase noise profile. The FOM_{VCO} degrades at higher frequencies as shown in Fig. 7, which shows FOM_{VCO} versus frequency for several state-of-the-art published VCOs implemented in CMOS [55]-[67]. The FOM_{VCO} envelope

indicated by the dashed line showing the trend of the best VCOs has a 9 dB per decade slope and is used to derive parameters for phase noise models at 71 GHz and 140 GHz. The steps from 29.55 GHz to 71 and 140 GHz correspond to 0.38 and 0.68 decades, for which the corresponding phase noise degradations are listed in TABLE II. The $20log_{10}\left(\frac{f}{f_o}\right)$ degradation is an overall degradation for the phase noise characteristics except for the high frequency noise floor region that is assumed to be constant. The FOM_{VCO} degradation affects only the VCO contribution starting at an offset of a few MHz.
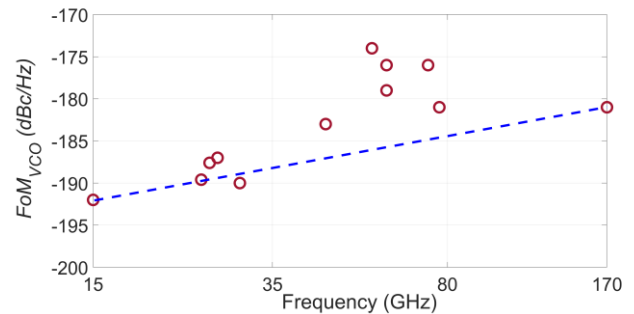

Fig. 7. FOM_{VCO} for state-of the art VCOs implemented in CMOS.

TABLE II
FoM Degradation

f	$20log_{10}\left(\frac{f}{f_o}\right)$ degradation	FOM_{VCO} degradation
29.55 GHz	0 dB	0
71 GHz	7.6 dB	3.4 dB
140 GHz	13.5 dB	6.12 dB

To determine the phase noise characteristics, the phase noise is first increased by the $20log_{10}\left(\frac{f}{f_o}\right)$ degradation according to TABLE II. Then parameters $f_{z,n}$, $\alpha_{z,n}$, $f_{p,m}$, and $\alpha_{p,m}$ are altered to obtain specified FOM_{VCO} degradation at 30MHz offset while maintaining a constant phase noise of -140dBc/Hz at large offset and at the hump around 1.55MHz offset. The resulting phase noise characteristics are shown in Fig. 8, with parameters listed in Table III for 71 GHz and 140 GHz.
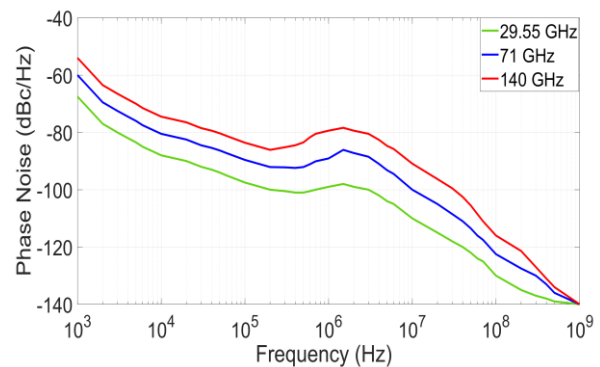

Fig. 8. Phase noise estimation for PLLs at 71 GHz and 140 GHz.

TABLE III
PHASE NOISE MODEL PARAMETERS

71 GHz, $PSD(0)$ 39.6 dB

$n.m$	$f_{z,n}$	$\alpha_{z,n}$	$f_{p,m}$	$\alpha_{p,m}$
1	$3(10^3)$	2.37	1	3.3
2	$395(10^3)$	2.7	$1.55\,(10^6)$	3.3
3	$758\,(10^6)$	2.53	$30\,(10^6)$	1
140 GHz, $PSD(0)$ 45.5 dB				
1	$3(10^3)$	2.37	1	3.3
2	$245(10^3)$	2.7	$1.55\,(10^6)$	3.3
3	$1144\,(10^6)$	2.53	$30\,(10^6)$	1

D. Comparator and Digital Decoder

Three single-bit comparators C_1, C_2 and C_3 are employed for 16-QAM demodulation as shown in Fig.9 where the input is a PAM-4 V_q/V_{in} signal. The effects of process voltage temperature variation (PVT) can be countered by employing automatic gain control (AGC) [68], [31] and adaptive reference voltage generators [69], [70]. A PAM signal offers superior performance in comparison to non-return-to-zero (NRZ) signalling under the effects of inter-symbol interference (ISI) and clock jitter [71], achieving data rates of 100 Gbps [72], [73]. The threshold values for C_1, C_2 and C_3 are set as TH_1, TH_2 and TH_3 respectively. The comparator output voltage levels V_1, V_2 and V_3 are high or low depending on the amplitude level of the input signal. For QPSK the Rx utilises two C_2 comparators, one each for V_q and V_{in} and PAM-2 inputs. For BSPK a single C_2 comparator is utilised for either V_q or V_{in} and a PAM-2 input.
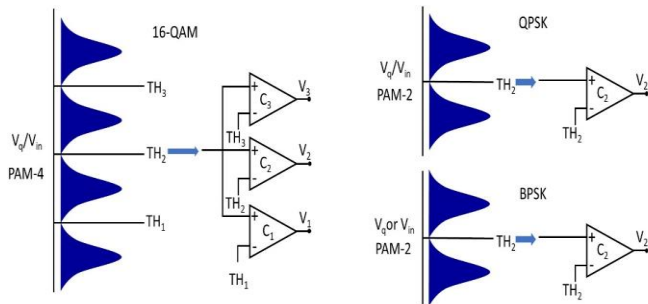

Fig. 9. Comparator with signal inputs.

Comparators can be implemented with one or two stages of preamplification followed by a track and latch stage. Normally a low gain (~10) preamplifier reduces the kickback caused by fast output transitions while reducing the probability of metastability. Higher gain values can increase the time constant thereby reducing the speed. The latch alternates between a reset phase and positive feedback stage that generates full-swing digital signals from the preamplifier output. State-of-art comparators can sample at 14 GS/s [74] and interleaving comparators can be employed to increase the sampling rates.

The digital decoder for 16-QAM is shown in Fig. 10. With V_{in} as input, the decoder employs V_2 as MSB and a second bit B_2 is produced by XORing V_3 and V_1. This results in a two-bit Gray mapping output of V_{in}. With V_q as the input, bit B_3 is obtained by inverting V_2, and the LSB is produced by XORing
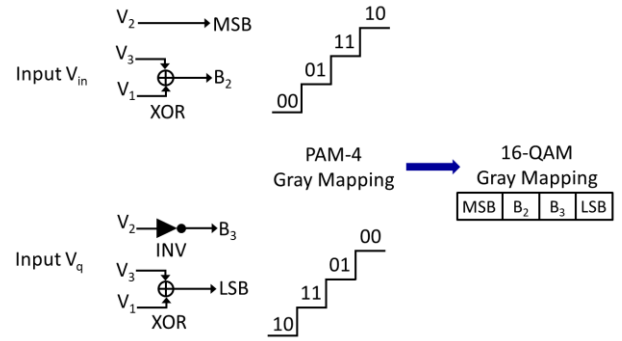

Fig. 10. Digital decoder for 16-QAM.

V_3 and V_1. Bits B_3 and LSB also result in a two-bit Gray mapped output of V_q. The final symbol is obtained by combining V_{in} and V_q bits, resulting in a four-bit 16-QAM symbol according to Gray mapping shown in Fig. 11.
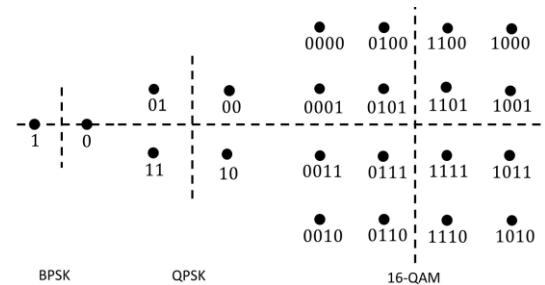

Fig. 11. Gray mapping and symbols.

The QPSK and BPSK decoders are shown in Fig. 12. For demodulating the QPSK symbol decoder inverts V_2 to obtain the MSB, and the LSB from inputs V_q and V_{in} respectively. This results in a QPSK symbol with Gray mapping shown in Fig. 11. For a BPSK symbol the output bit B_1 is obtained by inverting V_2 from either V_q or V_{in} as the input.
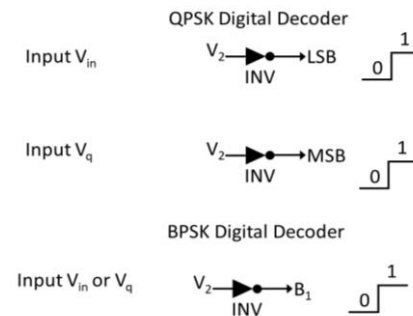

Fig. 12. Digital decoder for QPSK, BPSK.

The truth table values for four 16-QAM symbols are shown in TABLE IV which provides the PAM-4 2-bit quantised outputs for V_{in} and V_q. All 16-QAM symbols in Fig. 11 can be generated using appropriate combinations of V_{in} and V_q output values. The truth tables for QPSK and BPSK decoders are shown in TABLE V

TABLE IV
TRUTH TABLE 16-QAM DECODER

V_{in}					V_q				
V_3	V_2	V_1	MSB	B_2	V_3	V_2	V_1		LSB
1	1	1	1	0	1	1	1	0	0
0	1	1	1	1	0	1	1	0	1
0	0	1	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0

TABLE V
TRUTH TABLE

QPSK				BPSK	
$V_2 [V_q]$	$V_2 [V_q]$	MSB	LSB	$V_2[V_{in}]$	B_1
1	1	0	0	1	0
0	1	0	1	0	1
0	0	1	1		
1	0	1	0		

III. SIMULATION RESULTS

The LPAP Rx in Fig.2 was implemented in Simulink Matlab R2020a®. Simulations were undertaken for the signal inputs generated by the NYUSim v3.1 71 GHz and 140 GHz channels. Thermal noise was generated according to (6) and the LO phase noise as in Fig. 8. The Rx component values such as gain, insertion loss, linearity and noise figure employed are detailed in section IV.

A. BER Curves

The BER curves for the LPAP Rx and the ideal theoretical values with no channel coding for AWGN channels are shown in Fig 12. The LPAP performance is similar for 71 GHz and 140 GHz channels with the 140 GHz performing marginally better. This can be attributed to the signal at AFE being higher at -16 dBm for 140 GHz channel, as compared to -21 dBm for the 71 GHz channel.
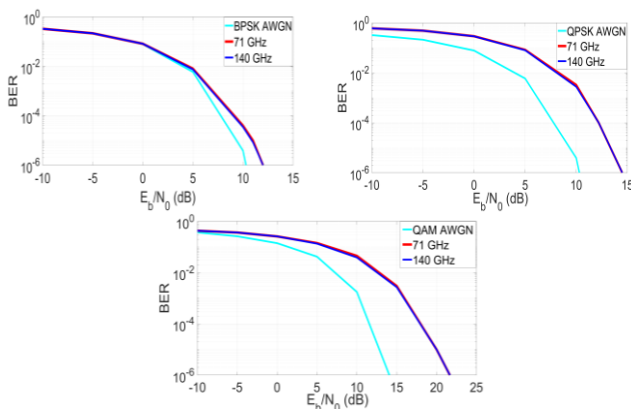
Fig. 12. LPAP Rx BER curves.

B. Decision Feedback Equalizer

A continuous time linear equalizer (CTLE), feed-forward equalizer (FFE), decision feedback equalizer (DFE) or a combination of these are normally employed for channel equalization [75], [76]. Another approach is to employ spatio-temporal equalization with beamforming in mmWave channels [77]. A DFE offers a significant advantage over CTLE and FFE since it cancels post-cursor ISI without noise and crosstalk amplification between the in-phase and quadrature channels. The DFE employed is shown in Fig.13.
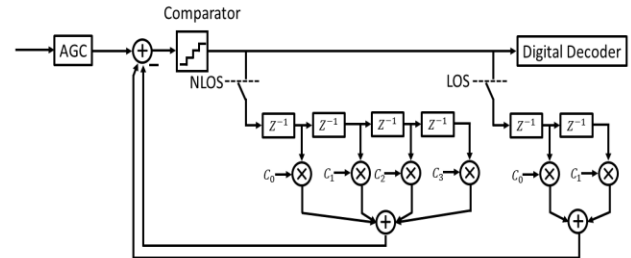
Fig. 13. DFE for LPAP Rx.

The automatic gain control (AGC) ensures a certain voltage level at the DFE input. It applies an adaptive variable gain to the input waveform to achieve the desired RMS output voltage. Averaging the RMS voltage over a specified number of symbols, AGC performs by increasing or decreasing the gain, or keeping the gain constant. The DFE samples data at each clock sample time and the amplitude of the waveform is adjusted by a correction voltage. The zero-forcing algorithm is employed to determine the correction factors necessary to eliminate ISI. Due to the sparse nature of mmWave channels a two-tap DFE is sufficient to equalize the 71 GHz LOS or no-line-of-sight (NLOS), and 140 GHz LOS channels. For the 140 GHz NLOS) channel a 4-tap DFE is required due to increased multipaths that occur indoors with sufficient power levels leading to ISI.

The normalized impulse response waveforms for the DFE are shown in Fig. 14 for the 71 GHz LOS and 140 GHz NLOS channel where more multipaths are visible for the latter.
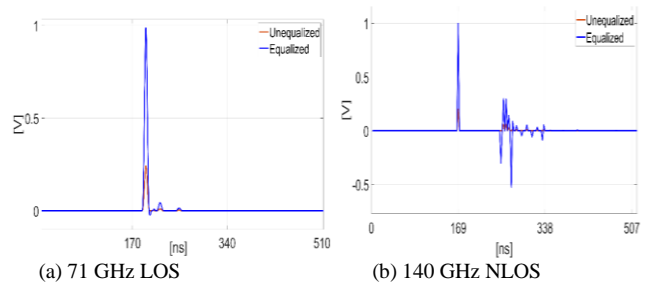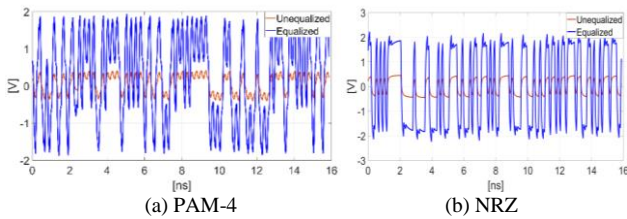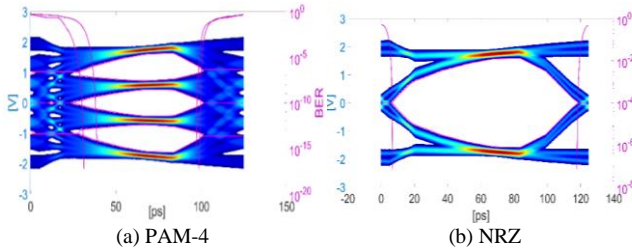
(a) 71 GHz LOS   (b) 140 GHz NLOS

Fig. 14. DFE Impulse response.

The pseudo-random binary sequence waveforms for PAM-4 (16-QAM) and NRZ (QPSK/BPSK) are shown in Fig.15. Eye diagrams and BER for PAM-4 and NRZ are shown in Fig.16.

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(a) PAM-4	(b) NRZ

Fig. 15. PRBS waveform.

(a) PAM-4	(b) NRZ

Fig.16 . DFE Eye diagrams with BER

The signal quality parameters for PAM-4 and NRZ are eye linearity (*EL*), vertical eye closure (*VEC*) and channel operating margin (*COM*) [78], [79]. *EL* is a measure of variance in amplitude separation (distribution) between the different PAM-4 levels. *EL* is always equal to or less than 1.0. The value 1.0 indicates that the separations between all levels are equal. *EL* is given by [78]:

$$EL = \frac{min(AV_{upp}, AV_{mid} \text{ and } AV_{low})}{max(AV_{upp}, AV_{mid} \text{ and } AV_{low})} \quad (11)$$

where AV_{xxx} is the mean of central 5% of eye amplitude values as shown in Fig 17. The *VEC* penalty is [78]:

$$VEC = 20\log_{10}\left(max\left[\frac{AV_{upp}}{V_{upp}}, \frac{AV_{mid}}{V_{mid}}, \frac{AV_{low}}{V_{low}}\right]\right) \quad (12)$$

The *COM* is defined as [79]:

$$COM = 20\log_{10}\left(\frac{A_s}{N}\right) \quad (13)$$

where N is the peak BER noise and A_s is the peak signal. *COM* combines the eye-mask and frequency-domain masks, with user-defined equalization parameters at the Rx. *COM* produces a signal-to-noise ratio (SNR) as a final value, which represents the channel performance and must be > 3 dB. The PAM-4 and NRZ measured parameters along with the DFE coefficient values are shown in TABLE VI.
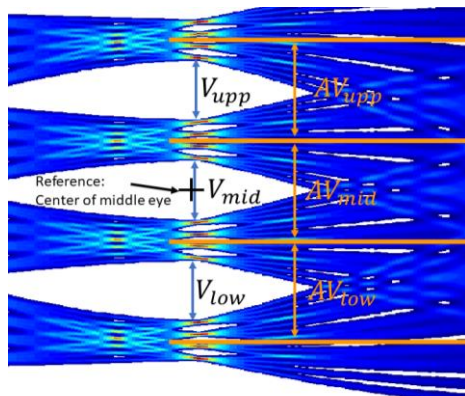

Fig. 17. Eye measurements.

TABLE VI
DFE EYE Parameters

Parameter	Value			
	LOS		NLOS	
	PAM-4	NRZ	PAM-4	NRZ
Eye Height Upper	0.81641 V	3.01 V	0.53835 V	1.6188 V
Eye Height Center	0.81636 V	-	0.53702 V	-
Eye Height Lower	0.81642 V	-	0.5385 V	-
Eye Width Upper	65.51 ps	112.34 ps	81.05 ps	116.21 ps
Eye Width Center	75.68 ps	-	81.54 ps	-
Eye Width Lower	65.51 ps	-	81.05 ps	-
Eye Area Upper	44.78 Vps	242.72 Vps	38.29 Vps	148.63 Vps
Eye Area Center	45.03 Vps	-	38.22 Vps	-
Eye Area Lower	44.80 Vps	-	38.28 Vps	-
COM	10.84 dB	18.47 dB	46.14 dB	54.85 dB
VEC	2.91 dB	1.1024 dB	0.042 dB	0.0157 dB
Eye Linearity	0.9979	-	0.9975	-
DFE Tap Weights	[-0.6041, -0.1951] V		[-0.5595, -0.0280, -0.0001 -0.0021] V	
Interior PAM-4 Threshold	1.162 V		0.54015 V	

C. Blocking and Interference

During beamforming the beam can be directed towards the Rx and prevent interference to nearby Rxs. The effects of interfering power which is offset by 5° in azimuth can be reduced by ~3-8dB depending upon the elevation offset [80]. This is for HPBWs from 13.4°-25.8°. Lower values of interference are likely since the Rx HPBW considered is 7° [81].

Rx protection from noise and interference can be achieved through requirements for performance parameters like ACS (adjacent channel selectivity) and blocking characteristics. Since the standards for ultra-high-speed Rxs are not available the 5G New Radio (NR) parameters are adopted for quantifying the interference as below:

- ACS is a measure of a Rx's ability to receive a wanted signal at its assigned channel frequency in the presence of an adjacent channel signal at a given frequency offset from the center frequency of the assigned channel. The required ACS is 23 dB (Table 7.5-1 [82]).
- Blocking characteristic is a measure of Rx's ability to receive a wanted signal at its assigned channel frequency in the presence of an unwanted interferer on frequencies other than those of the adjacent channels, without this unwanted input signal causing a degradation in Rx performance beyond a specified limit. (Table 7.2.2-1, 7.2.2-2 and 7.2.2-3 [82]). The blocker in the vicinity of a 71 GHz channel would be the 60 GHz IEEE 80211.ad signal.

The measured ACS for LPAP Rx with an adjacent signal at 79 GHz is 26 dB. For blocking, the LPAP Rx is able to demodulate the signal with CW interferer up to -6 dBm without any degradation in signal quality. For both cases it is assumed that the LPAP Rx and the interfering signals are perfectly beam aligned as the worst-case scenario.

Beamforming and network function virtualization (NFV) currently adopted for 5G networks provide an inherent

mechanism that would mitigate interference. High-frequency bands make it possible to increase antenna element density without increasing the physical size of the antenna which allows much narrower beams to be formed For 5G networks NFV is employed to perform the majority of processing needed to run commercial networks, via virtual network functions and by scheduling users. This can reduce interference significantly.

IV. CIRCUIT COMPONENTS AND POWER ANALYSIS

A. Receiver Linearity and Distortion
The state-of-the-art CMOS circuit parameters including non-idealities considered for simulation to obtain the BER curves in Fig. 12 are summarized in TABLE VII. The gain, noise figure and the third intercept point in various stages indicated by $i \in [1,5]$ of the LPAP Rx are given by G_i, NF_i and $IIP_{3,i}$ respectively.

TABLE VII
CIRCUIT PARAMETERS /NON-IDEALITIES

i	Component	Values
1	LNA [83]	G_1 18 dB, NF_1 8 dB, $IP_{3,1}$ -2.1 dBm, 11.7 mW
2	Phase Shifter [84,85]	G_2 -10 dB
3	Mixer[86]	G_3 11.6 dB, NF_3 15.8 dB $IP_{3,3}$ 3 dBm, 6.3 mW
4	Filter [87]	G_4 -1.5 dB
5	VGA [88]	G_5 11 dB, NF_5 9.05 dB, $IP_{3,5}$ 26 dBm, 22.5 mW
-	Thermal Noise	As per equation (6)
-	PLL	Phase Noise as per Fig. 8

According to International Telecommunication Union-Radio (ITU-R) recommendation the SFDR of a Rx accounting for distortion is given by:

$$SFDR = \frac{2}{3}(174 + IIP_3 - NF - 10\log_{10} B) \quad (14)$$

where IIP_3 and NF are the total third intercept point and noise figure of the Rx. The IIP_3 of M stages is given by [89]:

$$IIP_3 = \left[\sum_{i=1}^{M} \frac{\prod_1^{i-1} G_i}{IIP_{3,i}}\right]^{-1} \quad (15)$$

The noise factor for M stages is given by the Friss's formula:

$$f_M = f_1 + \frac{f_2-1}{G_1} + \frac{f_3-1}{G_1G_2} + .. + \frac{f_M-1}{G_1G_2..G_{M-1}} \quad (16)$$

where $NF = 10\log_{10} f_M$.

Using the values in TABLE VII, and from (14)-(16) the SFDR for the LPAP Rx is 46.48 dB. For a fixed bandwidth the design process requires a trade-off between the NF and IIP_3. Loss in front of a Rx stage improves the IIP_3, while increasing gain improves the NF. This is in contradiction to when defining the system specifications in each stage as a common practice and considering each performance parameter separately. Currently, there exists no technique for optimisation. Consider IIP_3 in (15) as a function such that:

$$f(x,y,z) = IIP_3 \quad (17)$$

where $x = IIP_{3,1}$, $y = IIP_{3,3}$, $z = IIP_{3,5}$; and gains G_i as constants $\forall i$. The gradient of $f(x,y,z)$ is given by:

$$\nabla f(x,y,z) = \begin{bmatrix} \frac{y^2z^2}{\theta} \\ \frac{C_2x^2z^2}{\theta} \\ \frac{C_3x^2y^2}{\theta} \end{bmatrix} \quad (18)$$

where:
$\theta = [yz + C_1xyz + C_2xz + C_3xy]^2$, $C_1 = G_1 + G_1G_2G_3$, $C_2 = G_1G_2$ and $C_3 = G_1G_2G_3G_4$. The normalised gradient vector is given by:

$$\nabla f_n(x,y,z) = 1.0\hat{X} + 0.5986\hat{Y} + 0.0003\hat{Z} \quad (19)$$

From (19) we infer that increasing $IIP_{3,1}$ would increase IIP_3 at a faster rate than for any increase in $IIP_{3,3}$ or $IIP_{3,5}$. This is shown in Fig. 18 where increase in IIP_3 is plotted for every 2 dB increase in $IIP_{3,i}$, $i = 1,3,5$. Further increase in SFDR can only be achieved by lowering NF_1. The LNA can accordingly be designed by employing SiGe HBTs. Such high-performance BiCMOS technology platforms with higher integration levels are currently being employed to address ultra-high-speed data rates [90]. Design of a wideband SiGe HBT LNA with $G_1 = 20.2$ dB, $IIP_{3,1} = 8.36$ and $NF_1 = 3.7$dB is given in [91], which improves the SFDR to 50.1 dB. The LNA power consumption is 17 mW.
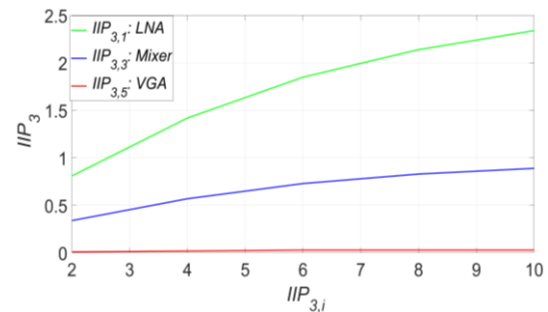

Fig. 18. SFDR improvement.

B. Discussion
For LPAP Rx, AFE and comparator technology determine the feasibility of demodulation. How high the RF frequencies can be processed is determined by the AFE and the comparator sampling rate determines the data symbol rate. Current BiCMOS/CMOS technology permits implementing the design of Rxs with low-power AFE with carrier frequencies as high as 125 GHz [37], and similar technology can be employed for implementing the LPAP Rx detailed in this paper. The comparators must have sufficiently high sampling rates to cover the wide signal bandwidth for ultra-high-speed data transfer. Assuming the power consumption values indicated in TABLE VII, the power breakdown as per configurations in TABLE VIII are given in TABLE IX. The state-of-the-art ADC in 20 nm CMOS has a FOM_{ADC} of 0.24 pJ, sampling rate of 16 GS/s with ENOB 6 bits [33]. Using (1) and $FOM_{ADC} = 0.24$pJ the power consumed by the ADC is determined. High-speed comparators are widely employed as low-power voltage slicers for decoding PAM-4/PAM-2

signals. Power consumption can be as low as ~1.7 mW for a 28-nm CMOS voltage slicer clocking at 30 GS/s [92], which is assumed in this paper.

TABLE VIII
RX CONFIGURATIONS

Rx	N_{RX}/PS/ LNA	N_S/VGA/ LO/Mixer	ADC	Comparator
ABF	32	1	1	x
HBF	32	2	2	x
DBF	32	32	32	x
LPAP	32	2	x	2

TABLE VIII
POWER CONSUMPTION*

Rx	LNA	MIXER	VGA	ADC	Comparator	Total
ABF	374.4	6.3	22.5	122.9	-	526.1
HBF	374.4	12.6	45	245.8	-	677.8
DBF	374.4	201.6	720	3932.8	-	5228.8
LPAP	374.4	12.6	45	-	1.7	433.7

*In mW.

The power breakdown of ABF, HBF and DBF is given in Fig. 19. The ADCs contribute the largest share ranging from 29% to as high as 85%, which is avoided by not employing them in the proposed LPAP Rx.
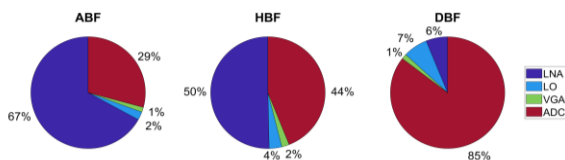

Fig. 19. ADC power consumption.

There are alternative approaches when using low-resolution ADCs i.e. 3.5-4 ENOB to lower the power requirements [93]-[99]. However, they do not consider the effect of wide bandwidths as in the case of ultra-high-speed data and algorithms at moderate sample rates of about 1GS/s [93]-[99]. For the expected ultra-high-speed data rates ADC power requirements will remain high even for lower resolutions. In comparison employing comparators the power requirements remain much lower for the similar data rates expected as shown in Fig. 20. The reference power taken is 1.7 mw, which is for a PAM-4 comparator at a sample rate of 30 GS/s [92].
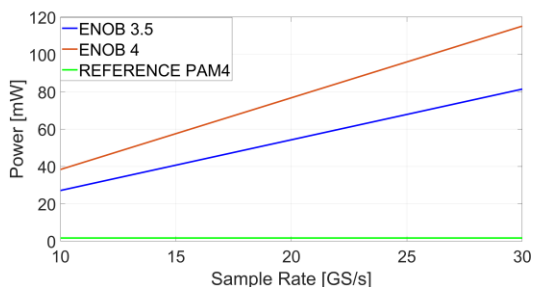

Fig. 20. Low resolution ADC power consumption.

The alternative approaches of low-resolution ADC algorithms are complex to implement and require additional

signal algorithms such as for synchronization, user scheduling and beamforming [94]-[98]. When employing low-resolution ADCs with ENOB of 3.5-4 the power requirement is 82mW-115mW at a sample rate of 30 GS/s, not accounting for the overheads for the additional signalling algorithms.

V. CONCLUSIONS

Designing energy-efficient mixed-signal and baseband units for ultra-high-speed Rxs require a paradigm approach such as analog processing which is detailed in this paper. The novel approach is based on RF correlation that can process ultra-high-speed data envisaged for B5G/6G/THz Rxs without the power-hungry ADCs. Circuit non-idealities such as linearity, noise figure, insertion loss, thermal and phase noise are taken into consideration. The 3GPP mmWave phase noise model is adopted to accurately model performance of LOs implemented in 28nm FD-SOI CMOS process. Two PAM-4 low voltage slicers are employed to replace the power-hungry ADCs. The digital decoder is not only able to support multiple modulations with a single architecture but also with the highest modulation reported so far for 16-QAM employing direct-demodulation. The digital decoder conforms to Gray mapping for the baseband signals minimizing the probability of bit error. Power analyses undertaken for current beamforming approaches requiring ADCs indicate a promising approach towards designing ultra-high-speed Rxs with low-power analog integrated circuit design solutions.
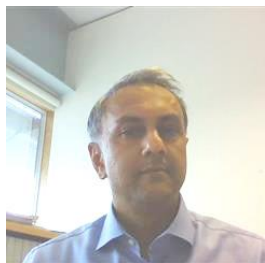
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