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OSPEN: an open source platform for emulating neuromorphic hardware

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ABSTRACT

This paper demonstrates a framework that entails a bottom-up approach to accelerate research, development, and verification of neuro-inspired sensing devices for real-life applications. Previous work in neuromorphic engineering mostly considered application-specific designs which is a strong limitation for researchers to develop novel applications and emulate the true behaviour of neuro-inspired systems. Hence to enable the fully parallel brain-like computations, this paper proposes a methodology where a spiking neuron model was emulated in software and electronic circuits were then implemented and characterized. The proposed approach offers a unique perspective whereby experimental measurements taken from a fabricated device allowing empirical models to be developed. This technique acts as a bridge between the theoretical and practical aspects of neuro-inspired devices. It is shown through software simulations and empirical modelling that the proposed technique is capable of replicating neural dynamics and post-synaptic potentials. Retrospectively, the proposed framework offers a first step towards open-source neuro-inspired hardware for a range of applications such as healthcare, applied machine learning and the internet of things (IoT).

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1. INTRODUCTION

With silicon pushed to its limits, we must look beyond conventional computing platforms. The brain realizes a huge number of tasks through flexible and power-efficient networks of neurons. To enable brain-like computations, a power-efficient neural fabric is needed to emulate the basic functionality of the human brain. The task of neural hardware implementation is challenging due to a large number of processing nodes (roughly 10^{11}) and rich interconnectivity (roughly 10^{15}) [1], [2]. Research work has recently focused on models which exhibit more plausibility to the human neural system. Similarly, wearable devices and sensors are commonly used for detecting abnormalities such as detection of seizures, patterns of movement, and behaviour [1]. However, continuous sampling of input signals requires power, hence neuro-inspired paradigms offer an alternative to the existing limitation of continuous signal measurement. The power aspect becomes even more important when it comes to applications based on lightweight portable devices.

Biologically plausible spiking neural models such as the spike response model (SRM) are particularly suitable in computational neuroscience because it is compute-efficient and captures most of the

biological dynamics [2]-[4]. Nonetheless, to efficiently emulate thousands of such neural entities on hardware/software platforms is challenging. As one of the main features of the human neural system is its parallel processing capability, during the past few years, significant advances have been made in techniques, methodologies, and applications of neural-based hardware [5]-[12]. The brain realizes a huge number of tasks such as adaptation, vision and recognition through flexible and power-efficient networks of neurons. It is challenging to investigate an unconventional multidisciplinary area of neural engineering because of the background knowledge required to understand biological principles and then apply them in computing-related applications. Growing research in the area of low-power neural engineering and related areas has triggered the interest to model such systems on electronic platforms [13]. The task of neural hardware implementation requires an extremely large number of processing nodes, rich interconnectivity, and adaptation mechanisms [14]. It is well understood that low-power devices with particular applications in environmental sensing, healthcare and internet of things (IoTs) represent unprecedented challenges with the growing need for trillions of interconnected devices, ubiquitous sensors, and actuators that are expected to be interconnected. There are several challenges that the scientific community faces today such as compatible architectures and platforms for such devices to talk to each other and actual hardware with battery-less energy scavenging techniques, to name a few.

This paper offers a novel neuro-inspired platform that could potentially be used for research as well as integrating several neuro-inspired applications such as healthcare electronics and integrated low-power sensors. Hence, IoT-based devices are particularly promising for applications in medicine and healthcare [15]-[18]. Such devices have greater potential to reduce the ever-increasing cost of care in developed as well as developing countries. To provide quality of care and remote healthcare monitoring facilities, it is imperative to have an open-source hardware platform for modelling, analysis, and prototyping. In this paper, results are reported from experiments conducted in both software and hardware. The hardware chip is fabricated with a 0.35 um complementary metal-oxide-semiconducto (CMOS) process [19], [20]. This paper offers a systematic approach to building a platform from software prototyping, silicon implementation, electrical characterization, and empirical modelling. Section 2 details the research method where spiking neural model was investigated in software domain. Section 3 presents the hardware circuits to capture neural responses akin to the biological neurons. The hardware structures were fabricated and characterized whereas the data extracted through the fabricated device was empirically modelled in the form of mathematical equations and embedded into software domain for benchmarking applications. It is envisaged that this work will offer an open-source platform where generic neural fabric is available to researchers and practitioners for prototyping applications in the domain of neuromorphic hardware. Our long-term objective is to offer the very first, an open-source neuromorphic hardware platform for artificial intelligence (AI) enabled healthcare devices and related industrial applications.

2. RESEARCH METHOD

Recent advances in machine learning necessitate computation-efficient paradigms on both software and hardware platforms. When spike-based computation models, such as spiking neural networks (SNNs), are run on neuromorphic hardware, they have a huge potential to reduce energy usage. Nonetheless, due to the large number of neurons and synapses required at a biological scale, simulating and mapping SNN architectures on a hardware platform is a daunting task. The proposed method takes a novel approach by simulating neuronal entities in software before capturing and replicating their dynamics. Rather than designing and fabricating custom hardware circuits and architectures for a specific application, generic customised neural cells are investigated and developed. Empirical models developed from the data extracted through the fabricated structures. This approach offers true replication of the neuromorphic hardware which is cost-effective and saves time and effort to develop neuro-inspired applications. As spiking neurons are considered more biologically plausible, they use spikes as the communication mechanism between different entities. Depending on the model, each spike can be defined as a binary event where the actual timestamp of the spike carries information. Spiking neuron communication behaviour is shown in Figure 1 where I_n are the input currents, s synapses and n the neuron membrane which connects with following synapses and outputs are generated, as denoted by O_n.

2.1. Neuron circuit simulations

In this work, an SRM model is considered for investigation and implementation. The membrane potential of the model can be represented by (1), whereas postsynaptic potential is represented by (2).

$$V_m(t) = \sum_{t_i^{(f)} \in F_i} \eta_i\left(t - t_i^{(f)}\right) + \sum_{j \in \Gamma_i} \sum_{t_j^{(f)} \epsilon F_j} w_{ij} \varepsilon_{ij\,(t-t^{(f)})} \quad (1)$$

$$\varepsilon_{ij}\left(t - t^{(f)}\right) = \frac{t}{\tau}\exp\left(-\frac{t}{\tau}\right) \quad (2)$$

As shown in (1), the expressions represent as follows: V_m is the membrane potential, η_i (action potential), $t_i^{(f)}$ (the last firing time of neuron *I*), $t_j^{(f)}$ pre-synaptic input spike from neuron *j*), $\varepsilon_{ij\,(t-t^{(f)})}$ (the PSP of neuron *i* caused by a spike from neuron *j*), w_{ij} (synaptic strength), F_i (the set of all firing times of neuron *I*, and Γ_i represents the set of all presynaptic neurons. Whereas in (2), tau represents the rise and fall time of the postsynaptic response.

In order to replicate and capture the neural dynamics, the simulated neural circuit is shown in Figure 2. As shown in the Figure 2, input stimuli (I_1 and I_2) are connected with two SRM neurons (N_1 and N_2) respectively where N_1 is considered excitatory and N_2 inhibitory. The neurons are connected via static synapses. The parameters used for simulating this circuit are shown in Table 1. To have insight into the biological domain, different papers were surveyed to collect realistic biological data sets. We need to know our limitations in terms of hardware implementation and the values required to develop a biologically plausible SNN platform. These parameters have also been widely used in computing-related tasks. For the neuron model and related parameters used for simulations, we refer the reader to [21] and [2].

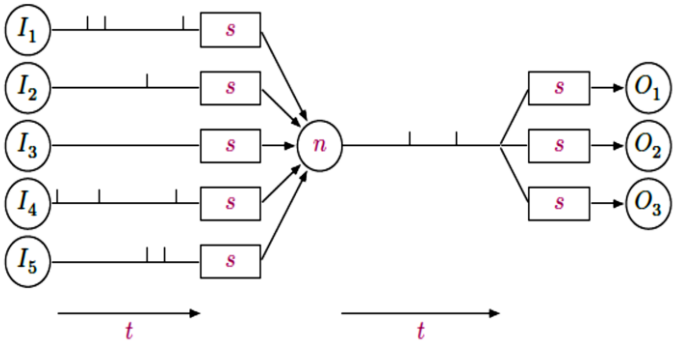


Figure 1. Standard spiking neuron with synaptic connections

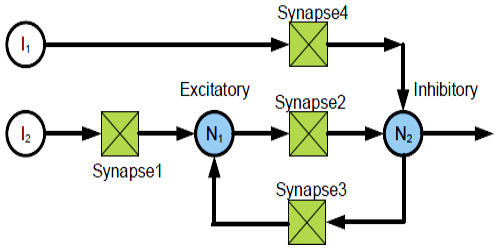


Figure 2. SRM circuit diagram

Table 1. Simulation parameters [9]

Parameters	Units
Membrane time constant	30 ms
Absolute refractory period	3 ms
Reset voltage	13.5 mV
Resting voltage	0 mV
Threshold voltage	15 mV
Background noise	13.5 nA
Input resistance	1 MOhms
Synaptic delay	1 ms

The software simulation results are shown in Figure 3 where the top plot shows the input stimuli (analogue and digital) and the second plot from the top shows the output spike times at different time steps. Plot 3 from the top shows the membrane potential of both neurons and the bottom plot shows the postsynaptic potentials for all four synapses. As shown in the figure, two inputs (analogue and spiking) were

connected with two neurons (excitatory and inhibitory) via synapses. Whereas the main difference between excitatory and inhibitory neurons is that the excitatory neurons fire an action potential in the postsynaptic neuron and inhibitory neurons inhibit the firing of an action potential. For further details on synaptic potentials and membrane dynamics, we refer the reader to [2].

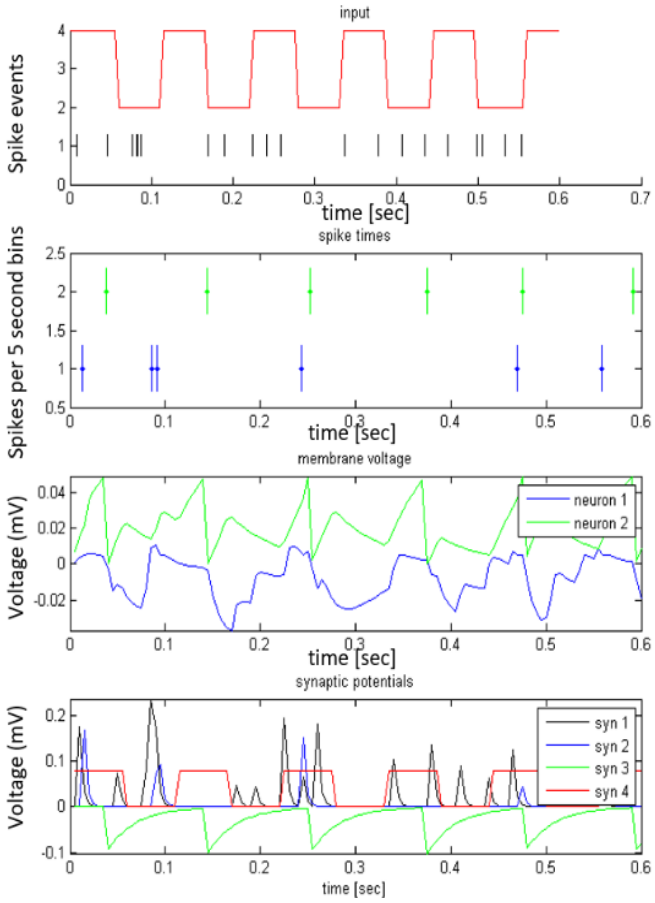


Figure 3. SRM circuit response in terms of membrane voltages and synaptic potentials

2.2. Postsynaptic response and membrane potential

As information in spiking neurons is conveyed through spikes where postsynaptic response plays an important role in neural dynamics. By increasing or decreasing the rise and fall times of the postsynaptic potential, the output firing patterns change to a greater extent [3]. To further examine the impact of input spike train on postsynaptic responses and membrane potentials, a rather simple model is emulated in software. This model includes a threshold voltage which is compared with the membrane potential. An output spike is generated if the membrane potential exceeds the threshold value, whereas a spike threshold is calculated for each time step. Figure 4 elaborates an input spike train, postsynaptic responses, corresponding membrane potentials, and output spike train. It is observed that during the rise and fall time of the postsynaptic potentials, the dynamics of a neuron change. The impact of τ was observed on the neural membrane accordingly.

The top plot in Figure 4 shows an input spike train whereas the middle plot shows the postsynaptic response and the bottom plot shows the membrane potential and output spikes. It can be seen that each input spike creates a postsynaptic response at a specific time step which is accumulated into the neuron's membrane. Once the membrane potential exceeds a certain threshold, output spikes are generated at a specific time interval. It can be inferred from these simulations that the spike times play an important role in neural signal processing where the output spikes translate the input spike frequency. The main purpose of simulating these circuits was to capture some of the neural dynamics and translate them into hardware structures for large-scale implementations.

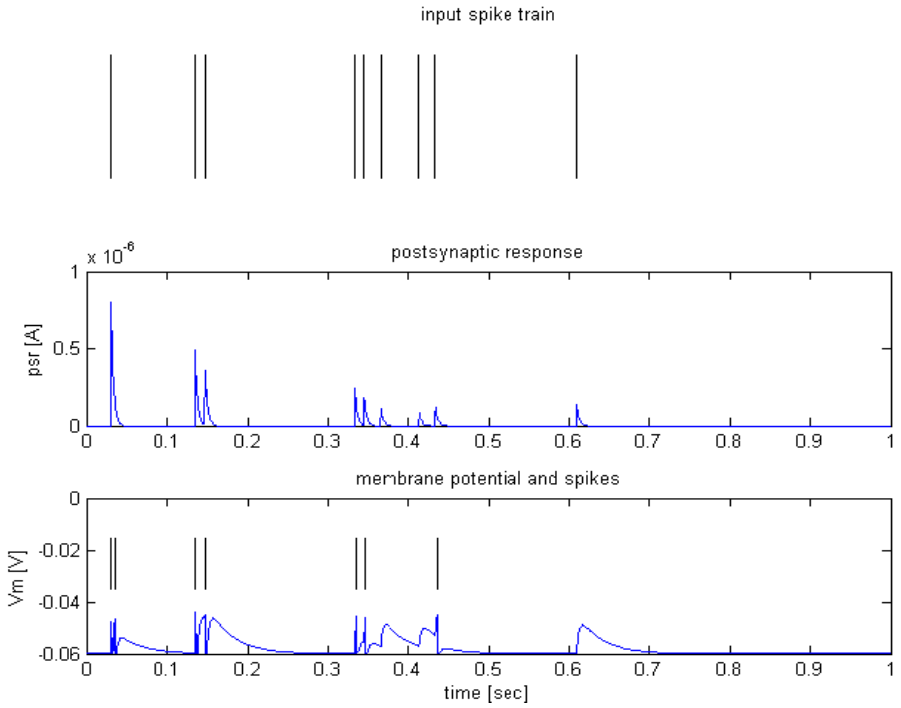


Figure 4. This figure shows the input spike train, postsynaptic responses and corresponding membrane potentials

2.3. Hardware modelling of postsynaptic potentials

Once the basic functionality of neural entities was examined through software simulations, hardware fabric was designed, fabricated, and characterized. The chip was fabricated by Europractice with the 0.35 um AMS n-well process. The basic circuits of synapses and neurons are shown in Figure 5. Further details are provided in [19], [20], [22].

To benchmark the characteristics of neural cells, several synapse/neuron blocks were implemented where each circuit on the chip comprised a synapse cell connected to a neuron circuit. As shown in Figure 5, in the absence of synaptic activity, the V_{IN} node sits at a voltage slightly lower than VDD, due to the leakage current at that point and the need for this to be sourced by M1. When a pre-synaptic neuron fires (V_{PRES}), electronic charge is transferred onto the output node of the synapse, reducing the value of V_{IN}. This transient reduction in voltage is fed through a buffer and measured on an oscilloscope. The PSP is formed by the charging and discharging of the capacitance, C present at the drain of M5. A current passing through M4, I_{M4} will charge the capacitor to a value V_{PSP}, and it is subsequently discharged by the current flowing through M5, I_{M5}, which defines the fall time of the PSP. Ideally, $I_{M4} >> I_{M5}$, so that the leakage current has no discernable effect on the charging of the capacitor. Once V_{PSP} reaches the switching threshold for the inverter M6/M7, the neuron 'fires', producing a voltage pulse at the V_{OUT} node, before V_{PSP} is discharged through M10. The layout of the chip is shown in Figure 6 which implements the circuits shown in Figure 5, alongside structures/circuits for characterisation and testing. An XOR benchmark was implemented on the chip and characterized. Further details on hardware implementation and benchmark applications are provided in [19], [23].

2.4. Hardware measurements

V_W, V_{PRES}, V_{LEAK}, and V_{DD} were supplied to the IC input using a semiconductor parameter analyzer, providing independent control over each voltage. The measurements were taken from the chip by direct probing. The outputs from the probe station were recorded using a Tektronix oscilloscope. Whereas voltage V_W sets the level of synaptic charge and V_{LEAK} controls the fall time of the PSP. Charge transfer through the synapse is initiated by the application of a single pulse to the V_{PRES} terminal of the synapse. The magnitude of the pulse is set to VDD, the 10-90% rise/fall times are 5 ns and the 50-50% pulse width is 20 ns. To analyze PSP response from the fabricated chip, extracted data is plotted and to further investigate the computational capability of fabricated structures, an empirical model was developed based on the data extracted from the chip. Figure 7 shows the PSPs which are sampled for $0<V_W<3.3$ V in 50 mV increments and V_{LEAK} is set to 0.24 V.

To provide a generic neural fabric to benchmark neuro-inspired applications, an empirical model was developed by Gaussian curve fitting. The data extracted from the fabricated chip was used to develop the empirical model as a function of weight. This model replicates neural dynamics and postsynaptic potential measured through a chip with a similar time scale (Figure 7 (a) and Figure 7(b)). The mathematical equation is shown in (3), where the response model is the product of three parts.

$$y = \left[y0 + Ae^{-\frac{x.(x-x_C)^2}{2w^2}}\right].(1-e^{-bx}).\varepsilon(x-t_{spike}) \quad (3)$$

These three parts are an amplitude version of the Gaussian peak function, a Box Lucas function, and a step function. Whereas *yo*, *A*, *b*, *w* and x_c are real constants and ε is a response kernel that exhibits the typical time course of an excitatory postsynaptic potential in terms of response voltage approaching zero from above. By using this approach, the responses of the spikes with different synaptic weights were modelled mathematically. It is particularly important to have an empirical model that mimics the actual behaviour of the fabricated device.

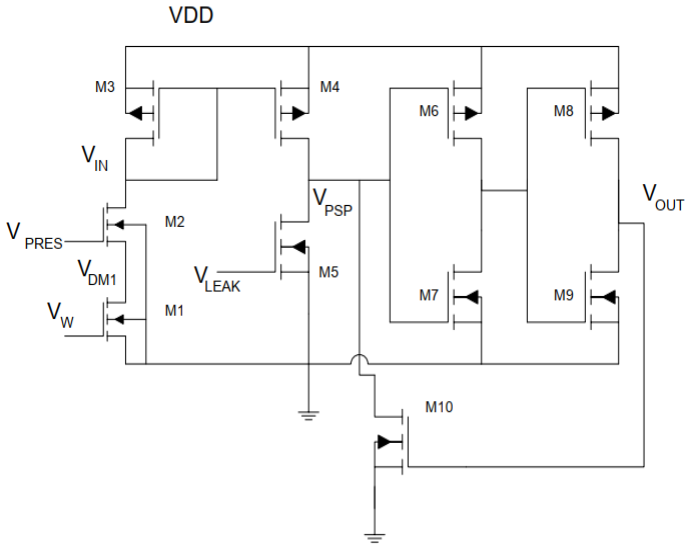


Figure 5. Synapse and neuron circuit [19], [20]

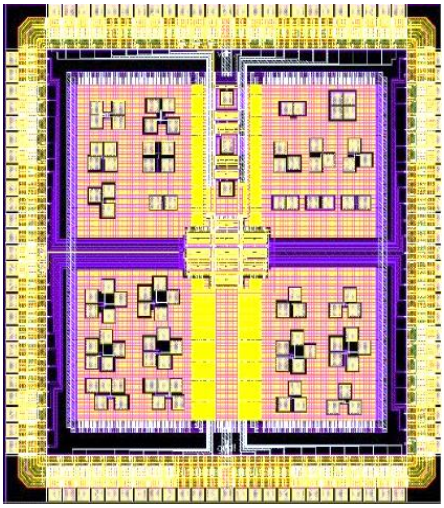
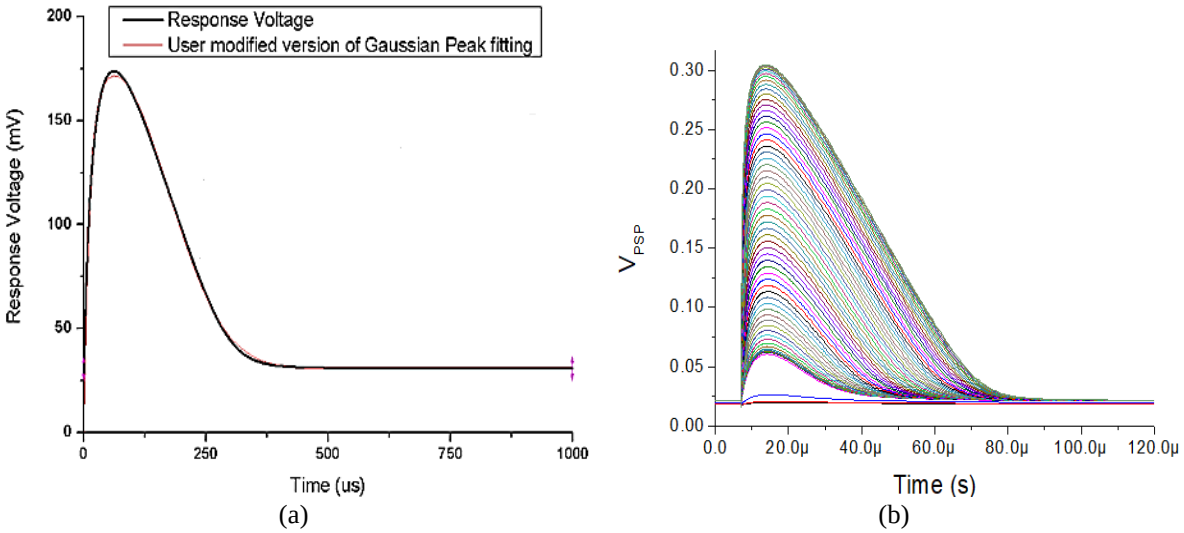


Figure 6. Chip layout (3.7x3.7 mm) [20]



(a) (b)

Figure 7. This figure shows the comparison between actual data extracted from the chip and the empirical model for (a) a single and (b) multiple synapses

3. RESULTS AND DISCUSSION

Previous research in neuromorphic engineering is mainly done through hardware implementations or software modelling. In particular, hardware implementations were constrained and were capable of characterizing the effects of a few variables. It was mainly due to the number of experiments needed to capture neural dynamics being specific and limited. Software-based approaches, nonetheless, capture high as well as low-level dynamics, without regard to any transistor or layout-level aspects, hence lacking accuracy at the device level. In order to observe neural dynamics at the device level and explore real-life engineering applications, it would be unrealistic not to consider the necessary process and layout-related information. For rapid development and prototyping of neuromorphic applications, novel approaches are needed to implement and analyze neuro-inspired paradigms. This paper demonstrated the viability of implementing neural dynamics on software and hardware platforms whereas the data extracted through fabricated neural structures were empirically modelled and provided as an open-source [24]. To investigate software based spiking neuron models in Python, readers are referred to [25]. The repository provided in [24] currently contains the code, empirically modelled postsynaptic potentials, neural membrane potentials, and mathematical equations that can be embedded into the software domain. The authors have provided this repository as an open-source platform for the neuromorphic research community to make use of the existing code, equations, and models and hope it would be further complemented with bespoke datasets and empirical models.

4. CONCLUSION

To summarize, this paper offers a proof-of-concept demonstration of the spiking neural circuits capturing some of the neural dynamics. It is shown by experimental results (software and hardware) that it is viable to look beyond traditional paradigms and explore neuro-inspired cells as computational entities. Empirical models were developed from the data extracted through the fabricated device and accuracy was confirmed. This work demonstrates the feasibility of an open-source neural hardware platform where neural fabric can be provided for rapid investigation and development. Authors have set up a GitHub repository where mathematical equations and MATLAB code for empirically modelled postsynaptic potentials and neural membranes are provided. Due to the analogue nature of neural cells and synapses, millions of such computational entities are possible to realize on-chip and with the provision of an open-source neuromorphic repository, further applications related to machine learning, deep neural networks and IoTs can be explored.

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