A Bidirectional ASIC for Active Microchannel Neural Interfaces

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***Abstract*—Closed-loop neural prostheses have been widely used as a therapeutic strategy for a range of neurological, inflammatory, and cardiac disorders. Vagus nerve stimulation has shown promising results for the monitoring and treatment of post-operation symptoms of heart transplant recipients. A prime candidate for selective control of vagal fibres is the microchannel neural interface (MNI), which provides a suitable environment for neural growth and enables effective control of the neural activity in a bidirectional system. This paper presents the design and simulation of an ASIC in 180-nm high-voltage CMOS technology, capable of concurrent stimulation and neural recording with artifact reduction in a seven-channel MNI. The analog front-end amplifies action potentials with a gain of 40 dB, presenting a common-mode rejection ratio of 81 dB at 1 kHz and a noise efficiency factor of 5.13 over the 300 Hz to 5 kHz recording bandwidth. A 42-V-compliant stimulation module operates concurrently and independently across the seven channels.**

Keywords—Bidirectional neural interface, biomedical electronics, high-voltage stimulation, microchannel electrodes, neural recording, vagus nerve stimulation.

I. Introduction

Denervation of the autonomic fibres following a heart transplant results in severe limitations in exercise capacity for patients suffering from heart failure due to chronotropic incompetence, which restricts the ability of appropriately increasing the heart rate to meet metabolic needs [1]. A recent approach to improve the quality of life of post-transplant patients includes electrical stimulation of the vagus nerve (CN X), that has shown benefits in correcting autonomic imbalance [2]. However, effective modulation of the vagus nerve requires a highly selective interface that provides concurrent stimulation and acquisition of neural activity for a truly bidirectional system. The measurement of meaningful signals from the nervous fibres poses several challenges for the design of a closed-loop implantable bioelectronic system.

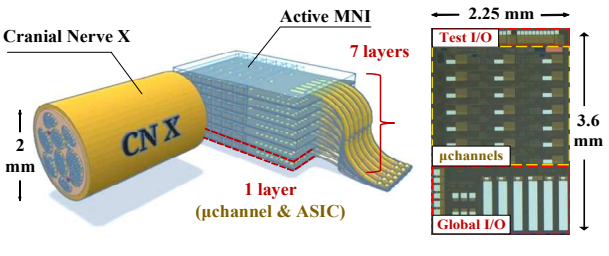
The trade-off between the selectivity and invasiveness of neural interfaces demands various considerations for the selection of the appropriate structure. Regenerative electrodes have shown promising results in providing a selective interface while guiding neural growth. In particular, the microchannel electrodes, which enclose groups of axons within insulating tubes, have enabled effective stimulation and recording of neural fibres independently from the position of the nodes of Ranvier. The increased extracellular resistance requires smaller stimulus amplitudes and results in larger recorded signals (neural spikes or action potentials). Typically, microchannels range up to 5 mm in length and 200 µm in diameter to minimise channel blockage while providing adequate space for vascularisation of the nerve [3]. High-density microchannel neural interfaces (MNIs) can overcome the limitations of electrode interconnects via multiplexed, on-chip contacts that access the channels more easily and limit device complexity. Moreover, on-site electronic circuits capable of stimulation and recording of the neural signals would allow concurrent multi-channel operation and high-quality acquisition of action potentials, while the structure of the MNI enables scaling of the system by stacking multiple units [4].

Action potentials recorded extracellularly are orders of magnitude smaller than the surrounding noise. Collecting meaningful data requires a common-mode rejection ratio (CMRR) in excess of 80 dB [5] via analog signal processing through in-situ amplification to minimise sensitivity to artifacts. Due to the high contact impedance of the microchannel electrodes, a large voltage compliance is necessary to deliver the required stimulus currents. This results in artifacts that can be detected by adjacent recording channels, causing distortion in the measured signal, or completely masking the biosignals. A method that carries out automatic detection and reduction of the stimulus artifacts was developed using a comparator and an adjustable band-pass filter [6], forming a closed loop to apply pole shifting upon detecion of artifacts. High-voltage (HV) stimulus currents are necessary to safely deliver balanced, biphasic pulses with varying frequencies to elicit or inhibit neural activity.

This paper presents the design and simulation of an ASIC for a bidirectional active MNI. The concept diagram shown in Fig. 1(a) represents seven stacked devices, each containing seven 300-µm-pitch microchannels with tripolar electrodes on the ASIC shown in Fig. 1(b). The interface aims to enclose sections of the thoracic branch of the vagus nerve within 49 channels. Section II outlines the system requirements for a multi-channel bidirectional interface with artifact reduction. Section III describes the top-level architecture and the system sub-blocks. Post-layout simulation results are shown in Section IV. Discussion and concluding remarks are presented in Section V.

II. System Requirements

Modulation of the vagus nerve fibres requires a biocompatible neural interface capable of safely delivering stimulus currents whilst adequately measuring neural signals to form a closed loop system. The safety of the implant must be ensured to avoid any toxic effects on the tissue or corrosive impacts on the electrodes.



(a) (b)

Figure 1. Active MNI; (a) conceptual view, and (b) ASIC micrograph.

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A. Neural Excitation

Electrical stimulation of the neural fibres in miniaturised interfaces requires electrode voltages above 10 V to deliver the necessary currents, which range from 5 µA to 25 µA in microchannels [4]. As the channel impedances reach 1.24 MΩ [3], activation of the fibres requires a voltage compliance exceeding 30 V. Restrictions in the maximum drain-to-source (V_{ds}) and gate-to-source (V_{gs}) voltages of standard CMOS transistors require advanced methods such as transistor stacking [7] or HV shielding [8] to operate safely and integrate the HV output stage with the LV circuits. Furthermore, the device should be capable of providing balanced stimulus pulses with a reliable control over the programmed current. A tripolar electrode configuration is preferable to deliver focused stimulus pulses [9].

A high-output-impedance current driver is required to limit the effects of load variation on the delivered charge and provide the necessary precision and sensitivity within a limited circuit footprint. Current-mode digital-to-analog converters (I-DAC) are typically implemented in conjunction with a high-voltage output driver that consists of current mirrors for a stable stimulus current [10]. Additionally, charge imbalance must be minimised by passive or active charge balancing to prevent the build-up of residual charge at the electrode.

B. Feedback Acquisition

Closed-loop interfaces have been widely developed for the peripheral nerves to provide advanced performance. Feedback can be obtained as biomarkers from the vagus nerve via measured action potentials, which range above 100 Hz in frequency with amplitudes varying from approximately 30 µV to 200 µV in silicone microchannels of the proposed dimensions [3]. Careful amplifier design is required to adequately record neural signals in the presence of noise sources that exceed 10 mV. Several techniques for low-noise amplifier (LNA) design have been developed to filter out-of-band noise sources and limit in-band sources such as the 1/f noise to limit contribution to the input-referred noise (IRN) and the noise efficiency factor (NEF), which highlights the noise-power trade-off [11]. Operational transconductance amplifiers (OTA) are a common element of neural recording systems, with cascode topologies achieving a high gain within a limited front-end area.

Concurrent neural stimulation and recording requires appropriate methods for the detection and mitigation of the resulting stimulation artifacts. Such techniques can be applied to prevent the recording of artifacts, to improve the resilience of the recording front-end for a linear response, or to reconstruct the measured signal at the cost of increased complexity and circuit area. Although the preventative measures cannot provide complete removal of the artifacts, they are often used to ease the requirements on the recording amplifier [12].

III. ASIC Architecture

A. Overal Structure

The active MNI chip has seven channels, each comprising stimulation and recording modules with independent control over the channel functions according to the received commands. Fig. 2 shows the system block diagram. It shows the circuits local to each microchannel comprising the stimulation module, recording front-end, and the local logic, as well as circuits global to the chip, including voltage and current biasing, an analog output stage comprising a 7-to-1 multiplexer and buffer for the measured signal, a power-on reset signal source with brown-out detection, and a global ID storage unit to identify one of seven ICs in a stacked interface.

The system is provided with six main I/O pads, which carry the ground line, the LV (1.8 V) and HV (42 V) supply voltages, a 1 MHz clock signal and a digital input line for communication, and an analog output for the recorded neural signal. Although multiple channels can stimulate at the same time, the system I/O pads enable single-channel recording with swift transitions across the seven IC channels. A pseudo-tripolar electrode arrangement is implemented via the three electrode pads ($E_{A,B,C}$) in each channel to limit the effects of interference on the recorded signal and achieve a more focused electric field during stimulation.

B. Stimulation Module

The high-voltage biphasic stimulus pulses are provided by current drivers local to each channel. These mirror the signal generated by a 5-bit I-DAC through two high-swing super-Wilson current mirrors at the outer electrode nodes E_B and E_C to achieve current steering. Each current mirror is supplied with two separate paths that determine the pulse polarity based on the digital signals for the cathodic (Φ_C) and anodic (Φ_A) phases. The I-DAC is designed using a binary-weighted topology to supply an output current ranging from 2 µA to 62 µA at each outer node, providing a maximum stimulus current of 124 µA through the central electrode pad. The output of the I-DAC is mirrored through a simple current mirror that enables a least significant bit (LSB) calibration at the outer pads. An overview of the HV stimulator output stage is shown in Fig. 3(a).

Thick-oxide transistors were selected for the output stage to ensure safe operation with a high voltage compliance; level shifters apply the pulse control signals Φ_C and Φ_A at the necessary voltage to ensure safe operation of the HV transistors and switches, which also provide a path to ground for passive charge balancing following a biphasic pulse. The high-swing super-Wilson current mirror at each outer branch is shown in Fig. 3(b).

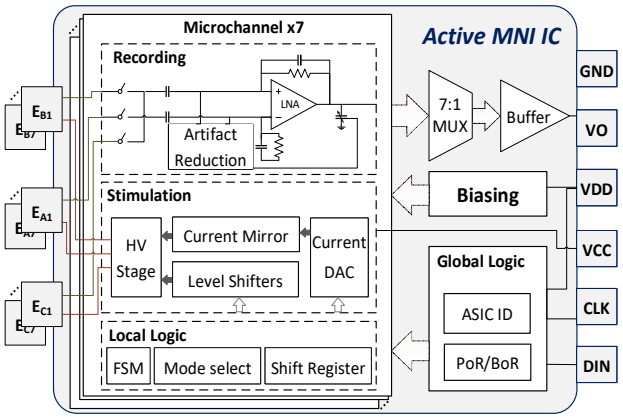

Figure 2. System block diagram of the active MNI IC (modified from [6]).

C. Recording Module

An LNA was designed using the ac-coupled capacitive network structure with a telescopic cascode OTA to achieve a high output impedance with a gain of 40 dB over the bandwidth of 300 Hz to 5 kHz. High-voltage blanking switches at each electrode pad provide protection from the HV pulses during same-channel stimulation. To achieve a small channel area and power with minimum PVT variation, the LNA feedback pseudo-resistors were designed using the parallel-NMOS architecture with optimum control over their equivalent resistance via a stable control current that is generated globally [6]. The OTA transistor parameters were selected to reduce the noise introduced by the input and load transistors while also achieving a trade-off between power consumption and open-loop parameters of the circuit for a stable response.

Two differential comparators and D flip-flops that detect the absolute value of the input signal exceeding a pre-defined threshold form the artifact detection unit. The resulting output pole shifts the amplifier's low-pass response by adjusting the output capacitor accordingly. Fig. 3(c) shows the neural recording module, which includes an AND gate to enable the pole shifting operation. This user-specified *BW_en* signal is extracted from the control command transmitted to all channels.

D. Digital Control

A 32-bit command frame can be received by the channel logic blocks to determine the state of the control switches that define the channel's operating mode, phase, and parameters. The stimulation modes provide low-frequency (LF, 10 Hz to 50 Hz) pulses to elicit neural activity, high-frequency (HF, 10 kHz to 20 kHz) pulses to block neural signals and chopped (500 kHz packets within a LF envelope) pulses [13] using a finite-state machine. The recording settings enable pole shifting. As the command signal is broadcast to all the channels on every chip, initial ID checks are carried out to determine the intended channel via three pull-up/down resistors at each channel that specify its local address along with the programmable global ID blocks that locate the desired ASIC. In addition to the stimulation and recording functionalities of the channel, the system can be commanded to read and store the three-bit global ID upon power-up and to carry out electrode pad electroplating for ASIC post-processing.

IV. Simulation Results

Post-layout simulations of the analog blocks have verified their performance. Parametric and transient analyses of the stimulus pulses were used to model the accuracy and matching of the biphasic pulses, while the quality of the recorded signal was determined via frequency analysis. The performance of the overall system was observed in a mixed-signal environment via a top-level digital testbench that cycles through the operating modes. The ASIC draws 0.49 mW during the idle state with 13.3% (64.9 µW) in each channel (43.4 µW for stimulation, 5.1 µW for recording, and 16.5 µW for logic) and 6.5% (32 µW) in the global region.

A. Electrical Stimulation

Rectangular stimulus pulses of varying settings were generated according to the logic control switches. The current steering outputs were modelled with unequal intensities via the individual LSB control bits. Monte Carlo analyses of the largest output (62 µA) setting showed an average value of 62.3 ± 0.5 µA, which can be calibrated prior to implantation.

A maximum phase mismatch of 3.4% was observed on the low-frequency 2 µA current setting, which can be accounted for with discharge phase duration. Fig. 4(a) illustrates the stimulus current (I_{STIM}) during the three modes, programmed to supply one cycle of LF pulses at 2 µA, followed by HF and chopped pulses at 22 µA.

B. Neural Recording

Initial frequency analyses on the amplifier were carried out during the optimisation process, resulting in an IRN of 6.3 μV_{rms} [Fig. 4(b)] and an NEF of 5.13, which are sufficiently low to detect the smallest predicted biopotential markers (30 µV). Further simulations confirmed a closed-loop amplifier gain of 40 dB [Fig. 4(c)] and a CMRR of 81 dB at 1 kHz [Fig. 4(d)], which exceeds the necessary performance. Monte Carlo analyses of the pseudo-resistor with 200 runs showed a standard deviation of 1.5% with PVT variations, which corresponds to approximately 23 Hz of variation in the frequency domain.

In addition to the sinusoidal input signals generated at varying frequencies to model the action potentials, composite forms of the signals with rectangular stimulus pulse artifacts

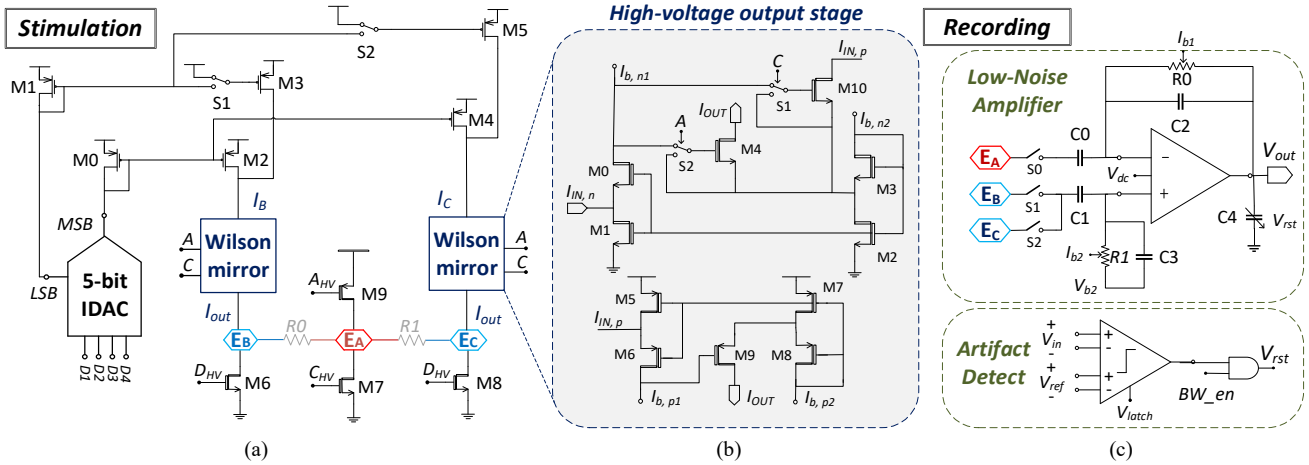

Figure 3. Schematics of the channel; (a) stimulation output, (b) super-Wilson current mirror, and (c) recording blocks [6].

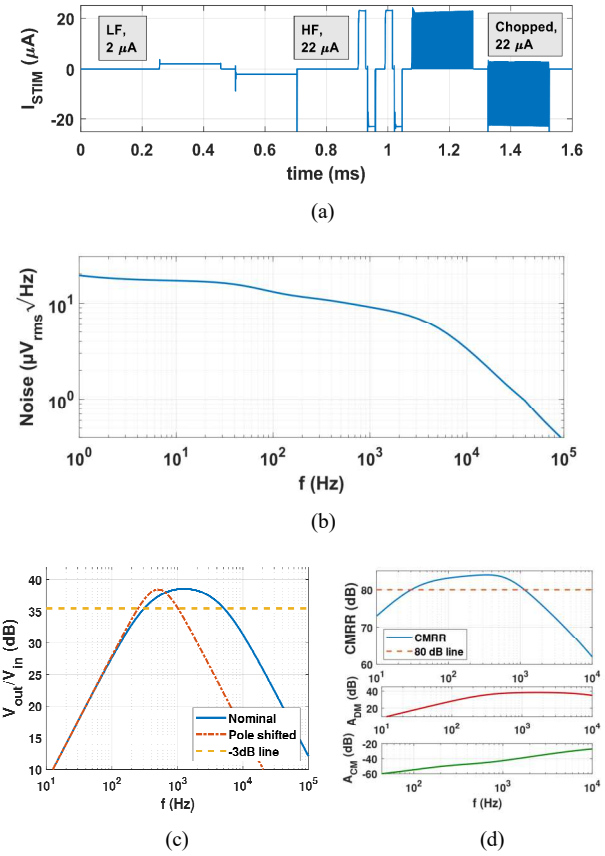

Figure 4. Simulated results of (a) stimulation modes, (b) recording path input-referred noise, (c) amplifier gain, and (d) amplifier CMRR.

were also provided to the inputs of the LNA and passed through an additional filtering stage at the output, providing a 54 dB artifact attenuation ratio. Table I provides a comparison with other work.

TABLE I. COMPARATIVE SUMMARY OF PERFORMANCE

	[14]	[15]	[16]	This work
Technology	130 nm	180 nm	65 nm	180 nm
Channel count	32 sense & stimulation	8 sense, 4 stimulation	64 sense, 4 stimulation	7 sense & stimulation
Electrode setup	Bipolar	Bipolar	Bipolar	Tripolar
Stimulation Compliance Amplitude Frequency	 3.3 V 3 mA 5 Hz	 - 600 μA 12 Hz	 ±11 V 10 μA – 10.2 mA 10 Hz	 42 V 2–124 μA 7.4 Hz – 20 kHz
Recording Bandwidth CMRR IRN (μV_{rms})	 1– 500 Hz > 70 dB 1.6	 1 Hz – 2 kHz - 5	 10 Hz – 1 kHz - 2.9	 300 Hz – 5 kHz 81 dB 6.3
Artifact attenuation	Yes	42 dB	60 dB	54 dB
Die size	10.9 mm^2	1.4 mm^2	4 mm^2	8.1 mm^2
Power draw	54.4 μW	3.96 μW	0.62 mW	0.49 mW

V. CONCLUSION

This paper has presented the design and simulation of an active microchannel neural interface that provides concurrent stimulation and recording of regenerated neural fibres. The system is intended for the vagus nerve for the treatment of post-operative symptoms of heart transplant patients. However, it can be implemented for a wider range of applications. Post-layout simulations of the ASIC have shown a amplifier response with a CMRR of 81 dB at 1 kHz and an overall NEF of 5.13. High-voltage stimulus pulses were observed at various frequencies with a 54 dB artifact attenuation within a total chip area of 8.1 mm^2.

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