Origin of trap assisted tunnelling in ammonia annealed SiC trench MOSFETs

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The interface between silicon carbide (SiC) and silicon dioxide (SiO 2 ) is of considerable importance for the performance and reliability of 4H-SiC trench metal oxide semiconductor field effect transistors (MOSFETs) and various different post oxidation anneals (POAs) have been used to optimize its quality. Whereas nitric oxide (NO) POA leads to very reliable and well performing MOSFETs, ammonia (NH 3 ) can further improve the device performance, however, at the cost of the gate oxide (GOX) reliability, e.g. leading to trap assisted tunneling (TAT). We investigate the origin of TAT and GOX leakage in differently annealed gate oxides experimentally, using 4H-SiC trench MOSFETs, and theoretically, using Density Functional Theory (DFT) simulations. Our findings reinforce the view that the NO anneal for SiC devices results in the best overall quality as devices annealed in NH 3 and nitrogen N 2 show higher oxide charge density and leakage currents. DFT simulations demonstrate that, contrary to what has often been assumed so far, NH 3 annealing leads to the formation of additional hydrogen related defects, which open leakage paths in the oxide otherwise not present in NO treated oxides.

1. Introduction

The wide band gap material SiC is an attractive alternative to silicon (Si)-based metal oxide semiconductor (MOS) structures for high power electronics. It offers higher breakdown fields and therefore higher blocking capabilities [1], a high melting point and high hardness [1], which makes it well-suited for applications in harsh environments, e.g. at high temperatures [2,3]. Even though well-performing SiC MOSFETs already exist, there is still room for improvement regarding their performance and reliability. For this reason, process variations are regularly studied to further optimize device performance, for instance via different post oxidation anneals (POAs). At the moment, POAs in NO are very common because they lead to a good balance between reliability and performance [4–6]. However, the NO POA has to balance two competing components during the anneal, which are defect passivation on one hand and SiC oxidation on the other hand. This additional oxidation may lead to the formation of new defects during the anneal [7,8]. For this reason, non-oxidizing annealing gases such as e.g. NH 3 have come into focus. Recent studies already showed the superior time-zero device performance of NH 3 annealed gate oxides in MOSFETs [9,10]. At the same time, a reduced device reliability in the form of increased gate leakage has been found (cf. [10] for details). It has been shown recently [11,12] that trap assisted tunnelling (TAT) in SiC/SiO 2 MOS capacitors employing a high-quality thermally grown oxide can be linked to intrinsic electron traps [13,14] within the SiO 2 .

In one of our previous studies [15] we found strongly increased TAT in NH 3 annealed trench MOSFETs and initially attributed this to intrinsic electron traps as well. However, this first guess is based on a very simplified approach of extracting the defect activation energy which is not sufficiently describing real trapping mechanisms. For this reason, in this work, the previous studies are extended towards identifying the cause of TAT in NH 3 annealed oxides via combining both experimental and theoretical work. Furthermore, the effect of different POAs on the gate leakage is studied and correlated with theoretical trapping and leakage models from literature. Our studies clearly suggest that TAT

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in the NH₃ treated oxides is not caused by an intrinsic electron trap as previously suggested [15] but rather by hydrogen related defects which are formed during the POA.

2. Experimental

2.1. Measurements

N-channel 4H-SiC trench MOSFET test structures fabricated on commercial n-doped Si-face substrates were studied. In these devices, the conductive channel forms along the a-plane whereas the trench bottom is along the Si-plane. Therefore, effects of both planes are expected to play a role in the gate oxide tunnelling behaviour. The gate oxide was deposited with chemical vapour deposition and afterwards annealed in NO, NH₃, N₂ or a combined process of an NO POA followed by a subsequent anneal in NH₃ (NO + NH₃). More details about the process parameters can be found in [10,15]. The N₂ POA here serves as a reference because according to a chemical analysis employing X-ray photoelectron spectroscopy (XPS) [16], this POA does not incorporate nitrogen (N) into the bulk of the oxide, as confirmed by SIMS measurements [17]. Nevertheless, our experiments show that the additional temperature treatment leads to a densification of the oxide compared to an as-deposited oxide.

Gate oxide tunnelling and breakdown were studied using continuous voltage sweeps and stress measurements similar to TDBB experiments. In order to study and identify the tunnelling mechanism, gate voltage sweeps were conducted. In [15] the dependence of the measurement temperature was studied. Here, the dependence of gate leakage of the processing parameters like POA temperature was studied. Here, the dependence of gate experiments. In order to study and identify the tunnelling mechanism, gate oxide was deposited with chemical vapour deposition and afterwards annealed in NO, NH₃, N₂ or a combined process of an NO POA followed by a subsequent anneal in NH₃ (NO + NH₃). More details about the process parameters can be found in [10,15]. The N₂ POA here serves as a reference because according to a chemical analysis employing X-ray photoelectron spectroscopy (XPS) [16], this POA does not incorporate nitrogen (N) into the bulk of the oxide, as confirmed by SIMS measurements [17]. Nevertheless, our experiments show that the additional temperature treatment leads to a densification of the oxide compared to an as-deposited oxide.

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2.2. Theoretical calculations

In order to further understand the degradation behaviour of these devices, a set of density functional theory (DFT) calculations has been performed. In our theoretical studies we consider defects in the bulk of amorphous (a)-SiO₂ far from the interface with SiC. Efficient tunnelling from SiC into defects in SiO₂ requires that electrons at the bottom of the SiC conduction band have energies close to defect charge transition levels. The latter are defined as Fermi level where two different charge transition levels. This methodology is discussed in the context of electron tunnelling in devices in Refs. [18,19]. We consider how charge transition levels (CTLs) of common defects in a-SiO₂ films change upon nitridation.

A library of 30 structures each containing 216 atoms representing bulk a-SiO₂ in periodic boundary conditions was created using the molecular dynamics (MD) and a melt-quench technique. These calculations used the Reax force field [20] implemented in the LAMMPS code [21] within a NPT ensemble and a cooling rate of 6 Kps⁻¹. These calculations are described in detail in Ref. [14].

Both the cell vectors and internal coordinates of periodic cells were then optimized using DFT to remove any residual strain. DFT calculations were carried out using the Gaussian Plane Wave method (GPW) [22] implemented in the CP2K code [23,24]. We used the hybrid PBE0-TC-LRC density functional [25] with a 2 Å truncation radius for non-local exchange interaction, 25% of Hartree–Fock exchange and DZVP basis set [25]. The efficient calculation of exchange integrals was facilitated by application of the ADMM approximation [25]. The plane wave cut-off and relative cut-off were set to 600 Ry and 60 Ry, respectively, with a convergence criterion of 1 × 10⁻⁶ eV per formula unit. The models generated by this procedure have densities ranging between 2.100 g cm⁻³ and 2.286 g cm⁻³. Unless stated otherwise, all calculations in this study will use this set of DFT parameters.

Most of the defect calculations were carried out in the bulk of a-SiO₂. To calculate charge transition levels we used the usual procedure for the calculation of defect formation energies [26]:

\[
E_t = E_{\text{def}} - E_{\text{bulk}} - \sum_i n_i \mu_i + q(E_s + \mu_s),
\]

where \(E_{\text{def}}\) is the energy of the defect cell, \(E_{\text{bulk}}\) is the energy of the non-defective cell, \(\mu_i\) is the chemical potential of the species \(s\), \(E_s\) is the energy of the valence band maximum, \(\mu_s\) is the Fermi level position and \(q\) is the defect charge. Here we use the total energy of the bulk in which we place the defect, \(E_{\text{bulk}}\), to calculate the formation energy. However, in the case of nitridation, the agent is added to an already defective network, so the above formulation should be changed to

\[
E_t = E_{\text{N(def)}} - E_{\text{bulk}} - \sum_i n_i \mu_i + q(E_s + \mu_s),
\]

where \(E_{\text{N(def)}}\) is now the total energy of the nitridated defect and \(E_{\text{bulk}}\) is the energy of the original defect cell. Each of the nitridated defects is referenced back to its non-nitridated counterpart. This allows us to calculate a formation energy using initial conditions that accurately relate to the device during anneal. We apply a finite-size electrostatic correction related to the use of periodic boundary conditions [27] to the total energies in calculations in the negative charge state. For the chemical potential we use the total energy of each molecule or fragment in the gas phase at 0 K.

2.3. Tunnelling mechanisms in MOS devices

Typical tunnelling mechanisms in MOS devices are direct and FN tunnelling. Direct tunnelling refers to tunnelling through the full, rectangular shaped barrier from the semiconductor towards the gate material or vice versa and is commonly observed for thin oxides < 5 nm [28]. In oxides thicker than 5 nm, as those used in this study, FN tunnelling is the dominant tunnelling mechanism. There, tunnelling takes place through a triangular shaped barrier from the semiconductor conduction band into the conduction band of the oxide [28]. The resulting current density \(J\) can be described as [28]:

\[
J = \frac{q E_s^2}{16 \pi n^3} \exp \left( -\frac{4 \sqrt{2m^* e q F_{\text{ox}}}}{3 h E_{\text{ox}}} \right)
\]

with the elementary charge \(q\), the oxide electric field \(E_{\text{ox}}\), the tunnelling barrier height \(F_{\text{ox}}\), the reduced Planck constant \(h\) and the effective electron mass \(m^*\) (0.093 times the electron mass [29]). With this relation, the tunnelling barrier can be extracted by fitting of the measurement curves to Eq. (3). Typical barrier heights, which may differ depending on the lattice plane and the existence of trapping effects, reported in literature for 4H-SiC Si-face are 2.7 eV to 2.8 eV [1,30], which matches our barriers (extracted from trench devices) presented in previous studies [10,15].

In addition to the two previously mentioned tunnelling mechanisms, trap assisted leakage paths may also exist. In this case, tunnelling is enabled by trapping and detrapping electrons and holes in oxide
traps which typically starts at lower fields than FN tunnelling. Due to the temperature activation of the underlying charge transfer mechanism [31], TAT exhibits a strong temperature dependence following an Arrhenius law [32,33].

3. Previous observations of trap assisted tunnelling in NH$_3$ annealed devices

As already discussed in earlier publications [10,15], NO, NH$_3$ and the combined process NO + NH$_3$ lead to different gate oxide leakage currents. Fig. 1 shows the gate current characteristics as a function of the gate voltage for differently annealed devices, summarizing the previously published results.

The thick blue curve represents the calculated FN tunnelling current using Eq. (3) and textbook values. As can be seen, NO and NO + NH$_3$ POAs lead to FN tunnelling starting around 5 MV/cm with a tunnelling barrier of 2.7 eV to 2.8 eV [15]. In contrast, NH$_3$ POA leads to an increased gate leakage at low oxide fields in addition to the FN behaviour which was previously identified as TAT [10,15]. For the N$_2$ POA a temperature independent tunnelling current was observed, that could not be clearly assigned to FN tunnelling [15] and was not properly understood at that point.

From the observation that no TAT is detected after any form of NO POA, the intrinsic electron trap [15,14] was suggested as one possible defect that might enable an additional leakage path in NH$_3$ annealed devices. At this time, it was suggested that the NO POA might eliminate this trap level because it is known to eliminate the majority of existing defects [34] whereas NH$_3$ does not. Recent additional studies have revealed that this first hypothesis presented in [15] and summarized above might not be fully correct. In the following sections, we will present a corrected hypothesis explaining the tunnelling and breakdown behaviour resulting after different POAs. We focus on the gate current characteristics resulting after NO, NH$_3$ and N$_2$ POA. In addition to further experimental data, we will link our results to recent theoretical breakdown and tunnelling studies based on DFT calculations.

Below, we first present the results of tunnelling experiments done on the trench MOSFET devices. Preliminary experimental results have already been published in [35]. Next we present the results of DFT calculations comparing the properties of common oxide defects and their nitried counterparts.

4. Experimental results

In this section, the gate leakage current for devices annealed in NO, NH$_3$, N$_2$, and a combined anneal of NO and NH$_3$ are studied. First, the gate oxide leakage of devices which received NO+NH$_3$ POA with different annealing temperatures $T_i$ and times $t_i$ were investigated ($T_1 < T_2 < T_3$ with 700°C < $T$ < 1500°C and $t_1 < t_2$). These results clearly show that, contrary to previous assumptions, the NO+NH$_3$ anneal does not suppress TAT. For annealing temperatures above $T_3$, TAT-like leakage currents can be observed in the resulting devices. The temperature in Fig. 1 is below this threshold temperature so it does not show any TAT. When comparing the resulting leakage current after an NH$_3$ anneal and the combined anneal, with identical annealing parameters for the NH$_3$ containing part of the process, we find that both processes lead to comparable tunnelling behaviours. So, NH$_3$ is the dominating annealing ambient leading to the increased leakage. Thus, a pre-existing trap level causing TAT can be excluded and we also conclude that the underlying defect level is not eliminated by NO POA, as previously suggested in [10,15].

Figs. 4 and 5 show the temperature and time dependence of the leakage currents for NH$_3$ annealed devices. Here, all temperatures studied are equal or larger than $T_3$ (i.e. lie above the temperature that increased tunnelling behaviour is observed in the resulting devices). It can be seen that the leakage current in the TAT regime increases for higher annealing temperatures and longer annealing times. With regard to the annealing temperature, a saturation is observed which can be understood with the dissociation of NH$_3$ during the anneal. The higher the temperature and the longer the annealing time, the more NH$_3$ or its
fragments can react with the interface so that more defects are formed and the leakage current increases.

Since the different POAs lead to a different amount of net oxide charges, the stress was performed for a constant $V_{th}$ overdrive. The reference stress bias for the NO annealed samples was 5 MV/cm and adjusted according to the respective $V_{th}$. The resulting gate current density as a function of the stress time can be found in Fig. 6. Note that no breakdown has been observed in the presented time window because of the low stress bias. Nevertheless, different levels of the leakage current have been observed for the different processes.

As one can see in Fig. 6, the NH$_3$ POA leads to a significantly higher leakage than the other processes. In these devices at these bias conditions, TAT was observed (cf. previous section) leading to the increased currents. The slight decrease of the leakage current over time for all processes can be explained with the blocking of some defects during the tunnelling process through the oxide. With threshold voltage measurements before and after the gate stress it was verified that the observed current decrease cannot be explained with a threshold voltage drift, which supports the above statement. Since this curve can be reproduced after bias removal and re-stressing the devices it seems to be fully reversible (not shown).

In order to investigate breakdown explicitly, the previously mentioned experiment was repeated using a larger stress bias close to breakdown. First, the breakdown voltage was extracted and a suitable stress bias to cause breakdown in reasonable time frames determined for each process variant. The highest effective breakdown field was achieved for NO annealed samples, followed by N$_2$ and NH$_3$. Since the NO annealed samples break the latest or at higher voltages, the stress biases determined for N$_2$ and NH$_3$ POA were transformed into a $V_{th}$ overdrive and the respective effective voltage was determined. Then, the TDDB results were compared to TDDB tests with a comparable effective field (const. $V_{th}$ overdrive) conducted on NO reference samples, respectively.

Figs. 7 and 8 show the probability plots for the TDDB of N$_2$ vs. NO treated oxides and NH$_3$ vs. NO treated oxides. In the latter case, no breakdown could be observed within the measurement time window for the NO annealed samples. In both probability plots, the NO annealed samples break the latest.
5. Theoretical simulations

5.1. Modelling methodology

To elucidate the experimental results above, we consider three defects in a-SiO$_2$, which without nitridation have charge transition levels close to the bottom of the SiC conduction band minimum (CBM) and thus could, in principle, participate in TAT. Since different types of POA have different effects on the TAT current and breakdown voltage, we investigate how the interaction of NO and NH$_3$ products with these defects affects their CTLS. In order to obtain the CTLS w.r.t. the SiC band edges we rely on experimental values for the band offsets at the SiC/SiO$_2$ interface. We focus on three defects: a so-called intrinsic electron trap (IET) [14], oxygen vacancy, and Hydroxyl E’ centre (HE) [36].

IETs originate from structural distortions in a-SiO$_2$ serving as precursors to trapping one or two electrons on one Si atom [14]. Initial calculations suggested that this distortion corresponds to wider than average O–Si–O angles approaching 132° and elongated Si–O bonds [14]. A single electron IET has a CTL at about 2 eV below the a-SiO$_2$ CBM, corresponding to 0.7 eV w.r.t. the SiC CBM. It has been shown that trapping of two electrons at IET weakens Si–O bonds and facilitates the creation of neutral O vacancies and interstitial O$^{2-}$ ions [37]. This defect creation mechanism is thought to be responsible for dielectric breakdown of a-SiO$_2$ films [37].

Out of the two other defects, O vacancy is usually assumed to be present in thermally grown or deposited a-SiO$_2$ films [38] and has 0/-1 CTL at around 1.9 eV below the SiO$_2$ CBM [39]. The Hydroxyl E’ centre was shown to be formed in a-SiO$_2$ films as a result of H atoms reacting with strained Si–O bonds [40]. It has a 0/-1 CTL at about 3 eV below the SiO$_2$ CBM [40]. Hydrogen is ubiquitous in electronic devices due to the mechanisms of film growth and anneal and can diffuse inside a-SiO$_2$ films during POA in ammonia due to dissociation of NH$_3$ into NH$_2$ and H at the surface [41]. Before discussing how the interaction of nitriding species with these defects change their properties and ability to contribute to TAT described above, we briefly outline the modelling methodology.

In the earlier work, IETs have been shown to form at O–Si–O bond angles greater than 132° [14]. However, in the present calculations electron trapping typically occurred already at the narrower 120° O–Si–O bond angles. This difference arises from the fact that full cell optimization of amorphous cells performed here with the hybrid density functional slightly changed their structure comparing to previous studies. The corresponding bond angle distributions can be seen in the supplementary information of Ref. [42]. Out of the 30 cells created for this study, 5 showed electron trapping, giving a similar concentration to the previous results [14]. These 5 sites are the ones that have NO and NH$_3$ added to them.

To study the distribution of properties of O vacancies and HE centres we have chosen two amorphous structures with densities of 2.2 g cm$^{-3}$ and 2.286 g cm$^{-3}$. The second has the highest density of the 30 structures and was chosen to try and emulate a higher density oxide as would be found in the near interface. However, on comparison of CTLS and formation energies, no significant difference was found. We fully sampled each of the 288 oxygen sites, over the 2 cells, creating either a HE centre or a neutral oxygen O vacancy. All structures were relaxed in the neutral and negative charge states to create distributions of CTLS.

Finally, we need to consider which molecular species are likely to penetrate inside a-SiO$_2$ film during anneal. Recently we have demonstrated how NO can diffuse inside the a-SiO$_2$ network [42]. These molecules remain intact and react with defects as discussed below. Baumvol et al. [41] suggested that ammonia is likely to dissociate into NH$_2$ and H at the surface. Our calculations [43] demonstrate that an average barrier for NH$_3$ to penetrate the hydroxilated SiO$_2$ surface is 2.4 eV and that for NH$_2$ is much lower at 1.6 eV. Therefore we assume that NH$_2$ fragments are more likely to interact with defects inside SiO$_2$ films and close to SiO$_2$/SiC interfaces. To model the effects of nitridation, we then consider the interaction of NO and NH$_2$ with IETs and NO with the O vacancy and HE centre.

5.2. Results of calculations

5.2.1. Intrinsic electron trap

In this section, we detail what happens to the CTL and geometry of IET when we coordinate NO and NH$_2$ to the Si of the wide O–Si–O bond angle. NH$_2$ was not considered due to steric reasons as it is too large to fit in the gap given by the wide O–Si–O angle, and the formation of NH is thought to be energetically too costly during the SiO$_2$ anneal [41].

NO interacts spontaneously with the negatively charged IET with the N atom docking towards the four-coordinated Si atom holding the extra electron (see Fig. 9 b). The extra electron in this configuration is preferentially transferred on NO rather than Si. NH$_2$ is also coordinated by N towards the extra electron (see Fig. 9 c). In both cases, the electron trapping 0/-1 level moves down towards the valence band of a-SiO$_2$ sitting 2.5 eV above the a-SiO$_2$ valence band (Fig. 9 a). This means that the level is moved far away from the conduction band of both Si and SiC, hence reducing the probability of electrons tunnelling through this defect and causing TAT.

The IET can trap a second electron and this has been shown to be the first step in a mechanism for oxide breakdown [37]. This mechanism relies on two localized electrons causing repulsive interaction and a Si–O bond weakening. When a second electron traps at the wide bond angle site, there is a large increase in the Si–O bond lengths, the longer of the two going from 1.75 Å to 2.42 Å, facilitating the creation of O vacancy and interstitial O$^{2-}$ ion [44]. When one of the nitriding species is coordinated to this site, the longer bond length decreases from an average of 2.42 Å to 1.88 Å due to the electron redistribution to a molecule. A shorter bond points to the network being stronger at these bi-electron trap sites meaning that these annealing procedures also make the gate oxide less susceptible to the formation of O vacancies during operation.[44]
5.2.2. O vacancy

The 0/-1 CTLs of O vacancy in a-SiO$_2$ have a range of values from 5.7 eV to 7.75 eV above the valence band of a-SiO$_2$ (Fig. 10). With respect to the SiC/SiO$_2$ conduction band offset, the modal peak of this distribution sits 1 eV above the SiC conduction band (Fig. 10), which makes these states amenable to electron transfer under bias.

The NO molecule can incorporate into the O vacancy either by its O or N atom. The calculations demonstrate that N atom coordinating with the dangling Si atoms of the O vacancy is the lowest energy configuration by an average 0.5 eV. When the NO molecule is added to the vacancy, the modal peak of the 0/-1 level moves from 6.75 eV to 4.5 eV above the VBM, ranging from 3 eV to 6 eV, above the a-SiO$_2$ VBM (see Fig. 10 a). This means that the nitridated levels sit much deeper in the band gap of the system compared to the original defect. This again points to there being a decrease in probability of electrons tunnelling through these defects.

5.2.3. Hydroxyl E' centre

As mentioned previously, this defect has to be considered because atomic H or H containing molecules (H$_2$, H$_2$O etc.) are ubiquitous during film growth, anneal and device operation and have been shown to create new defects [40]. The experimental results above, in particular Figs. 1–3, show that when anneals in NH$_3$ are performed there is an increased gate leakage current with respect to the NO annealed device. This can result from the dissociation of NH$_3$ into NH$_2$ and H at the surface during anneal [41] and H penetration into the SiO$_2$ film. As shown in Fig. 11, the HE centre has a 0/-1 level close to the CBM of SiC and is one of the prime candidates for TAT in these devices.

Since HE centres can result from ammonia anneal, here we consider only NO passivation of HE centre. In the neutral state, an unpaired electron of HE centre is localized on the three-coordinated Si atom of the broken Si–O bond, and in the negative state, the second electron is localized on the same Si atom. NO molecule docks to this Si atom by its N atom (see Fig. 11 b) sharing extra electrons with Si. As shown in Fig. 11 a, the 0/-1 level of the defect moves deeper into the band gap when NO is coordinated to it. However, the shift is not as drastic as the one for the O vacancy, with the modal peak moving from around 6 eV to 5 eV above the a-SiO$_2$ VBM, or iso-electronic with the CB of SiC to 1 eV below it. There is also a significant overlap of the two distributions (purple section of Fig. 11 a) with some of the NO coordinated levels located above the CB of SiC. When the interaction of the NO molecule with the O vacancy is compared to that with the HE centre, it shows that the latter only makes one bond with the NO molecule and so the interaction is weaker hence leading to the energy of the NO coordinated variant of the HE centres to be higher across the band gap of the device, hence shifting its CTL towards the CB. Hence, compared to the nitridated O vacancy, the nitridated HE centre more readily accepts electrons and so can still play a part in TAT processes.

6. Discussion and conclusions

We have presented a set of theoretical and experimental results from differently annealed SiC/a-SiO$_2$ devices. In this section both sets of results will be discussed together, linking the electrical measurements with the theoretical atomistic picture.

Trap assisted tunneling and oxide breakdown in differently processed 4H-SiC trench MOSFETs have been investigated along with
theoretical calculations of common oxide defects with and without NO coordination. It has been shown that an NH₃ anneal above a certain threshold temperature leads to the formation of new defect levels in the oxide which open additional leakage paths compared to oxides which were annealed in NO or N₂. One possible trap candidate to explain the observations is the Hydroxyl E’ centre. In contrast, in NO and N₂ annealed MOSFETs only FN tunnelling is observed. N₂ POA, however, leads to a reduced tunnelling barrier due to trap states close to the SiO₂ conduction band edge.

In electrical measurements of NO annealed devices, the gate current density is much lower than for N₂ annealed devices. Theoretically found CTLs of oxide defects show that the coordination to NO moves the defect level deeper into the band gap of SiC and a-SiO₂ thus decreasing tunnelling probability to nitridated defects, as the system would have to dissipate around 2 eV of energy to allow for tunnelling to occur. Therefore, we conclude the action of the NO anneal is to block potential electron trapping sites in a-SiO₂.

The IET is an important defect which has been shown to contribute to trap assisted tunnelling in devices that use a-SiO₂ as the gate oxide as well as facilitate the formation of O vacancies contributing to oxide degradation [37,44]. The 0/-1 CTL for the IET sits 1 eV above the CB of SiC and so it is a facile process for electrons to tunnel to it under bias. On nitridation, the trap level moves much deeper into the band gap of the system meaning that the probability of tunnelling to it decreases. This is shown in the electrical measurements of NO annealed devices, which have a much lower gate current density than the N₂ annealed devices, in which one assumes the IET is not passivated.

In NH₃ annealed devices, there is higher gate current density than for N₂ annealed devices. It has been suggested that this is due to the formation of defects in the oxide [41,45]. Devices with longer annealing times and higher temperatures have higher gate current densities than those with lower temperatures and times. This, coupled with the increased TAT behaviour for the NO + NH₃ combined anneal, shows that there is some formation of defects during this anneal. Our results suggest that formation of Hydroxyl E’ centres as a result of reactions of atomic H originating from NH₃ dissociation could be one of the reasons for this behaviour.

Furthermore, this study provides an insight into the breakdown behaviour of our devices demonstrating that the NO annealed devices require the highest breakdown field. The previous calculations suggest that the oxide degradation and breakdown are facilitated by trapping of two electrons at an already stretched Si–O–Si bond, enhancing bond breakage and by this the formation of new oxygen vacancies, which in turn can again act as new precursor sites [37,44]. The results of calculations presented here show that NO POA can at least partly relax these bonds and thereby reduce the number of precursors for oxide leakage paths and finally the oxide breakdown. On the other hand, the introduction of hydrogen either via the ammonia anneal or through processing can introduce new HE centres which are not fully passivated by NO. Therefore, the NO POA currently still seems to be the most efficient in order to obtain MOSFETs with reliable oxides.

CRediT authorship contribution statement

Judith Berens: Conceptualization, Investigation, Writing, Review. Manesh V. Mistry: Conceptualization, Formal analysis, Writing, Review. Dominic Walldhörl: Formal analysis, Review. Alexander Shluger: Project administration, Supervision, Resources, Conceptualization, Funding acquisition, Writing, Review. Gregor Pobegen: Project administration, Supervision, Resources, Conceptualization, Funding acquisition, Review. Tibor Grasser: Project administration, Supervision, Resources, Conceptualization, Funding acquisition, Review.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Fig. 11. Distribution of CTLs for the Hydroxyl E’-centre (blue) and its variant with NO coordinated to the dangling Si bond (a). The purple denotes the overlap between the nitridated and un-nitridated variants. (b) shows the geometry of an NO molecule coordinated with the hydroxyl E’-centre.
References