Emulation of a Multi-Stage Differential Amplifier Using one Single-Ended Device-Under-Test

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Abstract—A method to emulate multi-stage power amplifier (PA) architectures is presented. The technique predicts multi-stage PA performance. The method is based on an iterative procedure using transistor/branch PA active load-pull measurements to include inter-stage interaction. As a benefit, real-world performance of a multi-stage PA can be evaluated early in the design process. Compared to previous published work, the method requires only a single representative device-under-test to embody multi-stage architectures. Thus, a compelling measurement method for PA designers is presented. The method is demonstrated by emulating a two-stage differential amplifier at 2.14 GHz using single-tone signals.

Index Terms—Active load–pull, power amplifier, differential, emulation, measurement technique, inter-stage, multi-stage.

I. INTRODUCTION

Power amplifiers (PAs) with the best possible performance are required for future wireless communication systems. As such, the ability to accurately predict the performance of a PA in the design process becomes increasingly important. The best of such predictions often utilize load-pull measurements. Unfortunately, in general, conventional load-pull techniques cannot accurately predict the performance of multi-stage differential PA architectures. Conventional load-pull fails to capture the non-linear interaction between the transistors, in particular, the interaction via the inter-stage matching network, which may include coupling between multiple branches. Furthermore, any imperfections, such as imbalances in phase and amplitude and/or common-mode signals may exist during the actual operation of the PA. These imperfections may be affected by non-linear interactions between the transistors. It is therefore of crucial importance to capture such effects through measurements during the design process of the PA to accurately predict its performance.

Although bipolar differential (push-pull) PA stages have been explored for quite some years [1]–[5], they are only lately starting to appear in handsets [6], [7], especially with the migration to 5G. The advantages of such a differential architecture are higher impedance (for higher bandwidth), the neutralization of Cbc (stability), better isolation (less variation with input power), and high stable gain [1], [2]. This
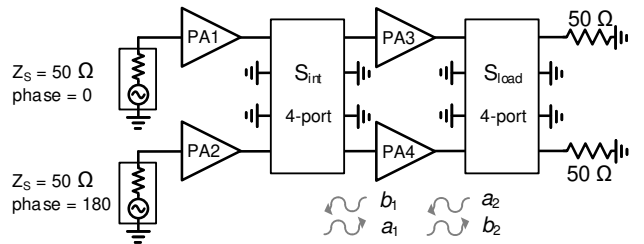

Fig. 1. Generic operation of a two-stage differential PA using four PAs and inter-stage and load networks, both are represented by 4-port S-parameter networks S_{int} and S_{load}.

architecture also allows better optimization of non-linearities, which is particularly important when operating in class-F or inverse class-F to maximize PA efficiency [4].

For technology development, load-pulling of simple single stage arrays of unit-cells [8] is a key tool for assessing device performance. While active mixed-mode load-pull is possible [3], it is more appropriate closer to the circuit level. A technique that can use device performance data to understand the performance in circuit applications allows for better technology trade-offs to be made.

A suitable load-pull measurement-based emulation method that accurately predicts the real-world performance of multi-transistor architectures was recently proposed. The technique was originally developed to analyze coupling effects between PAs in antenna arrays [9]. Subsequently, the technique was exemplified by emulating Doherty [10], outphasing [11], and differential [12] PAs. The emulation technique has been experimentally validated by comparing emulation measurement results to a realized antenna array [9] and a realized Doherty PA [10]. Building upon these results, this work, for the first time, presents the emulation of the inter-stage network of multi-stage PAs.

In this work, we propose an emulation method to find and characterize the behavior of multi-stage differential PAs. The procedure described in this paper utilizes branch amplifier measurements and S-parameters of the load and inter-stage networks. We experimentally demonstrate the method's capa-
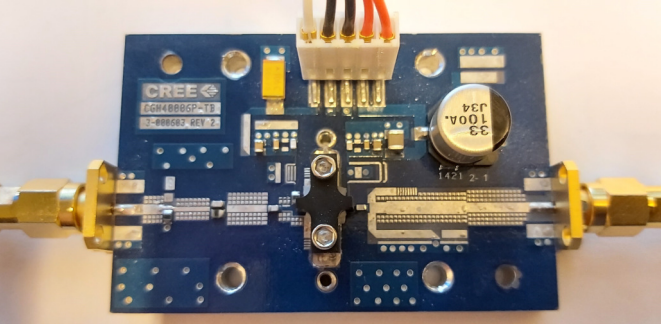
Fig. 2. CGH40006P-TB testboard applied as DUT during the experiments.

bilities by emulating a multi-stage differential PA for several bias points pairs, where the first driver stage is operated from class-C to class-B, and the end stage is operated mostly around class-B. Normally hidden performance characteristics, such as the individual driver gain, inter-stage power levels and load impedances, are revealed directly through this approach.

II. METHOD

The iterative procedure employed to perform mixed-mode active load-pull and emulation of differential PAs is explained in [10] and [12] and is shortly repeated here. The setup shown in Fig. 1 is considered. The starting point is the well-known formulation [13] of 2-port mixed-mode S-parameters $\boldsymbol{S_{mm}}$ and its standard 4-port S-parameter equivalent $\boldsymbol{S}$. From Fig. 1, the waves around the device-under-test (DUT) are defined: a_1 and b_1 at the input and a_2 and b_2 at the output. The differential waves of the mixed-mode formulation can be calculated after emulation [12], where the subscript d indicates differential mode, and $driver$ and end denote the two differential stages. The input and the differential-mode power delivered to the input and the load, respectively, are given by:

$$P_{del,d} = \frac{|b_{d2}|^2}{2Z_0} - \frac{|a_{d2}|^2}{2Z_0}, P_{in,d} = \frac{|b_{d1}|^2}{2Z_0} - \frac{|a_{d1}|^2}{2Z_0}. \quad (1)$$

The differential reflection coefficients for the driver and end stage are given by:

$$\Gamma_{load,d,driver}(f) = \frac{a_{d2,driver}(f)}{b_{d2,driver}(f)}, \quad (2)$$

$$\Gamma_{in,d,driver}(f) = \frac{b_{d1,driver}(f)}{a_{d1,driver}(f)}, \quad (3)$$

$$\Gamma_{load,d,end}(f) = \frac{a_{d2,end}(f)}{b_{d2,end}(f)}, \quad (4)$$

$$\Gamma_{in,d,end}(f) = \frac{b_{d1,end}(f)}{a_{d1,end}(f)}, \quad (5)$$

where f is the frequency.

The iterative procedure employed to emulate a single differential stage, where the DUT alternates between acting as the two branch PAs, is explained in [12]. Here, we perform this iterative method to emulate the load network of the end stage $\boldsymbol{S_{load}}$. Moreover, we used similar steps to emulate the inter-stage matching network $\boldsymbol{S_{int}}$ between the driver and end stage. Therefore, the specifics of the emulation of the inter-stage matching network is discussed briefly below.
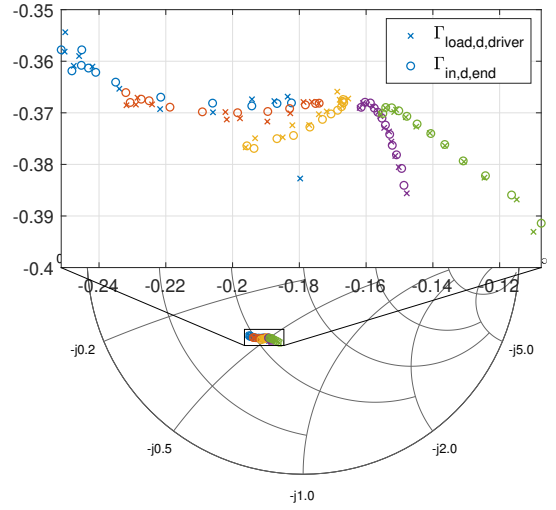

Fig. 3. Comparison between measured emulated $\Gamma_{load,d,driver}$ (x) to $\Gamma_{in,d,end}$ (o) for power sweeps for five bias pairs: Vg (driver, end).
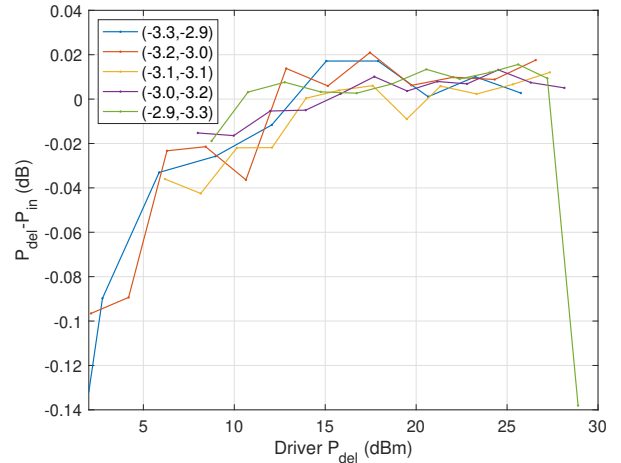

Fig. 4. Error in dB between measured $P_{deld,driver}$ and $P_{ind,end}$ for power sweeps for five bias pairs: Vg (driver, end).

From the 4-port S-parameter formulation for the intermediate stage, the resulting and incoming waves a_i and b_j for each amplifier, are calculated as follows:

$$a_i(f) = \sum_{j=1}^{4} S_{ij}(f) b_j(f), \quad (6)$$

where we followed the standard convention for the waves for S-parameters and i and j are the port numbers. These can be related to the waves of the individual devices/amplifiers for the driver differential stage:

$$PA1, b_2(f) = a_1(f), \quad PA1, a_2(f) = b_1(f), \quad (7)$$
$$PA2, b_2(f) = a_2(f), \quad PA2, a_2(f) = b_2(f). \quad (8)$$

And for the differential end stage as:

$$PA3, b_1(f) = a_3(f), \quad PA3, a_1(f) = b_3(f), \quad (9)$$
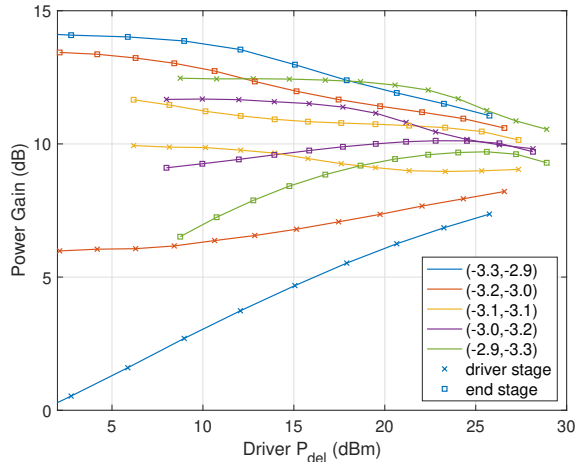$$PA4, b_1(f) = a_4(f), \quad PA4, a_1(f) = b_4(f). \quad (10)$$

Fig. 5. Measured individual stage power gain in dB for both the driver (x) and end (□) stage, for power sweeps for five bias pairs: Vg (driver, end).
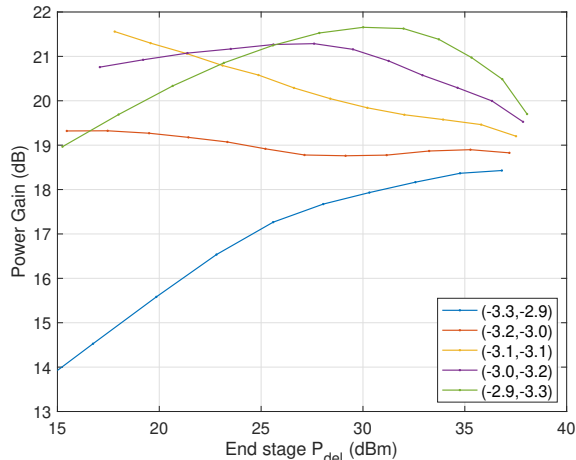

Fig. 6. Measured power gain of the complete amplifier in dB for power sweeps for five bias pairs: Vg (driver, end).

When these waves are known, the waves that will load the driver differential stage and the input waves to the differential end stage can be calculated using (6) and injected towards the DUT. This is subsequently repeated in an iterative fashion [10]. Once the full iteration procedure is completed, the waves at the inter-stage and end-stage output fulfil the target S_{int} and S_{load} matrix equations, all resulting waves are saved. Then, as an example, power, efficiency, and all reflection coefficients, including differential reflection coefficients for the full two-stage differential amplifier can be calculated.

III. EXPERIMENTS

A 6-W GaN HEMT CGH40006P packaged transistor from Wolfspeed is used as the active device representing all branch amplifiers. The drain supply voltage is set to 20 V. The branch PA testboard in Fig. 2 includes bias networks and supply feeds, stabilisation, fundamental input and output matching networks, and input and output second harmonic terminations. All measurements are performed using RF WebLab[1]. Har-

[1]www.dpdcompetition.com/rfweblab

monic components are not emulated, but are controlled by the harmonic termination on the testboard.

The experiments performed are single tone power-sweeps at 2.14 GHz for a set of gate bias pair, which vary the bias point of the driver from high class-C to around class-B. The end stage is kept around class-B. The gate bias pairs are the following: Vg (driver, end) = (-2.9, -3.3) (-3.0, -3.2) (-3.1, .3.1) (-3.2, -3.0) (-3.3, -2.9).

The emulated load of the end stage is 100 Ω. The emulated inter-stage network is given by $S_{dd11} = S_{dd22} = 0$ and $S_{dd12} = S_{dd21} = 1$, which represents a direct connection between the two stages. As such, for fundamental single tone only, the resulting emulation procedure can be verified by comparing the inter-stage reflections $\Gamma_{load,d,driver}$ to $\Gamma_{in,d,end}$ and by comparing the inter-stage power levels $P_{del,d,driver}$ to $P_{in,d,end}$, where both need to be identical.

Fig. 3 shows good agreement between the resulting differential input impedance of the end stage and the load impedance of the driver stage. Some points show some deviation, however due to the scale of the zoomed inset, the resulting load impedances of the driver stage are still very close to the measured input impedances of the end stage. One outlier, blue 'x', is shown in Fig. 3, which corresponds to a low driver output power level, below 0 dBm. Moreover, in Fig. 4 the differential output power of the driver stage is compared with the input power of the end stage. Some deviation, up to 0.1 dB can be observed, mostly for the lower input power levels. Nonetheless, over a large range of about 20 dB, excellent agreement is shown. As such, these results verify the proposed emulation measurement method.

The emulation method allows access to quantities, which are normally hidden inside the complete amplifier. For example, the individual differential power gain of the stages can be studied. Fig. 5 shows the power gain of the driver and end stage, respectively, plotted versus the driver output power, since this is also the input power of the end stage. The impact of changing the gate bias shows that the driver stage can be modified from expanding at lower gate voltages to compressing at higher gate voltages. Similar behavior but with a more restricted range is visible for the end stage. By letting the driver stage expand and the end stage compress, a flatter total amplifier gain, and thus lower AM-AM is possible, as shown in Fig. 6. This is clearly illustrated by the red curve corresponding to Vg (-3.2,-3.0).

A similar analysis can be made of the individual AM-PM curves, as given in Fig. 7. However, for this amplifier at these bias pairs, the AM-PM curves have similar input power dependence. As such the total AM-PM curve of Fig. 8 has not flattened. Nonetheless, a combination of bias settings and inter-stage mismatch can be exploited to flatten both the AM-AM and AM-PM behavior [14], [15]; something that can be easily investigated already at the design stage with the presented emulation measurement method.

The capability of the method is also illustrated by the results given in Fig. 3. The changes in the load or input impedance versus power indicate that a non-linear interaction between the
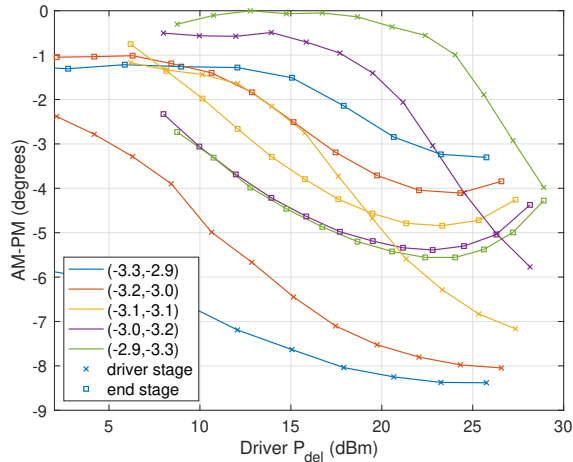
Fig. 7. Measured individual stage AM-PM in degrees for both the driver (x) and end (□) stage, for power sweeps for five bias pairs: Vg (driver, end).
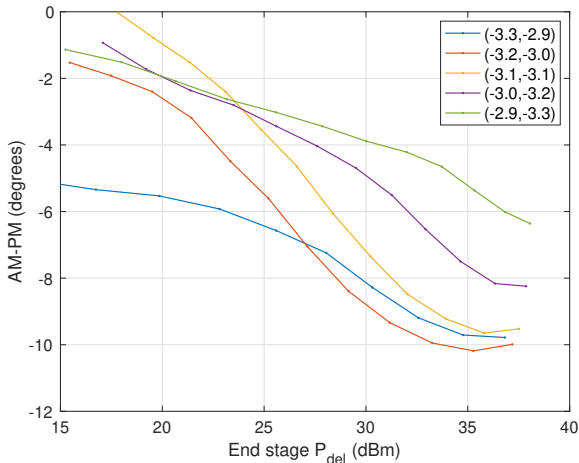

Fig. 8. Measured AM-PM for the complete amplifier in degrees, for power sweeps for five bias pairs: Vg (driver, end).

two stages needs to be taken into account to properly study linearity and distortion of the whole differential amplifier. Also note that for the fundamental single-tone ideal case as presented herein, with a direct connection between stages with no unbalances or cross-talk, the impact can be studied using conventional active and passive load-pull. However, when extending to modulated signals, only the presented active load-pull method will take this non-linear interaction correctly into account, since the waves not only represent current flowing into the device/PA, but also current that is emitted by the device/PA at inter-modulation and harmonic frequencies.

IV. Conclusion

It has been demonstrated that the emulation technique works for multi-stage differential power amplifiers. Its potential impact has been shown by emulating a multi-stage differential amplifier. The presented measurement technique enables early prediction of real-world performance while providing measurement-based understanding. Thus, advancing power amplifiers performance enabling future wireless systems.

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