Gate-based sensing of silicon quantum dot devices towards 2D scaling

by

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Declaration

I, Jingyu Duan, confirm that the work presented in this thesis is my own. The contents of this thesis are original and have not been submitted in whole or in part for any other degree in any university. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

Jingyu Duan

June 2022

Abstract

This thesis focuses on using the radio-frequency reflectometry technique for dispersive gate sensing of foundry fabricated silicon nanowire quantum dot devices. I will attempt to answer three questions relating to the scalability of these devices. How do electron and hole spin qubits perform in silicon quantum dots? How do we implement and distribute the placement of dispersive gate sensors in scaled-up quantum dot arrays? And how does a single dopant in the silicon channel affect the gate-defined quantum dot?

First, I investigate the difference between electron and hole quantum dots in an ambipolar nanowire device which successfully demonstrated reconfigurable single and double electron and hole quantum dots in the same crystalline environment. I further investigate the effective bath temperature of two-dimensional electron gas and two-dimensional hole gas by performing the thermometry experiment on the same type of device. Secondly, I demonstrate a two-dimensional quantum dot array enabled by a floating gate architecture between silicon nanowires. An analytical model is developed to study the capacitive coupling between remote quantum dots over different distances. Coupling strength under different qubit encodings is also discussed to show the best implementation for neighbour silicon nanowires. Finally, the in-situ dispersive gate sensing allows the measurement of the inter-dot transition between the bismuth donor-dot system. The novel implementation with bismuth donor can open up the possibility of a hybrid singlet-triplet qubit or transferring a coherent spin state between the quantum dot and the donor.

Impact statement

With the large computational spaces, fault-tolerant quantum computers can solve complex problems in academia and industry and have a significant impact on many fields of modern society. For instance, a quantum computer can simulate large molecules which helps researchers find novel materials, enzymes and new drugs. Quantum speed-up in optimization problems can help logistics and finance greatly. Quantum speed-up in artificial intelligence can help the processing of vast amounts of data for machine learning

The results in this thesis bring a few implementations of quantum dots based on CMOS technology and show one step closer to large scale quantum computer by demonstrating a scalable quantum dot bilinear array with a gate-based sensing technique. However, it might take a few decades or even longer for a useful silicon-based fault-tolerant quantum computer to be built.

The gate-based sensor demonstrated in this thesis has already been used as the thermometer for cryogenic temperature. Moreover, the highly-sensitive sensor in silicon also opens up research on fundamental theory for carrier-phonon coupling, and charge noise characterization. Finally, the high nuclear spin donor-dot system studied in this thesis also opens up research on quantum chaos study with a large Hilbert space.

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Publications and Conferences

Publications

- Duan, J., Lehtinen, J. S., Fogarty, M. A., Schaal, S., Lam, M. M. L., Ronzani, A., Shchepetov, A., Koppinen, P., Prunnila, M., Gonzalez-Zalba, F., & Morton, J. J. L. (2021). *Dispersive readout of reconfigurable ambipolar quantum dots in a silicon-on-insulator nanowire.* Applied Physics Letters, 118(16), 164002. https://doi.org/10.1063/5.0040259

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Chapter 1

Introduction

Since the latter half of the 20th century, the third industrial revolution has changed the world fundamentally, lifting the world's production efficiency to an unprecedented level. Two driving forces behind this fundamental change are the mass production of integrated chips (IC) and the constant scaling of the semiconductor-based transistors. In 1971, the first commercial IC chip - Intel 4004 contained 2,300 transistors [1, 2]. As of 2021, the latest Apple M1 chip can contain 30 billion transistors in roughly the same physical area. For several decades, the scaling of transistors with complementary metal-oxide-semiconductor (CMOS) process has followed the famously known Moore's law. Stressing the importance of integrated circuits and calling for more investment in advancing the integration complexity in the semiconductor industry, Gordon Moore, the co-founder of Intel, once suggested that the transistors in each integrated chip should double every 12 to 24 months. [3, 4]. However, since 2005, the pace of this scaling has slowed down as semiconductor manufacturing technology is reaching its physical limit. There is no more 'free' room at the bottom[1]. As the material thickness of the transistor reaches sub-10nm, at which leakage current due to direct quantum tunnelling becomes non-negligible, the switching speed and power consumption of the transistor become the bottleneck of this trend [5]. Meanwhile, a certain class of tasks grows exponentially difficult for classical computers' polynomial-time efficiency. It is estimated that global data centres likely consumed 205 terawatts-hour (TWh) in

[1]Feynman's talk 'Plenty of room at the bottom' is considered the birth of nanotechnology.

2018, equivalent to 1 percent of global electricity use. The power usage effectiveness of such data centres is dropping over time [6]. Many are asking, "what is next after the end of Moore's law?" [7]. Will the computation power be enough for the ever-growing information service? There are many answers for 'beyond CMOS' [8]. Quantum computing is one of the most promising alternatives that can substantially impact society. In many applications such as optimisation, a quantum computer offers the potential to save both energy consumption and execution time dramatically [9]. The potential application of quantum simulation will benefit the research development of big molecules such as pharmaceutical medicine or enzymes for industrial processes.

1.1 Quantum Computing and the Qubit

This year marks the 40th anniversary of quantum computing since the issue of *International Journal of Theoretical Physics* where the leading physicists and computer scientists discussed the 'Physics of Computation' [10]. In 1980, Paul Benioff introduced a quantum version of the Turing machine [11]. In 1981 Richard Feynman pointed out the limit of classical computers in simulating nature. He brought up the idea of the quantum computer, in which people could use such engineered quantum systems to simulate nature [12]. In the 1990s, Lov Grover and Peter Shor separately came up with the two seminal works on quantum algorithms demonstrating quantum speedup over the classical algorithm. Grover's search algorithm [13] could find a specific item in a randomly ordered data group, and Shor's factoring algorithm [14] could factorise an integer number much more effective than a classical computer. Controlling the evolution of quantum states has become a tool to help scientists investigate the quantum many-body problem. The variational quantum eigensolver algorithm is useful in computing the ground state energy of a Hamiltonian, which is central to quantum chemistry [15]. Other quantum algorithms like Harrow/Hassidim/Lloyd [16] method for linear systems open up the research into quantum machine learning.

Significantly reduced computation complexity by quantum computers can not

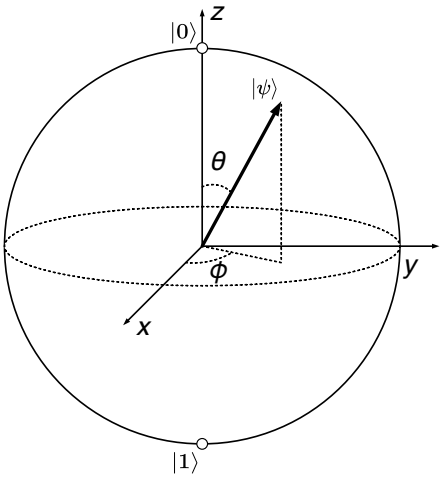


Figure 1.1 A qubit state $|\psi\rangle$ illustrated by Bloch sphere.

be achieved easily. It requires millions of interconnected functional quantum bits - known as the Qubit. A Qubit is analogous to the 'bit' encountered in classical computers. It is essentially a linear combination of quantum two-level system (TLS) with the properties of superposition and entanglement and can utilise such fundamental phenomena for information processing. The spin state of an electron in a finite magnetic field is a TLS formed by spin-up state $|0\rangle$ and spin-down state $|1\rangle$. Unlike the classical bit, which represents two discrete levels, a qubit can represent all probabilistic superpositions of the two levels written as the Equation 1.1. In this equation, θ and ϕ describe the spherical coordinates of a quantum state visualised in a so-called Bloch sphere with the two poles being $|0\rangle$ and $|1\rangle$ Figure 1.1. The pure state corresponds to a point on the surface of the Bloch sphere.

$$|\psi\rangle = \cos\frac{\theta}{2}|0\rangle + \mathrm{e}^{\mathrm{i}\phi}\sin\frac{\theta}{2}|1\rangle \tag{1.1}$$

Superposition expands the computing resource exponentially. The superposition of the n-qubit state can create a 2^n dimensional Hilbert space. It is possible to create entanglement between two or more qubits and make them evolve as a whole. Manipulations of qubits, such as rotation along a particular axis, can affect the probability distribution of all entangled quantum states. Performing logic gates with the inherent parallelism is one of the great powers of quantum computing.

1.2 Quantum Computing platforms

Along with the theoretical development of quantum computing, the experimental effort also started to shine in the 1990s. Molecular nuclei in the liquid state have demonstrated the quantum algorithm with nuclear magnetic resonance techniques [17, 18]. And soon, superconducting qubits followed with groundbreaking quantum control experiments [19]. David P. DiVincenzo summarised the conditions for constructing a quantum computer in 2000 [20]. DiVincenzo criteria provide an overview and guideline for this field despite different developed routes towards realising quantum computing. Such criteria are as follows:

A scalable physical system with well-characterised qubit: A qubit should be well-characterised with accurate physical parameters and a well-understood Hamiltonian. The energy of the qubit and its interaction with the environment, including other qubits, are fully described in the Hamiltonian. Insufficient or incorrect physical description in the Hamiltonian can cause errors in qubit manipulation. A scalable physical system requires a collection of interconnected qubits, and its interface apparatus scale together.

The ability to initialise the state of the qubits: The register must be initialised to a simple fiducial state before the computation. It is also desirable to have a supply of known states as the ancilla qubit for checking errors in quantum error correction. Usually, the ground state can be initialised from cooling or after T_1 relaxation time. The more generic way of initialisation is projecting the known states via measurement.

Long relevant decoherence times: Quantum states become classical after decoherence time which is the characteristic time for the qubit to maintain its superposition and entanglement. Decoherence time is affected by the interaction with its environment and neighbouring qubits. Without further quantum error correction, it is required that all the quantum computations should be performed within the decoherence time. The circuit depth is also

used to characterise a quantum computer. It reflects the hardware system's practical limit, which is bounded by the relative ratio between decoherence and quantum gate times.

A universal set of quantum gates: In classical computing, it is possible to create any set of logic gates with just NOR gate or NAND gate. Either of them is the universal logic gate of classical computing. Using universal logic gate can make the underline physical implementation more straightforward. Complex computation can be efficiently deducted into the simplest combination of the universal gate. Similarly, it is advantageous to map a suitable sequence of unitary transformations to a generic quantum algorithm. Solovay-Kitaev Theorem [21, 22] shows that it is possible to have a set of quantum gates to simulate other arbitrary gates with efficient approximation.

A qubit-specific measurement capability: After a quantum computation, each qubit state is read out accurately. Often, a quantum non-demolition readout is preferred. The qubit state is still collapsed to a specific state after measurement but is continuously available for the initialisation of a new task. Moreover, measurement capability needs to scale together with the qubit number. When measurement time is shorter than decoherence, it allows for more efficient quantum error correction without much overhead.

Divincenzo has added two criteria specific for quantum communication: **the ability to interconvert stationary and flying qubits** and **the ability to faithfully transmit flying qubits between specified locations**. Even though these seven criteria are extremely challenging and some require large engineering effort, these following experimental platforms successfully demonstrate all the basic elements of Divincenzo's criteria: nuclear magnetic resonance (NMR) [23], superconducting circuits [24, 25], ion-trap [26, 27], photon [28, 29], NV-centres in diamond [30], and semiconductor quantum dot (QD) [31–33]. With the effort from academics and industry, superconducting circuits and ion-traps become the most promising candidates to deliver quantum advantage in a noisy intermediate-scale quantum (NISQ) era [25, 27]. To achieve

fault-tolerant quantum computing for practical quantum speed up, it requires an enormous number of physical qubits (10^8) with a low error rate (99%) and long coherence time (>1 µs) to support logical quantum algorithm [34]. There still seem to be many challenges ahead—the quantity and quality of the qubit both matter in the long run. The relatively short decoherence time will lead to a shallow circuit depth, thus having a small quantum volume [35]. Meanwhile, as the number of qubits grows, the number of accompanied control electronics grows simultaneously. Moreover, cross-talk and overcrowding of signals lead to further decoherence [36]. Silicon spin qubit has recently engaged many academic researchers and industrial players like Intel and Imec [37, 38]. Silicon QD as the host hass relative long qubit coherence time [39], small footprint [36] and compatibility with CMOS process in scaling up the whole system [37, 40].

1.3 Rise of silicon and its challenge

The pioneering experiments of the spin qubit are demonstrated on III-V heterostructure semiconductor QD, including the spin initialisation and readout [31, 32], quantum control with exchange coupling [41]. However, III-V host material imposes strong decoherence on the spin qubit with 'non-zero' nuclear spin bath. This limits the spin qubit's coherence time T_2^* to less than 100 ns [42]. Silicon gains more interest as the natural silicon contains 95% of spin-zero nuclei isotope, and only 5% of ^{29}Si has a nuclear spin $I = 1/2$ [43]. This advantage is exploited by isotopic enrichment of the nuclei element ^{28}Si in the host material [44] to achieve a near-perfect 'spin vacuum' environment. To further understand silicon as the host of a qubit, other properties of silicon QD, including valley states [45, 46], orbital states [47], and noise spectra [48, 49], are also investigated. Recent progress of precise pulse engineering with careful consideration of qubit Hamiltonian has enabled two-qubit gate fidelity to reach above 99% crossing the surface code error correction [50–52]. The capability to operate at above 1 K puts spin qubit in a more economical position than other solid-state qubit platforms for the relaxed requirement of cooling budget [53–55].

At the same time, the control of electron spin qubit uses two methods:

electron spin resonance (ESR) with transmission line [33, 56] and electric dipole spin resonance (EDSR) with the help of micro-magnet [57, 58]. Both methods add up the fabrication complexity in scaling up the system, therefore all-electrical control of spin qubits is preferred to achieve faster and more scalable control. Hole spin qubit has stayed quiet in the first decade of the century but soon gained rapid progress in recent years owing to material stack and quantum control technique improvement. Subject to the strong spin-orbit interaction, hole qubit has achieved fast all-electrical two-axis control despite the drawback of sub-microseconds coherence time [59, 60]. Electron or Hole spin qubit? There are many discussion on which one is suitable for the large-scale quantum computer. Also, a scalable architecture is yet to be developed and demonstrated comparable results since all the key experiments aforementioned are demonstrated in few QDs devices.

1.4 This thesis

As introduced before, this thesis aims to address three questions relating to the scalability of foundry fabricated silicon quantum dot devices. **1. How do electron and hole spin qubits perform in silicon quantum dots? 2. How to implement and distribute the placement of dispersive gate sensors in scaled-up quantum dot arrays?** and **3. how does a single dopant in the silicon channel affect the gate-defined quantum dot?**

I use a recently-developed gate-based readout technique with a low-loss NbTi superconducting inductor [61, 62]. Firstly, I study the charge dynamics of the single and double quantum dots in the ambipolar silicon device fabricated at VTT. Secondly, a nanowire quantum dot device fabricated at CEA-LETI enabling measuring and coupling quantum dots in a two-dimensional scalable way is presented. Finally, I use the gate-based sensor to probe the spin dynamics of the silicon double quantum dot system formed by a bismuth dopant and a gate-defined quantum dot.

This thesis consists of eight Chapters. The first three Chapters of the thesis provide the necessary background on the current research in quantum computing

with silicon quantum dots, essential details of the project and the background theory of spin qubit and experimental details.

Chapter 2 outlines the silicon quantum dot theory for both electron and hole in the context of the DiVincenzo criteria. It also describes the background theory for dispersive readout of the quantum dot to reservoir and inter-dot signal.

Chapter 3 introduces the experimental details for the project. It first describes the fabrication of the different devices used in the project, ambipolar quantum dot device from VTT and scalable silicon nanowire device from CEA-LETI. The measurement setup includes cooling equipment for the necessary cold environment (mK), the electrical circuit for microwave and DC routing, PCB for holding chip and instruments for signal generation and acquisition.

The following four Chapters describe the main experiments and results of this project, using the theory from Chapter 2, aiming to measure single and double quantum dot charge and spin signal in the devices of Chapter 3.

Chapter 4 demonstrates reconfigurable single and double electron and hole quantum dots using the gate-based sensing technique. This work highlights the measurement of inter-dot charge transition of both electron and hole double quantum dots in the same crystalline environment, achieving a minimum integration time of 160 (100) µs for electrons (holes). I further investigate the effective bath temperature of two-dimensional electron gas and two-dimensional hole gas by performing the thermometry experiment on the same type of device. This work analyses the noise-broadening under the different regimes of dispersive gate sensing of the quantum dot.

Chapter 5 focuses on the scalability of foundry fabricated quantum dot devices. A floating-gate type nanowire device demonstrates the measurement capability across different silicon nanowires. Electrostatic coupling between quantum dots is measured and simulated for various distances—this guides the future scaling of the device into the second dimension.

Chapter 6 introduces a silicon nanowire device implanted with a bismuth dopant. The gate-induced quantum dot and bismuth dopant form a double quantum dot system. Using the gate-based sensing technique and pulsing. Pauli spin blockade is observed in the double quantum dot system. The binding energy

of 77 meV is measured for the bismuth donor, and an excited energy of 0.773 meV is measured for triplet states on the donor. The relaxation time between the singlet and triplet states is also measured. This work provides a novel implementation of a spin qubit in silicon and opens up new research directions on hybrid donor-dot spin qubit.

Chapter 7 summarises the key outcomes of the thesis and provides future directions on the open questions of the project.

Chapter 2

Background

For the understanding of the experiments, this Chapter briefly introduces the concepts of silicon quantum dot as the host for spin qubit and the background theory for dispersive readout of the quantum dot.

2.1 Silicon material

There are many types of quantum dot devices employed for quantum computing, including self-assembled QDs [63], defects in solids [64], and layered semiconductors which support two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG) in the inversion layer. In the context of this thesis, the QDs formed in the inversion layer in the Si-MOS device are discussed.

2.1.1 Conduction band and valence band

Silicon is the 14th element with the electron shell configuration: $1s^2$, $2s^2$, $2p^6$, $3s^2$, $3p^2$. The combined 3s and 3p orbitals form two energy bands in the solid: the bonding molecular orbitals at lower energy and the antibonding molecular orbitals at higher energy. There are four valence electrons per atom in silicon, resulting in the filled valence band and the empty conduction band. The calculated electronic energy band structure is shown in Figure 2.1. Silicon has an indirect bandgap $E_g = 1.12\,\text{eV}$ (the energy gap between valence band E_V and the conduction band E_C). The minimum conduction band is not at $k = 0$ but rather at a nonzero value $k = 0.85k_0$, where k_0 is the first Brillouin zone boundary. Due to the cubic

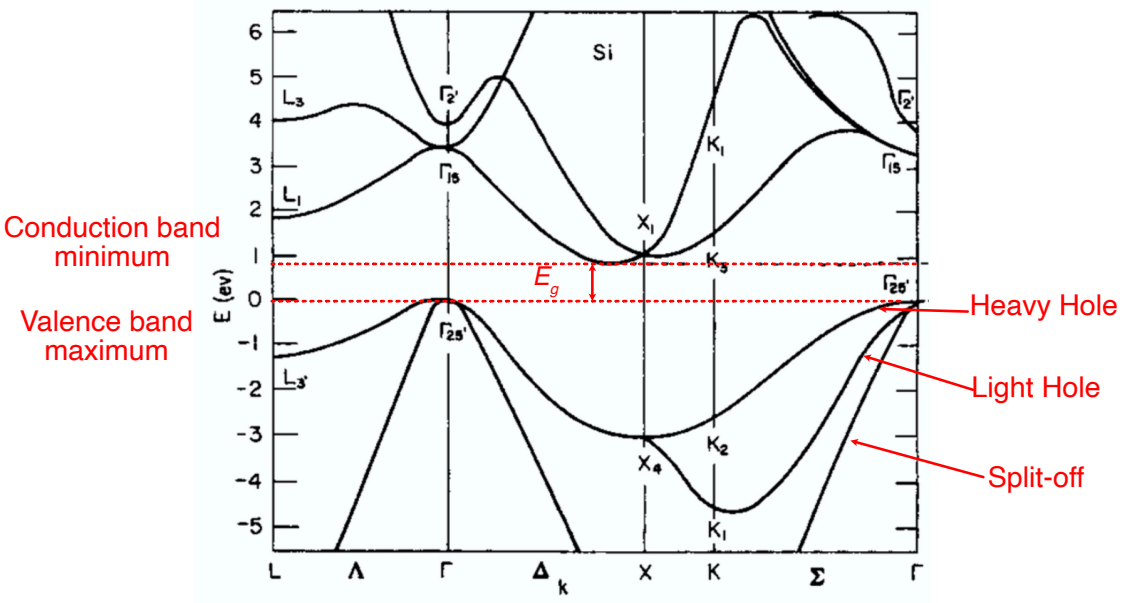


Figure 2.1 Band structure of bulk silicon showing the conduction band minimum, and valence band maximum with heavy hole, light hole band. Adapted from [65]

symmetry of bulk silicon, there are six equivalent minima in momentum k-space, which is also referred to as six degenerate valleys in the conduction band. The constant energy surfaces of the energy minima are ellipsoidal. An energy dispersion relation model is used to define the effective mass of the electron.

$$\frac{1}{m^*} \equiv \frac{1}{\hbar^2}\frac{\partial^2 E(k)}{\partial k^2} \tag{2.1}$$

Take the ellipsoidal z valley, for example, the symmetry demands behaviour along the transverse directions x and y be identical so the same effective mass m_t is used. The longitudinal z-direction has a different effective mass m_l. The energy dispersion of the valley at $k = 0$ is described by:

$$E(k) = E_\mathrm{C} + \frac{\hbar^2}{2m_0}\left[\frac{k_x^2}{m_\mathrm{t}} + \frac{k_y^2}{m_\mathrm{t}} + \frac{(k_z - k_0)^2}{m_\mathrm{l}}\right] \tag{2.2}$$

where m_l and m_t are effective masses for electron in the longitudinal and transverse direction. The values of the two effective masses are $m_\mathrm{t} = 0.19m_0$ and $m_\mathrm{l} = 0.98m_0$, with m_0 being the free electron mass [65].

Valence bands are constructed from p_z orbitals, which are highly anisotropic and overlap strongly in the z-direction. This makes the effective mass for electrons lower in the z-direction and higher in the xy-plane. As a result, two overlapped

heavy hole bands and one light hole band degenerate at $k = 0$. There is also a non-negligible split-off band separated 44 meV below the other subbands by the spin-orbit splitting. Near the $k = 0$ point, the energy dispersion is very simply defined by:

$$E(k) = E_{\mathrm{V}} - \frac{\hbar^2 k^2}{2m_h} \tag{2.3}$$

where m_{h} could take the value of heavy hole effective mass $m_{\mathrm{hh}} = 0.53m_0$, light hole effective mass $m_{\mathrm{lh}} = 0.15m_0$ and split-off band effective mass $m_{\mathrm{so}} = 0.23m_0$ [65].

2.1.2 Two-Dimensional Electron(Hole) Gas

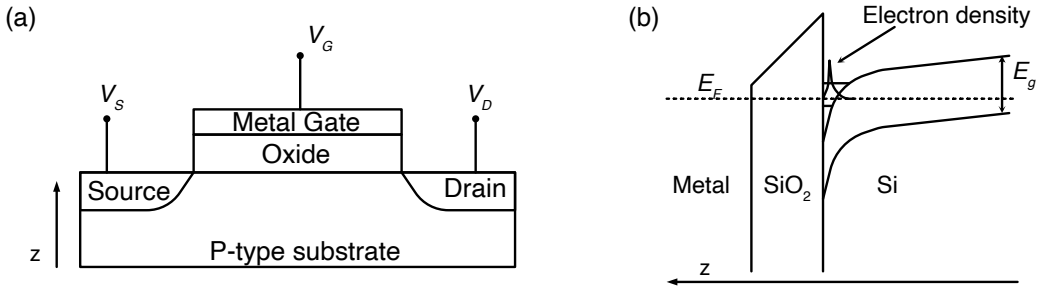


Figure 2.2 (a) schematic of an n-type MOSFET with source, drain and the gate electrode. (b) Band structure of the Si/SiO2 interface, a two-dimensional electron gas is formed in the inversion layer when the gate voltage exceeds the threshold voltage

Metal-oxide-silicon field-effect transistor(MOSFET) is the unit cell in the modern IC industry. Figure 2.2(a) shows a simplified schematic of n-type MOSFET device. Here n-type devices have n-type doped (P, As) silicon as source and drain, and the carrier in the channel is electron during normal operation. For the p-type device, the carrier is hole coming from p-type doped (B, Ga) silicon as the source and drain. During normal turn-on operation of n-type MOSFET, a gate voltage above threshold voltage $V_{\mathrm{g}} > V_{\mathrm{th}}$ is applied to the metal gate, electric charge is induced at the Si/SiO2 interface, and electron carrier flows from source to drain close to the interface. Figure 2.2(b) shows the band structure of Si/SiO2 interface in the vicinity under such condition. The energy band of the p-type Si substrate is bent towards the interface. The energy level of the conduction band (E_{C}) at the interface has lower energy than the

fermi level (E_{F}) of the p-type silicon substrate. As a result, electron bound states along the z-axis in silicon Figure 2.2(a) accumulate, thus leading to a two-dimensional electron subband in this inversion layer. In the 2D plane of 2DEG, electrons are unconfined in the xy plane and are confined by a triangular potential well perpendicular to the plane. Other confinement in the xy plane can be provided from the electrode. In a nanowire with high aspect ratio, a one-dimension channel with few subbands is naturally created from the physical dimension, and additional confinement towards 0D confinement can also be provided from the electrode. Similarly, for the p-type device, a two-dimensional hole subband can be formed when the energy level of the valence band satisfies ($E_{\mathrm{V}} > E_{\mathrm{F}}$). The 2DEG and 2DHG have high carrier mobility and low carrier density. In the semiclassical Drude model, the carrier movement under the electric field is described by the gain from the electric field and loss from the collision. The drift speed and mobility are defined as:

$$v = \frac{e\tau}{m^*}\mathrm{E}, \mu = \frac{\mathrm{v}}{\mathrm{E}} = \frac{\mathrm{e}\tau}{\mathrm{m}^*} \tag{2.4}$$

where E is the electric field, e is the elementary charge, τ is the average relaxation time due to collision. For a typical silicon MOSFET at room temperature. The typical carrier mobility for electron and hole in intrinsic silicon is $1450\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $505\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ respectly [66], and more details can be found on mobility study of silicon and germanium in the review [67].

2.2 Silicon Quantum Dot

Quantum dots are artificial nanostructures in a solid, typically consisting of many atoms and tightly bounded electrons [68]. They provide the confinement of free electrons or holes via exchange with a nearby reservoir. In this regime, Coulomb interactions play a dominant role compared to other energy scales.

2.2.1 Coulomb Blockade

Next, a qualitative description of the gate-defined quantum dot is introduced, as shown in Figure 2.3(a). A charge island is tunnel coupled to a nearby source /drain lead and capacitively coupled to a plunger gate.

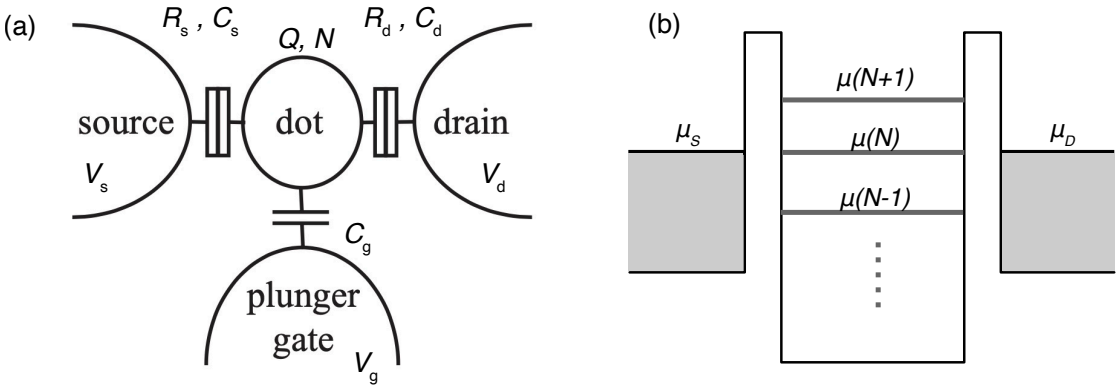


Figure 2.3 (a) Schematic representation of a quantum dot system with source and drain contacts and plunger gate. (b) Energy level structure of the system in the quantum dot. Adapted from [69]

The source and drain tunnel barriers represented by a resistance $R_{\mathrm{s/d}}$ and a capacitance $C_{\mathrm{s/d}}$. The tunnel resistance $R_{\mathrm{s/d}}$ should be larger than the resistance quantum R_{Q} to allow the measurement of charging energy whenever the tunneling coupling is weak enough to quantize the electron number N on the island.

$$R_{\mathrm{s(d)}} > R_{\mathrm{Q}} = h/e^2 \tag{2.5}$$

The total charge Q on this island has an integer number of the single electron charge $Q = Ne$, and this leads to electrostatic energy:

$$E_{\mathrm{el}} = \frac{Q^2}{2C} = \frac{e^2N^2}{2C} \tag{2.6}$$

The constant interaction model is based on the Coulomb interactions parametrized by constant capacitance C and voltages applied to the source V_{s}, drain V_{d}, and gate electrode V_{g}. The single-particle energy level is independent of these interactions and the number of electrons. The capacitance C_{Σ} is the sum of the capacitances between the dot and the source/ drain lead and the gate. With the increasing complexity of devices, capacitances to other parts of the device

can be added.

$$C_\Sigma = C_\mathrm{s} + C_\mathrm{d} + C_\mathrm{g} \tag{2.7}$$

This leads to the electrostatic energy of QD with N electrons:

$$E_\mathrm{el}(N) = \frac{(eN - C_\mathrm{s}V_\mathrm{s} - C_\mathrm{d}V_\mathrm{d} - C_\mathrm{g}V_\mathrm{g})^2}{2C_\Sigma} + \sum_{n=1}^{N} E_n(B) \tag{2.8}$$

A convenient way to describe the energy levels of the quantum dot is the electrochemical potential $\mu(N)$. It is defined as the change in total electrostatic energy when the N-th electron is added:

$$\mu(N) = E_\mathrm{el}(N) - E_\mathrm{el}(N-1) = \frac{e}{C_\Sigma}\left[(N-1/2)e - C_\mathrm{g}V_\mathrm{g} - C_\mathrm{s}V_\mathrm{s} - C_\mathrm{d}V_\mathrm{d}\right] + E_N \tag{2.9}$$

where each gate voltage V_s, V_d, V_g can affect the electrochemical potential individually. For convenience the dimensionless lever arm is defined to reflect this ratio:

$$a_i = \frac{C_i}{C_\Sigma} \tag{2.10}$$

Following the electrochemical potential of the electron in QD, the addition energy required to add the electron to the island is:

$$\Delta E_\mathrm{add} = \mu(N+1) - \mu(N) = \frac{e^2}{C_\Sigma} + E_{N+1} - E_N = E_\mathrm{C} + \Delta E \tag{2.11}$$

The addition energy consists of two parts: an electrostatic charging energy $E_\mathrm{C} = \frac{e^2}{C_\Sigma}$, and the energy spacing between two discrete quantum levels ΔE. $\Delta E = E_{N+1} - E_N$ comes from spacing between the single-particle energy. The last term of Equation 2.8 is a sum over the occupied single-particle energy levels $E_n(B)$, which depends on the characteristics of the quantum confinement. It arises when the dimensions of the QD is comparable or smaller than the electron Fermi wavelength in host material silicon ($\lambda_\mathrm{F} = 35$ nm) [65]. The spin and valley degrees of freedom in the quantum dot give this fine structure of the single-particle spectrum.

In order to resolve quantized energy levels and excited states, the thermal energy $k_\mathrm{B}T$ has to be well below the energy scales of the dot E_C and the single-particle energy ΔE. Therefore transport measurements of the quantum

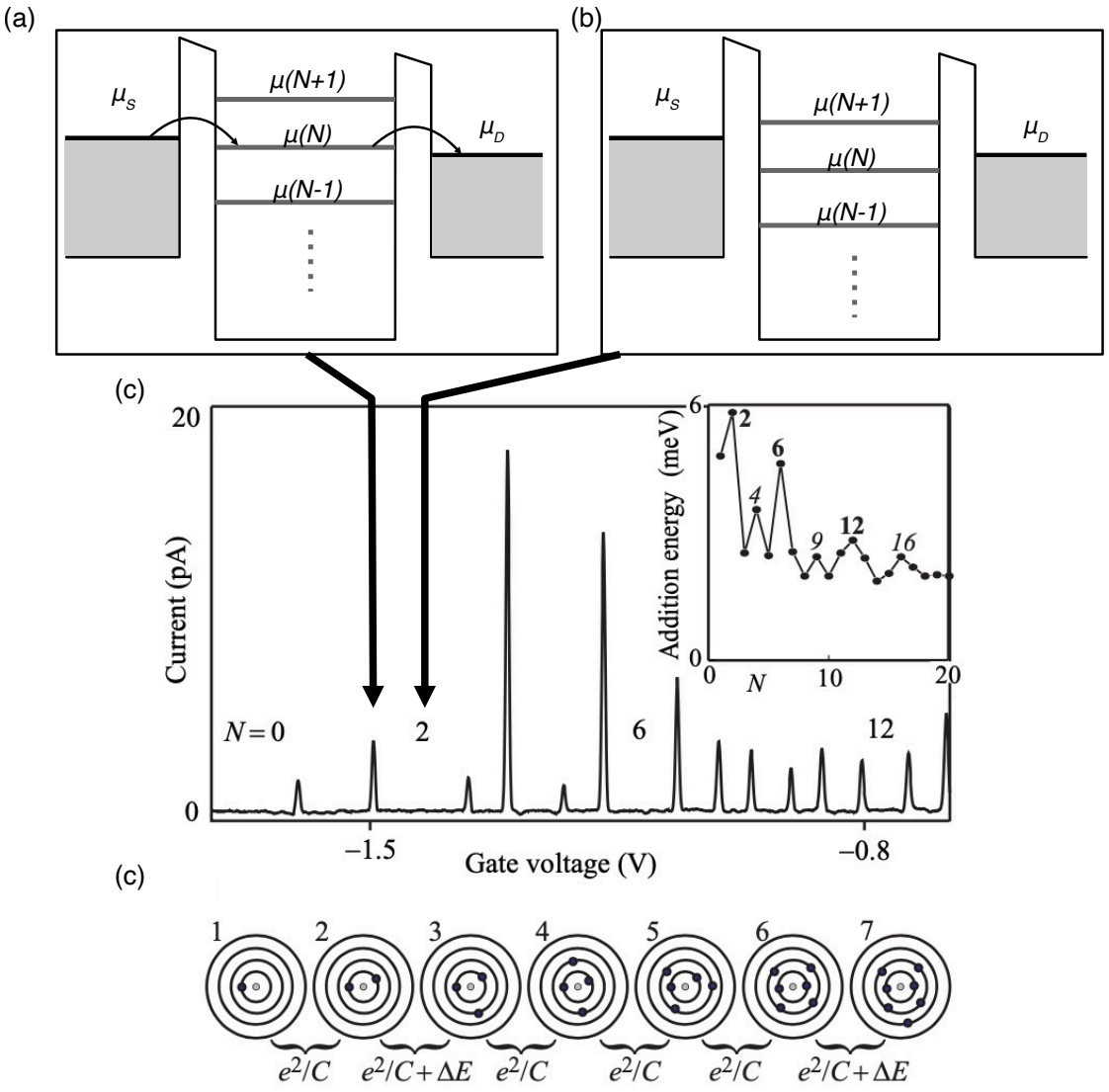


Figure 2.4 (a)Electrostatic energy of the quantum dot in linear transport regime. (b)Electrostatic energy of the quantum dot in Coulomb blockade regime. (c) Transport measurement of quantum dot showing Coulomb oscillation. (d) Quantum dot artificial atoms with filling energy shells in analogy with three dimensional atoms. (c,d)Adapted from [70]

dot are performed at cryogenic temperatures. The discrete energy spectrum of the quantum dot can be electrically probed. As shown in Equation 2.9 voltage on the electrode V_{s}, V_{d}, V_{g} can tune the electrochemical potential $\mu(N)$ linearly via the lever arm ratio.

Electrochemical potential $\mu_{\mathrm{s/d}}$ of the reservoir are set by the voltages on the source/drain leads. The source-drain bias determines the electrochemical potential $V_{sd} = (\mu_s - \mu_d)/e$. Electron density states in the reservoirs follow a Fermi-Dirac probability distribution $f(E)$ which leads to the broadening the states determined by temperature.

$$f(E) = \frac{1}{1 + e^{(E-E_{\mathrm{F}})/k_{\mathrm{B}}T}} \tag{2.12}$$

In the linear transport regime, when a small bias $V_{\mathrm{sd}} = V_{\mathrm{s}} - V_{\mathrm{d}}$ is applied between the source and drain, transport through the QD is only permitted when there are available levels $\mu(N)$ of the QD in the bias window determined by the bias V_{sd} as shown in Figure 2.4(a). In the other case, Figure 2.4(b) where there are no QD levels in the bias window, the transport is blocked, leading to a 0 current I_{sd} known as the Coulomb blockade. As gate voltage V_{g} tunes the electrochemical potential of QD to align and misalign with the bias window, regular spikes in the current(conductance) can be observed as a function of gate voltage V_{g} as shown in Figure 2.4(c). The ΔE_{add} is extracted (Figure 2.4(d)-inset) from the Coulomb blockade transport measurement, and a regular QD behaves like an artificial atom showing shell filling patterning for s- and p-shell [70].

In the non-linear transport regime $V_{\mathrm{sd}} > 0$, the window at which transport through the QD broadens as bias voltage V_{sd} increases. This characteristic leads to the so-called Coulomb diamonds pattern [69, 71]as shown in Figure 2.5(a). Outside the grey shaded area, the transport is blocked, and the number of electrons on the dot is constant. The highlighted black lines correspond to the situation where the electrochemical potential of source/drain is aligned to the electrochemical potential of the dot ($\mu_{\mathrm{s}} = \mu(N+1)$, $\mu_{\mathrm{d}} = \mu(N)$). From the constant interaction model, the slope for the boundary of Coulomb diamonds is obtained: $eC_{\mathrm{g}}/C_{\mathrm{s}}$ and $-eC_{\mathrm{g}}/(C_{\mathrm{g}} + C_{\mathrm{d}})$. In the shaded area where single-electron tunnelling occurs. An increase in current can be observed. These can be understood as an excited state entering the bias window as shown in Figure 2.5(b)(d). The addition energy ΔE_{add} and

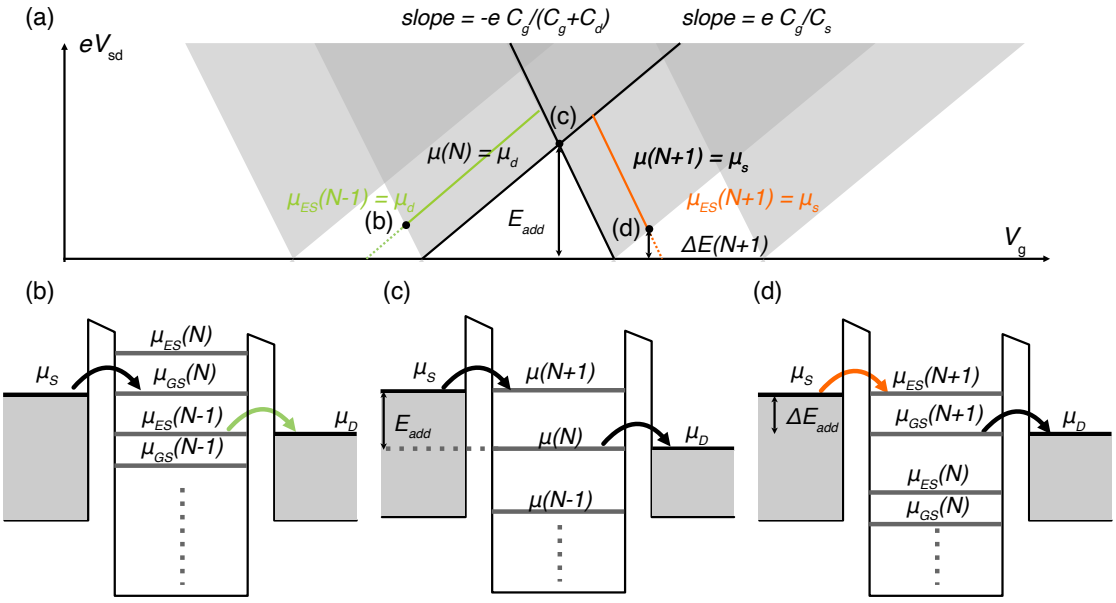


Figure 2.5 (a)Schematic plot of the transport current I_{sd} as a function of eV_{sd} and V_{g}. several scenario when the level alignment is indicated with energy schematic diagrams(b,c,d). (b)excited states $\mu_{\mathrm{ES}}(N-1)$ aligned with electrochemical energy of drain. (c)two QD levels $\mu(N)$ and $\mu(N+1)$ aligned with the electrochemical energy of the source and drain. (d)excited states $\mu_{\mathrm{ES}}(N+1)$ aligned with electrochemical energy of source. Adapted from [69]

single-particle level spacing $\Delta E(N)$ can be extracted from the Coulomb diamond measurement at the height shown in Figure 2.5(c)(d). The spin filling can also be studied further in Coulomb diamond measurement from magneto-spectroscopy by looking at the Zeeman energy shift of the Coulomb peaks [71].

2.2.2 Double Quantum Dots

This part will introduce the double quantum dot (DQD) system based on the previous constant interaction model and quantum transport discussed for single QD. The double quantum dots are capacitively and tunnel coupled with the mutual capacitance E_{Cm} and resistance R_{Cm} between each other. Similar to single QD, bot dots are coupled capacitively to the plunger gate via $C_{\mathrm{g1d1}}, C_{\mathrm{g2d2}}$, and nearby reservoir $C_{\mathrm{s(d)}}$. Additionally, cross-capacitances between plunger gate 1(2) and QD 2(1) is also introduced and given as $C_{\mathrm{g1d2}}, C_{\mathrm{g2d1}}$. The total capacitance of each quantum dot is defined as: $C_{1(2)} = C_{L(R)} + C_{g1(2)d1(2)} + C_{g2(1)d1(2)} + C_m$.

Expanding the single QD electrostatic energy to DQD, every charge on the node can be added up by the linear combination of each voltage via by the capacitance

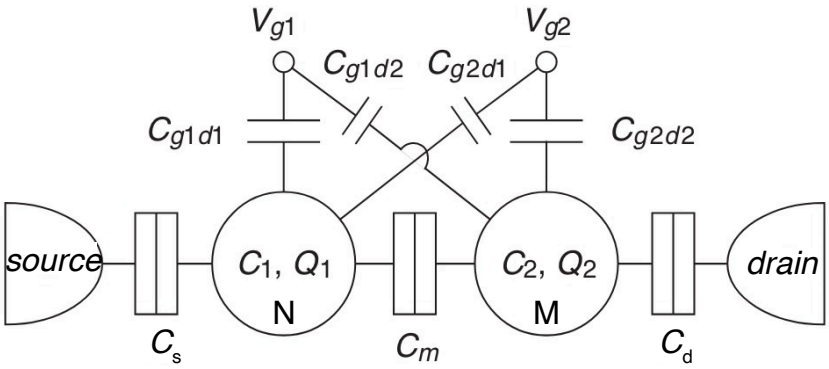


Figure 2.6 schematic of double quantum dot QD1,QD2 with source/drain leads and two gate voltages. Adapted from [72]

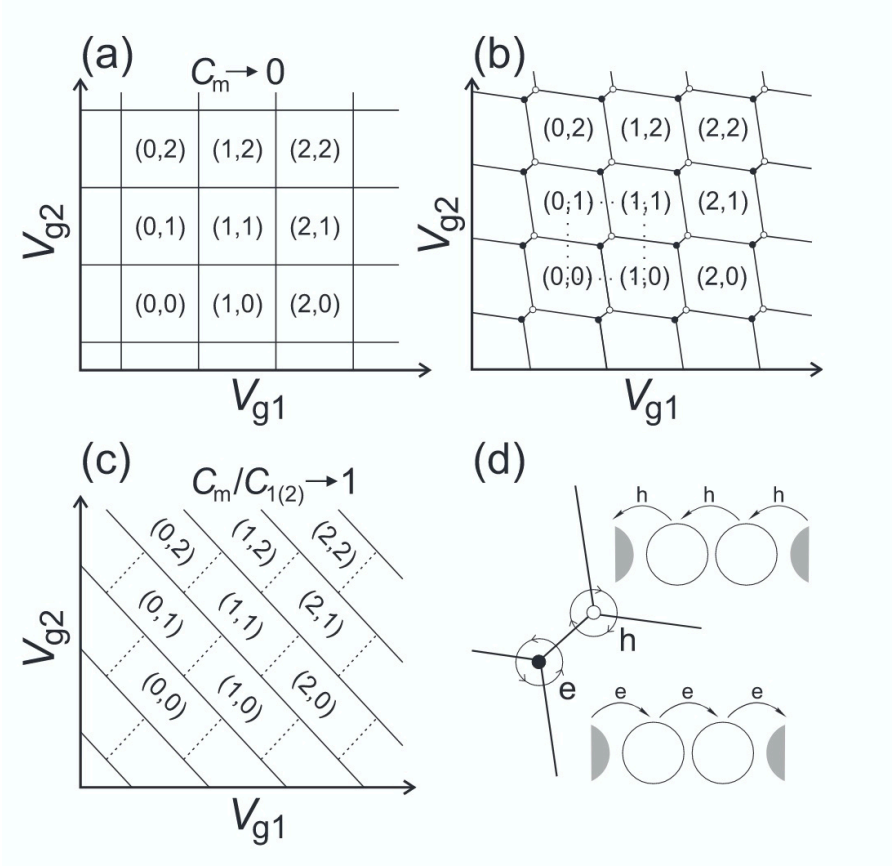
matrix $\overrightarrow{Q} = \mathbf{C}\overrightarrow{V}$. The electrostatic energy $E_{el}(N,M) = \frac{1}{2}\overrightarrow{V}\mathbf{C}\overrightarrow{V}$ of this double QD with N and M electrons on QD 1 and 2, respectively, is then given by

$$E_{el}(N,M) = E_{\mathrm{C1}}N^2/2 + E_{\mathrm{C2}}M^2/2 + E_{\mathrm{Cm}}NM + E_{n1}N + E_{n2}M \tag{2.13}$$

where $E_{\mathrm{C1(2)}}$ is the charging energies of the two dots correspondingly, E_{Cm} is the electrostatic coupling energy between them, and E_{n1} and E_{n2} are the single-particle energies of the two dots. With the sum of the capacitances directly coupled to each quantum dot defined as C, these energies can be expressed in terms of the capacitances as follows:

$$E_{C1} = e^2\frac{C_2}{C_1C_2 - C_m^2}, E_{C2} = e^2\frac{C_1}{C_1C_2 - C_m^2}, E_{Cm} = e^2\frac{C_m}{C_1C_2 - C_m^2} \tag{2.14}$$

To understand the DQD sytem, the **stability diagram** is introduced which visualizes the equilibrium charge states of two coupled QD connected in series. Figures 2.7(a-c) show the stability diagrams as a function of V_{g1} and V_{g2} for different regimes of inter-dot coupling. When C_{m} and $C_{\mathrm{g1d2(g2d1)}} = 0$, QD1 and QD2 is completely decoupled from each other and the corresponding gate. When $C_{\mathrm{m}}/C_{\mathrm{1(2)}} \rightarrow 1$, the mutal capacitance is big enough to dominate the total capacitance of QD, this means the two QD are strongly coupled and behave as a big single QD. In a typical DQD stabilit diagram where all coupling capacitance are intermediate, the triple point and inter-dot charge transistion can be observed in the so-called honeycomb diagram. At the triple points illustrated in



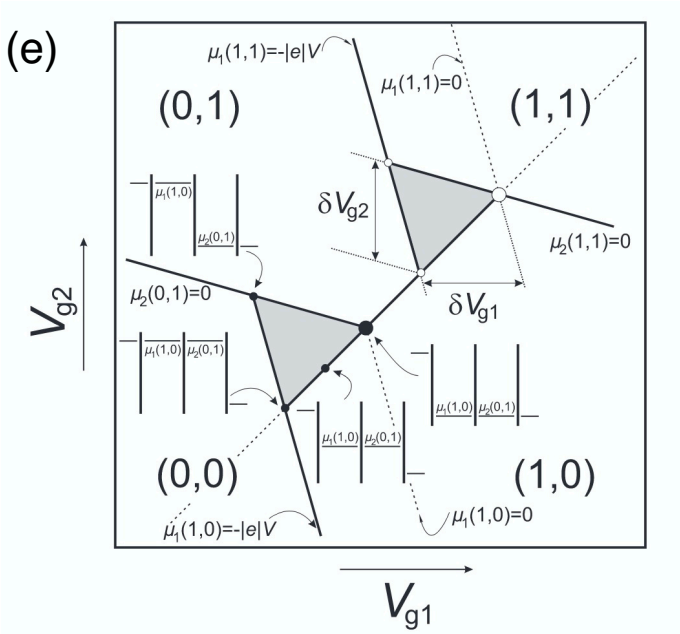


Figure 2.7 stability diagram of the double-dot systems with QD occupation numbers (N_1, N_2) for (a)small, (b)intermediate, and large(c) inter-dot coupling. (d) double-dot quantum transport at triple point. (e) bias-triangle Adapted from [73]

Figures 2.7(d), the energy levels of the two QDs are aligned with the source and drain thus leading to the quantum transport through the DQD. At high bias regime where $V_{sd} > 0$, these triple points broadens and turn into bias-triangle as shown in Figures 2.7(e). Within the shaded bias-triangle area, the electrochemical potentials of the DQD lies in the bias window of source and drain. The vertex of the bias triangle marks the alignment of QD1 and QD2 energy levels with corresponding source and drain. Furthermore, the successive alignment of ground and excited states contributes to conductance resonances within the bias triangles. The tunnelling of electrons through the potential barrier is spin conserved. In some special cases, where the electron system's initial and final state have orthogonal spin configurations, the transport is forbidden, and the tunnelling current is strongly suppressed. This event is called **spin blockade** and usually observed in double quantum dots transition with electron numbers (1,1) - (2,0) or effective configuration with filled shell [74]. From the transport measurements forementioned (Coulomb diamond and bias-triangle), charging energies, QD configurations, capacitances and inter-dot coupling can be all extracted.

2.2.3 Dopants in silicon

Another quantum dot realization in silicon is dopant. There are two methods to achieve precise dopant placement in silicon: ion implantation [75] and scanning probe lithography [76]. Figure 2.8(a) shows the crystal structure of single ^{31}P dopant in silicon. The electrostatic potential of a single-dopant atom is radially symmetric and steep, which creates the confinement of free electron. In Figure 2.8(b), a ^{31}P dopant atom has three charge states: the ionized D^+ state which corresponds to an empty dopant with a filled orbit which does not appear as an electron energy state, the neutral D^0 state with one electron bound to the dopant, and the negatively charged D^- state with two electrons in the outer shell bound to the dopant. The binding energy of the dopant is defined as the energy difference between D^- and D^0 states. A nearby gate electrode can electrically control the dopant charge state. The dopant in solid especially donor in silicon can be found in review [64]. The system Hamiltonian of the donor nuclear spin

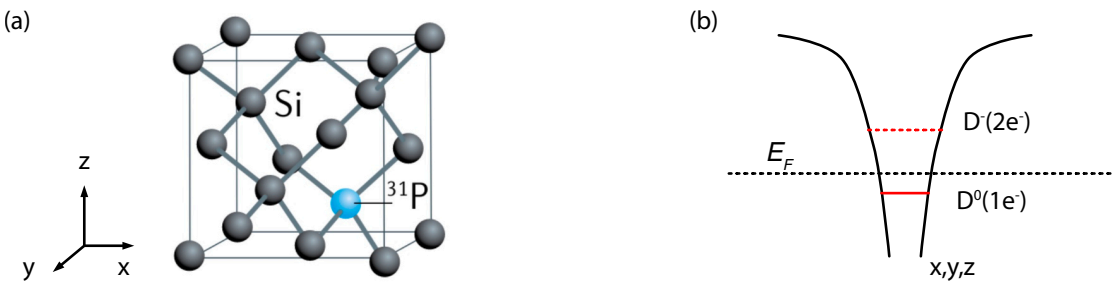


Figure 2.8 (a) crystal structure of single ^{31}P dopant in Silicon adapted from [77]. (b) Band structure of the single dopant quantum confinement with the corresponding atom ionized state.

and electron spin under applied static magnetic field B_0 can be written as:

$$H = H_z + H_{hf} + H_{ss} + H_{so} \tag{2.15}$$

The four terms describe the Zeeman, hyperfine, spin-spin and spin-orbit interactions. The first term Zeeman energy H_z consists of the electron spin and nuclear spin Zeeman energy:

$$H_z = \gamma_{\mathrm{e}}\mathbf{B}_0 \cdot \mathbf{S} - \gamma_{\mathrm{n}}\mathbf{B}_0 \cdot \mathbf{I} \tag{2.16}$$

where the $\mathbf{S}$ and $\mathbf{I}$ represents the electron and nuclear spin , $\gamma_{\mathrm{e}} = g_e\mu_e/h$ is the electron gyromagnetic ratio, with g_{e} being the electron g-factor. $\gamma_{\mathrm{n}} = g_{\mathrm{n}}\mu_n/h$ is the nuclear gyromagnetic ratio, with g_{n} being the nuclear g-factor and μ_n the nuclear magneton. $g_{\mathrm{e}} \approx 2$ is usually used for electrons in silicon. The hyperfine term describes the contact hyperfine interaction between the electron and donor nucleus:

$$H_{hf} = \mathbf{A_{hf}}\mathbf{S} \cdot \mathbf{I} \tag{2.17}$$

where $\mathbf{A_{hf}}$ is the hyperfine tensor, $\mathbf{S}\cdot\mathbf{I}$ creates the N-th dimensional Hilbert space(N $= dim(\mathbf{S}) \times dim(\mathbf{I})$). For phosphors donor in silicon, $I = 1/2, S = 1/2$, there are 4 eigenstates represented by $|m_s\rangle, |m_I\rangle$ for this system, where $|m_s\rangle = \pm 1/2$, and $|m_I\rangle = \pm 1/2$ [78]. For high nuclear spin number donor such as antimony($I = 7/2$) [79] and bismuth($I = 9/2$) [80] in silicon, a much larger hilbert space (16th, 20th dimensional respectively) can be created and quantum chaos experiments are explored in these system [81].

The spin-spin term consist of the exchange interaction dependent on energy detuning and spin dipole-dipole coupling $H_{dd} = \mathbf{DS}\cdot\mathbf{I}$ in which $\mathbf{D}$ is dependent on spatial separation $(1/r^3)$ between the spins [82]. The spin-orbit term $H_{so} = \mathbf{A_{so}L}\cdot\mathbf{S}$ where $\mathbf{L}$ is the orbital quantum number and $\mathbf{S}$ is the spin quantum number. The spin-orbit coupling $\mathbf{A_{so}}$ is large in the material system such as GaAs which has a high atomic number and bulk anisotropy in solids. The spin-orbit coupling is small in the silicon conduction band due to its bulk inversion symmetry. In the donor-dot system in Chapter 7, only Zeeman and the hyperfine term are considered.

2.3 Charge and Spin state in QD

2.3.1 Charge state

The first implementation of qubit in silicon is single electron charge state in tunnel coupled DQD. The one-electron charge states (0,1) and (1,0) representing whether the electron is on the right dot or the left, form the basis states $|0\rangle$ and $|1\rangle$. As shown in Figure 2.9(a). the energy detuning ε is defined as the gate voltage

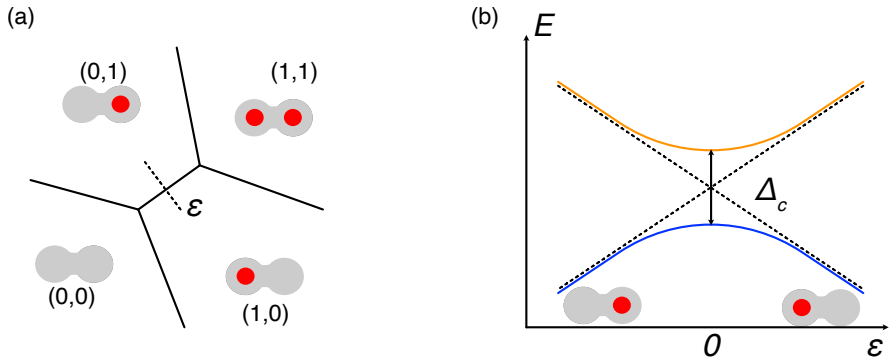


Figure 2.9 (a)stability diagram of double quantum dot with less than 2 electron, charge qubit encoded in the detuning (ε) direction with the (0,1) and (1,0) states (b)energy diagram of the double quantum dot as a charge qubits

variable which crosses the (1,0) and (0,1) interdot charge transition (IDT) and sets the energy splitting. The tunnel coupling, which represents the interdot tunnelling transition ($t_c = \Delta_c/2$) gives the off-diagonal terms in the Hamiltonian, leading to the overall Hamiltonian and eigenenergies given in terms of Pauli spin matrices $\sigma_{x,y,z}$ as:

$$H_c(\varepsilon) = -\frac{\Delta_c}{2}\sigma_x - \frac{\varepsilon}{2}\sigma_z \tag{2.18}$$

where the detuning ε is the difference in electrochemical potentials of the two dots. The eigenstates of this system (bonding and antibonding charge states) are represented by $E_{\pm} = \alpha|0\rangle \pm \beta|1\rangle$ bounded by an avoided crossing representing the energy level with no tunnel coupling.

$$E_{\pm} = \pm\frac{1}{2}\sqrt{\varepsilon^2 + \Delta_{\mathrm{c}}^2} \tag{2.19}$$

At zero detuning $\varepsilon = 0$, the eigenstates are shifted from the avoided crossing by the amount of t_{c} leading to the total splitting in between of $\Delta_{\mathrm{c}} = 2t_{\mathrm{c}}$ as shown in Figure 2.9(b) and the system has same probability to be in the (1,0) and (0,1) basis. At far detuning $\varepsilon \gg 0$, the system is almost classical and shows a classical charge state. With zero applied magnetic fields, the two eigenstates are spin-degenerate. It can be coherently driven between both states with microwave of which energy that matches the $E_{\mathrm{C}_{\pm}}$ splitting $hv = \sqrt{\varepsilon^2 + \Delta_c^2}$. The energy level spectroscopy and measurements of the charge qubit's coherence time can be performed through the process known as photon assisted tunnelling. With chopped microwave control, the charge fluctuation can be removed and measure the charge coherence time more acurately [32, 83].

2.3.2 Spin state

Silicon is an ideal environment for the spin state in the solid state, one and two-electron spin states in a quantum dot are considered in this following part. The non-zero magnetic field splits spin state of a single electron in quantum dot by the Zeeman energy $\Delta E_z = \mu_{\mathrm{e}} g B_z$. where μ_{e} is the Bohr magneton and g represents electron g-factor. The spin-up and spin-down electron defined by the applied field form the basis state $|\uparrow\rangle$ and $|\downarrow\rangle$ of the spin qubit. A spin qubit can be manipulated using Electron Spin Resonance (ESR) or Electron Dipole Spin Resonance (EDSR). With non-zero magnetic field B_0, microwave applied to an on-chip transmission line to create an oscillating magnetic field B_1, rotations between $|\uparrow\rangle$ and $|\downarrow\rangle$ can be coherently driven [56]. The alternative EDSR uses the oscillating electric field, which requires the interaction between the electric field and the electron spin. In silicon, the intrinsic spin-orbit coupling which couples the electric field and the

electron spin is weak. An external micro-magnet is used to create a magnetic field gradient that couples the electric field and the electron spin via synthetic spin-orbit coupling [57]. For hole spin qubit, the spin-orbit coupling at valence band is relative big [84], this removes the complexity in incorporating extra micro-structures in qubit devices.

The spin state of two electron in a quantum dot leads to four states. These singlet and triplet states are defined by following equations:

$$|S\rangle = (|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)/\sqrt{2}, \tag{2.20}$$

$$|T_0\rangle = (|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle)/\sqrt{2}, \tag{2.21}$$

$$|T_+\rangle = |\uparrow\uparrow\rangle, \tag{2.22}$$

$$|T_-\rangle = |\downarrow\downarrow\rangle. \tag{2.23}$$

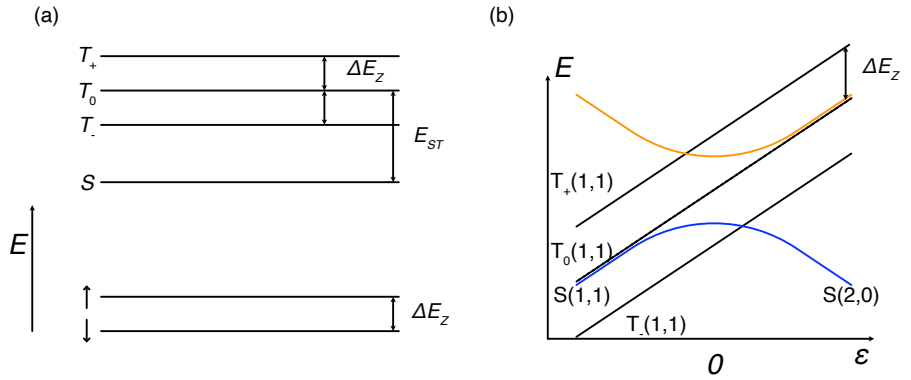


Figure 2.10 (a)stability diagram of double quantum dot with less than 2 electron, charge qubit encoded in the detuning (ε) direction with the (0,1) and (1,0) states (b)energy diagram of the double quantum dot as a charge qubits. Adapted from ref [71]

As shown in Figure 2.10(a), the ground state singlet with two electrons occupying the lowest orbital with antiparallel spins has a total spin quantum number $S_z = 0$. The other three triplets are degenerate at zero-field and they require one electron to occupy a higher orbital in the QD. In silicon, the energy difference between $S - T_0$ singlet-triple E_{ST} is a result of orbital-valley

mixing [71]. At a finite magnetic field, the T_+ ($S_z = 1$) state and the T_- ($S_z =$ -1) state are shifted by $\pm\Delta E_z$. It is proposed to use two spin states S and T_0 as the basis for the $S-T$ qubit which is resilient to magnetic noise [85]. The operation $S-T$ qubit is located in the (1,1)-(2,0) charge transition of the DQD. Figure 2.10(b) shows the energy-detuning plot of the two-spin energy states. Only considering the tunnelling coupling between $S(1,1) - S(2,0)$, the eigenstates of this DQD system at the finite field are S bonding and antibonding states and three triplet states. At the far detuning of $S(1,1) - (2,0)$ mixed state, the $S(1,1)$ and $T_0(1,1)$ are almost degenerate due to the small overlap between the electron wavefunctions. The two states are differed by the exchange coupling $J(\varepsilon)$. For a fixed tunnel coupling between the DQD, exchange coupling is dependent on the detuning ε, therefore controllable by gate voltages. Exchange coupling is used to drive qubit rotations between $S - T_0$ states. Pauli spin blockade lies in the $S(2,0) - T_0(2,0)$ energy difference E_{ST} for given detuning, therefore it is be used to initialize and readout the singlet-triple state [86].

Other spin state mixing such as $S - T_-$ is shown in Figure 2.10(b) and $T(1,1)$ and $T(2,0)$ not shown at high detuning of Figure 2.10(b). The $S - T_-$ crossing is mixed due to the host's spin-orbit coupling and nuclear spin. Angular momentum conservation leads to a simultaneous spin 'flop' of the neighbouring nuclear spin. This mixing in GaAs ($S - T_+$ for positive g-factor) could build up a nuclear spin polarization by repetitively driving detuning across the transistion [87, 88]. As a result, the inhomogeneous coherence time T_2^* is significantly increased [89]. This $S - T_-$ crossing is also studied in the donor-dot system (Chapter 7) as an indirect way to access the donor nuclear spin. $T(1,1)$ and $T(2,0)$ mixing via tunnel coupling occur at large detuning due to large valley-orbital energy splitting E_{ST} in QDs [90]. Moreover, at a high spin state with a high magnetic field, mixing of spin states with total spin angular momentum up to $S = 3$ has been demonstrated [91].

2.3.3 Charge readout

Measurement of single charge via direct transport is limited by the tunnel rates between the reservoir and integration time. Instead, local charge sensors are

proposed to determine the number of electrons in single or double quantum dots via electrostatic coupling. Charge sensors are realized in one-dimensional constrictions known as quantum point contact (QPC) or using charge islands such as single electron transistor (SET) or single electron box (SEB) [92, 93]. The charge sensor is placed close to the qubit device and biased at the point of maximum transconductance dI/dV for optimal sensitivity [94]. In order to benchmark the charge sensing performance, the noise spectral density $S_{\mathrm{I}}(\omega)$ and the sensitivity of the current to charge environment ($\partial I/\partial Q$) are used to define the charge sensitivity [95]:

$$\delta q = \frac{\sqrt{S_{\mathrm{I}}(\omega)}}{\partial I/\partial Q} \tag{2.24}$$

The current noise spectral density $S_{\mathrm{I}}(\omega)$ has three main contributors: the thermal noise [96, 97], the shot noise [98] and the charge noise [99]. It is calculated for a practical charge sensor at $T = 100\,\mathrm{mK}$, the dominant noise comes from the fluctuations in the nearby charge trap [100]. With the typical resistance ($R \sim 100\,\mathrm{k\Omega}$) of the measurement apparatus and the capacitive components ($C \sim 1\,\mathrm{nF}$) in the cables, the bandwidth of the charge sensor in DC transport is estimated to be in the order of kHz [101]. To further improve the sensitivity and bandwidth of the charge sensing measurement, radio-frequency (RF) electrometers are pioneered by Schoelkopf et al. [101] to overcome the dominating charge noise at low frequency. A sensitivities as low as $\delta q = 1\,\mu e/\sqrt{\mathrm{Hz}}$ is achieved with a measurement bandwidth up to 10 MHz [102]. Benefitting from the improvements in bandwidth, sub-microsecond measurement is possible for high fidelity readout of silicon spin qubit.

2.3.4 Spin readout

Measurement of spin state has been conventionally done with spin resonance techniques. Bulk spin resonance typically has the detection limit of 10^{13} spins [103]. This limit is brought down to 10^2 hundred spins by using micro-resonators [104, 105]. NV-centres could sense single spins in close proximity but are difficult to incorporate [106, 107]. In QD devices, **spin-charge conversion** is used to measure spin state indirectly via charge movement.

Spin-selective tunnelling: A energy-selective tunnelling method relys on exchanging electrons with the nearby reservoir to readout the spin state of the electron. At a magnetic field B_z, the spin up and down states of the electron ($\mu_\uparrow$ and $\mu_\downarrow$) are splitted by the energy ΔE_z. During the readout, the reservoir Fermi level μ_{res} is placed near the centre of the window between the $\mu_\uparrow$ and $\mu_\downarrow$ state. For a spin-up state, electron tunnels onto the reservoir and is then followed by an electron tunnelling back onto the spin-down state of the QD. On the contrary, an electron initially at a spin-down state remains in the QD and no tunnelling event happens [31]. This spin-dependent tunnelling event shows as a blip in the time-domain sensor signal, and the spin state can be determined as shown in Figure 2.11(a). The tunnelling rate of spin up and spin down state need to be slower than the measurement bandwidth for detection of tunnel event, and the Zeeman splitting window need to be much larger than the thermal broadening of reservoir fermi level for high-fidelity readout [108].

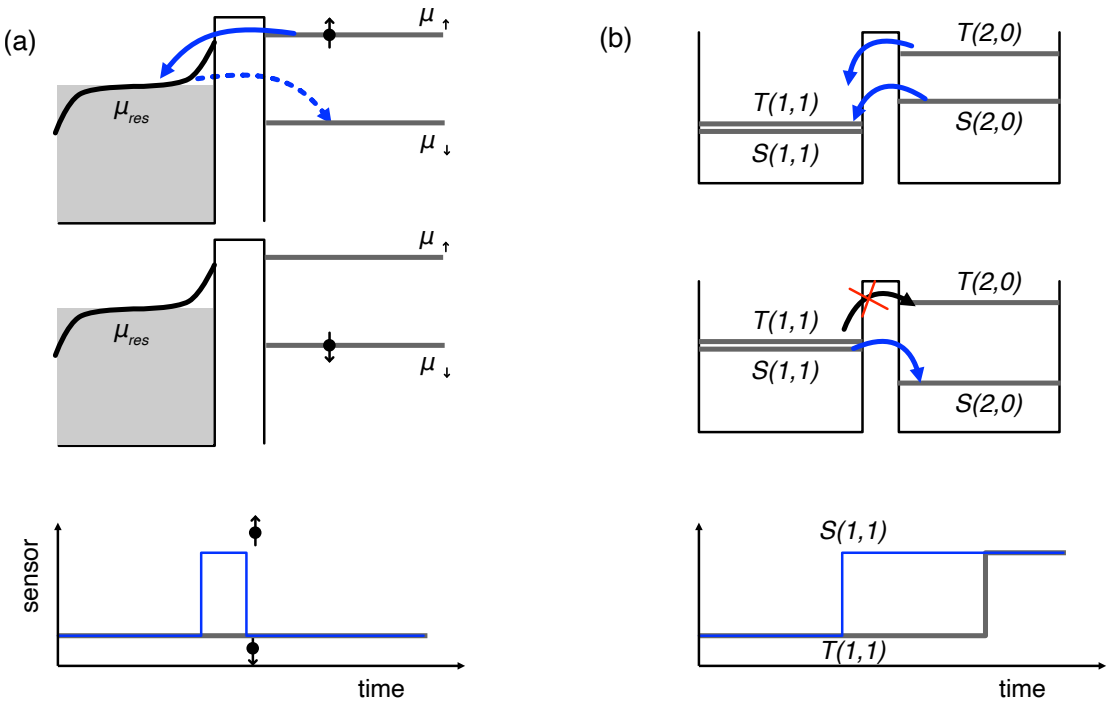


Figure 2.11 (a) the readout method based on Spin-selective tunnelling. (b) the readout method based on Pauli spin blockades.

Pauli spin blockade: In the DQD system, the spin state can be measured without the exchange with the reservoir by the Pauli spin blockade. At the detuning where (1,1) state is the ground state, both $T(2,0)$ and $S(2,0)$ state can transition to (1,1) state. While a detuning where the $S(0,2)$ state is ground

state, the $S(1,1)$ state transitions to $S(0,2)$ via elastic tunnelling, while the $T(1,1) - T(2,0)$ state remains blocked due to the orbital energy but can be lifted after spin relaxation time. This delayed charge transition can be monitored in the sensor signal and used to measure the spin state between $S - T$ or single spin state in the target QD.

2.4 Gate-based RF readout

Following the successful implementation of RF-QPC [109, 110], RF-SET [101, 111], gate-based RF sensors is developed and provided to be a compact, sensitive readout method and can be implemented in a scalable way for readout of spin qubits [112]. Unlike the previous RF techniques requiring the extra nanostructure (QPC or SET), the gate-based RF sensors read out the signal dispersively through a resonant circuit which connects to one of the gates near the QD. The reflection mode of RF readout is used in this thesis. The transmission mode of gate-based sensing can be found in reference: [113, 114]. In the gate-based configuration, the device capacitance has two main components: the geometric capacitances which comes from geometric capacitances in the nanostructures and voltage independent, and the parametric capacitances which comes from electron tunnelling event in the device. This parametric capacitance includes an electron charge tunnel induced tunnel capacitance and a state-dependent 'quantum capacitance' at the dispersive regime where the resonator and two level system are detuned [115, 116]. The gate-based sensing is centred around the voltage-dependent parametric capacitance C_{para}. It is implemented in the following two scenarios: **cyclic electron tunnelling between the QD and reservoir** and **inter-dot electron tunnelling between DQD** corresponding respectively to dot-reservoir transition (DRT) and inter-dot transition (IDT) in stability diagram.

2.4.1 Tunneling between the QD and reservoir

Consider a QD system coupled to reservoir and the gate, the gate can control the effective gate n_g in the QD. Figure 2.12 shows the energy diagram of QD at

the degeneracy point ($n_g = 0.5$), the QD is represented by the two-level system with levels E_0 (dot empty) and E_1 (dot occupied). The RF signal with amplitude $\delta n = C_g V_g^{RF}/e$ can drive the two-level system at f_0 across the inter-dot transition. When fast RF signal moves the system to the right of the degeneracy point, the excess energy $E_0 - E_1$ is then captured as a change in the resistance (Sisyphus resistance: R_{sis}) of the device during the inelastic relaxation process γ_- [117]. And time averaged charge $\langle ne \rangle$ with the RF signal cycle leads to the parametric capacitance $C_{para} = \partial \langle ne \rangle / \partial \varepsilon$ [62].

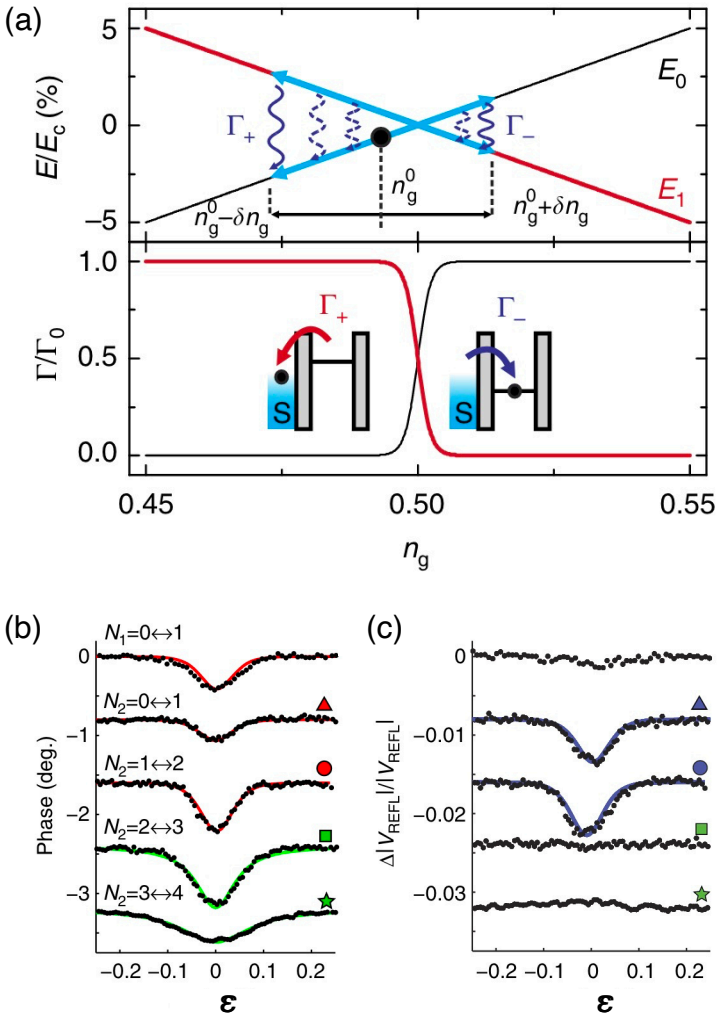


Figure 2.12 (a) Energy detuning diagram of the QD tunnel-coupled to a reservoir, and the QD tunneling rate from E_0 to E_1 at the degeneracy point. Phase (b) and magnitude (c) response of the resonator as a function of the detuning at different QD electron occupation. Adated from [62, 118]

Consider the reservoir density of states has a probability distribution dependent on effective temperature T_e. γ_0 is the constant tunnel rate far from the degeneracy.

The corresponding tunnel rates $\gamma_\pm$ in Figure 2.12(a) is:

$$\gamma_\pm = \frac{\gamma_0}{1 + e^{\pm \Delta E / k_B T_e}} \tag{2.25}$$

At **low tunnel rate** where $h\gamma_0 < \omega_0$, the capacitance C_{para} and Sisyphus resistance R_{sis} are given by [62, 118]:

$$C_{\text{para}} = \frac{e^2\alpha^2}{4k_B T_e} \frac{1}{1 + \omega_0^2/\gamma_0^2} \cosh^{-2}\left(\frac{\varepsilon}{2k_B T_e}\right) \tag{2.26}$$

$$R_{\text{sis}} = \frac{4k_B T_e}{e^2\alpha^2} \frac{1 + \gamma_0^2/\omega_0^2}{\gamma_0} \cosh\left(\frac{\varepsilon}{2k_B T_e}\right) \tag{2.27}$$

The value of dissipation is measured by reflection of signal shown in Figure 2.12(c). This signal is maximized at $\gamma_0 = \omega_0$ and tends to zero (eg. infinite Sisyphus resistance) for both $\gamma_0 \ll \omega_0$ (no charge movement) and $\gamma_0 \gg \omega_0$ (tunnel too fast to be captured), as dissipation is minimised. The same hold for tunnelling capacitance for $\gamma_0 \ll \omega_0$ but at $\gamma_0 \gg \omega_0$ dependent on T_e. When $h\gamma_0 \ll k_B T_e$, the full-width half maximum (FWHM) of the signal is dominated by the effective electron temperature, given by the equation $\varepsilon_{1/2} = 4\ln(\sqrt{2}+1)k_B T_e$, which allows for the primary thermometry experiments [119] to measure the electron temperature of the device. This technique is further discussed in the experiment of Chapter 5.

At **high tunnel rate** where $h\gamma_0 > \omega_0$, the probability of the excess charge in the QD due to tunnelling is the integral of the product of tunnel-broadened states $n_t(\varepsilon) = \frac{1}{\pi}\frac{\hbar\gamma_0}{(\hbar\gamma_0)^2+\varepsilon^2}$ and Fermi-Dirac distribution of electrons states $f(\varepsilon)$ in reservoir [120]. As a result the tunneling capacitance is the propotional to convolution of the two functions as:

$$C_{\text{para}} = e\alpha(f(\varepsilon) * n_t(\varepsilon))' = e\alpha(f(\varepsilon)' * n_t(\varepsilon)) \tag{2.28}$$

When $h\gamma_0 \gg k_B T_e$, as seen in Figure 2.12(b) in transition $N_2 = 2 \leftrightarrow 3$ and $3 \leftrightarrow 4$, electron tunnelling occurs elastically and out of phase with the drive and only produces a capacitive conponents:

$$C_{\text{para}} = \frac{e^2\alpha^2}{\pi} \frac{\hbar\gamma_0}{(\hbar\gamma_0)^2 + \varepsilon^2} \tag{2.29}$$

This can be seen as an extren condition of Equation 2.28 where Fermi-Dirac distribution is approximated as step function. And the FWHM of the signal is $\varepsilon_{1/2} = 2h\gamma_0$, from which the tunnel rate can be directly extracted.

The RF response of single QD coupled to reservoir can be used to directly readout in-situ electron occupation or utilised as the charge sensor similar to SET. Compared with the other charge sensors in which transport is necessary, the gate-based sensor is more compact for it only requires a single reservoir. This also leads to a different noise spectral density limited by Sisyphus noise [62]. The gate-based sensor in this configuration is referred as single electron box (SEB) [117] and used as single lead quantum dot (SLQD) sensor [121, 122].

2.4.2 Inter-dot tunnelling between DQD

The Sisyphus resistance and tunnelling capacitance in the DQD system can be expanded by looking at the gate capacitively coupled to both of the QD, the parametric capacitance is then dependent on both of the time-averaged excess electron numbers:

$$C_{\text{para}} = -e\left[\alpha_2 \frac{\partial \langle n_2 \rangle}{\partial V_g} + \alpha_1 \frac{\partial \langle n_1 \rangle}{\partial V_g}\right] = -e\alpha' \frac{\partial \langle n_2 \rangle}{\partial V_{\text{g}}} \tag{2.30}$$

with $\langle n_1 \rangle$,$\langle n_2 \rangle$ being the time-aver charge on QD1 and QD2. Since $\langle n_1 \rangle$ = -$\langle n_2 \rangle$ when QDs exchange electrons and the gate on inter-dot transistion level arm is $\alpha' = (\alpha_2 - \alpha_1)$ [116]. The time-averaged charge is expressed as :

$$\langle n_2 \rangle = \langle n_2 \rangle_- P_- + \langle n_2 \rangle_+ P_+ \tag{2.31}$$

where $P_\pm$ are the probabilities of the excess electron occupying the ground(-) or excited(+) state and $\langle n_2 \rangle_\pm$ are the average number of electrons in QD2 in the ground and excite state:

$$\langle n_2 \rangle_\pm = \frac{1}{2}\left(1 \pm \frac{\varepsilon}{\Delta E}\right) \tag{2.32}$$

And the parametric capacitance of a double quantum dot is obtained with $\Delta E = E_+ - E_- = \sqrt{\varepsilon^2 + \Delta_c^2}$ from Equation 2.19:

$$C_p(t) = \frac{(e\alpha')^2}{2\Delta_c}\Big(\underbrace{\frac{\Delta_c^3}{\Delta E^3}\chi_c}_{\text{quantum}} + \underbrace{\frac{\varepsilon\Delta_c}{\Delta E}\frac{\partial\chi_c}{\partial t}\frac{\partial t}{\partial\varepsilon}}_{\text{tunnelling}}\Big) \tag{2.33}$$

where $\partial\chi_c = P_- - P_+$. This parametric capacitance contains two parts that are detuning-dependent: the quantum capacitance which originates from the diabatic charge transitions and the finite curvature of the energy band [123] and and tunnellling capacitance arises from non-adiabatic processes, such as relaxation and thermal or resonant excitation.

The Sisyphus resistance and tunnelling capacitance is given:

$$C_t = \frac{(e\alpha')^2}{4k_BT_e}\left(\frac{\varepsilon}{\Delta E}\right)^2 \frac{1}{1+\omega_0^2/\gamma_0^2}\cosh^{-2}\left(\frac{\Delta E}{2k_BT_e}\right) \tag{2.34}$$

$$R_{sis} = \frac{4R_Qk_BT_e}{h\alpha'^2}\left(\frac{\Delta E}{\varepsilon}\right)^2 \frac{1+\gamma_0^2/\omega_0^2}{\gamma_0}\cosh\left(\frac{\Delta E}{2k_BT_e}\right) \tag{2.35}$$

From the temperature dependent time average charge, the quantum capacitance

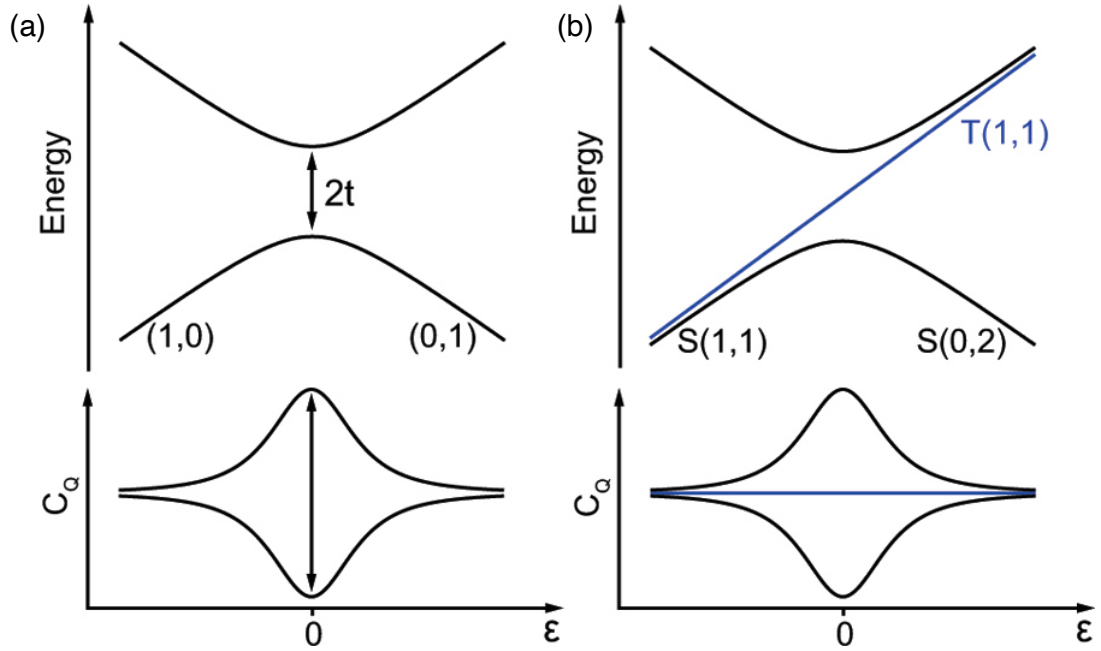


Figure 2.13 (a) energy diagram for (1,0)-(0,1) DQD with hybridized charge state and quantum capacitance as a fucntion of detuning. (b)energy diagram for (1,1)-(0,2) DQD with eigenstate of singlet and triplet and quantum capacitance as a fucntion of detuning. Adated from [124]

has been discussed with Sisyphus resistance and tunnelling capacitance in the same framework with a small-signal equivalent model [116]:

$$C_{\mathrm{q}} = \frac{e^2\alpha'^2}{2}\frac{\Delta_c^2}{\Delta E^3}\tanh\left(\frac{\Delta E}{2k_B T_e}\right) \tag{2.36}$$

Quantum capacitance is the essential components to differentiate the signal between singlet and triplet in the DQD system as shown in Figure 2.13. For charge hybridized state $E_{C_\pm}$ and singlet hybridized state $S(1,1)-(2,0)$, C_{q} have a finite value due to the non-zero curvature of the energy band. For triplet eigenstate $T(1,1)$, the $C_{\mathrm{q}} = 0$. This will be further discussed in Chapter 7.

Chapter 3

Experimental methods

This Chapter introduces techniques for fabrication and experimental characterisation of silicon nanowire devices. This consist of a section focused on fabrication processes for the devices developed at CEA-Leti and VTT[1]*, a section on the experimental methods and setup for device characterisation*

3.1 Silicon nanowire fabrication

A quantum dot requires confinement in all three dimensions. In GaAs and SiGe platforms, QD is achieved by the lateral heterostructure and depletion gating electrode. In planar silicon-metal-oxide-semiconductor(SiMOS) structure, QD is achieved by carefully designing multi-layered accumulation gating electrodes. Qubit readout and control have been recently demonstrated in a silicon nanowire(SiNW) device based on fully-depleted silicon-on-insulator (FD-SOI) technology fabricated at research foundry [125, 126]. Benefiting from the physical dimensions, SiNW offers natural confinement in the transverse and vertical direction of the channel. Therefore, the gating electrode complexity can be significantly reduced in a large scale device. Figure 3.1(a)(b) shows the single omega-shape gate wrapping around the SiNW and source/drain contact after the back-end process.

This thesis studied three types of SiNW devices: split-gate SiNW, bismuth-

[1]The author would like to thank every member from European project MOS-QUITO who made the collaboration possible, especially Silvano De Franceschi and Louis Hutin at CEA-Leti, Janne Lehtinen and Mika Prunnila at VTT.

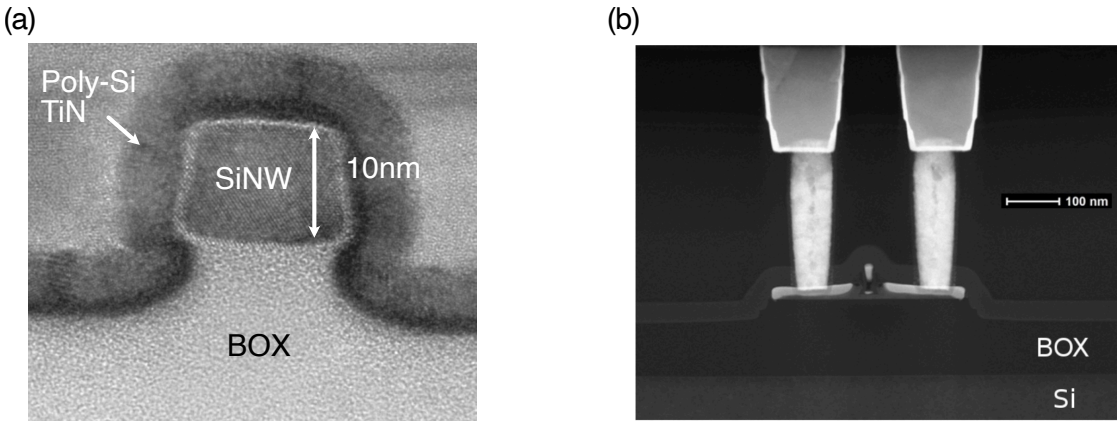


Figure 3.1 (a) Transmission electron micrograph(TEM) of the cross section of the SiNW. (b) TEM of the device after back-end process. Image courtesy, CEA Leti, Grenoble [125].

doped SiNW and ambipolar SiNW. Here simplified version of each fabrication process is presented to help understand important details of the devices.

3.1.1 Split-gate SiNW

In a SiNW field effect transistor device, separate QDs form at the edge of the cross-section due to an increased electric field at the corner. Inspired by the formation of such corner QDs, a split-gate design is proposed to have individual control of these QDs. This part introduces the fabrication process based on the FD-SOI fabrication process to achieve individual control of corner QDs in the SiNW channel. Deep ultraviolet(DUV) lithography and electron beam(e-beam) lithography are used in this fabrication.

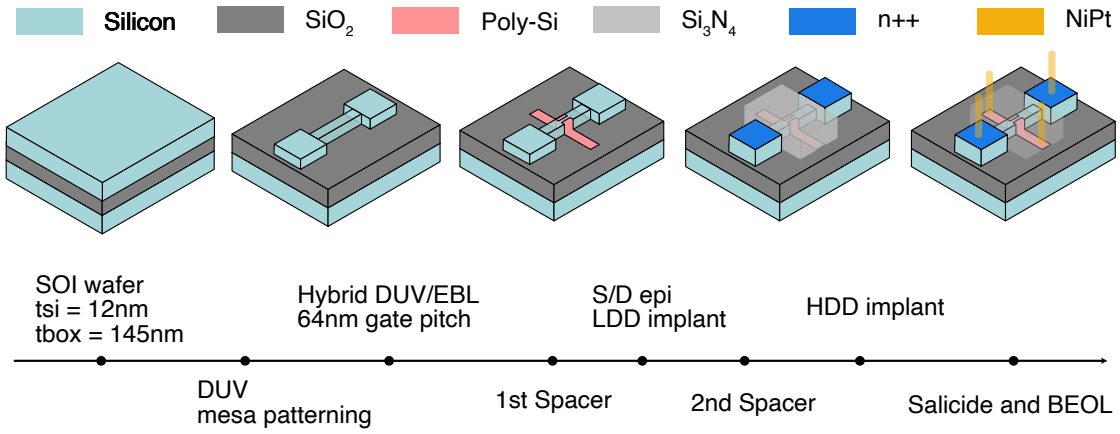


Figure 3.2 overview of the Split-gate SiNW fabrication process.

Starting from the 300 mm SOI wafers shown in Figure 3.2, the main

fabrication steps of the split-gate SiNW are 1. DUV mesa patterning, 2. hybrid DUV/e-beam gate deposition and patterning, 3. spacer deposition and source/drain implantation, 4. salicided contact and back end of line process for all electrodes. The 300 mm SOI wafers include 12 nm silicon on 145 nmm buried oxide(BOX). The active mesa patterning is achieved with DUV. Nominal width of 80 nm can be obtained from the 193 nm DUV process. It then follows the thermal oxidation and gate deposition process and leads to a MOS gate stack consisting of 6 nm SiO_2, 5 nm TiN and 50 nm polycrystalline silicon(Poly-Si). In order to achieve a 64 nm gate pitch, a hybrid DUV/e-beam scheme is developed to balance the advantage of speed and precision. The whole process consist of one DUV cycle and additional two e-beam cycles and follows a "Litho/Etch(DUV)-Litho/Etch(e-beam)-Litho/Etch(e-beam)" scheme as shown in Figure 3.3.

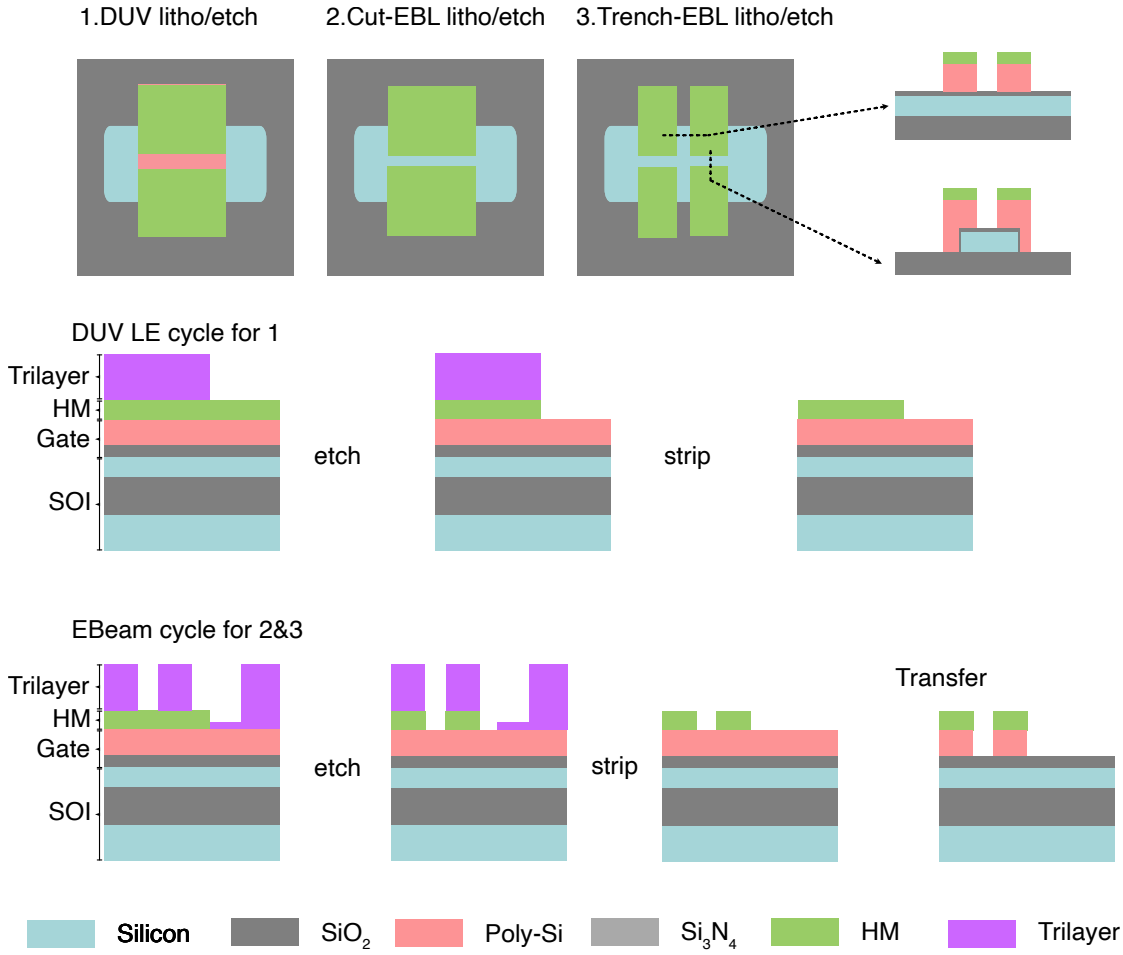


Figure 3.3 overview of the FD-SOI fabrication process.

Before the litho/etch cycle, a hard mask (HM) of SiO_2 and Si_3N_4 is deposited

on top of the Poly-Si gate. Then a trilayer (from top to bottom) of positive polarity photoresist, Si-rich anti-reflecting coating and spin-on carbon is used for lithography, as shown in Figure 3.3. This trilayer leverages a good Si_3N_4:spin-on carbon selectivity and uses a partial recess of the spin-on carbon layer in order to leave the top of the hard mask exposed while the Poly-Si protected. Both the photosensitive and electrosensitive photoresists are of the same positive polarity. The three litho/etch steps use DUV to define the active area for gate patterning, the first e-beam to create the gate split along the SiNW, and the second e-beam to create the trench between the two parallel gates.

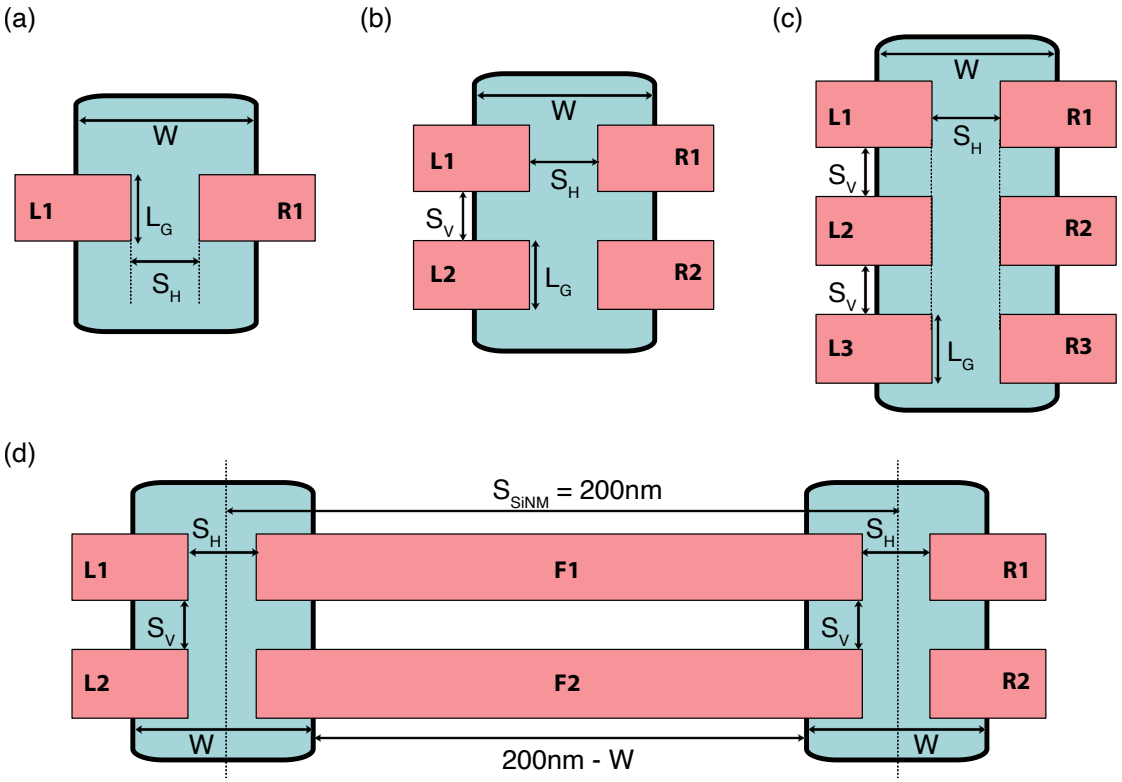


Figure 3.4 Top view of the relevant dimensions indicated for four type of split gate devices: (a) Single pair split gate device (1S-xxx) . (b) Double pairs split gate device (2S-xxx) . (c) Three pair split gate device (3S-xx). (d) Floating gate coupled split gate device(FL-xx). S_V: spacing between vertical parallel gates, S_H spacing between face-to-face gates, L_G: length of gate along the SiNW, W: width of SiNW, S_{SiNW}: spacing between two SiNW.

Then the first spacer of 34.5 nm Si_3N_4 is deposited to protect the intrinsic silicon from the ion implantation, which defines the source/drain reservoirs. This Si_3N_4 spacer also covers the split and trenches among the gates to offset phosphors dopants from the gate-defined QDs and inter-QD spacing from doping. Selective epitaxy raised the source/drain MESA for self-aligned lowly-doped drain(LDD) ion

implantation. The hard mask is only removed before starting the second spacer and highly-doped drain(HDD) ion implantation. Finally, the doped Poly-Si Gate and reservoir react with NiPt to form NiPtSi for self-aligned silicidation.

Table 3.1: Summary of the split gate SiNW device's dimension.

Device Key	L_G(nm)	S_V(nm)	S_H(nm)	W(nm)
1S26D	40	40	-	70
2S132	50	50	40	70
2S121	60	60	50	80
2S122	50	50	50	80
3S14	40	40	40	80
FL22	60	60	50	80
FL25	50	50	50	80

This process produces about 300 different designs in each die. The final device has a 7 nm silicon layer on 145 nm BOX with a gate stack of SiO_2(6 nm)/TiN(5 nm)/Poly-Si(50 nm). The width of the SiNW W ranges from 70 nm to 100 nm. The face-to-face split gate is symmetrically located on both sides of SiNW by design with the spacing S_H. As a result, the active gate-SiNW overlapping width is $(W - S_H)/2$. The overlapping width defines the active QD formation area together with the gate length L_G along the SiNW. The vertical spacing between parallel gate in the top view of device schematic in Figure 3.4 is S_V. The typical gate spacing and gate size values are 40 nm, 50 nm, and 60 nm. In this thesis, the physics of quantum dot's shape is not investigated. The choice of gate spacing and size is mainly used to study the dependece of distance on capacitance network model in Chapter 6. Figure 3.4(a-d) shows the top view of the relevant dimensions indicated for four types of split-gate devices. They are single pair split gate (L1, R1) devices with device key 1S-xxx, double pairs split-gate devices (2S-xxx), three pair split-gate devices (3S-xx), apart from the single SiNW device that can scale in one dimension with multiple pairs of split gates. Another floating gate device couples two SiNW with the floating gate(F1, F2) and split gates on the side of each SiNW(L1, L2, R1, R2). The centre-to-centre spacing between two SiNW is 200 nm. The key dimensions is summarized in Table 3.1.

3.1.2 Bismuth doped SiNW

Besides a gate-defined quantum dot, silicon's dopant or dopant cluster has been another primary experimental platform for quantum computing. This part introduces a modified process based on the split-gate SiNW fabrication process to achieve localised dopants in the SiNW channel. The experiments related to this type of device are discussed in Chapter 7.

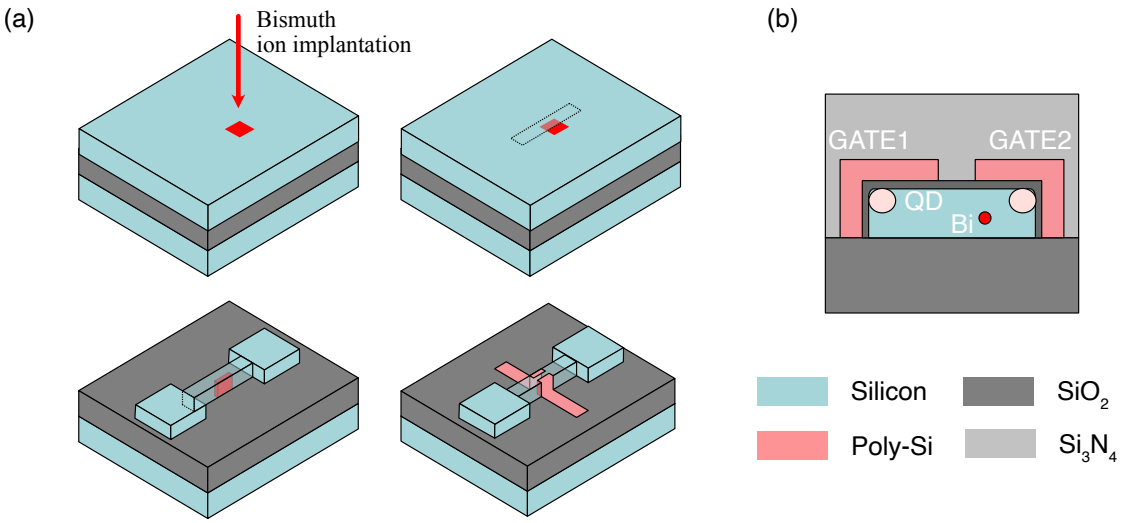


Figure 3.5 (a) simplified fabrication process for Bi doped SiNW. (b) cross section schematic of the final gate stack illustrating the formatin of gate-defined quantum dots and single bismuth dopant.

Different from the split-gate process, ion implantation precedes the SiNW patterning. Figure 3.5(a) illustrate simplified process of the modified process. The first step is thermal oxidation of the SOI layer that targets 4 nm oxide for the e-beam marks patterning. This 4 nm of thermal oxide preserved on the wafers prepares the stopping layer for later Bi ion implantation. An e-beam lithography step is then performed to define windows for silicon channel doping. Bi ion is implanted through the 4 nm of oxide(not shown) within the photoresist-defined windows in Figure 3.5(a). Importantly, the implantation window is designed in the relative position of the later SiNW and gate patterning, where it only allows one side of SiNW to be doped. The bismuth doping concentration targets at 6.25×10^{10} atom/cm^2 to achieve an average of a single bismuth atom under each gate. After the ion implantation process, the 4 nm of thermal oxide is removed and replaced by 2.5 nm plasma-grown

oxidation. The later SiNW patterning, gate patterning and S/D implantation follow the same process mentioned in the previous section 3.1.

The final device delivers an active doping area under one side of the split gates. The cross-section of the SiNW in Figure 3.5(b) shows the gate stack and illustrates the formation of gate defined quantum dots and a single bismuth dopant in the SiNW channel.

3.1.3 Ambipolar SiNW

This part introduces the devices fabricated on 150 mm SOI wafers with a customised CMOS process at VTT Micronova cleanroom facilities. The experiment related to this type of device is discussed in Chapter 4 and 5.

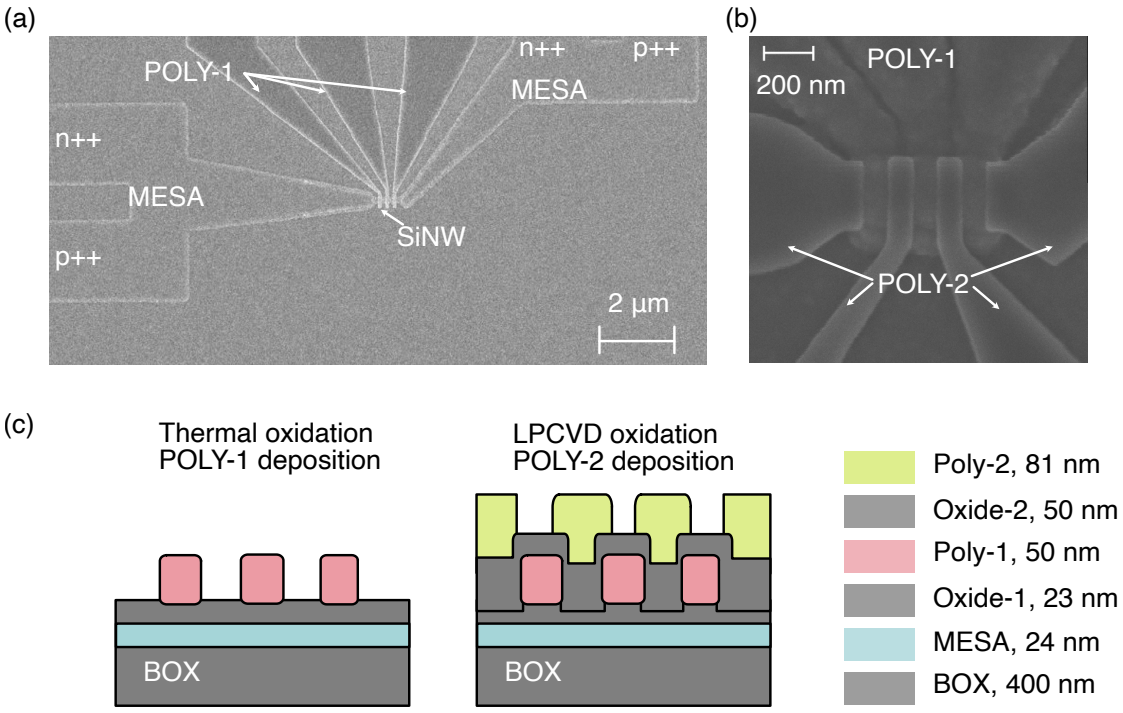


Figure 3.6 (a) Scanning electron microscopy(SEM) image of device after Poly-1 layer deposition and patterning. (b) SEM image of device after Poly-2 layer deposition and patterning. (c) cross section schematic of the device and gate stack

The SOI layer is thinned down to 35 nm (MESA) by thermal oxidation and oxide stripping and patterned to form the nanowires with ultraviolet (UV) and e-beam lithography. Figure 3.6 (a) shows the overall MESA and centre SiNW for formation of quantum dots. A 20 nm thermal SiO_2 is grown to provide the insulator between the SiNWs and the first gate layer. This step reduced the Si

layer to its final thickness of 24 nm. The first and second Poly-Si gate layers, Poly-1 and Poly-2, have 50 nm and 80 nm gate thickness and are degenerately doped with low energy phosphorous ion implantation. Figure 3.6 (b). From van der Pauw structures, we measured the room temperature resistivities of Poly-1 and Poly-2 thin films to be $\rho_1 = 1.14 \times 10^{-2}\,\Omega \cdot \mathrm{cm}$ and $\rho_2 = 1.9 \times 10^{-3}\,\Omega \cdot \mathrm{cm}$. The 35 nm thick SiO_2 dielectric layer between the polysilicon gate layers is grown by low-pressure chemical vapour deposition(LPCVD). Openings through the deposited dielectrics are etched on the source/drain regions (as shown in Figure 3.6(a)) of the MESA. And phosphorous (n ++) or boron (p ++) implantation is used to dope these regions. The shape of extended MESA allows connection from both of 'n++' and 'p++' regions to join SiNW, which serves as an extension of the reservoir. A 250 nmm thick SiO_2 is deposited with LPCVD, and the wafers are heated to 950 °C to activate the dopants and anneal the dielectrics. Contact holes for all three layers are etched with subsequent dry and wet etching processes. Finally, the BEOL is done with a metallisation layer consisting of 25 nm TiW and 250 nm AlSi, and the wafers are treated with a forming gas anneal passivation. The whole process consisted of eight UV and three e-beam lithography layers.

The cross-section of device and its gate stack is shown in Figure 3.6 (c). Poly-1 gates wrap around the SiNW with thermal oxide Oxide-1 in between. Oxide-2 thickness consists of the thermal oxide and LPCVDs grown integrated oxide between the Poly-2 gate and the MESA.

3.2 Experimental setup

The experiments performed on the device in this thesis are mostly done at cryogenic temperature. Connections are established to send and read out the signal. This section introduces various control and measurement electronics at different signal route stages, including the cryostat, circuit, and related active and passive components.

3.2.1 Cryostat wiring

The low-temperature results presented in this thesis is measured in two dilution refrigeration system BlueFors LD400 and BlueFors XLD in UCL QUES2T Lab[2]. Both cryostat systems use the bottom loading sample puck to hold the test device. LD400 system has the superconducting magnet[3] with a base temperature of 19 mK. XLD system has no magnet and a base temperature of 8 mK. The wiring of our cryostat is presented in the figure 3.7. It starts from the input connection at the room temperature ($T = 300$ K) to the coldest part of the system where the device sits. The good practice of wiring for dilution refrigeration system from scratch can be found in [127–129]. Here only describe the details of the low-frequency line and high-frequency line in the cryostat.

Low-frequency lines uses twisted pairs arranged in a loom (24-lines) made from constantan (4 K electronics) and PhBr for low thermal conductivity. These looms are thermalised at multiple stages (50 K, 4 K, 800 mK,100 mK) of the Dilution Refridgerator and filtered at the mixing chamber(MXC). Low pass filtering for this line is performed with commercially available QDevil-QFilter using multi-stage 7-pole π-filters ($f_c > 80$ MHz) and two-stage RC filter ($f_c > 130$ kHz) with an isolation to the ground and other channels > 2 GΩ. The Low-frequency lines are distributed via microD connectors/cables to the sample puck and the printed circuit board (PCB). Further filtering is implemented on the PCB.

High-frequency lines are implemented with semi-rigid coaxial cables that carry signals up to 18 GHz (SMA connectors) or 40 GHz (k-type connectors). The different stage at cryostat has different thermal budget. As a result, as shown in Figure 3.7, CuNi is chosen for control signal lines at stages below 4 K and superconducting Nb(Ti) is chosen for readout lines for the benefit of minimal signal loss. Stainless steel wiring is used for 300 K to 4 K for the reduced thermal conductivity at the cost of increased losses. The typical gate-based RF readout setup consists of the input drive and return signal lines. The attenuated drive signal first passes through the 1 GHz low pass filter (Minicircuit-VLF-1000+) at the MXC stage and then feeds into the coupler port of a cryogenic directional

[2]The author acknowledge help from Dr.Christoph Zollitsch, Dr. Michael Fogarty, and Dr. Simon Schaal for the installation of wiring and maintenance of the dilution refrigeration system

[3]6 Tesla primary coil in the z-direction with the persistent mode option

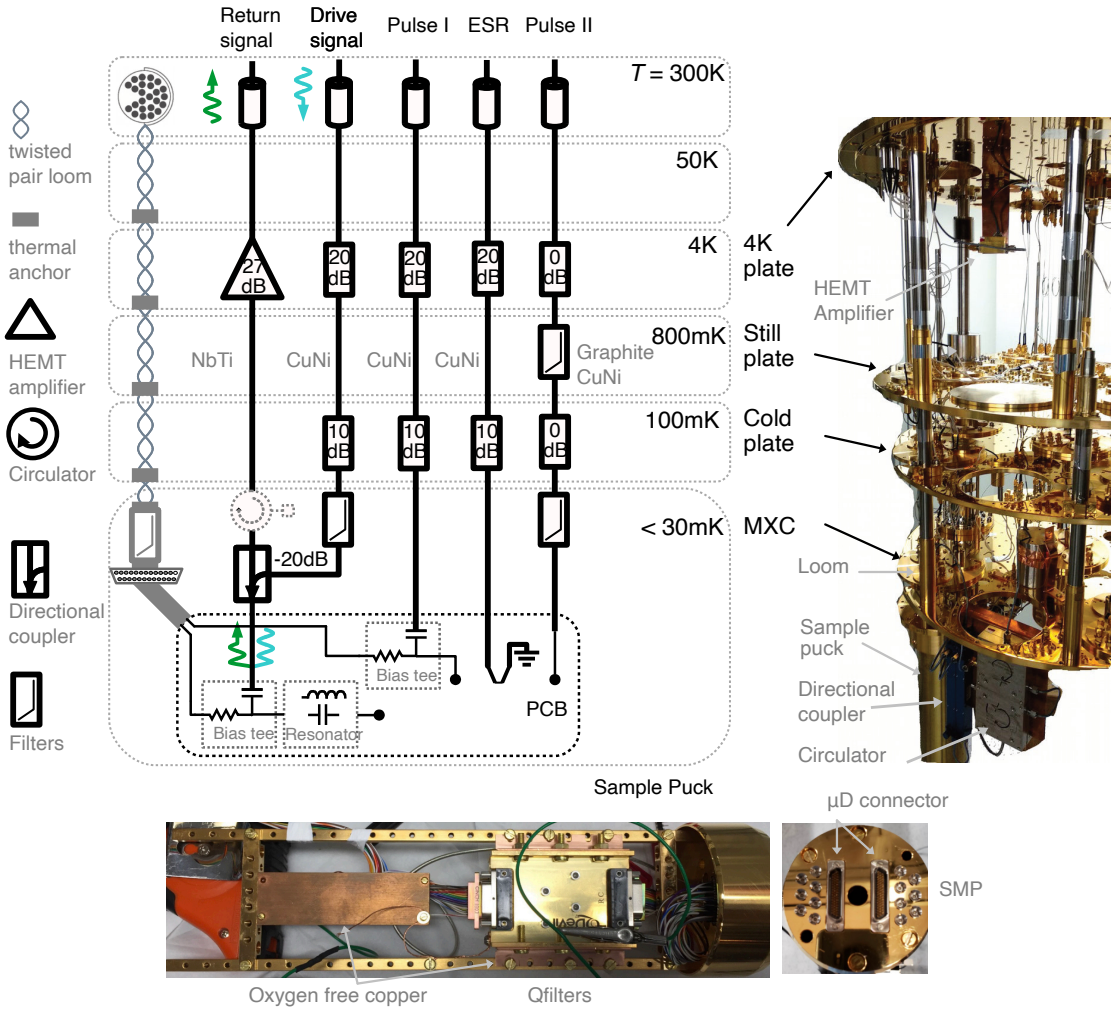


Figure 3.7 Wiring of dilution refridgeration with line schematic and actual picture of the system and components highlighted. This consists of the typical RF readout setup of drive and return signal line, and pulse and ESR lines for qubit control. Line schematic adapted from [129]

coupler (Krytar 158020-810). After reaching the gate of the device, it bounces back through the through" port. The circulator (Quinstar QCY-007020UM00, μ-metal shielded) is optional for Josephson parametric amplifier (JPA) to remove the leakage of JPA pump signal to device [130] and also provide sound isolation of the leakage from the return line. The return signal is amplified at the 4 K stage by the HEMT (Low noise factory-LNC0.6-2A) before feeding into the room-temperature electronics. Control pulses (Pulse I) can be delivered from the high-frequency line which joins the low-frequency line at the on board Bias-tee. A low-noise, low-frequency control pulse (Pulse II) could use the 0dB attenuators for thermalisation and flexible graphite-CuNi cables which benefit from the material's intrinsically large attenuation at high-frequency [131]. The ESR line is connected to shorted waveguide on the chip to generate strong ac magnetic fields for the ESR experiment. All the high-frequency lines are distributed via SMP connectors/cables to the PCB.

3.2.2 Measurement setup

Low-temperature transport measurements are performed with three methods: 1. Keithley 2400 source-meter for simple I-V scan; 2. through a current preamplifier (SR570) followed by voltage meter; 3. lock-in amplifier (SR830). Gate voltages are supplied using a voltage generator system (QDevil-QDAC). Other Simple waveforms are supplied using arbitrary waveform generators (AWG, Keysight 33522B).

Reflectometry: Room-temperature microwave components are used to send the 'drive' into and pick up the 'return' signal from the cryostat as shown in Figure 3.8. This room-temperature setup is made of seperate microwave components for homodyne detection based on IQ demodulation. For normal operation of reflectometry, a fixed frequency RF signal is generated from the signal generator(Rohde & Schwarz SMB 100A) and fed to a directional coupler (Minicircuit ZX30-17-5-S+) which splits the signal towards the LO port of the demodulator (Polyphase Quadrature Demodulator AD0540B) and towards the cryostat. After the drive signal reaches the QD device, the reflected RF signal goes through two room temperature amplifiers (Minicircuit ZX60-112 LN+) and

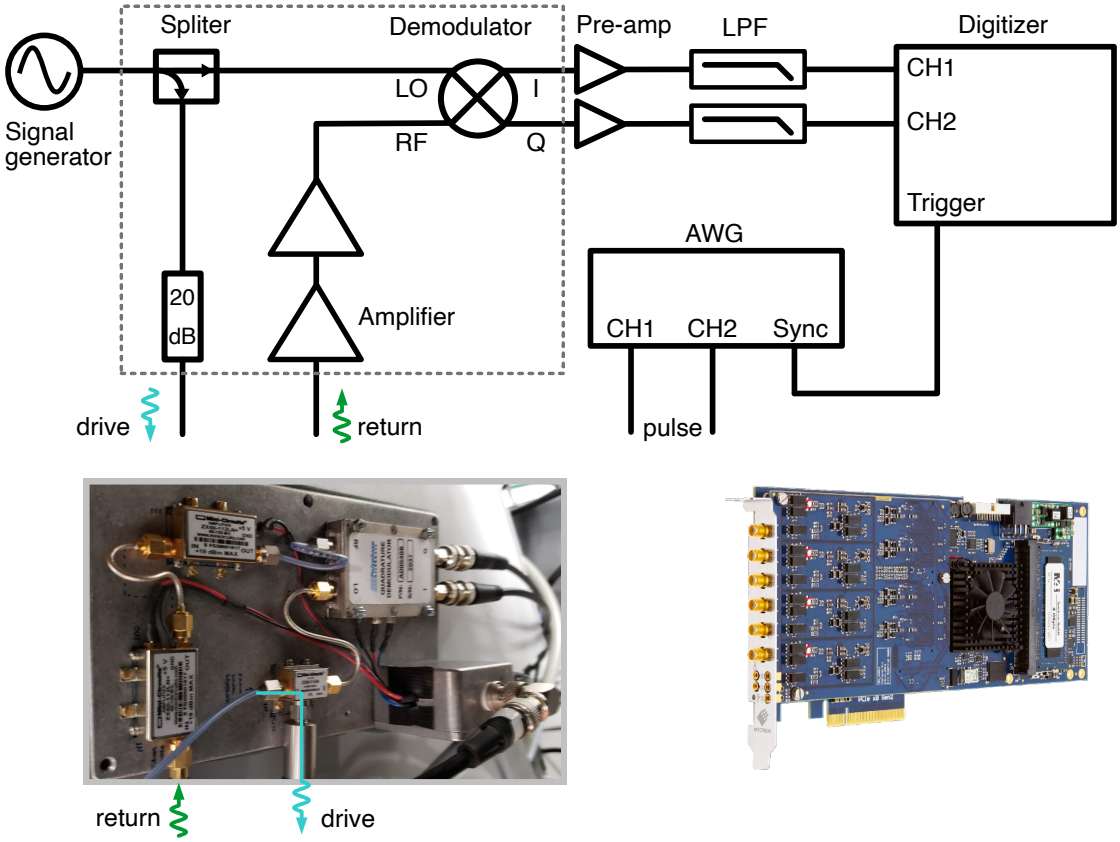


Figure 3.8 The reflectometry circuit consisting of the frequency source, low noise amplifier, demodulator and data acquisition instrumentation for homodyne detection.

feeds into the same demodulator's RF port. The returned RF signal is mixed with the local oscillator signal (LO) both in-phase $\cos(f_{\mathrm{LO}})$ and 90°-shifted $\sin(f_{\mathrm{LO}})$ at the demodulator. The perfect mixing of the signals follows the relations below:

$$A\cos(f_{\mathrm{LO}})\cos\left(f_{\mathrm{RF}}+\phi\right)) = \frac{A}{2}\left(\cos\left(f_{\mathrm{LO}}+f_{\mathrm{RF}}+\phi\right)+\cos\left(f_{\mathrm{LO}}-f_{\mathrm{RF}}-\phi\right)\right) \quad (3.1)$$

$$A\sin(f_{\mathrm{LO}})\cos\left(f_{\mathrm{RF}}+\phi\right)) = \frac{A}{2}\left(\sin\left(f_{\mathrm{LO}}+f_{\mathrm{RF}}+\phi\right)+\sin\left(f_{\mathrm{LO}}-f_{\mathrm{RF}}-\phi\right)\right) \quad (3.2)$$

By design, the signal on the 'LO' and 'RF' port of the demodulator are expected to have the same frequency $f_{\mathrm{LO}} = f_{\mathrm{RF}}$. After the low pass filter, which removes the high-frequency signal at $(f_{\mathrm{LO}} + f_{\mathrm{RF}} + \phi)$, only the low-frequency (DC) signal $(V_{\mathrm{I}}, V_{\mathrm{Q}})$ are generated at the in-phase (I) and quadrature (Q) port which could in turn construct the demodulated magnitude V_{R} and phase information ϕ:

$$V_{\mathrm{R}} = \sqrt{V_{\mathrm{I}}^2 + V_{\mathrm{Q}}^2} \quad (3.3)$$

$$\phi = \arctan(\frac{V_{\mathrm{Q}}}{V_{\mathrm{I}}}) \quad (3.4)$$

The demodulated IQ signal is amplified by the preamplifier (SRS560 or Spectrum SPA1231) and filtered by the first order low pass filter (surface-mounted resistor and capacitor on a customised PCB with a tunable range from 10 Hz to 100 kHz). The digitiser card eventually acquires the IQ signal with a 250 MS/s sample rate (Spectrum M4i-4421). The active components are powered by the same benchtop power supply with a clean ground. An arbitrary waveform generator (AWG) is used to trigger the digitiser's data acquisition of I and Q signals during the time of a specific gate voltage ramp. In this way, fast reflectometry measurements can be performed for large gate space of device scan. All the instruments mentioned in this section can be remotely controlled via the python-based data acquisition framework QCoDeS (https://github.com/QCoDeS/Qcodes).

3.2.3 PCB and circuit

Two types of PCB are used in this thesis: the 'Copenhagen' board and the 'QSD' board shown in Figure 3.9(b,c). The 'Copenhagen' board is based on modular interconnect system [132] with a signal board(motherboard), device board(daughterboard) and an interposer as shown in Figure 3.9(b). The motherboard is a mutiple-layered board which includes all the DC and microwave signal interconnects and the filters and bias tees. In total, 48 low-frequency lines and 16 high-frequency lines are hosted in the motherboard. The daughgerboard have space to hold the chip and DC/RF tracks where the bondwire could bond from to connect the chip bondpads. Electrical connections between the signal board and device board are achieved by springy coils of Au/BeCu wire ('Fuzz buttons'[4]) through the holes on the thin plastic of interposer. The 'marlin' daughterboard is designed to be compatible with the interposer connection and at the same time hosting a on-board 1:2 multiplexing circuit (shown in Figure 3.9) for RF readout. A similar circuit is designed at 'QSD' board with relaxed space and matched on-board waveguide. 'QSD' board directly connects from the molex connector to microD connector of the sample puck. The bias-tee and filtering is placed on both side of the board. In order to achieve good thermal contact, all PCBs are tightly mounted onto oxygen-free copper plates which are further connected to the mixing chamber of the dilution refrigerator during the experiments.

Superconducting spiral inductors is proposed to optimized the readout by reducing the self-capacitance. In this thesis, the off-chip superconducting spiral inductors are used limited by the stand-alone packaging of CMOS-QD devices. There are dedicated space on the PCB for the spiral inductors chip. Additional connections between the inductor chip and QD device chip are made with bondwires and PCB tracks as shown in Figure 3.10(b-d). Two batches of superconducting thin film chips are used in this thesis. The first batch contains 45 nm NbTiN thin film on a 2-inch high resistivity silicon wafer diced to 5 mm × 5 mm dies, and the second batch contains 100 nm NbTi on a 2-inch

[4]Custom Interconnects, Fuzz Buttons®, https://www.custominterconnects.com/fuzzbuttons.html

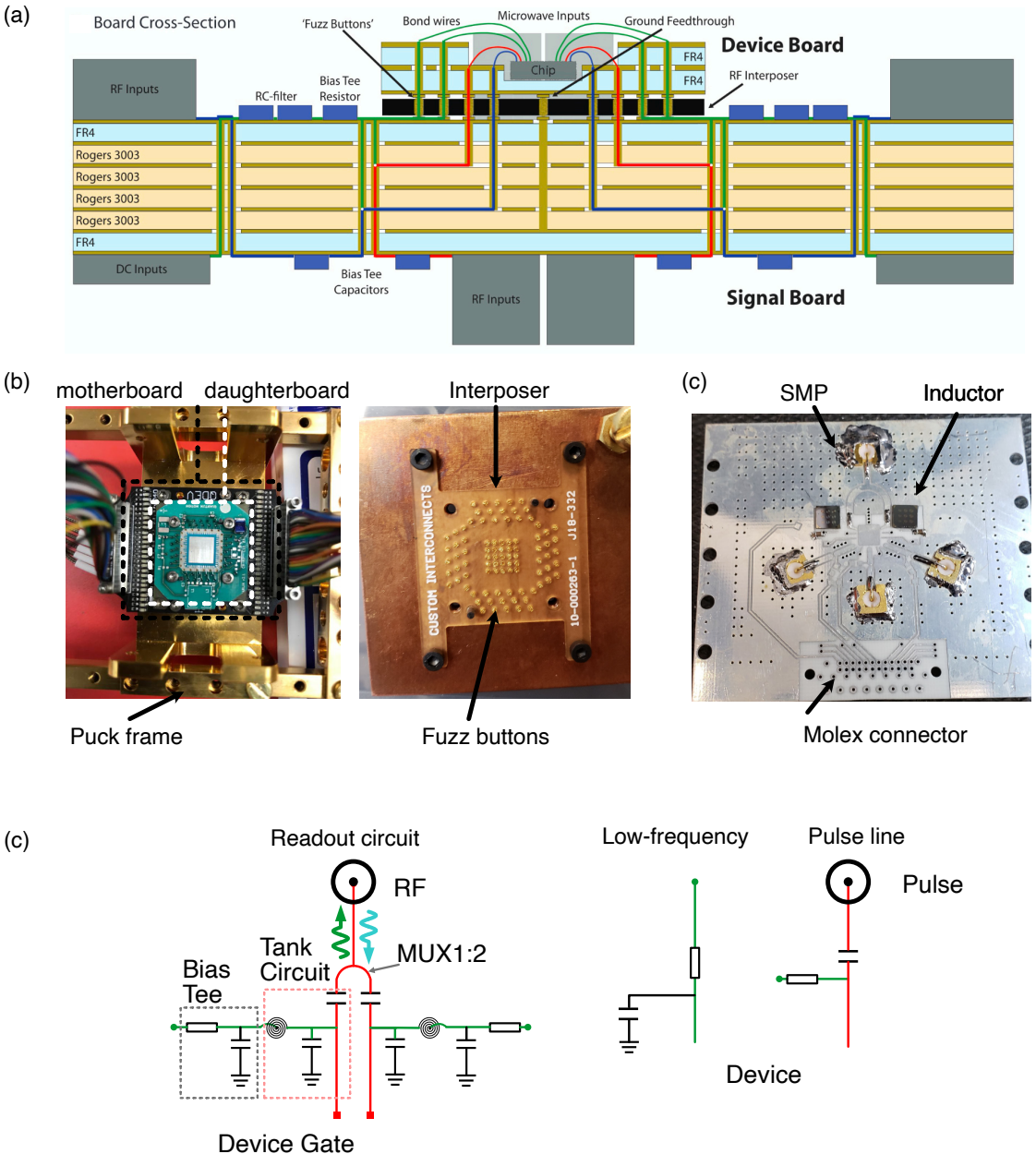


Figure 3.9 (a) schematic of modular interconnect system. Adapted from [132]. (b) pictures of modular system mounted on the frame of sample and a separate interposer on a copper plate. (c) circuit schematic of 'Marlin' daughter board with 1:2 frequency multiplexing.

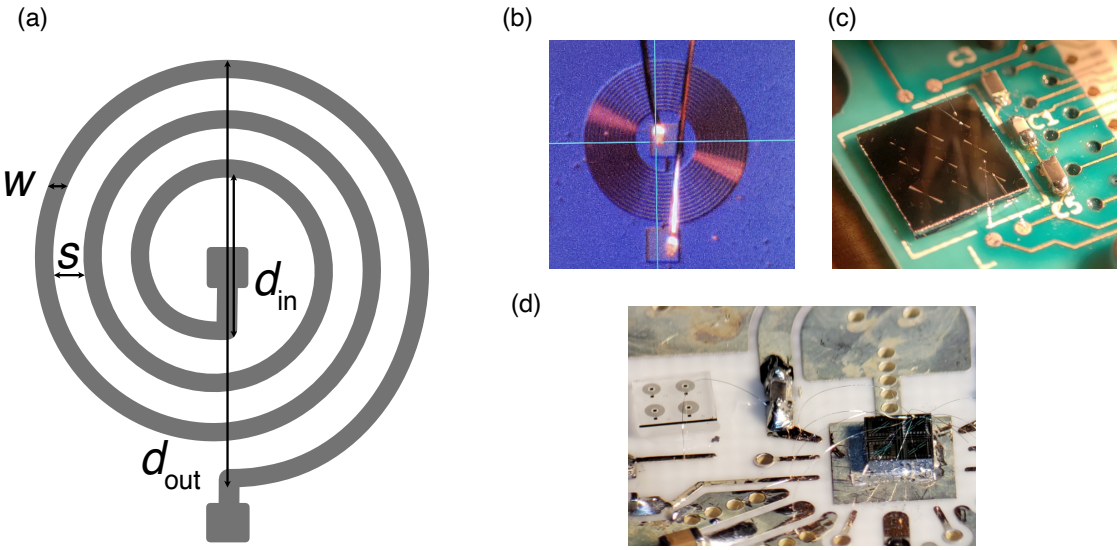


Figure 3.10 (a) schematic of circular spiral inductor with related dimension. (b) microscope image of batch-1 inductor chip. (c) image of batch-1 inductor chip on 'Marlin' daughter board. (d) image of batch-2 inductor chip on 1:2 multiplexing board.

C-plane sapphire, which is diced to 2.5 mm × 2.5 mm dies. The sputtering of both superconducting thin films is done with a commercial service at STAR Cryoelectonics. The patterning of the first batch is designed and fabricated at the LCN cleanroom. The patterning of the second batch is designed by me and fabricated at STAR Cryoelectonics. The total inductance of the spiral inductor is the sum of geometric inductance $L_{\rm geo}$ and kinetic inductance $L_{\rm kin}$. The $L_{\rm kin}$ is unpredictable in the first batch due to the uneven thickness of NbTiN thin film. Therefore, the 100 nm NbTi layer is intended to reduce the kinetic inductance $L_{\rm kin}$ to 0, so a good approximation $L_{\rm spiral} \simeq L_{\rm geo}$ can be used in the design to obatin the desirable inductance.

For a given circular shape, the spiral inductor is specified by the number of track turns: n, the track width w, the track spacing s, which result in the inner diameter $d_{\rm in}$ and outer diameter $d_{\rm out}$ as shown in Figure 3.10(a). A simple, accurate expression based on current sheet approximation [133] is used for simulation of the geometric inductance.

$$L_{\rm geo} = \frac{\mu_0 n^2 d_{\rm avg} c_1}{2} \left(\ln\left(c_2/\rho\right) + c_3\rho + c_4\rho^2\right) \tag{3.5}$$

where μ_0 is the permeability constant in the unit of H/m, the fill ratio ρ describe

how hollow the inductor is and is defined as $\rho = \frac{d_{\text{out}} - d_{\text{in}}}{d_{\text{out}} + d_{\text{in}}}$. The average diameter d_{avg} is defined as $d_{\text{avg}} = 0.5(d_{\text{out}} + d_{\text{in}})$. c_1, c_2, c_3, c_4 are layout dependent coefficients and for circular shape in this case, $c_1 = 1, c_2 = 2.46, c_3 = 0, c_4 = 0.2$ [133].

Chapter 4

Ambipolar quantum dots

In this Chapter, ambipolar gate-defined quantum dots in silicon-on-insulator nanowires are studied. I perform gate-based reflectometry of charge sensing for inter-dot charge transition of both electron and hole double quantum dots, achieving a minimum integration time of 160 (100) µs *for electrons (holes). I then use gate-based primary thermometry to study the electron-phonon and hole-phonon coupling in Chapter 5. These two results present the opportunity to benchmark electron and hole spin qubit and combine the long coherence times of electron spins with the electrically controllable hole spins in silicon in the same device. The relevant theoretical concepts for this Chapter can be found in Section 3.1.3. This work led to the publication:*

- Duan, J., Lehtinen, J. S., Fogarty, M. A., Schaal, S., Lam, M. M. L., Ronzani, A., Shchepetov, A., Koppinen, P., Prunnila, M., Gonzalez-Zalba, F., & Morton, J. J. L. (2021). *Dispersive readout of reconfigurable ambipolar quantum dots in a silicon-on-insulator nanowire.* Applied Physics Letters, 118(16), 164002. https://doi.org/10.1063/5.0040259

4.1 Electron and Hole quantum dots

4.1.1 State of art platforms

The spin degree of freedom of single electrons bound to quantum dots in silicon is considered one of the most scalable candidates to host quantum

information [134]. Rapid progress has been made in electron spin qubit in recent ten years. By isotopic purification of the material, the Hahn-echo coherence time has been extended up to 28 ms [[33]]. Material improvement and research of optimised quantum control enable magnetically-driven single and two-qubit control fidelities of over 99%[[51, 52, 135, 136]]. However, peripheral apparatus like ESR strip-line or micro-magnet are usually used to provide the control of qubit rotation [57]. All-electrical control of spin qubits via the spin-orbit interaction can be used to achieve faster and more scalable control. However, the intrinsic spin-orbit coupling of electron spins is too weak to induce high-fidelity coherent rotations [137]. In contrast, hole spins in the valence band are subject to stronger spin-orbit fields, enabling fast two-axis control of the qubit, albeit with the drawback of sub-microsecond coherence times [59, 138–141].

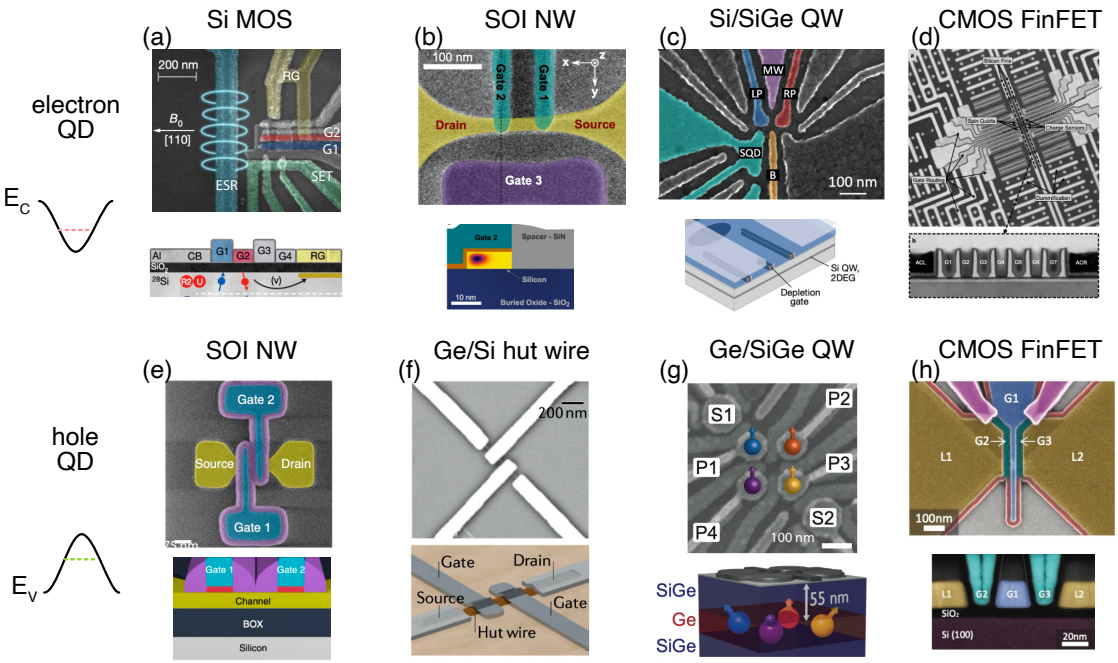


Figure 4.1 False-coloured scanning electrton microscope(SEM) images of quantum dot devices and view of corresponding material stack. (a-d) are electron spin qubit platforms and (e-h) are hole spin qubit platforms. (a) silicon MOS plannar device [136], (b) Si/SiGe heterostructure QW [51, 142], (c) SOI nanowire [137], (d) CMOS FinFET [37], (e) SOI nanowire [138],(f) Ge/Si hut wire [139], (g) Ge/SiGe heterostructure QW [60], (h) CMOS FinFET [143].

Figure 4.1 compares examples of four state-of-art spin qubit platforms with different geometries and material stacks for both electron and hole. The devices in Figure 4.1(a,c,f,g) are fabricated in the university clean room, and they pioneered many concepts of spin qubit readout and control technique. For

Table 4.1: Comparison of the electron and hole spin qubits platforms.

Parametrics	electron	hole
Relaxation time T1 (ms)	9000 [146]	16 [60]
Dephasing time T2 (ms)	28 [33]	0.1 [60]
Gate fidelity (1Q,2Q)	99.9%, 99.65% [39, 51]	99.9%,- [60]
Readout fidelity (at 1 us)	>99.7% [113, 130]	<70% [147]
Manipulation rate (MHz)	4.2 [137]	540 [148]
Qubit Footprint (nm^2)	50 × 50	20 × 20 (Si), 100 × 100(Ge)
Scaling (QDs array)	1 × 9, 2 × 4 [121, 149]	2 × 2 [60]
Temperature (K)	0.01 ∼ 1 [53, 54]	0.01∼ 4 [55]

example, the Si-MOS device explores the accumulation-mode quantum dot in silicon and isotopic purification of the material [141]. It is worth mentioning that a device of a similar architecture is established for hole spin qubit platform [144]. SOI nanowire devices in Figure 4.1(b,e) are fabricated in a research foundry, and they bridge the gap between functional qubit building block and scalable fabrication process. In recent years, there has been a successful demonstration of spin qubits in CMOS FinFET devices, as shown in Figure 4.1(d,h) from the industrial foundry. Due to the scattering of carriers in the crystalline environment, the difference in ionised impurity and phonon coupling strength leads to the different effective mass of electrons and holes. This directly impacts how electron and hole's wavefunctions spread out in physical space and determine the qubit's optimal footprint. Therefore, a high mobility channel is preferred for its low-disorder interface and relative relaxed critical feature size for higher fabrication yield. The typical silicon quantum dot footprint for electron is (50 × 50) nm^2 [33] and (20 × 20) nm^2 for hole [55]. The later developed high-mobility Ge/SiGe channel lifts the hole quantum dot footprint to (100 × 100) nm^2 [145]. The detailed comparison between state-of-art electron spin qubit and hole spin qubit is summarised in Table 4.1.

As summarised in above Figure 4.1, there have been various host materials and gate stacks for hosting the electron and hole spin qubits. MOS gate stacks are the material system that have successfully demonstrate electron and hole spin qubit. Recently, ambipolar quantum dot device, which can confine a single electron and hole, are interesting platforms to explore their performance for

quantum computing within the same crystalline environment [150, 151] and even combine the best features of both for novel implementations. Ambipolar transport has been previously demonstrated in group IV materials such as graphene [152], carbon nanotubes [153–155] and germanium [156]. In silicon MOS devices, ambipolar quantum dots have been achieved by integrating both n-type and p-type reservoirs in a single device [150, 151, 157–159], or by tuning the reservoir Fermi energy using doped source/drain electrodes such as NiSi [160]. Such ambipolar quantum dots have been studied via direct electrical transport, and recently, ambipolar charge sensing via single-electron and single-hole charge sensors has been demonstrated [161]. However, readout via gate-based charge sensors [162] or direct dispersive readout via spin projection in double quantum dots offers a compact and scalable measurement methodology with comparable measurement sensitivity and shorter integration time. Gate-based dispersive readout has been primarily developed in electron spin qubit readout and already demonstrated 99.9% readout fidelity at a measurement time of $1\mu s$. In hole spin qubit, it is still below 70%.

4.1.2 SOI device and experimental setup in the thesis

Here, I will introduce my work on ambipolar SOI nanowire devices with a MOS gate stack. The ambipolar device is fabricated with a double polysilicon gate layer technology, together with separate ambipolar carrier reservoirs to supply either electrons or holes. The detailed fabrication process of the ambipolar device is presented in Chapter 2.

Figures 4.2(a-d) show false-coloured scanning electron microscopy images and schematic cross-sections of the two types of devices studied here, hereinafter named Device I and Device II. These two devices have an effective SiNW cross-section of 24 nm × 24 nm. Device I consists of three polysilicon gates: two in Poly-1, with a gate length of 50 nm and pitch of 100 nm, and one Poly-2 covering the SOI area from source to drain. Device II consists of seven gates for the operation of the ambipolar quantum dots. Extension gates 1 and 7 accumulate carriers in the intrinsic silicon connecting the quantum dot "channel" area to the reservoirs. By applying a positive voltage on Gate 1 and Gate 7 above some threshold, $V_{\mathrm{e,th}}$,

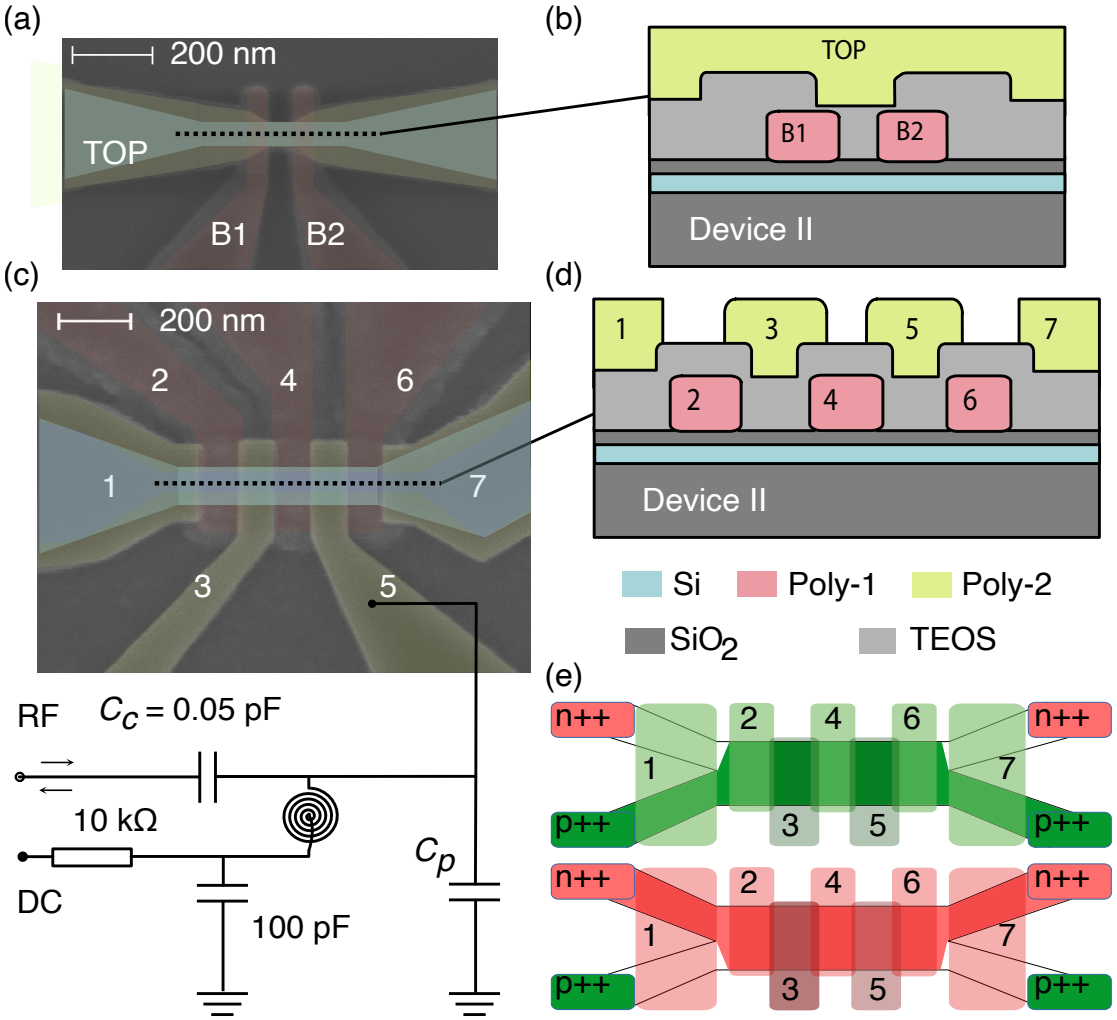


Figure 4.2 (a,c) False-coloured scanning electron microscope image of devices nominally identical to Device I and Device II. Gate 5 of Device II is attached to an LC circuit for dispersive readout. (b,d) Cartoon cross-sections of the stacked silicon channel, oxide and polysilicon gates along the dashed line in (a,c); and (e) schematic of ambipolar device operation mode, with the accumulation of electron or holes depending on the applied voltage on all the seven gates. Gates 1 and 7 extend from the implanted regions to the channel, while gates 2-6 define the quantum dots which confine single electron or holes.

the 2-dimensional electron gas (2DEG) is introduced to the channel, supplied by the n-type reservoir contact. Conversely, by applying a negative bias below $V_{\mathrm{h,th}}$ on the same gate, the 2-dimensional hole gas (2DHG) is introduced from the p-type reservoir contact, as illustrated in Figure 4.2(e). In contrast to the single top gate found in Device I, the distinct Gate 1 and 7 present in Device 2 allow for independent control of the left and right reservoir polarity. Gates 2-6 are used to confine quantum dots and tune tunnel coupling between the dots and to the reservoirs. Gates 2, 4, and 6 (Poly-1) wrap around the SiNW and have a gate length of 110 nm. Gates 3 and 5 (Poly-2) have a gate length of 120 nm and nominally overlap the Poly-1 gates by 10 nm.

Gate 5 is connected to an LC resonant circuit, consisting of a planar spiral NbTiN superconducting inductor on silicon for high sensitivity reflectometry readout [61, 130]. The choice of the gate here is motivated by the much lower resistivity for the Poly-2 versus Poly-1 gates, leading to better high-frequency performance, despite the expected lever arm from this gate on the quantum dots being lower. The parasitic capacitance is around 0.8 pF, and a surface-mount capacitor of 0.05 pF was used to decouple the resonator from the line [61]. All measurements were conducted at the dilution refrigerator base temperature of 10 mK. Together with the parasitic capacitance in the circuit, a resonance at 489.8 MHz with a resonant bandwidth of 1.64 MHz and a loaded quality factor $Q = 300$ and a coupling coefficient $\beta = 0.33$ is obtained. The NbTiN thin film thickness is 45 nm, and the total kinetic and geometric inductance of the spiral inductor is estimated to be 132 nH [[133]].

4.2 Charge state of ambipolar quantum dot

4.2.1 Transport measurement

The first study focus on the quantum dot formation in the SOI channel by measuring the source-drain current of Device I as illustrated in Figure 4.3(a). Both n-type and p-type transport currents are measured with a source-drain bias voltage $V_{\mathrm{sd}} = 2\,\mathrm{mV}$ applied across the source and drain contacts. Topgate threshold voltages for n-type and p-type conduction are measured to be

$V_{\mathrm{e,th}} = 0.40\,\mathrm{V}$ and $V_{\mathrm{h,th}} = -2.72\,\mathrm{V}$. The asymmetry in threshold voltages can be explained by the workfunction of the n-type doped polysilicon gates. When the silicon chanel are biased for n-type and p-type transport, barrier gates can pinch off the channel completely as shown in Figure 4.3(a). The barrier gates B1 and B2 have much lower threshold voltages $V_{\mathrm{e,th}} \simeq 0.2\,\mathrm{V}$ and $V_{\mathrm{h,th}} \simeq -1\,\mathrm{V}$ over the SOI channel because of the comparatively thinner gate oxide.

The SOI quantum dot device can be seen as a MOSFET, and when this transistor operates in the linear region (ohmic mode) with a source-drain bias voltage V_{sd}, the relation of its transport current I_{sd} and gate bias V_{g} can be approximated by Equation 4.1 with bulk-charge factor = 1 [163].

$$I_{\mathrm{sd}} = \mu_{\mathrm{e(h)}} C_{\mathrm{g}} \frac{W}{L} \left(\left(V_{\mathrm{G}} - V_{\mathrm{e(h),th}} \right) V_{\mathrm{sd}} - \frac{V_{\mathrm{sd}}^2}{2} \right) \tag{4.1}$$

in which W and L are the width and length of the silicon channel, C_{g} is the effective gate-oxide capacitance per unit area. From this equation, mobility can be obtained from the slope $m_{\mathrm{lin,e(h)}}$ of the transistor's I-V curve through the following relation.

$$\mu_{\mathrm{e(h)}} = m_{\mathrm{lin,e(h)}} \frac{L}{W} \frac{1}{V_{\mathrm{sd}}} \frac{1}{C_{\mathrm{g}}} \tag{4.2}$$

From the linear regions of the electrical transport curve in Figure 4.3(a), the mobilities of $\mu_{\mathrm{e}} = (608.4 \pm 3.4)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $\mu_{\mathrm{h}} = (259.8 \pm 1.9)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at 10 mK are extracted. A similar ratio of $\mu_{\mathrm{e}}/\mu_{\mathrm{h}}$ has been seen in planar ambipolar devices [151, 164]. In Figure 4.3(b,c), individual barrier gates can form a quantum dot in the silicon channel. Current peaks with a diagonal slope (see red stars) are attributed to a quantum dot formed between two barrier gates, coupled similarly to Gate B1 and Gate B2. Quantum dots can also form under the B1 and B2 gates themselves, thanks to additional confinement from the silicon nanowire itself, as seen in the vertical and horizontal current peaks (white boxes). From charge stability measurement at fixed barrier voltages shown in Figure 4.3(d,e), regular Coulomb diamonds corresponding to the central quantum dot in both electron and hole regimes can be observed, with respective charging energies $E_{\mathrm{C,e}} \simeq 5.4$ meV and $E_{\mathrm{C,h}} \simeq 3.2$ meV. From these measurements, exact capacitance values and

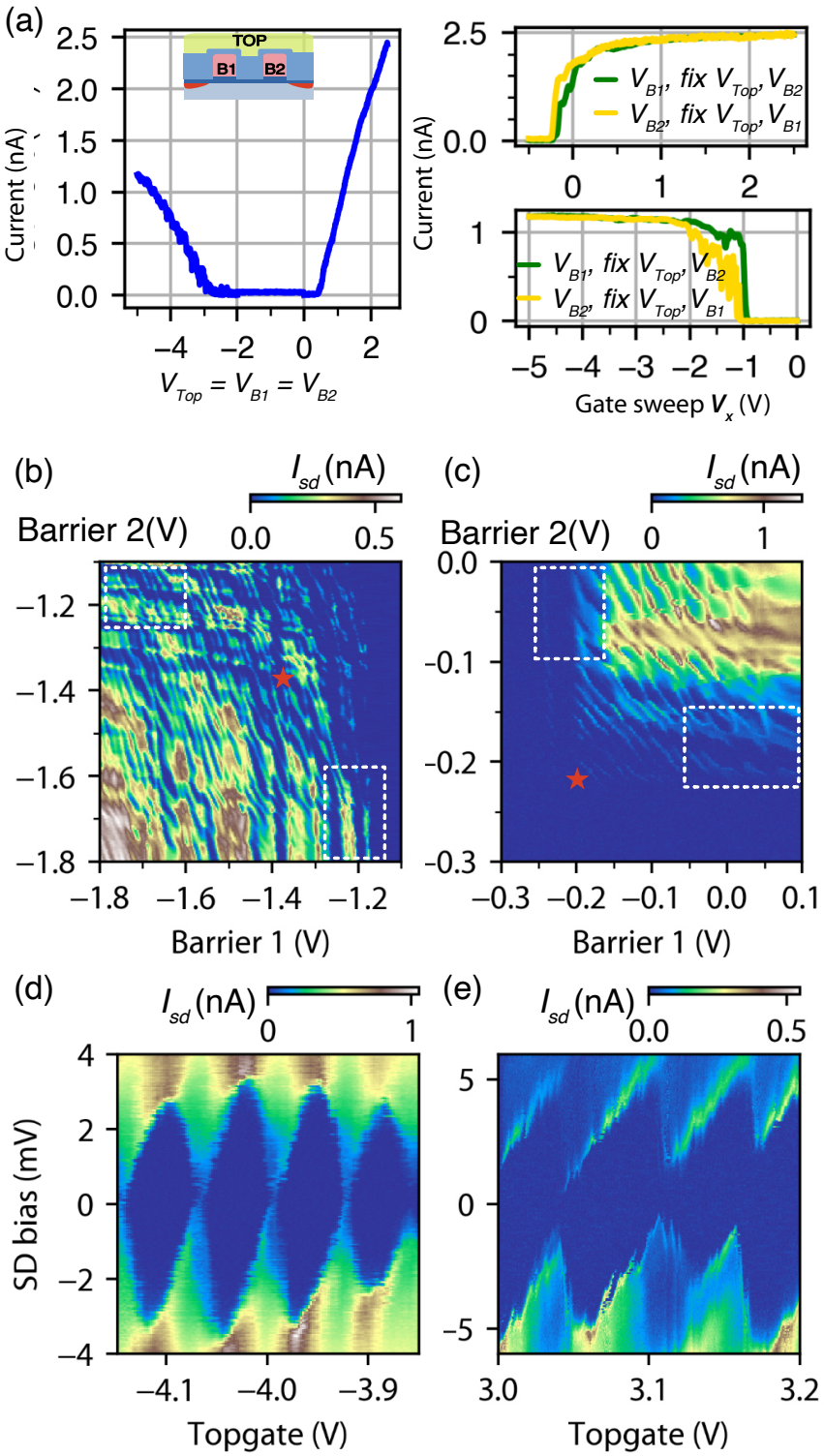


Figure 4.3 :(a)Transport measurements of Device I, (left)sweep of all gate ($V_{Top} = V_{B1} = V_{B2}$), (right1)sweep of barrier gate (B1,B2) while other gates fixed at 2.5V; (right2) sweep of barrier gate while other gates fixed at -5V, inset shows the schematic of double barrier gated nanowire (Device I). (b) p-type transport current as a function of each barrier gate B1,B2 at $V_{\mathrm{Top}} = -4.5V$. (c) n-type transport current as a function of each barrier gate B1,B2 at $V_{\mathrm{Top}} = 3V$. (d) transport measurement of p-type channel taken at B1 = -1.38V, B2 = -1.38V($\star$ in (b)),(d) transport measurement of n-type channel taken at B1 = -0.20V, B2 = -0.22V ($\star$ in (c))

Table 4.2: Electrostatic properties of the ambipolar quantum dots.

Device	QD	E_c (meV)	C_g (aF)	C_s (aF)	C_d (aF)	α
I (Topgate)	electron	5.4	2.2	25	3	0.074
	hole	3.2	2.4	30	18	0.048
II (Gate 5)	electron	17.4	1.7	4.0	3.5	0.18
	hole	10.6	2.6	12	0.4	0.17

gate lever arms for electrons and holes are extracted and summarised in Table 4.2.

The gate capacitance values are consistent with a nominal estimate of 2.5 aF based on a parallel-plate capacitor simplification, with total area $A = (50 \times 24)\ \text{nm}^2 \times 3$ (considering three sides of the wrap-around gate over the SOI channel) and stated oxide parameters — this suggests that these highly-occupied quantum dots are distributed across the entire SiNW cross-sectional area, as opposed to being localised within the SiNW corners.

Device II was similarly measured in transport and also using gate reflectometry. Each gate was confirmed to pinch-off the channel (see Figure 4.4(a,b)), while the Coulomb diamonds shown in Figure 4.4(c,d) indicate the formation of electron (hole) quantum dots under gate 5, having been measured with all other gates biased well above (below) the threshold voltage of 3 V (−4.5 V).

The measured lever arms and gate capacitances for this ambipolar quantum dot under gate 5 are presented in Table 4.2. These coulomb diamonds are measured in the few-carrier regime. Correspondingly, the dot-lead capacitance values are much smaller than for the highly-occupied quantum dots studied in Device I. As a result, the gate capacitance dominates, and the gate lever arms α are larger. Given the nominal 110 nm gate length in Device II, the measured gate capacitances indicate a smaller effective area of the quantum dot, suggesting that these few-carrier dots are now localised in the top corners of the SiNW cross-section. In order to study the electrostatic coupling of Poly-1 and Poly-2 gate over the SOI channel, transport measurements are performed on a device identical to the aforementioned Device II and observed regular coulomb diamond signature in both n-type and p-type quantum dots under Gate 4(Poly-1) and Gate 5(Poly-2) as shown in Figure 4.5. The lever arms of the gate on the quantum dot formed underneath Gate 4 and Gate

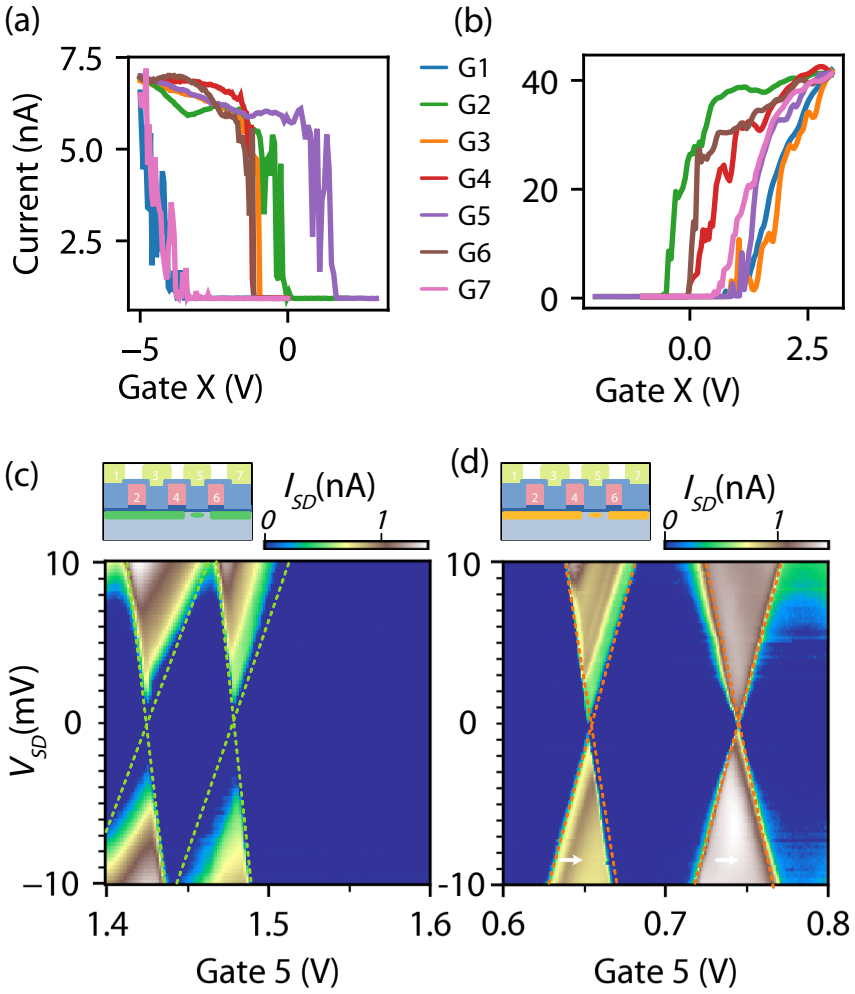


Figure 4.4 : (a) p-type transport measurement (V_{sd}= 2 mV) as a function of each gate where all other gates were biased at -4.5V. (b) n-type transport measurement (V_{sd}= 2 mV) as a function of each gate where all other gates were biased at 3V. (c) p-type source to drain current I_{sd} as function of Gate 5 and $V_{\mathrm{sd}}$when other gates were biased at -4.5V. (d) n-type source to drain current I_{sd} as function of Gate 5 and V_{sd} when other gates were biased at 3V.

5 are obtained by $\alpha = \Delta V_{sd}/\Delta V_g$, where ΔV_g is the separation in voltages of Gate voltages between boundaries of Coulomb diamond at a given ΔV_{sd} as indicated by the white dashed line in Figure 4.5. The extracted gate lever arm values are summarised in Table 4.3. A ratio of 2-3 between the lever arm of Gate 4 (Poly-1) and over the lever arm of Gate 5 (Poly-2) is observed. This ratio is understood as the noticeable difference in oxide thickness under Poly-1 and Poly-2 gates.

Table 4.3: Lever arms of Poly 1 and Poly 2

Gate	QD	α (eV/V)
Gate 4 (Poly-1)	electron	0.50 ± 0.05
	hole	0.352 ± 0.064
Gate 5 (Poly-2)	electron	0.162 ± 0.005
	hole	0.175 ± 0.006

I then move from the formation of single QD to double QDs in the device. Fixing the barrier bias voltagse for single QD coulomb diamond transport for both the Gate 3 and Gate 5, the double QD transport with the signature of bias-triangle is observed in Figure 4.6(a)(b). This is a p-type double QD formed under Gate 3 and Gate 5, with Gate 4 functioning as the barrier gate. Gate 2 and Gate 6 control the barrier between QDs and source/drain leads. Similar to coulomb diamond, bias-triangle indicates the well-defined double QD with charge transition boundary and mutual interaction. To further demonstrate the tunability of the barrier gate over the double QD coupling. Gate 4 is set to different values between -1V to -2V for the same voltages range of the transport measurement between Gate 3 and Gate 5 as shown in Figure 4.6(b)(c)(d). When Gate 4 = -1.1 V, the shape and boundaries of the bias triangles are clear. When Gate 4 = -1.2 V, the area of the bias triangles becomes bigger, which indicates the increase in QD size and mutual capacitance. When Gate 4 = -2 V, the two QDs under Gate 3 and Gate 5 merge into one QD, and only one charge transition line of this big QD can be seen in the transport measurements. Similar double QDs and tunability can be observed for n-type with corresponding voltages.

4.2.2 Dispersive readout of inter-dot transition

This section demonstrates a dispersive readout of reconfigurable ambipolar double quantum dots. In Figure 4.7(a–d), multiple ambipolar double quantum

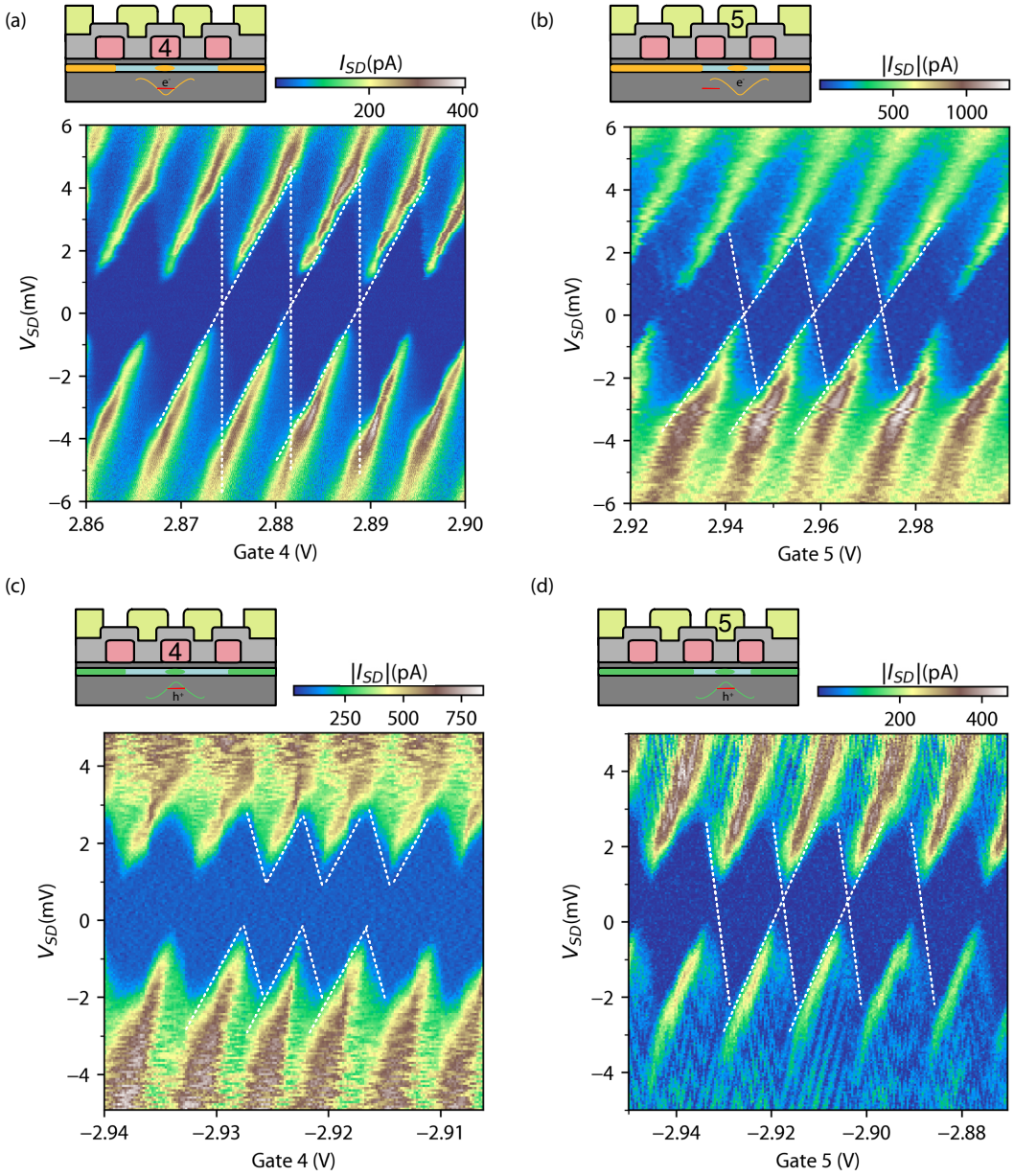


Figure 4.5 Source-drain current I_{sd} as function of Gate 4/ Gate5 and V_{sd}. (a) n-type quantum dot under Gate 4, Barrier Gate 3 = 0.2 V, Barrier Gate 5 = 1.1 V; (b) n-type quantum dot under Gate 5, Barrier Gate 4 = 0.24 V, Barrier Gate 6 = 0.33 V; (c) p-type quantum dot under Gate 4: Barrier Gate 3 = 0.3 V, Barrier Gate 5 = 0.45 V; (d) p-type quantum dot under Gate 5: Barrier Gate 4 = -1.1 V, Barrier Gate 6 = -0.99 V.

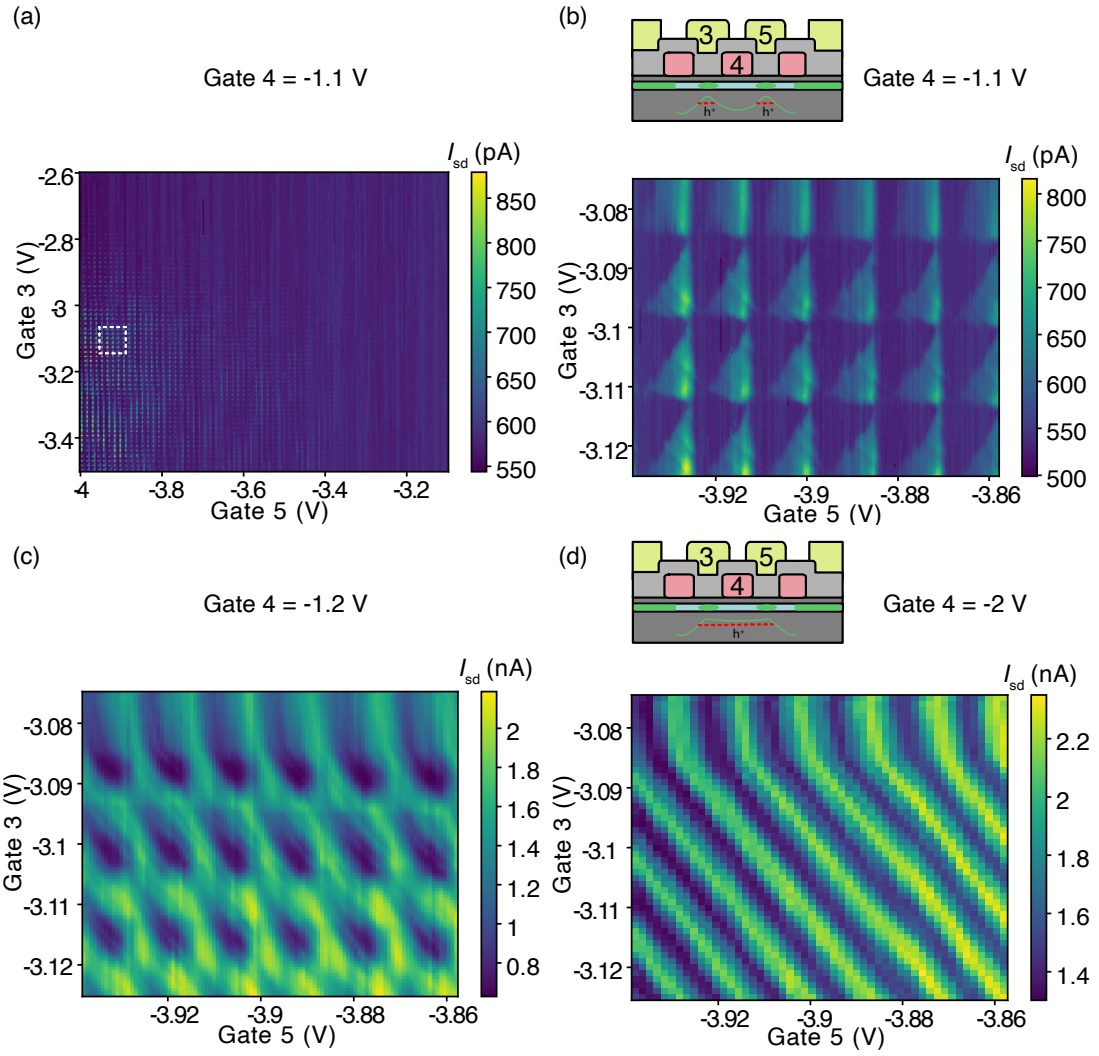


Figure 4.6 Transport measurement of I_{sd} showing charge stability diagram between the p-type double QD under Gate 3 and Gate 5 with Gate 4 functioning as the tunable barrier gate(I_{sd}= 4 mV): (a,b) overview and zoom-in charge stability diagram with Gate 4 = -1.1 V; (c) Gate 4 = -1.2 V. (d) Gate 4 = -2 V.

dots scenarios are presented: Double electron or hole quantum dots located either under gates 5 and 6 (with the source reservoir off) or under gates 4 and 5 (with the drain reservoir off).

The stability diagram for each scenario is measured by monitoring the normalised phase difference, $\Delta\Phi/\Phi_0$, between the incoming and outgoing radio-frequency signals from the resonator, where Φ_0 is the maximum phase difference. The IDTs within the pair of quantum dots are visible in all four different configurations. No IDTs were observed between dots formed under non-adjacent gates — the tunnel barriers formed under gates 2, 4 or 6 were evidently too opaque due to their length. The magnitude of the dispersive response at the IDT is essential for spin readout based on Pauli spin blockade since it determines the maximum signal [114, 165, 166]. In Figure 4.7(e), two-line traces of the IDT reflectometry signal from both electron double quantum dots and hole double quantum dots are taken, illustrated by the arrows in Figure 4.7(c,d), the demodulated quadrature and in-phase signals and filtered with a notch-filter at 16 kHz to suppress a noise peak attributed to the audio component of the pulse tube of the dilution refrigerator [167].

Figure 4.7(f) shows the scatter plot of these detuning-dependent traces in (I, Q) space, the dispersive peak at (I_s,Q_s) can be identified in the complex plane, facilitating the extraction of the SNR. Here the power SNR in dB is calculated as

$$\mathrm{SNR} = 20\log\left(\frac{I_s - I_0)^2 + (Q_s - Q_0)^2}{2\sigma_S^2}\right) \tag{4.3}$$

where I_0 and Q_0 are respectively the in-phase and quadrature components mean of the signal background and σ_s is the average 2D standard deviation of the background noise which can be seen as the radius of the dot around the noise background in the inset of Figure 4.7(f). $\mathrm{SNR_{e,IDT}} = 49.8$ and $\mathrm{SNR_{h,IDT}} = 52.9$ is obtained for integration time of 5 ms, indicating that this measurement configuration should provide a minimum integration time, for equivalent SNR = 1, of $\tau_\mathrm{e} = 160$ µs and $\tau_\mathrm{h} = 100$ µs for electron and holes respectively. The accurate extraction of minimum integration time should measure SNR at a number of integration time and extract the time at SNR=1 after a linear fit is performed [168]. In order to have a generalised comparison of the dispersive

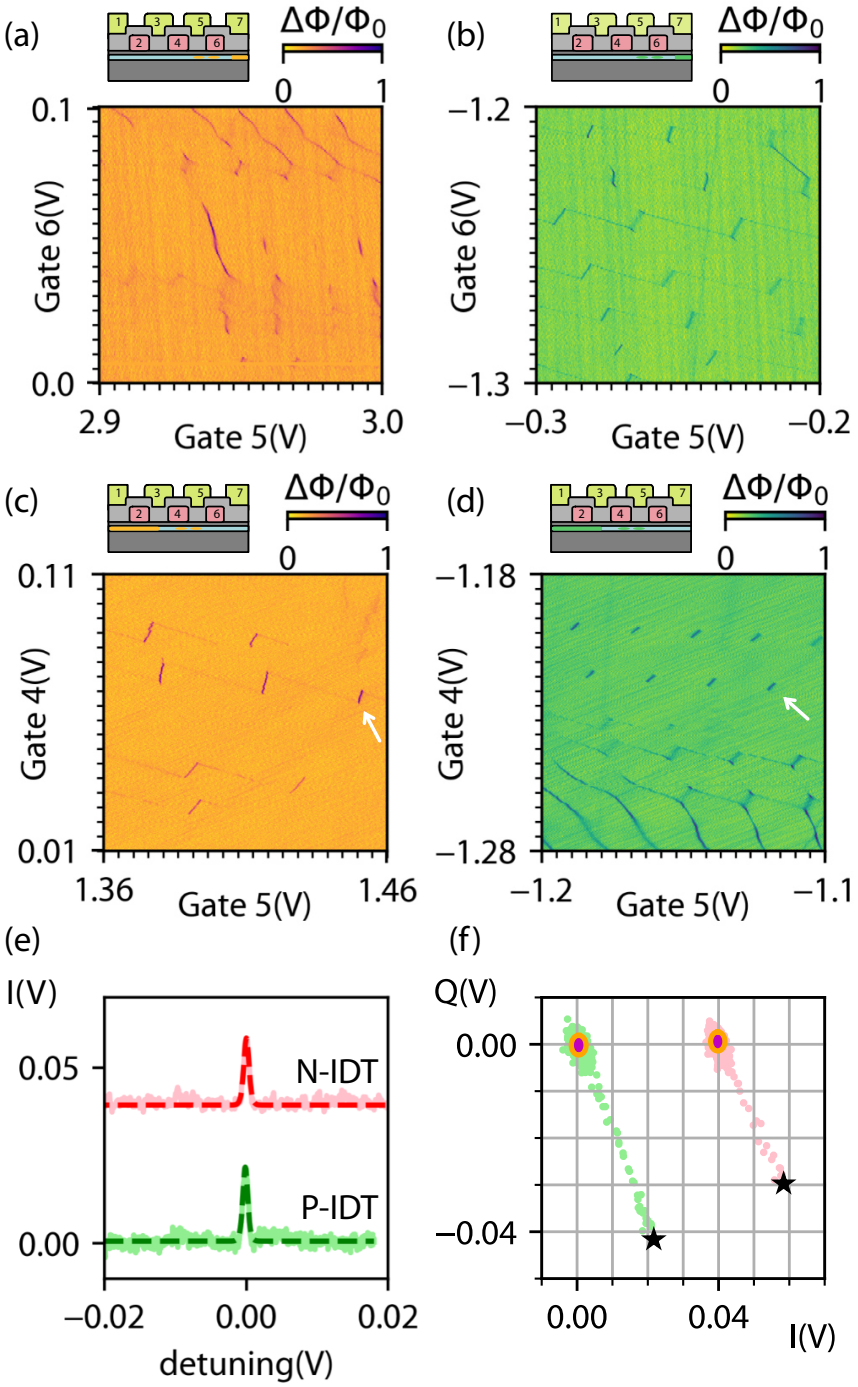


Figure 4.7 : (a-d) different ambipolar double dot configurations and their corresponding charge stability diagrams (a): electron double dots under gate 5 and 6,(b): hole double dots under gate 5 and 6, (c): electron double dots under gate 4 and 5, (d): hole double dots under gate 4 and 5, see Supp. (e) line trace and fit of homodyne quadrature signal I across IDT in n-type double dot (red, offset by 0.04V) and p-type(green) measured with input power P_c = -92 dBm. (f) Scatter plot of line trace from both quadrature signals in I-Q plane, signal peak (I_s,Q_s) of the line-fit($\star$), a 2D standard deviation of background I-Q signal. A 10 kHz low-pass filter to filter the homodyne quadrature signal IQ and took the average of over 300 traces to obtain a sufficient SNR.

readout SNR for electron and hole IDTs, tunable tunnel coupling between the double quantum dots is desired with the assist of barrier gate.

4.3 Thermometry with ambipolar quantum dots

The thermometer is an essential element in low-temperature experimental physics. A primary thermometer allows measuring electron temperatures via established physical relation without calibration to a second thermometer. The common technique includes current-sensing noise thermometry using the Johnson-Nyquist noise of a resistor [169]; current sensing noise thermometry using superconducting quantum interference devices [170]; Shot-noise thermometry using noise power of a biased tunnel junction [171, 172]; or Coulomb blockade thermometer [173, 174] taking use of the charging effects in two-terminal devices. QD and SET have also been used in thermometry experiments to measure electron temperatures [175, 176]. Recently a gate-based electron thermometer (GET) has been developed based on cyclic electron tunnelling between QD and the reservoir, which doesn't require electron transport or even galvanic contact to source-drain (with calibrated known temperature) [119, 120]. This GET proves to measure temperature accurately, fast, and compactly.

This section follows the dispersive readout study of ambipolar gate-defined QDs. Different broadening mechanisms of RF reflectometry signals are studied to understand the effective electron temperature and hole temperature from the thermometry experiments. Theory in Sergeev et al. [177] shows that electron-phonon coupling is determined by interference of electron scattering and elastic electron scattering from impurities and defects from impurities and defects. It has been experimentally demonstrated in doped silicon that holes are more strongly coupled to the lattice phonons than electrons at 300 mk [164]. It is suggested that the interband scattering between the heavy hole, the light hole and spin-orbit split valleys could contributed to additional conducting channel between holes and phonons [178]. Therefore, in the ambipolar QD device, hole reservoir is expected to have a lower effective temperature than electron reservoir. Using the GET to

investigate effective temperature in the ambipolar device will not only compare the two candidates for quantum computing but also stimulate further work on carrier-phonon coupling.

4.3.1 Temperature dependence

The single-electron quantum dot (e-QD) and hole quantum dot (h-QD) in the ambipolar device are used to investigate the effective electron temperature T_e of the corresponding reservoir. The temperature of the electrons in the device differs from the refrigerator temperature T_{bath} due to the freeze-out of electron-phonon coupling. Noise is another source of the elevated T_e than T_{bath}. Figure 4.8(a) describes the same setup as the previous dispersive readout experiments for the thermometry experiment. Here, the rf response of the resonator of the e-QD and h-QD is determined by the tunnel coupling between the dot and the reservoir and the effective electron temperature T_e.

As previously discussed, when $h\gamma_0 \ll k_B T_e$, the rf response of the resonator take the tunneling capacitance as:

$$C_{\text{t}} = \frac{e^2\alpha^2}{4k_B T_e} \cosh^{-2}\left(\frac{\varepsilon}{2k_B T_e}\right) \tag{4.4}$$

the Normalized phase response $\Delta\phi$ of the resonator is propotional to the change in C_{t} which broadens as the bath temperature T_{bath} increases as shown in Figure 4.8(b).

Lever arms for the single lead e-QD and h-QD are different than the what measured in the Coulomb diamond measurement since the capacitances are different in this configuration. The relation between the C_{t} and T_e at high bath temperature ($T_{\text{bath}} > 0.6\,\text{K}$) is used to determine the lever arms of e-QD and h-QD. The linefit with the function $A_{\text{fit}} \cdot cosh^{-2}\left(\frac{V_{\text{G5}}}{2k_B T_{fit}/\alpha}\right)$ is used to obatin the fitted temperatures T_{fit}/α for bath temerature 0.6 to 1.1 K. At this range, the linewidth broadening contributed from tunnel coupling is negligible therefore $T_{fit} = T_e = T_{\text{bath}}$. The fitted temperatures and controled bath temerature are ploted in Figure 4.8(c) where the lever arms for e-QD and h-QD is the inverse of the slope. The extrapolation of the linear fitted line perfectly crosses the

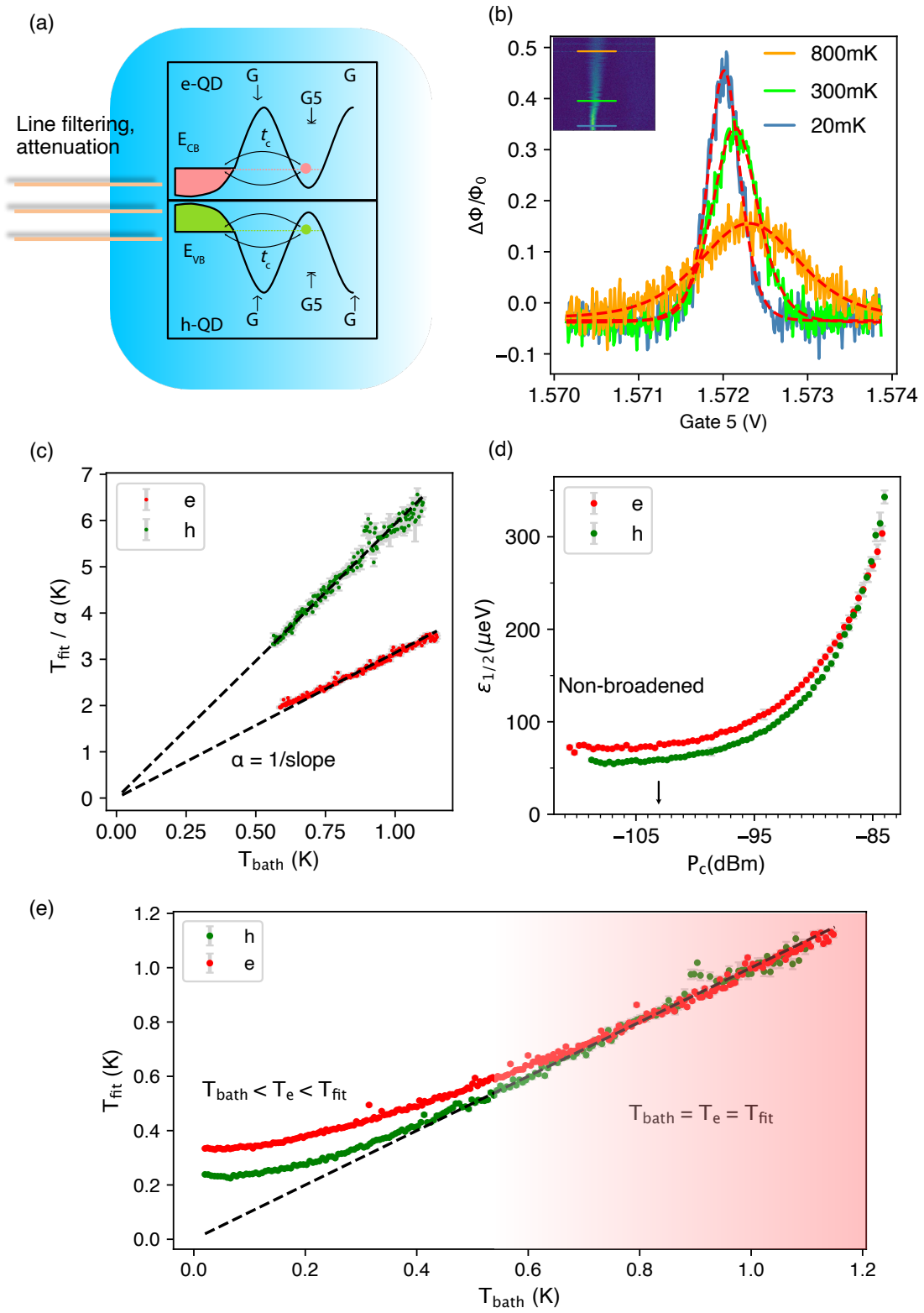


Figure 4.8 (a)Schematic of the gate-based electron thermometer for ambipolar device. (b) Normalized phase response $\Delta\phi$ of the resonator as a function of gate 5 voltage G5 swept across the DRT for different T_{bath} the inset shows DRT signal as a linear sweep of the T_{bath} in the y-axis .(c) Calibration of the G5 lever arm on the e-QD and h-QD respectively using linear extrapolation to $T_{\text{bath}} = 0$.(d)Calibration of the input power P_c to operate at the non-broadened regime for both e-QD and h-QD. (e) Fitted temperature as a funciton of the bath temperature for e-QD and h-QD.

$T_{\text{bath}} = 0$ and validates the model. In Figure 4.8(d), the FWHM ($\varepsilon_{1/2}$) of both e-QD and h-QD are ploted as a function of the carrier power P_c at the resonator. For high carrier power, $P_c > -98\,\text{dBm}$, $\varepsilon_{1/2}$ increases with P_c indicating the power broadenening in the DRT. For $P_c < -98\,\text{dBm}$, both $\varepsilon_{1/2}$ remain independent therefore the intrinsic linewidth due to electron tunneling can be observed. The temperature dependence experiments in this section all operate at the non power broadened regime $P_c = -103\,\text{dBm}$.

When the lever arms for e-QD and h-QD are pluged back to the Equation A.1 for temperature fitting, we can plot the obtained T_{fit} as a function of the bath temperature for the range 0.01 to 1.1 K in Figure 4.8(e). For bath temperature $T_{\text{bath}} < 0.6\,\text{K}$, the fitted temperature started to deviate from the dashed guideline $T_{\text{fit}} = T_{\text{bath}}$ due to non-negligible tunnel coupling and noise. As a result, the fitted temperature T_{fit} at the base temperature of the dilution refrigerator is 334.3 ± 1.5 mK for e-QD and 238.7 ± 2.4 mK for h-QD. At this point, the measured temperature from GET is bigger than the effective electron temperature T_e.

4.3.2 Tunable tunnel coupling

A tunable barrier gate can make the tunnel rate equivalent broadening much smaller than thermal bath fermi level broadening at base temperature, thus eliminating the contribution from tunnel-rate related broadening.

For the e-QD and h-QD coupled to the nearby reservoir shown in Figure 4.9(a), the gates controlling two sides of the barrier have a different effect on the tunnel coupling. In this experiment, e-QD is coupled to the right side reservoir close to Gate 4. Voltage increase on Gate 4 lowers the barrier and thus increases the tunnel coupling. In contrast, the voltage increase on Gate 2 lowers the barrier on the left side, effectively pulling the e-QD away from the reservoir, thus minimising the tunnel coupling. For h-QD coupled to the left side reservoir, Voltage increase on Gate 2 lifts the barrier to the reservoir while voltage increase on Gate 4 effectively pushes h-QD towards the reservoir. The FWHM of the DRT signal as the function of the corresponding gate is plotted in Figure 4.9(b-d).

The sequence of the barrier gate sweeping is done with the barrier gate close to the reservoir and then the push/pull barrier gate far from the reservoir. In this

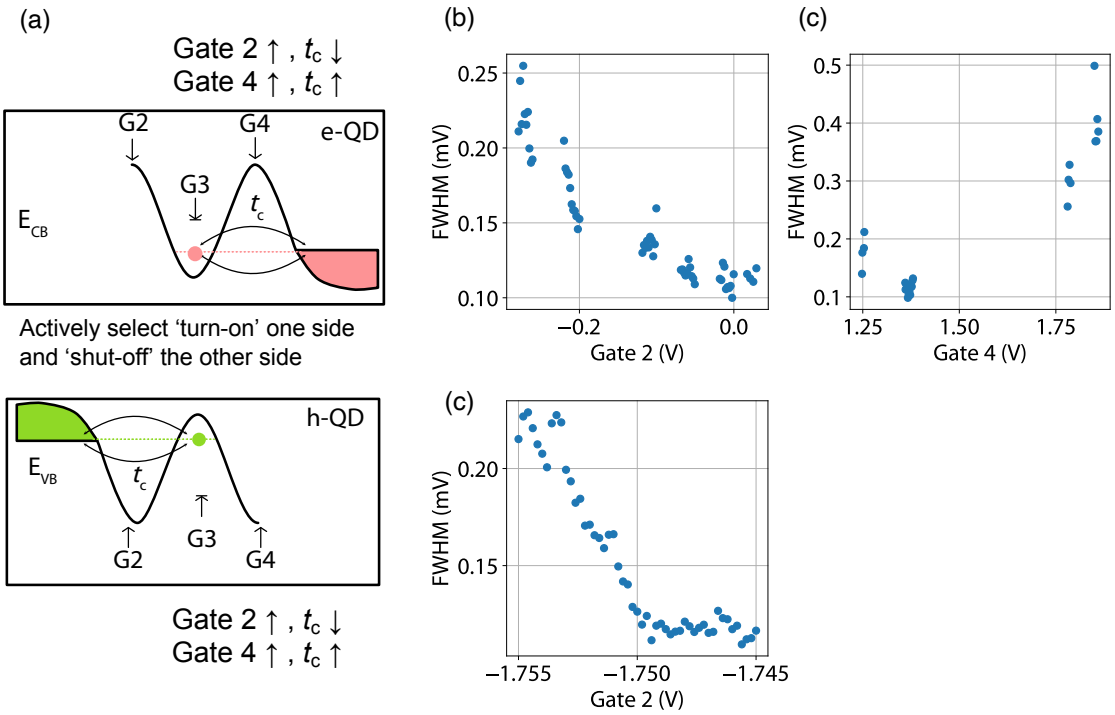


Figure 4.9 FWHM of the electron DRT as a function of the gate 2 voltages (b) and gate(4) (c) and FWHM of the hole-DRT as a function of the gate 2 voltages, the gate 4 tends to show less control over the hole-DRT.

experiment, Gate 4 tends to show less control over the FWHM of hole-DRT.

4.3.3 Noise characterization

Spectral density $S(\omega)$ measured in units [V^2/Hz] is used to characterize noise in the device. The noise-introduced fluctuations of the sensor in time is expressed as:

$$\Delta V(t) = V(t) - \langle V(t) \rangle \tag{4.5}$$

where $\langle V \rangle$ is the time average centre position. Convolution of the voltage fluctuations with itself leads to the autocorrelation function $C(\Delta t)$ defined as:

$$C(\Delta t) = \langle \Delta V(t) \Delta V(t + \Delta t) \rangle = \langle \Delta V(0) \Delta V(\Delta t) \rangle \tag{4.6}$$

The Fourier transform of the autocorrelation function gives the spectral density [69]. The voltage spectral density of e-QD and h-QD is plotted in Figure 4.10. Both have similar noise spectral at the range between 0.01 Hz and 0.1 Hz, but h-QD has much more noise above 0.1 Hz. The single-shot

measurement of the DRT in this experiment takes 0.02 s. Figure 4.10(c,d) shows the temperature broadened signal plotted as a function of the number of averages of the trace. Both e-QD and h-QD show a small FWHM with a high error bar due to low sensitivity and saturates at a long measurement time ($N > 10$). Gaussian and two-level-fluctuator noise can broaden the signal; the related study is described in A.

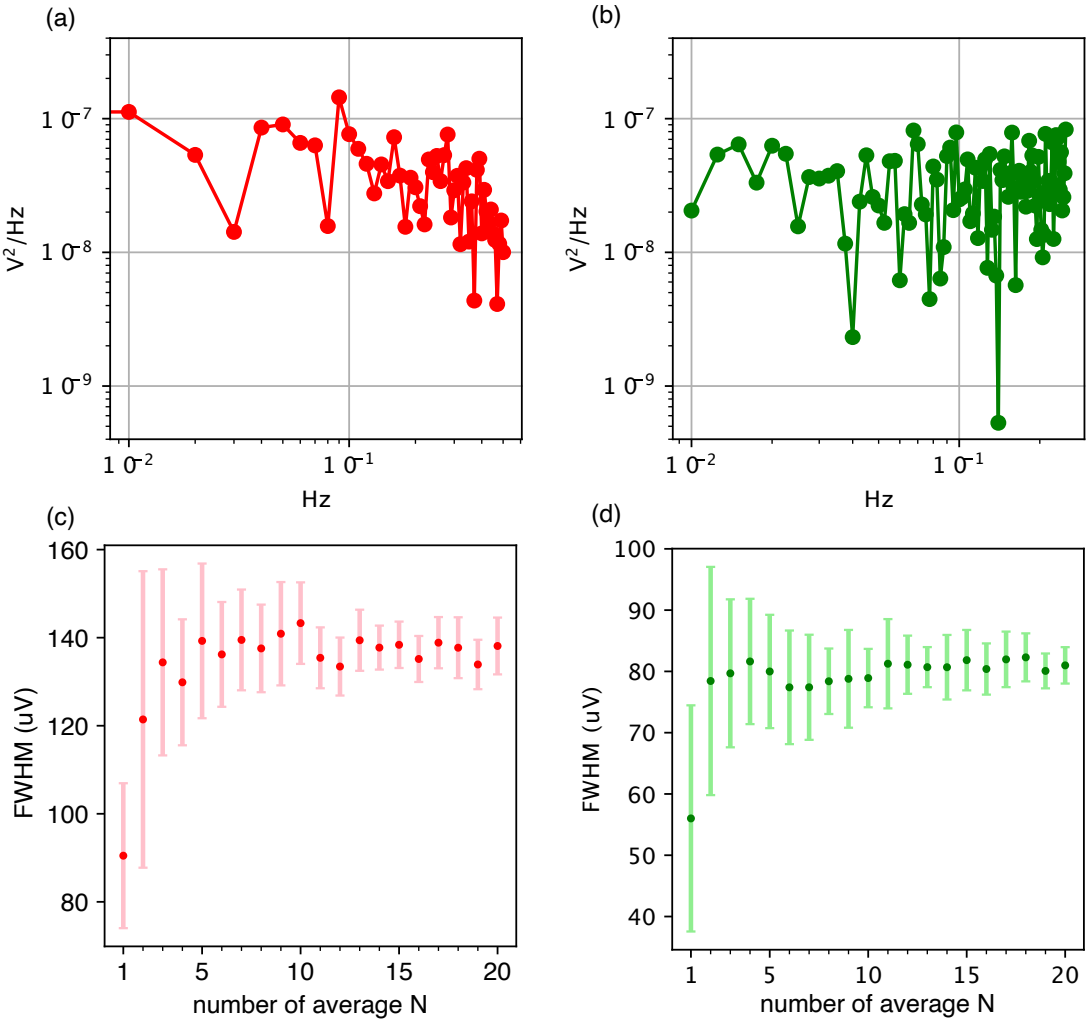


Figure 4.10 Spectral density in V^2/Hz for (a) e-QD and (b) h-QD signal; fitted FWHM as a function of the number of averaged trace for (c) e-QD signal and (d) h-QD signal.

The final thermometry experiments is operated at a non-tunnel broadened regime with the minimum integration time (0.02 s) of the experiments. To extract temeperature-broadened linewidth, a threshold is put on fitting where multiple-peak signal traces due to two-level fluctuator are ruled out. The electron temperature of e-QD coupled to reservoir (T_{fit}) is measured as

(85 ± 15) mK, and (T_{fit}) for h-QD is measured as (72 ± 14) mK. Based on the noise level of the e-QD and h-QD shown in Figure 4.10, the lower bound for the actual electron temperature is measured ($T_{\text{e}} = T_{\text{fit}} = (85 \pm 15)$ mK is), while the linewidth of h-QD is still the combination of thermal broadening and noise broadening ($T_{\text{h}} < T_{\text{fit}} = (72 \pm 14)$ mK).

4.4 Conclusion

The results in this Chapter has experimentally demonstrated the reconfigurable ambipolar quantum dots in an SOI multi-gate nanowire transistor. Good evidence suggests observation of the last hole/electron in the quantum dot. However, a more robust confirmation requires magneto-spectroscopy to examine shell-filling or spin-filling experiments. Double quantum dot with tunable barrier gate is also demonstrated with transport measurements.

The RF readout of the inter-dot transition is also achieved with the minimum integration time of the signal 160 (100) µs for electrons (holes). This sensitivity could be further enhanced by performing reflectometry using a gate in the Poly-1 layer: the larger lever arms of such gates should give an improvement factor of $\left(\frac{\alpha_{\text{e,Poly-1}}}{\alpha_{\text{e,Poly-2}}}\right)^2 \simeq 9$. Operating at a higher reflectometry frequency (e.g. 1.8 GHz) should yield a $\sim$ 5× SNR improvement due to reduced parasitic capacitance [168], while further improvements using a Josephson parametric amplifier [130] and critically coupled resonator could bring the integration time down to $\tau_{\text{SNR=1}} = 100$ ns, which is close to the state-of-art dispersive charge readout 10 ns [168, 179].

Thermometry experiments with the gate-based reflectometry allow us to probe the effective temperature of the reservoir and successfully demonstrated a lower hole reservoir temperature than electron resevoir temperature in the same device with exact same crystalline environment and cable connections. This experiment indirectly compares the electron-phonon and hole-phonon coupling rate in silicon and functions as the perfect toolbox for further study. A gate sensor with a high sensitivity to measure temperature broadened tunnel capacitance is desirable to eliminate the noise presented in the device. The rf response of gate-based sensor

replies on electron tunnelling between QD and reservoir and associated tunnelling capacitance when $\gamma > f_{\mathrm{r}}$. Therefore, the absolute sensing limit of the temperature range due to resonator is at $k_{\mathrm{B}}T_{\mathrm{e}}/h = \gamma \geq f_{\mathrm{r}}$. For a resonator with $f_{\mathrm{r}} = 500\,\mathrm{MHz}$, the lowest detectable electron temperature $hf_{\mathrm{r}}/k_{\mathrm{B}} = 24\,\mathrm{mK}$.

Chapter 5

Scalability of quantum dots array in SOI nanowire

In this Chapter, a scalable QD array device architecture is introduced, showing the charge sensing capability of QD with transport and gate-based reflectometry experiment. Loading of the first electron in 2×2 QD array is demonstrated. A floating-gate type nanowire device is presented to demonstrate the measurement capability across different silicon nanowires. Electrostatic coupling between QDs is measured and simulated for different distances—this guides the future scaling of the device into the second dimension. The sensing scheme in the scaled-up SiNW QD array device is briefly discussed in the end. This work led to the publication:

- Duan, J., Fogarty, M. A., Williams, J., Hutin, L., Vinet, M., & Morton, J. J. L. (2020). Remote Capacitive Sensing in Two-Dimensional Quantum-Dot Arrays. Nano Letters, 20(10), 7123–7128. https://doi.org/10.1021/acs.nanolett.0c02393

5.1 Quantum dots array

Spin qubits in silicon demonstrate the fundamental properties required for scaled quantum computation, with state-of-the-art one- and two-qubit operations demonstrating control fidelities approaching the requirements for fault-tolerant quantum error correction [51, 52]. While all control elements have been integrated into single devices with scalable readout mechanisms [86], much effort

is now being focused on developing these devices from simple laboratory prototype structures into scaled arrays of qubits capable of eventually yielding a quantum advantage [36, 180]. The promise of a highly developed materials system and mature fabrication industry, together with the success of laboratory and industry-grade prototype SiMOS quantum-dot-based devices [126] has led to the proposition of several approaches to foundry-compatible scaling into grid-based architectures of quantum dot arrays. These approaches range from densely-packed qubits with next-nearest-neighbour couplings [40], dot arrays partially-populated with qubits [37, 181] and arrays with qubit sites linked via mediating structures such as jelly bean QD [182, 183], coplanar waveguide[184, 185], surface acoustic wave [186] for remote qubit-qubit coupling.

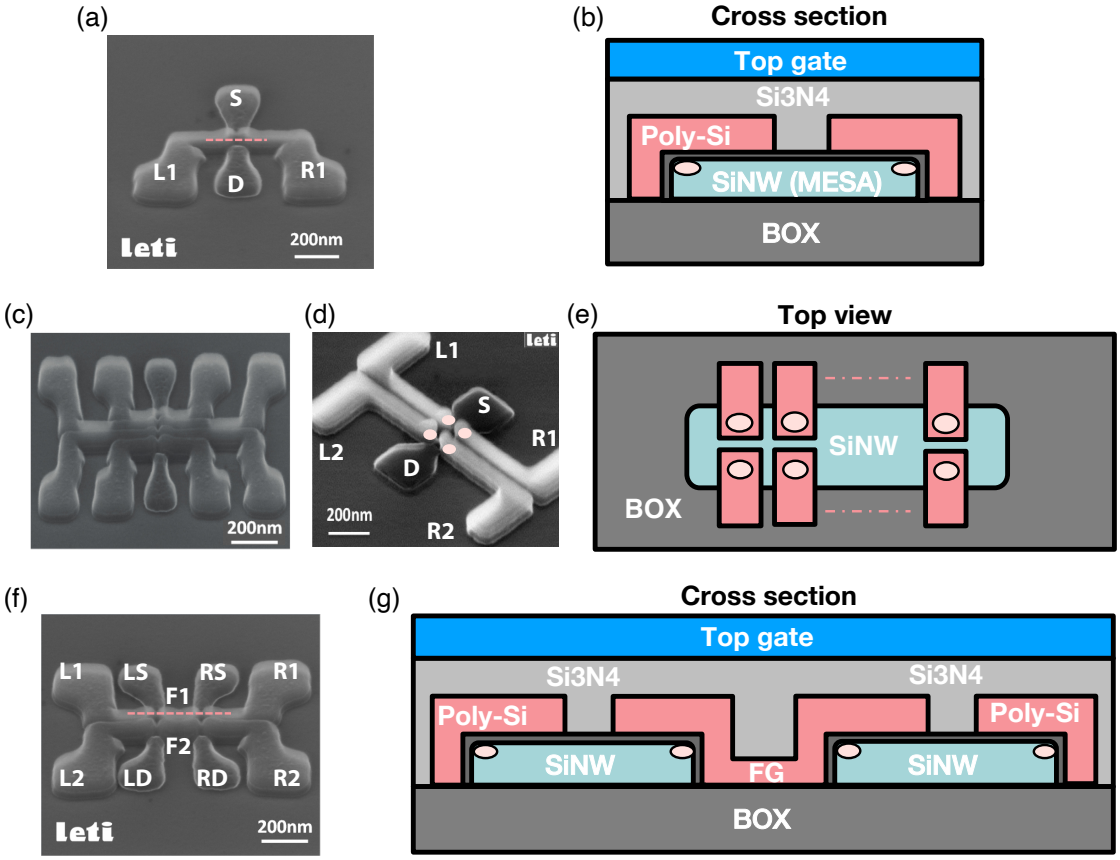


Figure 5.1 Oblique-angle Scanning Electron Micrograph illustrating the gate structure of the FD-SOI device: (a) single pair split-gate device, (c,d)two pair split-gate device, (f) floating gate device. Schematic of the SiNW gate: (b) cross section of face-to-face gate and SiNW, (e) top view of scalable split-gate device, (g) cross section of two coupled SiNW of floating gate device.

Based on the face-to-face quantum dots in the corners of the silicon channel, bilinear QD arrays have been demonstrated in split-gate SiNW devices, as shown

in Figure 5.1. Such a scalable QD array device allows for proximal sensor integration for charge and spin states through dispersive measurements using gate-based RF reflectometry. The advantages of these integrated sensors can be extended by mechanisms for *off-wire* coupling to sense the charge state of QDs located in remote locations within the quantum dot array. In order to enhance the capacitive coupling between spatially separated quantum dots, studies in planar GaAs/AlGaAs and Ge/Si heterostructures and carbon nanotubes have exploited a *floating gate* [187–189]; a metallic electrode which is galvanically isolated from, but capacitively coupled to, its immediate environment.

Here, utilising a single quantum dot sensor, a system capable of performing both proximal and remote capacitive charge sensing of QDs within a single silicon nanowire and distributed across two parallel nanowires is demonstrated. These results include single-wire variants, serving as isolated 1×2, 2×2 and 3×2 QD arrays. All devices described here are located in the same die, fabricated from an FD-SOI process [126](see 3for fabrication details). This approach uses floating gate electrodes to capacitively couple a sensor dot to quantum dots on remote nanowires whilst maintaining sensitivity to adjacent dots within the local nanowire. Next, the sensitivity to charge movement within these two schemes is quantified by experimentally benchmarking the device capacitance matrix, supported by cryo-SiMOS simulations.

The scanning electron micrograph (SEM) image in Figure 5.1(f) shows the floating gate device used in the remote sensing experiments. Two parallel nanowires, with centre-to-centre spacing of 200 nm, are fabricated with two central floating gates, F1 and F2, wrapping the interior edges of both, spanning the gap between the two silicon structures. Gates F1 and F2 are capacitively coupled to the surrounding gates by proximity but are otherwise electrically isolated. All gate structures are separated by a Si_3N_4 spacer which increases cross capacitance. The device is further encapsulated by 300 nm of silicon oxide, above which an additional Top gate T is deposited utilising a back-end metallisation layer(shown in Figure 5.1(g)). Full geometric details for the family of devices in this section can be found in Figure 5.2 and Table 5.1 I.

The charge sensor for these experiments consists of a two-terminal structure in

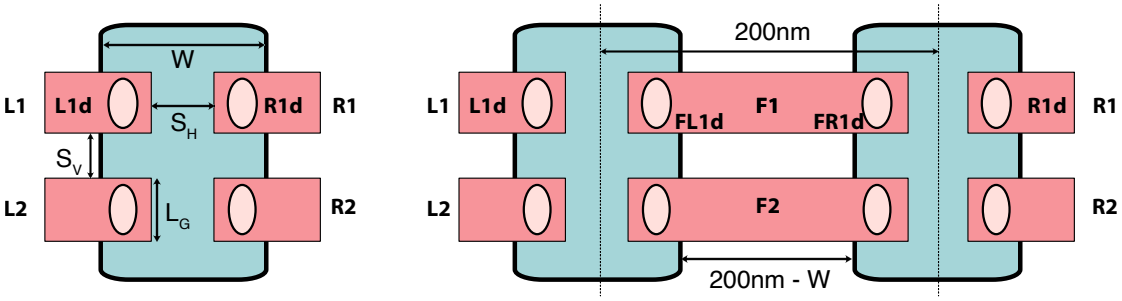


Figure 5.2 (a) Single 2 × 2 nanowire with relevant dimensions indicated. (b) Single 2 × 2 nanowire with relevant dimensions indicated.

which a charge island is connected to the single reservoir, known as a single electron box (SEB). The sensor is configured under a single gate, L1, utilising the dot L1d, which is coupled to an electron reservoir and measured using the reflectometry circuit depicted in Figure 5.4(b). With this configuration, the addition of electrons to the dots within the left nanowire can be inferred from either the transport current $I_{\mathrm{SD,L}}$ through the device with source-drain bias $V_{\mathrm{SD}} = 4$ mV, seen in Figure 5.4(c), or the S_{11} reflectometry signal $\Delta\Phi/\Phi$ (measured at $V_{\mathrm{SD}} = 0$ V) seen in Figure 5.4(d), which maps the same gate voltage space. Both measurements contain structure attributed to multiple dots within the 2×2 array of the left nanowire. Due to the low transport current through the device, discerning the occupancy of the dots via transport is a significant challenge, while the capacitive shifts due to the addition of an electron are readily detected in reflectometry, which can probe all proximal quantum dots down to the last electron transition. The SEB dot-lead transitions at lower SEB electron numbers are less visible due to the reduction in tunnelling rates below the RF frequency of the reflectometry measurement.

5.2 Charge sensing in single SiNW

The core dimensions of all the different devices used to compile the data in this section are tabulated in Table 3.1. Devices which couple nanowires via floating gates are identified by the 'FL' key, while the remaining devices are '2S' devices with 2×2 arrays formed in a single SiNW. Example measurements from a 2×2 QDs array under a single nanowire are illustrated in the stability diagrams in Figure 5.3, showing double-dot behaviour for pairwise combinations of the four

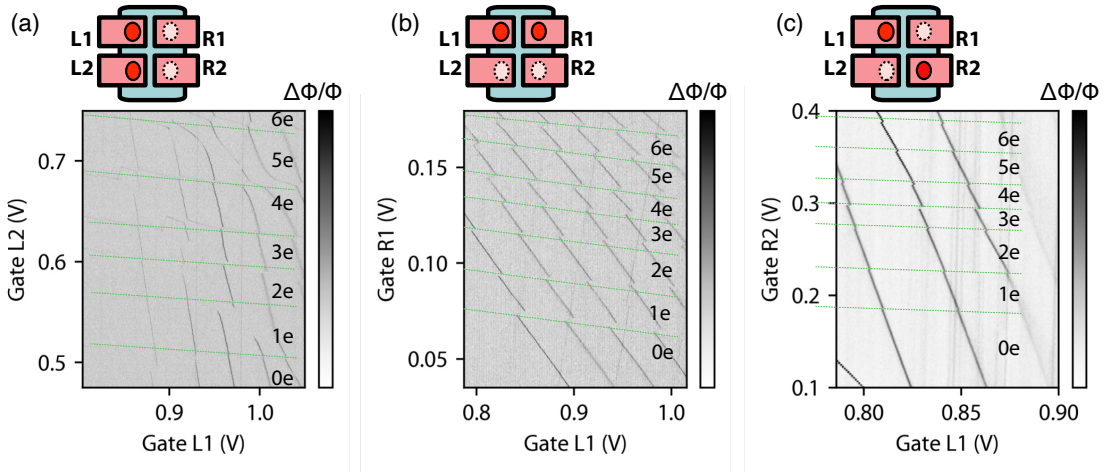


Figure 5.3 (a,b,c) charge stability diagrams showing all three dot-sensor(L1d) contributions in the 2×2 array, individually operated in a double-dot regime

voltage control inputs, demonstrating controllability over the four-dot locations. The stability diagrams are achieved by sweeping the corresponding control gate while holding the remaining voltages low enough to deplete the remaining dots to empty. Figure 5.3 shows from left to right, loading the first six electrons to dots D_{L2}, D_{R1} and D_{R2} in the '2S' device.

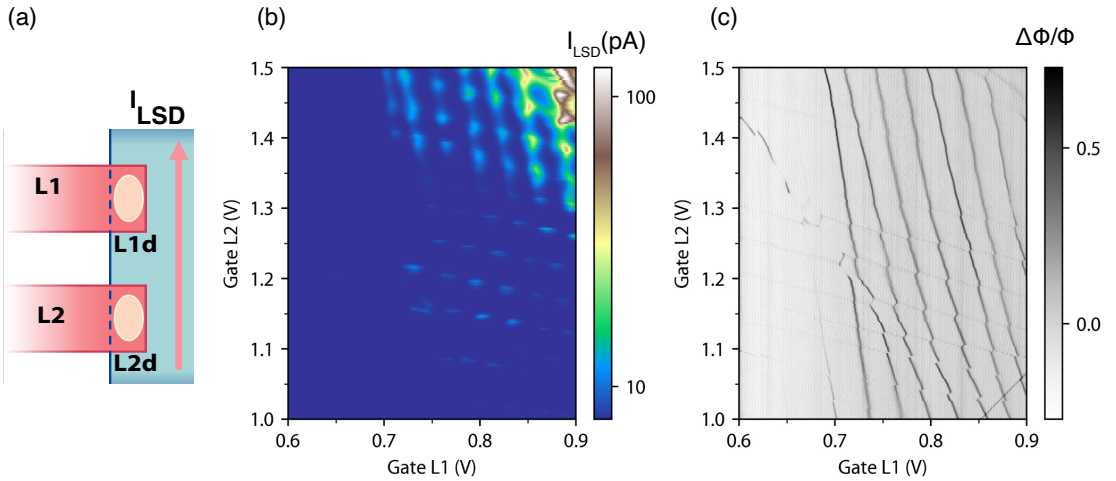


Figure 5.4 (a) Double-dot signatures within the SiNW through a transport current map of gate L1 vs L2 voltage-space with a Source-Drain bias 4 mV. (b)'single-electron box' sensor under gate L1. A zero-biased reflectometry measurement illustrates dot-lead charge transitions of the L1 sensor dot and capacitive shifts due to the addition of electrons to a local quantum dot defined under gate L2.

5.3 Remote sensing between two SiNWs

5.3.1 Charge sensing of quantum dots across SiNW

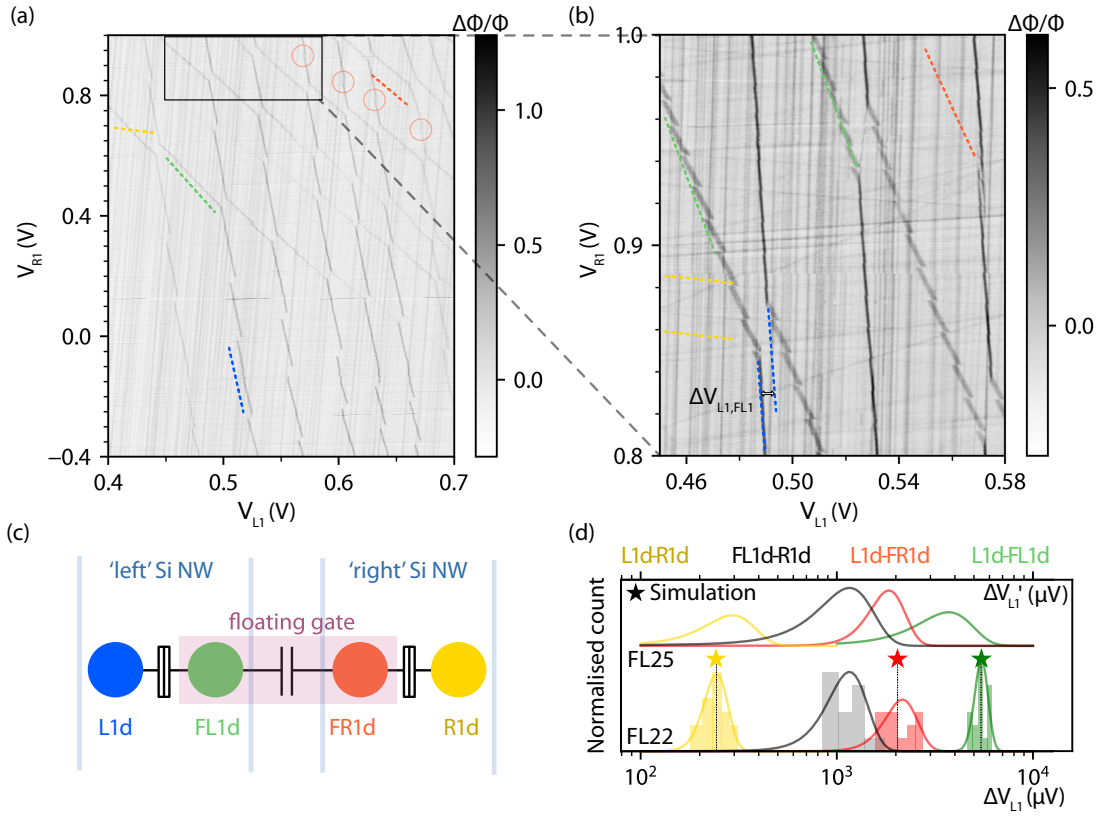


Figure 5.5 (a) Charge stability map in the L1 and L2 gate-space (top gate T potential $V_{\mathrm{T}} = 4\mathrm{V}$; V_{L2} and $V_{\mathrm{R2}} = -1\mathrm{V}$). (b) Zoom-in of (a) illustrates the different capacitive shifts of the sensor dot-lead transition due to loading electrons into different quantum dots along the floating gate direction. (c) Schematic of the remote sensing showing quantum dots as a network of charge nodes and capacitors. Dashed lines indicate dot-lead transitions in the stability diagram with corresponding quantum dot colour. (d) Histogram of capacitive shifts induced on the sensor dot by a charge transition in another quantum dot measured at various anticrossings, following the colour-coding in (c), normalised as a dot L1 Coulomb peak shifts ΔV. The coloured solid-line is the normalised fit to a Gaussian probability density function of the histogram, which attributes to the same quantum dot. (★) show calculated values from a COMSOL finite element simulation. Grey curves and histogram represent capacitive shifts from transitions in dot R1d measured using FL1d dot-lead transition. All data described above are from device 'FL22' — a normalised fit of the $\Delta V'$ histogram from a similar device 'FL25' is shown vertically offset above.

As the floating gates are galvanically isolated, the top metal gate T is used to assist in the accumulation of quantum dots under floating gates, primarily via

the mutual capacitance between gates F1, F2 and T. Simultaneously, both V_{L2} and V_{R2} are set to a depletion mode to avoid the formation of quantum dots under gates L2, R2 and F2, to effectively 'shut-off' the lower half of the device by electron depletion. With the voltage sweep of V_{L1} and V_{R1} shown in Figure 5.4(a), and noting the influence of the floating gate F1, which is capacitively coupled to both active gates, electrons can be loaded into dots L1d and R1d, as well as dots FL1d and FR1d, from their neighbouring reservoirs. Charge detection of these four distinct quantum dots is shown in the stability diagram measured in the reflectometry phase signal Figure 5.4(a). It includes the remote sensing of dots FR1d and R1d, located in the 'right' SiNW, detected by the sensor dot L1d, located in the 'left' SiNW. The sensor dot L1d is estimated to hold ≈10 electrons in this voltage range, where dot-reservoir charge transitions can be observed directly as a phase peak. Then the remaining three different quantum dots capacitively coupled to the sensor is identified through two complementary criteria:

(1) Through the ratio of cross capacitance between the two active gate voltages V_{L1} and V_{R1} and the dot.

(2) Through direct charge detection by the sensor dot, assessing the magnitude of the capacitive shift upon the sensor.

For the voltage map between V_{L1} and V_{R1} shown in Figure 5.5(a), each of the four dots capacitively couple to the L1 and R1 electrodes with differing strength, and the four quantum dots present with reference are illustrated to the colour code shown in the capacitance connectivity diagram of Figure 5.5(c). In Figure 4.3(a) and 4.3(b), the blue dashed line indicates the dot-lead charge transition of the SEB, L1, which naturally has the highest lever arm to V_{L1}. The other three coloured dashed lines highlight each remaining variety of dot-lead charge transition. The floating-gate-induced quantum dot in the left SiNW FL1d (green) is more strongly coupled to the sensor gate L1 due to its proximity, while in the SiNW on the right, the other floating-gate-induced quantum dot FR1d (red) and gate-induced quantum dot R1d (yellow) are more strongly coupled to gate R1. When quantum dot FL1d is sufficiently occupied, the increase in tunnel rates allows for FL1d dot-lead transitions to be directly detected in the reflectometry phase shift signal.

This signal allows us to trace the number of electrons in sensor dot L1d. This approach can be further quantified by comparing the cross-capacitance ratios $\alpha_{(i,j)}$ calculated as the degree to which gate L1 influences the other dot-lead transitions in voltage space. Assuming $\alpha_{(\mathrm{L1,L1})} = 1$, this method yields $\alpha_{(\mathrm{FL1,L1})} = 0.173$, $\alpha_{(\mathrm{FR1,L1})} = 0.124$, $\alpha_{(\mathrm{R1,L1})} = 0.005$. Therefore, a significant drop in the cross-capacitance ratio is apparent for groups of dots under spatially separated gates.

A second quantitative approach to distinguish the different quantum dots coupled to the sensor is to analyse the strength of the capacitive coupling between the sensor dot L1d and each of the remaining dots. Figure 5.5(d) shows the histogram of the shifts $\Delta V_{(\mathrm{L1},i)}$, expressed in terms of the gate L1 voltage V_{L1}, arising from the capacitive shift in the sensor dot L1d due to the addition of an electron to some other dot i [73]. I use a peak-finding algorithm near a capacitive shift of interest in Figure 5.5(b) and take the difference between the shifted dot-lead reflectometry peaks, extrapolated to the same value of V_{R1}. The capacitive shifts extracted in this way group naturally into three distinct sets, each corresponding to the transitions in another quantum dot indicated following the colour code in Figure 5.5(c). Being located in the same nanowire, FL1d (green) is the most strongly coupled to the sensor dot, while the other floating-gate-induced quantum dot FR1d (red), located in the remote nanowire, shows a slightly weaker coupling. The R1 gate-induced quantum dot R1d (yellow) in the remote nanowire shows the weakest coupling but can still be detected. A normalized fit of the probability density function of each group provides the mean capacitive shift referenced against the sensor dot gate voltage: $\Delta\overline{V}_{(\mathrm{L1,FL1d})} = 5.47$ mV, $\Delta\overline{V}_{(\mathrm{L1,FR1d})} = 2.16$mV, $\Delta\overline{V}_{(\mathrm{L1,R1d})} = 0.243$ mV. These values show good agreement to simulations of the capacitance matrix for this device structure.

As specific charge transitions FL1d are directly visible in the phase response, a corresponding capacitive shift between dots FL1d and R1d can also be extracted, which is the symmetric analogue to the sensor dot coupling through the floating gate to FR2d. Data corresponding to such $\Delta V_{(\mathrm{L1d,FR1d})}$ shifts are shown in grey in Figure 5.5(d), and indeed fall within a similar range to $\Delta V_{(\mathrm{L1,FR1d})}$. This asymmetry is not captured in our simulations and is most

likely due to finite lithographic misalignment between the patterns of the nanowire and the split between the gates. Based on automated overlay controls and tools specifications, I estimate that the cuts, although centred on the nanowires by design, are probably shifted by 5-10nm on a typical device. In this case, the asymmetry translates into stronger lever-arm parameters for the dots defined along the right edges of the nanowires and is systematically observed in other devices [146, 168]. Finally, to show the consistency of these values across different devices the fabricated on the same die, the same set of measurements are performed on a second device and plot the extracted Gaussian fits to $\Delta V_{(i,j)}$ for each pair of dots on the same axis in Figure 5.5(d).

To demonstrate the enhancement of capacitive coupling arising from the floating gates, I compare results from floating gate devices with those from devices with similar dimensions containing only single, isolated silicon nanowires. In order to facilitate the comparison of results from different devices, sensor dots and lever arms, I use a measure of the SEB sensitivity to the charge transitions in nearby quantum dots based on normalising the voltage-referenced capacitive coupling by the additional voltage required to add an electron to the SEB: $\Delta q = \Delta V_{(\mathrm{L1},i)}/V_{\mathrm{C_{L1d}}}$, where $\Delta V_{(\mathrm{L1},i)}$ is the detected voltage shift in V_{L1} arising from coupling to dot i, $V_{\mathrm{C_{L1d}}}$ is the change in V_{L1} required to add an electron to the sensor dot L1d.

I first study the normalised SEB charge sensitivity within a 2×2 quantum dot array in a single silicon nanowire. Here the inset of Figure 5.8 compares the capacitive coupling between dots formed on opposite edges of the nanowire, between adjacent dots formed along the common SiNW edge, and also between diagonally coupled next-nearest neighbour quantum dots. These configurations are shown in the inset, which illustrates configurations for sensing dots in a neighbouring SiNW, with coupling facilitated through the floating gate. The data in Figure 5.8 are obtained from three single-nanowire devices, each consisting of a 2×2 quantum dot array, as well as the corresponding single-nanowire arrays within two floating-gate devices. The *intra-wire* normalised sensitivities Δq fall off quickly with increasing separation between the quantum dots, though a single power-law cannot be used to describe the overall

trend with distance for all couplings due to the difference in mutual capacitance for dots located on the same or opposite edges of the nanowire.

5.3.2 Capacitance network model

In the COMSOL simulation, the quantum dots are modelled as conducting ellipsoids closely matching the asymmetric manifolds defined by a Schrödinger-Poisson study of the single electron effective mass approximation under the device geometry [190]. The dopants in the channel can also be modeled as perfect conductor with respect to its bohr radius. In the model of this section, only four quantum dots and surrounding gates are considered. As the device scales up, more quantum dots (dopants) and gates are included in the model which in turn add up to the total capacitance C_Σ of the sensor dot and slightly degrades the sensitivity. All the electrostatic interactions are summed up as the 'first order' mutual capacitances and 'second order' indirect capacitances.

In order to analyse the effect of the floating gate electrode, the second-order shift in the chemical potential of the sensor dot L1d of the form dot → FG → sensor is included. With respect to the simplified device capacitance network as shown in Figure 5.6, the floating gate is treated similarly to the quantum dots from Ref. [73], while maintaining a fixed charge to reflect the electrical isolation of the gate.

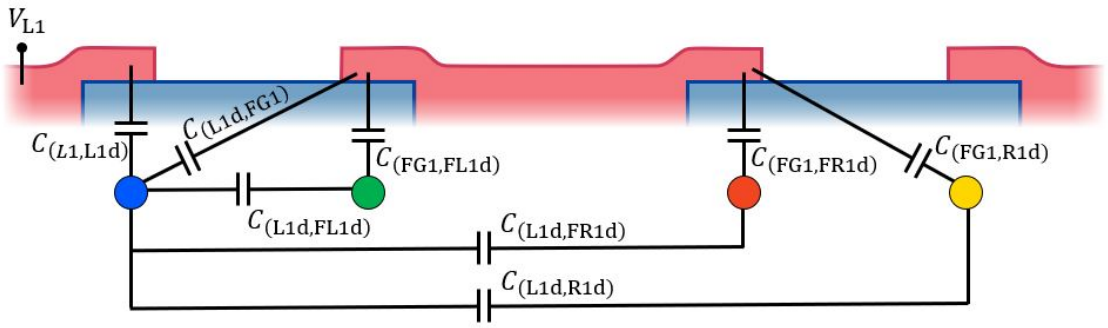


Figure 5.6 Simplified capacitive network of the dual-nanowire device illustrating a 1×4 array slice. The influence of the floating gate electrode is captured by the additional cross-capacitances highlighted.

Following the analysis in Ref. [73], a "first order" sensor voltage shift, which is due to the addition of an electron and direct dot-dot mutual capacitances is given by:

$$\Delta V^{(1)}_{(\mathrm{L1,FL1d})} = \frac{|e|}{C_{(\mathrm{L1,L1d})}} \cdot \frac{C_{(\mathrm{L1d,FL1d})}}{C_{\Sigma\mathrm{FL1d}}} \tag{5.1}$$

$$\Delta V^{(1)}_{(\mathrm{L1,FR1d})} = \frac{|e|}{C_{(\mathrm{L1,L1d})}} \cdot \frac{C_{(\mathrm{L1d,FR1d})}}{C_{\Sigma\mathrm{FR1d}}} \tag{5.2}$$

$$\Delta V^{(1)}_{(\mathrm{L1,R1d})} = \frac{|e|}{C_{(\mathrm{L1,L1d})}} \cdot \frac{C_{(\mathrm{L1d,R1d})}}{C_{\Sigma\mathrm{R1d}}} \tag{5.3}$$

where the elements can be extracted from the Maxwell capacitance matrix, detailed in Appendix.§(capacitance matrix) of the reference [190], for each data point in the parametric sweeps described in the main text. From Figure 5.7, it can be seen that this first-order effect is highly suppressed where there is a large separation between the dots, as the direct mutual capacitance between the dots and the SEB sensor L1d rolls off with distance with a power-law ranging from $\Delta q \propto d^{-3.0}$ to $d^{-2.5}$ (additional decay fits can be seen in Figure 5.7). Most of these decays fall close to the d^{-3} dependence measured for planar devices in silicon [149, 191], possessing a high density of metallic electrodes present that can contribute to a screening effect of the charge. This is contrasted with the face-to-face decay rate of $d^{-2.5}$, where most of the metal between the two dots has been removed. Now taking the effective shift in the floating gate into account, a "second-order" approximation to the sensor voltage shift is obtained:

$$\Delta V^{(2)}_{(\mathrm{L1,FL1d})} = \frac{|e|}{C_{(\mathrm{L1,L1d})}} \left[\frac{C_{(\mathrm{L1d,FL1d})}}{C_{\Sigma\mathrm{FL1d}}} + \frac{C_{(\mathrm{L1d,FG1})}}{C_{\Sigma\mathrm{FG1}}} \cdot \frac{C_{(\mathrm{FG1,FL1d})}}{C_{\Sigma\mathrm{FL1d}}} \right] \tag{5.4}$$

$$\Delta V^{(2)}_{(\mathrm{L1,FR1d})} = \frac{|e|}{C_{(\mathrm{L1,L1d})}} \left[\frac{C_{(\mathrm{L1d,FR1d})}}{C_{\Sigma\mathrm{FR1d}}} + \frac{C_{(\mathrm{L1d,FG1})}}{C_{\Sigma\mathrm{FG1}}} \cdot \frac{C_{(\mathrm{FG1,FR1d})}}{C_{\Sigma\mathrm{FR1d}}} \right] \tag{5.5}$$

$$\Delta V^{(2)}_{(\mathrm{L1,R1d})} = \frac{|e|}{C_{(\mathrm{L1,L1d})}} \left[\frac{C_{(\mathrm{L1d,R1d})}}{C_{\Sigma\mathrm{R1d}}} + \frac{C_{(\mathrm{L1d,FG1})}}{C_{\Sigma\mathrm{FG1}}} \cdot \frac{C_{(\mathrm{FG1,R1d})}}{C_{\Sigma\mathrm{R1d}}} \right] \tag{5.6}$$

where the $C_{(\mathrm{L1d,FG1})}$ term represents the coupling between the sensor and the floating gate, and $C_{(\mathrm{FG1},i)}/C_{\Sigma i}$ represents the charge capacitively induced on the floating gate, distributed by a factor of $1/C_{\Sigma\mathrm{FG1}}$. It is the total capacitance of the floating gate which is then subject to geometrical dependencies upon the parameter sweeps. The comparisons within Figure 5.7(a) illustrates that, for sensing dots in the remote nanowire, the second-order contribution due to the floating gate is dominant, giving rise to the advantage of the floating gate electrodes for long-

range capacitive sensing.

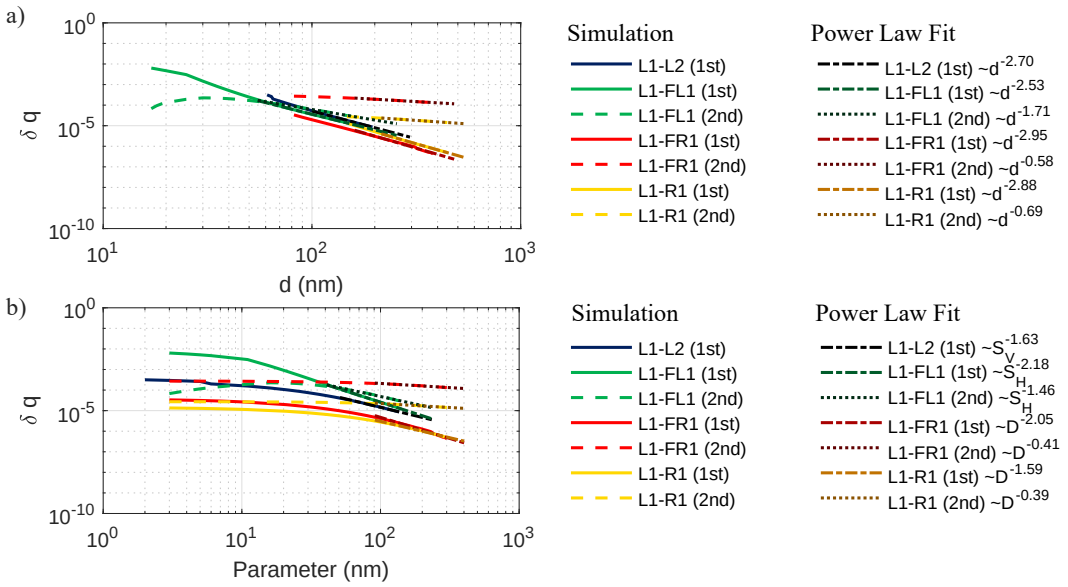


Figure 5.7 (a) Illustration of the first order and second order solutions to the detected charge on the sensor, normalised to sensor dot charge, as a function of the dot-dot separation. (b) Illustrates the decay rate as a function of the design elements within the device architecture.

While the core aim of this section is to compare the additional sensitivity to charge movements in remotely located quantum dots as facilitated by the floating gate, for completeness, this second-order effect of the floating gate also enhances the sensitivity to FL1d (located within the same nanowire as the sensor but under the floating gate). Such an enhancement is absent for the equivalent dot in a single-nanowire 2×2 array, where all electrodes are pinned to a supply voltage, and the trend lines are shown in the main text for face-to-face dots in the same nanowire; therefore, consider only this first-order effect.

5.3.3 Sensitivity decay over distance

The effects of dot separation on mutual capacitance have been studied in the reference [149, 191], I quantify the effects of the specific design parameters of these nanowire QD devices on the mutual capacitance. As shown in Figure 5.7(b) the x-axis is rescaled so that it is with respect to the input design parameters described in Figure 5.2 and Table 3.1. Here the trends plateau as each design parameter begins to approach the size of the quantum dot, moving to a regime which would be physically challenging to realise in fabrication. The reduction in

sensitivity due to the input parameter follows a different trend when compared to the dot-dot distance d. The reduction in sensitivity due to the face-to-face gap between electrodes S_h is the largest, at $\Delta q \propto S_\mathrm{h}^{-2.18}$, reduced to $\Delta q \propto S_\mathrm{h}^{-1.46}$ when this dot is located beneath a floating gate. The S_v gap between the two gates along the nanowire gives rise to $\Delta q \propto S_\mathrm{v}^{-1.63}$. For the floating gate, the dimensions of the floating gate contribute to the self-capacitance of the electrode, which, in turn, contributes to the decay in sensitivity. For the floating gate geometry in this work, $\Delta q \propto D^{-0.41}$ is obtained. However, this could be subject to further device optimisation, outside the scope of this work but discussed in the context of GaAs planar devices in reference [192].

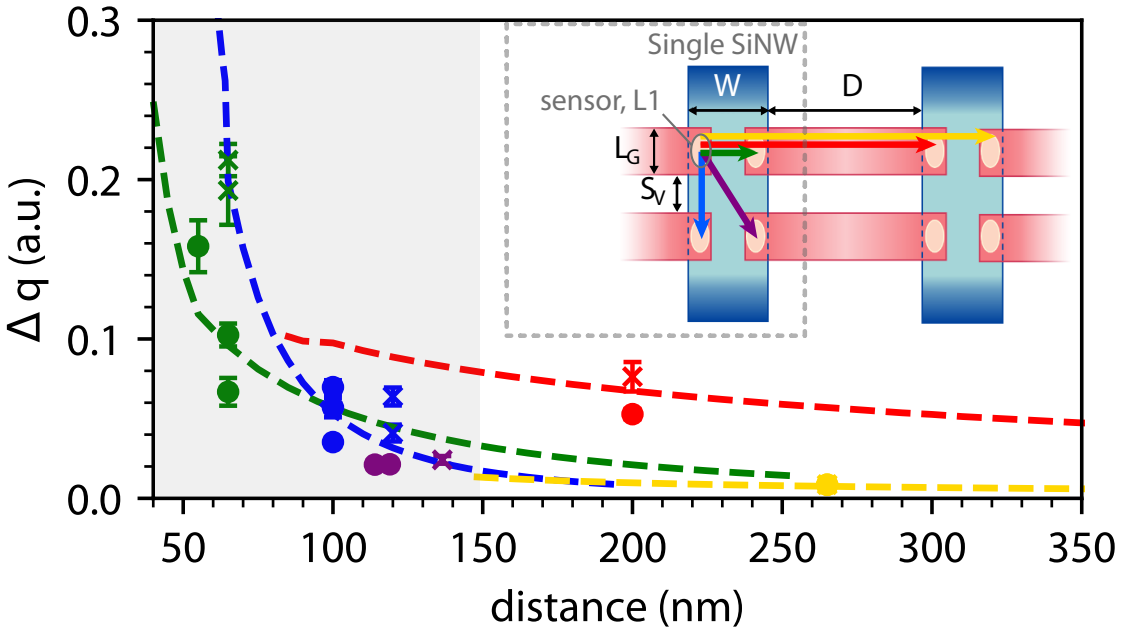


Figure 5.8 Voltage shifts in the sensor dot arising from capacitive coupling to other quantum dots are normalised against the addition voltage of the individual SEB to compare measurements from two floating gate devices and three single-nanowire devices (×, $L_\mathrm{g} = 60$ nm; ◯, $L_\mathrm{g} = 50$ nm). Arrows in the inset illustrate the type of sensing: green, blue and purple data points relating to sensing within a single-nanowire and are obtained from both types of devices. Red and yellow data points required floating gate devices). COMSOL simulations are used to obtain parameter sweeps relating to each class of dot being sensed, following the colouring in the inset — a single normalisation is applied to all simulated curves. Error bars in the data include the uncertainties in both the capacitive voltage shifts and addition voltages.

Modelling the quantum dot as conducting ellipsoids, the Maxwell capacitance matrix for varying centre-to-centre dot separation d is calculated, along with other

nanowire design parameters. Each of the parametric sweeps from the simulations (dashed lines in Figure 5.8) settles to a power-law attributed to each sensor-dot configuration: nearest-neighbour couplings along the edge of the nanowire (L1d-L2d) or across the nanowire (L1d-FL1d) have couplings which decay approximately as $\Delta q \propto d^{-2.8}$ or $d^{-2.5}$ respectively, over the range of distances studied here. Data for a next-nearest neighbour configuration L1d-FL2d, where the dots are positioned diagonally across the wire, is shown for completeness but not modelled. For the 'remote sensing' configuration where charge transitions are detected through the floating gate, the normalised capacitive coupling is sustained over a much greater distance, as reflected in the experimental data and simulations. By sweeping the floating gate length (approximated to be the SiNW separation, D) simulations show that the two dots under each corner of the floating gate have a coupling which is dominated by the second-order capacitive coupling via the floating gate at these distances, and decays only as $\propto D^{-0.4}$. Combined with the additional spacing of the nanowire width local to the SEB, this results in an coupling decay for the dot L1d-FR1d configuration which can be approximated as $\Delta q \propto d^{-0.6}$ in the range studied here. As a result, the mutual capacitive shift for dot L1d-FR1d remains relatively high, even at distances exceeding 300 nm, as shown in Figure 5.8.

Coupling the sensor to dot R1d now involves three degrees of separation from the sensor, with a corresponding drop in sensitivity for short separations. However, the action of the floating gate leads to a much more gradual decay in sensitivity with the distance that goes as $\Delta q \propto d^{-0.7}$ in our simulations. As a result, for distances above $d \approx 220$ nm, the floating gate mediated coupling between dots arranged on opposite edges of *different* nanowires exceeds that from two dots on opposite edges of the same silicon nanowire. Furthermore, the charge distribution due to floating gate geometry could be optimised to yield a stronger absolute coupling while maintaining the much more gradual decay with distance [192].

The above experimental measurements and simulations indicate decays in capacitive coupling strength which fall off more slowly than $\propto d^{-3}$, as previously observed within arrays of Si/SiGe planar quantum dots [191, 193]. However, such measurements were made within planar quantum dot devices with a high density

of metallic gate electrodes, expected to screen mutual capacitive coupling. Indeed, considering only the first-order approximations to capacitive couplings, our simulations also show decays that approach d^{-3}. In contrast, the devices studied here contained a relatively low density of metallic gate electrodes. The fabrication of the split-gates involved the etching of metal that is then substituted by SiN. The result is a reduced decay rate in sensitivity as a function of dot-dot separation — most strikingly when facilitated by the capacitively coupled floating gate. Instead of screening charge movement, the floating gate propagates the effect of charge movement over a distance to be chosen as a design parameter, coupling charge between two otherwise separate silicon structures. While the simulations can capture well the trends in the different classes of coupling, the residual spread in experimental values across the measurements may be due to the asymmetry in realistic devices, not captured by the simulations, which can influence not only the dot to dot geometrical distance but also the device lever arms.

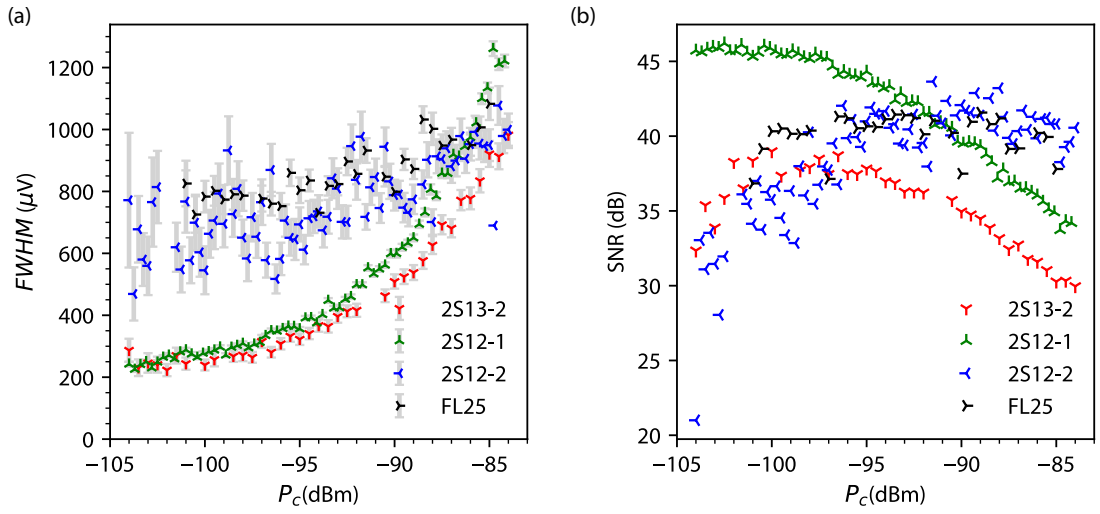


Figure 5.9 (a) Sensor dot-lead signal linewidth full width half maximum (FWHM) as a function of power delivered at device. (b) Power SNR as a function of power delivered at device with integration time 0.4 ms.

The capacitive shifts measured between QDs, both locally and on distinct nanowires, are well above the full width at half-maximum (FWHM) of the SEB dot-lead charge transition. The RF-power dependence of different sensor dot-lead transitions is measured against the input carrier power Pc at resonance frequency to observe the broadening of sensor linewidth FWHM and its impact on the

power SNR as shown in Figure 5.9. Power SNR in Figure 5.9(b) is defined between signal Coulomb peak and background noise. The measurement integration time is 0.4 ms. All four dot-lead linewidths reach intrinsic limits (due to dot-lead tunnel rates and near neighbour reservoir electron temperature) for $P_C \leqslant -90$ dBm. The selected dot-lead transition of 'FL25' and '2S122' experience much higher tunnel rates which in term lead to lower SNR. When $P_C \geqslant -90$ dBm, the dot-lead linewidths are dominated by the effects of the RF drive used in the reflectometry measurement, with a corresponding degradation in SNR. Assuming a Lorentzian lineshape for the measured SEB charge transition, any capacitive shift greater than twice the FWHM gives at least 94% of the maximum sensor contrast (e.g. for spin-dependent tunnelling readout). Based on our simulations and the intrinsic FWHM of the sensor transition of 0.24 mV, dot L1d-FR1d type couplings mediated by the floating gate could be used to achieve spin readout for distances up to 500 nm without a reduction in readout contrast.

In addition to applications for sensing, the capacitive coupling has been used to realise local multi-qubit interactions in various systems, including singlet-triplet qubits [194] and charge qubits [195, 196]. Meanwhile, several approaches to scaling quantum dot arrays pursue long-range coupling between qubits to facilitate the integration and fan-out of control electronics and suppress charge leakage [36, 183]— solutions to realising such two-qubit gates include exploiting an RKKY mediating exchange interaction [182, 183] or coupling via a superconducting resonator [197]. Multi-qubit operations utilising capacitive coupling via floating gates, coupling two singly-occupied planar dot structures, have been proposed to produce a spin-spin coupling Hamiltonian $H_{S-S} \simeq J_{12}(\sigma_x^1\sigma_x^2 + \sigma_y^1\sigma_y^2)$ when the Zeeman energy $E_Z \gg J_{12}$ and where $\sigma_{x,y,z}$ are the Pauli matrices in the relevant qubit basis [192], which can be used to implement the iSWAP operation [198]. Combining the assumptions within Ref [[192]] with the parameters of the devices studied here and spin-orbit coupling strength for silicon [199], a coupling of $H_{S-S} \simeq 10^3$ Hz is estimated under realistic device operating conditions between FL1d and FR1d with nanowire separation $\sim$ 200nm, which is too weak for practical applications.

However, utilising the floating gate to couple two singlet-triplet qubits via $H_{\mathrm{ST-ST}} \simeq J_{12}/2((\sigma_z - I) \otimes (\sigma_z - I))$ [194], where I is the identity matrix, exploits the much stronger electric-dipole coupling to achieve the CZ operation. For the nanowire geometry presented here (i.e. with singlet-triplet qubits arranged on each nanowire and the nearest dots of each pair separated by $\sim$ 200nm), $H_{\mathrm{ST-ST}} \simeq 10^{12}$ Hz via the model in Ref. [[192]] is obtained, this leads to an even more favourable coupling approach in this geometry due to reduced oxide thickness. In Si/SiGe devices, coupling between charge qubits $H_{\mathrm{C-C}} \simeq g/4((I - \sigma_z) \otimes (I - \sigma_z))$ mediated by the mutual capacitance term [195, 196] has been demonstrated with a strength of $\approx$ 15 GHz over dot separations of 130 nm [196], while for the device geometry studied here the results predict $H_{\mathrm{C-C}} \simeq 10^{11}$ Hz for dots separated by 200 nm on different nanowires.

5.4 Sensing scheme for scaling up

In the long SiNW device with 2×N (N⩾3) QD array, only the QD at both ends of the SiNW close to the reservoir can function as a dot-lead sensor. The SEB sensor relies on constant cyclic interaction between the single carrier and reservoir. This mechanism limits the sensing range of the SEB sensor. It is possible to extend the reservoir to the middle of SiNW but at the cost of the original gate-defined QD area. Therefore it is interesting to investigate if IDT transition can function as an internal/external sensor in the middle of the SiNW 2×N QD area. The IDT signal between double QD, once tuned, does not reply on cyclic exchange with a nearby reservoir and is also less affected by reservoir temperature.

Figure 5.10 shows the scheme for the proof of concept experiment to use the IDT between QD L1d and R1d to sense the charge transition of L3d and R3d. A frequency multiplexed circuit (see 3.2.3 for the details of circuit and resonator) is used with resonators RF1 and RF2 attached to Gate L1 and Gate R3. Only one tone is sent to the device when performing the charge sensing experiment. The 2×3 device is first tuned up to the inter-dot transition of L1d and R1d by resonator-RF1 reflected phase ϕ_1 as shown in Figure 5.10(a) and then switched to the inter-dot transition of L3d and R3d sensed by resonator-RF2 reflected phase ϕ_2. When the

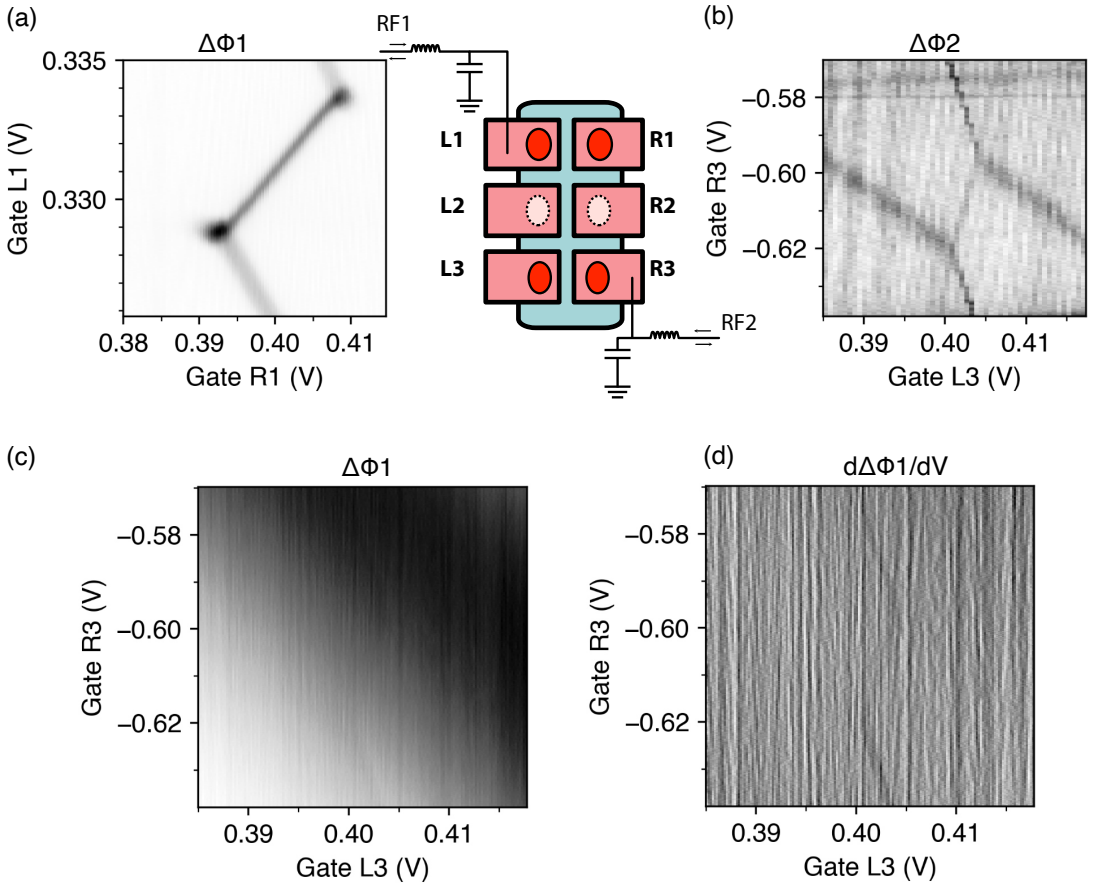


Figure 5.10 Charge stability diagram of a 2×3 QD device measured using frequency multiplexed circuit. (a) charge stability map of L1d and R1d with ϕ_1. (b) charge stability map of L3d and R3d with ϕ_2. (c) charge stability map of L3d and R3d with ϕ_1 signal, background showing the IDT of L1d and R1d. (d) charge stability map of derivative of ϕ_1 signal for illustration of L3d and R3d charge transition

gate space of interest is mapped out, the following charge sensing experiments is done with Gate L1 and R3 fixed at the IDT of double QD while sweeping the Gate L3 and R3 across the double QD of L3d and R3d. Gate compensation is not applied in this experiment. Therefore the IDT of L1d and R1d can be seen in the background of the stability diagram as shown Figure 5.10(c). Compared with the stability diagram from in-situ sensor RF2, the signals of L3d and R3d are much less visible and not suitable for qubit readout experiments as expected from previous benchmarking experiments in Figure. 5.8 when dot-to-dot distance $d > 150$ nm, the capacitive shift is smaller than the FWHM of the sensor signal. Considering the practical QD size and gate pitch in silicon, it is ideal for performing charge sensing experiments in the unit of 2×2 of QD array to prepare for later qubit experiments. Furthermore, the proof of concept sensing scheme with IDT is viable but with a smaller distance.

With a simple 2×2 QD array, it takes a well-trained quantum engineer a few hours or even days to find the optimal operation point of interest. As the device scales up to 2×N array, the complexity and difficulty of such task grows quadratically with N. Automatic detection of signal and search for qubit operation point is therefore desirable. A neural network[1] is then developed and trained to predict the gradients from the θ histogram (where θ is the set of angles between the x-axis and the normal to the charge transitions) acquired from the Hough transform of the data-set [200]. The gradient of dot-lead and inter-dot transition(IDT) can reveal the cross capacitance ratio in a 2×2 QD array and can be used to construct a virtual gate. The gradient of the 2D map can be obtained by converting the map into Hough space:

$$\rho = x \cdot \cos(\theta) + y \cdot \sin(\theta) \tag{5.7}$$

The simplified steps for the automatic protocol are as follows: 1. Import raw data of charge stability diagram. 2. Put threshold and binarise map into scattering data points (x, y). 3. Convert data points into Hough space (ρ, θ) according to Equation. 5.7. 4. Extract histogram of θ values distribution to a neural network. 5. The predicted gradients are then used to extract the partial transformation

[1]The author acknowledge Giovanni A. Oakes for implementation of neural network

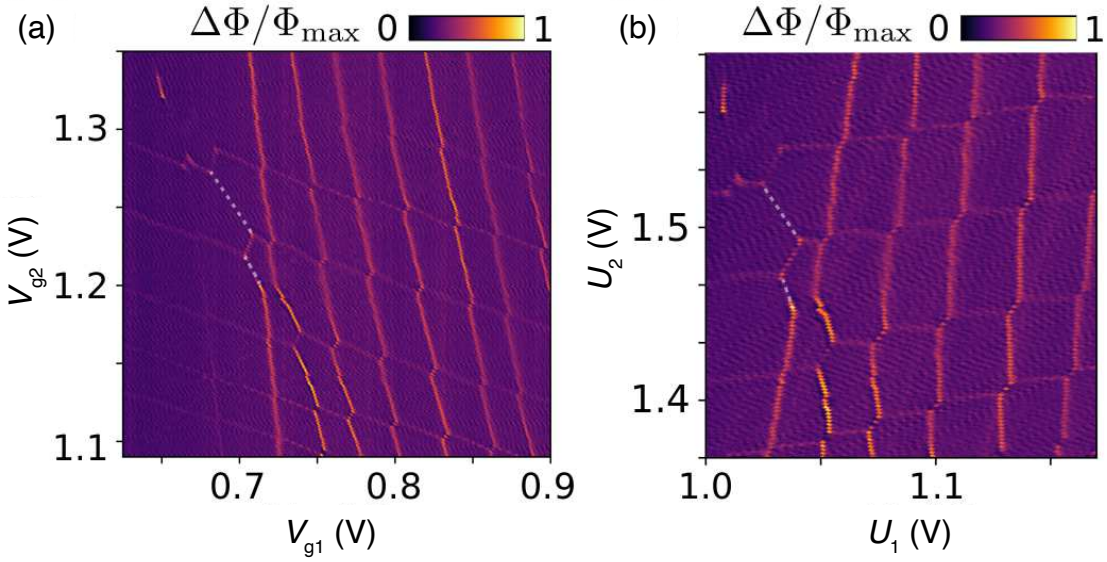


Figure 5.11 (a) Charge stability diagram of a 2×2 QD device measured using RF reflectometry. The z-axis represents the normalised phase shift of the reflected signal where high-intensity regions indicate charge transition, and intrude QD is highlighted by the white dashed line. (b) Data is partially rotated into virtual voltage space predicted by the neural network.

matrix. 6 Apply partial transformation to obtain virtual voltage space.

In Figure 5.11, the trained neural network is tested on experimental data of a 2×2 QD array. The predicted partial virtual voltages shows an average angle between the dot-lead transitions in virtual voltage space of 89.28±0.44°, approaching the ideal 90°.

5.5 Conclusion

This Chapter has demonstrated through experiments and simulation the effect of integrating floating gate electrodes to extend the sensitivity range of a single capacitive sensor, highlighting, in particular, the potential to couple quantum dots located on distinct silicon nanowires.

The action of the floating gate between neighbour silicon nanowire leads to a gradual decay in sensitivity with the distance that goes as $\Delta q \propto d^{-0.7}$ in our simulations compared with the $\propto d^{-3}$, as previously observed within arrays of Si/SiGe planar quantum dots. As a result, for distances above $d \approx 220$ nm, the floating gate mediated coupling between dots arranged on opposite edges of *different* nanowires exceeds that from two dots on opposite edges of the same

silicon nanowire. Based on our simulations and the intrinsic FWHM of the sensor transition of 0.24 mV, dot L1d-FR1d type couplings mediated by the floating gate could be used to achieve spin readout for distances up to 500 nm without a reduction in readout contrast. Furthermore, with the simulation results, the coupling between the singlet-triplet qubits $H_{\mathrm{ST-ST}}$ arranged on each nanowire and the nearest dots of each pair separated by $\sim$ 200nm) can be as high as 10^{12} Hz. For long bilinear quantum dot arrays, a proof-of-concept sensing via the inter-dot transition is demonstrated. This could be utilised for in-array quantum dots

Chapter 6

Dispersive readout of a donor-dot spin system

This Chapter introduces a silicon nanowire device implanted with bismuth dopants. The gate-induced quantum dot and a single bismuth dopant form a double quantum dot system. Using the gate-based sensing technique, Pauli spin blockade is observed in the double quantum dot system. The binding energy of the bismuth dopant is measured to be 77 meV*, and the excited energy of triplet states on the bismuth dopant is measured as* 0.773 meV*. With the pulsing scheme, the relaxation time between the singlet and triplet states on the donor-dot system are measured to be* 14 µs *and* 17 µs *at magnetic field of 1.2 T. This work provides a novel implementation of a possible spin qubit in silicon and opens up new research directions on hybrid donor-dot spin qubit*

6.1 Donor in silicon

Group-V dopant in silicon (donor) is an ideal quantum dot to host the electron and nuclear spin qubits. In Kane's seminal work[201], an array of phosphors-donors in silicon electronic device is proposed to act as nuclear spin qubits. Since then, single phosphors atom has been experimentally demonstrated via two main fabrication techniques: scanning tunnelling microscope lithography [76] and deterministic single ion implantation [202]. High-fidelity readout and quantum control have been successfully demonstrated in ^{31}P nuclear

spin qubit [50, 78, 203]. However, nuclear spin resonance is much slower than the electron spin resonance causing a slow gate time in the corresponding qubit system. Electrons hosted on donor cluster[204] or donor-dot system [205] stand out as it combines the fast gate time of electron and long coherence time of donor nuclear spin [206]. The hyperfine coupling term is utilised as an extra knob for electron-electron interaction other than exchange coupling [207] and could also be exploited for long-range coupling[208]. Electron spin readout has been demonstrated in the other Group-V donor Antimony (Sb) [209]. Furthermore, it is possible to utilise the quadrupole interaction to electrically drive the single ^{123}Sb nuclear spin state coherently [79]. Other donors such as As and Bi are reported to have quadrupole effects. And ^{209}Bi with a nuclear-spin, $I = 9/2$, also offers the potential to access a even larger Hilbert space than ^{123}Sb $I = 7/2$. The large hyperfine coupling ($A = 1.48\,\mathrm{GHz}$) of bismuth also leads to so-called 'clock transition' ($df/dB \to 0$) for noise resilient ESR transitions at low magnetic field [80].

6.2 Ionised charge state of donor

The SiNW device corresponding to the '1S26D' Device listed in Table 3.1 has the gate length $L_g = 40\,\mathrm{nm}$ and nanowire width $W = 70\,\mathrm{nm}$. Two face-to-face split gates wrap onto the nanowire with a separation between the gates $S_v = 40\,\mathrm{nm}$. Furthermore, this SiNW channel is doped with bismuth with the average of one dopant under each gate defined by the ion-implantation process. The fabrication details are described in Chapter 3.1.2. As shown in Figure 6.1(a), both gates are supplied with the DC voltage, which can electrically induce quantum dots in the corners of the nanowire. The RF signals are applied to the Gate1 for RF reflectometry readout, and the pulse signal is applied to Gate2 for fast manipulation of the charge and spin state of the QDs.

The charge transitions for the quantum dots and donors in the device can be mapped out by sweeping the gate voltages V_{G1} and V_{G2} while monitoring the phase of the reflected RF signal. The reflectometry signal depends on the tunnelling rate of DRT; not all DRT is visible in the stability diagram in

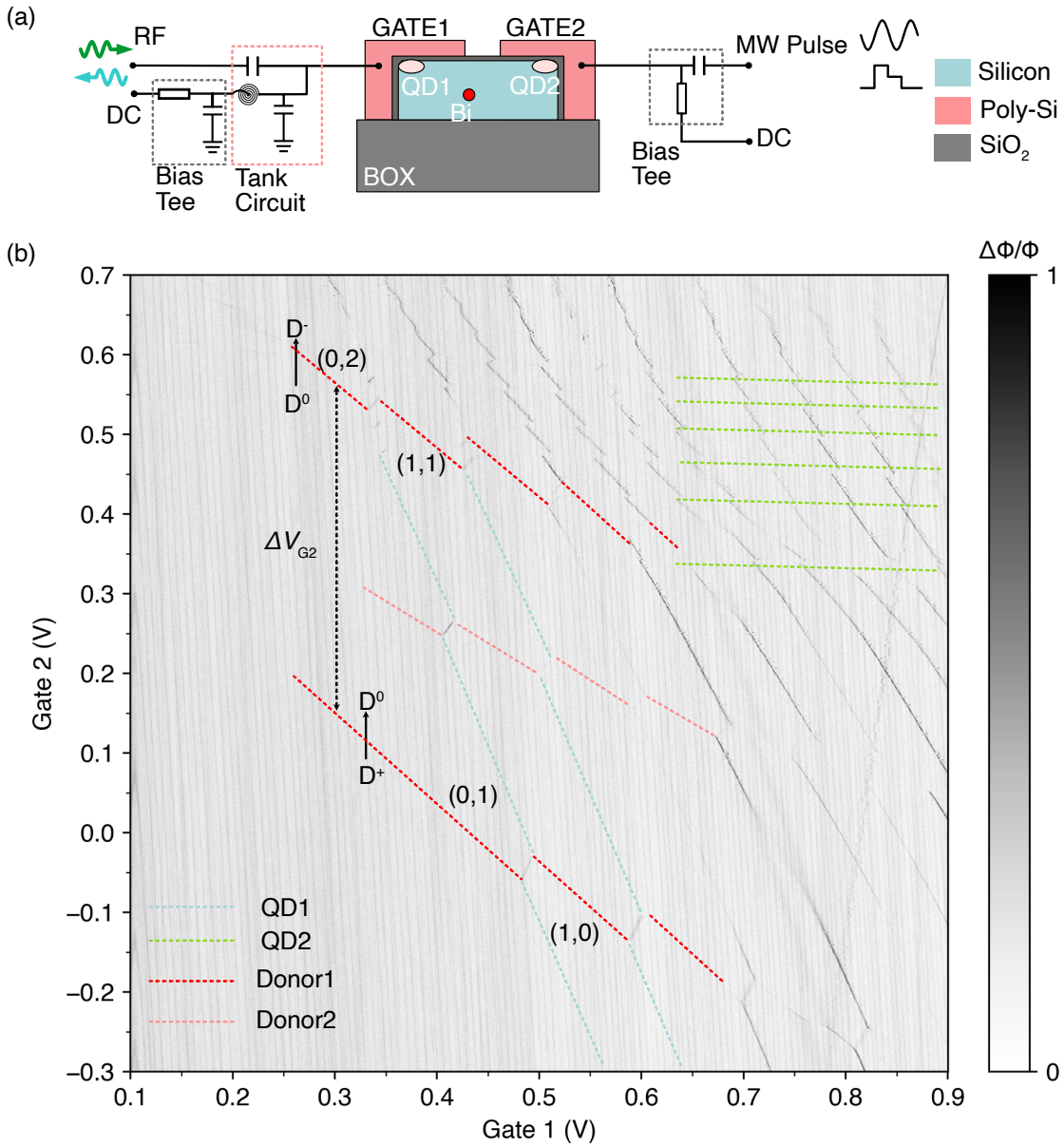


Figure 6.1 (a) cross-section schematic of the bismuth-dopped SiNW device with readout circuit connected to Gate1 and pulse circuit connected to Gate2; (b) normalized phase response of the reflected signal showing the stability diagram as the function of the gate voltages V_{G1} and V_{G2} with the dot-to-reservoir transition of QDs and donors (dashed line).

Figure 6.1(b). If the dimensionless slope $\frac{\Delta V_{G2}}{\Delta V_{G1}}$ between the two active gate voltages is used to group the dot-to-reservoir transitions to corresponding QDs. The donor1-to-reservoir transitions has the slope of -1.1 as illustrated by the red dashed line in Figure 6.1(b). There are two transitions representing $D^+ \leftrightarrow D^0$ and $D^0 \leftrightarrow D^-$ charge transitions of the donor1. The donor2-to-reservoir transition (pink dashed line) has the slope of -0.73 and only the first transition is visible in the stability diagram. In Figure 6.1(b) $(n_{\mathrm{QD1}}, n_{\mathrm{donor1}})$ represents the number of electrons confined in the QD1 and donor1 respectively. And the following parts of this Chapter focus on the inter-dot transition (IDT) (1,0)-(0,1) and (1,1)-(0,2) of this QD-donor system. The charging energy of the donor is measured to be $E_{\mathrm{C}} = \alpha_{(\mathrm{G2-donor})}\Delta V_{\mathrm{G2}} = (77 \pm 4)\,\mathrm{meV}$ where $\alpha_{(\mathrm{G2-donor})}$ is the lever arm of Gate2 on donor and ΔV_{G2} is the charging voltage between the $D^+ \leftrightarrow D^0$ and $D^0 \leftrightarrow D^-$ charge transitions. The experimentally measured charging energy for neutral isolated bismuth donor in silicon is 71 meV. As a comparison the charging energy for phosphors donor has been experimentally measured to be 45 meV [210, 211]

6.3 Pauli blockade of donor-dot

This section focuses on the spin states of two electrons hosted on the donor-dot system. Firstly, the rf amplitude response from the gate sensor is plotted in Figure 6.2(a) as G1 and G2 sweep slowly across the (1,1) to (0,2) inter-dot transition. As the magnetic field increases, the T_- at IDT becomes the ground state at $\varepsilon = \varepsilon_0$ due to the Zeeman splitting. The magnetic field is chosen as $B = 3\,\mathrm{T}$ and the $S_0 - T_-$ anticrossing sits far away from the zero-detuning point (ε_0) so that the rf tone does not drive the $S_0 - T_-$ states during measurement of S_0 hybridised states. Then, a continuous two-level pulse is applied to Gate 2 with a 50 ns load level sitting at the (0,1) region and 950 ns measure level sitting at the IDT region while G1 and G2 sweep slowly across the same voltage space as Figure 6.2(a). Two distinctive traces corresponding to the hybridised states of S_0 and T_- are visible in the pulse-on stability diagram as shown in Figure 6.2(b). As shown in energy- detuning plot Figure 6.2(c), both S_0

and T_- are not ground states. The full Hamiltonian of the donor-dot system, including the hyperfine coupling term, is described in Appendix B.

The load time of the two-level pulse is set longer than the tunnelling rate of QD1 to allow the loading of the electron and shorter than the relaxation time of excited two-electron spin states to preserve the population of excited states. After the load level, the mixture of singlet and triplet states created at the (0,1)-(1,1) transition is pulsed to the corresponding bias to measure the quantum capacitance as the curvature of eigenenergy due to the interdot tunnel coupling. Admittedly, this two-level pulse is not the best way to obtain the maximised signal for S_0 and T_- individually but a good method to measure two states in the same stability diagram. The interdot tunnel coupling for S_0 and T_- states at 3 T are extracted as $\Delta_S = 9.4\,\mathrm{GHz}$, $\Delta_{T_-} = 19.5\,\mathrm{GHz}$.

Pulse spectroscopy at magnetic field $B = 3\,\mathrm{T}$ for different pulse amplitude is plotted in Figure 6.2(d). Here, a 50% duty-cycle square wave pulse at 1 MHz is applied to Gate 2 as it sweeps slowly across the (0,1)-(1,1) and (1,1)-(0,2) transitions as indicated by the black dashed line in stability diagrams. For QD1 $0 \leftrightarrow 1$ transition, the square wave splits the signal as the amplitude of the pulse increases. Pulsing on and off, the QD1 has a similar signal strength. For hybrid S_0 states, the signal only appears at the blue dashed line area, where a mixture of states (left: $\varepsilon > \varepsilon_{QD1}$) or the ground state (right: $\varepsilon > \varepsilon_{ST_-}$) is available. Similarly, for hybridised T_- states, the signal is only presented where a mixture of states (left: $A > 0.8$ mV) or the ground state ((left: $A < 0.8$ mV)) is available. Magnetospectroscopy of the QD1 dot-to-reservoir and inter-dot-transition is plotted in Figure 6.2(e). For the DRT, a single spin is concerned ($m_s = 1/2$) and the Zeeman splitting shifts $0 \leftrightarrow 1$ transition ε_{QD} downwards, while for $T_-(1,1)$ state at (1,1)-(0,2) IDT ($m_s = 1$), Zeeman splitting shifts $T_-(1,1)$ down and causes the $S_0 - T_-$ crossing ε_{ST_-} upwards. The slope of the two charge transitions due to Zeeman spliting are determined by $\frac{\Delta B}{\Delta V} = \frac{\alpha}{m_s \mu_\mathrm{B} g}$. The centre of voltages of ε_0, ε_{ST} from pulse spectroscopy at different magnetic fields and ε_{QD}, ε_{ST_-} from the magnetospectroscopy are plotted in Figure 6.2(f) from the Lorentz fit. By performing the linear fit of the ε_{QD}, ε_{ST_-} values against the magnetic fields, the lever arms on QD1 and donor1 from

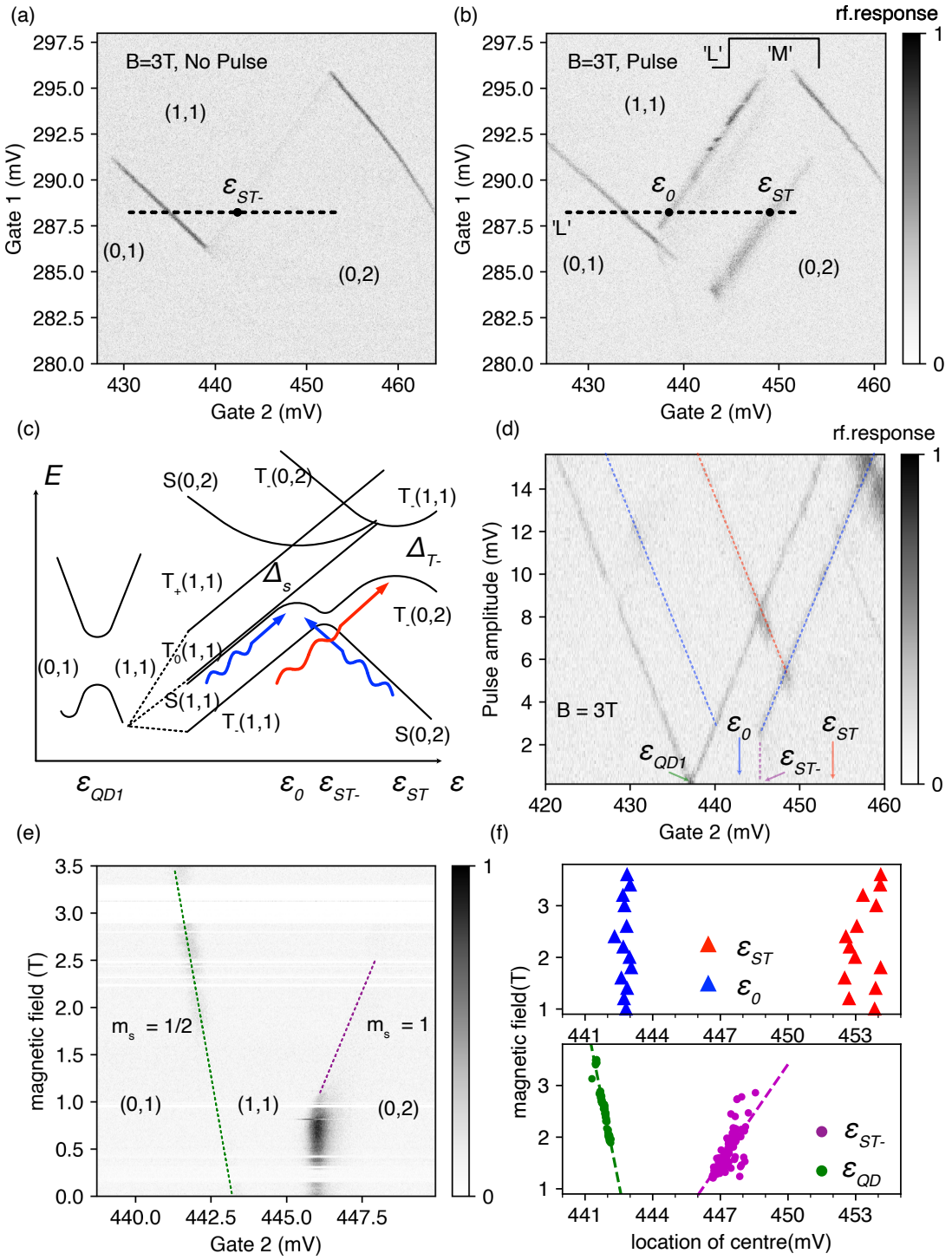


Figure 6.2 (a) stability diagram of donor-dot system at the (1,1)-(0,2)transition at 3 T; (b) stability diagram of donor-dot system at the (1,1)-(0,2)transition at 3 T with a two-level pulse; (c) the energy level diagram showing the quantum dot charge transition and the two-electron spin states; (d) Pulse spectroscopy with 50% duty-cycle square wave at magnetic field $B = 3\,\mathrm{T}$, the pulse amplitude is converted to actual gate voltage after line attenuation; (e) Magnetospectroscopy of the QD1 DRT and donor-dot IDT signal; (f) fitted centres of signal peak for different energy state at different magnetic field.

Gate 2 are extracted to be $\alpha_{(\mathrm{G2-QD})} = 0.127 \pm 0.004$ and $\alpha_{(\mathrm{G2-IDT})} = 0.073 \pm 0.010$. As a result, the lever arm on donor from gate 2 $\alpha_{(\mathrm{G2-donor})} = \alpha_{(\mathrm{G2-IDT})} + \alpha_{(\mathrm{G2-QD})} = 0.20 \pm 0.01$ [118] can also be obtained for charging energy in previous section.

The zero-detuning of hybrizied S_0 state ε_0 and hybridized T_- state ε_{ST} stay unchanged with magnetic field. This is expected as the Zeeman splittings of $S_0(1,1)$, $S_0(0,2)$ states is zero and Zeeman splittings $T_-(1,1)$, $T_-(0,2)$ is of the same value $\mu_B g \Delta B$. Therefore the zero-detuning of hybridized T_- and hybridized T_0 is the same. The excited orbital state of the two spin state in donor E_{ST} can be measured by $e\alpha_{(\mathrm{G2-IDT})}(\varepsilon_{ST} - \varepsilon_0) = (0.773 \pm 0.106)\,\mathrm{meV}$. This energy is also observed in Figure 6.2(b) as the distance between the visible traces $S_0(0,2)$ and $T_0(0,2)$ in the pulse-on stability diagram at 3 T.

6.4 Spin dynamics in donor-dot

In this section, spin dynamics of the $S_0 - T_-$ states is investigated. A two-level pulse (Pulse1) is used to measure the relaxation time (T_1) of $S_0 \to T_-$ and $T_- \to S_0$ process around the $S_0 - T_-$ anticrossing. The pulse starts at the detunning ($\varepsilon_1 > \varepsilon_{ST_-}$) with certain load time (t_{load}). This prepares a mixture of S_0 and T_- states depending on t_{load}. The detuning is then pulsed to zero-detuning (ε) to measure the S_0 signal. The measure time (t_{measure}) is set as 60 µs during which the S_0 fully relaxed to T_- ground state. The signal of the $S_0 \to T_-$ relaxation process is plotted in Figure 6.3(b) which are averaged over 8000 rf response traces. The rf response (fitted from the exponential decay as in inset of Figure 6.3(b) at zero detuning has the time constant of 14 µs. The long measure time always prepare the ground state T_- at zero detuning, therefore the triplet population at the beginning of Pulse1 is close to 1. By varying the total duration of t_{load}, the $T_- \to S_0$ at ε_1 can be measured. This relaxation process is plotted as the averaged rf response for different t_{load} in Figure 6.3(c). An exponential decay is fitted to the response and produce $T_{1,T_- \to S_0} = (17 \pm 1)\,\mu\mathrm{s}$.

Landau–Zener (LZ) sweeps [212] are used to characterise the gap size of $S_0 - T_-$ anticrossing. The $S_0(0,2)$ state is prepared as detuning ε sweeps through the

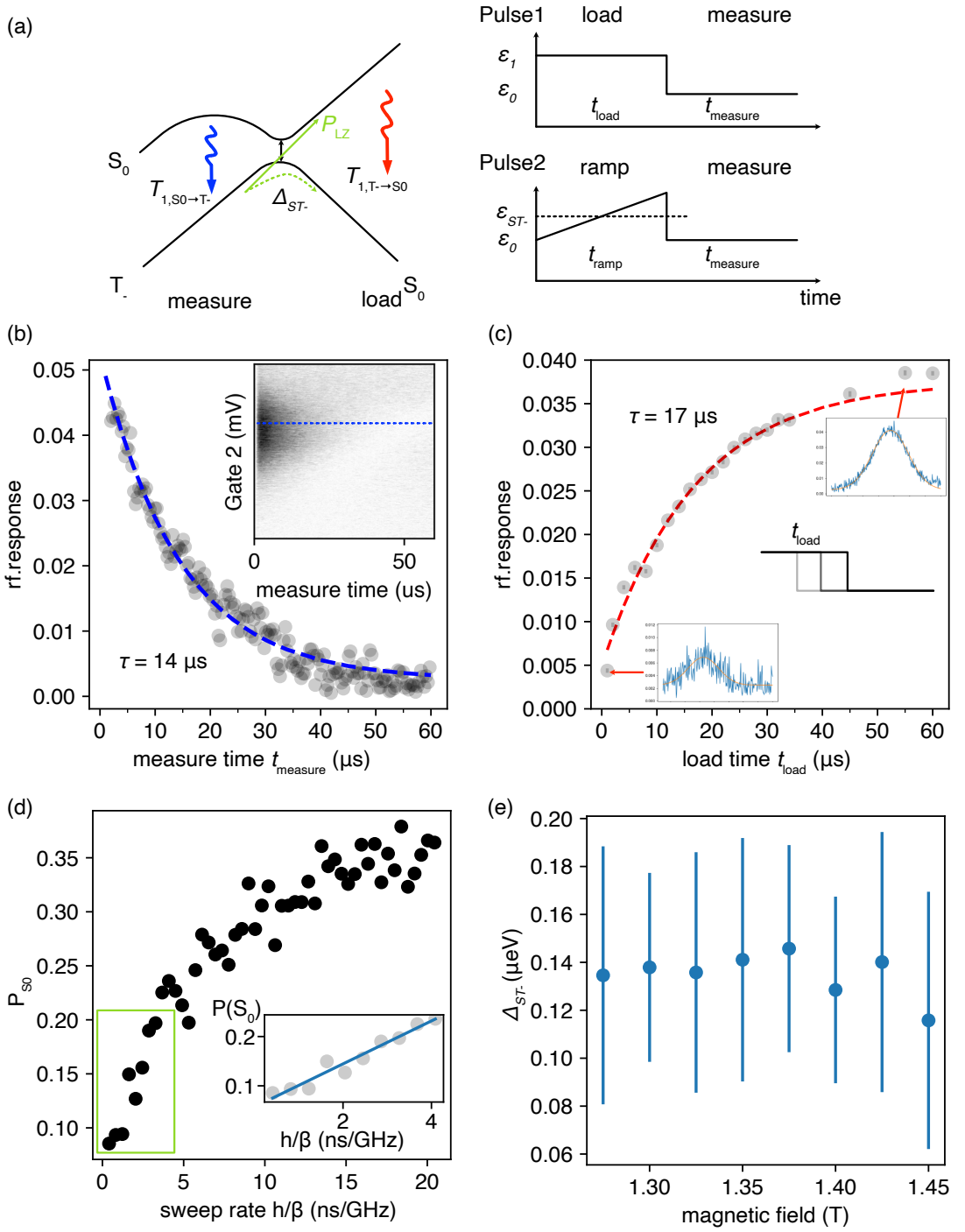


Figure 6.3 (a) Anticrossing of the S_0 and T_- state and the pulse sequences used for spin relaxation (Pulse1) and LZ sweep (Pulse2) ; (b) rf response during the measure time (t_{measure}) of Pulse1 showing the exponential decay of $S_0 \rightarrow T_-$, the inset shows the decay over different Gate 2 bias; (c) averaged rf response for different Pulse1 as the function of the total load time t_{load}; (d) Data for a series of LZ sweeps with varying ramp rates, the horizontal axis is represented by h/β in the unit of ns/GHz), inset: data and linear fit for fast sweeps such that $P_{S_0} < 0.25$. (e) extracted Δ_{ST_-} for different magnetic field

anticrossing ε_{ST_-} with varying rates. In Pulse2 shown in Figure 6.3(d), this is achieved by changing the total duration of load time (t_{load}). The probability for an $S_0 - T_-$ transition is given by the LZ formula [212, 213]

$$P_{\mathrm{S_0}}(t) = 1 - \exp\left(\frac{-\left(2\pi\left|\Delta_{\mathrm{ST_-}}(t)\right|^2\right)}{\hbar\beta}\right) \tag{6.1}$$

where $\beta = d(E_{T_-} - E_{S_0})/dt$ is the sweep rate, with E_{S_0} and E_{T_-} representing the the energies of the S_0 and T_- levels.

Following the LZ sweep, $P_{\mathrm{S_0}}(t)$ is the singlet return probability. The return probabilities P_{S_0} is normalized against the rf response of fully relaxed $S(2,0)$ states measured as Figure 6.3(c). The return probability P_{S_0} is plotted as the function of ramp rate (h/β). To accurately measure Δ_{ST_-}, a linear fit is performed for fast sweep at $P_{S_0} < 0.25$ as shown in the inset of Figure 6.3(d). Δ_{ST_-} is found to be (138 ± 40) neV at 1.25 T. The Δ_{ST_-} values at different magnetic field are plotted in Figure 6.3(e). The experiments are mainly operated at $B > 1$ T where $S_0 - T_-$ anticrossing sits at $S(0,2)$ side far from zero-detuning, the hyperfine coupling is close to zero due to its dependence of charge hybridization [208]. In this regime, the hyperfine coupling of the single bismuth nucleus has a minimum effect on $S_0 - T_-$ anticrossing and $S_0 - T_-$ anticrossing mainly from the spin-orbit interaction. The measured Δ_{ST_-} value is similar to the spin-orbit coupling measured in isotopically enriched ^{28}Si singlet-triplet qubit [214]. P_{S_0} saturates less than 1 in the LZ sweep experiments, which has been attributed to charge noise during pulsing by reference [88].

6.5 Conclusion

This Chapter has studied the charge and spin dynamics of a donor-dot system formed by a gate-induced quantum dot and a single bismuth dopant. The ionised charge state of the bismuth donor is observed via the inter-dot transition in the double quantum dot system. The binding energy of ion-implanted bismuth in silicon nanowire is measured as 77 meV. Furthermore, excited energy of triplet states on the bismuth dopant is measured as 0.773 meV via pulse spectroscopy

experiment. With careful choice of pulsing scheme, the relaxation time of $S_0 \rightarrow T_-$ and $T_- \rightarrow S_0$ at 1.2 T is measured as 14 µs and 17 µs respectively. LZ sweep allows for probing the energy of $S_0 - T_-$ anticrossing probing $\Delta_{ST_-} = (138 \pm 40)$ neV. This is attributed mainly to spin-orbit coupling due to the charge dependence of the hyperfine coupling at high magnetic field.

Chapter 7

Conclusion and outlook

In this Chapter, I summarise the main achievements and discuss future directions of related research questions in this thesis.

7.1 Achievements

7.1.1 Dispersive readout of ambipolar quantum dots

This work demonstrates several core ingredients which can be used to benchmark electron and hole spin qubits in the same silicon device. The RF readout of the inter-dot transition is the basis of Pauli-blockade-based spin measurement. The minimum integration time of current experiment is 160 (100) µs for electrons (holes) which can be theoretically brought down to 100 ns with choice of gate, resonator frequency and JPA. Furthermore, the electron and hole dot-lead charge transition detected by RF reflectometry can compare the electron-phononn and hole-phonon in the same silicon chip. The effective electron temperature (85 ± 15) mK and (72 ± 14) mK is measured for n-type and p-type reservoir respectively. In the thermometry experiment, the noise broadening of dispersive signal can be detrimental to the accuracy of effective electron temperature. An optimized gate sensor with shorter minimum integration time can be used to eliminate the white noise and two-level-fluctuator noise.

7.1.2 Charge sensing via floating gate

This work has demonstrated through experimenting and simulating effect of integrating floating gate electrodes to extend the sensing range of a single capacitive sensor, highlighting, in particular, the potential to couple quantum dots on distinct silicon nanowires. Different capacitive coupling strengths within single silicon nanowire and neighbour silicon nanowires are presented. With the floating gate, a gradual decay in sensitivity with the distance that goes as $\Delta q \propto d^{-0.7}$ in our simulations compared with $\propto d^{-3}$, as previously observed within arrays of Si/SiGe planar quantum dots. Based on the simulations and the intrinsic FWHM of the sensor transition, the coupling between quantum dot across the different nanowire mediated by the floating gate can be used to achieve spin readout for distances up to 500 nm without a reduction in readout contrast. Finally, a sensing scheme with inter-dot transition is also briefly discussed.

7.1.3 Charge and spin dynamics of a bismuth donor-dot system

This work has experimentally demonstrated a single ion-implanted bismuth donor coupled to the gate-induced quantum dot. The ionised charge state of the bismuth donor is observed using the gate-based rf sensor. Furthermore, Pauli spin blockade is observed in the two-electron donor-dot spin system. The binding energy, excited electron triplet states of the bismuth dopant are measured to be 77 meV and 0.773 meV respectively. This is the first experimental report of these values for shallow bismuth dopant in silicon. Moreover, relaxation time T_1 between singlet and triplet states from different pulsing experiments is measured as $T_{1,S_0 \to T_-} = 14\,\mu s$, $T_{1,T_- \to S_0} = (17 \pm 1)\,\mu s$. Using the LZ sweep, $\Delta_{ST_-} = (138 \pm 40)\,neV$ is measured for the $S_0 - T_-$ anticrossing at 1.2 T which mainly comes from spin-orbit coupling in silicon.

7.2 Future diections

7.2.1 CMOS qubit

The complementary combination of NMOS and PMOS is the key to low-power modern electronics. The interplay of electron and hole spin qubit can also benefit silicon quantum computing. In silicon, ambipolar p-n double quantum dot formation is difficult to measure through direct transport current due to the energy bandgap of silicon— RF readout of the dot-lead charge transition can enable neighbouring quantum dots to be sensed as in the capacitive shift of sensor transition at zero source-drain bias [190]. Furthermore, an experimental platform which hosts both electron and hole spin qubit can utilise the long coherence time of electron spin and all-electrical control of hole spin for optimised silicon qubit.

7.2.2 Long distance electrostatic coupling

In future devices with overlapping gate architecture [193], the second layer of gate electrodes can be used independently tune the quantum dots confined under the floating gates and achieve remote interactions. Given the substantial promise of spin qubits formed along the quasi-1D arrays, along the edges of silicon nanowires [146], the enhanced capacitive couplings measured here using floating gates provide a potential route to couple qubits distributed across individual nanowires and thus for scaling in a second dimension. On the other hand, temperature dependence of the capacitance network model and electrostatic coupling is worth investigating. It can help the circuit optimization when interfacing silicon qubit with low temperature electronics and also provide insights for 'high temperature' spin qubit [215] that operates at above $SI1$K.

7.2.3 Hyperfine driven singlet-triplet spin qubit

For our donor-dot system, a further study of the singlet-triplet states at a low magnetic field is required to resolve the spin funnel of the donor-dot system. Different pulsing schemes can be developed to utilise LZ sweep to control the

bismuth nuclear spin state via $S_0 - T_-$ anticrossing. Hyperfine-driven singlet-triplet qubit has been demonstrated with gate speed 57 MHz in the phosphors donor-dot system. The high nuclear spin $I = 9/2$ and large hyperfine $A = 1.48$ GHz of bismuth donor can produce an even higher driving frequency, ranging from 300 MHz to 3 GHz depending on the nuclear spin state.

Appendix A

Noise analysis of dot-to-reservoir signal

Considering the Gaussian noise present at the quantum dot coupled to its nearby reservoir; the tunnelling capacitance is given as:

$$C_{\mathrm{t}} = \frac{e^2\alpha^2}{4k_BT_e}\cosh^{-2}\left(\frac{\varepsilon + S_{\mathrm{i}}}{2k_BT_e}\right) \tag{A.1}$$

where S_{i} follows the gaussian distribution of the noise which moves the centre of the capacitive response.

The fitted FWHM for averaged signal over 10000 samples of white noise is plotted in Figure A.1(a). The fitted data aligns perfectly with the convolution of the gaussian distribution and the signal trace, which effectively describes the noise-broadened signal similar to the tunnel-rate broadened signal. For the different level of Gaussian noise plotted as a function of the sampling size, the FWHM initially stay unaffected for a small number of samples and start to saturate to a noise-broadened regime for a large number of samples.

For the two-level-fluctuator noise at $f = 10\,\mathrm{kHz}$, the broadened signal is plotted as a function of the integration time for different TLF noise amplitude S_{m} in Figure A.1(c).

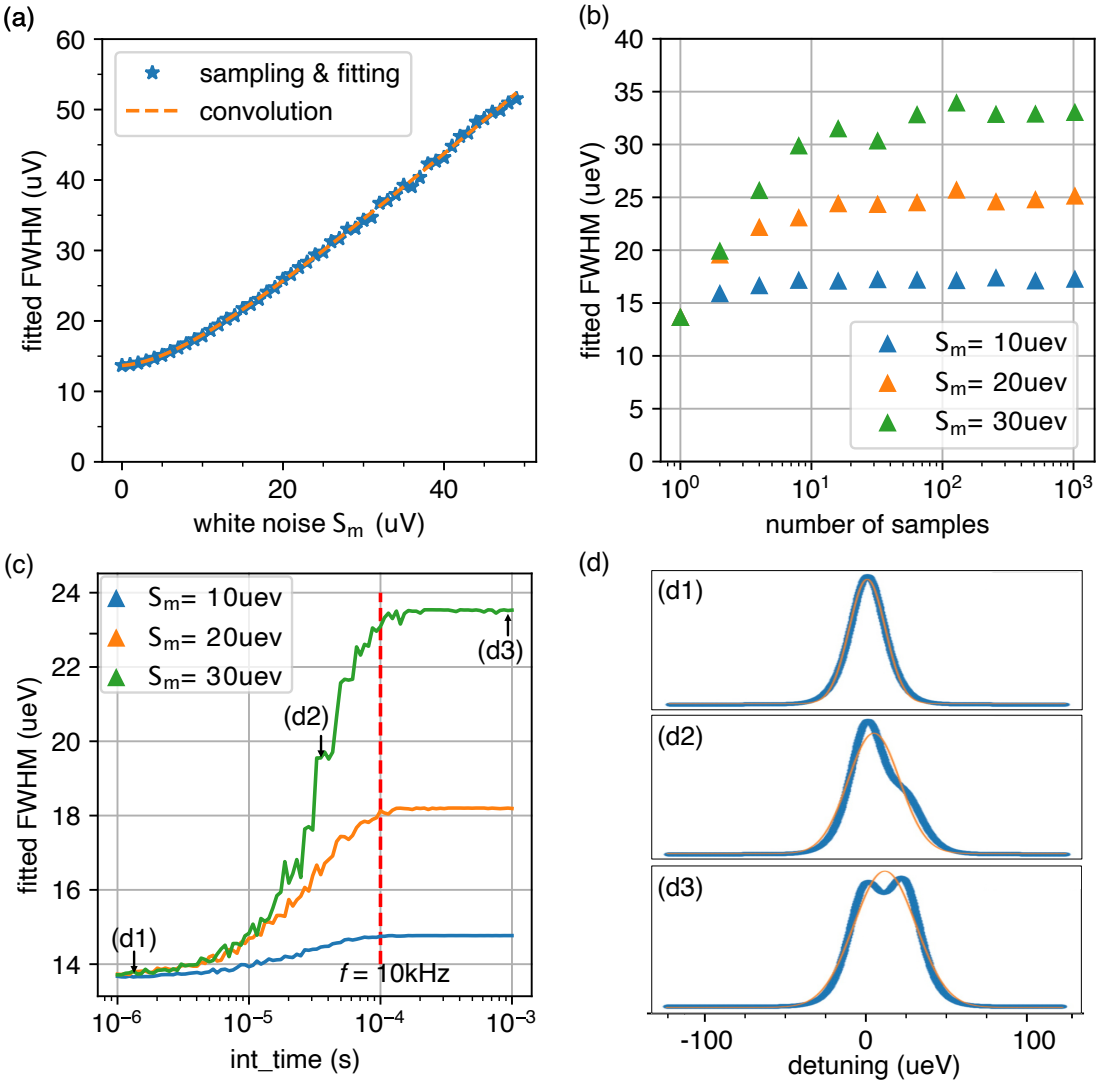


Figure A.1 (a) Fitted FWHM for $\star$: sampling of white noise on the temperature broadened signal and $--$: convolution of the gaussian distribution and temperature broadened signal; (b) Fitted FWHM for white noise broadened signal as a function of the sampling size for different white noise sigma S_{m}; (c) Fitted FWHM for TLF noise at $f = 10\,\mathrm{kHz}$ broadened signal as a function of the integration time for different TLF noise amplitude S_{m}; (d) line trace at three different regime of the TLF noise broadened signal shown in (c).

Appendix B

Hamiltonian of donor-dot electron spin system

The spin hamiltonian for the donor dot system in constructed in Wolfram Mathematica notebook with the physical parameters taking the following values : $AA = 1.475\,169 \times 10^9\,\mathrm{Hz}$, $J = 0$, $\mathrm{g_{donor}} = 2$, $\mathrm{g_{dot}} = 2$, $\mathrm{g_n} = 0$, $\mu_B = 9.27 \times 10^{-24}/6.63 \times 10^{-34}\mathrm{Hz\,T^{-1}}$, $t = 9.4\,\mathrm{GHz}$. The overall matrix is too big to shown and also contain eigenstate such as $T_0(0,2)$ and $T_+(0,2)$ not paticular relavant in this thesis. In theory the complete hamiltonian should also be as large 80×80 matrix, here only the $S(0,2)$ state for $I = 9/2$ are included in the and other the $T(0,2)$ states are excluded in this simulation. The construction of this 50×50 hamiltonian matrix is shown in Figure B.1.

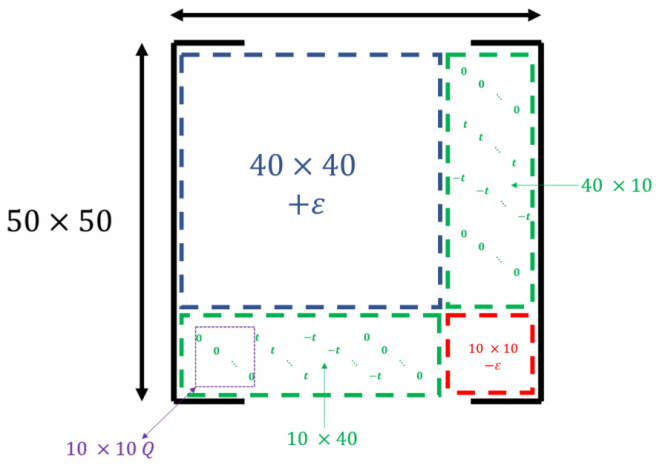


Figure B.1 schematic of 50×50 matrix of donor-dot system.

Electron spin matrices (Electrons always S=1/2):

In[1]:=
```
(Sz=PauliMatrix[3]/2);
(Sx=PauliMatrix[1]/2);
(Sy=PauliMatrix[2]/2);
```

Nuclear spin matrix:

In[2]:=
```
(Spin=9/2);
(dim=2Spin+1);
(Ix=Table[(DiscreteDelta[i-j+1]+DiscreteDelta[i-j-1])1/2
Sqrt[Spin(Spin+1)-(-Spin+i-1) (-Spin+j-1)],{i,dim},{j,dim}]);
(Iy=Table[(DiscreteDelta[i-j+1]-DiscreteDelta[i-j-1])(1/2i )
Sqrt[Spin(Spin+1)-(-Spin+i-1) (-Spin+j-1)],{i,dim},{j,dim}]);
(Iz=Table[(DiscreteDelta[i-j])(Spin-i+1) ,{i,dim},{j,dim}]);
(FullSimplify[Ix]);
(FullSimplify[Iy]);
(FullSimplify[Iz]);
```

Combine Matrices:

In[3]:=
```
(IIz=KroneckerProduct[IdentityMatrix[4],Iz]);
(IIx=KroneckerProduct[IdentityMatrix[4],Ix]);
(IIy=KroneckerProduct[IdentityMatrix[4],Iy]);
(SSx_dot=KroneckerProduct[Sx,IdentityMatrix[dim*2]]);
(SSy_dot=KroneckerProduct[Sy,IdentityMatrix[dim*2]]);
(SSz_dot=KroneckerProduct[Sz,IdentityMatrix[dim*2]]);
(SSz_donor=KroneckerProduct[IdentityMatrix[2],Sz,IdentityMatrix[dim]]);
(SSx_donor=KroneckerProduct[IdentityMatrix[2],Sx,IdentityMatrix[dim]]);
(SSy_donor=KroneckerProduct[IdentityMatrix[2],Sy,IdentityMatrix[dim]]);
```

Build Spin Hamiltonians for the (1,1) states:

In[4]:=
```
(H_hyper=AA((SSz_donor.IIz)+(SSy_donor.IIy)+(SSx_donor.IIx)));
(H_exch=J((SSz_donor.SSz_dot)+(SSx_donor.SSx_dot)+(SSy_donor. SSy_dot)));
(H_Zee=Bμ_B(g_donorSSz_donor+g_dotSSz_dot));
(H11_tot=(H_hyper+H_exch+H_Zee);
```

Add the (2,0) state:

```
In[5]:= (H_Big=ArrayFlatten[
        {{H11_tot-DiagonalMatrix[ConstantArray[ϵ,dim*2*2]],
        SparseArray[{},{dim*2*2,dim}]},{SparseArray[{},{dim,dim*2*2}],
        g_n B Iz +DiagonalMatrix[ConstantArray[ϵ,dim]]}]);
```

Add the tunneling terms between S(1,1) and S(2,0):

```
In[6]:= tmat=t IdentityMatrix[dim];
        zerodim=SparseArray[{},{ dim,dim}];
        (H_tunnel=ArrayFlatten[{
        {zerodim,zerodim,zerodim,zerodim,zerodim},
        {zerodim,zerodim,zerodim,zerodim,tmat},
        {zerodim,zerodim,zerodim,zerodim,-tmat},
        {zerodim,zerodim,zerodim,zerodim,zerodim},
        {zerodim,tmat,-tmat,zerodim,zerodim}}]);
        (H_All=H_Big+H_tunnel);//MatrixForm
```

Figure B.2 shows eigenstates of the 50×50 hamiltonian matrix plotted as the function of detuninng energy at three different magnetic field: B = 0 T, B = 0.2 T, B = 2 T. At B = 0 T, the eigenstates due to hyperfine coupling overlapped with its corresponding singlet/triplet states. Each cluster contains 10 $(2*I+1)$ eigenstates. The $T_0(1,1)$ and $S_0(1,1)$ are seperated by zero-field splitting of 7.3 GHz [80].

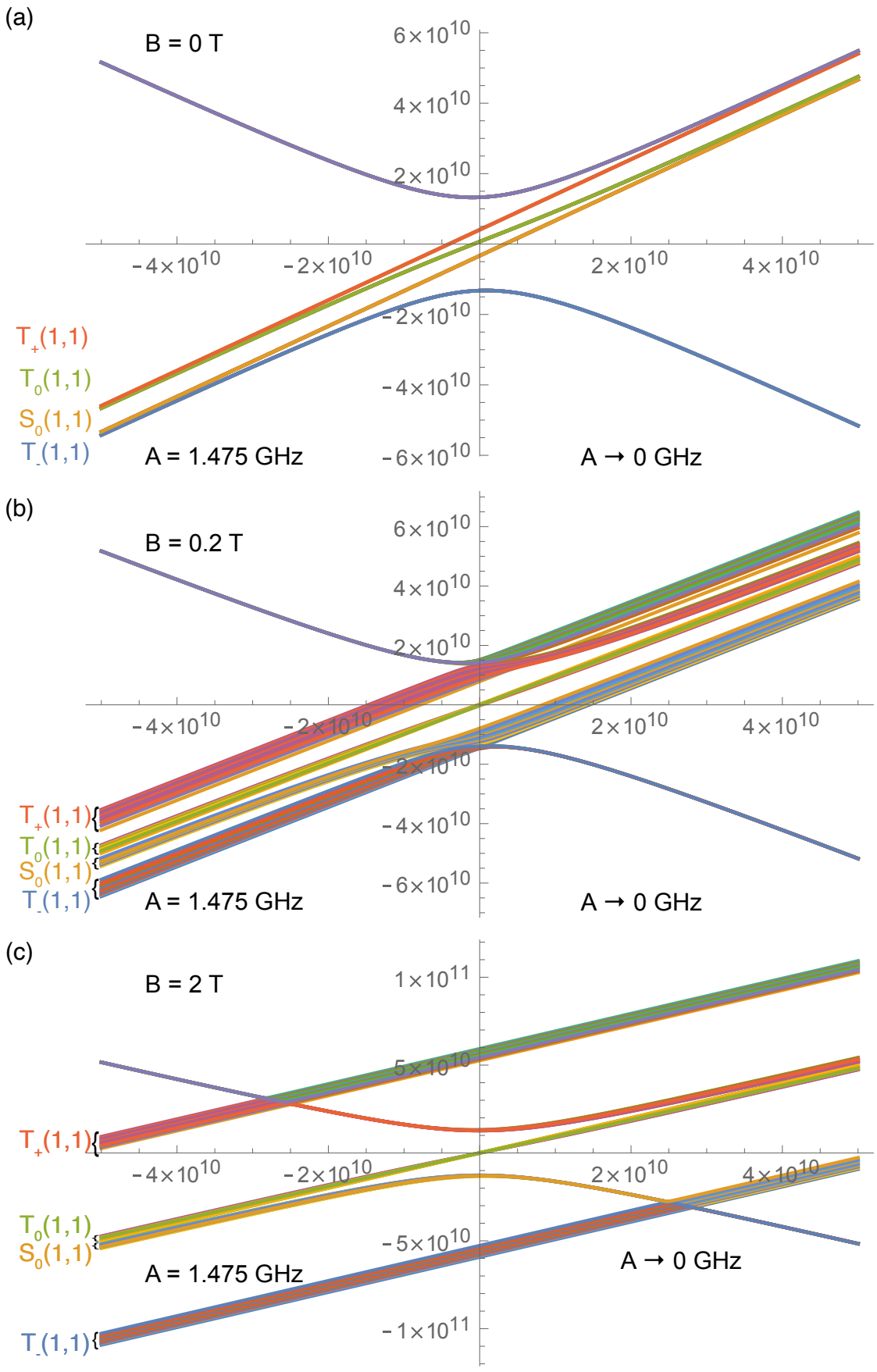


Figure B.2 Eigenenergies (Hz) of the 50 eigenstates plotted as a function of the energy detuning (Hz) at (a) B = 0 T, (b) B = 0.2 T and (c) B = 2 T.

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