

Diamond Nanowire Transistor with High Current Capability

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Carrier confinement in nanowire (NW) structures can offer a host of new material properties compared to bulk electronic devices. Diamond can be considered an ultimate semiconductor given its superlative electronic, physical, and optical properties. However, the development of diamond device technology has been hindered by doping problems in conventional device structures. Here, heavily doped diamond NWS, some 15 nm wide and only 1–2 nm deep overcome these issues and offer a significant advance in NW technology; transistor action can be induced with remote side gates alone, without the need for semiconductor junctions. Quasi-ballistic transport is most-likely responsible for extraordinary current handling capability of the NW transistors fabricated here at some 20 MA cm^{-2} , being around $0.04 G_0$. This unipolar technology opens up a new paradigm in diamond nanoelectronic device technology.

1. Introduction

Diamond's exceptional electronic properties have been exploited to create a nanowire (NW)-based device displaying extraordinary current handling capabilities. These devices offer a new paradigm in diamond electronic device technology, overcoming issues normally associated with the lack of an

effective shallow dopant in diamond. Extreme nm-material confinement can result in novel electronic, photonic, thermal, electrochemical, mechanical, and biological properties as compared to bulk materials.^[1] Semiconductor (Si, GaAs, etc.) NWs, that is 1D like structures with one or more dimensions measured in nanometers and arbitrary lengths, often extending to microns or even millimeters, have received extensive attention. This is because they offer the potential to exploit novel electronic, photonic, thermal, electrochemical, mechanical, and biological properties^[1] due to their dimensionality. This leads to many potential applications such as in nanoelectronics,^[2,3] nanophotonics,^[4,5] bio- and

chemical-sensing,^[6,7] and optoelectronics.^[8] Semiconductor NWs are also being considered as potential building blocks of post-CMOS devices to sustain the downward scaling required in next-generation integrated circuits.^[9]


NW devices formed from carbon nanotubes (CNTs) have also aroused considerable interest since they can support ballistic transport, i.e., conduction with negligible electrical resistivity caused by scattering, and can display quantum effects;^[10] quasi-ballistic carbon nanotube devices have been reported with current densities exceeding Si and GaAs devices.^[11] However, the fabrication of integrated CNT devices can be problematic due to the need to place and contact individual CNTs into circuit patterns. In contrast, semiconductor NWs can be rationally and predictably synthesized in single crystal forms with all key parameters controlled, including chemical composition, diameter, length, doping, and electronic properties.

Diamond can be considered to be a wide bandgap (5.5 eV) semiconductor with extreme electronic properties in terms of carrier mobilities, electric field breakdown strength and thermal conductivity.^[12] Diamond has extreme optical properties, immense chemical and chemical robustness, and resilience to high temperature and high radiation environment. Thus, there is enormous potential for diamond devices to be both extreme in electronic properties and capable of being deployed in extreme environmental conditions. Diamond is readily doped to become p-type in character by the addition of boron, although in modest doping concentrations the boron forms an acceptor state at 0.37 eV from the valence band meaning little boron is active at room temperature. In contrast, at high concentrations, such as 10^{20} cm^{-3} , the emergence of an impurity band diminishes

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the activation energy and the diamond ultimately displays quasi-metallic conduction at room temperature.^[13] However, in this condition, hopping conduction dominates and low carrier mobility results. This, combined with the lack of an effective shallow n-type dopant have hindered the development of diamond devices using conventional transistor structures.

A particularly novel NW transistor has recently been reported by Colinge et al.^[14] which operates without the need for the traditional p–n junction structures associated with conventional transistor technology, greatly simplifying fabrication processes. This device was based upon p⁺ or n⁺ ($\approx 5 \times 10^{19} \text{ cm}^{-3}$) silicon NWs ($\approx 10 \text{ nm}$ deep and a few 10s' of nms wide) with an underlying SiO₂ layer. These NW “fins” were then surrounded by localized gate structures which were used to modulate current through the silicon NW structures; the polysilicon conductive gate contacts were isolated from the NWs themselves with a gate oxide. As opposed to modulating the channel current by affecting a depletion layer in a p–n structure, the device more simply depleted the whole conductive structure with the field applied by the gate overlying the NW. This was possible given the small dimension of the NW meaning that modest applied voltages led to high applied field strengths. Given that diamond can be readily doped p-type, such a unipolar device is of great interest within the scope of diamond technology; it is this form of novel NW device that is explored here. Diamond NWs are fabricated and the current flowing through modulated by side “gates” which apply an electric field in an analogous way to the Si device reported in the paper by Colinge and co-workers.^[14] In the case here, the side gates themselves were diamond NWs (with metallic ohmic contacts) separated from the current carrying NW by an air-gap.

Existing examples of diamond NWs are vertical rather than lateral, i.e., diamond tips which are unsuited to electronic applications, since device integration and contact technology are difficult.^[15] Here, a completely new type of diamond NW is shown; ultrathin (nm) heavily boron-doped layers grown epitaxially on single crystal diamond substrates are used to fabricate lateral diamond NWs. While the NWs are nominally resistive, when side gate structures are electrically biased, the resistance diminishes dramatically resulting in extraordinary levels of currents through the NWs. The magnitude of the currents is most reasonably explained by the emergence of ballistic carrier transport; an explanation for this is given. These new structures open up the possibility of a whole new paradigm in diamond electronic device physics and technology.

2. Experimental Section

Ultrathin heavily boron-doped layers were used, grown on high-quality synthetic single crystal diamond substrates, using a plasma method as described previously.^[16] It is important to prepare the substrate carefully, and introduce a buffer layer before depositing the doped-layer; such methods have been previously described.^[17] Thus, carefully prepared (100) orientated-type Ib HPHT single crystal diamond substrates were used for the growth of ultrathin doped layers (Element Six/DMD Ltd). The layers were grown using microwave plasma CVD with H₂, CH₄, and B₂H₆ feed gases. Details of the CVD synthesis of delta-doped layers have been reported previously.^[18] The

epilayers used here were grown to be 1–2 nm in thickness and were judged to have $[B] \approx 10^{20} \text{ cm}^{-3}$ as discussed below.

Critical to the development of laterally defined NWs was the use of e-beam lithography with suitable resist technology. An acid cleaning step was first applied which is known to leave the surface oxygen terminated and free from so-called surface conductivity that is associated with hydrogen-terminated surfaces.^[19] Next an e-beam resist (4% hydrogen silsesquioxane, HSQ) was spun onto the doped epilayer covered substrates in clean room conditions. The substrate and resist were then selectively exposed to 30 kV electrons (Raith 150-two e-beam lithography machine). HSQ shows good selectivity as a mask when exposed to an oxygen reactive ion-etching (RIE) plasma. This enabled a mesa etch process to leave isolated ultra-thin boron layers supported upon insulating diamond regions protruding from the insulating diamond substrate. The mesa etch depth was $\approx 100 \text{ nm}$. The resultant NW had a line width of $\approx 15 \text{ nm}$, yielding a cross-sectional area of $\approx 15 \text{ nm}^2$, fanning out to $>100 \text{ nm}$ to enable contacting. The mesa etch process also produced four side gates, two each side of the NW such that a field could be applied across the NW; to ensure isolation a gap of $\approx 50 \text{ nm}$ was left between the side-gate boron-doped structures. The side gate structures were also produced with fan-out regions for contacting. Twin side gates physically isolated from the diamond NW itself, were chosen to enable a relatively linear field to be applied over an extended region of the length of the NW. The separation prevented a leakage current between the gates and the NW, provided the field strength was maintained at less than the breakdown strength of air. Finally, Ti/Pt/Au ohmic contacts (subsequently annealed at 500 °C to ensure ohmic character) were deposited on the fan out contact regions of the NW and the side gate regions. **Figure 1** shows a process flow schematic for the fabrication of the NW devices; 1) shows the diamond substrate with the ultrathin heavily doped epitaxial layer grown on top, 2) mesa-isolation of heavily boron-doped NW and side gate regions from the underlying insulating diamond substrate, and 3) ohmic contacts on each of the mesa-etched regions for the purposes of contacting. All *I*–*V* measurements were taken using probes within a vacuum system attached to a Keithley 4200 semiconductor analyzer.

3. Results and Discussion

Considerable international effort has gone into the development of ultrathin heavily doped diamond layers, often “capped” with an undoped diamond layer, in pursuit of the potential device performance advantages offered by so-called “delta-doping”; the diamond layers used here were grown during a collaboration between the authors and others in this context.^[16] In the current case uncapped delta-like—ultrathin—heavily boron-doped ($>10^{20} \text{ cm}^{-3}$) layers were used. Data for the boron doping profile, measured by elastic recoil detection analysis (ERDA), for this material is shown in **Figure 2**; the surface of the sample is nominally taken to be at the position labeled as 0 nm, indicating a doped layer of $\approx 1 \text{ nm}$, with a peak boron doping concentration of $\approx 8 \times 10^{20} \text{ cm}^{-3}$. Note, no “capping layer” is present on these samples – the ultrathin doped layer forms the outer surface region. It has been shown previously^[13] that boron

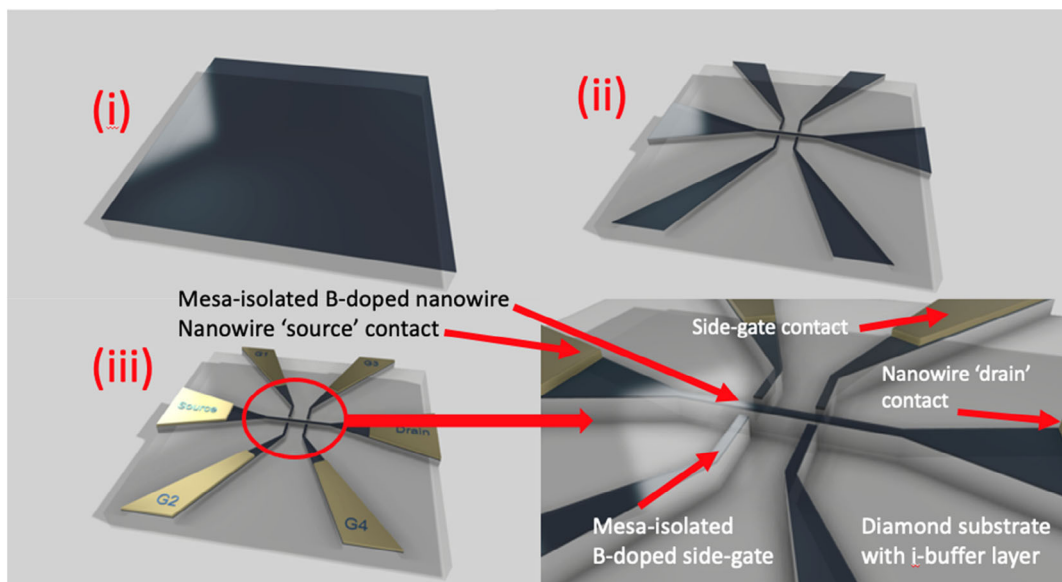


Figure 1. Schematic of process flow showing i) diamond substrate with CVD-grown buffer layer (≈ 100 nm) onto which the ultrathin (≈ 1 nm) heavily boron-doped ($\approx 10^{20}$ cm $^{-3}$) epitaxial layer was grown ii) etching for mesa-isolation of heavily boron doped layer supported on insulating diamond to form both the NW and side gate regions from the underlying insulating diamond substrate-buffer (gap between the side gate structures ≈ 50 nm) and iii) ohmic contacts (Ti-Pt-Au) formation on the fan-out regions of the mesa-etched NW and side gates regions for the purposes of contacting. For the purposes of clarity, the contacts each side of the NW are labeled as “source” and “drain” indicating the current flow within the NW.

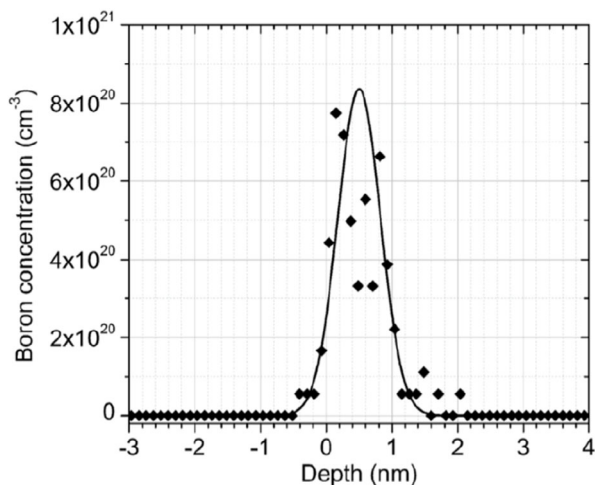


Figure 2. A plot of the boron profile of a typical delta layer used here, measured by ERDA showing a full width at half maximum of ≈ 1 nm. Solid line represents a Gaussian fit to the measured data.

concentrations of this order result in quasimetallic conductivity with meV activation energies (and low carrier mobility) in diamond.^[13,16] Following the mesa isolation steps (discussed above), but prior to the metallization step, the device structure with the NW and fan-out regions (for ohmic contact formation) and the four side-gates are clearly visible, and labeled, in **Figure 3**.

Without an electrical bias being applied to the side gates, current flowing from the through the NW (each end termed the source to drain regions) was ohmic in nature as expected,

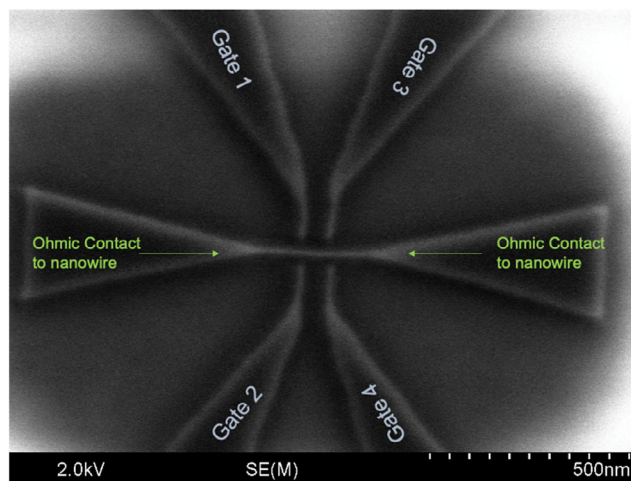


Figure 3. SEM image of the heavily boron-doped mesa-isolated NW and fan-out regions (for ohmic contact formation) and the associated four side gates, also with fan-out structures for the purpose of contacting. The gap between the side gates on each side of the NW is ≈ 50 nm; each pair of gates, 1 and 3 as well as 2 and 4, are electrically connected to—this allows near uniform field to be applied across the NW.

although only measurable in the $< nA$ region. This suggests a resistance for the NW and contacts system of around a $> G\Omega$. The ohmic character of the contact is to be expected for the high boron doping level of the samples here, and the choice of Ti-Au-Pt as the contact metallization. The calculated resistance, $\approx 10 G\Omega$, is high as expected given that the diamond NW has a cross-sectional area of only ≈ 15 nm 2 .

The conductivity changed dramatically upon the application of a bias voltage to the side gates. **Figure 4** shows the measured current density flowing through the NW (left axis) plotted against the voltage applied to (all four) gate structures. Here, a voltage is being applied from one end of the NW to the other (analogous to source-to-drain in a transistor, labelled as V_{DS}) of 3.25 V with an applied side-gate voltage up to 200 V. Side-gating of NWs to produce transistor like action has been demonstrated before silicon technology, obviating the need for p–n junctions, as discussed above.^[14] In this case, the region separating the gate from NW (which here is analogous to the channel of a transistor) is a physical gap, as opposed to SiO_2 . With application of a 200 V side-gate bias, it can be seen that the NW resistance drops to around 100 k Ω , giving a current density through the NW of $20 \times 10^6 \text{ A cm}^{-2}$. To ensure that potential gate leakage currents are not interfering with these measurements, **Figure 5** shows the gate-to-NW current (labeled as gate-to-drain, I_{GD}) plotted as function of the gate voltage, again up to 200 V. It is clear that the gate leakage current remains remarkably low, $\approx 0.1 \text{ nA}$, some seven orders of magnitude lower than the measured I_{DS} current; this is the case for variation of V_{DS} in the explored range of 1–10 V. Indeed, as opposed to that seen with conventional FET designs, the large value of I_{DS} seen at high values of I_{GS} shows little sensitivity to the value of V_{DS} in the range of 1–10 V explored here. Likewise, the “on” current through the NW also showed little sensitivity to the value of V_{DS} in the range measured. The observations within Figure 4 show that the NW device is behaving as a controllable resistor; the NW current being controlled by the gate voltage—a transistor.

The measured NW current at $20 \times 10^6 \text{ A cm}^{-2}$, is higher than achieved for conduction in metals and comparable to the best CNTs (30 MA cm^{-2});^[20] the level in CNTs can only be explained on the basis of ballistic transport, that is conduction with little carrier scattering within the NW. The extraordinary magnitude of the current observed here for the diamond NW suggests that conduction is occurring with little carrier scattering within the

NW in a comparable manner to CNTs where quasi-ballistic transport has been reported.^[11] As noted above a similar design that used here has been reported before using silicon technology; however, such a device did not display quasi-ballistic transport.^[14] In the current case the current density, at $\approx 20 \text{ MA cm}^{-2}$, is such that it can be asserted that the side-gating effect must be constraining the conducting channel through the diamond NW away from the sides of the channel. This effective loss of the “skin-effect” which otherwise leads to strong carrier scattering, results in carrier flow with sufficiently low scattering that it is best described as a form of quasi-ballistic conduction. That the level of I_{DS} is relatively insensitive to the value of I_{DS} when in this condition is also suggestive that conduction is not “ohmic” as would be expected for a channel region in a conventional FET. At a side gate voltage of 200 V, and a V_{DS} (NW voltage) value of 3.25 V a conductance value can be calculated as $0.04 G_0$, a value never reported for diamond conductivity at room temperature previously. As indicated earlier, the lateral diamond NW technology developed here is fully compatible with rational device design with arrays of NWs fabricated with conventional semiconductor processing technology (Figure 1).

Constraints imposed by the need for CNT sorting, processing, alignment, and contacts methodology give rise to nonidealities when CNTs are implemented in densely packed parallel arrays such as those needed for useful technology, resulting in the conductance in individual CNTs departing from ideal ballistic conditions. The “champion” devices with $0.46 G_0$ conductance per tube approached the room temperature fundamental quantum conduction limit $2G_0 = 4e^2 h^{-1} = 155 \mu\text{S}$, i.e., when the elastic mean free path of the carrier is larger than the length of the wire. As noted above, a similar design to that used here, where side gates control the conductivity through the wire, has been proposed previously in silicon technology.^[14] In the current case, when the current capability of this transistor is allied with the advantages of diamond as an electronic material (such as electric

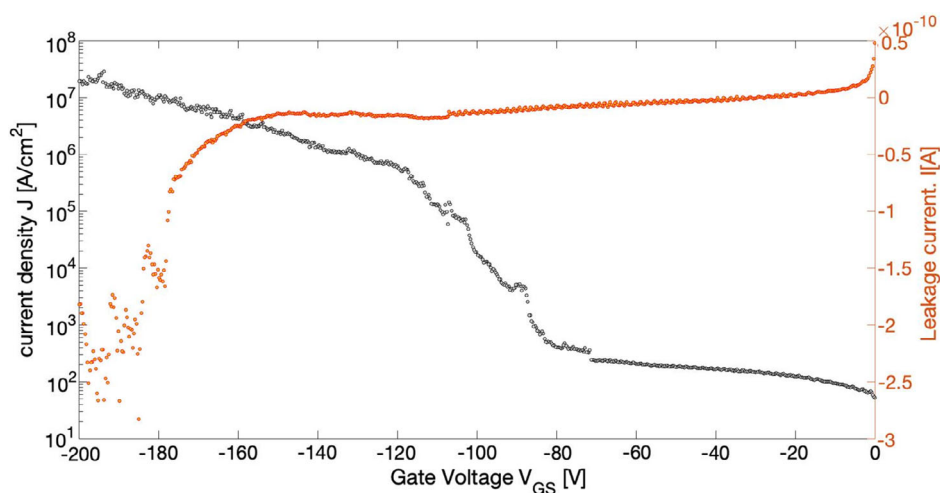


Figure 4. Left, axis, a voltage across the NW (similar to a source-drain voltage [V_{DS}]) of 3.25 V is being applied with an increasing side-gate voltage up to 200 V. A dramatic increase in the current through the NW is apparent reaching a value of $\approx 20 \text{ MA cm}^{-2}$. Also plotted (right axis) is the gate voltage, V_{GS} , plotted as a function of gate current, I_{GD} , for a range of V_{DS} . Very low gate leakage currents are apparent at $\approx 0.1 \text{ nA}$, seven orders of magnitude lower than the on-current, I_{DS} .

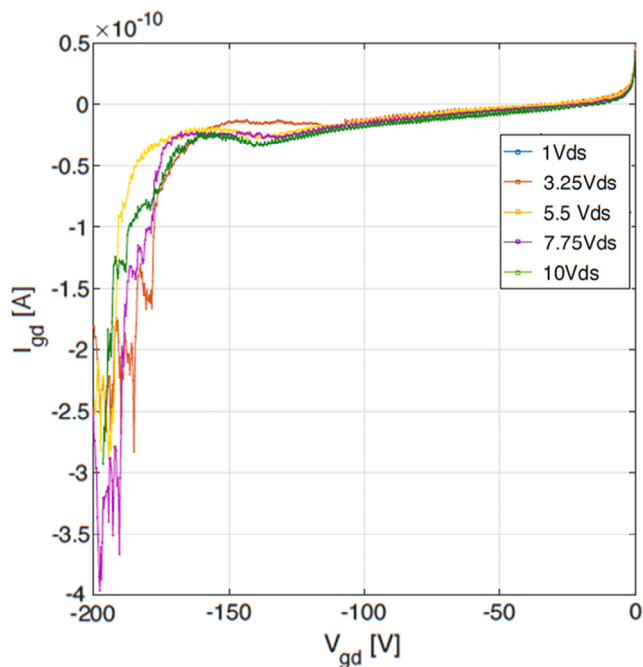


Figure 5. Plot of $V_{G D/S}$ against $I_{G D/S}$ as a function of $V_{D/S}$. It can be clearly seen that although a form of soft breakdown emerges at the highest gate voltages applied the increase is very small, the values remaining in the nA range, and are similar for all $V_{D/S}$ values.

breakdown field strength, thermal conductivity and extreme chemical/physical/radiation resilience) real promise for a new generation of devices for use in extreme environments can be identified.

4. Conclusion

While unipolar semiconducting (Si) NWs have been used to produce transistor-like characteristics using side gating across the NW, such structures do not show ballistic carrier transport at room temperature. In terms of CNT technology, constraints imposed by the need for CNT sorting, processing, alignment, and contact methodology give rise to nonidealities when CNTs are implemented in densely packed parallel arrays such as those needed for useful technology. This results in the conductance in individual CNTs departing from ideal ballistic conditions, in addition to the significant limitations this imposes on the technology of device fabrication. In contrast, here lateral p-type diamond NWs have been realized that display extraordinary levels of electrical conduction at room temperature. This is most likely attributable to a form of field-induced quasi-ballistic carrier transport within the NW induced by the field applied via the side gates. The emergence of these current levels most likely arises from this field constricting carriers within the NW to reduce the otherwise evident scattering from the walls of the NW, thus creating a controllable NW resistor, more commonly known as a transistor. This offers a new paradigm of diamond electronic device technology, overcoming issues normally associated with the lack of an effective n-type dopant and the need to operate unipolar

p-type devices at elevated temperature to activate the boron dopant. Combined with other advantages of diamond as an electronic material, such as electric breakdown field strength, thermal conductivity and extreme chemical and physical resilience, this breakthrough may significantly enhance the emergence of high-performance diamond nanoelectronic devices.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

The work was conceived by A.C.P.T. and developed by A.C.P.T., M.A.R. and R.B.J., being planned in detail by A.C.P.T. Experiments and fabrication were performed by A.C.P.T., S.Y., Z.A.K. and S.D.S. The work was supervised by R.B.J. and M.A.R. Results were analysed by all authors, including R.J.M. All authors contributed to the preparation of the manuscript, including M.A.R. before his untimely death.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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