A DC Model for Organic Electrochemical Transistors and Analysis of Their Performance as Voltage Amplifiers

Farnaz Fahimi Hanzaei  
Electronic and Electrical Engineering  
University College London, U.K.  
farnaz.fahimi.19@ucl.ac.uk

Peter J. Langlois  
Electronic and Electrical Engineering  
University College London, U.K.  
p.langlois@ucl.ac.uk

Anastasios Polyravas  
Electronic Engineering  
University of Cambridge, U.K.  
ap2053@cam.ac.uk

Ivan B. Dimov  
Electrical Engineering  
University of Cambridge, U.K.  
ib20@cam.ac.uk

Richard H. Bayford  
Natural Sciences  
Middlesex University, U.K.  
r.bayford@mdx.ac.uk

George G. Malliaras  
Electrical Engineering University of  
Cambridge, U.K.  
gm603@cam.ac.uk

Andreas Demosthenous  
Electrical and Engineering  
University College London, U.K.  
a.demosthenous@ucl.ac.uk

Abstract—Organic electrochemical transistors (OECTs) have received a great deal of attention, especially in biomedical applications, since their emergence in the mid-1980s. Despite many efforts on modeling these transistors, simulating OECT-based circuits is still a challenge due to a lack of precise mathematical models. In this paper, some of the main features of OECTs are analyzed and a DC model is proposed that closely mimics the transistors’ characteristics compared to the well-accepted Bernards–Malliaras (B–M) model. While OECTs are mostly considered as transconductance amplifiers, the potential of using these transistors as voltage amplifiers is investigated here with measurements at various drain-source voltages. Compared to the B–M model, the proposed model has improved matching up to 3.6% between simulations and measurements of the analyzed transistors.

Keywords—organic electrochemical transistor, SPICE model, transconductance, Verilog-A, voltage gain, volumetric capacitance

I. INTRODUCTION

Organic electrochemical transistors (OECTs) are three-terminal devices (gate, drain and source) that usually operate in the depletion region, where their p-type variation is most-commonly used due to its material stability at room temperature [1]. Employing an aqueous electrolyte with ion carriers for the gate-channel insulator, as opposed to the gate-oxide used in MOS transistors, is a significant feature of these types of transistors [2]. In the absence of any gate voltage, the number of hole carriers in the p-type polymer semiconductor channel is at a maximum level. Applying a positive voltage to the gate electrode repels cations in the electrolyte, which then travel toward the channel and compensate for the holes available in the channel (in a sense, de-dope the semiconductor) [2, 3]. As a result, both the ionic (mobility in the range of $10^{-4}$ to $10^{-2}$ cm$^2$V$^{-1}$s$^{-1}$) and electronic (mobility in the range of 0.1 to 10 cm$^2$V$^{-1}$s$^{-1}$) charge carriers interactively play a role in the drain current modulation process, which leads to the relatively low bandwidth of OECTs (in the range of a few kHz) [4]. In addition, the large volumetric gate-channel capacitance ($\sim$ mFcm$^{-3}$) due to the usage of an electrolyte insulator raises the OECT’s transconductance ($g_m$ in the range of mS) and allows for a low operating voltage [2]. The facts that OECTs have a low fabrication cost, are flexible and biocompatible, while at the same time benefit from a high gain and low operating voltage, make them an attractive option particularly for biomedical applications [2, 5-7].

In order to simulate organic transistor-based circuits, a model that can closely represent the characteristics of these transistors is required. Several models have been reported for OECTs based on both analytic and numerical approaches [8-10]. While the available analytic models are useful for assessing the performance of OECTs, they lack sufficient accuracy due to the currently limited understanding of the physics of these devices [9]. The available numerical models, on the other hand, might have high complexity [11] or precision issues [12].

In this paper, a simple and accurate DC model for p-type depletion-mode OECTs is proposed with improved performance compared to the existing Bernards–Malliaras (B–M) model for organic transistors [8]. Additionally, the challenges in using OECTs as voltage amplifiers are investigated by operating the transistors at different drain-source voltages. In Section II, a background on the B–M model is reviewed and parameters that are effective in an OECT’s behavior are detailed. In Section III, the proposed model is discussed and the measured I-V characteristics obtained from sample OECTs are compared with the models. An analysis of the voltage gain of OECTs is also presented in this section. In Section IV, the simulated and measured performances of an OECT-based common-source amplifier are compared showing the good accuracy of the proposed model. Concluding remarks and future directions are drawn in Section V.

II. OECT BEHAVIOR

A. B–M Model

In 2007, Bernards and Malliaras proposed a physical model (Equation (1)) that mimics MOS transistors’ behavior with the plate capacitance being replaced by the volumetric equivalent in OECTs [3, 8]. In the model the drain current is calculated by dividing OECTs into (i) an electronic subcircuit (based on Ohm’s law) and (ii) an ionic subcircuit (based on the linear RC equivalent of an electrolyte interface).

$$I_{CH} = \begin{cases} G \left[ 1 - \frac{V_{GS}}{2V_T} \right] V_{DS} & \text{for } V_{DS} > V_{GS} - V_T \\ -G \left[ \frac{V_{GS}-V_T}{2V_T} \right]^2 & \text{for } V_{DS} < V_{GS} - V_T \end{cases}$$
where $W$, $d$ and $L$ are the width, thickness and length of the semiconductor channel, respectively, and $V_{GS}$, $V_{DS}$ and $V_T$ refer to the gate-source, drain-source and threshold voltages. The $\mu$ and $C^*$ parameters represent the hole mobility and volumetric capacitance, indicating the effect of electronic and ionic properties on the drain current of the transistor [3, 8]. The following subsection summarizes some of the OECT-specific behaviors and their dependence on the parameter variations according to the B–M model and some empirical investigations.

B. OECT Dependence on Parameter Variation

The large volumetric capacitance in OECTs plays a deterministic role in their performance [13]. A gate-channel capacitance more than seven orders of magnitude larger than MOS transistors enables OECTs to operate at a relatively low voltage (less than 2 V) [14]. Furthermore, the dependence of the transconductance of OECTs ($g_m$) on the $C^*$ element makes it three orders of magnitude larger than the $g_{m}$ of MOSFETs, a property that allows for OECTs to be a suitable choice as transconductance amplifiers [2]. Also, the $g_{m}$, its maximum value $g_{m}^{\text{max}}$ and the gate-source voltage at which $g_{m}^{\text{max}}$ occurs, $V_G(g_{m}^{\text{max}})$, can be tuned by the factor $Wd/L$ [3, 5]. Higher $W/L$ and larger thickness result in a more positive $V_G(g_{m}^{\text{max}})$ and a greater $g_{m}^{\text{max}}$ value. Additionally, the drain-source voltage and gate-electrode material are parameters that can affect $g_{m}^{\text{max}}$ and $V_G(g_{m}^{\text{max}})$. A $V_{DS}$ with an absolute value smaller than 0.6 V slightly shifts the $V_G(g_{m}^{\text{max}})$ toward more positive values and significantly reduces $g_{m}^{\text{max}}$ [15].

Based on the above, $g_{m}^{\text{max}}$ can be ‘engineered’ to take place at zero gate-voltage by manipulating $W$, $d$ and $L$ to avoid utilizing two supply voltages, one for the drain-source and the other for the gate-source. In biomedical applications, this can prevent damaging biological tissue by applying a DC bias for a long period [15]. The temporal response of the transistor to a pulse applied to the gate depends on the $RC$ time constant of the electrolyte-channel equivalent circuit [8, 10], where the $RC$ is proportional to $d/\sqrt{WL}$. Therefore, there is a design trade-off between $g_{m}$ and the maximum speed of the transistors when changing the channel thickness [3, 16]. Moreover, as the thickness increases, the threshold voltage moves toward more negative values and the saturation region in the $I_D - V_{DS}$ plot fades away [11].

III. OECT MODELING AND VOLTAGE GAIN ANALYSIS

The DC model presented in this paper is developed based on I-V measurements from 40 OECTs with a nominal $W \times L = 50 \mu m \times 50 \mu m$, a thickness varying from 80 nm to 450 nm, and overlaps (between the channel and the contacts) in the range of 5 $\mu m$ to 30 $\mu m$. Non-polarizable Ag/AgCl electrodes are used for the gate electrode [17]. The overlap affects the frequency response (not considered here), and the thickness is a deterministic factor in the steady-state transconductance ($g_m$) [18]. The ionic current that flows from the gate to the channel is purely capacitive and at DC is near zero (in practice, the gate-source leakage current is in the nA range) [3].

A. Proposed DC Model

Comparing the OECT measurements with the B–M model reveals that despite being an adequate representative of the transistors, the model’s accuracy should be improved. In particular, examining the $I_D - V_{DS}$ characteristics of the transistors before reaching saturation, in most cases the B–M results descend toward the more negative values of the currents faster than the actual data. The error becomes more pronounced in larger thicknesses where the effect of saturation is weaker. This error may be compensated to a certain extent by controlling the slope in the B–M equation through the $V_{GS}$ coefficient. Based on empirical observations, the coefficient is chosen as a function of $V_{GS} (A$ in Equation (2)) so that it is larger when the $V_{GS}$ is closer to zero and becomes smaller as $V_{GS}$ increases. Note that $A = 1/V_T^2$ returns the same B–M equation. Moreover, the slope might need a slight adjustment through the parameter $N (0 < N < 1)$ in the equation, to account for any changes due to different thicknesses and also subtle transistor-to-transistor variations.

$$I_{CH} =$$

$$\begin{cases} 
\frac{GV_T}{2} ((A + \frac{1}{V_T^2})V_{GS} - V_T) V_{DS} - AV_{DS}^2 & \text{for } V_{DS} > V_{GS} - V_T \\
-G \frac{(V_{GS} - V_T)^2}{2V_T} & \text{for } V_{DS} < V_{GS} - V_T
\end{cases}$$

$$A \approx \left(1 - \frac{V_{GS}}{3V_T}\left(\frac{N}{V_T^2}\right)\right)$$

**Fig 1.** Comparison of $I_D$ vs. $V_{DS}$ characteristic plots for measurements (black lines), Equation (1) (red lines) and Equation (2) (blue lines). Parameters $d = 100 \text{ nm}$, $V_T = 0.55 \text{ V}$ and $N = 0.95$ (left panel), and $d = 200 \text{ nm}$, $V_T = 0.65 \text{ V}$ and $N = 0.85$ (right panel).
where $V_T$ is the threshold voltage and $G$ is as in (1), which can be inferred from the minimum current at zero $V_{GS}$. The $I_D - V_{DS}$ characteristics for two sample OECTs with thicknesses of 100 nm and 200 nm are plotted in Fig 1 using the measurements as well as B–M and the proposed model (in all cases the source voltage is grounded). Calculating the relative difference of the measurements from both the B–M model and the proposed model shows that the new model of (2) improves over B–M by more than 1% in the case of the transistor with 100 nm thickness and 3.6% for the 200 nm transistor (similar results were obtained when testing four separately fabricated transistors with corresponding thicknesses). Also, it is worth noting that the curves merge when approaching higher $V_{GS}$ values, stemming from the fact that the proposed model retains B–M’s equation for the saturation region.

Both (1) and (2) provide a relatively straightforward representation of the OECT performance and assume a notable saturation region similar to that in MOS transistors. However, in most cases, this assumption does not appear to be realistic in practice. Particularly, for thicknesses >100 nm, no significant saturation in OECTs is observed except perhaps for very small current values. This leads to a very low output resistances of the transistors which hinders their performance as voltage amplifiers. Using lower thicknesses, on the other hand, limits the transistor gain. To further investigate this issue, the next subsection provides an analysis of the voltage gain of OECTs.

### B. Voltage Gain of OECTs

The low output resistance at the drain-source of OECTs originates from the fact that in these transistors the voltage should normally be limited within the potential window. This is to avoid the electrochemical instability due to electrolysis of the electrolyte and also to keep power consumption at a low level [19-21]. To comply with this limit, the DC voltage-drop across each pair of contacts should not exceed 1.23 V [19]. Therefore, a maximum of $-0.6$ V drain-source voltage is commonly used so that the gate-source voltage can also be varied from 0 to 0.6 V. As a result, the current would not reach saturation in this voltage range, and therefore, OECTs are mostly known as transconductance amplifiers with a high $g_m$ rather than voltage amplifiers.

To investigate the potential of OECTs for voltage amplifiers, the performance of transistors has been examined here, under different drain-source voltages and within a range where electrochemical stability still holds (up to $-0.8$ V). As shown in Fig 2, the effect of saturation is more pronounced when $V_{DS}$ goes beyond $-0.6$ V. Also, Fig 3 demonstrates the output conductance ($g_{ds} = \partial I_D / \partial V_{DS}$) of two transistors for $V_{DS}$ varying from zero to $-0.6$ V and $-0.8$ V. As expected, the $g_{ds}$ approaches zero when the maximum $|V_{PS}|$ is increased, and therefore, the intrinsic voltage gain $g_m / g_{ds}$ increases (intrinsic voltage gain = 14 and 60 (V/V) at $V_{GS} = 0$ for $V_{DS} = -0.6$ and $-0.8$ V, respectively).
These observations illustrate that, although the power consumption is slightly increased, a four-fold larger gain can be obtained by biasing the circuit such that the $V_{DS}$ of the transistor is more negative than $-0.6$ V. Moreover, in that case, (1) and (2) could provide a more realistic representation of the transistor performance in the saturation region. In other words, considering a saturation region with an infinite output resistance would be a more acceptable estimation where, similar to MOS transistors, the voltage gain would mainly depend on the load resistance of the amplifier (e.g., in a common-source configuration).

![Fig 5. OECT-based inverter simulated in Cadence. $V_{ss} = -0.8$ V and $V_{GSS} = 0.3$ V.](image)

**IV. Simulations**

In order to validate the proposed DC model in (2), the model was transferred into Cadence Virtuoso using Verilog-A language. Simulating an inverter of the type shown in Fig 5, based on the transistor of Fig 2 (with a load resistance of $1\, k\Omega$, $V_{GS} = 0.3$ V and $V_{S} = -0.8$ V) resulted in a voltage gain of 2.559 V/V. Based on the measurements in Fig 4 (the left panel), the $g_{m\text{max}}$ for $V_{GSS} = 0.3$ V is 2.479 mS, which closely matches the simulated value of the gain ($A = g_{m\text{max}}R_{\text{load}}$). The large signal drain voltage in response to a 100-mV AC signal is also visualized in Fig 4 (the right panel) from both the measurements and simulations. As shown in the figure, the AC output voltage from the simulation also very closely follows the measured result, illustrating the accuracy of the developed model in describing OECTs for SPICE simulations.

**V. Conclusion**

This paper has provided a brief summary of the various parameters that affect the performance of OECTs and some of the key available trade-offs. Using features of the B–M model, a new enhanced DC model for OECTs has been proposed based on multiple measurements collected from the transistors. The additional parameters in the proposed model provide an improved performance compared to the B–M model in all cases analyzed. Given the importance of voltage-gain in circuit design, the potential of OECTs as voltage amplifiers has been investigated and a number of possible challenges have been discussed. The proposed DC model has been implemented in Verilog-A Cadence environment. The simulated and measured results show the high accuracy of the model in representing OECT-based circuits. The model may be further improved by considering the actual output resistance of the transistors instead of an ideal infinite resistance. Future work will consider the AC behavior of the transistors to create a comprehensive model for OECTs.

**REFERENCES**


