THE DESIGN OF HIGH FREQUENCY
AND
ULTRA-NARROW-BAND SWITCHED-CAPACITOR FILTERS

by

Andrew Keith Betts

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(University of London)
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ABSTRACT

This thesis is concerned with the design of Switched-Capacitor (SC) circuits for applications in the MHz range, and for applications requiring bandpass filters with relative bandwidths of much less than 1% (i.e. $Q >> 100$). Both of these design goals are presently beyond the capability of standard, commercial SC circuits, which all use CMOS processes. In the first case, the limitations of the CMOS FET's make it extremely difficult to design circuits with sufficiently small settling times for accurate processing of signals in the MHz range. In the second, large capacitor spreads and high sensitivity to non-ideal circuit phenomena make it impractical to build conventionally designed filters with relative bandwidths less than about 1%.

The high-frequency goal has been approached using GaAs MESFET technology, combined with new circuit design and optimisation techniques. Novel integrator circuits with low sensitivity to amplifier gain and immunity to amplifier input offset are presented (these phenomena are far more significant in GaAs than Si technologies). The circuits are used in the design of a demonstrator GaAs SC filter, which has been carefully optimised using automated symbolic analysis techniques.

In the work on narrow-band filters, the limitations of advanced multi-path SC filter architectures are analysed using Monte-Carlo techniques based on a high-level abstraction of the filter architecture. This analysis highlights the large influence of unwanted 'mirror components' on filter responses, resulting from the mismatch of passband centre frequencies of the individual filters in the multi-path system. To alleviate these problems, a new 'N*M' multi-path architecture is proposed, which uses 'pseudo-N-path' techniques to advantage. Finally, novel pseudo-N-path circuits with very low sensitivity to amplifier gain are presented.
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to Sue, with Love
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1.1 General introduction

This thesis is concerned with the design of Switched-Capacitor (SC) circuits. The SC technique is an efficient method for implementing analogue functions in integrated circuit (IC) form and for applications in the audio frequency range it is used extensively in mixed analogue/digital systems. SC circuits tend to have higher precision than integrated continuous-time circuits, and consume less area and power than comparable digital designs, so together the three techniques allow an optimum balance between system performance, flexibility and cost.

A clear trend in the communications industry is towards broadband systems, as ever higher data rates are required to support planned new services, associated with ISDN and its possible successors [4]. These new systems are heavily based on integrated circuit technology, and there is a continuing drive to integrate as many analogue and digital functions as possible into a single IC [128]. In line with these trends, the object of this work is to extend SC design techniques in two directions. Firstly, to transfer the SC technique, and its benefits, to GaAs technology, where it should allow the design of very high speed SC circuits and their integration with other high-speed, GaAs-based systems. Secondly, to develop new SC architectures to allow filters to be built with much narrower relative-bandwidths than was previously possible using Switched-Capacitor techniques. This will require the development of design techniques to overcome limitations in current narrowband SC filters, and should allow the wider use of integrated analogue filters for narrowband signal processing.

The use of GaAs in commercial applications, where its excellent optical and electronic properties are invaluable at high-frequencies, has recently become far more widespread. Microwave Monolithic Integrated Circuits (MMICs) have recently reached a state of maturity where foundry services are widely available, and this has opened up the possibility of employing GaAs in SC design. However, while optoelectronic and MMIC circuits operate at frequencies in excess of 1GHz, GaAs SC designs aim to process signals in the MHz range. New circuit architectures and design methods will therefore be described that deal with difficulties particular to the use of GaAs at MHz frequencies. These are applied to the design of a demonstrator GaAs SC circuit, fabricated using a commercial D-MESFET process. Extensive simulations of the filter show that it should be capable of operating at significantly higher frequency than previously reported Si or GaAs SC filters.

Work on narrow-band SC circuits has been based on an evaluation of
current techniques for narrow-band SC filtering, taking into account known process tolerances and their effect on filter behaviour. This theoretical investigation has highlighted some important difficulties in currently available structures, and new circuits have been developed to overcome these problems. The new structures combine a variety of multi-rate sampling techniques in a combination particularly suited to the characteristics of SC filters. In particular, the new circuits make maximum use of the available dynamic range of SC circuits, which is frequently the limiting factor in the implementation of narrow-band SC filters.

1.2 Organisation of thesis

This introductory chapter presents background material and reviews past work relevent to this thesis. Chapters 2-4 are concerned with high-speed SC circuits, though many of the ideas presented also apply to SC circuits in general. Chapter 2 gives detailed analyses of existing and novel SC architectures with low sensitivity to amplifier gain, emphasising the importance of building blocks that can be efficiently configured in second- and higher-order filters. Chapter 3 analyses general amplifier-capacitor networks containing one and two amplifiers to determine the time-constants of these systems, showing how the results may be used to predict the settling-properties of complex SC circuits. Chapter 4 then describes a demonstrator GaAs SC filter design, exploiting results from the previous two chapters. Chapters 5 and 6 concern multi-path and multi-rate narrow-band SC filters. The former analyses existing structures for Ultra-Narrow-Band filtering, taking into account technological limitations that affect accuracy. This leads, in chapter 6, to new structures which overcome some of the aforementioned limitations, and also to a new single-path circuit with dramatically reduced sensitivity to amplifier gain. Finally, chapter 7 draws conclusions from the work presented in the thesis, and suggests directions for future work.

1.3 SC circuits: their background

1.3.1 The development of SC circuits

Historically the development of SC circuits was motivated by filter applications [1]. These are still the mainstay of SC technology and, since they have the same basic operating principles as other SC circuits, we will use them as a convenient vehicle for explaining fundamental aspects of SC
circuit design and, in the research work to be described, they are used as a 'testbed' for new circuit techniques.

Fig. 1.1 Bandpass elliptic filter, centre freq. 1kHz, bandwidth 200Hz.

Switched-Capacitor technology is an integrated circuit technology, particularly suited to CMOS processes. Prior to the use of SC circuits a major obstacle to the integration of analogue functions in the frequency range up to 1GHz had been the difficulty in integrating circuits with time-constants of the required electrical size and accuracy. To illustrate this point, fig.1.1 shows a 6th order elliptic bandpass filter, with a centre frequency of 1kHz and a bandwidth of 200Hz (this filter is also used later in this thesis as a source of example data). For the component values shown it can be calculated that to integrate such a filter directly would require a chip whose longitudinal dimensions were of the order of centimetres. Hence, the total area of the chip would be around 6 orders of magnitude larger than is normally considered practical (of course, when the operating frequency is raised by this factor, to approximately 1GHz, passive components may again be realised directly, as they are in MMIC's).

Fig. 1.2 Active continuous time integrator building blocks
(a) RC type (b) MOSFET-C type (c) transconductor-C type

An alternative for audio frequencies is to use the techniques adopted for hybrid filters, where the inter-relationships of the circuit's currents and voltages are simulated using resistors, capacitors and
operational amplifiers [2]. An essential building block in such circuits is the integrator, and an active-RC integrator is shown in fig.2a. The use of such circuits is quite restricted, however, since, using available IC processes, resistor and capacitor values cannot be accurately defined (typical errors for R's and C's are uncorrelated and around +/−10%) and, in addition, the chip area required to realise these values for audio applications is frequently excessive. One approach to these problems is to replace the resistors in these circuits with active elements, biasing them in such a way that they give the desired resistive effect. Two variations of this strategy, again applied to an integrator building block, are shown in figs.1. 2b-c. The first of these is a MOSFET-C circuit, where a MOSFET, biased in its linear region of operation by the control voltage $V_c$, is used in place of the resistor of fig.1.2a. Similarly, in the circuit of fig.1.2c, a transconductance amplifier and a load capacitor form an integrator, and in this case the time constant and linearity of the circuit would be controlled through $g_m$, which could be altered by changing a bias current or voltage within the amplifier. The major disadvantage of circuits based on both of these building blocks is that a large proportion of chip area and design effort must be devoted to the design of subsidiary control circuits to set the main circuit's transfer function, and to reduce the non-linearities in the resistive elements [129].

1.3.2 Basic Principles & Applications of SC circuits

The SC technique overcomes the restrictions on active-RC circuits and their derivatives by using switched-capacitors to obtain a resistive effect. These capacitors are charged and discharged by switching their plates between different nodes in the circuit, thus providing charge flow between nodes that depends on the value of these capacitors and the rate at which they are clocked. The essential characteristics of such a circuit are set by capacitance ratios, and such ratios can be defined with an error as low as 0.1% using capacitor sizes convenient for circuit integration [5,6]. A circuit that realises an integrator using the SC technique is shown in fig.1.3 [3]. Note that an analogue switch may be easily realised in MOS technologies using an FET, as shown, whereas bipolar processes are not used for SC circuits since they lack a device suitable for the switching element.
It should be appreciated that the key to the whole circuit operation is accurate charge transfer between the \( C_1 \) and \( C_2 \) capacitors when the switch at the input to the operational amplifier closes. However, at every node in an integrated circuit there will be parasitic capacitances connected to ground or some other voltage source, and these are frequently significant in size compared to the intentional capacitors. An important property of the particular SC circuit shown is that it is 'parasitic insensitive', so that, for the case of an ideal amplifier, these unwanted capacitors do not affect the circuit transfer function [130].

This integrator building-block is used to realise the 6th order filter
introduced earlier by first identifying certain currents and voltages of the original 'prototype' filter as 'state variables', then drawing their inter­relationship with a signal flow graph (SFG), as shown in fig. 1.4. In this diagram the branch weights are functions of the passive components in the prototype filter. Briefly, the integration operations shown in the SFG (the $1/s$ functions), may then be implemented using the integrator building block just introduced, with switched and unswitched capacitor branches interconnecting these blocks to perform the remainder of the SFG operations. The resulting SC filter, which inherits the good sensitivity properties of the prototype filter, is shown in fig. 1.5.

![SC filter diagram](image)

Fig. 1.5 SC filter corresponding to SFG of fig. 1.4.
The main advantages of SC circuits are small size and high precision compared to other analogue solutions, and potentially very low power consumption [131]. In addition, they have the major benefit of using CMOS processes, which, because of advances in the digital field, are widely available. These factors make SC circuits an economical solution for medium and large scale production, and they have been particularly widely used in telecommunications systems [132-134]. Many standard components, such as A-D and D-A converters, also incorporate SC circuits [137], and stand-alone programmable SC filters are also available [135,136]. The latter circuits exploit the fact that the characteristics of an SC circuit may be easily altered by changing its clock frequency and/or switching certain groups of capacitors into and out of the circuit, giving them limited programmability.

The main competitor to SC circuits is Digital Signal Processing (DSP) technology, well known for its advantages of programmability, lack of parameter drift and the wide range of signal processing functions that it can perform. However, these advantages are achieved at the price of circuit size, complexity and power consumption and, when making general comparisons, it appears that SC technology is positioned somewhere between DSP and active-RC technologies both in terms of cost and functionality [138].

1.3.3 Performance Limits of SC Circuits

There are a number of fundamental factors limiting the performance of SC circuits, all of which have an important impact on the work to be described.

Component Limitations: Capacitors will have a finite Q-factor, since their dielectrics cannot be perfectly insulating, and this limits the achievable Q-factor for any SC filter. In Si technology it is possible to manufacture capacitors with Q's in excess of 10,000 [2], and so this factor does not impose a severe design limitation, but it will be seen later that this may not be the case in other technologies.

The intrinsic gain of a FET ultimately limits amplifier gain, and so it follows that the 'virtual-earth' node of the amplifier in the circuit of fig.1.3 is not exactly at earth potential. It can be shown that this limitation results in gain and phase errors for the integrator [8], although alternative integrator architectures may be used to reduce these effects (see below). Amplifier bandwidth has a similar effect on SC circuit performance since, even if an amplifier did have infinite DC gain, it only has a finite time in which to settle to its final output voltage during a given clock phase. This means that there is some error in the amount of charge transferred onto the integration capacitor, also resulting in gain and phase errors [8].

When used as a switching element the FET on-resistance not only
limits the rate at which charge can pass through the switches, hence limiting maximum circuit speed [2], it is also a source of thermal noise (see below). The finite off-resistance of the switch allows charge leakage from storage capacitors, and, together with FET junction leakage, sets a lower limit on the clock frequency of the circuit. Further difficulties are caused by the transistor's parasitic capacitances, which are non-linear, and allow unwanted signal feedthrough between nodes, causing signal distortion.

**Matching**: Limitations on the accuracy with which capacitors and transistors can be manufactured means that both these components suffer from mismatch problems. Mismatch in capacitors leads directly to errors in the transfer function of circuits, and is a cause of concern in demanding applications. Transistor mismatch becomes problematic in amplifier design, and sets a minimum for the input offset error that can be achieved [7]. The latter is not usually a serious problem, however, since the resulting DC offset at the output of an SC filter can be removed with simple circuit techniques [2].

**Noise**: The transistors contribute several types of noise to the circuit, the most important types being thermal and flicker noise [2,9]. Flicker noise in a FET is dominant at low frequencies, and a 'corner frequency' is defined at which this effectively disappears into the wideband thermal noise. This frequency varies from process to process and from technology to technology; typical values for Si MOSFET and GaAs MESFET processes are 1kHz [2,139] and 10MHz [139] respectively. These intrinsic noise sources are accompanied by clock-feedthrough noise, though the impact of the latter can usually be reduced by lowpass filtering the circuit output signal, since a circuit is normally designed so that clock feedthrough is well separated from the frequencies of interest. However, the clock-feedthrough mechanism also causes signal distortion which can only be alleviated by very careful design [10].

**Sampling**: The fact that the SC technique requires that a signal be sampled imposes a number of constraints on the designer. Firstly, a commonly used design method for filters with order greater than two is to base them on the design of a continuous-time passive prototype filter (as outlined above). However, the design process requires the continuous-time equations describing the passive prototype to be converted into equations for the sampled-data SC filter. The resulting equation in the z domain must be of a form that can be practically implemented using SC techniques, and this restricts us to use of the Bilinear or LDI transforms [2]. Since neither of these transforms perfectly preserves the characteristics of the original equations, the resulting filter transfer function does not exactly match that
of the prototype filter [16]. In addition, the accurate realisation of the resistive terminations of the prototype filter presents some difficulties [16]. These filter synthesis problems can be tackled with a number of techniques [11,12] and, fortunately, recent improvements in computer-based synthesis programs are also coming to the rescue in this area [13].

More serious drawbacks of the sampled-data technique are aliasing, imaging and sample-and-hold distortion. The effect of sampling a continuous-time signal is illustrated by fig.1.6, which shows how bands of frequencies are "folded back" on top of the baseband response, which is from DC to the 'Nyquist frequency', \(\omega_s/2\) [14].
Fig. 1.7 Imaging & reconstruction of sampled signal

Imaging is the dual to aliasing and concerns the conversion of a sampled signal into a continuous-time one. This process is shown in fig. 1.7. The sampled-data system is idealised, and considered to be processing infinitely narrow data samples. These samples must pass through a hold function before they can be filtered in the continuous domain, as shown. The spectrum of the sampled signal is only drawn up to half the clock frequency, since processing within the sampled-data system is necessarily limited to this baseband. It can be seen that the hold function has introduced a $\sin(x)/x$ attenuation, and that the baseband signal is 'imaged' around multiples of the sampling frequency. Ideally, the (lowpass) filter shown will eliminate all images above the baseband, leaving a reconstructed signal $Y_c$.

Fig. 1.8 Standard SC system with anti-alias & anti-image filters
In standard single-path SC circuits, where one is concerned only with processing baseband signals (ie. those from DC up to the Nyquist frequency), the detrimental effects of aliasing and imaging are substantially reduced by including continuous-time lowpass filters in series with the inputs and outputs, as shown in fig.1.8. These attenuate signals at frequencies below the Nyquist frequency, and so eliminate unwanted frequency components. The effects of sampling are not confined just to the signals that are intentionally being processed, however, and aliasing of wideband noise within the circuit is a significant problem for SC circuits. This noise, whose origins have already been mentioned, is folded back into the baseband in exactly the same way as discussed for the filtered signals. There is therefore an accumulation of noise in the baseband, and circuit dynamic range is reduced. The noise is band-limited by the circuit's resistor-capacitor network and by the amplifier bandwidth, and so the latter must not be made any higher than is absolutely necessary for adequate amplifier settling behaviour. Analysis shows that the overall thermal noise power in a standard SC circuit, where the amplifier bandwidth has been set according to this criteria, is proportional to $kT/C$, where $k$ is Boltzmann's constant, $T$ the absolute temperature, and $C$ is the unit-size of a circuit capacitor. The switch on-resistance, $R_{on}$, does not enter the equation, since increasing $R_{on}$ has the dual effect of increasing resistive thermal noise and decreasing the noise bandwidth, and these effects cancel. The main design parameter determining noise level is therefore the circuit capacitance, implying that some trade-off exists between circuit speed, which requires low circuit capacitance, and dynamic range, which requires low noise levels.

1.4 GaAs for high-speed SC circuits

1.4.1 Past work

GaAs SC circuits offer the attractive possibility of sampled-data analogue signal processing in the range 1-100MHz, making it suitable for a range of applications, including IF and agile filtering for radar systems [32,34], clock recovery in communication receivers [32], high-frequency A-to-D and D-to-A converters [43], and anti-alias and anti-image filters for new generations of GaAs DSP circuits [44-47]. In contrast to other areas of SC circuit design, where interest peaked during the early 1980's [15], the field of high-frequency design has been active more recently, and many of the papers cited in this thesis have appeared since 1986. General issues in the design of high-frequency SC filters have been dealt with by a number of papers [16,17,18], and review papers dealing with the particular problems posed by GaAs technology
have also appeared [19,20,21]. Quite recently, books on GaAs technology have been published with chapters dedicated to GaAs SC circuits [22,23,24], and recent sessions of the IEEE ISCAS conferences have also been given over to the subject [25,140].

The earliest reference found to an SC circuit processing signals in the MHz range was due to Matsui et al who used highly optimised, but quite simple, SC circuits for video signal processing [26,27]. Pioneering work on more complex filter circuits was performed by Choi et al, who produced a 6th order elliptic bandpass filter with a centre frequency at 260kHz using 4µ CMOS technology [28]. Another early demonstration of a high-frequency (15MHz) SC filter was given by Ribner et al [29]. At about the same time the first reported work on GaAs SC filters was undertaken by workers at STC and Imperial College London [30-35], though initial results were disappointing, since many of the difficulties in using GaAs (see section 1.4.3) had not yet been appreciated. Other groups have now also started working in the GaAs SC area, and some results have recently been reported [36,37]. Research into high frequency CMOS has also continued, with particularly impressive results being reported recently by Song, who has produced a 10.7MHz bandpass filter using 2.25µ CMOS technology [38-40]. This achievement represents a considerable challenge to GaAs SC research from the point of view of frequency performance. Some work has been done recently on a radically different approach to high-frequency SC circuit architectures, in which the customary separation of amplifier, switch and capacitor is no longer observed, and the smallest identifiable circuit unit is an integrator. This circuit has been reported recently, and results from a trial fabrication are still awaited [41].

1.4.2 Commercial exploitation of GaAs

GaAs circuits were originally developed for their excellent properties in microwave applications. These include high speed, low noise, a low susceptibility to ionising radiation, and good temperature stability [60]. The first Microwave Monolithic Integrated Circuits (MMIC's) appeared on the market in 1974, and the industry is growing steadily [23]. The current increase in the market for Direct Broadcast Satellite (DBS) satellite systems is expected to be a continuing stimulus for growth in this sector, and a number of manufacturers now offer foundry facilities, thus allowing widespread use of this technology [47,61-63].

There is also an increasing interest in using GaAs for high-speed digital circuits [47,49,64] and some foundries specialise in this area (eg. [65]). GaAs digital circuits offer several advantages over Si ECL, their closest competitor, including lower speed-power product and much higher device
Not only have digital GaAs building-blocks with impressive clock rates been reported [66-69], thus demonstrating the capabilities of the technology, but also commercial systems are coming into widespread use. Hewlett Packard recently reported a 1GHz 6-bit A/D converter, which uses a GaAs sampler at its front-end, and this circuit has now been incorporated into a commercial oscilloscope [70,71]. In a review of progress in the GaAs industry, Vlahos summarises work done to redesign standard Si parts for implementation in GaAs [72], the manufacture of standard parts clearly indicating a well established technology. The American DoD has invested heavily in the development of GaAs digital circuits, and work on a complete GaAs microprocessor is well advanced [73,74]. Also, the processors at the heart of the latest Cray supercomputer - the Cray 3 - are of GaAs. Finally, the recent appearance of commercial GaAs operational amplifiers [75-77] demonstrates the widening use of GaAs at MHz frequencies, and shows that it is not confined simply to digital circuits. For further information on recent progress in the GaAs electronic industry the reader is referred to the extensive literature now available [72,77-80].

Critical application areas for GaAs are optics and opto-electronics. The lattice structure of GaAs makes it a valuable opto-electronic material [81], and it has been exploited extensively in optical sensors and light-emitting diodes for many years. The ever-increasing demands of the telecommunications industry, coupled with advances in optical fibre technology [82], have stimulated a prodigious amount of research into opto-electronic materials and devices. In particular, there is currently a strong interest in developing opto-electronic IC's (OEIC's) - circuits which combine optical devices, such as photodetectors and laser-diodes, together with their electronic drive circuitry on a single chip - and GaAs is a major component of these systems [83,84]. The benefits to the telecommunications industry of OEIC's are potentially enormous, and the market for the devices is correspondingly large [83].

It can be seen that there is a large and increasing amount of activity in the areas of GaAs microwave, digital, optical and optoelectronic circuits. We propose that these activities will have a large spill-over effect into the GaAs analogue area, reinforcing the already existing incentives to develop GaAs analogue circuits. Possible spin-offs from these areas include, from the microwave field, the use of GaAs analogue circuits for IF-frequency processing, allowing the complete integration of front-end and IF circuits onto a single GaAs chip. Similarly, analogue pre- and post-processing may be required for certain GaAs DSP systems, and this might be more conveniently done with circuits that could be integrated with the GaAs DSP. Furthermore, the extensive use of GaAs in the different fields described ensures the
continual refinement of GaAs processing technology, and therefore the gradual removal of some of the technological obstacles to developing GaAs analogue circuits. Research in this area is therefore underpinned by the large amount of research and development in other application areas and this, we believe, ensures the relevance of novel circuit development work using GaAs.

1.4.3 Technology issues for GaAs SC circuits

The most important physical and electronic properties of GaAs are compared with those of Si in fig.1.9, where some indication of the relationship between these properties and important design issues are drawn. For example, following the topmost path in the diagram from left to right shows that the large bandgap of GaAs compared to Si (indicated by the top left-hand box) causes the thermal conductivity of GaAs chips to be low (top-centre box), which gives cooling problems in designs using such chips (top-right-hand box). Note that, since only electronic properties are considered, the fact that GaAs is a direct-bandgap material is not highlighted in the diagram, even though it is of fundamental importance in optical applications. The reader is left to explore the relationships drawn in the diagram, and is referred to [81] for a more detailed explanation of the GaAs device physics on which it is based. The right-hand column of the diagram is an effective summary of the advantageous and disadvantageous properties of GaAs for realising analogue IC's, and of the five highlighted advantages the crucial ones for high-frequency performance are low stray capacitance and high FET gain-bandwidth product. These two factors will now be considered in detail.
In the past the speed advantage of GaAs circuits over Si has been somewhat overstated, leading to disappointment in recent years that earlier expectations have not been met. Simple arguments based on the relative peak mobility of electrons in intrinsic (undoped) GaAs and Si led to a widespread belief that GaAs devices were inherently about five times faster than their Si counterparts [141]. Unfortunately, this view took little account of the complex
physics of the devices. In particular, the presence of dopant in GaAs leads to a significant reduction in electron mobility, so that doped GaAs and Si are in fact quite similar from this point of view [48]. It is nonetheless a fact that the most advanced GaAs devices have been consistently faster than their Si bipolar competitors for a number of years [49]. Also, although detailed comparisons of the speed of GaAs and Si technologies shows that the advantage of the former over Si bipolar is only slight [23,50], SC circuits require a FET technology for the realization of switches, and it is known that Si MOSFET transistors are much slower than GaAs MESFETs [51]. The possibility now exists to combine some of the high-frequency advantages of Si bipolar with the insulating-gate advantage of MOSFETs by using BiCMOS technologies, and many new processes have been developed [51-56]. However, the frequency performance of npn transistors in BiCMOS processes is still significantly lower than can be achieved with GaAs, and the highest reported $f_t$ of the bipolar transistors from the latter references is 9GHz [55,56]. This compares with $f_t$ figures of around 20GHz for pure bipolar processes [50], and an $f_t$ of 80GHz reported for a 0.2µm GaAs MESFET process [57]. Such a high bandwidth FET clearly allows the design of amplifiers with shorter settling-times, which is one of the key factors in limiting the clock frequency of an SC circuit.

![Fig.1.10](image)

Fig.1.10 (a) Parasitic sensitive SC integrator, (b) CMOS switch, (c) switch realization in GaAs

A great advantage of GaAs for SC applications is that it is far less troubled by parasitic capacitances than Si. To appreciate the reasons for this, consider the simple, parasitic-sensitive SC integrator shown in fig.1.10 [2], where the capacitors $C_{s1}$ to $C_{s4}$ and $C_{j1}$ to $C_{j4}$ are parasitic. $C_{s1}$ and $C_{s2}$ are interconnect capacitances, caused by coupling between adjacent metal connections or between these connections and the substrate or well over which they run. $C_{s3}$ is an amalgamation of the interconnection capacitances
for that node, the input capacitance to the amplifier, and any parasitic
associated with the left hand plate of \( C_2 \). \( C_{s4} \) is the bottom plate parasitic
capacitance of \( C_1 \), and its top-plate parasitic is considered negligible. The

capacitors \( C_{j1} \) to \( C_{j4} \) are made-up of the junction capacitance at the sources
and drains of the switches. Now, assuming an ideal amplifier with a perfect
virtual earth, the only parasitics shown in fig.1.10a which will affect the
transfer function of this circuit are \( C_{j2}, C_{j3} \) and \( C_{s2} \), since they add directly to
the effective value of \( C_1 \). All the other parasitics are either grounded or
driven from a voltage source, and do not affect the charging and discharging
of \( C_1 \). Some other parasitics, caused by the \( C_{gs} \) capacitance of the switches,
may also be significant, as will be discussed shortly.

Now, a typical CMOS design will use a complementary switch, such as
that shown in fig.1.10b, in order to cancel clock-feedthrough effects. Taking
parameters for a typical digital process [58], and using minimum geometry
switches (\( W=4\mu, L=2\mu \)) it is found that the \( C_j \) of one switch terminal is
approximately 20fF. The unavoidable) interconnection capacitance between
the connecting metal layer and the substrate is about 20\( \mu \)F/m\(^2\), which
indicates that a typical circuit node, connected to two switches and about 100\( \mu \)
of interconnect may have a parasitic capacitance of approximately 50fF. Since
unit capacitor sizes are usually minimized to conserve chip area (and, if
appropriate, maximise circuit speed), they are frequently as low as 100fF, and
so the parasitic clearly has a very significant value.

The situation is quite different for GaAs, however. In this case, the
semi-insulating substrate means that interconnection capacitances between
the metal and the substrate are negligibly small, as are the parasitics between
the device junctions and the body material (the resistivity of Si substrates is at
least 3 orders of magnitude lower than that of GaAs substrates [23, ch.5]). Out
of the parasitics so far considered, this leaves the capacitance at the input to
the amplifier which, as has been mentioned, has little effect on the circuit
through being attached to the amplifier virtual earth. There is, however,
another important parasitic in GaAs, which is the gate-channel capacitance of
the switching FET's. The effect of this parasitic is small in Si due to the use of
complementary switches, where the gate parasitic on the n-channel device is
approximately cancelled by that of the p-channel device (see fig.1.10b). Such
complementary structures are not possible using a D-MESFET process, and so
a simple switching-element, such as that shown in fig.1.10c must be used.
The value of the parasitic gate capacitance would typically be around 10-20fF,
but its actual effect on the circuit transfer function will depend on the position
of the switch in the circuit and the values that \( V_C \), the switch control voltage,
switches between. Overall, the combination of fast active devices and low
parasitics is seen to give GaAs great potential for use in high-speed SC circuits.

Other technology issues that are important to GaAs SC circuits are the early-saturation-effect and the device threshold voltage. We define the threshold voltage, \( V_t \), as the value of \( V_{gs} \) for which a MESFET goes into its cutoff region. In a classic JFET model the value of \( V_{ds} \) for each knee in the device output characteristic is a function of \( V_{gs} \), and is equal to \(|V_t|\) for \( V_{gs}=0\) [100]. Some processes produce devices where the knees of the curves on the output characteristic all occur at approximately the same value of \( V_{ds} \), where this knee voltage is significantly lower than \(|V_t|\) [106]. The modified behaviour is sometimes known as the early saturation effect [102], and occurs primarily in processes with high device thresholds [198]. This effect is a consequence of the strong electric field under the gate of short-channel MESFETs, which alters the mechanism for drain-current saturation from a ‘pinchoff’ effect to electron-velocity-saturation [81]. It may be put to good use in some circuits, where novel configurations can be used to keep devices in saturation [102]. The absolute value of \( V_t \) is also an important issue in some processes, since it has a large impact on switch design and on overall circuit power consumption. This issue is returned to later.

1.4.4 GaAs SC circuit techniques

**Amplifiers**: Amplifier design using GaAs MESFETs is more difficult than with Si CMOS for a number of reasons. Firstly, the lack of a p-channel device (one of the drawbacks in using GaAs cited in the right-hand column of fig.1.9), makes it far more difficult to achieve economical level shifting than, for example, with the popular CMOS folded cascode amplifier [2]. The latter structure is impossible without a complementary device. GaAs MESFET processes generally lack an enhancement device also, and this further restricts design freedom. To aggravate matters, the low intrinsic gain of GaAs MESFETs makes it difficult to achieve the required 60dB gain figure.

![Fig.1.11 Two-stage GaAs op-amp](image-url)
Fig. 1.11 shows a 2-stage GaAs op-amp [31], based on the same structure as the classic CMOS 2-stage op-amp [2]. We first note that the number of devices in this design is 22, twice that of the folded cascode amplifier just referred to. Ten of these devices are accounted for by the level-shifting diodes, a consequence of being restricted to a single device type. The gain of this amplifier when fabricated was around 40dB, such a low figure being a direct consequence of the low intrinsic FET gain. Amplifier settling time was approximately 2ns.

As for CMOS designs, amplifier bandwidth may be improved by moving to a single-stage structure, and some work has been done in this area. Fig. 1.12 shows a single-stage double-cascode amplifier, with a single-ended input, which can achieve a gain of around 60dB and a typical minimum settling time for a 1μ GaAs process of 630ps [23, ch.10]. Briefly, transistors $M_2$ and $M_3$ are used to cascode the input device $M_1$, while the current-source load is provided by $M_4$, which is "bootstrapped" by $M_5$ and $M_6$. The left-hand chain is carefully arranged to provide the required bias levels. The design well illustrates the price that must be paid for high gain and bandwidth, since the large number of devices in the output chain will restrict output swing and, therefore, dynamic range, and the absence of a differential input will result in a poor PSRR. To directly extend this structure to provide a differential input would firstly require duplicating every device, then adding another series transistor to give the tail of the differential pair. The result would be a monstrous circuit, and so alternative methods for adapting this structure for differential input have been explored [87]. They do, however, result in what is effectively a two-stage structure, and amplifier phase margin is sacrificed as a result. Another potential inconvenience of the circuit is that there is a level shift from input to output of $-V_{SS}$, since the input must be at a quiescent voltage of $V_{SS}$. 


The difficulty in designing high-gain GaAs amplifiers has led to a considerable effort to develop circuit architectures that function accurately using amplifiers with gain<60dB. The solutions that have emerged can be divided into two categories. Firstly, a number of circuits have been produced that have a low sensitivity to amplifier gain [88-91], so that the error due to amplifier gain is less than that produced in a conventional circuit [8]. Secondly, some proposed circuits use an a-priori knowledge of the amplifier gain so that it may be compensated for by predistortion of the circuit transfer function [92-94]. The use of novel architectures to overcome the gain limitations of GaAs amplifiers is a key factor in the work described in this thesis.

Work on high-frequency SC circuits in both GaAs and CMOS technologies requires careful optimisation of all aspects of circuit operation, but the settling behaviour of the amplifiers is particularly important in determining the maximum clock frequency which can be achieved. The analysis and optimisation of amplifier settling-time has therefore been treated by several groups of workers [27,97-99], and is also examined in detail later in this thesis.

**Switches**: Consider the case of a capacitor being charged from a voltage source via a MESFET switch, as shown in fig.1.13a. If the charge on the capacitor at \( t=0 \) is zero, then it can be shown that the time to charge the capacitor to a voltage \( V_{\text{out}} \) is a function of \( V_{\text{in}} \) and, importantly, when \( V_{\text{in}} \) has a value \( V_g - V_t \), this charge time becomes infinite. This is caused by the ever decreasing value of \( V_{gs} \) as the source voltage of the FET is charged towards \( V_{\text{in}} \). The consequent increase in channel resistance prolongs the charge time indefinitely.
Such problems are overcome in Si MOS circuits by either (i) raising $V_g$ to a high value, equal to or greater than the circuit's positive supply voltage, and/or (ii) using complementary devices, so that at least one of the two FETs conducts during the switch on-period (see fig.1.10b). These solutions are not available to the GaAs designer, however. In the first case, setting $V_g$ to a high value risks forward-biasing the Schottky-diode gate junction, causing unwanted charge to be injected into the circuit. In the second case, complementary devices are not available in standard GaAs processes for technological reasons; the low mobility of holes in GaAs makes p-type devices slow and unattractive for manufacture (see fig.1.9).

The solution to both of these problems is to control $V_g$ from the voltage at the driven switch terminal, ensuring that its value is sufficiently high for efficient circuit operation, while simultaneously guarding against forward biasing of the gate junction. Fig.1.13b shows schematically how this is achieved, with a Switch Control Circuit (SCC) controlled by two inputs, one from the driven switch terminal, the other from the switch clock line. A number of alternative designs for SCC circuits in GaAs have been proposed [30,36], and we review the main issues in their design using the example shown in fig.1.14, which comes from an early SC filter design [32].
In this diagram, the SCC consists of transistors $M_1$ to $M_4$, while $M_5$ is the transmission gate FET that the SCC is attempting to control. The switching operation is as follows. To turn the switch off, the clock input to the SCC, $V_c$, is set to $V_{ss}$, which turns $M_4$ on and therefore pulls the gate of $M_5$ down to near $V_{ss}$ (the exact voltage depending on the device width ratio of $M_3$ to $M_4$). The $V_{gs}$ of $M_1$, (40$\mu$) is slightly positive in this state, as the current passing through it is the sum of the saturated drain currents of $M_2$ (40$\mu$) and $M_3$ (10$\mu$), both of which have $V_{gs} = 0$. To turn the switch off, the gate of $M_4$ is pulled down at least one threshold voltage below $V_{ss}$, thus cutting off $M_4$ and effectively turning $M_3$ into a conducting transmission gate connecting the gate of $M_5$ to the source of $M_1$. The $M_5$ gate is, therefore, driven to a voltage approximately equal to that at the analogue input. The diagram indicates the relative sizes of the FETs in the SCC, showing that the SCC and switch require a total of 12 unit-sized FETs (in contrast to the 2 or 3 units for a complementary CMOS switch). A similar circuit has been proposed in [102] with diodes connected across the $M_3$ transistor to provide a fixed voltage swing at the gate of $M_5$, and so avoid signal dependent clock feedthrough.

Fig.1.15 shows an SCC proposed by Harrold [101] which differs from the previous example in that it is an 'unbuffered' design, where current for the SCC is drawn from the analogue input, $V_{in}$. This strategy clearly impacts the design of the preceding amplifier's output stage, which needs greater current-driving capability, but has the advantage of simplifying the SCC itself. Diodes are included to make the signal swing at the $M_5$ gate approximately constant (not as many are required as in the Larson design because of differences in the process used), and so signal-dependent clock feedthrough is reduced. The cascode device, $M_2$, is included to minimise the variation in current drawn by the SCC, as such variations produce an
IR potential drop across the amplifier output impedance which are coupled into the signal path to give another form of signal-dependent clock feedthrough.

![Unbuffered SCC](image)

Note that not all of the switches in a GaAs SC circuit will require an SCC. In the case of a capacitor being discharged from an initial voltage $V$ to ground it can be shown that the discharge time is only a weak function of $V$. In this case, there is also no risk of forward-biasing the MESFET gate and adequate on-conductance is assured. An SCC is therefore not required to control the discharge of capacitors to ground or virtual ground, and this fact is exploited in circuit designs [101].

The requirement for switch off-resistance, $R_{off}$, is that the time constant given by the product of $R_{off}$ and the load capacitor be much larger than a clock period, and this criteria is easily met by high-speed GaAs SC circuits. The speed of switching is determined by the gate capacitance of the switching element and the driving ability of the circuit used to switch it, and this should be made much faster than the $R_{on}C$ time constant. The final requirement on the switches is that they should produce as little noise as possible. In order to reduce clock feedthrough, switch sizes should be reduced as far as is consistent with having adequate on-conductance, as this will minimise switch parasitic capacitances. In this respect, GaAs generally gives a better compromise between clock feedthrough levels and switch on-resistance than Si MOS, as MESFET parasitic capacitances are lower than in Si (due mainly to shorter gate-lengths achievable in GaAs technology), and the voltage swings at the switch gates are lower (due to the use of SCC's). Clock feedthrough levels may also be reduced by cancellation from complementary switch devices, a standard technique in CMOS technology. Since GaAs processes do not provide a complementary device, however, a possible alternative is to use a dummy switch to inject cancelling
clock noise. However, this option, which has been tried in NMOS technology [2], is known to have limited effectiveness [142] and has not, to our knowledge ever been used in GaAs circuits. A more comprehensive technique for reducing clock-feedthrough is to use a fully differential filter implementation [28], for which clock-feedthrough noise and power supply variations appear as common mode signals, and therefore will not affect filter response. Again, however, no such implementation has been reported yet for a GaAs circuit.

The other major source of switch noise is intrinsic thermal and flicker noise. In the past, the high levels of flicker noise common in GaAs MESFET's has been a cause for concern. The corner frequency for flicker noise in GaAs is generally around 10MHz, which is about the same as the signal bandwidth of GaAs SC systems. However, when calculating the noise spectrum in a sampled system it is necessary to take account of aliasing effects, and these substantially increase the effect of thermal noise [2]. Since all of the 1/f noise components are well below the Nyquist frequency of any GaAs SC circuit, they are not increased by aliasing, and the effective corner frequency for the 1/f noise is substantially reduced. As in Si, therefore, switch thermal noise is dominant in GaAs circuits, and similar performance limitations apply [103,104].

**Capacitors:** The different types of capacitor available for GaAs process are distinguished by the dielectric used (Silicon Nitride or Polyimide) and by the layout of the devices (overlay or interdigitated). In addition, the deposition technique used for the dielectric may also significantly effect device characteristics [60, ch.10]. The factors that the circuit designer will be concerned with are (i) the capacitance per unit area (ii) the Q-factor, and (iii) the ratio-accuracy of the capacitors. The first two of these will almost certainly mandate the use of a Silicon Nitride dielectric, since polyimide is generally deposited in much thicker layers than Silicon Nitride and gives impractically low capacitance per unit area for SC applications (see chapter 4). Even more important, it gives capacitors with lower Q factor, with values from 50 to 100 being typical at MHz frequencies [23]. It is also because of Q-factor considerations that overlay capacitors are chosen in favour of the interdigitated type, which typically have Q-factors less than 10 at MHz frequencies.

**Models:** In GaAs circuits, accurate modelling of the MESFETs frequently represents a challenge, since processes are often only characterised at frequencies of interest to microwave applications (ie ≥1GHz), and accurate large signal models of the devices, for use with standard analogue simulation programs such as Spice [105], are rarely available. Furthermore, even if such
models are available they often have characteristics that cannot be represented by the standard simulation program transistor models. For these reasons a large body of work has been dedicated to modelling the large-signal behaviour of MESFETs. This ranges from proposals for new algorithms for modelling large-signal MESFET behaviour [106], to special techniques for using existing simulators [107-109] and work on particular aspects of MESFET behaviour, such as output frequency dispersion [110,111]. Work on new simulation programs, which have considerably more flexibility in the specification of device models than their predecessors, has recently been published [112-114]. Details of the steps taken in this project to overcome the limitations of available models and simulation programs are described later in this thesis.

1.5 Narrow-Band filtering using SC techniques

Definitions: The relative bandwidth of a bandpass filter with bandwidth BW (Hz) and centre frequency $f_0$ is defined as:

$$RBW = \frac{100 \times BW}{f_0}$$

Also, the filter $Q$ is defined as:

$$Q = \frac{f_0}{BW}$$

For convenience, we shall refer to filters with relative bandwidths between 10% and 1% as Narrow-Band (NB), with 1% > RBW > 0.1% as Very-Narrow-Band (VNB), and with RBW < 0.1% as Ultra-Narrow-Band (UNB).

1.5.1 Background

The increasingly efficient exploitation of the electromagnetic spectrum, and corresponding increase in high-frequency signal processing applications, has inevitably raised designers' interest in narrow-band filter techniques. Although the narrowest bandwidth specifications are presently to be found in the high MHz and GHz frequency ranges, where Surface Acoustic Wave (SAW) filters are used to realise Q's of many thousands [115], FM communication systems also frequently require high-Q filters, and bandpass filters with relative bandwidths of a fraction of a percent may be needed for some FM applications [116]. At the low end of the spectrum, very narrow-band transmit and receive filters are required for circuits such as tone detectors [193]. They are also important in applications where many digital signals of low baud-rate are to be transmitted on a single audio-frequency
It was demonstrated in section 1.3.2 that SC circuits offer significant advantages over other IC technologies for specifications requiring quite high precision with low power and chip area. In the low MHz frequencies, successful implementation of narrow-band SC circuits may allow their use in applications formerly covered by SAW filters, especially if the application would benefit from the tunability available in an SC filter. At low frequencies, the cost advantages over digital solutions have already been established. For these reasons, a considerable effort has been invested in developing narrow-band SC filters, and some of this work is reviewed in the next sub-section.

Our investigation has been particularly motivated by contributions to the subject by J. Franca [94, 118, 125-127, 194-197], who developed detailed multi-rate filtering schemes, based on earlier work for digital circuits, for application to SC filters. The most ambitious of these schemes was for bandpass filtering systems with relative bandwidths down to 0.01%, and it is with these systems that we are primarily concerned. Although the cost of implementing such systems is high, the prospect of producing integrated, easily-tunable building-blocks is correspondingly attractive. The quest to meet the objective of UNB SC filtering stretches the capabilities of current IC technology near to its limits. Research into circuits for implementing UNB SC filters therefore not only has the aim of producing useful filter systems, it also allows us to explore the boundaries of what is possible using SC technology.

1.5.2 Techniques for narrow-band SC filters

Conventional single-path ladder filters are used for some NB filter applications, but their realisation becomes progressively more difficult as the relative bandwidth is decreased for three main reasons. Firstly, the dynamic range of an SC filter tends to decrease in proportion to increasing filter Q [39]. Also, high-Q SC filters have high capacitor spreads [2], and finally, high-Q filters have high sensitivities to component variations and imperfections [28, 119]. An example of what can presently be achieved is provided by Song & Gray [39] who produced a 6th-order elliptic bandpass SC filter with Q = 55 and a centre frequency of 3.1MHz. Its dynamic range was 46dB for an allowed 1% intermodulation distortion. A previous design by Choi et al [28] achieved a dynamic range of 70dB for a filter with a Q of 40 at 260kHz. Some of the limitations in conventional high-Q filters were overcome by the use of N-path techniques, a concept first introduced by Franks & Sandberg [120] to overcome similar problems in active-RC filters.

An N-path filter is shown schematically in fig. 1.16. It consists of N nominally identical filters which are switched into the signal path in turn,
such that each samples the input signal at a rate $f_s=1/T$. The Nyquist frequency for each path filter acting alone is $fs/2$, but the sampling frequency at the input and output of the complete N-path filter is $N*fs$ and, as a consequence, its Nyquist frequency is $N*fs/2$. Its frequency response is, from inspection of the diagram, the same as that of the path filters from which it is composed, but now the baseband is defined up to $N*fs/2$ and if the transfer function of these path-filters is lowpass then useable bandpass responses are generated at multiples of the clock frequency. These bandpass functions correspond to the alias responses of the path-filters but, since the baseband of the N-path system has now been extended to $N*fs/2$, they may be used without ambiguity. By setting a high ratio of clock-to band-edge frequency for the path-filters these bandpass responses may be made narrowband without encountering any of the noise and sensitivity problems of a single-path filter, since the noise and sensitivity properties of the N-path system are the same as those of the lowpass path-filters.

Fig.1.16 An N-path filter

Correct operation of the N-path filter relies upon precise matching of the path filters, however. Any path mismatch, due to inevitable component variations, will result in deviation of the N-path filter response from its ideal shape and the production of residual aliases (mirror components). As an implementation example, Von Gruenigen et al [121] produced a 4-path filter based on a first-order lowpass cell, achieving a relative bandwidth of 1.15% at a centre frequency of 1kHz. This was done using a capacitor spread of approximately 45 and the circuit had a quoted signal-to-noise ratio of 71dB and a mirror frequency rejection of 45.1dB.

An important problem affecting this and other designs that use lowpass
path-filters is that, because the resulting bandpass responses are centred at multiples of the clock frequency, in-band clock feedthrough noise and mirror components drastically reduce the dynamic range of the circuit (see also [2]). One way of avoiding in-band clock-feedthrough is to use high-pass path-filters [122], but unfortunately this does nothing to reduce mirror-frequency components produced within the passband [119,121]. These problems led to the proposal of pseudo-N-path (PNP) filters [123], which can be derived from a given N-path filter by taking a single path-filter from the latter, then modifying every integrator so that it cyclically stores and retrieves N different states of its integration capacitor [119]. An integrator circuit that achieves this end is shown in fig.1.17 [119]. In this circuit, the op-amp and integration capacitor, $C_{s4}$, are shared between all of the N paths and the integrator charge for paths not being used at any given instant is stored on the capacitors $C_{s1}$-$C_{s3}$. This principle is applied to produce a filter by replacing integrators in a conventional lowpass filter by the PNP integrator shown. This extends the baseband of the resulting filter to $N*fs/2$ and the filter has a bandpass response at multiples of fs, as for a normal N-path filter.

Fig.1.17 A RAM-type pseudo-N-type (PNP) integrator building-block, (N=3)

The major advantage of this pseudo-N-path approach is that, because $C_{s1}$-$C_{s3}$ are merely storage capacitors and do not ideally appear in the integrator transfer function, the path mismatch problems of true N-path filters are eliminated. Unfortunately, this "RAM-type" PNP circuit does not completely eliminate the problem of in-band clock-feedthrough and mirrors, since imperfect charge-transfer onto and off-of the (imperfectly-matched) capacitors $C_{s1}$-$C_{s3}$ causes the latter to appear in the integrator transfer function. This is a significant limitation on circuit performance and so to overcome it the 'Circulating-Delay' PNP circuit is frequently employed [119]. In contrast to the RAM-type cell, the Circulating-Delay circuit, shown in

45
Instead, it shunts the stored integrator states from one storage capacitor to the next so that every charge packet follows the route $C_{s4} \rightarrow C_{s3} \rightarrow C_{s2} \rightarrow C_{s1} \rightarrow C_{s4}$. Thus every path is truly identical and mirrors are not produced. Furthermore, if we let the circuit's single clock frequency be $N*fs$ then it can be shown that the circuit has its first bandpass response at $fs$, so that clock-feedthrough is out-of-band. Against its advantages, the circulating-delay cell requires the amplifier to operate $(N+1)/2$ times faster than the RAM-type for a given filtering frequency, and the increased number of charge-transfers increases the degradation in the filter transfer function due to non-ideal effects.

![Image of a Circulating-Delay-type PNP integrator building-block, (N=3)](image)

**Fig.1.18** A Circulating-Delay-type PNP integrator building-block, (N=3)

One other important PNP structure, known as the 'hybrid' PNP [124], combines some of the properties of the RAM and Circulating-Delay structures, although at a higher component cost than either of them. An example 3-path circuit is shown in fig.1.19. The operation of the circuit causes charge to circulate through $(N-1)$ distinct paths so that any asymmetry in those paths introduces clock-feedthrough at multiples of $fs/(N-1)$, not in the main passbands, which are centred at multiples of $fs/N$. For the same reason, mirrors are also out of band. In this example, where $N=3$, the circulation paths are $C \rightarrow C_4 \rightarrow C_1 \rightarrow C_3 \rightarrow C$ and $C \rightarrow C_4 \rightarrow C_2 \rightarrow C_3 \rightarrow C$. The other advantage of this structure is that its speed is equal to that of the RAM-type circuit, since there are only two clock phases at frequency $fc$, the sampling frequency at the input to the integrator. A slight disadvantage of the circuit, in addition to the implementation cost, is that the number of charge-transfers per cycle of operation is greater than that for the RAM-type circuit, and so its sensitivity to amplifier gain-bandwidth-product will be correspondingly increased.
An important limiting factor in the use of PNP structures is their poor noise performance when compared to pure N-path structures. For example, it has been shown that noise figures in a Circulating-Delay PNP filter are around $N$ times higher than in an equivalent N-path circuit [143], a factor which clearly disadvantages PNP filters with respect to their N-path counterparts. An alternative method for obtaining narrow-band filters, but without using multiple paths, is to make constructive use of an SC filter's alias and image responses by using bandpass anti-alias and anti-image filters [118,125,126]. Such a filter is called a single-path frequency-translated (SPFT) system, and is illustrated in fig. 1.20. At the front-end of the filter system is an anti-alias filter (AAF) which consists of a continuous-time bandpass AAF followed by an SC bandpass AAF, and only passes signals in a selected Nyquist band of the core filter. This involves an increased design effort for the SC AAF and AIF filters, but the overall result is much more efficient than a conventional system [127,128]. The output of the filter inevitably suffers some attenuation due to the sample-and-hold effect, and this attenuation is one of the factors that limits the applicability of the technique. It is estimated that, for an SPFT system based on a single-path bandpass filter with a $Q$-factor of $Q$, the maximum 'Q-enhancement factor', $K$, obtainable from the system is about 28. This would give a maximum effective $Q$ of $Q_{eff}=28Q$ [125].

In order to increase the achievable $Q$-enhancement-factor above this
limit, Franca proposed the use of N-path frequency-translated (NPFT) systems. Such a system, illustrated in fig.1.21, is identical to the SPFT filter, except that the core filter is now an N-path filter with bandpass path-filters, so that the Nyquist frequency of the core filter is increased from $f_s/2$ to $N^*f_s/2$ and sample-and-hold attenuation consequently reduced. Important considerations in the design are, firstly, the use of bandpass path-filters to eliminate the problems of in-band clock-feedthrough and mirrors and, secondly, the partial cancellation of mirror components by the N-path structure, which is important in reducing the selectivity requirements of the anti-alias and anti-image filters.

Fig.1.20 A Single-Path Frequency-Translated (SPFT) filter system, (a) filter structure, (b) details of frequency response
1.5.3 Structures for Ultra-Narrow-Band SC filters

This subsection will briefly consider and compare the potential of the alternative filter structures introduced above for UNB filtering applications.
<table>
<thead>
<tr>
<th></th>
<th>passband frequency, $f_0$</th>
<th>clock-feedthrough frequency</th>
<th>number of charge-transfers per cycle</th>
<th>number of clock phases per cycle</th>
<th>main strength</th>
<th>main weakness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple N-path</td>
<td>$fs.n/N$</td>
<td>$fs.n/N$</td>
<td>1</td>
<td>2N</td>
<td>simplicity</td>
<td>path mismatch</td>
</tr>
<tr>
<td>Circulating-Delay PNP [230]</td>
<td>$fs.n/N$</td>
<td>$fs.n$</td>
<td>$N+2$</td>
<td>$N(N+1)$</td>
<td>absence of in-band mirrors &amp; clock noise</td>
<td>sensitivity to amplifier gain-bw</td>
</tr>
<tr>
<td>RAM-type PNP [230]</td>
<td>$fs.n/N$</td>
<td>$fs.n/N$</td>
<td>3</td>
<td>2N</td>
<td>speed cf. Circ-Delay design</td>
<td>in-band clock noise</td>
</tr>
<tr>
<td>Hybrid PNP [230]</td>
<td>$fs.n/N$</td>
<td>$fs.n/(N-1)$</td>
<td>5</td>
<td>2N</td>
<td>speed cf. Circ-Delay design</td>
<td>component cost</td>
</tr>
</tbody>
</table>

Fig.1.22 Comparison of characteristics of the N-path filter with different PNP filters

The relative merits of a simple N-path and different classes of PNP filter are summarized in fig.1.22 and fig.1.23. In all cases the circuits being compared are integrator blocks with a maximum clock frequency of $fs$. Considering fig.1.22 first, column 1 gives the positions of the bandpass responses when the integrator block is used in a lowpass structure, which, from the theory of N-path filters already discussed, results in useable bandpass responses at multiples of $fs$ up to the modified Nyquist frequency of $N*fs/2$, where $fs$ is the sampling frequency of each of the (pseudo) paths. It can be seen that only the Circulating-Delay and hybrid blocks have the desirable property of zero in-band clock-feedthrough, and that there is a tradeoff between these two of gain-bandwidth-product sensitivity against component cost (see fig.1.23). Although it has already been indicated that noise considerations preclude the exclusive use of such structures to attain UNB filtering, it will be shown later in this thesis that they do have a role to play.
Fig.1.23 Comparison of the implementation cost of the N-path filter with different PNP filters

<table>
<thead>
<tr>
<th></th>
<th>number of op-amps</th>
<th>number of switches</th>
<th>number of capacitors (critical valued in brackets)</th>
<th>number of clock phases</th>
</tr>
</thead>
<tbody>
<tr>
<td>simple N-path</td>
<td>N</td>
<td>N+3</td>
<td>N+1 (N+1)</td>
<td>N+2</td>
</tr>
<tr>
<td>Circulating</td>
<td>1</td>
<td>2N+6</td>
<td>N+2 (2)</td>
<td>N+1</td>
</tr>
<tr>
<td>Delay PNP [230]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RAM-type PNP</td>
<td>1</td>
<td>2N+6</td>
<td>N+2 (2)</td>
<td>2(N+1)</td>
</tr>
<tr>
<td>[230]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hybrid PNP</td>
<td>2</td>
<td>2N+8</td>
<td>N+2 (2)</td>
<td>2N</td>
</tr>
<tr>
<td>[230]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig.1.24 compares the capabilities and limitations of different single- and multi-path structures, with and without frequency translation. The kernel filter types considered are lowpass, highpass and bandpass, where the kernel filter type of a multi-path structure refers to the type of the path-filter. Each structure has its properties summarised in the corresponding box, with the approximate minimum RBW followed by a list of the most important factors setting that limit. As indicated, the approximate minimum RBW's for the NP/LP, NP/HP and SP/BP cases are taken from [118, table 1.2]. To briefly explain the summary information, it is first seen that a single-path filter based on a bandpass kernel (SP/BP) is limited from the point of view of narrow-band operation by considerations of dynamic range, sensitivity and capacitor spread (bottom-left box). Moving one box to the right, it is seen that this situation is alleviated by the use of an SPFT structure, although the achievable $Q$ for this solution is limited by the maximum $Q$-enhancement factor, which is related to the complexity of the AAF and AIF (as discussed above). The remaining entries in the table are all for multi-path implementations, the first of which is the simple system with a lowpass kernel, and suffers from in-band clock-feedthrough and mirror components. The NP/BP has no special limitations listed, though its path-filters clearly have the same constraints as the SP/BP structure, and the achievable RBW will depend on the maximum value of $N$ that it is practical to implement.
The remaining entries should be easily understood from the background material in the previous section, and so we shall not comment on each of them. Clearly, as one moves towards the bottom-right of the table the achievable filter $Q$, for given restrictions on in-band noise, dynamic range etc., tends to increase, while the size and complexity of the system increases also.

<table>
<thead>
<tr>
<th>Kernel filter</th>
<th>Filter System Type</th>
<th>SP</th>
<th>SPFT</th>
<th>NP</th>
<th>NPFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP lowpass</td>
<td>not applicable</td>
<td>not applicable</td>
<td>1% *</td>
<td>1/K %</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1. clock f.t. 2. IB mirrors</td>
<td>1. clock f.t 2. IB mirrors 3. AAF/AIF</td>
<td></td>
</tr>
<tr>
<td>HP highpass</td>
<td>not applicable</td>
<td>not applicable</td>
<td>1% *</td>
<td>1/K %</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1. IB mirrors</td>
<td>1. IB mirrors 2. AAF/AIF</td>
<td></td>
</tr>
<tr>
<td>BP bandpass</td>
<td>3% *</td>
<td>3/K %</td>
<td>3/N %</td>
<td>3/NK %</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1. dynamic range</td>
<td>1. AAF &amp; AIF</td>
<td></td>
<td>1. OB mirrors 2. AAF/AIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2. sensitivity</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3. cap. spread</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

KEY: IB = in-band, OB = out-of-band, K = Q-enhancement factor, * = [118, table 1.2.]

Fig.1.24 Comparison of properties of multi-rate filter architectures

Now, it has been pointed out that the reduction in dynamic range caused by in-band clock-feedthrough and mirrors is unacceptable for many applications, and so only those structures where these two phenomena are out of band will be considered further. This leaves only the SPFT and NPFT as realistic candidates for SC UNB filter designs, and of these two the NPFT filter structure clearly has greater potential for ultra-narrow-band operation. The main factors that will set the minimum, achievable relative bandwidth using this structure will be (i) the minimum bandwidth of the path filters, which is mainly limited by dynamic range and capacitor-spread considerations, (ii) mismatch between the path-filters, which leads to a distorted response and residual alias components (mirrors), and (iii) the size and complexity of the total filter system. The first and last of these limitations may be evaluated in a straightforward way for any given design specification, but assessment of mismatch between path-filters, caused by random errors in their components, is a long, computationally intensive task, made all the
more formidable by the complexity of the circuits required for an NPFT filter. However, a multi-path filter with highly-selective path filters is likely to be particularly vulnerable to these mismatch effects. An important advantage previously cited for the NPFT filters was that the accompanying AAF and AIF filters would not be required to have such a high selectivity as for an equivalent SPFT design, since the alias and image responses nearest to the passband are ideally cancelled by outphasing from the different paths. Clearly, this cancellation of mirror components will be affected by path-filter mismatch, and it is important to quantify this effect before designing the AAF and AIF filters.

Overall it can be seen that the mismatch phenomena will play an important role in determining the performance of an NPFT filter, although the acquisition of quantitative data to describe its effects is difficult using standard tools. The effect of statistical errors in the components of NP and NPFT filters is a topic that has received little attention in the open literature, and will therefore be explored in some detail in chapter 5. That chapter will describe the NPFT filter in detail, then present a statistical analysis of several NPFT filters using tools specially designed for that purpose. Conclusions drawn from the results of this work have inspired new circuit developments, and these will be described in chapter 6.

1.6 Research Objectives

In the area of GaAs SC circuits the main objective of this work has been to demonstrate new techniques for producing accurate high-speed circuits with available commercial technology. Interest has been focused on the problem of sensitivity to the low amplifier gains typically associated with such processes, and with optimising the circuit configuration to fully exploit the speed potential of the technology. A parallel objective, in a distinct but related piece of theoretical work, has been to predict the performance limits of current narrow-band SC architectures, to assess their feasibility for UNB filtering, and to produce design improvements where possible. The division of the work into these two separate areas came about both because of the personal interests of the author, and because of logistical considerations associated with the GaAs chip-design project.
1.7 Statement of originality

We consider that the following are the most significant results of the research presented in this thesis and are, to the best of our knowledge, original. We indicate below which of the results have been published to date. The work on narrowband filtering has also been instrumental in winning two SERC research grants.

In chapter 2: the treatment of integrator-pairs, as opposed to single integrators, is new and is an essential prerequisite to identifying efficient structures for second- and higher-order filters. A direct consequence of this was the discovery of the 'UCL87' integrator-pair: [159] Betts A.K., Taylor J.T., Haigh D.G., "Spike-free Biphase Switched-Capacitor Integrator-Pair with Low Sensitivity to Non-Ideal Op-Amp effects", Electronics Letters, 18th Feb 1988, pp.202-204.


In chapter 3: the analysis of a general dual-amplifier network is original, as are some of the special-case results derived from it. The amplifier characterisation technique is based on [145], but the improvements and extensions constitute an important step forward, and this is the first time that such a comprehensive method has been described: [158] Betts A K, Taylor J T, Haigh D G, "An Improved Characterisation Technique for Amplifiers used in High-Speed Switched-Capacitor Circuits", Proc European Conf on Circuit Theory & Design 1989, pp.309-314

In chapter 4: the balanced switch design is original, as is the single-stage GaAs amplifier. Also, the work reported is the first attempt to use the Plessey III-V process for analogue functions in the MHz range, and all modelling and circuit design work is to this extent original. The work was performed in collaboration with Dr D.G.Haigh, who made the major contribution to the amplifier design and also implemented the layout. The author contributed the work described in chapters 2 and 3, the new models described, and the key ideas in the switch design: [146] (above): [147] (above): [148] Haigh D G, Toumazou C, Betts A K, "Switched Capacitor Circuits &
Operational Amplifiers”, chapter 10 of [23]:


In chapter 6: the idea of the N*M-path filter structure is original. Also the principle of Same-Sample-Correction circuits is new, as are the single- and pseudo-N-path circuits derived from it: [149] (above)

Finally the principle of Last-Cycle-Correction circuits is original (although it has been developed independently by Baschirotto [150]), and the pseudo-N-path circuits derived from it are also new: [199] Betts A K, Taylor J T, "A Finite-Gain-Insensitive Circulating-Delay type Pseudo-N-Path Filter", to appear in Electronics Letters, Oct-1990.


2. SC BUILDING BLOCKS WITH LOW SENSITIVITY TO NON-IDEAL AMPLIFIER EFFECTS

2.1 Introduction

2.2 Integrator Pairs: past work and new developments
2.2.1 General
2.2.2 Review of published integrator-pairs
2.2.3 UCL 1987 integrator-pair (U87)

2.3 Detailed Study of Selected Integrator-Pairs
2.3.1 Analysis including parasitics
2.3.2 Filter design
2.3.3 Simulation results
2.3.4 Component cost

2.4 Further Advances
2.4.1 New symbolic analysis tools
2.4.2 Revised Nagaraj 1986 integrator-pair (N86r)
2.4.3 N86r properties explained
2.4.4 Filter simulation for N86r

2.5 Summary & Conclusions
2.1 Introduction

A switched-capacitor (SC) integrator-pair consists of an inverting and a non-inverting integrator which may be connected together to form a two-integrator-loop, an essential component in ladder and biquad filters. The particular difficulty in designing amplifiers with high gain and low input offset in GaAs technology means that SC building blocks with low sensitivity to these phenomena are of special interest. Several groups of researchers have been developing such circuits in the past few years [144,151-153], and the work now being reported set out initially to review available literature for building blocks that might be useful in a GaAs SC circuit. The survey led to the development of a novel integrator-pair, which was then subjected to detailed hand- and simulation-analyses. Further work is then described which benefitted from the production of a new tool - a symbolic signal-flow-graph analyser - greatly facilitating the symbolic analysis and, therefore, the fundamental understanding of the integrator pairs. New properties were discovered in known circuits allowing a further novel integrator-pair to be proposed. The latter circuit was used as the basis for an IC design, which is the subject of chapter 4.

2.2 Integrator Pairs: past work and new developments

2.2.1 General

Previously published integrator-pairs, illustrated in fig.2.1 to 2.5, are reviewed with the aim of identifying circuits with low sensitivity to amplifier gain. Part 'a' of the circuit diagrams (eg. fig.2.1.a) shows the integrators as they are usually presented in the literature, with single SC branches feeding into the inverting terminal of the amplifier. The figure also defines (i) a mnemonic for the integrator-pair (used for later reference), (ii) the date first proposed, and references, (iii) the delay for each integrator of the pair (in units of the clock period, T), (iv) the gain and phase error expressions. The latter expressions follow the notation used in [8]. Part 'b' of the diagram (eg. fig.2.1.b) shows the integrator-pair as a number of sub-circuits that could be used to build a ladder filter. This may be done by appropriate interconnection of the inverting- and non-inverting-integrator subcircuits with the branch subcircuit(s) shown. Thus, an estimate of the component-cost in a complex filter can be readily obtained if the number of integrators and branches in that filter is known, by using the table at the foot of this figure. The estimate obtained might be slightly less than the true component cost as the diagram does not show how zero-forming unswitched-capacitors or termination branches are realised. Another factor to be taken into account is the number
of clock signals required by each of the integrator-pairs when configured in a two-integrator-loop, as some require multi-phase clocks [144,154].

When considering the expressions for \( m(\omega) \) and \( \theta(\omega) \) note that the latter error is the most significant with respect to implementation of ladder and biquad filters [8]. It has been shown that for a bandpass SC ladder filter the effect of \( m(\omega) \) is equivalent to errors in the values of the components of the prototype LCR filter, and that this shifts the centre frequency of the filter response [8]. The effect of \( \theta(\omega) \) is equivalent to losses in the L and C elements or, equivalently, to leakage of charge from the integration capacitors, and this degrades the filter Q-factor [8]. While the former effect may be compensated by predistortion of the filter response, the effects of phase error cannot be reduced in this way. It has also been shown that a positive value of \( \theta(\omega) \) produces Q reduction, whereas a negative value results in peaking, and may therefore lead to stability problems [153]. We therefore wish to find integrators for which, given an amplifier gain of \( A \), the phase error is positive and significantly lower than for a conventional integrator. If the phase error is written in the form:

\[
\theta(\omega) = \frac{\theta_1(\omega)}{A} + \frac{\theta_2(\omega)}{A^2} + \frac{\theta_3(\omega)}{A^3} + \ldots
\]  

(2.1)

then it can easily be shown that for an integrator to have a phase error much lower than in a conventional circuit, then \( \theta_1(\omega) < 1 \) must apply, and we will refer to integrators satisfying this condition as FGI integrators. Although many FGI integrators require \( \omega T < 1 \) for \( \theta_1(\omega) < 1 \) to hold, an important subclass of FGI integrators will be shown to satisfy the condition \( \theta_1(\omega) = 0 \), for all signal frequencies. This property allows circuits to be designed with low ratios of clock-to-filtering frequencies, \( f_s/f_0 \), while maintaining low sensitivity to amplifier gain. It is especially important in high frequency filters, as it allows \( f_s \) to be minimised for a given \( f_0 \), and also in narrow-band filters, where a low \( f_s/f_0 \) ratio will tend to reduce a circuit's capacitor spread [118]. We therefore define two FGI properties, as follows:

- **FGI1 property**..............\( \theta_1(\omega) < 1 \) for \( \omega T < 1 \)

- **FGI2 property**..............\( \theta_1(\omega) = 0 \) for all \( \omega \)

where \( \theta(\omega) \) is given by (2.1).

The first of the circuits presented (fig.2.1) is the conventional integrator, while the remainder all possess either the FGI1 or FGI2 properties. In addition, all of the latter circuits are immune to amplifier input offset and have reduced sensitivity to low frequency amplifier noise, as these properties
are closely linked to the FGI phenomenon [152]. The purpose of this section is
to give a concise summary of the properties of each alternative integrator-
pair, and to assess their implementation cost and requirements. Note that
parasitic effects are not included in this comparison, although they are
quantified for selected integrator-pairs in sections 2.3 and 2.4.

2.2.2 Review of published integrator-pairs

**Conventional integrator-pair (M80):** These integrators were first
proposed for their low sensitivity to parasitic capacitances, which tends to zero
as the amplifier gain tends to infinity. They have since become the standard
integrator building-block for SC filters on account of their simplicity and
flexibility. For further discussion of these circuits the reader is referred to the
literature (eg. [2]).

**Temes 1984 integrator-pair (T84 : FGI2 type):** These building-blocks
were first proposed for their offset-compensation characteristics, and analysis
shows that they also possess the FGI2 property. They have a number of
drawbacks, however. The presence of a switch in the integrating capacitor
branch causes the amplifier to go open-loop for a part of the clock-cycle. In this
open-loop condition a small input offset voltage is amplified by the amplifier
open-loop gain and may cause the output to slew to one of the supply rails,
resulting in a large spike on the amplifier output at each clock transition. The
amplifier will also need extra time to recover from the unwanted slewing,
thus reducing the maximum frequency of operation of the filter, and/or the
accuracy of its response. Further serious difficulties arise when the simple
single-input integrators are split into blocks suitable for building a ladder
filter. The large number of capacitors and switches required is apparent from
fig.2.2.b. Also, an extra hold-capacitor and switch is needed to satisfy the
sampling requirements at the input of the non-inverting integrator.

**Nagaraj 1985 integrator-pair (N85 : FGI1 type) :** This building-block
was first proposed for its tolerance to finite amplifier gain, the effect of which
on the integrator response is reduced substantially by exploiting high
correlation between successive input samples to the integrators when \( \omega T << 1 \). Note the negative sign of the phase error; this tends to cause peaking in the
filter response [153]. Both inverting and non-inverting integrators are stray-
sensitive, since the the points 'X' and 'Y' in fig.2.3.a act as virtual-earths
when the amplifier gain is infinite. The implementation-related drawbacks
of this integrator-pair are similar to those of T84, above. As with T84, the
amplifier is allowed to go open-loop for a part of the clock cycle (in this case
the part of the cycle when neither the 'e' nor 'o' switches are on), and this
causes amplifier slewing. The large number of capacitors and switches needed
in a ladder filter implementation is an obvious drawback. Also, an extra
capacitor and pair of switches is needed in each inverting integrator input branch to satisfy the sampling conditions at that input.

**Haug 1985 integrator-pair (H85 : FGI1 type)**: This integrator-pair, which was first proposed for its tolerance to finite amplifier gain, is very similar to N85. However, it is not parasitic-insensitive, as the transfer function is affected by capacitances to ground from nodes X and Y in fig.2.4a. Neglecting parasitics, the effect of finite amplifier gain on the response is reduced substantially when $\omega T << 1$. Unlike N85, however, $\theta(\omega)$ is positive-signed, and so the problem of peaking in the filter response does not occur. As with the previous two integrator-pairs the amplifier is allowed to go open-loop for a part of the clock cycle, and this causes amplifier slewing. The large number of capacitors and switches needed in a ladder filter implementation is an obvious drawback. Also, an extra capacitor and pair of switches is needed in each inverting integrator input branch to satisfy the sampling conditions at that input.

**Nagaraj 1986 integrator-pair (N86 : FGI2 type)**: This building block was first proposed for its tolerance to the effects of finite amplifier gain. Both inverting and non-inverting integrators are stray-insensitive for infinite amplifier gain, the points 'X' and 'Y' in fig.2.5 acting as virtual earths, and the pair has the FGI2 property. The circuit may be implemented in a ladder filter using significantly fewer components than the FGI integrators so far presented, requiring only one extra switch and one extra unit-sized capacitor over the conventional integrator, M80. The major drawback with this circuit is the need for four clock signals in order to implement a two-integrator loop. It also has the problem of amplifier slewing during the part of the clock cycle where the amplifier feedback path is broken.

(a) Circuit : M80, Conventional integrators
Originated : April 1980
Delay: 0 inverting, 1 non-inverting
Refs: [3] (proposed), [8] (detailed analysis)

![Circuit Diagram](image)

\[ m(\omega) = \frac{1}{A} \left( 1 + \frac{C_1}{2C_2} \right) \]
\[ \theta(\omega) = \frac{C_1/C_2}{2 \Delta \tan(\omega T/2)} \]

(b) Subcircuits:

![Subcircuit Diagram](image)

Component cost:

<table>
<thead>
<tr>
<th>Inverting</th>
<th>Non-inv.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Caps. in integrator</td>
<td>C2</td>
</tr>
<tr>
<td>Caps. in i/p branch</td>
<td>4</td>
</tr>
<tr>
<td>Switches in integrator</td>
<td>1</td>
</tr>
<tr>
<td>Clock phases in TIL</td>
<td>2</td>
</tr>
</tbody>
</table>

Fig.2.1 M80 data
(a) Circuit: T84, Temes 84 integrators
   Originated: June 84
   Delays: 0 inverting, 1 non-inverting
   Refs: [151] (proposed), [153] (some analysis)

   ![Subcircuits:](image)

   $$m(\omega) = -\frac{1}{A} \frac{1 + C_1}{C_2}$$
   $$\theta(\omega) = \frac{C_1}{A} \sin(\omega T)$$

(b) Subcircuits:
   ![Subcircuits:](image)

   Component cost:
   - Inverting: $C_2$, $2C_1$
   - Non-inverting: $C_2$, $6C_1$
   - Clock phases in TIL: 2

   Fig.2.2 T84 data

---

(a) Circuit: N85, Nagaraj 85 integrators
   Originated: July 85
   Delays: 0 inverting, 1/2 non-inverting
   Refs: [152] (proposed), [153] (some analysis)

   ![Subcircuits:](image)

   $$m(\omega) = -\frac{1}{A} \left(1 + \frac{C_1}{C_2} - \cos(\omega T)\right)$$
   $$\theta(\omega) = -\frac{C_1}{A} \sin(\omega T)$$

(b) Subcircuits:
   ![Subcircuits:](image)

   Component cost:
   - Inverting: $C_2 + 2C_1$, $4C_1$
   - Non-inverting: $C_2 + 2C_1$, $C_1$
   - Clock phases in TIL: 2

   note: $C_3 = C_4 = Cu$, the unit capacitor

   Fig.2.3 N85 data
(a) Circuit: H85, Haug 85 integrators
Originated: Nov 85
Delays: 0 inverting, 1/2 non-inverting
Refs: [153] (proposed)

\[ m(\omega) = \frac{1}{A} \left( 1 + \frac{C_1}{C_2} \right) \]
\[ \theta(\omega) = \frac{C_1 / C_2}{A^2 \tan(\omega T / 2)} \text{ for } \omega T << 1 \]

(b) Subcircuits:

inverting

non-inv.

Component cost:

<table>
<thead>
<tr>
<th></th>
<th>Inverting</th>
<th>Non-inv.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Caps. in integrator</td>
<td>C2+Cu</td>
<td>C2+Cu</td>
</tr>
<tr>
<td>Caps. in i/p branch</td>
<td>4C1</td>
<td>C1</td>
</tr>
<tr>
<td>Switches in integrator</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>Switches in i/p branch</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>Clock phases in TIL.</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

note: C3 can be set to the unit capacitor, Cu

Fig.2.4 H85 data

(a) Circuit: N86, Nagaraj 86 integrators
Originated: Oct 86
Delays: 1/2 inverting, 1 non-inverting
Refs: [144] (proposed)

\[ m(\omega) = \frac{1}{A} \left( 1 + \frac{C_1}{C_2} \right) \]
\[ \theta(\omega) = \frac{C_1 / C_2}{2 A^2 \tan(\omega T / 2)} \]

(b) Subcircuits:

inverting

non-inv.

branch into either integrator

Component cost:

<table>
<thead>
<tr>
<th></th>
<th>Inverting</th>
<th>Non-inv.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Caps. in integrator</td>
<td>C2+Cu</td>
<td>C2+Cu</td>
</tr>
<tr>
<td>Caps. in i/p branch</td>
<td>C1</td>
<td>C1</td>
</tr>
<tr>
<td>Switches in integrator</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Switches in i/p branch</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Clock phases in TIL.</td>
<td>4</td>
<td>2</td>
</tr>
</tbody>
</table>

note: C3 can be set to the unit capacitor, Cu

Fig.2.5 N86 data
This is a novel integrator-pair made-up from the T84 inverting and the N86 non-inverting integrators [159]. As with the these two integrators, this building-block is parasitic-insensitive for infinite amplifier gain, the phase error is inversely dependent on $A^2$ and the desirable circuit properties do not depend on the condition $\omega T<<1$ being met (i.e. the pair has the FGI2 property). The component cost is approximately the same as that of N86, but the new pair has the advantage of only requiring a two-phase clock in order to implement a two-integrator-loop. To overcome the amplifier slewing problem, already explained in the context of the N86 and T84 integrators, we use the 'Matsumoto' modification, as follows. Matsumoto has observed that a continuous feedback path can be established for certain SC building blocks, without affecting their transfer function, by the addition of an extra capacitor between two nodes, provided those nodes are driven to defined voltages in all clock phases [155]. These capacitors are labelled $C_m$ in fig.2.6. During the guard-intervals between the e- and o-clock phases the continuous feedback path of capacitors, which is completed by $C_m$, simply holds the amplifier at its previous output voltage. Note that this modification cannot be made for all of the FGI integrators. For the inverting integrator of N85, for example, it may appear possible to connect $C_m$ between the amplifier output and node 'Z' of fig.2.3.a. When N85 is split into sub-circuits suitable for implementing a ladder filter, however (fig.2.3.b), node 'Z' is no longer voltage-driven during the odd phase because of the sample-and-hold circuit that has been introduced. It would therefore cause an error in the charge held in the input branch.

From the foregoing discussion this new integrator-pair appears more effective and economical than any of those considered so far. The drawbacks described for the T84, N85 and H85 integrator-pairs mean that they are only of historical interest, while the N86 pair has the disadvantage of requiring four clock signals. However, both the N86 and U87 pairs have excellent phase error expressions and, considering their relative simplicity and suitability to the Matsumoto modification, they both seem likely to be of practical use. These integrator-pairs have therefore been selected for a more detailed study, which is reported in the next section.
2.3 Detailed Study of Selected Integrator-Pairs

2.3.1 Analysis including parasitics

Method: Following [8] the transfer function of each integrator was written in the form:

\[ H_d(\omega) = (1 + m(\omega))H_I(\omega) e^{j\theta(\omega)} \]

\[ = \frac{H_I(\omega)}{1 - m(\omega) - j\theta(\omega)} \]  

(2.2)

where \( H_I(\omega) \) is the ideal transfer function of the integrator. Each circuit was examined to determine which of its nodes were 'parasitic-affected'; these were taken to be the nodes which were not always connected to either a voltage source or to ground. The circuits were then redrawn with extra capacitors to ground from each of these parasitic-affected nodes and analysed as shown in the next three sub-sections. The complexity of the resulting expressions was reduced to an acceptable level by ignoring inter-parasitic effects (i.e. neglecting any terms that involved the product of two parasitics) and by neglecting terms with factors of \( 1/A^2 \) (resp. \( 1/A^3 \)) in the expressions for \( m(\omega) \) (resp. \( \theta(\omega) \)).
All of the expressions to be presented in this section have been derived by manual algebraic manipulation, though they were later checked using a computer-based symbolic analysis program. Only the key results are presented here.

Conventional integrators: The circuit analysed is shown in fig.2.7 and gives:

\[
m(\omega) = -\frac{1}{A} \left(1 + \frac{C_1}{2C_2} + \frac{C_3}{C_2} + \frac{C_4}{2C_2}\right) \tag{2.3}
\]

\[
\theta(\omega) = \frac{(C_1+C_4)/C_2}{2A \tan(\omega T/2)} \tag{2.4}
\]

where \(C_3\) and \(C_4\) are parasitics. Note that these expressions apply equally to the inverting and non-inverting integrators, and that as \(A\) tends to infinity \(m(\omega)\) and \(\theta(\omega)\) tend to zero, as one would expect for a parasitic-insensitive circuit.

N86 integrators: The circuit analysed is shown in fig.2.8 and gives:

\[
m(\omega) = -\frac{1}{A} \left(1 + \frac{C_1}{C_2} \left(1 + \frac{C_5}{C_3}\right) + \frac{C_3}{C_2} + \frac{C_4}{C_2} \left(1 + \frac{C_5}{C_3}\right) + \frac{2C_5}{C_2} + \frac{C_6}{C_2}\right) \tag{2.5}
\]
\[
\theta(\omega) = \frac{1}{2A^2 \tan(\omega T/2)} \left( \frac{C_1}{C_2} + \frac{C_4}{C_2} + \frac{C_5}{C_2} \left( \frac{1 + \frac{C_1}{C_3}}{C_{5}C_2} + \frac{C_6}{C_2} \right) \right)
\]  

(2.6)

where \( C_4, C_5 \) and \( C_6 \) are parasitic capacitances. Note that these equations apply equally to the inverting and non-inverting integrators and that the N86 integrators have the basic parasitic-insensitive property, since \( m(\omega) \) and \( \theta(\omega) \) tend to zero as \( A \) tends to infinity. For finite gains, a comparison of (2.3) and (2.5) shows the gain error to be larger than, but of the same order as, that for a conventional integrator. However, inspection of the expression for \( \theta(\omega) \) shows that the desirable FGI2 property of the N86 integrators, established in section 2.2, is maintained even when parasitic capacitances are included in the analysis. This explains Nagaraj's observation in the original publication of the N86 integrator that parasitics had little influence on performance [144]. The physical mechanisms underlying this phenomenon will be investigated in more detail in section 2.4. This analysis has been done for the circuit as originally specified by Nagaraj in [144], and this only considers the transfer function to the output in the e-phase. Section 2.4 will also consider the transfer function when the output is sampled "illegally" in the o-phase.

<U87 integrators>: The non-inverting U87 integrator is identical to the non-inverting N86 integrator, and so the preceding comments apply. The inverting integrator for the integrator-pair is taken from the T84 integrator-pair, and the circuit to be analysed is shown in fig.2.9. The result is:

\[
m(\omega) = -\frac{1}{A} \left( 1 + \frac{C_1}{C_2} + \frac{C_4}{C_2} \frac{C_6}{C_1} \cos(\omega T) \right)
\]  

(2.7)

\[
\theta(\omega) = -\frac{1}{A} \frac{C_6}{C_1} \sin(\omega T) + \frac{1}{2A^2 \tan(\omega T/2)}\left( \frac{C_1}{C_2} + \frac{C_4}{C_2} + \frac{C_5}{C_2 + C_5} + \frac{C_6}{C_2} \right)
\]  

(2.8)
where $C_4$, $C_5$ and $C_6$ are parasitics. The expressions show that this integrator has the basic parasitic-insensitivity property, since $m(\omega)$ and $\theta(\omega)$ tend to zero as $A$ tends to infinity. For finite amplifier gain a comparison of (2.3) and (2.7) shows the gain error to be larger than, but of the same order as, that for a conventional integrator. Examining the phase error it is seen that $C_6$ contributes a negative factor (which leads to peaking in the filter response [4]) and that its magnitude depends on a factor $1/A$, rather than $1/A^2$. It is also multiplied by $\sin(\omega T)$, and so its influence is substantially reduced for $\omega T<<1$, but nevertheless it would be desirable to minimise $C_6$ in a real implementation. The contributions of all the other parasitics to $\theta(\omega)$ are multiplied by $1/A^2$, and so their contribution to the phase error will be much lower than for a conventional integrator.

2.3.2 Filter Design

The 'test-bed' filter used for this work has already been introduced, in chapter 1, where the synthesis of a conventional SC filter from an LCR ladder prototype was briefly explained. This section will describe the differences between the conventional SC filter and those using the N86 and U87 integrator-pairs.

**N86 Design**: The filter design using N86 integrators is shown in fig.2.10 and differs from that using conventional integrators in the following respects.

As stated earlier, the circuit of fig.2.5.a cannot be used directly to implement a two-integrator-loop because the total delay produced in the inverting plus non-inverting integrators numerator functions is $z^{-3/2}$. The master clock period is therefore divided into three, instead of two, phases and we modify the clocking scheme as follows. The inverting integrator is virtually unaltered, as shown by fig.2.11.b. This is the same as in fig.2.5.a, but with the odd phase replaced by phase 1 and the even phase replaced by 2. The non-inverting integrator must now be configured to sample input during phase 2 and output the next updated voltage during the following phase 1. In the circuit of fig.2.5.a the non-inverting integrator uses the even phase to both sample a new input and give an updated output voltage, while the odd phase is a 'charge redistribution' phase during which the circuit can be thought of as doing internal computations. In order that the circuit produces the desired delay the 'sample input' and 'sample output' phases are split, (corresponding to phases 2 and 1 respectively) and phase 3 is used for 'charge redistribution'. The resulting circuit is shown in fig.2.11.c; note that two of the switches have to be on in both phases one and two, and so a fourth clock signal is required in the implementation. A comparison of circuit operation with that of fig.2.5.a is given in fig.2.11.d, showing how the same basic operations are
carried out over three clock phases, rather than just two.

Fig. 2.10 6th-order SC elliptic bandpass filter using Nagaraj (N86) integrator-pairs

The next difference from the conventional design concerns the unswitched capacitors (k4b, k2d, k6d, and k4c). These connect inverting integrator outputs to the virtual earths of other inverting integrators. In a
conventional design the 'sample-input', 'charge-redistribution' and updated-voltage output' operations are all done during a single phase and the amplifier outputs do not change during the other phase. Consequently, the zero-forming capacitors may be permanently connected without affecting circuit operation. For the N86 inverting integrators, however, where the amplifier voltages change during both phases 1 and 2, the effect of having a zero-forming capacitor connected in phase 1 is to alter the charge stored on the capacitor at the input terminal. In order not to upset correct circuit operation it is therefore necessary to place a switch in series with each zero-forming capacitor so that it is only connected during phase 2, when the inverting integrator outputs are sampled. The terminations are implemented in exactly the same way as for the conventional integrator, which is not an ideal method, as the gain and phase errors associated with these branches will be given by the same expressions as for the conventional integrators (ie. they will not possess the finite-gain insensitivity property that is achieved by the other switched-capacitor branches in the circuit). An alternative uses a Parasitic-Compensated Toggle Switched-Capacitor [160], but requires four times the capacitance and several extra switches. Finally, six 'Matsumoto' capacitors were added to the circuit to prevent the amplifier slewing problem, as described in section 2.8.

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Fig.2.11 Four-phase N86 integrator-pair (a) clocking scheme, (b) inverting integrator, (c) non-inv. integrator, (d) comparison with 2-phase version
U87 Design: The filter design using the U87 integrator-pair is shown in fig. 2.12 and differs from the conventional one in fewer respects than for N86. The number of clock phases is unaltered, the inverting and non-inverting integrator transfer functions are identical to those for M80, and terminations can be realised using the same finite-gain insensitive branches as are connected to all the other switched inputs. It is, however, necessary, to have switches in series with the zero-forming capacitors, as there are charge transfers taking place in the even clock phase which would be disturbed by their presence, which is only needed for the inverting integrator output 'calculation' in the odd phase. Finally, as for the N86 design, 'Matsumoto' capacitors are added to overcome the amplifier slewing problem.

Fig. 2.12 6th-order SC elliptic bandpass filter using UCL 1987 (U87) integrator-pairs
2.3.3 Simulation results

Simulations were performed on the conventional, N86 and U87 filters for clock ratios $f_s/f_0 = 25$ and $f_s/f_0 = 10$, both with and without parasitics. The main results are presented in figs.2.13 to 2.17.

**Parasitics excluded:** Fig.2.13 compares the bandpass filter responses using conventional and the U87 integrator-pairs for $f_s/f_0 = 25$, using an amplifier gain of 100. On this scale the same graphs for the N86 integrator-pair, and for the case $f_s/f_0 = 10$, are not significantly different. The plots show that, while the conventional filter has a completely misshapen passband response and has lost several dB's of gain, the U87 filter is virtually unaltered in these respects. Both versions of the filter have suffered a shift in centre frequency towards DC, and these shifts are approximately equal. This reflects the similarity in the values of $m(\omega)$ for these two cases.

Figs.2.14a and 2.15a (2.14b and 2.15b) compare the detailed filter response in the passband using the conventional and N86 (U87) integrator-pairs for $f_s/f_0 = 25$ and $f_s/f_0 = 10$ respectively. In each case the FGI integrator filter response for an amplifier gain of 100 is being compared with a conventional filter response with amplifier gain 1000. Also included in the plots are the ideal responses and the response of the conventional filter using amplifiers with gains of 100, while the responses for the FGI integrators using amplifiers with gains of 1000 do not differ perceptably from the ideal responses. Comparing the performances of the N86 and U87 filters they are seen to be very similar, although the N86 filter has a larger peak-gain error. This is attributed to the way in which the termination branches were implemented, which made them more sensitive to the amplifier gain than the other branches of the filter (this deduction is confirmed by the results in sub-section 2.4.4).

**Parasitics included:** Figs 2.16 to 2.17 repeat the same sequence of plots as 2.14 to 2.15, only with parasitic capacitances included. To simulate what was felt to be a worst-case, two parasitic capacitors to ground were introduced for every original capacitor in the circuit. Each parasitic capacitor was a third the size of its originator, with one connected to the 'top' plate and the other to the 'bottom' plate. Additionally, a unit-sized capacitance was connected between every amplifier input and ground. This sequence of figures is significantly different from its 'parasitic excluded' counterpart. Comparing figs 2.16.a and 2.16.b (ie. the $f_s/f_0 = 25$ plots) we see that the N86 filter has a larger centre-frequency shift and peak-gain error than the U87 filter. The latter shows slight peaking, but has an otherwise excellent response, giving a similar deviation from the ideal as the conventional filter (with ten times the amplifier gain). The same comments apply to 2.17 ($f_s/f_0 = 10$), although the peaking in the U87 filter is now quite marked. This is attributed to the
negative phase error from the $C_6$ parasitic (see (2.8)), which becomes more significant as $f_s/f_0$ is decreased. The generally poorer response of the N86 filter is again attributed to the way in which the terminations were implemented (this deduction is confirmed by the results in sub-section 2.4.4).

Fig. 2.13 Bandpass filter response, U87, $f_s/f_0=25$, no parasitics
Fig. 2.14a Filter passband details, $f_0/f_s = 25$. No parasitics, N86
Fig. 2.14b Filter passband details, $f_s/f_0=25$. no parasitics, U87
Fig. 2.15a Filter passband detail, $f_s/f_0=10$, no parasitics, N86
Fig. 2.15b  Filter passband detail, $f_s/f_0 = 10$, no parasitics, U87
Fig. 2.16a Filter passband detail, $f_s/f_0=25$, with parasitics, N86
Fig. 2.16b Filter passband detail, $f_0/f_o=25$, with parasitics, U87
Fig. 2.17a Filter passband detail, $f_s/f_0=10$, with parasitics, N86
Fig. 2.17b Filter passband detail, $f_{\text{f}}/f_{\text{p}}=10$, with parasitics, U87

<table>
<thead>
<tr>
<th>fc/fp</th>
<th>capacitor spread all</th>
<th>total capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>143</td>
<td>669, 681, 704</td>
</tr>
<tr>
<td>25</td>
<td>36</td>
<td>210, 222, 246</td>
</tr>
<tr>
<td>10</td>
<td>14</td>
<td>124, 136, 165</td>
</tr>
</tbody>
</table>

switches: 24, 40, 42

clock phases: 2, 4, 2

Fig. 2.18 Filter implementation-cost comparison
2.3.4 Component cost

Fig. 2.18 gives a summary of component cost for the bandpass filter for different values of $f_s/f_0$. The number of switches for the N86 and U87 filters are 40 and 42 respectively, compared to 24 for a conventional filter. The relative increase in total capacitance increases as the capacitance spread decreases, since the extra unit-valued capacitors in the N86 and U87 filters then become more significant. The worst case increase shown is for the filter at $f_s/f_0 = 10$, and is about 33%. The most important advantage of the UCL 87 integrator-pair over the Nagaraj pair is that it is implemented using a two-phase clock. The N86 filter requires four different clock signals, which implies extra clock-generating circuitry and bus lines, as well as a lower maximum frequency of operation.

2.4 Further Advances

2.4.1 New symbolic analysis tools

The work described in the preceding section relied heavily on manual algebraic manipulation of large expressions. It became clear that a computer program to aid the symbolic analysis of these types of circuits would be valuable. At the time, only one such tool was known of [161], but that was not available to us. General purpose computer programs were also on the market [162,163], but these were not specifically orientated to circuit design problems, and most of them were quite expensive. It was therefore decided to write a program (called MASON) that took the signal-flow-graph (SFG) definition of a system as input, and calculated its transfer function using Mason's rule [164]. A further program (PS) was written to aid the simplification of the transfer functions produced, as MASON was capable of producing very complex expressions. The SFG input format was a particular strength of the programs since (i) an SFG can be used to describe a wide variety of systems (the programs have also been extensively used for the work described in the next chapter), and (ii) the exercise of translating a circuit into an SFG was frequently quite instructive in itself. MASON and PS are described in more detail in appendix 1, where an example of their use is given.

Having produced the MASON and PS tools, they were first used to confirm the analytical formulae produced in the previous section. It was then possible to examine properties of the circuits not amenable to hand analysis - such as second order effects of parasitics - and to rapidly evaluate the transfer functions of new and modified circuits. The most significant result of these exploratory analyses concerns the N86 circuit, and this section will be used for a detailed re-evaluation of this circuit. It will be shown that the circuit has an
important property that was not previously appreciated, and which allows it to be economically formed into two-integrator loops, with bi-phase clocking, while maintaining the FGI2 property.

2.4.2 Revised Nagaraj 1986 integrator-pair (N86r)

A modified version of the integrator-pair of fig.2.5 is presented in fig.2.19. The clocking arrangement of the inverting integrator has been modified to give zero delay from input to output, so that it can now be directly connected to the non-inverting integrator to form a two-integrator-loop, without any additional circuitry. Matsumoto capacitors have also been added. The integrator is drawn for analysis in fig.2.20, where it should be noted that the positive amplifier input terminal has been designated as an independent input, $V_n$. 

![Fig.2.19 N86r data](image)

![Fig.2.20 N86r integrator with parasitics](image)
Using charge conservation for both the clock phases, a number of equations may be written to describe the operation of the integrator, then drawn as the SFG shown in fig. 2.21. Note that both the o- and e-phase outputs are represented, and so the SFG may be used to compare the transfer functions for sampling in the "legal" e-phase and the "illegal" o-phase. Also, since the amplifier's positive input terminal is separately represented it is easy to explore the transfer function to the output of any signal that can be referenced to this input. An obvious example of this would be amplifier noise, while another is to see the effects of amplifier gain. This is achieved by the dashed branch in the figure, which feeds back a signal $-V_0^x/A$ from the output to $V_{n}^x$, where $x$ represents either the e- or o-phase signal. Assuming that any terms with a factor of $1/A^3$ may be neglected, then the e- and o-phase transfer functions are found to be:

$$H_e(z) = \frac{N_e(z)}{D(z)}$$

$$H_o(z) = \frac{N_o(z)}{D(z)}$$

with:

$$D(z) = (1 - z^{-1})(1 + \frac{d_1}{A} + \frac{d_2}{A^2}) + \frac{d_3}{A^2}$$

$$N_e(z) = z^{-1/2} \frac{C_1}{C_2} \left(1 + \frac{g(z)}{A}\right)$$

$$N_o(z) = z^{-1} \frac{C_1}{C_2} \left(1 + \frac{g(z)}{A}\right)$$

where $d_1, d_2$ and $d_3$ are real numbers and, when terms that include the product of two or more parasitics are neglected:
Note that \( g(z) \) becomes real for \( C_3 = C_2 \) and zero parasitics. Now, by comparing (2.9) and (2.10) with (2.2) it can be shown that:

\[
m_e(\omega) = -\frac{d_1 - n_1}{A}
\]

(2.16)

\[
\theta_e(\omega) = -\text{Im} \left( \frac{1}{A^2 (1 - z^{-1})} \right)
\]

(2.17)

\[
m_d(\omega) = -\text{Re} \left( \frac{d_1 - g(z)}{A} \right)
\]

(2.18)

\[
\theta_d(\omega) = -\text{Im} \left( \frac{-g(z) + \frac{1}{A^2} \left[ -d_1 - g(z) + \frac{d_3}{1 - z^{-1}} \right] \right)
\]

(2.19)

It is found that:

\[
d_1 = 2 + \frac{C_1 + C_3}{C_2} + \frac{C_4}{2C_2} + \frac{2C_5}{C_2} + \frac{2C_6}{C_2} + \frac{C_1 C_5}{2C_3} + \frac{C_5}{C_3}
\]

(2.20)

\[
d_3 = \frac{C_1}{C_2} + \frac{C_4}{C_2} + \frac{C_1 C_5}{2C_2 C_3} + \frac{C_1 C_6}{C_2 C_3} + \frac{C_5}{C_2}
\]

(2.21)

so using (2.14) to (2.19) with (2.20) and (2.21) gives complete expressions for the gain and phase error of the integrator for sampling in both output phases. It can be verified that the results for \( m_e(\omega) \) and \( \theta_e(\omega) \) are in agreement with the earlier hand calculations (eqns. (2.5) & (2.6), and [159]) and that the 'parasitic-free' expressions are:

\[
m_e(\omega) = \frac{-1}{A} \left( 1 + \frac{C_1}{C_2} + \frac{C_3}{C_2} \right)
\]

(2.22)

\[
\theta_e(\omega) = \frac{C_1 / C_2}{2A^2 \tan (\omega T / 2)}
\]

(2.23)

\[
m_d(\omega) = \frac{-1}{A} \left( 1 + \frac{C_1}{C_2} - \cos(\omega T) \left( 1 - \frac{C_3}{C_2} \right) \right)
\]

(2.24)
\[
\theta_0(\omega) = -\frac{\sin(\omega T)}{A} \left(1 - \frac{C_3}{C_2}\right) + \frac{C_1/C_2}{2A^2\tan(\omega T / 2)}
\] (2.25)

The latter expression shows that the circuit actually has the \text{FGI2} property when sampled during the "illegal" o-phase, provided \(C_3=C_2\). Furthermore, if parasitics are included while retaining \(C_3=C_2\) (2.25) becomes:

\[
\theta_0(\omega) = \frac{C_6 \sin(\omega T)}{C_2 A} + \frac{1}{2A^2\tan(\omega T / 2)} \left(\frac{C_1}{C_2} + \frac{C_4}{C_2} + \frac{C_1C_5}{C_2C_3} + \frac{C_1C_6}{C_2C_2}\right)
\] (2.26)

showing that the very low sensitivity of the phase to finite amplifier gain is retained for \(\omega T<<1\), even in the presence of parasitics for sampling in the o-phase also.

The properties predicted by the foregoing expressions were verified by comparison with simulation results using SWITCAP on the inverting M80 and N86r integrators. The gain and phase responses of the two integrators when the output was sampled in the o- and e-phases with amplifier gains set to 100 were compared to (ideal) responses where amplifier gain was effectively infinite (1e9), and errors were computed from:

\[
m(\omega) = 1 - \frac{G_{1e}(\omega)}{G_{1e2}(\omega)}
\] (2.27)

\[
\theta(\omega) = \phi_{1e}(\omega) - \phi_{1e2}(\omega)
\] (2.28)

where \(G_A(\omega)\) and \(\phi_A(\omega)\) are gain and phase values for amplifier gain \(A\). For both integrators the \(C_1\) and \(C_2\) capacitors were set to unity and results were obtained for the N86 integrator with \(C_3=1, C_3 =100\) and \(C_3 =0.01\). The phase errors for e-phase output sampling are compared in fig.2.22. It can be seen that the phase error of the conventional integrator has the expected tangential characteristic, while that of the N86 integrator is much smaller than for its conventional counterpart for all values of \(C_3\) and at all frequencies. It can readily be verified that the absolute error values on the graph are in close agreement with the predictions of (2.23).
Corresponding results for output sampling during the α-phase are shown in fig.2.23, where the phase errors for the conventional integrator and,
importantly, the N86 integrator with \( C_3 = C_2 = 1 \) are very similar to those for e-phase output sampling. This confirms the prediction of (2.25) that the N86 integrator sampled in either output phase has the FGI2 property when \( C_3 = C_2 \). When this condition is not met, however, the phase error in the o-phase may be significant. For \( C_3 = 100 \) (2.25) shows that the \( C_3 / C_2 \) term dominates the phase error, which becomes too large to be shown on fig.2.23. For \( C_3 = 0.01 \) the phase error approximates to:

\[
\theta(\omega) = -\frac{1}{A} \sin(\omega T / 2)
\]  

(2.29)

and this expression is confirmed by fig.2.23, where a positive sine function can be clearly identified. Again, the absolute values predicted by (2.25) are in good agreement with the simulation.

Fig.2.24 shows the gain error for the integrators with output sampled in the e-phase. Again, good agreement with predicted values is found, and it is seen that the N86 gain error for \( C_3 = 0.01 \) is less than for \( C_3 = C_2 \). Since it has already been seen that \( C_3 \) has little effect on the integrator's phase error when the output is sampled in this phase, some advantage may result from \( C_3 \ll C_2 \) for integrators with "legal" sampling. Finally, fig.2.25 shows the gain errors for output sampling in the o-phase. The gain error for the conventional integrator is unchanged compared to the e-phase, as expected, while that for N86 agrees with the predictions of (2.24). Errors for \( C_3 = 100 \) are again too large to be shown.

![Fig.2.24 Gain errors - e-phase](image-url)
2.4.3 N86r properties explained

The foregoing section has revealed the following interesting and useful properties in the N86r pair. With reference to fig. 2.20:

(i) When sampled in the e-phase the circuit always has the FGI2 property.

(ii) The parasitic-free circuit sampled in the o-phase possesses the FGI2 property when $C_3 = C_2$.

(iii) The circuit sampled in the o-phase, when parasitics are included and $C_3 \neq C_2$, has the FGI1 property (i.e. low sensitivity to amplifier gain when $\omega T \ll 1$).

Before using these circuits in an IC design it is very important to gain an qualitative understanding of their operation. We therefore examine the N86r integrators of fig. 2.20 in more detail to see what physical mechanisms account for their behaviour.
(i). e-phase FGI property: The parasitic-free transfer function for sampling in the e-phase will first be derived in a way that highlights the charge-sharing operations occurring on each clock phase. Four consecutive phases, e1, o1, e2 and o2 will be used and the change in charge on a capacitor $C_x$ from phase $y$ to phase $z$ will be written as:

$$\Delta^{y}q_{x}$$

By definition:

$$\Delta^{e1e2}q_{2} = \Delta^{e1o1}q_{2} + \Delta^{o1e2}q_{2}$$ (2.31)

Connecting $C_2$ to node B for the o-phase causes it to share charge with $C_1$ and $C_3$:

$$\Delta^{e1o1}q_{2} = -\Delta^{e1o1}q_{1} - \Delta^{e1o1}q_{3}$$ (2.32)

but the right-hand plate of $C_3$ is isolated during the o-phase, so:

$$\Delta^{e1o1}q_{3} = 0$$ (2.33)

hence:

$$\Delta^{e1o1}q_{2} = -\Delta^{e1o1}q_{1}$$ (2.34)

In the next phase, e2, charge is redistributed between $C_2$ and $C_3$ via the amplifier input node:

$$\Delta^{o1e2}q_{2} = \Delta^{o1e2}q_{3}$$ (2.35)

and using (2.33):

$$\Delta^{o1e2}q_{2} = \Delta^{e1e2}q_{3}$$ (2.36)

and substituting (2.34) and (2.36) into (2.31) gives:

$$\Delta^{e1e2}q_{2} = -\Delta^{e1o1}q_{1} + \Delta^{e1e2}q_{3}$$ (2.37)

This is readily converted to the z-domain equation:

$$C_2(1-z^{-1})V_{o}^e\left(1+\frac{1}{A}\right) = -C_1 z^{-1/2}(V_{i}^o - V_{B}^o) - \frac{C_3}{A}(1-z^{-1})V_{o}^e$$ (2.38)

which can be rewritten:

$$V_{o}^e = -\frac{C_1 z^{-1/2}(V_{i}^o - V_{B}^o)}{C_2(1-z^{-1})\left(1+\frac{1}{A}\left(1+\frac{C_3}{C_2}\right)\right)}$$ (2.39)
where $V_{x}^{y}$ is the voltage at node $x$ in phase $y$. This equation highlights the crucial role of $V_{B}^{0}$ in determining the phase error in the circuit. By comparing (2.39) with the transfer function of an ideal integrator it is seen that the integrator has zero phase error only when:

$$V_{B}^{0} = K.V_{i}^{0}$$

(2.40)

where $K$ is a constant. $V_{B}^{0}$ is found by expanding (2.33), which gives:

$$V_{B}^{0} = \frac{1}{A}(V_{o}^{0}z^{-1/2} - V_{o}^{0})$$

(2.41)

$V_{o}^{0}$ is calculated from charge-redistribution at B during phase $o$ which, expanding (2.34), is:

$$V_{o}^{0} = (1 + \frac{1}{A})V_{o}^{0}z^{-1/2} - \frac{C_{1}}{C_{2}}(V_{i}^{0} - V_{B}^{0}) + V_{B}^{0}$$

(2.42)

Substituting this into (2.41) gives:

$$V_{B}^{0} = \frac{1}{A}(V_{o}^{0}z^{-1/2} - (1 + \frac{1}{A})V_{o}^{0}z^{-1/2} + \frac{C_{1}}{C_{2}}(V_{i}^{0} - V_{B}^{0}) - V_{B}^{0})$$

(2.43)

Now, the two $V_{o}^{0}z^{-1/2}$ terms cancel, and the expression may then be simplified, using $1/A^{2}<<1$, to give:

$$V_{B}^{0} = \frac{1}{A} \frac{C_{1}}{C_{2}}V_{i}^{0}$$

(2.44)

This satisfies the criteria for zero phase error in the e-sampled transfer function, given by (2.40). The cancellation that resulted in (2.44) can be traced back to the voltages sampled on $C_{2}$ and $C_{3}$ during the e-phase. The error voltage on $C_{2}$ in the e-phase, $V_{o}^{e}/A$, is stored by $C_{3}$ then cancelled during the following o-phase by charge-transfer between $C_{2}$ and $C_{3}$ through node B. Hence, although some error is sampled at the output during phase e, the error in the stored charge is corrected before the start of the following e-phase (i.e. errors are not remembered from one clock-cycle to the next). The net integrator loss from cycle to cycle is therefore zero to first order in $1/A$ and, since integrator loss and phase error go hand-in-hand, this correction mechanism explains the low phase error of the N86 integrator. It also follows that the error sampled at the output during the e-phase contributes to the gain error term only. Note that the cancellation is between voltages generated during a single clock phase, and so correlation between voltages in successive phases is not needed. This explains why the circuit retains its finite gain.
insensitivity property for all signal frequencies.

(ii). \(\alpha\)-phase FGI2 property (when \(C_2=C_3\)) : To investigate the transfer function to the \(\alpha\)-phase output we start with:

\[
\Delta^{\alpha\alpha_2}q_2 = \Delta^{\alpha\alpha_2}q_2 + \Delta^{\alpha\alpha_2}q_2
\]  
(2.45)

then, following similar working to before:

\[
\Delta^{\alpha\alpha_2}q_2 = \Delta^{\alpha\alpha_2}q_3 = \Delta^{\alpha\alpha_2}q_3
\]  
(2.46)

\[
\Delta^{\alpha\alpha_2}q_2 = -\Delta^{\alpha\alpha_2}q_1
\]  
(2.47)

and combining (2.45)-(2.47):

\[
\Delta^{\alpha\alpha_2}q_2 = \Delta^{\alpha\alpha_2}q_3 - \Delta^{\alpha\alpha_2}q_1
\]  
(2.48)

which gives, from inspection of the circuit:

\[C_2(1-z^{-1})(V_0^\circ-V_B^\circ) = -z^{-1/2}(1-z^{-1})C_3 \frac{V_0^\circ}{A} - C_1(V_i^\circ-V_B^\circ)\]  
(2.49)

This combines with (2.41) to give:

\[V_0^\circ = C_2 \left(1 + C_3 \frac{1}{A} \right) = -\frac{C_1}{C_2} \frac{V_i^\circ-V_B^\circ}{1-z^{-1}} + V_B^\circ \left(1 - \frac{C_3}{C_2} \right)\]  
(2.50)

Hence, as previously discovered, the transfer function is a constant multiple of the ideal integrator transfer function only for \(C_3=C_2\). Again, (2.41) has been used to provide a term which gives cancellation between charges stored on \(C_3\) and \(C_2\) and again the cancellation charges result from voltages sampled during the same \(\epsilon\)-phase. Once again, therefore, the operation does not require \(\omega T<<1\), although the correction for accurate (FGI2) \(\alpha\)-phase output does now depend on the ratio \(C_3/C_2\).

(iii). \(\alpha\)-phase FGI property for \(\omega T<<1\) : Equation (2.25) also shows that the N86 integrator sampled in the \(\alpha\)-phase has finite gain insensitivity under the conditions \(C_3\neq C_2\), \(\omega T<<1\). To see the reason for this we return to the charge equation governing the \(\alpha\)-phase output:

\[
\Delta^{\alpha\alpha_2}q_2 = \Delta^{\alpha\alpha_2}q_3 - \Delta^{\alpha\alpha_2}q_1
\]  
(2.48)

From inspection of the circuit:

\[q_2^\circ = C_2(V_0^\circ-V_B^\circ) \quad \text{and} \quad q_3^\circ = C_3 \left(\frac{V_0^\circ}{A} - V_B^\circ \right)\]  
(2.51)
Now, for $\omega T << 1$ the input signal, $V_i$, will change little from one sample to the next and, since it was shown in (2.44) that $V_b^0$ is proportional to $V_i$ to first order, the same must follow for $V_b^0$. It follows that the contribution of $V_b^0$ to $\Delta_{\omega 2}q_2$ and $\Delta_{\omega 2}q_3$ becomes negligible as $\omega$ tends to zero, so that (2.48) and (2.51) give:

$$\left(C_2 + \frac{C_3}{A}\right)_{\omega 2}V_b^0 = -C_1(V_i^0 - V_b^0)$$  \hspace{1cm} (2.52)$$

hence:

$$V_i^0 \left(1 + \frac{C_3}{AC_2}\right) = \frac{V_i^0 C_1 / C_2}{1 - z^{-1}} \left(1 - \frac{C_1}{AC_2}\right)$$ \hspace{1cm} (2.53)$$

which has the correct form for zero phase error. It is therefore seen that the linear relationship between $V_b^0$ and $V_i^0$ (a relationship that was earlier attributed to cancellation of charges from $C_2$ and $C_3$ at node B) causes node B to be an excellent, quasi-DC reference point at low input signal frequencies. There is therefore very little integration charge loss as $C_2$ is switched between node B and the amplifier input on successive cycles, and this low loss accounts for the reduced phase error.

2.4.4 Filter simulation for N86r

**Design:** In this subsection the filter simulations of sub-section 2.3.2 will be repeated, but using the new N86r integrator-pair in order to demonstrate the suitability of this pair for use in SC ladder filters. In fact the filter design, which is shown in fig.2.26, differs from that of a conventional one in only a few respects. The number of clock phases is unaltered, the inverting and non-inverting integrator transfer functions are identical to those for M80, and terminations can be realised using the same finite-gain insensitive branches as are connected to all the other switched inputs. It is, however, necessary, to have switches in series with the zero-forming capacitors, as there are charge transfers taking place in the even clock phase which would be disturbed by their presence, which is only needed for the inverting integrator output 'calculation' in the odd phase. Finally, 'Matsumoto' capacitors are added to overcome the amplifier slewing problem.

**Simulation results:** Simulations were performed only for the case $f_s/f_0=25$, as it was felt that enough information was already available to extrapolate the performance for other $f_s/f_0$ ratios. Fig.2.27 compares the response of the N86r-based filter using $A=100$ amplifiers with those of conventional filters using $A=100$ and $A=1000$. A highly improved response is observed, similar to that obtained earlier using the U87 pair. This reflects the similarity in the expression for gain and phase error in the two pairs.
critical importance is the response obtained including amplifier parasitics, and this is shown in fig.2.28. As before, the parasitics are modelled be generating a grounded parasitic at either node of each 'intentional' capacitor, equal to one third of the value of that intentional capacitor. In addition, a unit-sized grounded capacitor is attached to the input of each amplifier. The figure shows a well-maintained response for A=100, similar in quality to that for a conventional integrator with A=1000, though slightly shifted towards DC. This shift is attributed to the larger gain error in the N86r integrator pair. Comparing this figure with fig.2.16, it is seen that the N86r response is very similar to that for U87 when parasitics are allowed for in both filters, although there is a larger centre-frequency shift for the former. Comparing the gain error expression for the two functions, this extra shift can be accounted for by the larger terms in the $m(\omega)$ expression for N86r. Comparing the phase error expressions, on the other hand, it is seen that the phase error for the U87 integrator-pair will become larger than that for N86r when the $fs/fo$ ratio is decreased, and also it will be negative. A simulation of an N86r filter for $fs/fo=10$ would therefore be expected to show less peaking than was apparent for the U87 filter in fig.2.17. Comparing fig.2.28 with the parasitic-affected N86 response of fig.2.16 (ie. using the original N86 integrators and a 4-phase clock), it is seen that the N86r response is significantly closer to the ideal. This supports the earlier interpretation of the fig.2.16 data that the poor response was due to termination errors.
Fig. 2.26 SC filter, N86r integrator-pairs
Fig. 2.27 Filter passband detail, $\text{N86r}, f_s/f_0=25$, without parasitics
Component cost: An updated table of the component costs for the sixth-order filter, now including N86r, is shown in fig.2.29. The number of switches and the total capacitance values for the N86r filter are exactly the same as for the N86 filter discussed earlier. Compared to the conventional filter, therefore, the N86r filter requires 40 switches compared to 24 and slightly more capacitance (222 cf. 210 units). Compared to the previously favoured U87 filter, the N86r version uses slightly fewer switches (40 cf. 42) and has a lower total capacitance. In addition, the N86r integrator-pair has the major practical advantage of being formed from two identical integrators. This leads to an easier and more economical design process, particularly at the layout stage, where the use of identical units enables a speedier and more compact solution to be reached. A less important, but significant advantage is that working with a single type of integrator is conceptually easier, and minimises the database of measurement and theoretical data associated with the design.
Table: Revised component cost for 6th order filters

<table>
<thead>
<tr>
<th>fc/fp spread</th>
<th>capacitor spread</th>
<th>total capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>all</td>
<td>all</td>
<td>M80 N86 U87 N86</td>
</tr>
<tr>
<td>100</td>
<td>143</td>
<td>669 681 704 681</td>
</tr>
<tr>
<td>25</td>
<td>36</td>
<td>210 222 246 222</td>
</tr>
<tr>
<td>10</td>
<td>14</td>
<td>124 136 165 136</td>
</tr>
<tr>
<td>switches</td>
<td>24 40 42 40</td>
<td></td>
</tr>
<tr>
<td>clock phases</td>
<td>2 4 2 2</td>
<td></td>
</tr>
</tbody>
</table>

Fig.2.29 Revised component cost for 6th order filters

2.5 Summary & Conclusions

Existing FGI integrators were collated in the form of integrator-pairs suitable for implementing ladder and other filters, and their properties compared. This work led to the proposal of a new pair (U87) which featured low phase sensitivity to amplifier gain and economical interconnection for a two-integrator-loop. The new circuit was also free of the problem of amplifier slew during the guard interval between clock phases as it was able to make use of 'Matsumoto capacitors'.

Three circuits - the conventional (M80) pair, the Nagaraj (N86) pair, and the new (U87) pair - were selected for detailed analysis. Equations for the circuits' gain and phase errors, including parasitics, were derived and the N86 and U87 errors found to be small compared to the conventional circuit even with parasitics included. Simulation studies based on a 6th order elliptic bandpass filter confirmed these results, showing that the N86 and U87 versions of the filter give far more accurate filter performance than the M80 version when low-gain amplifiers are used. They also highlighted the increased implementation cost of an N86 design compared to a U87 one, and it was concluded that the U87 circuit was a strong candidate for implementing an FGI SC filter.

The development of a computer-based symbolic analysis tool allowed the further exploration of circuit possibilities and the discovery of a new mode of operation for the N86 integrator that allows it to be formed into a revised integrator-pair (N86r) using only a two-phase clock. The circuit samples one of the integrators in the pair in the phase formerly considered "illegal" but maintains the FGI2 property (ie. phase error proportional to $1/A^2$, independent of signal frequency) by setting a capacitor value that was formerly unimportant equal to the integration capacitance. The low amplifier gain sensitivity of the circuit is slightly reduced when parasitics are considered, although the phase error is still very low for $\omega T<<1$. The revised
integrator-pair has been shown to be similar in accuracy to the previously recommended U87 pair, but significantly more economical to implement. The fact that the revised pair consists of two identical integrators was seen to be a very significant practical advantage for circuit implementation. It is finally concluded that the N86r pair is the most attractive of the FGI-pairs considered, both in terms of accuracy and economy.
3. SETTLING-TIME ANALYSIS AND CHARACTERISATION OF EMBEDDED AMPLIFIERS

3.1. Introduction

3.2. SC Circuit Analysis using the Linear Transconductor Model
   3.2.1 General
   3.2.2 Analysis of a Single-Amplifier Network
   3.2.3 Analysis of a Dual-Amplifier Network

3.3. An Improved Amplifier Characterisation Method
   3.3.1 Introduction
   3.3.2 Characterisation Requirements
   3.3.3 Characterisation Procedure
   3.3.4 Example

3.4. Summary
3.1 Introduction

This chapter deals with the analysis of high-speed Switched-Capacitor circuits that use transconductance amplifiers, a subject that is important both in its own right, and as a preliminary to the GaAs SC circuit design to be described in the next chapter. The limitations of present circuit analysis and amplifier characterisation techniques, which are central to the optimization of such circuits for operation at maximum clocking frequencies, are identified, and two improvements are presented. Firstly, the analysis of settling-time for amplifiers embedded in a capacitor network is extended from the present single-amplifier treatment to a dual-amplifier analysis. This allows the settling behaviour of circuits with inter-amplifier coupling to be predicted much more accurately than was previously possible. Secondly, an amplifier characterisation method is proposed that takes into account the effect of amplifier parasitic capacitances; these were neglected in a previous method, but will be shown to be very significant in high-speed circuits.

3.2. SC Circuit Analysis using the Linear Transconductor Model

3.2.1 General

Transconductance amplifiers are frequently used in high-speed SC applications [26-28,102,145]. Compensation of the amplifier is normally arranged so that the amplifier's settling behaviour is dominated by a single low-frequency pole on the negative-real axis, and under these conditions the amplifier is accurately modelled by a linear transconductor. Compensating the amplifier for linear operation has two main advantages. Firstly, the settling behaviour is relatively easy to predict and control, since the low-frequency pole position is dominated by capacitors external to the amplifier (rather than being strongly dependent on parasitics). Secondly, approximately linear operation allows an economical tradeoff to be made between amplifier size and settling-time, since an increase in one corresponds to a decrease in the other. In contrast, if an amplifier has predominantly non-linear behaviour (ie. its settling is strongly influenced by high frequency poles and is underdamped) then a decrease in amplifier size will decrease settling-time also, since decreasing the amplifier drive capability will decrease the overshoot resulting from a step-input response. This situation is inefficient, since it implies that the amplifier is oversized.
It has previously been argued that the behaviour of an embedded amplifier of the single-stage cascode type will be dominated by a high frequency pole, so that its settling is underdamped [28]. However, an analysis is presented in appendix 2 to show that this is not generally the case. Further evidence that the linear-transconductance model has wide applicability is given by Haigh et al [165], who showed that it is straightforward and desirable to design the amplifier embedding for approximately linear operation. The latter work described a method for optimising the settling behaviour of an SC circuit. Having characterised an amplifier and derived a linear model for it, the SC circuit was represented in each clock phase by a number of single-amplifier networks, as shown in fig.3.1. The effective capacitative load for a linear transconductance amplifier in this configuration is well known [165], and so the SC circuit may be quickly optimised, using any design freedom available, to minimise the circuit's worst-case settling-time. A limitation of this procedure is that not all SC circuits may be accurately decomposed into a single-amplifier network in all clock phases. To circumvent this problem the method analysed one amplifier at a time, treating the remainder as ideal, so that inter-amplifier coupling was effectively ignored. However, it will be shown that significant coupling frequently exists between amplifiers in practical SC circuits, and has an important effect on settling-times. The case of a dual-amplifier network, as shown in fig.3.2, is particularly important, firstly because of its direct applicability to biquad filters, but also because the information obtained for dual-amplifier systems frequently gives insight into the behaviour of larger circuits. In spite of this, a general analysis for the settling properties of a dual-amplifier network is not presently available. This section will present such an analysis.
As a first step, some aspects of the single-amplifier network will be reviewed. The method used for the dual-amplifier analysis will then be explained and, since the general solution for the poles of the network is extremely unwieldy, the results will be interpreted using certain interesting special cases (a complete solution is given in appendix 3). The use of the results to calculate amplifier effective capacitance loads is also described.

3.2.2 Analysis of a Single-Amplifier Network

Solution of Network Equations: The network to be analysed is shown in fig.3.1. It can be shown that there is a single pole at:

\[ p_1 = -\frac{gm}{C_i + C_i + C_i C_i / C_f} \]  

(3.1)

implying that the effective capacitance seen by a transconductance amplifier in the above configuration is [165]:

\[ C_{\text{eff}} = C_i + C_i + C_i C_i / C_f \]  

(3.2)

The time constant associated with \( p_1 \) is therefore:

\[ \tau = C_{\text{eff}} / gm \]  

(3.3)

and it can be shown that this time constant dominates the settling behaviour of the system\(^1\).

Optimisation of Amplifier Scaling Factor: The effect of changing the dimensions of the amplifier (scaling the amplifier) on the network time

\(^1\)In particular, if the grounded terminal of \( C_i \) is switched to some constant voltage source, so that a step input is applied to the system, then the zero in the response from this input to the output will not affect the system settling-time.
constant will now be investigated. To do this, account has to be taken of the
self-loading effect of the input and output capacitances of the amplifier itself
\((C_g \& C_o)\), which are shown in fig.3.3. Comparing figs 3.3 and 3.1 it is seen
that:

\[ C_i = C_I + C_g, \quad C_I = C_L + C_o \quad (3.4) \]

A unit-sized amplifier is defined as that which has a transconductance
\(g_{m0}\), and input and output capacitances \(C_{g0}\) and \(C_{o0}\) respectively. We
further define a Linear Scaling Property (LSP) whereby, for an amplifier
possessing the LSP, scaling by a factor \(X\) will give new values of transconductance, input capacitance and output capacitance:

\[ g_m = X.g_{m0}, \quad C_g = X.C_{g0}, \quad C_o = X.C_{o0} \quad (3.5) \]

For circuits where the LSP applies, therefore, we can combine (3.2) and (3.3)
with (3.4) and (3.5) to obtain:

\[ \tau = \frac{C_{ext}}{X} + C_{g0} + C_{o0} + \frac{C_{o0}C_I/C_f + C_{g0}C_L/C_f}{g_{m0}} + \frac{X.C_{g0}C_{o0}}{C_{fgm0}} \quad (3.6) \]

where the following definitions are used:

\[ \tau_0 = C_{ext}/g_{m0} \quad (3.7) \]

\[ C_{ext} = C_I + C_L + C_f/C_f \quad (3.8) \]

Differentiating with respect to \(X\) in (3.6) and setting the differential to
zero, it can be shown that there exists a value of \(X\) for which \(\tau\) is a minimum.
This value is defined as the optimum scaling factor, and is given by:

\[ X_{opt} = \sqrt{\frac{C_fC_{ext}}{C_{g0}C_{o0}}} \quad (3.9) \]

Substituting (3.5) in (3.9) for \(X = X_{opt}\) gives:

\[ C_gC_o = C_fC_{ext} \quad (3.10) \]
This equation, which confirms the result of Matsui et al [27], indicates that, for the simple transconductor model chosen, the optimum scaling of the amplifier is such that the amplifier input and output capacitors are of the same order of magnitude as the capacitors in the external network.

3.2.3 Analysis of a Dual-Amplifier Network

A general network containing two transconductance amplifiers is analysed in order to obtain information about its settling characteristics. The system is second order, and an expression for its denominator function is presented. This function is quite complex, and the analysis was only made possible using the MASON and PS symbolic analysis tools, originally developed for the work of the previous chapter (they are described in appendix 1).

General Solution of Network Equations: The network to be analysed is shown in fig.3.2 and may be represented by the SFG in fig.3.4, where the following definitions are used:

\[ c_{sj} = \sum_{i \neq j} C_{ij} \quad (3.11) \]

The application of Mason's rule, by the MASON computer program to compute the denominator function, \( D(s) \), of this SFG results in a quadratic:

\[ D(s) = as^2 + bs + c \quad (3.12) \]

where

\[ a = \tau_1 \tau_2 - A + \frac{C_{13}^2 C_{24}^2 + C_{14}^2 C_{23}^2}{g_{m1} g_{m2} C_{f1} C_{f2}} \quad (3.13) \]

\[ b = \tau_1 + \tau_2 + B \quad (3.14) \]

\[ c = 1 - \frac{C_{14} C_{23}}{C_{f1} C_{f2}} \quad (3.15) \]
\[ \tau_n = \frac{C_{in} + C_{in} + C_{in} C_{in}/C_{fin}}{g_{m n}}, \quad n = 1 \text{ or } 2 \quad (3.16) \]

\[ C_{l1} = C_{10} + C_{14}, \quad C_{l1} = C_{20} + C_{24} + C_{23}, \quad C_{f1} = C_{12} \quad (3.17) \]

\[ C_{l2} = C_{30} + C_{23}, \quad C_{l2} = C_{40} + C_{24} + C_{14}, \quad C_{f2} = C_{34} \quad (3.18) \]

It can be shown that \( A \) and \( B \) are positive quantities, and they are given in full in appendix 3. Note that, for the analysis that follows, the capacitors \( C_{f1} \) and \( C_{f2} \) are constrained to be non-zero.

![Diagram](image)

Fig. 3.4 SFG for the general dual-amplifier network of fig. 3.2

The physical interpretation of (3.12-3.18) is started by comparing (3.12) with the common representation of a quadratic function:

\[ D_{quad}(s) = s^2 + 2\epsilon \omega_n s + \omega_n^2 \quad (3.19) \]

where \( \epsilon \) is called the damping factor of the system and \( \omega_n \) the natural frequency. If \( \epsilon < 1 \) then the system has a pair of complex conjugate poles, and is underdamped; if \( \epsilon = 1 \) then it has two identical poles and is said to be critically damped; if \( \epsilon > 1 \) then it has two real negative poles and is overdamped [164].

By comparison of (3.12) and (3.19) and considering the poles of \( D(s) \) it can be readily shown that:
Note that the larger time constant, $\tau_-$, will normally dominate the settling characteristics. The validity of (3.13-3.18) and (3.20-3.22) have been checked by extensive SPICE simulations of dual-amplifier networks, using ideal transconductors.

**Effect of amplifier coupling:** The above expressions have been used to examine the dual-amplifier network of fig.3.5, where two single-amplifier networks, with all unit-sized (1F) capacitors, are connected by one other unit-sized capacitor. The transconductance of amplifier 1, $g_{m1}$, is set to unity (1 mho) and the effect on the dominant network time-constant of varying $g_{m2}$ is plotted in fig.3.6 (this plot is confirmed by SPICE simulation). Now, if amplifier 2 were ideal then it can be calculated that $C_{eff1} = 5F$. Thus, amplifier 1 would have a time constant of 5s, as is confirmed by the asymptote of fig.3.6 for $g_{m2} \to \infty$. In fact, the plot shows that the dominant system time-constant increases rapidly above this value for $g_{m2}$ less than about 2S, and is about 40% greater at $g_{m1} = g_{m2} = 1$ mho. This clearly demonstrates the importance of taking the interaction between the amplifiers into account when estimating the system time constant. This conclusion is also strongly supported by simulations of dual-amplifier networks containing amplifiers represented at transistor level [158].

![Fig.3.5 A dual-amplifier network to demonstrate the significance of inter-amplifier coupling](image-url)
Special Case 1: Consider the case of a network where:

\[(C_{13} = 0 \ OR. \ C_{24} = 0) \ AND. \ (C_{14} = 0 \ OR. \ C_{23} = 0) \quad (3.23)\]

As Fig.3.2 shows, the capacitors in (3.23) are those linking the inputs and outputs of the two transconductors. It turns out that the condition (3.23) is satisfied in a great number of practical cases (including those to be examined in section 3.4). Given (3.23) we have, from (3.13-3.15):

\[a \leq \tau_1 \tau_2, \ b \geq \tau_1 + \tau_2, \ c = 1 \quad (3.24)\]

Using (3.24) in (3.20) gives:

\[\varepsilon \geq \frac{\tau_1 + \tau_2}{2 \sqrt{\tau_1 \tau_2}} \quad (3.25)\]

and from this it can be shown that, for \(\tau_1\) and \(\tau_2\) real, \(\varepsilon \geq 1\). Thus, for the important class of circuits which satisfy (3.23), the settling is always overdamped.

Special Case 2: For this special case:

\[C_{13} = C_{23} = C_{24} = 0 \quad (3.26)\]
Note that (3.26) will apply to many frequently encountered SC two-amplifier circuits. For example, both the 'low-Q' and 'high-Q' SC biquads in [2] fit this model. Given this constraint, (3.13-3.15) become:

\[ a = \tau_1 \tau_2 - A, \; \; b = \tau_1 + \tau_2, \; \; c = 1 \] (3.27)

and, from the full expression for \( A \) in appendix 3:

\[ A = \tau_{14} \left( \frac{C_{11} C_{i2}}{C_{f1} C_{f2}} + \frac{C_{11}}{C_{f1}} + \frac{C_{i2}}{C_{f2}} \right) \] (3.28)

where

\[ \tau_{14} = \frac{C_{14}}{\sqrt{g_{m1} g_{m2}}} \] (3.29)

Thus, for the special case defined by (3.26), the parameters \( a, b \) and \( c \) are given by a relatively simple function of \( \tau_1, \tau_2 \) and \( A \). Substitution into (3.20-3.22) then gives the key system parameters. These expressions are simple enough to be evaluated 'by hand' whereas, in general, it is impractical to compute (3.13-3.22) without the aid of a computer.

**Special Case 3:** It is interesting to consider the case where (3.26) holds and also:

\[ A << \tau_1 \tau_2 \] (3.30)

Under these conditions (3.22) gives the approximate expressions:

\[ \tau_+ = \min(\tau_1, \tau_2), \; \; \tau_- = \max(\tau_1, \tau_2) \] (3.31)

The reason for this simple result is as follows. Condition (3.30) becomes true when \( C_{14} \) becomes small in comparison to the other capacitors in the network. Since, given condition (3.26), this is the only capacitor coupling the two amplifiers, (3.30) means that the amplifiers are only very weakly coupled. It is to be expected that the poles of the system will approach those of the two first order systems that the network decomposes into when \( C_{14} = 0 \). This is in fact what has happened, as can be confirmed by comparing the definitions for \( \tau_1 \) and \( \tau_2 \) (given by (3.16)) with the time constant for the single-transconductor network derived in the previous section (equations (3.2-3.3)). The zeros of the system now have an important role in determining the settling behaviour of the system. If, for example, the transfer function from node 1 to 2 is calculated, then a zero appears in the numerator which nearly cancels the \( \tau_2 \) pole (i.e. the
pole attributable to amplifier 2). Clearly, the reverse happens if the transfer function from nodes 3 to 4 is calculated, in which case a zero appears to cancel the $\tau_1$ pole. This special case therefore demonstrates the continuity between the treatments of the single- and dual-transconductor networks.

Eqn. (3.30) is also a good objective measure of when inter-amplifier coupling begins to have a significant effect on amplifier settling-times. To quantify this limit, fig.3.7 plots the affect of $A$ on $\tau_-$ and $\tau_+$ when $\tau_1$ and $\tau_2$ are (artificially) fixed at one second. As expected from the discussion above, $\tau_+$ and $\tau_-$ converge on unity as $A$ tends to zero, and it is seen that they are within 10% of their final values at $A \sim 0.01$. As a good rule of thumb, therefore, one could say that we require:

$$A < \frac{\tau_1 \tau_2}{100}$$

(3.32)

for inter-amplifier coupling to have a negligible effect on amplifier settling-time.

A further interesting feature is seen by combining (3.20) with (3.27) and (3.30). This results in:

$$\varepsilon = \frac{\tau_1 + \tau_2}{2\sqrt{\tau_1 \tau_2}}$$

(3.33)

which has a minimum of $\varepsilon = 1$ when $\tau_1 = \tau_2$. This suggests that, in general,
Critical damping may be approached by designing the system to have $\tau_1$ and $\tau_2$ as near to equal as possible. Conversely, it suggests that a system with widely differing $\tau_1$ and $\tau_2$ will be heavily overdamped.

**Effective Capacitance Load** : It follows from the definition of an effective load that for linear amplifiers:

\[ \tau_{domn} = \frac{C_{effn}}{g_{mn}}, \quad n = 1 \text{ or } 2 \tag{3.34} \]

where $\tau_{domn}$, $C_{effn}$ and $g_{mn}$ are the dominant time constant, the effective load capacitance and the transconductance respectively for amplifier $n$. Since $\tau_{dom1}$ and $\tau_{dom2}$ may be obtained from expressions previously derived, the effective loads may be computed from:

\[ C_{eff1} = \tau_{dom1}gm_1 = \tau - gm_1 \tag{3.35} \]
\[ C_{eff2} = \tau_{dom2}gm_2 = \tau - gm_2 \tag{3.36} \]

for a network where there is significant coupling between the amplifiers. Equations (3.35-3.36) therefore give a simple method for calculating the effective loads on each of the amplifiers in the dual-amplifier network.

**Optimisation of Amplifier Scaling Factor** : A knowledge of the optimum amplifier scaling factors, $X_{1_{opt}}$ and $X_{2_{opt}}$, is important to the design process, as it provides a design target and a reference by which a given design may be judged. In principle one could find these parameters by substituting expressions for the amplifier's scaled transconductances and capacitances into (3.13-3.18) and (3.20-3.22), then using the result to minimise the settling-time with respect to $X_1$ and $X_2$. However, the resulting simultaneous equations for $X_1$ and $X_2$ are non-linear, and so numerical techniques are called for. To do this, for a given set of capacitors in the network, $\tau_-$ must be computed as a function of $X_1$ and $X_2$, generating a three dimensional surface where the minima in $\tau_-$ corresponds to the desired $X_{1_{opt}}$ and $X_{2_{opt}}$. To find a convenient starting point for this search, it is useful to return to special case 3, defined by (3.26) and (3.30). Under these conditions, from (3.31):

\[ \tau_- = \max(\tau_1, \tau_2) \tag{3.37} \]

Inspection of the definitions of $\tau_1$ and $\tau_2$ in (3.16) shows that $\tau_1$ (resp. $\tau_2$) is independent of $X_2$ (resp. $X_1$) in this case. It is therefore straightforward to minimise $\tau_1$ (resp. $\tau_2$) as a function of $X_1$ (resp. $X_2$), and, following similar working to that in section 2, show that, in this special case:
\[ X_{\text{opt}} = \sqrt[3]{\frac{C_{\text{fn}} C_{\text{ext}}}{C_{\text{gn}} C_{\text{dn}}}}, \ n = 1 \text{ or } 2 \]  
(3.38)

where

\[ C_{\text{ext}} = C_{\text{in}} + C_{\text{Ln}} + C_{\text{Ln}} C_{\text{Ln}} / C_{\text{fn}}, \ n = 1 \text{ or } 2 \]  
(3.39)

Equation (3.38) gives an approximate optimum point, \( X'_{\text{opt1}}, X'_{\text{opt2}} \), from which a search for the actual optimum may be started. One would expect, following the discussion of this special case above, that the true optimum will move further away from the point defined by \( X'_{\text{opt1}}, X'_{\text{opt2}} \) the stronger the coupling between the amplifiers becomes.

### 3.3. An Improved Amplifier Characterisation Method

#### 3.3.1 Introduction

The previous chapter used a linear-transconductor model of an amplifier in order to analyse circuit settling properties, and it is known that this model frequently describes single-stage amplifiers. It is therefore important to have a simple and general method for finding the parameters that characterise such an amplifier, and to know if the linear-transconductance model can be applied in a given embedding.

Haigh et al have presented an amplifier characterisation technique based on Matsui's formula for the amplifier's effective load [165]. In this method, the amplifier to be characterised is simulated in a circuit such as that shown in fig.3.8, with \( C_I \) set to zero. A short current-pulse is injected in order to give the desired step output, then the settling-time is measured. This is plotted on the characterisation graph for a range of values of \( C_L \), as shown in fig.3.9, which uses the fact that, when \( C_g \) and \( C_o \) are neglected, the effective load is equal to \( C_L \). In this graph, the area to the right of the minimum in each line corresponds to linear amplifier settling, while that to the left is where settling is underdamped. The graph is used for the optimisation of an SC circuit by first placing each amplifier in its embedding for each clock phase and calculating values of effective input, output and feedback capacitances (\( C_I, C_L \) and \( C_f \)). Since the amplifier parasitic capacitances, \( C_g \) and \( C_o \), are neglected in this method, the effective load is approximately equal to \( C_{\text{ext}} \).
The settling-time corresponding to this effective load is then read from the characterisation graph, and any available design freedom used to adjust circuit capacitor values for minimum worst-case settling-time. This is generally achieved when the effective loads in each phase differ as little as possible, so that the amplifier may operate at points near the minimum in $t_s$ in all three phases.

From the forgoing description, it is seen that the assumption that $C_g$ and $C_o$ are small occurs at two points in the characterisation method. Firstly, when the amplifier is characterised and, secondly, when the characterisation data is being used to optimize an SC circuit. The actual contribution of $C_g$ and $C_o$ to the amplifier's effective load is, from (3.2), (3.4-3.5) and (3.8):

$$C_{\text{eff}} = C_{\text{ext}} + X \left( C_{g0} + C_{o0} + \frac{C_f C_{o0}}{C_g} + \frac{C_{f L} C_{g0}}{C_f} \right)$$  \hspace{1cm} (3.40)
which is only valid if:

$$C_g + C_o \ll C_i + C_L$$

(3.41)

for all scaling factors of interest. For the case of optimum amplifier scaling, however, we have:

$$C_g C_o = C_f C_{ext}$$

(3.10)

This shows that at the amplifier scaling for minimum settling-time the parasitics are of the same order as the external capacitors, and implies that $C_g$ and $C_o$ do have a significant effect on $C_{eff}$ in this important case. A general characterisation method must therefore take $C_g$ and $C_o$ into account.

### 3.3.2 Characterisation Requirements

To find the parameters that characterise the amplifier when it is in its linear region of operation, we return to (3.6):

$$\tau = \frac{\tau_0}{X} + \frac{C_g 0 + C_o 0 + C_o C_i / C_f + C_g 0 C_L / C_f + X C_g 0 C_o 0}{g_m 0 C_f g_m 0}$$

(3.6)

which shows that, in order to characterise the amplifier for its linear region of operation, the parameters $C_g 0, C_o 0$ and $g_m 0$ must be determined.

In addition to this, it is important to know the limit of linear operation of the amplifier. For this work, the transition point between linear and non-linear operation is taken to be that where a decrease in the amplifier's effective load first produces an increase in settling time (this occurs when settling first becomes underdamped). We therefore define the Scaling Limit, $\kappa$, as being the minimum effective load required to ensure linear operation for a unit-sized amplifier:

$$\kappa = C_{eff} \text{ at } t_{s_{\text{min}}} \text{ for } X = 1$$

(3.42)

The value of $\kappa$ will depend on the amplifier design and the definition of the unit amplifier size. Equation (3.42) implies that, in a given embedding, the maximum amplifier scaling factor to maintain linear operation is:

$$X_{\text{max}} = C_{eff} / \kappa$$

(3.43)

Note that the previously derived expressions for $C_{eff}$ are valid for the
linear region of operation up to and, by continuity, including the transition point with the non-linear region.

### 3.3.3 Characterisation procedure

The procedures to be described are based on multiple simulation of a simple single-amplifier circuit. Each simulation therefore takes very little computer run-time, and, since most computer systems make it straightforward to perform such simulations in a 'batch-mode', the procedures are efficient to implement.

**Transconductance**

The transconductance of the amplifier can be found by simulating a unit-sized amplifier in a network such as that in fig.3.8, ensuring that the load capacitance is chosen such that \( C_{\text{eff}} \) is much larger than the amplifier parasitic input and output capacitances. The settling-time of the amplifier, \( t_s \), for a given percentage settling accuracy, \( \rho \), is then found for a number of \( C_{\text{eff}} \) values and a graph plotted of \( t_s \) vs. \( C_{\text{eff}} \). Provided all the \( C_{\text{eff}} \) data values were sufficiently large, this will be a straight line with slope, \( m \), and \( g_{m0} \) is given by:

\[
g_{m0} = \frac{\ln(100/\rho)}{m} \quad (3.44)
\]

**Parasitic input and output capacitances**

First, to find \( C_{g0} \), a unity-scaled amplifier is placed in a network such as that shown in fig.3.8, with the \( C_I \) and \( C_L \) capacitors set as follows:

\[
C_I = 0, \quad C_L \gg C_{g0}, \quad C_L \gg C_{g0} \quad (3.45)
\]

Using (3.45) in (3.6) with \( X=1 \) gives the approximate expression:

\[
\tau = \frac{C_L + C_{g0} C_L / C_I}{g_{m0}} \quad (3.46)
\]

From this equation it is seen that a plot of \( \tau \) vs \( 1/(C_I g_{m0}) \) will give a straight line with slope \( m = C_L C_{g0} \) and intercept on the \( \tau \) axis at \( \tau = C_L / g_{m0} \). Hence, to find \( C_{g0} \), the settling time of the amplifier in response to a unit step is simulated for a range of \( C_I \) values then the aforementioned graph is plotted and \( C_{g0} \) found from:

\[
C_{g0} = \frac{m}{C_L \ln(100/\rho)} \quad (3.47)
\]

Similarly, to find \( C_{o0} \), the same network is used but with:

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In this case it can be shown that:

\[ \tau = \frac{C_I + C_{g0}C_I/C_f}{g_m0} \]  

(3.49)

and a simple modification of the procedure for finding \( C_{g0} \) can be used to find \( C_{o0} \).

Note that, for a unity-scaled amplifier with \( C_I = C_L = 0 \):

\[ \tau = \frac{C_{g0} + C_{o0} + C_{g0}C_{o0}/C_f}{g_m0} \]  

(3.50)

It is tempting to suggest that \( \tau \) be plotted against \( 1/(C_fg_m0) \) for this case, then \( C_{g0} \) and \( C_{o0} \) might be derived from the slope and intercept of the straight line produced (ie. both values could be derived from a single plot). This is not practical, however, as with \( C_I = C_L = 0 \) the amplifier settling will generally be underdamped and it will not behave as a linear transconductor. Equation (3.6) would not, therefore, apply. For similar reasons it is important, when setting \( C_L \) in (3.45) and \( C_I \) in (3.48), to make the capacitors large enough to adequately compensate the amplifier.

**Scaling Limit:** Having obtained \( C_{g0} \) and \( C_{o0} \), a unit-scaled amplifier is simulated in a capacitor network, as shown in fig.3.8, but with:

\[ C_I = K_I C_U, \ C_L = K_L C_U, \ C_f = K_f C_U \]  

(3.51)

so that the effective capacitative load seen by the amplifier is given by:

\[ C_{\text{eff}} = K_I C_U + C_{g0} + K_L C_U + C_{o0} + \frac{(K_I C_U + C_{g0})(K_L C_U + C_{o0})}{K_f C_U} \]  

(3.52)

A current pulse is applied to the system and the settling-time measured to obtain a single \( C_{\text{eff}}, ts \) data point. This procedure is repeated for different values of \( C_{\text{eff}} \) by altering the unit-capacitance, \( C_U \), of the network, then recalculating \( C_{\text{eff}} \) from (3.2). These results are then plotted on a graph, an idealised version of which is shown in fig.3.10. In this diagram, the points to the right of the minimum in ts lie on a straight line that passes approximately through the origin; this is where the amplifier is sufficiently compensated to behave as a linear transconductor. To the left of the origin the amplifier is under-compensated, settling is underdamped and settling-time rises.
The minimum point of the graph represents the limit of linear transconductance operation, and so $\kappa$ can be simply read from the $C_{\text{eff}}$ axis (for more detail on how a single-stage cascode amplifier behaves near this limit, see appendix 2). It should be noted that a given amplifier may not exhibit the described deviations from ideal transconductor behaviour for all amplifier embeddings. If a particular amplifier has very large $C_{g0}$ and $C_{o0}$ values then it may be considered to be internally compensated. If, on the other hand, $C_{g0}$ and $C_{o0}$ are both very small, then underdamped settling is bound to occur at some point as $X$ is increased in a given capacitor network. In between these extremes, the occurrence of underdamped settling will depend on the details of the capacitor network in which the amplifier is embedded. For this reason, as well as to safeguard against any possible procedural errors, it is recommended that several sets of data are taken, using different values of $K_I$, $K_L$ and $K_f$, and plotted on the same graph.

### 3.3.4 Example

Fig.3.11 shows the circuit diagram of the folded-cascode transconductance amplifier to be used for this example, which is based on [2] and simulated using ES2 $2\mu$ device models [167]. The test circuit used in the SPICE simulations is shown in fig.3.12. The devices $L_f$ and $E_f$ are used to force the initial transient solution to a reasonable bias point, and the voltage-
controlled current source at the input isolates the input capacitor, $C_{in}$, from
the amplifier. By setting $C_{in}$ equal to $C_f$ a reasonable voltage step at the
amplifier output is ensured for all values of $C_I$ and $C_L$.

Fig. 3.11 Single-stage folded-cascode amplifier to illustrate characterisation method.

The straight-line data used to obtain $g_m 0$, $C_g 0$ and $C_o 0$ is shown in
figs. 3.13 to 3.15. The values derived, using the method described above, are
also shown on the figures, and are in close agreement with theoretical
expectations. Also, the small error margins in the slopes testifies to the
accuracy of the results.
**Fig. 3.13** Amplifier characterisation graph - \( g_m \) calculation

**Fig. 3.14** Amplifier characterisation graph - \( C_{g0} \) calculation
The graph used to find the Scaling Limit, $\kappa$, is shown in fig.3.16, and was obtained using two different capacitor networks (given by $K_I=1$, $K_L=0$, $K_f=2$ and $K_I=0$, $K_L=1$, $K_f=2$ respectively). The graph clearly shows a linear region to the right of the minimum (which has a slope equal to that of fig.3.13, confirming $g_{m0}$), and a scaling limit of $\kappa=3.2\text{pF/unit scaling factor.}$
The figure is also used to highlight the difference in results when the $C_{g0}$ and $C_{00}$ parasitics are neglected. The data plotted without taking account of parasitics clearly gives a different Scaling Limit to the recommended method, as well as a different slope ($g_m$) in the linear region. Further example data that supports these results is given in [158].

### 3.4 Summary

The chapter has presented a set of analytical results for a dual-amplifier network that were not previously known and shown, with a simple example, that inter-amplifier coupling has a significant effect on settling times. The results are important in view of the large number of SC circuits that form sub-networks containing two or more amplifiers in different clock phases. The formulae allow networks with two amplifiers to be analysed exactly, and give useful insight into the behaviour of larger networks.

It has been shown that the settling in a dual-amplifier network is overdamped for a special-case that includes nearly all practical SC circuits. The settling-time in a second special case, which includes many practical biquad filters, was given by a formula of relatively low complexity, suitable for hand calculations. It also allowed a condition to be derived which gave an objective measure of whether inter-amplifier coupling would have a significant effect on settling-times in a given embedding. A third special case, where inter-amplifier coupling was very weak, demonstrated the continuity between the single- and dual-amplifier analyses. The method for calculating the effective load on each of the amplifiers in the dual-amplifier circuit was seen to be a natural consequence of the time-constant calculations. Finally, it was seen that the theoretical optimum scaling factors for the amplifiers in the dual-amplifier network are not given by closed-form expressions, as they had been in the single-amplifier case, and so approximate expressions were derived as a starting point for a numerical search procedure.

To complement the above work, a general characterisation method for transconductance amplifiers was given. A previous method was first reviewed, and it was shown that its omission of amplifier parasitics compromised the important objective of producing characterisation data independent of the amplifier embedding. The parameters needed in an improved characterisation method were then identified, and simple simulation techniques for obtaining them described.
4. THE DESIGN OF A GaAs SC FILTER

4.1. Introduction

4.2. Design
4.2.1 Process and FET model
4.2.2 Switch Design
4.2.3 Amplifier Design and Characterisation
4.2.4 Circuit Optimisation
4.2.5 Layout and final design parameters

4.3 Circuit performance

4.4. Summary and Conclusions
4.1. Introduction

It was shown in chapter 1 that GaAs has several properties that favour the implementation of high-speed SC circuits, although these are counterbalanced by difficult technical challenges. This chapter describes the design of a GaAs SC filter, exploiting the work described in the previous two chapters. (Note that extensive background information on the issues involved in GaAs SC circuit design is given in chapter 1, and that various aspects of the design are also described in [146,147,148,158]). The design specification was initially taken to be the same as that used in earlier demonstrator GaAs SC circuits [31,32], that is, a second-order filter with lowpass and bandpass outputs and a Q of 16 (although the Q specification was later reduced because of constraints on the realisation of capacitors). The circuit was targeted at clock frequencies up to 500MHz, to give filter centre frequencies up to 40MHz. The process used was known to produce FETs with low intrinsic gain, $g_m/g_o$, and so it was decided at an early stage that using a circuit with low sensitivity to finite amplifier gain would be advantageous. Following the work described in chapter 2 the filter shown in fig.4.1 was taken as a starting point, and, in order to maintain a well-understood reference, this was developed in parallel with its conventional counterpart, shown in fig.4.2. Capacitor values are shown for both circuits in fig.4.3, and the $C_x$ capacitors are included in the conventional circuit to reduce the difference in amplifier loads in the o- and e-phases [184] (this is unnecessary in the FGI design because of the extra load from the $C_h$ and $C_m$ capacitors).

![Fig.4.1 Second-order SC filter using n86r integrator-pair](image_url)
Fig. 4.2 Second-order SC filter using conventional integrator-pair

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Fig. 4.3 Initial design values for circuits in figs. 4.1 & 4.2.

4.2. Design

4.2.1 Process and FET model

Accurate modelling of GaAs MESFETs for analogue circuits is beset by two main difficulties. Firstly, non-linear MESFET models are still in an immature state, and no general agreement exists as to the best modelling approach [47, 23: ch.3]. Although simulator programs incorporating non-linear MESFET models do exist, they are not widely available, and, in any case, the accuracy of some of them appears to depend on the particular process used [184, 109]. Secondly, since available GaAs processes are almost always developed with microwave applications in mind, the foundry data is generally given for linear operation above approximately 1GHz using a restricted range of bias conditions, with little data for lower operating frequencies and only relatively little information on non-linear performance [60: ch.10, 186, 187]. Interpretation and extrapolation of this data is therefore an important, difficult and dangerous
The Plessey f14 process was used for the project. It features 0.7μ gate-length MESFETs (0.5μ drawn), and is the predecessor to the f20 process described in chapter 2 of [23]. Unfortunately the device characteristics for these processes are not ideally suited to the design in hand. A high device threshold voltage (~2.5v) and low intrinsic gain (gm/go~16) are two of the main drawbacks, and appear to be significantly more severe for this process than for some of its competitors (eg.[188,166]). Although these parameters are not critical for microwave applications, we will show that they have a large impact on analogue designs for the MHz range. (For this reason, in fact, we are currently working with Plessey, Cossor Electronics and Bradford University in a project that aims, amongst other things, to improve the usefulness of the Plessey process for such applications). The foundry data was in the form of S-parameter tables for frequencies above 1GHz under a number of bias conditions, and for devices with gate widths of 300μ [187]. The minimum realizable gate width recommended by the foundry engineers was 16μ, and so we supplemented the S-parameter data with low-frequency measurements on FETs with gate widths of 16μ, 24μ and 34μ [189]. 16μ was subsequently chosen as the unit gate-widths for the design.

Mixed-mode simulation requires use of multiple models. Parameters optimized for each model depend on device operating conditions.

Strategy of using several model subcircuits overcomes the limitations in using Spice simulator.

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Fig.4.4 Multiple-subcircuit model of MESFET

1funding from SERC/RAL pump-priming award scheme
2funding from DTI Advanced Technology Programme
The simulator used was Spice 2G6 [171], which has no MESFET model, and so special techniques were adopted to model accurately the range of device features in which we were interested. This was done by identifying features of the model which were the most important for particular modes of MESFET operation. Three different model sub-circuits were developed, each of them optimised for the accurate reproduction of a particular set of characteristics, as illustrated in fig.4.4. These models were:

**Digital mode model:** In the digital parts of the circuit, which provide the clock signals, the devices go through the extreme range of operating points. For this mode of operation, it is important to have an accurate large-signal model, and the model subcircuit used is shown in fig.4.5. The early saturation effect (see chapter 1) is modelled using the voltage-controlled voltage source (VCVS) at the JFET gate, giving correct DC conditions [108]. Output conductance dispersion is modelled by devices $C_{oac}, R_{oac}$ and $R_{ode}$. For this process the on-state output conductance is only weakly dependent on $I_d$, so the the JFET parameter LAMBDA is set to zero and $g_o$ is completely determined by these devices. The diodes in the JFET are also nullified (by setting $I_s$ to 1e-20) since the JFET gate voltage has been artificially modified by the VCVS and can no longer be used to calculate the non-linear capacitances associated with these diodes. The MESFET diode junction is instead modelled by the external $D_{gs}$ and $D_{gd}$. MOSFET Mcutoff gives zero conductance when in the off state, as required. The static characteristic for the model is shown in fig.4.6 and gives excellent agreement with static measured data.

![Fig.4.5 Subcircuit for digital MESFET model](image-url)
Fig. 4.6 Static characteristic, measured vs. simulated for digital MESFET model

**Analogue mode model:** In the amplifiers and buffers, the devices are permanently biased in the saturation region at a relatively stable operating point. The model for these devices is optimised to give correct values for $g_m$, $g_o$, capacitance values and DC voltage operating point. The sub-circuit for this model is obtained from that in fig.4.5 by removing the $M_{cutoff}$ and adjusting the model parameters. Conformity with measured small-signal device data was confirmed by simulation of a two-transistor inverter, which gave gain values in agreement with those derived from S-parameters for frequencies above the dispersion frequencies.

**Switch mode model:** The devices used to realise the switches in the SC circuit experience extreme operating points and must be symmetrical with respect to drain and source. In this mode it is also important to accurately simulate on-resistance and cutoff voltage. The model subcircuit is a completely stripped-down version of that in fig.4.5, consisting only of the device J1 plus a parallel resistor-capacitor combination between drain and source to determine capacitative feedthrough and off-resistance.
4.2.2 Switch Design

As mentioned in chapter 1, it is important to avoid forward-biasing the gate of the MESFET switch, and so a switch control circuit (SCC) is required to restrict the amplitude of this gate voltage. We decided to design a buffered SCC, so that the amplifier scaling could be approximately independent of the number of SCC's that it was driving. Although it has been suggested that the SCC should be designed to have a fixed output-voltage swing, in order to avoid signal-dependent clock feedthrough [102], extensive SPICE simulations to find the total harmonic distortion in a first-order filter using SCCs with and without a fixed output-voltage swings, were inconclusive and did not confirm this. No provision was therefore made for a fixed output-voltage swing in this SCC design. Our main considerations were compactness of layout, minimisation of power consumption, and ease of test (given the uncertainty in some of the modelling data, we wished to retain the option of adjusting as many circuit parameters as possible).

![Switch-control circuit (SCC) with switch device T6 (Vdd=-Vss=5v)](image)

The SCC used is shown in fig.4.7, where T6 is the switch device. $V_{inp}$ and $V_{inm}$ are complementary clock signals which turn S3 and S5 on and off in a complementary manner. As a result, the source-follower S1 has a drain current which is the same in both switching states and its source voltage is approximately equal to the signal voltage $V_{sig}$. Thus the voltage on the gate of T6 alternates between $V_{sig}$ and $V_{ss}$, closing and opening the switch. The gate width multiplying factors for the devices relative to the minimum gate width are given in brackets in the figure. The fact that S1 is a minimum size device is an advantage resulting from the complementary switching. As far as simulation is concerned, device T6 is represented by a switch-mode model and the remaining devices by digital-mode models.
fig.4.8 Clock-generation circuit (Vss=-5v, Vss2=-15v, Vbias1=-7.5v, Vbias2=-13v)

The complementary clock signals $V_{inp}$ and $V_{inm}$ required by the SCC's are generated at one point on the chip by a clock generator consisting of two identical channels, one for each clock phase, each of which has the structure of fig.4.8. This circuit is essentially a hard-driven long-tailed-pair with diodes to define the low-level output signals to $V_{bias1}$ - 0.6v. The latter method of defining the low level was chosen in preference to using a string of transistors (a) to avoid using a long string of diodes and (b) to allow experimentation with the switch turn-off voltage.

Example switching waveforms are shown in fig.4.9, where the upper trace is the output of an SCC with a signal input voltage of zero volts. The lower two traces are the complementary switching input voltages to that SCC, as generated from the clock-generator circuit of fig.4.8. Now, referring to the circuit of fig.4.1, the switches with quiescent terminal voltages at approximately $V_{ss}$ ($e2$, $e3$, $o1$ and $e5$, $o4$, $o5$) are realised as simple MESFETs switched directly by the clock-generator, while the remaining switches are driven by SCC's, which are in turn driven by the clock-generator $V_{outp}$ outputs. The fact that the clock-generator output is suitable for both of these tasks is a significant economy, and is a consequence of using a single-ended input amplifier, with a quiescent voltage of $V_{ss}$ (so that the switches $e2$ and $o4$ at the amplifier inputs must have one terminal connected to $V_{ss}$). Another attractive feature of the clock waveforms is that the relative timing of the SCC and clock generator outputs is compatible with requirements for minimising distortion due to clock feedthrough, as discussed in [10]. When the findings of the latter work are adapted to the FGI integrator circuit it is found that, for example, the 'turn-on' edge of the $e1$ switch must precede that of the $e2$ & $e3$ switches, while the 'turn-off' edge must follow them. It can be seen from fig.4.9 that this is indeed what happens, and inspection of the SCC and clock-generator circuits shows that this sequence is guaranteed by the switching sequence of the circuits' transistors.
The width of the switch-MESFETs was set to the minimum of 16μ in order to minimise clock feedthrough, this width giving an acceptable on-resistitance of approximately 300Ω (see below). Dummy switches with grounded sources and drains were connected to the $V_{outm}$ outputs of the clock generators in order to balance the load due to switches directly driven by the $V_{outp}$ outputs, thus preserving the balance of the clock-generation circuit. In fact, this balanced switching circuit architecture offers the possibility of cancelling some clock-feedthrough by employing dummy switching devices to inject compensating clock pulses into the signal path, and this possibility may be worth investigating for a future design.

4.2.3 Amplifier Design and Characterisation

For the circuit architecture of fig.4.1 the amplifiers must have a DC gain of about 40dB, and the single-stage single-cascode architecture of fig.4.6 having a single-ended input was adopted. In fig.4.10, the current source load device $F3$ is kept in saturation by its bootstrap transistor $F4$ fed by diode connected MESFETs $F6$, $F7$ & $F8$, and source follower $F12$. The use of diodes for level shifting allows the use of identical minimum size devices for bias MESFETs $F5$ to $F14$, and was adopted in preference to techniques relying on device width ratioing [190]. This strategy is a direct consequence of the modelling work, when it was realised that, since the normal linear dependence of $g_o$ on $I_d$ did not occur in these devices, device ratioing techniques would result in a loss in amplifier gain. The input/output chain in fig.4.10 comprising $F1$-$F4$ determines the amplifier transconductance and slew rate and the gate widths of the devices are defined as an amplifier scaling factor multiplied by the minimum gate width (16
microns). Both of the amplifiers in the final design have a scaling factor of three, the choice of which will be discussed below. From simulations using the analogue-mode model the amplifier DC gain is found to be 36dB, and the bandwidth and phase margin, using 80fF load, are 3.6GHz and 70 degrees respectively. Since the devices in any one column of the amplifier all have the same width, the layout of the amplifier is particularly compact [147].

The amplifier was characterised using the method outlined in chapter 3, and the data produced is discussed in detail in [158]. To summarize, for a unit sized amplifier, defined as having all device widths equal to 16μ:

\[
\begin{align*}
C_{g0} &= 22fF \\
C_{o0} &= 1.9fF \\
g_{m0} &= 1.80(±0.14)\text{mS} \\
\kappa &= 85(±9 / -6)fF / \text{unit}
\end{align*}
\]  

(4.1)

4.2.4 Circuit Optimisation

The above amplifier characterisation data will be used with the formulae of chapter 3 to optimise and compare the circuits of figs 4.1 and 4.2. The parameters used are defined in chapter 3.

*Conventional biquad analysis:* In the e-phase this circuit splits into two single-amplifier networks, and analysis gives:

\[
\tau_1 = 23.4pS, \quad \tau_2 = 35.4pS
\]

(4.2)

where \(\tau_1\) and \(\tau_2\) are defined in (3.16) and \(X_1=X_2=7\) has been chosen for reference. The dual-amplifier network formed in the o-phase conforms to the second special case examined in chapter 3, and so (3.13-3.18) and (3.27-3.29) can be used to show, for \(X_1 = X_2 = 7\):
\[ \tau_+ = 28.2\, pS, \quad \tau_- = 57.5\, pS \]  
(4.3)

which, when compared to (4.2) shows that settling in the o-phase will limit the maximum clock frequency of the circuit. It is also found that:

\[ A = 118\, pS^2, \quad \tau_1 \tau_2 = 1801\, pS^2 \]  
(4.4)

so that the inequality in (3.32) is not obeyed, and coupling between the amplifiers is therefore significant in determining settling times. This was confirmed using Spice simulations. Using numerical optimisation it was further found that:

\[ X_{1\text{opt}} = 37.5, \quad X_{2\text{opt}} = 27.5 \]  
(4.5)

for which:

\[ \tau_- = 36.7\, pS \]  
(4.6)

and it can be seen from fig.4.11 that this is a fairly broad minima. Fig.4.12 plots the effective load on the amplifiers against \( X=X_1=X_2 \), and compares this with the scaling limit, given by the line \( C_{\text{eff}}=\kappa \cdot X \). Points to the right of this line are beyond the scaling limit, and so it can be shown from the graphs that:

\[ X_{1\text{max}} = 2, \quad X_{2\text{max}} = 5 \]  
(4.7)

Fig.4.11a Dominant time constant as function of \( X_1 \) (o-phase, conventional circuit)
That is, it is not possible to scale the amplifiers to the values given by (4.5), and the minimum settling-time of the network is actually set by the tendency for amplifier settling to become underdamped. For the above maximum scaling factors we find:

\[ \tau_\infty = 125 \text{pS} \]  

(4.8)
Fig. 4.12a Effective amp. loads as a function of scaling (conv. circuit, e-phase)
**FGI biquad analysis**: This circuit splits into two single-amplifier networks in the e-phase and forms a dual-amplifier network in the o-phase, and these can be rearranged to conform with the general single- and dual-amplifier network configurations using the 'star-T' transformation shown in fig.4.13 [191].

```
\[
C_{ac} = \frac{C_A C_C}{C_a + C_b + C_c} \\
C_{ab} = \frac{C_A C_B}{C_a + C_b + C_c} \\
C_{bc} = \frac{C_b C_C}{C_a + C_b + C_c}
\]
```

Fig.4.13 Capacitor "star-T" transformation

In the e-phase it is found that:

\[
\tau_1 = 89.0\, pS, \quad \tau_2 = 71.5\, pS
\]  \hspace{1cm} (4.9)
where $\tau_1$ and $\tau_2$ are defined in (3.16) and $X_1=X_2=7$ has again been chosen for reference. The dual-amplifier network formed in the o-phase gives, for $X_1=X_2=7$:

$$\tau_+ = 49.1\, pS, \quad \tau_- = 187.6\, pS$$  \hspace{1cm} (4.10)

so the o-phase settling again determines the maximum clock frequency of the circuit. Using numerical optimisation it was further found that:

$$X_{1\, opt} = 40.0, \quad X_{2\, opt} = 80.0$$  \hspace{1cm} (4.11)

for which:

$$\tau_- = 101.3\, pS$$  \hspace{1cm} (4.12)

and it can be seen from fig.4.14 that this is a fairly broad minima. Fig.4.15 plots the effective load on the amplifiers against $X=X_1=X_2$, as was done for the conventional circuit. From these graphs it can be shown that:

$$X_{1\, max} = 28, \quad X_{2\, max} = \text{unlimited}$$  \hspace{1cm} (4.13)

![Fig.4.14a Dominant time constant as function of $X_1$ (o-phase, FGI circuit)](image-url)
Fig. 4.14b Dominant time constant as function of $X_2$ (o-phase, FGI circuit)

Hence, although it is not possible to scale the amplifiers to the extreme given by (4.11), there is much greater freedom for choosing $X_1$ and $X_2$ than for the conventional circuit. Close examination of the formulae describing the settling times reveals that the feature of the circuit that allows unlimited scaling of amplifier 2 is that $C_{L2}$ is large compared to $C_{f2}$. This has a multiplying effect on $C_{f2}$ which adequately compensates the amplifier.

From fig.4.14 it is seen that the choice $X_1 = X_2 = 20$ gives $\tau = 120\,\mu$s, which is approximately the same as the minimum achievable by the conventional circuit. It is therefore seen that the ultimate speeds of the conventional and FGI circuits are similar, although quite different amplifier scaling factors must be used to achieve these speeds. This indicates that the ultimate speed of the circuits are directly related to the minimum amplifier settling-time (the settling-time at the Scaling Limit), which is the same for both circuits, while the size and complexity of amplifiers required to approach this limit is significantly different. The larger scaling factors required for the FGI circuit are a consequence of the extra circuitry needed to produce the FGI property, and clearly offset some of the advantages in using the FGI approach. The limitations imposed by chip area and power consumption are therefore likely to be important for this design.
Fig. 4.15a Effective amp. loads as a function of scaling (FGI circuit, e-phase)
Further optimisation of the FGI circuit is achieved by treating $C_{h1}$ as a free design variable. Fig.4.16 is a plot of $\tau$ vs. $C_{h1}$ for $X_1=X_2=7$ in the o-phase, and shows that this time-constant is quite sensitive to $C_{h1}$, and a value of 0.4pF was chosen for the design. Although this violates the criteria for minimum phase error for integrator 1, established in chapter 2, the consequent increase in phase error is found from (2.25) to be negligible, and this was confirmed in simulations.
4.2.5 Layout and final design parameters

The circuit was laid out with buffer circuits on both the bandpass and lowpass outputs, occupying a total area of 1mm by 2mm. The buffer design is described in [147]. In addition, individual test circuits for an amplifier, a buffer, a switch and individual FET's were included, so that the final chip area was approximately 4mm².

The size and quality of capacitors were critical factors. Engineers previously involved in GaAs SC work at STC [31,32] had indicated that polyimide overlay capacitors had poor Q-factors, though this observation does not agree with information from other sources [60]. Recent information [185] suggests that packaging may have a large influence on the quality of such capacitors, since polyimide may absorb moisture when exposed to air, thus increasing leakage. Silicon Nitride (Si₃N₄) overlay capacitors were thought to have adequate Q-factors, but the very high capacitance per unit area suggested difficulties in realising the smaller capacitors. Measurements were made to resolve these issues and are described in [23:ch.10]. They indicate that polyimide
capacitors do have an inadequate Q-factor for this application (although hermetically sealed samples were not used for the tests), while Si3N4 overlay capacitors could be used to give a minimum capacitor value of 0.11pF and a Q-factor of approximately 280 at 1MHz. Smaller capacitor values were then achieved by connecting unit capacitors in series. Such a strategy is possible in GaAs because of the very low substrate conductance, which results in correspondingly low parasitic capacitances from the capacitor plates to ground. In spite of this, we decided to increase the minimum capacitor size (C11) from 1/16 units to 1/8 units in order to reduce the length of the series-connected capacitor chain, thus reducing the filter Q from 16 to 8.

| Unit transistor width, microns : 16.00 |
| Unit capacitor size, pF 0.055 (two 0.11pF caps in series) |

**Scaling factor and power budget:**

<table>
<thead>
<tr>
<th></th>
<th>mW/unit</th>
<th># units</th>
<th>scaling</th>
<th>total mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>amp output chain</td>
<td>31.70</td>
<td>2</td>
<td>3.00</td>
<td>190.20</td>
</tr>
<tr>
<td>amp bias chain</td>
<td>63.00</td>
<td>2</td>
<td>1.00</td>
<td>126.00</td>
</tr>
<tr>
<td>buffer output chain</td>
<td>31.40</td>
<td>2</td>
<td>1.00</td>
<td>62.80</td>
</tr>
<tr>
<td>buffer bias chain</td>
<td>63.00</td>
<td>2</td>
<td>1.00</td>
<td>126.00</td>
</tr>
<tr>
<td>clock generator</td>
<td>61.80</td>
<td>2</td>
<td>2.00</td>
<td>247.20</td>
</tr>
<tr>
<td>SCC</td>
<td>34.20</td>
<td>6</td>
<td>1.00</td>
<td>205.20</td>
</tr>
</tbody>
</table>

**grand total** 957.40 mW

**Final capacitor values (#units):**

| C1  | 2.00 | C2  | 2.00 |
| C11 | 0.125| C12 | 1.00 |
| Ch1 | 4.00 | Cm2 | 1.00 |
| C21 | 1.00 | Cm1 | 1.00 |

Fig.4.17 Final design parameters & power consumption for FGI filter

Amplifier scaling was performed by altering only the widths of devices in the output chain, since the size of devices in the bias chains (the rightmost two columns of FETs) had a negligible influence on amplifier properties. The power consumption of the circuit turned out to be a limiting factor on amplifier scaling, as predicted above. It was decided to keep total dissipation below 1W if possible, and this could only be achieved by restricting the amplifier scaling factor to 3. Fig.4.17 shows final design parameters and power budget for the chip. Comparing the scaling factors with the optimum values calculated in the
previous section clearly shows the sacrifice in filter performance due to power considerations.

4.3 Circuit performance

The final circuit design was simulated and compared with the alternative, conventional design using SCiAP [192]. This simulator allows resistors as well as capacitors in the SC circuit simulation, and hence enables the effects of switch on-resistance and amplifier bandwidth to be calculated. The on-resistance of the 16μ FET switching element was estimated from the Vgs=0 curve of the device static characteristic to be approximately 300Ω, and the gain and unity-gain bandwidth of the amplifier (above the dispersion frequencies for \( g_m \) and \( g_0 \)) were found from SPICE simulations to be 36.4dB and 3.6GHz respectively. The unit capacitance size was set at 0.1pF, somewhat larger than the design value of 0.055pF, in order to give worst-case amplifier loadings that account for any inaccuracy in the unit capacitor size and unmodelled parasitics. Using these values with a clock frequency of 250MHz the results in fig.4.18(a) compare the response of the FGI circuit with the ideal circuit response and that of a conventional design using the same switches and amplifiers. The peak of the FGI circuit's response is 0.5dB lower than the ideal, and occurs at a frequency 0.7MHz lower. This compares with a peak 2dB lower than the ideal for a conventional circuit, and a frequency shift of 0.4MHz. The shape and Q-factor of the FGI circuit is therefore clearly better preserved than that of the conventional circuit, though not dramatically so. The larger frequency shift is due to the larger gain error of the Nagaraj 86 integrators compared to the conventional ones, as discussed in chapter 2. The relatively small difference between the FGI and conventional circuits, in sharp contrast to earlier comparisons based on a 6th-order filter (chapter 2), are due to the low order and Q of the test filter. In spite of this, the response of the FGI filter is distinctive enough to demonstrate its finite-gain-insensitivity property in a practical test. Such a verification of correct circuit operation would open the way to it being used in higher-order filters, where the FGI property would give a greater advantage over conventional structures. Operation of the circuit with a clock frequency of 500MHz was also simulated, and the result is shown in fig.4.18(b). This shows that operation up to 500MHz clocking frequency should be possible, giving a bandpass frequency of 40MHz, well in excess of the highest bandpass centre frequency so far achieved by GaAs SC circuits of 12MHz[166].
Additional simulations were performed to find out what effect a higher FET on-resistance, Ron, would have on performance, and fig.4.19 was obtained for the same circuits as in fig.4.18, but using Ron=1kΩ. It is seen that the higher on-resistance has a negligible effect for 250MHz clocking frequency, but causes considerable Q-enhancement for 500MHz. This indicates that the circuit is close to its clocking frequency limit at 500MHz.
A final check on circuit operation was performed with a full SPICE simulation of the 2nd-order filter in the time-domain. The simulated response at one of the amplifier outputs is shown in fig.4.20. Quite large (>1v) spikes are apparent in the guard intervals, due to the small value of the feedback capacitances provided by $C_{m1}$ and $C_{m2}$ in this period. These spikes are insufficient to send the amplifier into saturation, however, and do not appear to slow the settling in the main clock intervals. As discussed above, the worst-case settling is in the o-phase, and in fact the time-constant for settling in this phase is calculated from the formulae of chapter 3 to be 149pS. This compares with a value estimated from the SPICE simulation output of 198+/-14pS which, taking into account the RC time constant for charging of capacitors through the
switches, is in good agreement. It follows that the time for 0.5% settling is approximately 910pS, a value that accords well with the prediction from the SCNAP results of a maximum clock frequency of around 500MHz.

![Voltage vs Time Graph](image)

**Fig.4.20 SPICE simulation of filter operation**

Unfortunately, due to innumerable delays in the circuit fabrication and test-jig manufacture, measured results are not yet available for this circuit. We do hope to have them shortly.

### 4.4. Summary and Conclusions

A new MESFET model that uses different subcircuits depending on the mode of device operation has been used to develop the 2nd-order FGI SC filter proposed at the end of chapter 2. This model has been employed successfully to take account of a number of important device phenomena ($g_m$ & $g_o$ dispersion, device symmetry, early saturation etc.) that critically affect the design but are not integrated into any model supported in a known, available simulator program. New switch-control and clock-generation circuits have been designed using balanced architectures. They have been shown to give output waveforms that efficiently match, both in timing and voltage levels, the requirements of the overall filter. A single-stage cascode amplifier has been designed and thoroughly characterised using the methods described in chapter 3. This allows optimisation of the circuit to take place (also following procedures described in chapter 3) and preferred amplifier scaling-factors and capacitance values to be determined. Final design parameters were then modified to take account of power supply considerations and the low limit on realisable capacitor values. Simulations on the final design predict a maximum clock frequency of approximately 500MHz, giving a maximum bandpass centre-frequency of about 40MHz and significantly exceeding that achieved by other workers to date. Unfortunately, although the
circuit has now been fabricated, it has not yet been possible to confirm this prediction with measurements.

The most important limiting factor on the clocking frequency for this circuit has proved to be power consumption. The figure of nearly 1W for this second order filter is related to the large difference in the maximum and minimum supply voltages, and to the large number of active circuit blocks required when compared to a CMOS implementation. These factors are in turn the result of having only a single device type, which excludes a number of design options, of the low intrinsic gain of the device, which leads to the use of cascoding techniques, and of the MESFET's non-insulating gate, which requires the use of special switch-control and clock-generation circuits. In addition, the device threshold of the process used was considerably higher than that of comparable designs (eg,[166]), and this had the effect of increasing both power supply voltages and power consumption. Thus, although this design exercise has certainly proved the feasibility of very high speed SC circuits using GaAs, it is concluded that advances in process technology are required in order to allow the design of less power-hungry circuits which would be suitable for high-order filter implementations.
5. ANALYSIS OF STRUCTURES FOR ULTRA-NARROW-BAND FILTER SYSTEMS

5.1 Introduction

5.2 N-Path and N-Path Frequency-Translated Filters
5.2.1 Mathematical Description
5.2.2 Nyquist bands
5.2.3 AAF & AIF requirements

5.3 Statistical Properties of UNB Systems
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5.4 Summary and Conclusions
5.1 Introduction

The design issues for narrow-band SC circuits have already been reviewed in chapter 1, where it was shown that, for circuits aimed at ultra-narrow-band filtering (relative bandwidth < 0.1%), the N-path frequency-translated (NPFT) architecture seems the most favourable. It was also pointed out that, while the effects of component tolerances and mismatch were qualitatively understood for these circuits, no quantitative data was available to describe certain critical phenomena. This chapter begins with a more detailed review of the NPFT architecture than was given in the first chapter, and goes on to describe new work on the analysis of important mismatch effects in such circuits.

5.2 N-Path and N-Path Frequency-Translated Filters

5.2.1 Mathematical description

Consider an N-path (NP) filter, the 0th and nth paths of which are represented in the time domain by fig.5.1.

![Fig.5.1 N-path filter in the time domain](image)

![Fig.5.2 Pulse stream representing ideal sampler](image)
The incoming analogue signal, $x(t)$, is sampled by an ideal sampler to give the sampled signal for the $n$th path, $x_{sn}(t)$. The sampling operation is represented by a mixer, where the analogue signal is convolved with a stream of unit-mass pulses, as shown in fig. 5.2, and the sampling instants for each path are staggered by a multiple of $T/N$. We can write:

$$u(t - \frac{nT}{N}) = \sum_{m=-\infty}^{\infty} \delta(t - [m + n/N]T) \quad (5.1)$$

where $\delta(t)$ is the Dirac function, which is equal to unity at $t=0$ and zero elsewhere. Now, it can be shown that [168]:

$$u(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT) = \frac{1}{T} \sum_{m=-\infty}^{\infty} e^{j2\pi mt/T} \quad (5.2)$$

and so:

$$u(t - nT/N) = \frac{1}{T} \sum_{m=-\infty}^{\infty} e^{-j2\pi mn/N} e^{j2\pi mt/T} \quad (5.3)$$

Taking Fourier transforms:

$$U_{\Phi}(\omega) = \frac{1}{T} \sum_{m=-\infty}^{\infty} e^{-j2\pi mn/N} \delta(\omega - 2\pi n/T) \quad (5.4)$$

From figs. 5.1 and 5.2:

$$X_{sn}(\omega) = X(\omega) U_{\Phi}(\omega) \quad (5.5)$$

so

$$X_{sn}(\omega) = \frac{1}{T} \sum_{m=-\infty}^{\infty} e^{-j2\pi mn/N} X(\omega) \delta(\omega - 2\pi m/T) \quad (5.6)$$

$$X_{sn}(\omega) = \frac{1}{T} \sum_{m=-\infty}^{\infty} e^{-j2\pi mn/N} X(\omega - 2\pi m/T) \quad (5.7)$$

Also from figs. 5.1 and 5.2:

$$Y_{s}(\omega) = \sum_{n=0}^{N-1} X_{sn}(\omega) H_{n}(\omega) \quad (5.8)$$

Now, for an ideal filter:

$$H_{n}(\omega) = H(\omega) \quad \text{for all } n \quad (5.9)$$

so that:

$$Y_{s, \text{ideal}}(\omega) = \frac{H_{0}(\omega)}{T} \sum_{n=0}^{N-1} \sum_{m=-\infty}^{\infty} e^{-j2\pi mn/N} X(\omega - 2\pi m/T) \quad (5.10)$$

but:
\[ \sum_{n=0}^{N-1} e^{-j2\pi mn/N} = 1 \quad \text{for } m = kN, \ k \text{ an integer} \]

\[ = 0 \quad \text{otherwise} \]  

so that:

\[ Y_{s,\text{ideal}}(\omega) = \frac{H_0(\omega)}{T} \sum_{m=-\infty}^{\infty} X(\omega - 2\pi mN/T) \]  

Now, the summation in (5.12) is a mathematical expression of the aliasing operation inherent in a sampled circuit, showing that there will be a response at frequency \( \omega \) from all input signals with frequency \( \omega - 2\pi mN/T \), where \( m \) is any integer. However, in this case, because of the factor \( N \) in \( X(\omega - 2\pi mN/T) \), it is seen that the effective sampling frequency of the circuit is \( N/T \), \( N \) times higher than the actual sampling frequency of each path of the filter. This advantageous situation has been produced by outphasing of signals from the different paths of the filter, an action expressed mathematically by (5.11). If the filter paths are not identical then (5.8) becomes:

\[ Y(\omega) = \frac{1}{T} \sum_{n=0}^{N-1} \sum_{m=-\infty}^{\infty} H_n(\omega)e^{-j2\pi mn/N} X(\omega - 2\pi m/T) \]  

and since \( H_n(\omega) \) must now be included in the summation, cancellation of signals with \( m \neq kN \) is no longer exact and (5.11) cannot be used. Finally, to complete the description of filter operation, the effect of the zero-order-hold function is included to give:

\[ Y(\omega) = \frac{\sin(\omega T/2N)}{\omega T/2N} \sum_{n=0}^{N-1} \sum_{m=-\infty}^{\infty} H_n(\omega)e^{-j2\pi mn/N} X(\omega - 2\pi m/T) \]  

When interpreting this expression it should be remembered that \( H_n(\omega) \) is a periodic function in the frequency domain with period \( 2\pi/T \).

### 5.2.2 Nyquist bands

Before further discussion of the implications of (5.14), we shall define variables and introduce terminology that will aid the description of multi-path systems in the frequency domain. The systems to be described have the architecture of figs.5.1 and 5.2.

**Nyquist bands:** It will be useful to divide the frequency axis into bands of width \( \omega_s/2 \), where \( \omega_s \) is the sampling frequency of the path filters, as shown
shown in fig.5.3. These bands will be referred to as the Nyquist bands of the
filter and we shall refer to Nyquist band 1 as the baseband of the path filter.
Hence:

\[ (b_x - 1) \frac{\omega_s}{2} \leq \omega_x < (b_x + 1) \frac{\omega_s}{2} \quad \text{for } b_x \geq 1 \]
\[ b_x \frac{\omega_s}{2} \leq \omega_x < (b_x + 1) \frac{\omega_s}{2} \quad \text{for } b_x \leq -1 \]  \hspace{1cm} (5.15)

where \( b_x \) is band \( x \), \( x \) any integer and may be positive or negative. We
will also define absolute band numbers as follows:

\[ B_x = |b_x| \]  \hspace{1cm} (5.16)

Fig.5.3 Nyquist bands in an N-path filter system with path-filter sampling frequency \( f_s \).

**Input & output bands, \( b_{in} \) & \( b_{out} \)**: The input and output bands of the
filter system are the Nyquist bands in which input signals are applied and
output signals are monitored respectively. It follows that if one is measuring
the alias response of a system then there is only one output band, while there
will be a number of input bands. Conversely, if one is measuring the image
response of a system then there will only be one input band, while there will
be a number of output bands.

**Reference band, \( b_r \)**: The reference band for a simulation or analysis of
an alias or image response is the Nyquist band to which the simulation or
analysis refers. Thus, if the alias response of a system is to be investigated
then the reference band is the band in which output is monitored, while for
an image response the reference band is the band in which input is applied.

**Principal band, \( b_p \)**: The principal band of an NP or NPFT filter is the
band for which the associated AAF and AIF have been designed to give the
main filter response. It follows from this definition that for an NPFT filter
\( b_p > N \).

Note that in designing an NP or NPFT filter one is mostly interested in
finding the alias and image responses with reference to the main passband of
the filter system, and so frequently \( b_r = b_p \). This is not a general rule,
however, and so the distinction between the reference band and the principal band should be maintained. The former is a function of the
analysis in hand, while the latter is a function of the filter system being
An example will clarify these definitions. Consider a single-path bandpass filter \((N=1)\) for which the alias response is to be measured. The baseband filter response is shown in fig.5.4. Note that the response of the filter in this baseband is unambiguous, since there are no alias or image effects produced if only signals within the baseband are considered. Now, the alias response of the filter for input bands 1 to 4 with reference band, \(b_r = 1\) is shown in fig.5.5.

This shows, for example, that an input signal strength \(V_o\) at frequency \(\omega_s - \omega_0\) will produce an output signal at frequency \(\omega_0\) (in the reference band) of strength \(V_o\). (The equivalent diagram for \(b_r=2, 3, \ldots\) would be identical in appearance to fig.5.5, but would require a different interpretation: ie. it would give the response in band 2, 3, ..etc. to inputs from all the other bands.) The principal band has not been specified in this example, but for a conventional single-path filter it would be set to \(b_p=1\), while for an SPFT filter one would choose \(b_p>1\).
To complete this section, we now briefly look at the requirements for anti-alias and anti-image filters in multi-path systems. In fact, since the imaging process is the dual of aliasing, the discussion will concentrate on anti-alias filters, and the differences in the requirements of anti-image filters simply highlighted where appropriate. First, consider the AAF requirement for an ideal 3-path filter based on bandpass path-filters, as illustrated in fig.5.6.

If the effect of path-mismatch on the filter response is also considered then the selectivity of the AAF must be increased in order to reject mirror responses, as shown in fig.5.7. Clearly, to minimise the selectivity required for the AAF, (i) the mirrors must be as weak as possible, (ii) the mirrors must be spaced as far as possible from the main response and, (iii) the alias responses must be spaced as far as possible from the main response. The first goal is achieved by reducing path mismatch as far as is practicable, while the second goal requires $\omega_0 = \omega_s/4$ [118], which can be understood intuitively from inspection of fig.5.6. The third goal is met by appropriate choice of the principal band which, for a simple N-path filter is just a case of choosing the band so that the passband is far enough away from the extended Nyquist frequency, $N\omega_s/2$, to suit the capabilities of the AAF. For an NPFT filter it can be easily verified that the separation between the main response and the nearest alias is maximized if the former is in the band:\

![Diagram of AAF requirement for an ideal 3-path filter with bandpass path-filters.]

![Diagram of effect of path mismatch on the AAF requirement for a 3-path filter with bandpass path-filters.]

Fig.5.6 AAF requirement for an ideal 3-path filter with bandpass path-filters.

Fig.5.7 Effect of path mismatch on the AAF requirement for a 3-path filter with bandpass path-filters.
where \( i \) is an integer and \( b_0 \) is in the baseband of the corresponding \( N \)-path filter and given by:

\[
\begin{align*}
  b_0 &= \frac{N+1}{2} \quad \text{for } N \text{ odd} \\
  b_0 &= \frac{N}{2} \text{ or } \frac{N}{2} + 1 \quad \text{for } N \text{ even}
\end{align*}
\] (5.18)

If the passband of the path-filters is written:

\[
\omega_0 = \omega_s/m
\] (5.19)

then the separation of the centre frequencies of the main passband and the nearest alias is:

\[
\begin{align*}
  \Delta \omega &= \left( \frac{N-1}{2} + \frac{2}{m} \right) \omega_s \quad \text{for } N \text{ odd} \\
  \Delta \omega &= \left( \frac{N}{2} - \frac{2}{m} \right) \omega_s \quad \text{for } N \text{ even}
\end{align*}
\] (5.20)

Thus for maximum separation:

\[
b_0 = \frac{N+1}{2}, \quad m = 4, \quad N \text{ odd}
\] (5.21)

Now, for a principal band on the positive frequency axis, \( b_p \), the passband centre frequency is given by:

\[
\omega_p = \omega_s \left[ \text{int} \left( \frac{b_p}{2} \right) - \frac{(-1)^{b_p}}{m} \right]
\] (5.22)

where \( \text{int}(x) \) represents the integer truncated value of \( x \). This implies that the relative bandwidth of the filter has been increased relative to that of the path-filters by a factor:

\[
k = \frac{\omega_p}{\omega_o} = m \left[ \text{int} \left( \frac{b_p}{2} \right) - \frac{(-1)^{b_p}}{m} \right]
\] (5.23)

or:

\[
k = \frac{m \cdot b_p}{2} - 1 \quad \text{for } b_p \text{ even}
\]

\[
k = \frac{m \cdot b_p}{2} - \left( \frac{m}{2} - 1 \right) \quad \text{for } b_p \text{ odd}
\] (5.24)

and for \( m=4 \):

\[
k = 2b_p - 1
\] (5.25)
$k$ is called the $Q$-enhancement factor (terminology from [118]). The nearest alias response to $\omega_p$ will appear at a frequency which is a reflection of $\omega_p$ through the nearest integer multiple of $N \cdot \omega_s/2$ (the Nyquist frequency of the ideal $N$-path filter). This ‘reflection frequency’ is given by:

$$\omega_r = \frac{N}{2} \omega_s \text{int} \left( \frac{\omega_p}{N \omega_s/2} + 1/2 \right)$$

(5.26)

Now, the distance to the nearest alias is given by:

$$\Delta \omega = 2 \lambda \omega_p - \omega_r$$

(5.27)

so that:

$$\Delta \omega = N \omega_s \frac{\omega_p}{N \omega_s/2} - \text{int} \left( \frac{\omega_p}{N \omega_s/2} + 1/2 \right)$$

(5.28)

Assuming that $N$ and $b_r$ are chosen to maximize $\Delta \omega$, then the nearest alias responses to $\omega_p$ will be approximately equidistant from it, and so $\Delta \omega$ can be used to define an approximate relative bandwidth for the AAF:

$$RBW_{aaf} = \frac{\Delta \omega}{\omega_p}$$

(5.29)

A further factor influencing the choice of $N$ and $b_r$ in a filter is the amount of sample & hold attenuation suffered at the output, as this can reduce the circuit’s dynamic range. This attenuation factor is, from (5.14), given by:

$$\alpha_{sh} = \frac{\sin(\omega_p T / (2N))}{\omega_p T / (2N)}$$

(5.30)

Equations (5.22), (5.24), (5.29) and (5.30) can be used to tabulate values of $RBW_{aaf}$ and $\alpha_{sh}$ for different chosen values of $N$, $b_r$ and $m$. As an example of this, fig.5.8 shows $RBW_{aaf}$ and sample & hold attenuation, $\alpha_{sh}$, plotted against $b_r$ for $N=3$ and $m=4$. Distinctive peaks in both these parameters are apparent, and, in a filter design, a reference band should be chosen that combines a high $RBW_{aaf}$ with a low $\alpha_{sh}$ (ie. $\alpha_{sh}$ as close to 0dB as possible). This choice would usually be made while trying to maintain some minimum $Q$-enhancement factor which, it is seen from (5.24), must increase monotonically from left to right on the chart. Similar charts are shown in figs.5.9 and 5.10 for $N=12$ & $N=25$ respectively. The latter graph is particularly interesting, as $N$ is so high that the $RBW_{aaf}$ and $\alpha_{sh}$ functions...
are quasi-continuous. Several different tradeoffs between $b_r$, $RBW_{aaf}$ and $\alpha_{sh}$ are therefore possible. By choosing $b_r$ near to the first peak in $RBW_{aaf}$ (ie. $b_r = (3N+1)/2=38$) one would minimise the required selectivity of the AAF and also the sample & hold attenuation, but at the expense of the $Q$-enhancement factor. Choosing $b_r = (7N+1)/2=88$, near to the right-hand peak in $RBW_{aaf}$ would maximize the $Q$-enhancement factor, but at the expense of AAF selectivity and sample & hold loss. Finally, choosing the second peak ($b_r = (5N+1)/2=63$) provides a compromise between the extremes just mentioned.

An alternative approach to the design would be to first fix the desired $Q$-enhancement factor, and hence the main passband, $b_p$, then find the value of $N$ to suit the AAF and AIF requirements. A graph supporting this approach is shown in fig.5.11, where the AAF approximate relative bandwidth and the filter system sample and hold attenuation are plotted against the number of paths in the system, $N$, for $b_r=51$, $m=4$.

![Fig.5.8 Relationship between AAF selectivity, sample & hold attenuation and reference band for $N=3$, $m=4$.](image)
Fig.5.9 Relationship between AAF selectivity, sample & hold attenuation and reference band for $N=12, m=4$.

Fig.5.10 Relationship between AAF selectivity, sample & hold attenuation and reference band for $N=25, m=4$. 

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We now consider the effect of mirror responses on the calculations made above. Clearly, strong mirror responses will place additional selectivity constraints on the AAF. If the position of the NPFT response in the reference band is given by (5.19) and \( m \) is set to 4, then it is easy to show that the separation of the nearest mirror from the main response is:

\[
\Delta \omega_m = \omega_s / 2 \quad (5.31)
\]

Let us first suppose that the mirror frequency rejection of the NPFT filter is so poor that the AAF has to be relied upon completely to reject the mirrors. Following the argument used to write an approximate relative bandwidth for the AAF to reject alias responses (equation (5.29)), we can define the approximate relative bandwidth required of the AAF to reject the mirrors:

\[
RBW_{aaf} = \Delta \omega_m / \omega_p \quad (5.32)
\]

A plot of this function against \( b_r \) is shown in fig.5.12 for \( b_r=51 \), demonstrating that under these circumstances the selectivity requirement of the AAF becomes impractical (compare this figure with figs.5.8 to 5.10). It can be concluded that the mirror frequency cancellation in the NPFT filter must be good enough to significantly relax the selectivity requirement of the AAF if
the filter system is to be realizable. The degree of cancellation required will, of course, depend on the specification for stopband attenuation, but one could guess that minimum values would normally lie in the range -30 to -60dB. It is, in fact, the task of the next section to quantify these mirror strengths as a function of path mismatch in NP and NPFT systems.

![Graph showing relationship between AAF selectivity and reference band when mirror components are equal in strength to the main passband.](image)

**Fig.5.12 Relationship between AAF selectivity and reference band when mirror components are equal in strength to the main passband.**

### 5.3 Statistical properties of UNB systems

#### 5.3.1 General

A critical factor in the operation of an NPFT filter is the cancellation of alias components (mirrors) from each of the path-filters. This produces an extended baseband, as explained above, and allows the use of anti-alias and anti-image filters of relatively low selectivity to select the desired frequency components at the filter system input and output. For comparison, an SPFT filter of the same RBW and using the same kernel filters would be required to use anti-alias and anti-image filters with $N$ times the selectivity (see fig.1.24). Path-mismatch in an NPFT filter leads to imperfect alias and image cancellation, however, and the production of mirror components. It will also result in deformation of the passband shape. Considering the demanding nature of a UNB filter specification, it is of utmost importance to accurately quantify the effects of path-mismatch, and the strength of mirror-components...
Modular filter analysis: Statistical information for a filter response may be obtained by performing a Monte-Carlo analysis on a filter circuit [169], where component values are varied randomly in a large set of simulations. However, for a large filter system, such as an NPFT filter, a straightforward Monte-Carlo analysis has a number of drawbacks. Firstly, the complexity and number of components in an NPFT filter makes the computation unwieldy, resulting in long computer run-times and storage requirements. Secondly, an NPFT filter is, in fact, a filter system, made up of a number of filters that are designed separately. It therefore makes sense to analyse the statistical properties of these filters individually, then combine the resulting information in a higher level calculation to obtain statistical data on the complete NPFT system. This modular approach also requires far less computing power than the simple 'brute force' method, as the reduction of the statistical properties of the component filters in the NPFT system to a relatively small number of parameters allows for a much faster analysis. A further advantage of the modular approach is that it allows the sensitivity and tolerance requirements for the path-filters to be accurately specified in advance of their detailed design. With the appropriate tools, one can experiment with the path-filter specification by first setting a nominal, ideal transfer function, then varying its statistical parameters to assess their effect on the NPFT system transfer function, and hence on the yield of an IC implementation. This will reduce the number of iterations required in the design of the path-filters.

High-level filter parameters: The characteristics of a bandpass filter may normally be summarised by a few 'high-level' parameters, such as
centre-frequency, bandwidth, peak-gain, passband ripple, transition-band and stopband rejection. This is illustrated in fig.5.13. Variations in the components of the filter (capacitor values, amplifier gains etc.) will cause each of these parameters to vary. There will in general be correlation between errors in different parameters which will depend on details of the filter design, as will the distribution of these errors. In addition, the errors in underlying component values may have inter-correlations, and these will influence the error distributions in the high-level parameters. These high-level parameters will be referred to frequently in the discussion that follows, as they are the basis of our statistical description for path-filters.

Path-filter centre-frequency mismatch: An important difference between the NPFT and other multi-path filters for narrow-band filtering is the use of a bandpass path-filter, which avoids the serious reductions in dynamic range caused by in-band clock-feedthrough and mirror-frequency components. It also means, however, that one of the principle advantages of other SC NP and PNP structures- the fixing of the passband centre at a known fraction or multiple of a clocking frequency, independent of any capacitor ratio - no longer exists. In assessing the feasibility of the NPFT structures the effect of the inevitable centre-frequency mismatch of the path-filters will be of particular interest.

5.3.2 Analysis Method

A modular approach to the statistical analysis of NP and NPFT systems has been adopted for this work. As discussed above, the statistical properties of the system's path-filters are described by the ideal transfer function plus statistical parameters to describe variations in the characteristic 'high-level' parameters of the path-filters, such as their centre-frequency and bandwidth. This data is then used to compute the response of the complete filter system, taking into account independent random variations in the path-filter transfer functions.

The implementation of this method has required that a special-purpose software program be written, called MONTY, and this will now be briefly described. MONTY consists of a number of discrete programs that are brought together using MSDOS batch files. The inter-relationship between MONTY and its input and output data is shown in fig.5.14.
The program takes as its input the definition of an ideal path-filter response, which is produced by a conventional analysis program, such as SWITCAP or SPICE [170,171]. The other input to the program is the number of paths in the filter system, information on the reference, input and output bands to be used for the analysis, and the statistical data for the path-filters. For the current version of the software, the high-level path-filter parameters that can be varied are just the centre-frequency, peak-gain and bandwidth. Furthermore, the analysis assumes that there is no correlation between errors in these parameters, and that their error distributions are Gaussian. The program input therefore simply indicates which of the high-level parameters is to be varied, and with what standard deviation. Following the discussion in the previous sub-section, it is easy to see that this model of path-filter statistical behaviour is highly simplified. Nevertheless, it will be shown that it produces results from which important conclusions can be drawn.

Having taken its input, the program generates N different path-filter responses by perturbing the ideal response according to the given statistical data. These responses are then combined to compute the overall response of an N-path filter using that particular set of path filters. The ideal path-filter response, $H_{\text{ideal}}(\omega)$, which must be specified only in the path-filter baseband, is input into the programme as a set of data points with the format:

$$\text{frequency}(\text{Hz}) \ \text{gain}(\text{dB}) \ \text{phase}(\text{degs})$$
As mentioned, these points may either be generated 'by hand' or, more commonly, taken from the output of some other programme, such as SWITCAP. Thus, the analysis may be applied to responses of arbitrary shape, and this feature also makes it very easy to "switch path-filters" and investigate the effect on the NP or NPFT system. The format of the programme output is of the form:

\[ \text{input\_frequency(Hz) output\_frequency(Hz) gain(dB)} \]

and the combination of input- and output-frequencies computed depends on the user's specification of the input and output frequency bands, a reference band, and the clock frequency. In the case of multiple input bands, the program computes the output in the reference band for all the specified input bands, thus showing the N-path filter's alias and mirror responses. In the case of multiple output bands being specified, the program computes the baseband response and all its images up to the highest output band.

The perturbation of the path-filter responses is controlled by an error number, \( \varepsilon_n \), which is generated with a Gaussian distribution that has an average value of zero and a standard deviation specified at the input to the programme. To generate variations in the path-filter centre-frequencies the \( n^{th} \) path-filter response is calculated from

\[ H_n(\omega) = H_{\text{ideal}}(\omega(1 + \varepsilon_n)) \]  

(5.33)

Variations in path-filter gain are modelled using:

\[ H_n(\omega) = (1 + \varepsilon_n).H_{\text{ideal}}(\omega) \]  

(5.34)

and in bandwidth:

\[ H_n(\omega) = H_{\text{ideal}}(\omega + \varepsilon_n(\omega - \omega_0)) \]  

(5.35)

where \( \omega_0 \) is the centre frequency of \( H_{\text{ideal}}(\omega) \).

To compute the response of the filter system the program assumes a unit-amplitude stimulus at a frequency, \( \omega_{in} \). It must then compute the filter system response at a frequency \( \omega_{out} \), where \( \omega_i \) and \( \omega_{out} \) are related according to the particular pair of input and output bands being considered by:

\[ \omega_{in} = \omega_{out} - M\omega_s \]  

(5.36)

where:
\[ M = \frac{B_{out} - B_{in}}{2} \text{ for } B_{out} - B_{in} \text{ even} \]
\[ M = \pm \frac{B_{out} + B_{in} - 1}{2} \text{ for } B_{out} - B_{in} \text{ odd} \]  

(5.37)

and the positive sign is taken when \( \omega_{in} \) acts as the independent variable, else the negative sign is taken (when \( \omega_{out} \) is the independent variable). The above expression is fully derived in appendix 4. The filter response can then be derived directly from (5.14), which gives:

\[ H_N(\omega_{in}, \omega_{out}) = \alpha_{sh} \sum_{m=-\infty}^{\infty} \sum_{n=0}^{N-1} H_n(\omega_{out}) e^{-j2\pi mn/N} \cdot X(\omega_{out} - 2\pi m/T) \]  

(5.38)

where \( \alpha_{sh} \) is an expression for the sample and hold attenuation, and where \( H_N \) has been written as \( H_N(\omega_{in}, \omega_{out}) \) to remind us that either \( \omega_{in} \) or \( \omega_{out} \) could be used as the independent variable (they are related by (5.36)). Now,

\[ X(\omega_{in}) = \delta(\omega_{in}) = \delta(\omega_{out} - M\omega_{s}) \]  

(5.39)

so that:

\[ H_N(\omega_{in}, \omega_{out}) = \alpha_{sh} \sum_{n=0}^{N-1} H_n(\omega_{out}) e^{-j2\pi Mn/N} \]  

(5.40)

Since \( H_n(\omega_{out}) \) is periodic in the frequency domain, but is only specified in the baseband of the path-filter, it is computed from:

\[ H_n(\omega_{out}) = H_n(\omega_{out} - i\omega_{s}) \]  

(5.41)

where \( i \) is chosen such that \( (\omega_{out} - i\omega_{s}) \) is in the baseband of the path-filter. If required, the program can suppress the sample and hold attenuation calculation by setting \( \alpha_{sh} \) to unity.
Fig. 5.15a Typical program input and output:
baseband response of ideal 4th order LUT filter

Fig. 5.15b Typical program input and output:
alias response of 3-path filter, $\sigma_f=0.1\%$
Figs.5.15a-c show some typical program input and output data. The path filter baseband response (fig.5.15) is that of a 4th-order LUD ladder with a relative bandwidth of 2% and a clock frequency of 4kHz. The filter was designed using the PANDDA SC-filter synthesis package [172]. This ideal path-filter response was used as the basis of a 5-path filter, and a typical response for reference band 3 when the standard deviation of the path-filter centre-frequencies is set to 0.1% is shown in fig.5.15b. This shows the mirror responses due to inputs in bands 2 and 4 at about 15dB below the level of the main response. The image response, which shows the effect of sample-and-hold attenuation on a number of output bands, is shown in fig.5.15.c. The image responses have all been translated to the baseband for convenience of presentation but would, of course, appear in their respective output bands.

An important element of the software package is the extraction of key information from the NP and NPFT filter system responses, such as those in fig.5.15.b and 5.15.c. Clearly, several hundred graphical representations of filter system transfer functions are of little use. The first attempt at solving this problem was to write a computer program to extract the high-level parameters characterising a response (bandwidth, peak gain etc.) from the MONTY output data. The resulting summary data was collected in a tabular form for statistical analysis, but it was found that even after this extraction process there remained much irrelevant data, and the latter obscured some of the interesting features present in the MONTY output. Also, it quickly became clear that changes in the shape of the passband filter system response
were a far less serious problem than the issue of distortion produced by mirror components, and this is illustrated by figs.5.16a-d.

Fig.5.16a shows the result of extreme mismatch in a 3-path filter where the path-filters are 6th-order elliptic with a 1% relative bandwidth in the baseband. It is the poorest of a set of 10 responses obtained when the standard deviation of the filter centre frequency, $\sigma_{cf}$, was set to 0.5%. Clearly, passband ripple is very large, the bandwidth is approximately doubled and the peak gain is much lower than in the ideal response. In fact, the peak gain in the passband is less than that of the mirror response in band 3, which is indicated at the top of the diagram. Fig.5.16b shows another example response from the same batch, but with significantly better results. Although the centre frequency shows a greater variation than in the previous example, the general quality of the response is much better and this is reflected in a higher peak gain in the passband and weaker mirror responses. Figs.5.16c-d show the two extremes of a batch of 10 responses obtained using the parameters $N=3$, $RBW=1\%$, $\sigma_{cf}=0.1\%$. It is perhaps surprising to see that the quality of the passband response is well maintained even for the worst case in the batch (fig.5.16c), while in the best case it differs little from the ideal. The strengths of the mirror frequency components are still very significant, however, being only 10.4dB below the passband in the first case, and 28dB in the second. The most relevant piece of information that could be extracted from the output data was therefore the peak gains of the mirrors relative to the peak gain of the main response. For these reasons our original data-extraction program was replaced by a simpler routine that computed the peak gain in each of the Nyquist bands of the filter. The output from this program was then fed into a spreadsheet program [173] for further computation on the relative strengths of the mirror responses, and to produce statistical data and graphical output of the results.
Fig.5.16 Effects of path-mismatch in a sample 3-path filter
($f_s=4.0, \text{baseband } cf=1.0, b_r=2$)
5.3.3 Verification of method

Two checks were performed to confirm the accuracy of the MONTY program output, the first based on a known relationship between the alias and image responses of any given filter, the second on a comparison with a statistical analysis of a 3-path filter performed using SWITCAP.

From (5.40) we write an expression for $H_{N}(\omega)$, which excludes the affects of sample and hold attenuation:

$$H_{N}(\omega) = \sum_{n=0}^{N-1} H_{n}(\omega) e^{-j2\pi Mn/N}$$

(5.42)

Now let us consider the relationship between the alias and image responses of a given filter. For the alias response we have $\omega in$ as the independent variable and can write:

$$H_{N}(\omega_{in}) = \sum_{n=0}^{N-1} H_{n}(\omega_{in}+M_{a} \omega_{s}) e^{-j2\pi M_{a} n/N}$$

(5.43)

similarly, for the image response we write:

$$H_{N}(\omega_{out}) = \sum_{n=0}^{N-1} H_{n}(\omega_{out}) e^{-j2\pi M_{i} n/N}$$

(5.44)

Using (5.41), (5.43) and (5.44) can be written as:

$$H_{N}(\omega_{a}) = \sum_{n=0}^{N-1} H_{n}(\omega_{a}) e^{-j2\pi M_{a} n/N}$$

(5.45)

$$H_{N}(\omega_{i}) = \sum_{n=0}^{N-1} H_{n}(\omega_{i}) e^{-j2\pi M_{i} n/N}$$

(5.46)

Taking (5.41) into account it is clear from this that:

$$H_{N}(\omega_{a}) = H_{N}(\omega_{i})$$

(5.47)

for

$$\omega_{a} = \omega_{i} + k_{1} \omega_{s}$$

(5.48)

and

$$M_{a} = M_{i} + k_{2} N$$

(5.49)

where $k_{1}$ and $k_{2}$ are any integers.
Fig. 5.17 SWITCAP output showing relationship between image & alias bands

Fig. 5.18 MONTY output showing relationship between image & alias bands

Now consider the image and alias responses of a filter for which the reference band is chosen, *in both cases*, to be:
where \( N \) is odd. From (5.37) it can be shown that for the image response in band \( b_r-1 \):

\[
M_{d}(b_r-1) = \frac{N-1}{2}
\]  

(5.51)

and for the image response in the same band\(^1\):

\[
M_{i}(b_r-1) = -\frac{N-1}{2}
\]  

(5.52)

Similarly, for the alias and image responses in band \( b_r+1 \):

\[
M_{d}(b_r+1) = \frac{N+1}{2}
\]  

(5.53)

and

\[
M_{i}(b_r-1) = -\frac{N+1}{2}
\]  

(5.54)

both of which satisfy (5.49). Hence, for frequency points that satisfy (5.48), the alias response of the filter in band \( b_r-1 \) should be identical to the image response in band \( b_r+1 \). Conversely, the image response of the filter in band \( b_r-1 \) should be identical to the alias response in band \( b_r+1 \). This observation is also confirmed by the data in the two tables, and has an important consequence. If a filter is designed with \( N \) odd and the principal band is set to \( b_p=(N+1)/2 \), as was shown to be optimum in (5.21), then the peak gain of the strongest alias (mirror) in the two adjacent bands must be equal to the peak gain of the strongest image in the two adjacent bands. Thus the AIF specification for the rejection of residual image responses will be the same as the AAF specification to ensure adequate rejection of the mirrors. Hence, a statistical analysis of the alias response of such a filter applies equally to the image response for this important special case.

The second check was done by comparing results with a statistical analysis of a 3-path filter using SWITCAP. The circuit chosen for the comparison was necessarily simple in order to minimise the time for the SWITCAP analysis, and it is shown in fig.5.19.

\(^{1}\) In fact, it can be shown that, for a given \( b_r \), \( M_a=-M_i \) in any give band.
Fig.5.19 Second-order filter used for SWITCAP simulations to check against predictions of new software.

Now, it is easily shown that for this circuit operated with $\omega_s >> \omega_0$ the bandpass output has a centre frequency:

$$\omega_o = \frac{1}{T} \sqrt{\frac{C_4 C_5}{C_1 C_2}}$$

and a Q-factor:

$$Q = \frac{\omega_o T}{C_3/C_1}$$

For this check, $C_1$ and $C_2$ were set to unity, $Q$ set to 100 and also $C_4 = C_5 = C_E$. The value of $C_E$ was then set individually for each path-filter in each run of the SWITCAP simulator using a random number generator such that the distribution of $C_E$ was Gaussian with a standard deviation of 0.1% and an average value that gave $\omega_s/\omega_0 = 12.5$. From (5.55) above it can be seen that this should give a Gaussian variation of the centre frequency of the path-filters of 0.1%. The SWITCAP input files were set to produce the alias response of the filter where the reference band was chosen as band 3. The peak gain in band 2 of the alias response was then extracted from the data produced, as this represented the peak gain of the mirror component closest to the passband. 100 such peak gain values were collected.
For comparison, the new software took the ideal transfer function of the path-filter in fig.5.19 and also computed alias responses of 3-path filters based on this path-filter, where the standard deviation of the centre frequency of the path-filters was 0.1%. Again, the reference band was set to band 3 and the peak gain of the mirror response in band 2 extracted from the resulting data. A comparison of the results obtained by the two routes is given in fig.5.20, where it can be seen that the distribution of the data are, to a very good approximation, the same. From this it is concluded that the new software is indeed giving accurate predictions for N-path filters where the path-filters have random errors of the type being simulated. As well as producing the same shaped distribution as the SWITCAP simulations, the new software also predicts the same absolute values of the responses. Together with the outcome of the first check, which showed that critical relationships between the alias and image responses of a filter were accurately reproduced, the results verify the accurate functioning of the software.

5.3.4 Results of Analysis
A series of analyses were performed on SC N-path filters using bandpass path-filters with relative bandwidths of 1% and 2%, where the path-filter 'high-level' parameters, centre-frequency, gain and bandwidth, were assigned standard deviations of 0.5%, 0.25%, 0.1% and 0.05%. These figures were chosen as they included in their range specifications already achieved by
example systems (eg. [39]) and also projections of the best feasible performances [125]. The tolerances also correspond to the limits of capacitor ratio accuracy achievable in an IC process [5,6], which is the main factor that determining the accuracies of the centre frequency and bandwidth.

Three types of path filter were used; a 6th-order elliptic type, a 4th order LUD type, and a simple second order filter. The number of paths in the filters were varied between 3, 7 and 15. Each set of 100 data points can therefore be described by 5 parameters, as follows:

<table>
<thead>
<tr>
<th>path-filter type</th>
<th>ELL, LUD or BQD</th>
</tr>
</thead>
<tbody>
<tr>
<td>relative bandwidth</td>
<td>1% or 2%</td>
</tr>
<tr>
<td>$N$</td>
<td>3, 7 or 15</td>
</tr>
<tr>
<td>parameter varied</td>
<td>centre-frequency (cf), gain (pg) or bandwidth (bw)</td>
</tr>
<tr>
<td>standard deviation</td>
<td>0.5%, 0.25%, 0.1% or 0.05%</td>
</tr>
</tbody>
</table>

For each measurement we set $b_r=(N+1)/2$ and $m=4$, in accordance with the criteria for optimum spacing between the alias and passband, as given in (5.21). Using the above notation, fig.5.21 gives a summary of the data to be discussed in this sub-section. The discussion will start by considering only the data produced by peturbing the path-filter centre frequencies.

1 In fact, it is the order, rather than the type of these filters which has most significance. These particular examples happened to be readily available and although for a strict comparison one would be required to keep the filter type constant when varying the order, this shortcoming is not believed to affect the validity of our results.
Perturbation of path-filter centre-frequencies: The results obtained for the case of the 6th order elliptic filter with 1% relative bandwidth and perturbed centre frequencies are tabulated in fig.5.22a and presented graphically in fig.5.22b. The table shows the average peak gain and its standard deviation in the passband, while the level recorded for the mirror components is the difference between the strongest peak of the two mirrors closest to the passband and the peak gain in the passband.

As explained earlier, this parameter is chosen since it is the one that most affects the selectivity requirement for the AAF. The two columns to the far right of the table give some information about the distribution of the data points, the first column giving the percentage of responses where the mirror rejection was better than average, while the second shows the percentage where the mirror rejection was better than the average plus one standard deviation.
We begin our discussion of these results by first noting the latter distribution data, which indicates a slightly non-Gaussian distribution. Examples of this are shown in figs.5.23 and 5.24, which are representative of all the data collected. For a precisely Gaussian distribution the number of responses with a better-than-average mirror-rejection would be exactly 50%, and the number with rejection better than the average plus one standard deviation would be 84.1% [205]. By comparison, our average values, for 1200
data points, are 44\% and 86\% respectively. The reason for this is that, although the perturbations to the individual path-filter centre-frequencies have a Gaussian distribution, they are combined non-linearly by (5.40) to give the filter system transfer function. Taking this distribution data into account, the vertical axis for the plot in fig.5.22b has been set to the average of "max_mirr-pg" plus one standard deviation of "max_mirr-pg", with the resulting figure being termed "mirror_rejection". That is:

\[
\text{mirror_rejection} = \text{avg}(\text{max_mirr-pg}) + \sigma(\text{max_mirr-pg})
\]  

(5.57)

This means that the points on the plot represent the mirror rejection that will be achieved by 86\% of a typical sample, and this is chosen as a reasonable measure of the filters' mirror-rejection characteristics. In terms of implementation, this means that if a UNB filter system is designed to accommodate the mirror rejection given by this plot, then, all other process-related factors being ideal, the yield would be 86\%.

Fig.5.23 Distribution of data points for ELL, cf, N=7, σcf=0.25\%
The horizontal axis of the graph is plotted on a log scale, as this brings out the linear relationship between the mirror rejection and the standard deviation of the error in the path-filter centre-frequencies. The unity slope indicates that doubling the standard deviation will halve the mirror rejection, which is an intuitively reasonable result. The graph also shows that, for a given standard deviation, the mirrors are weaker for larger \( N \). This shows that, all else being equal, the likelihood of good cancellation of the mirror components increases as \( N \) increases, which is also intuitively reasonable.

Taking some specific examples from the graph data, it can be seen that a 3-path filter where the path-filter centre-frequency accuracy is +/-0.1\% has, for a guaranteed yield of 86\%, a mirror rejection of about -5dB. For a 15-path filter this figure improves to -13dB. Extrapolating from the graphs, an \( N=3 \) (resp.\( N=15 \)) filter where 86\% of the circuits have a mirror rejection better than 20dB requires \( \sigma_{cf}=0.015\% \) (resp.0.051\%). For a rejection of 40dB this figure becomes 0.0011\% (resp.0.0054\%).
Fig. 5.25 shows data collected under the same conditions, except that the relative bandwidth of the path filters is doubled to 2%. Comparing this with fig.5.22b it is seen that the 2% relative bandwidth data consistently has 6dB more mirror rejection that the 1% relative bandwidth data. This implies that the mirror rejection for a given type of path-filter is a linear function of the ratio of the path-filter centre frequency error and the relative bandwidth of the path-filter. It would be interesting to find out under what conditions this relationship holds. When they do hold, fig.5.22b could be used as a normalised graph to look up the expected mirror rejection for path-filters of different bandwidths by shifting the x-axis appropriately.
At this stage it is useful to introduce data that can be directly related to a filter that has been fabricated. Careful examination of the paper by Song & Gray [131], which concerned the fabrication of a 6th-order SC bandpass filter with a $Q$ of 55 (relative bandwidth = 1.8%) suggested that the standard deviation of the mean centre frequency for the filter was between 0.17% and 0.25% (It is difficult to be more precise than this since, although the paper quotes a 'Centre Frequency Accuracy' of +/-0.5%, examination of the relevant figures suggests that this figure corresponds to between 2 and 3 standard deviations). The corresponding normalised values of $\sigma_{cf}$ are 0.09% and 0.14% and so, from the graph of fig.5.22b, this indicates that, if this filter had been used as a path-filter in an $N$-path filter, then the mirror-rejection would probably have been between 5.5dB and 12dB for $N=3$, or between 13dB and 20dB for $N=15$. This clearly does not represent good cancellation of the mirror components by the $N$-path filter, and the AAF in a system that used such a path filter could not rely on partial mirror cancellation to relax its specification significantly. The cancellation is particularly poor for low values of $N$. 

Fig.5.26 Graph for LUD,cf,2%
Next, compare the data in figs. 5.25, 5.26 and 5.27, which are all for path-filters of 2% relative bandwidth, but with each using a different type of path-filter. As before, all the data lines have unity slope, and so attention is focussed on the absolute levels of mirror rejection in each case. It is found that for the $N=3$ responses, the mirror rejection of the LUD-based filters are 2.9dB lower than those for the ELL-based filters, while the BQD-based filters have mirror rejections that are on average 6.3dB below those for the LUD-based filters. Clearly, the type and order of the path-filters has a significant influence on their mismatch sensitivity, with higher order filters being more sensitive.
Perturbation of path-filter gain & bandwidth: Figs. 5.28 and 5.29 present data for variations of the path-filter gain and bandwidths respectively. A linear relationship between the mirror rejection and the standard deviation of the errors in the path-filters is again seen in both the graphs, as it was for the data from centre-frequency perturbations. Comparing the data in fig. 5.28 with that in 5.22b, it is seen that the mirror rejection is 50-60dB better for a given standard deviation in the path-filter error, clearly showing that the $N$-path response is far less sensitive to path-filter gain and bandwidth variations than it is to variations in the path-filter centre-frequency.

![Graph for ELL, pg, 1%](image)

Fig. 5.28 Graph for ELL, pg, 1%

<table>
<thead>
<tr>
<th>$N$</th>
<th>sdev%</th>
<th>$20\log (s_d)$</th>
<th>avg</th>
<th>stderr</th>
<th>avg</th>
<th>stderr</th>
<th>avg+stderr</th>
<th>$% &gt; \text{avg}$</th>
<th>$% &gt; \text{avg+stderr}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0.50</td>
<td>-6.02</td>
<td>-0.23</td>
<td>0.00</td>
<td>-46.77</td>
<td>5.48</td>
<td>-41.29</td>
<td>41</td>
<td>91</td>
</tr>
<tr>
<td>3</td>
<td>0.10</td>
<td>-20.00</td>
<td>-0.23</td>
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<td>-60.11</td>
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avg: 42  87

Fig. 5.29 Table of data for ELL, bw, 1%
5.4 Summary and Conclusions

The effect of path-filter mismatch in NP and NPFT systems has been described and the consequences for the selectivity specification of the AAF and AIF in such systems discussed. It was seen that the level of mirror and residual image-frequency components in Ultra-Narrow-Band systems might have a large impact on this selectivity specification. Following these observations, a general statistical analysis of the effects of path-mismatch in NP and NPFT systems has been described, based on purpose-built tools that allow the effect of many different system parameters to be readily evaluated.

The data presented here has allowed us to make several observations for the N-path model used in the analysis, where the effects of path-filter centre-frequency, gain and bandwidth errors were isolated, and where a Gaussian error distribution in these high-level parameters was assumed. They are:

i. the mirror rejection is a linear function of the standard deviation in the error of the parameter that is varied.

ii. for a given filter, the mirror rejection improves as \( N \) is increased.

iii. the ratio of the standard deviation of the path-filter centre-frequency error to its relative bandwidth seems to be a critical factor in determining the mirror rejection.

iv. all other things being equal, the strength of mirror components increase when the order of the path filters is increased.

v. the N-path mirror rejection is far more sensitive to variations in path-filter centre-frequency than to variations in path-filter gain or bandwidth.

In addition, it was shown by reference to data from the literature on example realisations that the expected mirror-component levels in practical NP and NPFT systems would be very significant. The levels expected would certainly require that the associated AAF and AIF be designed to give significant rejection of the mirrors, which would dramatically increase their selectivity specification. In conclusion, therefore, it seems that the problem of sensitivity to variations in the path-filter centre-frequencies will be an important one when using NP and NPFT structures for the realization of UNB filter systems, and that this is particularly significant for systems with low values of \( N \).
6. NEW CIRCUITS FOR ULTRA-NARROW-BAND FILTER SYSTEMS

6.1 Introduction

6.2 N*M-path Frequency-Translated Filters
6.2.1 N*M-path filter scheme
6.2.2 Non-ideal effects in pseudo-M-path filters

6.3 Reduction of non-ideal effects in pseudo-M-path filters
6.3.1 General
6.3.2 Same-Sample-Correction (SCC) FGI circuits
6.3.3 Symbolic Analysis of SCC circuits
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6.4 Summary & Conclusions
6.1 Introduction

The previous chapter has shown that the design of an NPFT filter is considerably hampered by the high sensitivity of mirror and image components to centre-frequency mismatch of the path filters. In this chapter we will propose and investigate a new circuit architecture that overcomes these mismatch problems. The new architecture requires the use of pseudo-N-path (PNP) filters, and so the non-ideal properties of these circuits are reconsidered in this context. Although the noise characteristics of PNP circuits are known to be poor when compared to equivalent N-path circuits [143], it will be shown that the noise performance of the new architecture will not be degraded by the use of PNP filters. The deleterious effects of amplifier gain and bandwidth on the new system are potentially serious, however, and so work on the development of new PNP circuits with reduced sensitivity to amplifier gain is described. Novel circuit techniques are introduced and new circuits with dramatically reduced sensitivity to amplifier gain presented.

6.2 N*M-path Frequency-Translated Filters

In the context of the new N*M-path configuration, we will henceforth refer to pseudo-M-path (PMP), rather than pseudo-N-path (PNP), filters. Thus, in an N*M-path filter (see below), the N will always refers to the number of paths in the main filter, while the M will refer to the number of pseudo-paths in the path-filters.

6.2.1 N*M-path filter scheme

![Diagram of N*M-path filter system](image)

fig.6.1 (a) conventional NPFT filter system, (b) N*M-path filter system
In this subsection we explore the possible advantages of a new type of NPFT architecture [149], where the path-filters of the standard NPFT system are replaced with pseudo-M-path filters, as shown in fig.6.1. We call the new arrangement an N*M-path architecture, and it differs from the original NPFT system in that the bandpass responses of the path-filters are now generated by frequency-translation of a lowpass response, as can be understood from the background information on pseudo-M-path filters given in chapter 1.

An example N*M-path filter, with N=5 and M=4, is shown in fig.6.2c, and the detail of its path-filters is given in figs 6.2b and 6.2c. Note that the switch labelling of x and y phases relates to the clocking scheme of fig.6.2, so that each path-filter uses a different pair of clock signals. In line with the terminology of the previous chapter we define the circuit in fig.6.2b as the kernel filter, which in this case is second order. The pseudo-4-path path-filters therefore have a 4th-order bandpass response at $f_s/4$, where $f_s$ is the single clock frequency of the system.

The important advantage of this new arrangement, compared to the conventional system where single-path bandpass path-filters are used, is that
ideally the centre-frequency of the path-filter responses depend only on the clock frequency, $f_s$ [119,123], which is common to all the path-filters. In fact, these centre frequencies will also have some dependence on circuit capacitance values when amplifier characteristics are non-ideal, but this dependence is weak (see below). Following the findings of the previous chapter, ie. that sensitivity to path-filter centre-frequency mismatch is an important limiting factor for an NPFT system, it is seen that the new N*M-path architecture substantially improves the potential of a filter system for UNB applications.

Differences in the frequency responses of the NPFT and N*M-path systems are illustrated in fig.6.3. In fig.6.3a-b the schematic baseband responses of conventional single-path and pseudo-4-path path-filters are shown. Figs.6.3e-f compare the alias responses of two 5-path filters using the different path-filters, where the reference band is taken as band 3.

Note that the pseudo-M-path path-filter produces twice as many mirror components as the single-path path-filter due to the unwanted responses at DC and $f_s/2$ in its baseband. It has been shown by Patangia [174,175], however, that it is possible to remove unwanted responses at even multiples of $f_s/2$ by a simple modification of the pseudo-M-path cell, effectively giving a cosine filter in series with the pseudo-M-path filter, as illustrated by figs.6.3b-d. With such a modification the pseudo-M-path filter has the same baseband response as the single-path filter, so that the 5*4-path filter has the alias

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response shown in fig.6.3g. This is identical to the schematic frequency response of the conventional 5-path filter (fig.6.3e), but with the important difference that the mirror responses are substantially reduced due to the improved matching of the path centre-frequencies. Following the findings of the previous chapter, it can be seen that this improvement applies to the reduction of the partially-cancelled image responses also.

The PMP filters can have any of the several known architectures considered in sub-section 1.5.2 [124,176,177,178], but a particularly suitable choice seems to be that of the circulating-delay architecture shown in the example [119]. This not only has the advantages of zero in-band clock-feedthrough and mirror components, but also has a clocking scheme well suited to incorporation in the N*M-path structure. If, as in the example given, an N*M-path filter has M=N-1 then the clocking-scheme for the whole filter is exactly the same as that for a single pseudo-M-path filter.

This chapter will concentrate on the two most widely known types of PMP filter in order to establish general results and design techniques which could later be adapted to other architectures. We therefore review some of the non-ideal effects that beset the Circulating-Delay- and RAM-type PMP cells already introduced in fig.1.17 and fig.1.18 (chapter 1), assessing them in the light of the proposed new mode of operation.

6.2.2 Non-ideal effects in pseudo-M-path filters

**Amplifier limitations:** If an amplifier is not slew-rate limited, then the main limitations on its performance will be caused by its DC gain, $A_0$, its gain-bandwidth product, $GBW$, its internal noise and its input-referred offset voltage. The effect of the amplifier's DC gain and gain-bandwidth product is to limit the accuracy of every charge-transfer operation. This limitation is particularly important in PMP filters since the number of charge-transfer operations per amplifier per unit time is significantly greater than in an N-path filter performing the same function. This difference with the equivalent N-path circuit is caused by the need to store and retrieve charges on the integration capacitors in the PMP circuit, operations that are not required in the N-path case. Of the other effects, amplifier noise is usually not as important as the $kT/C$ noise associated with the switches and capacitors (dealt with below), and the effect of the input-offset voltage will be automatically reduced, without extra component cost, if any steps can be taken to reduce the sensitivity to amplifier gain [152].

The choice of bandwidth for an amplifier involves a tradeoff between the accuracy of the charge transfer operations, which benefit from a high bandwidth, and the circuit noise levels, which can be reduced by lowering bandwidth [2]. Given an appropriate choice, however, charge-transfer
accuracy is still limited by the DC gain of the amplifier. In conventional single-path SC circuits, amplifier gains of 60dB normally give acceptable filter performance [2], but the situation is different in PMP filters, and fig.6.4 shows the response of a pseudo-7-path filter using circulating-delay-type cells and 60dB amplifiers. It has an extra in-band insertion loss of 2.0-3.5dB, as well as significant distortion of the passband shape. This degradation would increase for larger M [119] and therefore represents a limiting factor in the achievement of narrow relative bandwidths. Further data on these effects is given by Palmisano et al [179], where it is shown that, although the sensitivity of the centre-frequency to amplifier gain is low, its effect on passband gain and Q is very significant. The influence of amplifier gain on PMP circuits has been analysed [119], and shows that the resultant error increases linearly with the number of pseudo-paths for a Circulating-Delay-type cell, whereas it is constant in a RAM-type cell, and in both cases it is higher than in the corresponding N-path filter. These differences are related to the number of charge transfers occurring per unit time in the two types of circuit and highlight the importance of this parameter to filter performance. It has been shown that the amplifier gain required to reduce these effects to negligible levels is of the order of 80-90dB for a 3-path Circulating-Delay filter [179], and it will be even higher for larger M. Such gains are difficult to realise in FET technologies, and must be bought at the expense of amplifier bandwidth and dynamic range. The alternative RAM-type filter, if based on a lowpass kernel, is unsuitable for most applications due to problems of in-band clock-feedthrough (discussed in chapter 1). Even if a high-pass kernel filter is used, however, finite amplifier gain and bandwidth allow storage capacitors to affect the transfer function, causing in-band mirror components. This leads to an unacceptable loss of dynamic range in many applications [119], and effectively makes finite-gain effects just as onerous in the RAM-type as in the Circulating-Delay-type circuits.

In spite of the high sensitivity of the passband gain and Q to amplifier gain, the sensitivity of the centre-frequency to this parameter is still very low. In the response of fig.6.4, for example, the centre frequency is within 0.027% of the ideal. Furthermore, it is not this deviation from the ideal centre frequency, but rather the difference in the centre-frequency deviations of each path, which will determine the quality of the N*M-path filter. To quantify this, the example pseudo-7-path filter was simulated to find its maximum and minimum centre-frequencies when the gains of the two amplifiers, A1 and A2, say, were varied between 900 and 1100 - a worst-case amplifier gain of 1000+/-10%. The maximum and minimum conditions were found to be A1=900, A2=1100 and A1=1100, A2=900 respectively, and the centre-
frequencies under these two conditions differed by only 0.013%. Further relevant data is to be found in reference [179], where it was shown that in a 3-path circulating-delay filter based on a first-order lowpass circuit, an amplifier gain of 1000 produced a shift in centre frequency from the ideal of only 0.05%. Furthermore, from the given graphical data, it can be calculated that for $A=1000\pm10\%$ the centre frequency variation is $\pm0.005\%$ (consistent with the values obtained for the example above) and that the rate of change of centre-frequency with bandwidth is negligibly small, provided the nominal amplifier bandwidth is sufficiently high with respect to the clocking frequency.

![Diagram](image)

**Fig.6.4** Simulated response of a circulating-delay-type pseudo-7-path filter, second-order lowpass kernel, amplifier gain 60dB.

These findings indicate that, given normal amplifier tolerances, the centre-frequency matching of PMP bandpass filters is considerably better than could be achieved for conventional single-path filters, where centre frequencies cannot normally be made more accurate than approximately $\pm0.1\%$ (see chapter 5). In order to further quantify this improvement it would be necessary either to do practical tests, or to do Monte-Carlo simulations to obtain detailed statistical information on the variation of the centre frequency of a pseudo-M-path filter for different distributions of amplifier gain and bandwidth. Even without such additional data, however, it is clear that the use of a PMP filter within an N-path structure will substantially reduce mismatch of the path-filter centre frequencies. The high sensitivity of the
passband gain and $Q$ remains, however, and this problem is returned to below.

**Noise limitations:** One of the major drawbacks attributed to PMP filters is a poor noise characteristic when used to realise narrow-band filters [143], and this has led several groups of workers to disregard them in certain applications [118,122]. The analysis presented by Nossek showed that a PMP filter based on a first-order kernel, realising a second-order bandpass function, has a noise level that is significantly worse than that of the first-order kernel filter [143]. By contrast, an N-path filter realising the same second-order bandpass function would have identical noise characteristics to the first-order kernel filter [2]. In an N*M-path filter, however, we are interested in comparing the noise level in the PMP filter with that in a single-path filter that has the same bandpass characteristic, since the basic feature of an N*M-path filter is that the single-path filter has been replaced by a PMP filter, and we wish to ensure that this substitution does not degrade noise performance (and hence dynamic range). We therefore compare the noise levels in a PMP filter based on a first-order kernel with that of a second-order single-path filter and show that this comparison places the PMP structure in a favourable light. Hence a meaningful comparison with Nossek's results can be made.

The noise at the output of an SC filter is made up of two components - a 'direct component' and a 'sampled-and-held component' [180]. The direct component is simply the result of all noise sources at the circuit output during the output-sampling-phase (OSP). It is calculated by first computing the transfer function from all noise sources to the output during the OSP, multiplying them by the spectral density of the sources, then summing appropriately. The sampled-and-held component of the noise is that noise which is sampled onto the capacitors in the circuit in any phase other than the OSP. This is then transmitted to the output according to the z-domain transfer-function from each capacitor to the output in the OSP. The calculation of the sampled-and-held noise therefore requires, firstly, the computation of the continuous-time transfer-function from every noise source to every capacitor in every clock phase other than the OSP, then the computation of the z-domain transfer-function from every capacitor to the output, again for every clock-phase other than the OSP.
The noise calculations must also take into account the bandlimiting effects of the RC networks and the amplifiers, as well as aliasing of wideband noise due to undersampling by switch action. It is also important to accurately model the amplifier characteristics in the circuit; the results obtained for amplifiers modelled as Voltage-Controlled-Voltage-Sources and Voltage-Controlled-Current-Sources may be quite different, for example [104]. Fortunately, the comparison that we wish to make may be done using a few, simple calculations that give some insight into the factors that effect the relative noise performance of the circuits. The circuits to be compared are shown in fig.6.5a-b and, with the component values shown, they have similar bandpass characteristics centred at 1kHz.

For the first step in the analysis we will show that the direct component of the in-band noise is much smaller than the sampled-and-held component in the PMP circuit. The circuit formed by the PMP filter in phase 1 is shown in fig.6.5c, where the switches are shown in series with their independent
equivalent noise sources, each with rms amplitude $V_n$. The resistance $R_{on}$ would typically be of the order of 1kohm, while the unit capacitor value will be of the order of 0.1 to 1pF, and so at the frequencies of interest (around 1kHz) the impedance of the switches in series with the capacitors is approximately equal to that of the capacitors alone. It is then a straightforward matter to show that the direct output noise voltage is:

$$V_{n,dir} = V_n \sqrt{2} \quad (6.1)$$

Nossek has shown that, at the filter centre frequency, the noise sources of the switches $s7\_0$, $s8\_0$ and $s9\_0$ are enhanced by by a factor $\alpha \sqrt{3}$, where $\alpha$ is the capacitor spread, $C_x/C_0$, and the switch $s_{x,y}$ is that which connects nodes $x$ to $y$. This means that the sampled-and-held noise from just one of the sources at this frequency is given by:

$$V_{n,sh} = \frac{C_x}{C_0}V_n \sqrt{3} \quad (6.2)$$

which is much greater than $V_{n,dir}$. This shows that, for frequencies of interest, the sampled-and-held noise is far larger than the direct noise in the PMP circuit. In order to show that the total noise level in the PMP circuit is no worse than that in the single-path circuit, it will therefore be sufficient to show that the total sampled-and-held noise in the PMP circuit is less than that in the single-path circuit.

<table>
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<th>Single-path filter:</th>
<th>Pseudo-3-path filter:</th>
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<tbody>
<tr>
<td>switch</td>
<td>$V_n^2$</td>
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<tr>
<td>$s1_12$</td>
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</tr>
<tr>
<td>$s13_0$</td>
<td>2294.4</td>
</tr>
<tr>
<td>$s10_0$</td>
<td>2190.2</td>
</tr>
<tr>
<td>$s16_0$</td>
<td>2190.2</td>
</tr>
<tr>
<td>$s17_18$</td>
<td>2190.2</td>
</tr>
<tr>
<td>$\sqrt{\sum V_n^2}$</td>
<td>94.2</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>$\sqrt{\sum V_n^2}$</td>
<td>48.3</td>
</tr>
</tbody>
</table>

Fig.6.6 Comparison of noise transfer functions from sources to output in PMP and single-path filters

To simplify the analysis, we assume that the noise enhancement factor due to undersampling of wideband noise is similar in both circuits, as this
allows us to compare the circuits using their baseband responses only. We therefore compute, using SWITCAP, the output noise in the OSP due to the noise-source of each switch during its on-phase, with the exception of the switches that are actually on during the OSP. The results of such a computation are shown in fig.6.6, which show that, for the single-path filter, the noise transfer function from all the e-phase switches to the o-phase output, with the exception of s11_12, are greater than 30dB at the filter centre-frequency. The reason for this high value can be understood qualitatively by considering, for example, the relative effects of noise from the s11_12 and s13_0 switches. Clearly, at the centre-frequency, the transfer-function from the s11_12 source to the output will be unity, since it is in series with the actual filter input. Now, noise from the s11_12 switch enters the circuit via the C11 capacitor, which converts the sampled noise voltage into a charge packet which is then transferred to C1 in the o-phase. Similarly, noise from s13_0 enters the circuit via the C11 and C21 capacitors and is transferred onto C1 in a subsequent o-phase but, in a given e-phase, the charge packet created on C21 is considerably larger than that on C11, due to the relative size of the capacitors. The transfer function from the s13_0 noise source to the output will therefore be greater than that due to the s11_12 source by a factor approximately equal to the ratio C21/C11 (ie. 50).

In the PMP circuit, this same mechanism explains the relative noise outputs due to s1_2, s3_0, s7_0, s8_0 and s9_0, where the capacitor ratio is smaller, at 16. The switches s6_5, s7_5 and s8_5 contribute nothing to the sampled-and-held noise figure since they do not cause a noise signal to be sampled by any capacitor. This can be verified by calculating the noise output due to a source in series with a feedback capacitor around an amplifier; it is found that the noise output equals the source voltage, implying that the voltage drop across the capacitor (ie. the noise sampled onto the capacitor) is zero.

The tables finally show the total sampled-and-held noise in the two circuits (assuming that all sources are independent), and it is seen that the figure for the pseudo-3-path circuit is approximately half that in the single-path circuit, proving that the overall noise level in this PMP filter is certainly no worse than in a single-path circuit performing the same function. This result indicates that the replacement single-path path-filters with PMP filters, in order to create an N*M-path structure, should create no additional noise problems.

Conclusions: The proposed new N*M-path filter structure overcomes problems associated with centre-frequency mismatch in the bandpass path-filters of NPFT systems, but introduces new non-idealities, associated with the
use of PMP filters in the structure. We have shown, however, that the level of noise in a narrow-band PMP filter is typically no worse than in an equivalent single-path circuit, and that noise problems in PMP filters do not compromise N*M-path systems. The effects of amplifier gain on passband gain and $Q$ in a circulating-delay PMP filter, and on the strength of mirror frequencies in a RAM-type PMP filter, have been shown to be significant, however. The next sub-section will therefore introduce new circuits that significantly reduce the effects of finite amplifier gain on the performance of PMP filters.

6.3 Reduction of non-ideal effects in pseudo-M-path filters

6.3.1 General

Following the experience gained with the design of integrator stages suitable for the implementation of GaAs circuits, described in chapter 2, we apply some of the same techniques to the design of PMP filters with low sensitivity to non-ideal amplifier effects. Following the results of that previous work on FGI circuits, it was expected that the effects of finite amplifier gain could be reduced, resulting in FGI PMP circuits. It should be noted that such structures may be useful not only for narrowband, recursive filters, but also for FIR structures, where the circulating storage capacitors may be used to form a tapped delay line [181].

6.3.2 Same-sample-correction (SSC) FGI circuits

To explain the operation of the new circuits we first describe an intermediate development, shown in fig.6.7. This is a PMP integrator based on the single-path FGI integrator of Nagaraj [89], the properties of which were explored in chapter 2. Consider the operation of the circuit under steady-state conditions with $\omega T << 1$, where $\omega$ is the signal frequency and $T$ the period for the 1, 2, 3 and 4 clocks. In this case the circuit output voltage will change little from one clock phase to the next, and the charges held on the storage capacitors will therefore be close in value. Now, in the $o$-subphase the $C_h$ capacitor will sample the error-voltage at the virtual-earth terminal of the amplifier:

$$\epsilon = -V_o(t_o)/A$$  \hspace{1cm} (6.3)

In the subsequent $e$-subphase the right-hand plate of the $C_h$ capacitor is isolated, so the charge on it cannot change, and it follows that the voltage at node $X$ is:
For $\omega T<<1$ we have $V_{o(t_0)} \approx V_{o(t_0)}$, as explained, so that $V_x$ is much less than the amplifier's virtual-earth voltage. Node X therefore acts as a 'super-virtual-earth', and charge-transfers via that node in the e-subphase have reduced error. However, although this action endows the circuit with the FGI property for low signal frequencies (ie. $\omega T<<1$), the essence of a PMP filter is that it produces bandpass responses at sub-multiples of the clocking frequency, ie. $\omega_0 \sim 2\pi k/NT$, $k$ an integer $\leq N/2$. Hence, the condition $\omega T<<1$ does not hold in the critical passbands, and the error-compensation mechanism breaks down.

Now, it was shown in chapter 2 that the FGI property of the single-path Nagaraj integrator did not in fact depend on the condition $\omega T<<1$ - an important advantage of the structure over alternative FGI integrators. The pseudo-M-path adaptation of this filter has lost this desirable property, however, and the reasons for this may be understood from the detailed analysis of the Nagaraj circuit in section 2.4.3. It is shown there that the low phase error of the single-path integrator is due to the stored charge on the integration capacitor being corrected from cycle to cycle so that, for an analysis to first order in $1/A$, the amplifier gain, $A$, causes no charge loss from the integration capacitor from cycle to cycle. In the PMP circuit, however, the integration capacitors are changed on each clock phase, and so the correction mechanism is destroyed unless the integration capacitors all hold approximately the same charge. This condition is only met when $\omega T<<1$.

![Fig 6.7 Prototype FGI PMP integrator](image-url)

To have effective error-correction at all signal frequencies an FGI PMP circuit must obtain an error-correction voltage that relates to the amplifier output voltage being computed in the current clock phase. This will allow any error in the charge stored on the integration capacitor to be corrected before that capacitor is exchanged for another storage capacitor in the next
clock phase. This poses a tricky problem, since the error-voltage is itself to be used in the computation of the amplifier output, and cannot be obtained before that output has first been computed. The conflict is resolved by basing the computation of the error-voltage on an estimate of the amplifier output for each clock phase, which must be computed in the first half of that phase. To do this, the original clock phases must be split into two sub-phases and the circuit must give two outputs in each sampling-period. The output in the first sub-phase has low accuracy, and is used to calculate an error-voltage; the output in the second sub-phase benefits from a correction based on the error-voltage, and is highly accurate.

A circuit which will do this is shown in fig.6.8. It has been developed from the previous circuit of fig.6.7, but it can be seen that most of the capacitors and switches in the circuit have been duplicated in order to enable the computation of an extra output voltage and, hence, an accurate error-correction voltage. The operation of the circuit is as follows. During phase e, the upper section of the circuit, whose elements ideally match those of the lower section, computes an estimate of the amplifier output, $V(t_e)$. At the same time an error voltage is sampled onto $C_h$ equal to $V(t_e)/A$. During phase o the lower section of the circuit computes an accurate output by using the improved virtual-earth at node B, which results from adding the error-correction voltage on $C_h$ to the voltage at the amplifier input, $-V(t_o)/A$. Now, $V(t_o)=V(t_e)$, no matter what the signal frequency, so it follows that the voltage at node B is approximately zero. Hence the node acts as a 'super virtual-earth'. Since the compensating action of the circuit relies on the computation of both error voltage and output voltage in the same sampling-period, we call this type of circuit the 'same-sample-correction' (SSC) type. Note that the input to the circuit must come either from a similar integrator stage or from a sample & held source.
Gain errors (dB) :  
<table>
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<th>freq OSP</th>
<th>conv. delay</th>
<th>prototype delay</th>
<th>FGI-PMP</th>
<th>PMP</th>
<th>PMP</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 e</td>
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<td>-0.0004</td>
<td>-0.0021</td>
<td>-0.0002</td>
<td>-0.0002</td>
</tr>
<tr>
<td>60 e</td>
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<td>-0.0003</td>
<td>-0.0020</td>
<td>-0.0002</td>
<td>-0.0002</td>
</tr>
<tr>
<td>100 e</td>
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<td>-0.0021</td>
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Fig.6.9(a) Comparison of gain errors in PMP integrators

Phase errors (deg) :  
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Fig.6.9(b) Comparison of phase errors in PMP integrators
The performance of the conventional and the new same-sample-correction FGI 3-path integrators were compared, and the results are shown in fig.6.9. This table shows the gain and phase errors for different types of PMP integrators using 60dB amplifiers. These errors are calculated in exactly the same way as in the investigations of SP FGI circuits in chapter 2, ie:

\[
m(\omega) = 1 - \frac{G_{1e}\phi(\omega)}{G_{1e}\phi(\omega)}
\]

\[
\theta(\omega) = \phi_{1e}\phi(\omega) - \phi_{1e}\phi(\omega)
\]

where \( G_A(\omega) \) and \( \phi_A(\omega) \) are gain and phase values for amplifier gain \( A \). The clocking frequency was set to 3kHz, hence the sampling frequency of the pseudo-paths is effectively 1kHz and a bandpass response is obtained at that frequency. The table shows the errors near DC and near 1kHz for the circuits of figs.6.5a (conventional), 6.7 (prototype FGI) and 6.8 (SSC) in columns 2 to 4 respectively (the results in column 5 will be discussed later). For completeness, the results for sampling the output in both phases are shown. The poor performance of the prototype FGI-PMP circuit near 1kHz is evident, even though it gives reduced errors near DC. In contrast, the errors obtained for the new SSC-FGI PMP integrator are very low indeed and it can be shown that its performance using a 60dB amplifier is about the same as that of a conventional circulating-delay PMP circuit using an amplifier with 100dB gain.

During circuit development, where slightly different configurations were investigated, it was discovered that one feature of the clocking scheme was particularly important for achieving these highly accurate results. Referring to fig.6.8 it is seen that the switches connecting the right-hand-sides of the storage capacitors to ground are turned-on in phases 1, 2, 3 and 4. If the amplifier were ideal, then these phases could be changed to 1e, 2e, 3e and 4e for the upper storage capacitors and 1o, 2o, 3o and 4o for the lower ones. It can be shown that, with a finite-gain amplifier, changing the switch-phasing as suggested on the lower storage capacitors has virtually no effect, but making this modification to the upper storage capacitors significantly degrades the filter accuracy. The reason for this is that during the \( o \)-phase, with the clocking scheme shown in the diagram, a pair of the upper storage capacitors is connected in series to the amplifier output, causing their charge to be redistributed in such a way as to reduce the error in charge transfer that occurred during the previous \( e \)-phase. This is illustrated for the case of the phase-4 charge transfers between the \( C_{s2} \) and \( C_{s5} \) capacitors in fig.6.10.
Fig. 6.10a shows the circuit in the e-phase, where charge is transferred from $C_{s2a}$ to $C_{s5a}$ via the amplifier virtual earth. $C_{s2b}$ and $C_{s5b}$ are connected to the amplifier output during this phase, but any change in their charges is overwritten during the following o-phase, shown in Fig. 6.10b, where charge is transferred from $C_{s2b}$ to $C_{s5b}$ via the circuit's improved virtual earth. As explained, this charge transfer leads to a highly accurate amplifier output, but it also results in a redistribution of charge between $C_{s5a}$ and $C_{s2a}$, so that the charges on these two capacitors become very close to those on $C_{s2b}$ and $C_{s5b}$ respectively. This improves the accuracy of the e-phase output significantly and seems to be the main factor explaining the extremely high accuracy of this circuit.

Circuit comparisons were done based on the filter introduced in Fig. 6.2d. If we set $C_1=C_3=1.0$ then the lowpass filter has $Q=1$, and if the integration capacitors are constrained to be equal then $C_a=C_b=16.0$ gives a relative bandwidth of 2% for the passband at $f_s$. All the examples in this section will use an effective path-filter clock frequency of $f_s=1kHz$; thus, in a circulating-delay filter the lowest actual clock frequency is $M \times 1kHz$, while in a RAM-type circuit it is simply 1kHz.
The second-order filter has to be modified slightly for the SSC integrators, as shown in fig.6.11. The main changes are some of the switch phases and, of course, the duplication of all the capacitors. The response of pseudo-7-path filters using the conventional and the SSC circuits with 60dB amplifiers is shown in fig.6.12. The improvement obtained using the SSC circuit is quite spectacular, as it is virtually indistinguishable from the ideal response.
The component costs, compared to a conventional PMP filter, for these major improvements in performance are that the number of switches and capacitors in the circuit is approximately doubled and the time for amplifier settling is halved. There is also a small increase in the complexity of the clocking scheme, although most switches are driven by the same clocks required for a conventional PMP filter. The implementation cost of this and other PMP filters is discussed further in section 6.3.4.

The SSC principle is also applicable to the RAM-type PMP integrator, as shown in fig.6.13. The effect of finite gain on $H_0$ and $Q$ in RAM-type circuits...
is much less than that in a circulating-delay circuit since the number of charge transfers per unit time is reduced, and does not increase with M [119]. The most serious effect of finite gain in such a circuit is that it allows the mismatch in storage capacitors to affect the transfer function, resulting in in-band mirror frequencies. Since, for a set of storage capacitors, the mirror frequency amplitudes will decrease with increasing amplifier gain, it was anticipated that the new SSC circuit, which effectively increases amplifier gain, would reduce these mirrors. To test this theory, the second order filter of fig.6.14 was used; this is based on a high-pass single-path filter, so that the passband will not be affected by clock-feedthrough. Simulations were done by setting the storage capacitors in the conventional and SSC RAM-type cells equal to known, mismatched values, shown in fig.6.15. The level of the mirror frequency responses in the passband, which was from 440 to 560Hz, were then tabulated, as shown. In the first pair of simulations, denoted conv-1 and SSC-1, the mirror-rejection is approximately 30dB better in the SSC circuit than in the conventional one. A second simulation of the conventional circuit, but with two of the storage capacitors effectively interchanged (conv-2), shows that the mirror component levels have very little dependence on the order in which the mismatched capacitors are connected, as was expected. When the order of the storage capacitors in the SSC was changed, however, the mirror components increase dramatically and become slightly stronger than those in the conventional circuit (SSC-2). This unexpected result was confirmed using a first-order lowpass filter, where a similar increase in mirror components was observed when the top and bottom halves of the circuit became mismatched. Also, in spite of the increase in the mirrors produced by this mismatch, the basic FGI property of the circuit remains intact, and the passband response of the SSC circuit is still much closer to the ideal than that of the conventional circuit.
This phenomena is not completely understood, since, from an initial inspection, the improved virtual earth on the lower plate of $C_h$, which is the hub of the FGI circuit's operation, should ensure that there is better charge-transfer between the integration and storage capacitors in the lower half of the SSC circuit than in a conventional one. Hence, according to this theory, storage capacitor mismatch in the lower half of the circuit should have a reduced effect on the transfer function and mirror components should be reduced. That this is not the case must be associated with the very high sensitivity of any multi-path circuit to mirror components - an observation made in chapter 5. It is supposed that in this circuit some, as yet unidentified, second-order effect that is a function of the matching in the two halves of the circuit, rather than just of the matching between the storage capacitors in the lower half, comes into play and maintains the mirrors at a similar level to that in a conventional circuit. We therefore conclude that the RAM-type SSC cell will not reduce in-band mirrors below those in a conventional RAM-type cell and the SSC principle is restricted to Circulating-Delay-type circuits.
### Storage Capacitor Values

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<th>outfreq (Hz)</th>
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<th>SSC-1 dB</th>
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Fig.6.15 Mirror component levels in conventional and SSC RAM-type PMP filters with mismatched storage capacitors (pseudo-3-path, 2nd-order kernel, fc=3kHz, A=60dB).

### 6.3.3 Symbolic Analysis of SSC circuits

![Single-path equivalent of circulating-delay SSC PMP integrator](image)

In order to improve our understanding of the SCC circuit, the single-path equivalent of the PMP circuit of fig.6.8 is analysed. This single-path circuit is shown in fig.6.16, and its operation is described by the SFG of fig.6.17 (derived using charge conservation is the circuit of fig.6.16). This was analysed using the symbolic-mathematics software written by the author (appendix 1), neglecting terms with a factor of $1/A^3$ and using $C_{1a} = C_{1b} = C_1$ and $C_{xa} = C_{xb} = C_x$. The resulting transfer function when the output is sampled in the $o$ phase is:

$$H(z) = \frac{-C_1/C_2 z^{-1/2}}{D(z)}$$  \hspace{1cm} (6.7)

where

$$D(z) = (1-z^{-1}) \left(1 - \frac{1}{A^2} \left(3 + \frac{C_h}{C_2} + \frac{C_h^2}{C_2^2} + \frac{1}{1-z^{-1}} \left[3 \frac{C_1 C_h}{C_2 C_2} + 6 \frac{C_1}{C_2} \right] + \frac{1}{(1-z^{-1})^2} \frac{3 C_1^2}{C_2} \right) \right)$$  \hspace{1cm} (6.8)

Now, for a narrow-band PMP filter based on a lowpass kernel the
integration capacitors will be much larger than the feed-in or \( C_h \) capacitors so, using the techniques described in chapter 2, the gain and phase errors are given by:

\[
m(\omega) = \frac{3}{A^2} \left( 3 + 3 \frac{C_h}{C_2} + 3 \frac{C_1}{C_2} \right)
\]  

\[
\theta(\omega) = \frac{3C_1/C_2}{A^2 \tan(\omega T/2)}
\]

Hence the largest terms in the expressions for \( m(\omega) \) and \( \theta(\omega) \) have factors of \( 1/A^2 \). Comparing this result with those for the FGI circuits in chapter 2 it is seen that this is not only significantly better than the result for conventional integrators, where both gain and phase errors contain factors of \( 1/A \), it is also significantly better than the other single-path FGI circuits, where at least the gain error has a factor of \( 1/A \). These are very encouraging results, and the form of these gain and phase error expressions strongly supports the design strategy adopted.

\[g(z) = \frac{C_1a + C_h}{A} + C_2a \left( 1 + \frac{1}{A} \right) (1 - z^{-1})\]

\[h(z) = \frac{C_h}{A} + C_2b (1 - z^{-1})\]

\[\text{Fig.6.17 SFG for circuit of fig.6.16}\]

At this point, some differences between the single-path circuit just analysed and the FGI PMP circuits should be noted. Experimentation with the
FGI PMP circuit has shown that the connection of the grounded switches on the right-hand-side of the \( C_\text{s} \) capacitors during the o-phase is important in achieving maximum insensitivity to \( A \). The situation is not quite the same in the single-path cell, however, and in that case the e-phase output is no more accurate than in a conventional circuit.

The high accuracy of the o-phase output - better than any of the circuits discussed in chapter 2 - raises the question, "can this single-path circuit be considered a useful single-path building-block?". The answer to this is positive, since the circuit is clearly a high quality, stand-alone FGI integrator. It should also be noted that a Matsumoto capacitor [317] can be connected to the single-path circuit in order to avoid the spiking-problem in the switch guard-intervals (this is not possible for the PMP circuit). A possible drawback of the integrator for filtering applications is that it may not be used directly with its non-inverting counterpart to form a two-integrator loop. This is because the total delay through a cascaded inverting- and non-inverting pair is greater than one clock period and, as discussed in chapter two, integrators with this characteristic require extra circuitry to configure them in a two-integrator-loop. In spite of this, the very high accuracy of the circuit will certainly make it attractive for many applications.

### 6.3.4 Last-Cycle correction (LCC) FGI circuits

We now describe a further novel FGI PMP integrator which achieves the same aim as the one just described, but without performing two output voltage calculations [199]. The circuit operation exploits the narrow-band nature of the filter, and only provides finite-gain compensation for signals in the narrow passband. It uses the fact that, if the circuit is excited by a signal at exactly the passband centre, then the circuit’s sampled output voltage will cycle through only \( M \) different levels. A given output voltage sample may therefore be used to predict the output \( M+1 \) samples in the future. This will also allow the amplifier finite-gain error voltage to be predicted in advance, and used to compensate that future error. For this reason the technique has been named "Last-Cycle-Correction" (LCC). The principle of using finite-gain-error prediction to compensate narrow-band SC filters with a low \( f_s/f_o \) has been independently discovered by Baschirotto [150]. However, the application of this principle to PMP filters has not previously been described. In fact, these circuits are especially suited to this technique since they are always designed for narrow-band operation with low \( f_s/f_o \) and also they are especially vulnerable to the effects of amplifier finite gain [179].
A 3-path Circulating-Delay version of the new circuit is shown in fig.6.18. The switch phasing is arranged so that the error-correction voltage sampled onto the $C_{h1}$ capacitor during phase 1 is effectively stored for $N(N+1)$ phases and appears on the $C_{h2}$ capacitor to correct the phase 1 charge transfer $N(N+1)\tau$ later, where $\tau$ is the length of one clock phase. To verify this, consider a number of charge transfers in more detail. A charge packet arriving on $C_{s4}$ from $C_0$ in sub-phase 1e will produce an error-correction voltage on $C_{h1}$ in sub-phase 1o. This correction voltage will be used in 4e to transfer the charge on $C_{s4}$ to $C_{s3}$, but will be immediately regenerated on $C_{h4}$ in sub-phase 4o. Similarly, the transfer of charge from $C_{s3}$ to $C_{s2}$ will use the error-correcting voltage on $C_{h4}$, but this will be regenerated on $C_{h3}$ in sub-phase 3o. Eventually, $N(N+1)$ phases after its original generation on $C_{h1}$, the error-correction voltage is used by $C_{h2}$ to correct another charge transfer from $C_0$ to $C_{s4}$.

Now, a Circulating-Delay PMP filter will have bandpass responses at $f_0 = n.f_s/N$, where $n$ is a positive integer, and clock phase of length $\tau = 1/f_s(N+1)$, and so, assuming the circuit is in a steady state, the change in circuit output voltage over $N(N+1)$ clock phases will be:

$$\delta = V_o(2\pi f_o\tau + \phi) - V_o \left(2\pi f_o \left( t + \frac{N(N+1)}{f_s(N+1)} \right) + \phi \right)$$

which is equal to zero when $V_o(t)$ is a sine wave, and which confirms the predicting nature of the circuit. It follows that, for frequencies close to $f_0$, the error-correcting voltages stored on the $C_h$ capacitors are accurate enough to give good finite-gain compensation. Hence, for filters with small relative
bandwidths the compensation is effective for all in-band signals.

Fig. 6.19 Circulating-Delay LCC pseudo-7-path filter based on 2nd order kernel

Fig. 6.20 Frequency response for circuit of fig. 6.19

Comparing the gain and phase errors of the integrator, shown in fig.6.9, with those of its rivals, it is seen that both errors are substantially reduced compared to the conventional Circulating-Delay circuit, but are somewhat higher than in the SSC integrator. This is confirmed by simulations of a pseudo-7-path filter using 60dB amplifiers, shown in figs. 6.18 to 6.20. It can be seen that, while the conventional circuit has an in-band gain 2.0-3.5dB below the ideal, the response of the new circuit differs by only a fraction of a dB (0.14dB). It is also found that the deviation of the centre frequency of the new filter is reduced by about one order of magnitude. The cost compared to a conventional PMP circuit for this substantial improvement in performance is that the time allowed for amplifier settling is halved, due to the
introduction of the extra e- and o- sub-phases, the complexity of the clocking scheme is increased (although some economy can probably be made by deriving the 1e, 1o, 2o, etc. sub-phases locally) and that the number of switches in the integrator cell is approximately doubled. Finally, \( M-1 \) extra (minimum-sized) \( C_h \) capacitors are required.

\[
\begin{array}{|c|c|c|}
\hline
\text{# switches} & \text{# clock phases} & \Sigma C \\
\hline
\text{conventional} & 2M + 6 & M + 1 & C_0 + (M+1)Cs \\
\text{SSC} & 4M + 14 & M + 5 & 2C_0 + 2(M+1)Cs + Ch \\
\text{LCC} & 4M + 8 & 3M & C_0 + (M+1)(Cs+Ch) \\
\hline
\end{array}
\]

Fig.6.21 Comparative implementation cost of conventional, SSC and LCC PMP-integrator blocks.

A comparison of the implementation cost of the new circuit with the conventional and SSC types is given in fig.6.21. It can be seen that the circuit requires fewer switches and has significantly lower total capacitance than the SSC PMP integrator. In spite of its slightly higher sensitivity to amplifier gain when compared to the SSC building block, this circuit may therefore be an attractive option in many applications.

The LCC principle can also be applied to the design of a RAM-type PMP cell. However, clock-feedthrough considerations make it desireable to use highpass kernels for RAM-type designs, so that passbands are centred at odd multiples of \( fc/2N \). That is:

\[
f_o = \frac{n f_s}{2N} \quad n \text{ odd} \quad (6.12)
\]

Unfortunately, the LCC strategy does not work with the values of \( f_o \) given by (6.12), as can be verified by substituting (6.12) into (6.11). It is therefore restricted to use with lowpass kernel filters.
6.4 Summary and Conclusions

To overcome the problems of path-filter centre-frequency mismatch in NPFT filters, an N*M-path filter has been proposed. This is produced by replacing the single-path filters in an NPFT structure with PMP filters. Non-ideal effects in PMP filters have been examined in the context of their use in the new structure, and it has been recognised that the effects of amplifier finite DC gain are particularly severe.

It was found that the development of a finite-gain-insensitive (FGI) PMP integrator by direct translation of the single-path Nagaraj circuit [89] did not produce the required FGI property at the filter bandpass frequency. The interchange of storage capacitors between the amplifier input and output, a clear difference from the single-path circuit, caused the circuit only to have the FGI property for $\omega T << 1$. A new 'Same-Sample-Correction' (SSC) circuit, where the error-correcting mechanism works entirely within one sampling window, has been shown to give accurate operation independent of signal frequency. When the SSC principle is applied to a Circulating-Delay PMP circuit the result is a dramatically reduced sensitivity to amplifier gain. This result is emphasised by the symbolic analysis of a single-path version of the the circuit (a pseudo-one-path integrator, in effect) which showed that both gain and phase errors are inversely proportional to the square of the amplifier gain. The latter circuit is itself a useful FGI single-path integrator. In spite of this success, it has not been possible to produce a RAM-type integrator with reduced mirror components using the SSC principle, and possible reasons for this have been given.

We have also demonstrated the effectiveness of a new 'Last-Cycle-Correction' (LCC) PMP integrator, which exploits the narrow-band nature of the PMP filter to predict amplifier errors from information in the previous signal cycle. Again, this principle works well for Circulating-Delay cells, but cannot be applied to RAM-type cells. This is because RAM-type PMP filters must be based on highpass kernel filters in order to avoid in-band clock feedthrough, while the LCC principle requires a lowpass kernel. Three powerful new FGI circuits have therefore been developed, the SSC-PMP, the single-path equivalent of the SSC-PMP, and the LCC-PMP. The two PMP circuits will find applications in many multi-path applications, including N*M-path filters. The single-path integrator has been a useful analytical device for investigating the SSC-PMP circuit, and is also most effective in its own right.
7. CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

7.1 Discussion of results

7.2 Possible further work

7.2.1 GaAs CS filters
7.2.2 N*M-path filters
7.2.3 FGI circuits
7.2.3 Symbolic analysis tools
7.1 Discussion of results

The main objectives of this work were to develop and demonstrate high-speed switched-capacitor (SC) circuits using available commercial GaAs IC technology, and to investigate SC structures for Ultra-Narrow-Band filtering. These two distinct areas of work benefitted considerably from the cross-fertilization of ideas and techniques, and from the development of special purpose computer-based tools. The SFG-based symbolic analysis package is a prominent example of this, and was a major factor in the development of ideas in both of the main research areas. Particular benefits also arose from the transfer of techniques for finite-gain-insensitive (FGI) SC circuits from the GaAs IC project to the UNB filtering work, allowing the development of FGI pseudo-N-path (PNP) filters. An important transfer has also occurred in the opposite direction, since a single-path FGI integrator, developed as a bi-product of the work on FGI PNP filters, may be of considerable use in GaAs IC's. We now summarise and discuss the principal results of the work in this thesis.

Following a general introduction in chapter 1, chapter 2 focuses on the design of FGI integrators, placing particular emphasis on circuits that can be economically formed into two-integrator loops, and where the phase error has very low sensitivity to amplifier gain at all signal frequencies. "Spike free" circuits, where the amplifier has a continuous feedback path, are preferred. The interconnection issue is highlighted by correlating all available information on integrator-pairs (ie. complementary inverting and non-inverting integrators), so that the cost of using such pairs in second- and higher-order filters can be assessed. From this work a novel integrator pair, meeting all the foregoing requirements, was produced, and its feasibility confirmed in simulations.

This work was taken a step further by the development of a symbolic analysis tool, MASONPAK, greatly facilitating a thorough and systematic analysis of the FGI integrators. An important property of the Nagaraj integrator was discovered that allows the inverting- and non-inverting circuits to be directly interconnected, without any increase in the phase sensitivity, by a suitable choice of the capacitor at the input of the inverting integrator's amplifier. This discovery was later confirmed by other workers. A detailed analysis of the Nagaraj integrator also allowed the physical mechanisms underlying its excellent properties to be explained for the first time.

Chapter 3 addresses the problem of the optimisation of high-speed SC circuits and presents the settling-time analysis of a general, fully-
interconnected dual-amplifier network (i.e. a network consisting of two amplifiers where every node is connected to every other node by a capacitor). The results of this analysis are directly applicable to the detailed optimisation of two-amplifier circuits, where the amplifiers may be modelled as linear transconductors. The importance of taking inter-amplifier coupling into account in many practical systems is amply demonstrated, and objective criteria for deciding when such coupling may be neglected are established. The symbolic expressions obtained for the system time-constants in particular special cases allow a qualitative understanding of the factors affecting performance to be quickly acquired, while the full, general expressions may be used to rapidly generate quantitative data. The analysis results are also very relevant to the design of systems with more than two amplifiers, such as ladder filters, since they allow inter-amplifier coupling to be examined on a pair-by-pair basis, thus improving the understanding of a complex system of interacting components. The chapter goes on to describe a comprehensive amplifier characterisation method which generates the data necessary when using the aforementioned expressions to predict circuit settling-times. The method is aimed at high-speed SC circuits where, in order to minimise settling times, amplifiers must be scaled so that their parasitic capacitors are similar in size to the effective external load capacitance. Unlike in previous methods we therefore take full account of these parasitics, so that the results are applicable no matter what embedding is used for the amplifier.

Chapter 4 describes the implementation of the second-order filter developed in chapter 2, using the Plessey GaAs MIMIC process. The distinctive device modelling problems resulting from the non-standard use of this process are described, and the novel combination of techniques used to overcome them are presented. The use of a multiple-subcircuit model, where each different subcircuit is optimised according to a particular aspect of MESFET behaviour, is shown to be a workable solution that overcomes the restrictions of available simulators. It reveals, for example, that amplifier designs relying on device-width ratioing are unattractive in this technology (such an observation could not have been made using a standard JFET model). The design of amplifier and switch-control subcircuits are described. Since the FGI circuit architecture allows the use of comparatively low-gain (<60dB) amplifiers, and because of the difficulty in designing a high-gain amplifier for the given process, a simple single-stage, single-cascode amplifier was designed. New, balanced switch-control and clock-generation circuits were also developed, and give output signals where the high and low levels are particularly well-matched to the rest of the circuit. The balanced nature of the circuits also suggests that strategies for clock-feedthrough cancellation may be possible, though this development has not yet been explored. Application
of the characterisation procedure and analysis techniques from chapter 3 revealed that the maximum clocking frequency for the design was strongly limited by power consumption considerations, which would make the implementation of higher order GaAs SC filters most difficult. A high device threshold voltage and the lack of an insulating-gate FET (which means that switch-control circuits are required) are seen to be two important contributors to this problem. In addition, although the FGI architecture is shown to be capable of similar clock speeds to a conventional circuit, the extra capacitors and switches in the FGI system make it consume more power for a given clocking frequency. This is again a process-related problem, since the FGI architecture was adopted in response to the problem of limited intrinsic FET gain, $g_{m}/g_{o}$. It is concluded that developments addressing these severe process limitations are essential before further progress can be made.

In spite of these problems, simulations indicate that filtering frequencies up to 40 MHz (a clocking frequency of 500 MHz) will be possible for the circuit described, before appreciable degradation in performance is noticed. Delays in fabrication and packaging have not allowed us to confirm this with measurements, however. If it is achieved, such a filtering frequency will be the highest so far achieved using SC circuits.

Chapters 5 and 6 describe work on Ultra-Narrow-Band filtering systems. Chapter 5 first introduces notation for, and gives a mathematical description of, N-Path (NP) and N-Path Frequency-Translated (NPFT) filter systems. The selectivity requirements of the anti-alias and anti-image filters in such systems are discussed, and it is noted that the feasibility of the NPFT system depends on adequate cancellation of mirror and residual-image frequency components. The structure of the NPFT system, which uses bandpass path-filters, and the very narrow bandwidths required of these path-filters in an ultra-narrow-band system, makes path-filter mismatch an important design issue. The analysis of mismatch phenomena was therefore undertaken using purpose-built software tools. These tools were designed to allow key parameters in multi-path systems to be quickly and easily investigated, and emphasise a modular approach to the construction and analysis of the filter system. It was established that the duality of the aliasing and imaging phenomena allows statistical information on the strength of mirror responses to be directly applied to residual-image responses also. Simulation results for the mirror responses show that the strength of mirrors in an N-path system decreases with increasing N, and is also strongly related to the relative bandwidth and order of the path-filters. It also conclusively demonstrates that for an ultra-narrow band NPFT filter, given typical IC process tolerances, centre-frequency mismatch in the path-filters would lead
to very significant mirror component levels. The resulting high selectivity requirement for the anti-alias and anti-image filters in such a system seriously compromises their practical implementation.

Chapter 6 presents several new circuits to overcome the above mismatch problems. The use of pseudo-N-path filters in place of the normal single-path path-filters in an NPFT system is advocated, as such filters produce a bandpass response that is effectively fixed with respect to the clock frequency, which is common to all the path-filters. The new structure is called an N*M-path filter and, since it relies on pseudo-N-path (PNP) filters for its implementation, the effects of non-ideal phenomena on the latter are examined in the context of this new configuration. The effects of amplifier gain on the favoured circulating-delay type PNP filter were found to be severe and so, using the knowledge acquired on single-path FGI integrators, new FGI-PNP circuits were developed. Particular problems created by the use of multiple storage capacitors in PNP circuits were overcome using two alternative predicting techniques, named "Same Sample Correction" (SSC) and "Last Cycle Correction" (LCC). We have shown that both these techniques, when applied to circulating-delay structures, result in circuits with responses that cannot be achieved by their conventional counterparts, even using amplifiers with ten times the gain. A remarkable bi-product of the SSC development was a single-path FGI circuit where both the gain and the phase error have very low sensitivity to amplifier gain. This integrator is the most accurate that we know of, when both gain and phase are taken into account.

7.2 Possible further work

7.2.1 GaAs CS filters

The further development and characterisation of GaAs IC processes, specifically to meet the requirements of analogue IC design in the MHz range, is required. Several specific potential improvements have been identified in this thesis, but the main requirement is for a strong link between process development and circuit development programmes. Although one of the main objectives of this work was to use available foundry processes, commercially attractive SC circuits do not seem possible with the process used, despite very careful optimisation of our designs. The problem of high power consumption seems most serious, implying added off-chip costs (eg. for heat-sinking and power supplies), and limiting the complexity (order) of the filter due to on-chip power considerations. We are presently involved in a collaborative project that has these process-development goals, together with Plessey Research, Cossor Electronics and Bradford University in a DTI-
sponsored Advanced Technology Programme. At the circuit level, future designs should proceed with low power consumption as a design goal. Otherwise, the most pressing areas seem to be in amplifier design, where further work towards a differential-input circuit is needed, and in the switching circuits, where possible ways of minimising clock-feedthrough should be investigated. Finally, it is very important that as much data as possible is obtained from the circuit already fabricated, and this work is in hand.

### 7.2.2 N*M-path filters

A practical investigation of N*M-path ultra-narrow-band (UNB) filters, to produce prototype integrated circuits, is desirable. Considering the demanding specification that such filter systems place on the component sub-filters, it will be necessary to either incorporate very high-gain (>60dB) amplifiers into these systems, or to use FGI PNP circuits. Also, since many applications for UNB filters will be at frequencies that are high for SC technology, the amplifiers must have a relatively high slew-rate and bandwidth. For these reasons we feel that the use of BiCMOS technology for implementing N*M-path systems should be investigated (in the UK, such a project can now take advantage of fabrication opportunities offered by the Esprit Eurochip initiative). The relative cost in terms of Si area, power consumption and performance between the high-gain amplifier solution and the use of FGI PNP circuits could then be accurately assessed. While the integration of a complete N*M-path system is the ultimate goal, we feel that a practical intermediate step is to fabricate alternative path-filters, then combine them into an N*M-path system at the PCB level. This would allow the properties of a fully integrated system to be predicted, while retaining the maximum number of options for circuit testing. This approach has been endorsed by the SERC(UK), who have recently awarded to us a research grant to carry out such a project.

### 7.2.3 FGI circuits

The single-path SSC FGI integrator should be investigated further, and possible ways for using it in two-integrator loops studied. Its possible use in non-filtering applications, such as in $\Sigma\Delta$ converters, is also worth careful study. For the SSC PNP filter, a theoretical study into how, if at all, the SSC principle may be adapted to RAM type PNP circuits is worthwhile. Also, the use of SSC PNP structures for FIR filtering is attractive, and will be investigated. IC implementations of all the SSC and LCC circuits presented in this thesis will be of considerable practical interest, and such work is now
being undertaken as a result of the SERC award mentioned above.

7.2.4 Symbolic analysis tools

Experience with computer-based symbolic analysis tools, developed during the course of this PhD work, has shown that such tools greatly assist the qualitative understanding of a wide variety of systems. By removing some of the tedium in error-prone hand calculations, and by encouraging a structured approach to the solution of systems of equations, the software may be instrumental in acquiring a better understanding of circuit properties. Our current software is based on a signal-flow-graph (SFG) representation of circuit currents and voltages, and it would be most useful if this were extended. The ability to enter circuit descriptions using other types of representation would be a great step forward, so that, for example, circuits could be entered as netlists of switches, capacitors, amplifiers etc. Most of the theoretical problems encountered in doing this have been treated in the literature, and so the work should be a development project with the aim of enabling future research discoveries.
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APPENDICES

A.1 MASON & PS symbolic analysis tools

A.2 Analysis of a Single-Cascode Amplifier

A.3 Dual-amplifier-network denominator function

A.4 Input & Output bands in a sampled-data system
Appendix 1, MASON & PS symbolic analysis tools

MASON & PS are the principle tools out of a 'software package' which we have called MASONPAK. The first tool, MASON, computes the symbolic transfer function of a Signal Flow Graph (SFG) between two specified nodes using Mason's rule [164], and its operation will be explained using the example shown in fig.A1.1.

Fig.A1.1 Example signal flow graph - s domain

filename eg2.mas
Biquad filter [Gregorian & Temes, p.286]
-----------------------------------------------
BRANCHES
Vin   Va  1  0
Va    Vb  K0/w0  0
Va    Vc  K1  0
Va    Vc  K2  1
Vb    V1  -1  -1
V1    Vc  -w0  0
Vc    Vd  -1  -1
Vd    Vc  w0/Q  0
Vd    Vb  w0  0
Vd    Vout  1  0

filename: eg2.tfn
Network defined by file eg2.mas
Biquad filter [Gregorian & Temes, p.286]
-----------------------------------------------
numerator:
-2 -K0
-1 -K1
0  -K2
denominator:
-2  w0*w0
-1  w0/Q
0  1

(b)

Fig.A1.2 (a) File eg2.mas: netlist defining SFG , (b) File eg2.tfn: transfer function computed
The SFG is represented to the program as a netlist, shown in fig.A1.2a. Each line in the part of the netlist defining the branches gives the source and sink nodes for each branch, then the branch weight. The latter is expressed as a constant followed by a power to which the main variable in the system, normally s or z, is to be raised. To take the Vb-to-V1 branch as an example, the constant factor is -1 and the power for s is -1, so the branch weight is -1/s. The separation of the main variable (in this case s) from the other symbols in the SFG (K0, ω0 etc.) is done for reasons of program efficiency. Once the netlist file has been produced it is then input to the MASON program and the input and output nodes of the desired transfer function are specified. The program then computes the transfer function, which is shown for this example in fig.A1.2b. The format for the output is that each line represents one term of a polynomial in the main variable, with the power of the main variable first, then the coefficient. Thus the example shown has the result:

\[ H(s) = \frac{V_{out}}{V_{in}} = \frac{-K_0 s^{-2} - K_1 s^{-1} - K_2}{\omega_0^2 s^{-2} + \frac{\omega_0}{Q} s^{-1} + 1} \]

The MASON program consists of several independent routines, the most visible of which is written in Prolog [182], while the rest are in C [183]. The Prolog routine is used as the interactive front-end to the program, and also to compute all the loops and forward-paths in the SFG - a necessary step before Mason's rule can be applied. This task is particularly suited to the object-orientated Prolog language, since the required search procedures are an inherent part of the language structure. The forward-path and loop information, which may be inspected and is useful for cross-checking the input netlist, is fed via an intermediate file to a C routine for the remainder of the calculation.

The next tool, called 'PS', is for the manipulation of symbolic polynomial expressions. This allows systematic and error-free manipulation of equations that are too cumbersome for convenient hand calculations. The tool may either be used interactively or by specifying a set of instructions in an input file, and results may be stored in a 'log file'; hence, program sessions may be systematically planned, modified and recorded. At the heart of the program is a set of 10 registers, labelled p0 to p9, which are each capable of storing a polynomial in some variable (s, say) of arbitrary length. The format for the polynomials is the same as the output format of the MASON program, thus allowing easy transfer of data between the two. All operations in the program are applied to the p0 register, which has a similar role to the accumulator in a standard microprocessor. The available instructions are as follows, where [<arg>] represents an optional argument:
Although we do not have space to explain fully all these instructions, the following example, which acts on the output of computations from the MASON program, should give a flavour of using PS. The example will show the manipulation and simplification of the transfer function of the z-domain SFG shown in figA1.3. The SFG is, in fact, the z-domain version of fig.A1.1, and it is seen that the integrator functions now contain a polynomial in the denominator. Since MASON can only deal with branch weights that are simple polynomials, the denominator function is represented by \(D(z)\) (\(D(z) = 1 - z^{-1}\)) producing the output transfer function shown in fig.A1.4a. The instructions used by PS to simplify this expression and, in particular, expand \(D(z)\), are shown in fig.A1.4b, which is the listing of a file called by the 'f command in PS. It can be seen that the first instruction in this file is to open a log file, eg3.log, to record the results of the manipulations, and the log file is shown in fig.A1.4c. Comparison of the instruction file and the log file should give a good insight into the program operation. To summarise the calculations, the transfer function is originally defined as:
\[ H(z) = \frac{C_1 C_3}{C_1 A C_1 B D(z)^2} z^2 - 1 + \frac{C_{11}}{C_1 B D(z)} C_{1B} + \frac{C_{12}}{C_1 A C_1 B D(z)^2} z - 1 + \frac{C_4}{C_1 B D(z)} + 1 \]  

(A1.2)

The numerator and denominator are then multiplied by \( D(z)^2 \), \( C_A \) and \( C_B \) are set to 1 and \( D(z) \) is expanded to give:

\[ H(z) = -\frac{C_{12} C_1 A z^{-2}}{C_1 A C_1 B z^{-2}} + \frac{(C_1 C_3 - 2 C_1 C_2 A - C_{11} C_1 A) z^{-1} + C_{11} C_1 A + C_{12} C_1 B}{C_1 A C_1 B} \]  

(A1.3)

Although this is a simple example, systematic application of these tools allows symbolic expressions of considerable complexity to be derived and manipulated.
Network defined by file eg3.mas
Biquad filter in z domain [Gregorian & Temes, p.286]

numerator :
\[-1 -C1*C3/C1A/C1B/D(z)/D(z)\]
\[0 ( -C11/C1B/D(z) - C12/C1B )\]

denominator :
\[-1 C2*C3/C1A/C1B/D(z)/D(z)\]
\[0 ( 1 + C4/C1B/D(z) )\]

(a)

| eg3.psu |
| eg3.log |

The following comes from eg3.tfn:

numerator :
\[-1 -C1*C3/C1A/C1B/D(z)/D(z)\]
\[0 -C11/C1B/D(z)\]
\[0 -C12/C1B\]

denominator :
\[-1 C2*C3/C1A/C1B/D(z)/D(z)\]
\[0 1\]
\[0 C4/C1B/D(z)\]

m p1

denominator :
\[-1 C2*C3/C1A/C1B/D(z)/D(z)\]
\[0 1\]
\[0 C4/C1B/D(z)\]

m p2

Now have numerator stored in
register p1 & denominator in p2

\[D(z) = 1 - z^{-1} \ldots \text{ store in p3}\]
\[-1 -1\]

m p3

Now simplify numerator & denominator,
apply same operations to each

\[= p1 \ast D(z) \ast D(z)\]
\[r D(z) \ast p3\]
\[= p1 \ast C1A \ast C1B\]

numerator :
\[p\]
\[= p2 \ast D(z) \ast D(z)\]
\[r D(z) \ast p3\]
\[= p2 \ast C1A \ast C1B\]

denominator :
\[p\]

(b)
The following comes from eg3.tfn:
numerator:
input poly:
-1 -C1*C3/C1A/C1B/D(z)/D(z)
 0 -C11/C1B/D(z)
 0 -C12/C1B

denominator:
input poly:
-1 C2*C3/C1A/C1B/D(z)/D(z)
 0 1
 0 C4/C1B/D(z)

Now have numerator stored in register p1 & denominator in p2
D(z) = 1 - z^-1 store in p3

Now simplify numerator & denominator, apply same operations to each
p = p1
r D(z)*D(z)
= C1A*C1B

numerator:
p
-2 -C12*C1A
-1 -C1*C3
-1 2*C12*C1A
-1 C11*C1A
 0 -C11*C1A
 0 -C12*C1A

denominator:
p
-2 C1A*C1B
-1 -2*C1A*C1B
-1 -C1A*C4
-1 C2*C3
 0 C1A*C1B
 0 C1A*C4

Fig.A1.4 (a) File eg3.tfn: result of calcs. on fig.A1.3 SFG, (b) file eg3.psu: instructions to control
manipulation of expression in (a), (c) file eg3.log: results of using eg3.psu
Appendix 2, Analysis of a Single-Cascode Amplifier

A single-stage cascode amplifier is shown in fig.A2.1 in simplified form, embedded in a capacitor network (Ci, Ci and Cl, where Cl and Ci include the parasitic amplifier input and output capacitances). The small-signal equivalent circuit is shown in fig.A2.2. To simplify the analysis, identical transistors are assumed, so that g_m1 = g_m2 and g_o1 = g_o2. Using this, the transfer function of the circuit can be found and written as follows:

\[ \frac{V_o}{V_{sig}} = \frac{N(s)}{D(s)} \]  
(A2.1)

where:

\[ D(s) = s^2 + \left( \frac{g_m + g_o}{C_p} \left[ \frac{1}{C_{eff}} + \frac{C_i}{C_f C_{eff}} \right] \right) + \frac{g_m^2}{C_p C_{eff}} = 0 \]  
(A2.2)

\[ C_{eff} = C_i + C_f + \frac{C_f C_i}{C_f} \]  
(A2.3)

\[ C_p = C_{p1} + C_{p2} + C_{p3} \]  
(A2.4)

and the following assumptions have been used:

\[ g_o << g_m \]
\[ C_{p2} << C_{p1}, \quad C_{p2} << C_i, \quad C_{p2} << C_l \]
\[ C_{p3} << C_{p1}, \quad C_{p3} << C_i, \quad C_{p3} << C_l \]  
(A2.5)
The open-loop poles are first found by setting $C_f$ to zero in (A2.2). This results in:

$$p_1 = -\frac{g_m C_p^2}{C_i}$$  \hspace{1cm} (A2.6)

$$p_2 = -\frac{g_m}{C_p}$$  \hspace{1cm} (A2.7)

Now, it is well known that when feedback is applied to the amplifier (i.e. $C_f$ is made non-zero) these real poles will approach each other along the negative axis, and eventually meet and split to form a pair of complex poles. Until this splitting occurs the amplifier settling characteristics will be dominated by the lower frequency pole, and the amplifier will behave approximately like a linear transconductor with a settling time-constant given approximately by $t_s = C_{eff}/g_m$ (see chapter 3). When the poles become complex, settling behaviour will be underdamped, with the settling time-constant depending on the real part of the complex poles. As the load on the amplifier is decreased, settling will become progressively more underdamped, so that settling-time increases with decreasing capacitative load. It follows that there will be a settling-time minimum at the threshold between these two types of settling behaviour. At this point the system has two real poles which are approximately equal to:

$$p_{crit} = -\frac{g_m}{2C_p}.$$  \hspace{1cm} (A2.8)

(In fact, minimum settling time occurs when the settling is slightly underdamped, so that the overshoot is just equal to the maximum error in settling. Using the formulae for this overshoot in [97], it has been shown that for 0.5% settling the minimum in $t_s$ occurs for a damping factor of 0.925). This behaviour is illustrated for a real amplifier by fig.A2.3, which has been taken from [158], and is the characterisation data for the amplifier described in chapter 4 using a number of different amplifier embeddings.)
From (A2.2) it can be shown that critical damping occurs when:

$$C_p = \frac{C_{\text{eff}}}{4}$$  \hspace{1cm} (A2.9)

The latter equation therefore locates the $t_s$ minimum under the stated conditions. Examination of fig.A2.1 shows that:

$$C_{p1} = C_{gs2} + C_{ds1} + C_{\text{substrate}}$$  \hspace{1cm} (A2.10)

$$C_{p2} = C_{gd1}$$  \hspace{1cm} (A2.11)

$$C_{p3} = C_{ds2}$$  \hspace{1cm} (A2.12)

where $C_{\text{substrate}}$ is the effective parasitic capacitance from the $V_s$ node to the substrate. It follows that the approximations in (A2.5) are likely to be valid for technologies where gate-source and substrate capacitances are the dominant parasitics. However, it can be shown that (A2.9) is not substantially altered even if this is not the case. It follows from (A2.9) that near the settling-time minima the effective amplifier load is of the same order as the amplifier parasitic capacitances. Provided, therefore, that $C_{\text{eff}}$ is significantly larger than these parasitics, amplifier settling will be overdamped and the settling time-constant determined by $g_m$ and $C_{\text{eff}}$ (see chapter 3). The linear transconductor model is therefore applicable in most practical situations.

The results of this analysis can be tested on the amplifier characterisation data given in fig.A2.3. From the analysis above, and using MESFET modelling data to calculate parasitic values, (A2.9) predicts that at the minimum in $t_s$:

$$C_{\text{eff}} \approx 4C_p \approx 4C_g \approx 80\,\text{fF}$$  \hspace{1cm} (A2.13)

Also, for the curve using $C_{\text{eff}} \approx C_l$ and embedding 2:

$$C_l \approx 12C_g / 5 \approx 48\,\text{fF}$$  \hspace{1cm} (A2.14)

Both of these predictions are in excellent agreement with the data shown.
Fig. A2.3 Amplifier characterisation data for different embeddings
Appendix 3, Dual-amplifier-network denominator function

The application of Mason's rule, by the MASON computer program to compute the denominator function, \( D(s) \), of the dual-amplifier network described in chapter 3 results in a quadratic:

\[
D(s) = as^2 + bs + c
\]  

(3.12)

where

\[
a = t_1 + t_2 + \]

\[
(c_{13,c13,c24,c24} + c_{14,c14,c23,c23})/gm1/gm2/Cf1/Cf2 - A
\]

(A3.15)

\[
b = t_1 + t_2 + B
\]

(A3.16)

\[
c = 1 - c_{14,c23}/Cf1/Cf2
\]

(A3.17)

\[
t_1 = (C_{11} + C_{11} + C_{11,C11}/Cf1)/gm1
\]

(A3.18)

\[
t_2 = (C_{12} + C_{12} + C_{12,C12}/Cf2)/gm2
\]

(A3.19)

\[
A = \\
-2*C_{11}*c_{23}*c_{24}/Cf1/gm1/gm2 + C_{11}*c_{23}*c_{24}/Cf1/gm1/gm2 \\
-2*C_{12}*c_{14}*c_{24}/Cf2/gm1/gm2 + C_{12}*c_{14}*c_{24}/Cf2/gm1/gm2 \\
-2*C_{11}*c_{13}*c_{14}/Cf1/gm1/gm2 + C_{11}*c_{13}*c_{14}/Cf1/gm1/gm2 \\
-2*C_{12}*c_{13}*c_{23}/Cf2/gm1/gm2 + C_{12}*c_{13}*c_{23}/Cf2/gm1/gm2 \\
-2*c_{13}*c_{14}*c_{23}*c_{24}/Cf1/Cf2/gm1/gm2 + c_{13}*c_{14}/Cf2/gm1 \\
-2*c_{13}*c_{14}/gm1/gm2 + c_{13}*c_{14}/gm1/gm2 \\
-2*c_{13}*c_{23}/gm1/gm2 + c_{13}*c_{23}/gm1/gm2 \\
-2*c_{13}*c_{24}/gm1/gm2 + c_{13}*c_{24}/gm1/gm2 \\
-2*c_{14}*c_{23}/gm1/gm2 + c_{14}*c_{23}/gm1/gm2 \\
-2*c_{14}*c_{24}/gm1/gm2 + c_{14}*c_{24}/gm1/gm2 \\
-2*c_{23}*c_{24}/gm1/gm2 + c_{23}*c_{24}/gm1/gm2 \\
-C_{11}*C_{12}*c_{24}*Cf1/Cf2/gm1/gm2 + C_{11}*C_{12}*c_{24}*Cf1/Cf2/gm1/gm2 \\
-C_{11}*c_{23}*c_{24}/Cf2/gm1/gm2 + C_{11}*c_{23}*c_{24}/Cf2/gm1/gm2 \\
-C_{11}*c_{23}*Cf1/gm1/gm2 + C_{11}*c_{23}*Cf1/gm1/gm2 \\
-C_{11}*c_{24}*Cf1/gm1/gm2 + C_{11}*c_{24}*Cf1/gm1/gm2 \\
-C_{12}*c_{13}*c_{14}/Cf1/gm1/gm2 + C_{12}*c_{13}*c_{14}/Cf1/gm1/gm2 \\
-C_{12}*C_{13}*c_{14}/Cf2/gm1/gm2 + C_{12}*C_{13}*c_{14}/Cf2/gm1/gm2 \\
-C_{12}*c_{13}*Cf1/gm1/gm2 + C_{12}*c_{13}*Cf1/gm1/gm2 \\
-C_{12}*c_{13}*Cf2/gm1/gm2 + C_{12}*c_{13}*Cf2/gm1/gm2 \\
-C_{13}*C_{13}/gm1/gm2 + C_{13}*C_{13}/gm1/gm2 \\
-C_{14}*C_{14}/gm1/gm2 + C_{14}*C_{14}/gm1/gm2 \\
-C_{23}*C_{23}/gm1/gm2 + C_{23}*C_{23}/gm1/gm2 \\
-C_{24}*C_{24}/gm1/gm2 + C_{24}*C_{24}/gm1/gm2 \\
-c_{13}*c_{23}/gm1/gm2 + c_{13}*c_{23}/gm1/gm2 \\
-c_{13}*c_{24}/gm1/gm2 + c_{13}*c_{24}/gm1/gm2 \\
-c_{14}*c_{23}/gm1/gm2 + c_{14}*c_{23}/gm1/gm2 \\
-c_{14}*c_{24}/gm1/gm2 + c_{14}*c_{24}/gm1/gm2 \\
-c_{23}*c_{24}/gm1/gm2 + c_{23}*c_{24}/gm1/gm2 \\
-c_{24}*c_{24}/gm1/gm2 \\
B = \\
-2*C_{11}*c_{23}*c_{24}/Cf1/gm1/gm2 + C_{11}*c_{23}*c_{24}/Cf1/gm1/gm2 \\
-2*C_{12}*c_{14}*c_{24}/Cf2/gm1/gm2 + C_{12}*c_{14}*c_{24}/Cf2/gm1/gm2 \\
-2*C_{11}*c_{13}*c_{14}/Cf1/gm1/gm2 + C_{11}*c_{13}*c_{14}/Cf1/gm1/gm2 \\
-2*C_{12}*c_{13}*c_{23}/Cf2/gm1/gm2 + C_{12}*c_{13}*c_{23}/Cf2/gm1/gm2 \\
-2*c_{13}*c_{14}*c_{23}*c_{24}/Cf1/Cf2/gm1/gm2 + c_{13}*c_{14}/Cf2/gm1 \\
-2*c_{13}*c_{14}/gm1/gm2 + c_{13}*c_{14}/gm1/gm2 \\
-2*c_{13}*c_{23}/gm1/gm2 + c_{13}*c_{23}/gm1/gm2 \\
-2*c_{13}*c_{24}/gm1/gm2 + c_{13}*c_{24}/gm1/gm2 \\
-2*c_{14}*c_{23}/gm1/gm2 + c_{14}*c_{23}/gm1/gm2 \\
-2*c_{14}*c_{24}/gm1/gm2 + c_{14}*c_{24}/gm1/gm2 \\
-2*c_{23}*c_{24}/gm1/gm2 + c_{23}*c_{24}/gm1/gm2 \\
-C_{11}*C_{12}*c_{24}*Cf1/Cf2/gm1/gm2 + C_{11}*C_{12}*c_{24}*Cf1/Cf2/gm1/gm2 \\
-C_{11}*c_{23}*c_{24}/Cf2/gm1/gm2 + C_{11}*c_{23}*c_{24}/Cf2/gm1/gm2 \\
-C_{11}*c_{23}*Cf1/gm1/gm2 + C_{11}*c_{23}*Cf1/gm1/gm2 \\
-C_{11}*c_{24}*Cf1/gm1/gm2 + C_{11}*c_{24}*Cf1/gm1/gm2 \\
-C_{12}*c_{13}*c_{14}/Cf1/gm1/gm2 + C_{12}*c_{13}*c_{14}/Cf1/gm1/gm2 \\
-C_{12}*C_{13}*c_{14}/Cf2/gm1/gm2 + C_{12}*C_{13}*c_{14}/Cf2/gm1/gm2 \\
-C_{12}*c_{13}*Cf1/gm1/gm2 + C_{12}*c_{13}*Cf1/gm1/gm2 \\
-C_{12}*c_{13}*Cf2/gm1/gm2 + C_{12}*c_{13}*Cf2/gm1/gm2 \\
-c_{13}*C_{13}/gm1/gm2 + c_{13}*C_{13}/gm1/gm2 \\
-c_{14}*C_{14}/gm1/gm2 + c_{14}*C_{14}/gm1/gm2 \\
-c_{23}*C_{23}/gm1/gm2 + c_{23}*C_{23}/gm1/gm2 \\
-c_{24}*C_{24}/gm1/gm2 + c_{24}*C_{24}/gm1/gm2 (A3.20)

(A3.21)
Appendix 4, Input & Output bands in a sampled-data system

To show:

That, in calculating the response:

\[ H_{N}(\omega_{in}, \omega_{out}) = \sum_{n=0}^{N-1} H_{n}(\omega_{out}), e^{-j2\pi n/N} \]  \hspace{1cm} (A4.1)

for given input and output bands, \( b_{in} \) and \( b_{out} \), that:

\[ M = \frac{B_{out} - B_{in}}{2} \text{ for } B_{out} - B_{in} \text{ even} \]
\[ M = \pm \frac{B_{out} + B_{in} - 1}{2} \text{ for } B_{out} - B_{in} \text{ odd} \]  \hspace{1cm} (A4.2)

given that:

\[ \omega_{in} = \omega_{out} - M \omega_{s} \]  \hspace{1cm} (A4.3)

where:

\[ B_{x} = |b_{x}| \]  \hspace{1cm} (A4.4a)

and \( b_{x} \) is defined by:

\[ (b_{x} - 1) \frac{\omega_{s}}{2} \leq \omega_{x} < b_{x} \frac{\omega_{s}}{2} \text{ for } b_{x} \geq 1 \]
\[ b_{x} \frac{\omega_{s}}{2} \leq \omega_{x} < (b_{x} + 1) \frac{\omega_{s}}{2} \text{ for } b_{x} \leq -1 \]  \hspace{1cm} (A4.4b)

**Proof:**

**Case 1:** \( b_{in} \geq 1, b_{out} \geq 1 \)

Combining (A4.3) and (A4.4) gives:

\[ \frac{b_{out} - 1}{2} - \frac{b_{in}}{2} < M < \frac{b_{out}}{2} - \frac{b_{in} - 1}{2} \]  \hspace{1cm} (A4.5)

if we define:

\[ \Delta \equiv b_{out} - b_{in} \]  \hspace{1cm} (A4.6)

then (A4.5) may be written:

\[ \frac{\Delta - 1}{2} < M < \frac{\Delta + 1}{2} \]  \hspace{1cm} (A4.7)

which has no solution for \( \Delta \) odd, but for \( \Delta \) even gives:

\[ M = \frac{\Delta}{2} \]  \hspace{1cm} (A4.8)

Following a similar method it can be shown that:

**Case 2:** \( b_{in} \leq 1, b_{out} \geq 1 \)

No solution for \( \Delta \) even, but for \( \Delta \) odd:
Case 3: $\text{bin} \geq 1$, $\text{bout} \leq 1$:

No solution for $\Delta$ even, but for $\Delta$ odd:

$$M = \frac{\Delta+1}{2}$$  \hspace{1cm} (A4.10)

The case $\text{bin} \leq 1$, $\text{bout} \leq 1$ is of no interest and so, collecting the above results:

<table>
<thead>
<tr>
<th>$M$</th>
<th>$\Delta$</th>
<th>$\text{bout}$</th>
<th>$\text{bin}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(\text{bout}-\text{bin})/2$</td>
<td>even</td>
<td>positive</td>
<td>positive</td>
</tr>
<tr>
<td>$(\text{bout}-\text{bin}-1)/2$</td>
<td>odd</td>
<td>positive</td>
<td>negative</td>
</tr>
<tr>
<td>$(\text{bout}-\text{bin}+1)/2$</td>
<td>odd</td>
<td>negative</td>
<td>positive</td>
</tr>
</tbody>
</table>

Now from (A4.4a):

$$B_{\text{in}} = |b_{\text{in}}|, \quad B_{\text{out}} = |b_{\text{out}}|$$  \hspace{1cm} (A4.11)

This gives:

<table>
<thead>
<tr>
<th>$M$</th>
<th>$\Delta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(B_{\text{out}}-B_{\text{in}})/2$</td>
<td>even</td>
</tr>
<tr>
<td>$\pm (B_{\text{out}}+B_{\text{in}}-1)/2$</td>
<td>odd</td>
</tr>
</tbody>
</table>

where the positive sign is taken for $b_{\text{in}} \leq 1$ and the negative sign for $b_{\text{out}} \leq 1$. This proves the correctness of (A4.2), as required.

In practice, if $\omega_{\text{in}}$ (resp. $\omega_{\text{out}}$) is the independent variable then $b_{\text{in}}$ (resp. $b_{\text{out}}$) is taken to be positive. Thus the positive sign is used if $\omega_{\text{out}}$ is the independent variable in the calculations, else the negative sign is used.