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All-MBE grown InAs/GaAs quantum dot lasers with thin Ge buffer layer on Si substrates

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Abstract

A high-performance III-V quantum-dot (QD) laser monolithically grown on Si is one of the most promising candidates for commercially viable Si-based lasers. Great efforts have been made to overcome the challenges due to the heteroepitaxial growth, including threading dislocations (TDs) and anti-phase boundaries (APBs), by growing a more than 2 μm thick III-V buffer layer. However, this relatively thick III-V buffer layer causes the formation of thermal cracks in III-V epi-layers, and hence a low yield of Si-based optoelectronic devices. In this paper, we demonstrate a usage of thin Ge buffer layer to replace the initial part of GaAs buffer layer on Si to reduce the overall thickness of the structure, while maintaining a low density of defects in III-V layers and hence the performance of the InAs/GaAs QD laser. A very high operating temperature of 130 °C has been demonstrated for an InAs/GaAs QD laser by this approach.

Keywords: QD laser, thin Ge buffer layer, MBE

1. Introduction

Driven by the ever-growing data throughput worldwide, contemporary communication systems demand tremendous data transmission speed and bandwidth, and low power consumption inside data centres. Under these circumstances, Si-based photonic integrated circuit (PIC) has emerged as a promising candidate to fulfil these requirements. Most of the passive components in PIC have already been realised, coming with a great progress towards a fully Si-based PIC [1-4]. However, a reliable and electrically pumped Si-based laser that can be directly integrated into these PICs, remains a scientific challenge. Because of the indirect bandgap nature of Group-IV bulk materials, Si and Ge are difficult to be fabricated as efficient light emitters [5-8]. By contrast, III-V compound semiconductors with direct bandgaps demonstrate robust optical properties and provide an efficient gain medium for a laser source [9-15]. Although hybrid integration of III-V photonic components on Si substrates has been pursued with some success, in the long term, monolithic growth of III-V on Si is superior in terms of lower material cost and higher

production yield [16-18]. Nevertheless, monolithic growth of III-V material on Si is very challenging. The large lattice mismatch, incompatible thermal expansion coefficients and different symmetry between Si and the III-V materials lead to the generation of threading dislocations (TDs), thermal cracks and anti-phase boundaries (APBs), respectively [19-24]. All these defects generate non-radiative recombination centres, and hence dramatically hinder the laser performance in terms of operating temperature, output power and reliability [24, 25]. Previously, III-V buffer layers with thickness of more than 2 μm were extensively used to reduce the density of TD and suppress the propagation of APBs. However, this relatively thick III-V buffer layer leads to the formation of thermal cracks as the total thickness of III-V layers on Si for III-V lasers over 5 μm [20]. The formation of thermal cracks will significantly reduce the yield of Si-based III-V lasers. Therefore, a reduction of III-V buffer thickness represents an essential step towards full integration of III-V-on-Si optoelectronic circuits in the future.

Quantum dots (QDs), which provide 3-dimensional quantum confinement of carriers, have attracted extensive

scientific research in the last few decades [26, 27]. A laser that using III-V QDs as gain medium offers low threshold current density, high temperature performance and long lifetime, which surpasses its quantum-well (QW) counterparts [25, 28-33]. Moreover, QD structure is believed to be more defect-insensitive compared with bulk and QW structures. TDs easily produce a large amount of non-radiative recombination centres when penetrating through QW or bulk materials. However, TD can only “kill” a few QDs without affecting the others, hence the performance of a QD-based device will not significantly degrade [17]. The impressive performance of III-V QD lasers monolithically grown on Si can be also attributed to an efficient reduction of defect density during the epitaxial growth. In order to prevent the formation of APBs, Si substrates with 4-6° misorientation towards [110] have been used to form bi-atomic height Si steps [34, 35]. In addition, it has been demonstrated that strained-layer superlattices (SLSs), acting as dislocation filter layers (DFLs), sufficiently reduce the TD density (TDD) from $1 \times 10^{10} \text{ cm}^{-2}$ to around 10^6 cm^{-2} before they propagate into the gain medium [17, 21]. Such a solution demands a thick III-V buffer layer to allow the use of an adequate number of DFLs, which leads to the appearance of thermal cracks due to the release of the built-in thermal strain. Replacing part of GaAs buffer layer with a thin and low-defect-density Ge layer is considered as an economical solution to prevent cracking without affecting device performance negatively. Here it should be noted that Ge is widely used to replace Si as the p-channel in CMOS devices on the Si platform, as its hole mobility is four times higher than that of Si [36].

Developing an InAs/GaAs QD laser device monolithically grown on Ge/Si virtual substrate (VS) has achieved remarkable progresses [37, 38], but all high-quality Ge/Si VSs were manufactured by metal-organic chemical vapour deposition system and then transferred into molecular beam epitaxy (MBE) system for further laser structure epitaxy. However, this method complicates the fabrication procedure for high performance MBE-grown InAs QD laser grown on Ge/Si VS and increases the cost of manufacturing. An all-MBE grown InAs/GaAs QD laser and Ge buffer on Si substrates are thus highly desired as it will not only reduce the growth cost but also simplify the integration process. Unfortunately, there is rarely an III-V MBE equipped with a Ge effusion cell along with an ultra-high temperature heating stage ($>1000^\circ\text{C}$) to provide high quality thin Ge epi-layers. If Ge and III-V epi-layers are grown in separate MBE chambers, it is crucial to keep the Ge epi-layer perfectly clean and smooth during the transfer of wafer between MBE chambers, as the presence of any contaminants such as oxides, carbon or other organic impurities will lead to formation of defects in the subsequent III-V epitaxy. In this work, an InAs/GaAs QD laser on a Ge/Si VS was grown by a twin-chamber MBE system, consisting of a Group-IV and a III-V chamber. The Ge buffer layer was grown on a Si substrate in the Group-IV chamber before transferring to the III-V chamber for III-V epitaxy. An ultra-high-vacuum transfer chamber between these two chambers is used to keep a pure and smooth Ge epi surface before GaAs growth, to avoid potential contamination

during the wafer transfer process. Here, an implementation of a thin Ge layer in the InAs/GaAs QD laser structure has been demonstrated to reduce the total thickness of the III-V layer while maintaining a low TDD level. Lasing was observed up to 130°C under pulsed operation for InAs/GaAs QD lasers grown on a Ge/Si VS by using this unique twin MBE system.

2. Crystal Growth and device fabrication

In this work, InAs/GaAs QD laser structure was grown on Si substrate. An n-type Si (100) substrate with 4° offcut toward [110] was used in this study to prevent the formation of APBs while depositing polar III-V materials on non-polar Group-IV substrates. *In-situ* deoxidisation process was performed for the Si substrate at 1100°C for 20 min in Group-IV MBE chamber prior to the growth. In order to understand the propagation of TDs in the GaAs buffer layer on Ge/Si VS and Si substrate, two samples were grown for comparison. One sample contains a 300-nm-thick Ge/Si VS and a 350-nm-thick GaAs buffer before the deposition of DFLs, while the other sample only contains 650 nm GaAs in the buffer layer. Note that the growth conditions were identical for both samples during the growth of all subsequent layers. The laser structure is shown schematically in Figure 1, containing an optimised 300 nm Ge/Si VS [39]. The growth started with a three-step growth technique for the thin Ge layer. The first two Ge layers were grown at 250°C and 500°C for 50 and 100 nm, respectively. Five-cycle *in-situ* annealing between a high temperature of 850°C and a low temperature of 450°C were then carried out with a 5-minute hold time applied at both temperatures. This approach helps to enhance the mobility of TDs and thus promote their self-annihilation. Finally, a 150-nm-thick Ge cap layer was grown at 600°C to smooth the surface. After the growth of the Ge/Si VS, the wafer was transferred from Group-IV chamber to the III-V chamber through an ultra-high vacuum chamber for the further III-V epitaxy. This was followed by the deposition of a Ga pre-layer on Ge, which is believed to provide a better surface morphology than As pre-layer technique in forming single-domain GaAs [9]. In order to enhance the material quality, four sets of $\text{In}_{0.18}\text{Ga}_{0.82}\text{As}/\text{GaAs}$ SLS DFLs were implemented [40], after the growth of 350 nm of GaAs in the buffer layer. Each set of DFL consists of five repetitions of $\text{In}_{0.18}\text{Ga}_{0.82}\text{As}/\text{GaAs}$ SLSs followed by a 300-nm-thick high temperature grown GaAs spacer layer were grown to suppress the propagation of TDs. *In-situ* thermal annealing was carried out for the SLS to enhance the mobility of TDs and thus increase the probability of TD annihilation. After that, a 1300 nm n-type doped $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ cladding layer and a 30 nm un-doped $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ were deposited. The active region is formed by seven-layer InAs/GaAs dot-in-well (DWELL) structure separated by a 42 nm GaAs spacer layer [41], in which part of the GaAs is p-type doped. Each layer of DWELL consists of 2.7 monolayers of InAs grown on a 2 nm

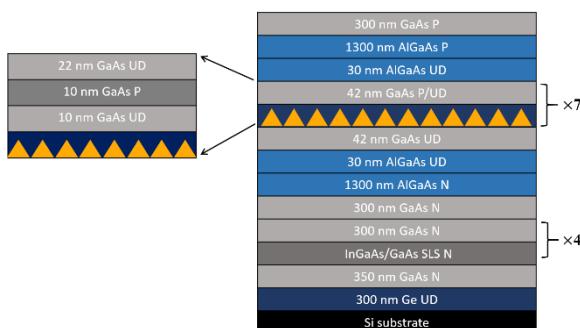


Figure 1. Schematic diagram of the InAs/GaAs QD laser structure grown on Si substrates.

In_{0.18}Ga_{0.82}As layer and capped with a 6 nm In_{0.18}Ga_{0.82}As layer. Above the active region, another 30-nm-thick un-doped Al_{0.4}Ga_{0.6}As guiding layer and 1300 nm of p-type doped Al_{0.4}Ga_{0.6}As were grown. Finally, a 300 nm p-type GaAs contact layer completed the growth. The surface morphology of all grown samples was analysed by atomic force microscopy (AFM) in standard tapping mode. The optical properties of the InAs/GaAs QDs are examined by the photoluminescence at room temperature. Transmission electron microscopy (TEM) was used to investigate the propagation of TDs in the buffer layer as well as in the DWELL active region. Electron channelling contrast imaging (ECCI) was used to investigate the crystallographic properties of the grown samples. The laser characteristics of the fabricated InAs/GaAs QD laser devices were measured under pulsed conditions, where a pulse width of 1 μ s and 1% duty cycle were used.

The broad-area InAs QD laser device was fabricated with a stripe width of 25 μ m using standard photolithography and wet chemical etching techniques. The ridge was etched to about 200 nm above the active region. Ti/Pt/Au and Ni/GeAu/Ni/Au were deposited on the p+ GaAs contact layer and exposed n+ GaAs buffer layer to form the p- and n-metal contacts, respectively. After thinning the Si substrate to around 120 μ m, the laser bar was cleaved into the desired cavity length of 3 mm, and no highly reflective coating was applied to the mirror facets.

3. Results and discussions

Figure 2 (a) and (b) show cross-sectional TEM images of TD propagation in III-V buffer layers grown directly on Si substrate and on the Ge/Si VS, respectively. A high density of TDs is generated at the GaAs/Si interface and Ge/Si interface due to large lattice mismatch between materials. As shown in Figure 2(a), most of the defects generated at the GaAs/Si interface are confined within the first ~150 nm of the GaAs region thanks to the 2-step growth method [10, 21]. However, the TDs propagate freely upward before meeting the first DFL with a high density value of $\sim 10^9$ cm⁻² [17]. In contrast, the TDs generated at the Ge/Si interface have a significant lower density in the thin Ge layer as a result of high temperature

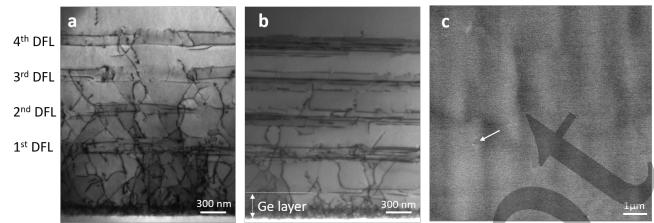


Figure 2. Cross-sectional bright-field TEM results of (a) GaAs buffer layer grown on Si substrate and (b) GaAs buffer layer grown on Ge/Si VS. Both (a) and (b) have the same total thickness and consist of 4-set DFLs. (c) ECCI image showing TDD level for GaAs buffer layer grown on Ge/Si VS after 4th DFL. Arrow indicates single TD observed on the surface.

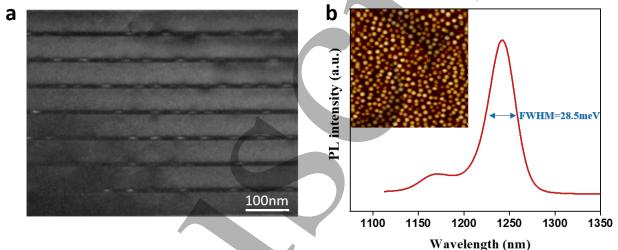


Figure 3. (a) Cross-sectional dark field TEM image of a defect-free 7-layer QDs active region. (b) Room-temperature photoluminescent spectrum of the InAs/GaAs QD active region. Inset: a $1 \times 1 \mu\text{m}^2$ AFM image of uncapped InAs QDs grown on a Ge/Si VS.

cyclic thermal annealing, as shown in Figure 2(b). The thermal stress induced by cyclic thermal annealing enhances the glide of TDs and thus promotes self-annihilation of TDs, during the growth of the thin Ge epilayer [42, 43]. A TDD of $\sim 6 \times 10^8$ cm⁻² is obtained after the growth of this 300 nm Ge layer, which is similar to TDD level after the first DFL for GaAs monolithically grown on Si [17, 39]. Since Ge has an almost identical lattice constant to GaAs, a very limited number of misfit dislocations is introduced during the epitaxy of GaAs on Ge, leading to few additional TDs propagating towards DFLs. As shown in Figure 2 (a) and (b), the SLSs can effectively suppress the propagation of TDs. A reduction of TDD can be clearly observed as TDs pass through each set of DFLs. The built-up strain inside of SLS forces TDs to bend at the SLS interface and propagate towards the wafer edge, hence increasing the possibility of TD annihilation. A final TDD of 4×10^6 cm⁻² is obtained after the four sets of DFLs, as indicated in the ECCI image shown in Figure 2(c). Nevertheless, Figure 2(b) shows that after three sets of DFLs, no TDs are observed; the final DFL may be unnecessary and an optimised buffer layer with lower thickness is feasible.

Figure 3(a) illustrates a visible defect-free active region, demonstrating the high effectiveness of the DFLs and Ge growth shown in Figure 2(b). The optical properties of these QDs are shown in Figure 3(b), where a room temperature photoluminescence emission peak wavelength at ~ 1250 nm with a narrow full width at half maximum (FWHM) of 28.5

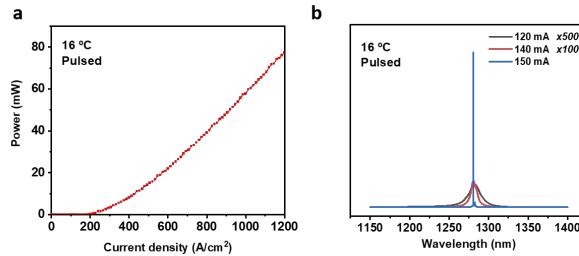


Figure 4. (a) LI measurement of InAs/GaAs QDs monolithically grown on a Ge/Si VS under pulsed operation at 16°C . (b) Emission spectra of InAs/GaAs QDs monolithically grown on a Ge/Si VS with various injection current under pulsed operation at 16°C .

meV were obtained. A typical AFM image of uncapped QDs grown under the same growth conditions as those in the laser structure on the Ge/Si VS is shown in the inset of Figure 3(b), which suggests a QD density of $5 \times 10^{10} \text{ cm}^{-2}$.

Figure 4(a) shows the light-against-current (LI) measurement of the InAs/GaAs QD laser monolithically grown on Ge/Si VS under pulsed operation at 16°C . The measured laser threshold current density is about $200 \text{ A}/\text{cm}^2$, corresponding to $28.6 \text{ A}/\text{cm}^2$ per QD layer. The maximum output power of $\sim 78 \text{ mW}$ was obtained from a single facet when the injection current density reached $1200 \text{ A}/\text{cm}^2$. The emission spectra of InAs/GaAs QD laser monolithically grown on Ge/Si VS with various injection currents at 16°C are presented in Figure 4(b). At a low injection current of 140 mA , only amplified spontaneous emission is present. Once the injection current increases to 150 mA , a typical laser emission with a peak wavelength of 1279 nm can be clearly observed.

Since robust temperature stability is necessary to support a laser device working under extreme conditions, the InAs/GaAs QD laser grown on Ge/Si VS was tested at a range of operating temperatures, as illustrated in Figure 5(a). The maximum operating temperature of 130°C was achieved for the InAs/GaAs QD laser grown on Ge/Si VS. However, 130°C is the upper limit of our temperature controller. Since no thermal rollover is noticed when the laser operates at 130°C , it suggests this device can work at even higher temperatures. The characteristic temperature T_0 is calculated as 153.4 K between 16°C and 36°C , and it decreases to 48.4 K from 36°C to 130°C as a result of increased carrier escaping rate at higher temperatures, as shown in Figure 5(b) [25]. This T_0 result is comparable with the previously best reported InAs laser grown on Ge/Si VS with p-type modulation doped active regions [38]. In addition, this laser device demonstrates a highly stable slope efficiency from 16°C to 130°C . Although a sharp reduction of the slope efficiency is observed from 16°C to 36°C , it remains constantly at $\sim 0.03 \text{ W/A}$ from 36°C to 66°C . The slope efficiency decreases at an increasing rate as the thermal escape of carriers happens more frequently at higher temperatures, as presented in Figure 5(c). The slope efficiency measured at 130°C remains $\sim 1/3$ of the value measured at 16°C , indicating the laser device has high thermal stability.

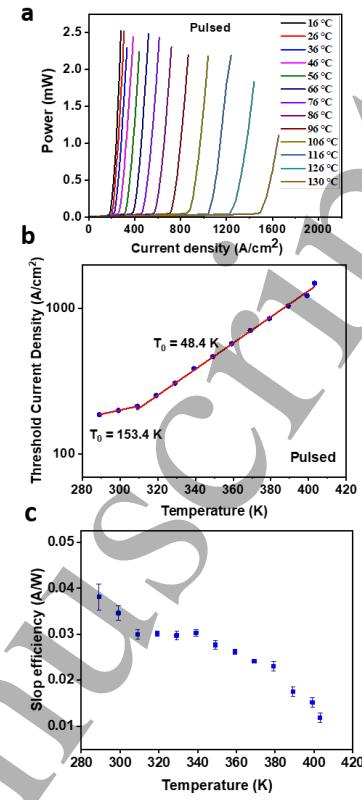


Figure 5. (a) LI measurements at various temperatures under pulsed mode. (b) Characteristic temperature T_0 calculated under pulsed mode from 289 K to 403 K . (c) The variation of slope efficiency calculated under pulsed mode from 289 K to 403 K .

4. Conclusion

In this paper, we have demonstrated a high-performance InAs/GaAs QD laser grown directly on a Si substrate with a thinner buffer layer. With the help of high temperature cyclic thermal annealing of the thin Ge buffer layer, a dramatic reduction in the TDD can be observed before the TDs propagate into the DFLs. Fewer sets of DFLs are hence feasible in an InAs/GaAs QD laser structure. Employing the Ge/Si VS helps to eliminate thermal cracking issues and thus is expected to boost the total yield. In order to test the feasibility of implementing a thin Ge buffer layer in the InAs QD laser structure, an InAs QD laser device was grown directly on the Ge buffer. The laser threshold current density under pulsed operation was measured as $200 \text{ A}/\text{cm}^2$, corresponding to $28.6 \text{ A}/\text{cm}^2$ for each QD layer. A maximum output power of $\sim 78 \text{ mW}$ was obtained from a single facet. Lasing was observed up to 130°C . Further improvements in threshold current density and temperature performance are possible with further optimising the growth and fabrication processes. This work demonstrates the feasibility of replacing a part of the thick GaAs buffer layer with a thin Ge layer, without affecting the laser performance, and forms a basis for

- improving output yield for monolithic integration of Si photonics in the future.
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- ### Disclosures
- The authors declare no conflicts of interest.
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