InP DHBT Single-Stage and Multiplicative Distributed Amplifiers for Ultra-wideband Amplification

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***Abstract*—This paper highlights the gain-bandwidth merit of the single stage distributed amplifier (SSDA) and its derivative multiplicative amplifier topologies (i.e. the cascaded SSDA (C-SSDA) and the matrix SSDA (M-SSDA)), for ultra-wideband amplification. Two new monolithic microwave integrated circuit (MMIC) amplifiers are presented: an SSDA MMIC with $7.1\,\mathrm{dB}$ average gain and $200\,\mathrm{GHz}$ bandwidth; and the world's first M-SSDA, which has a $12\,\mathrm{dB}$ average gain and $170\,\mathrm{GHz}$ bandwidth. Both amplifiers are based on an Indium Phosphide DHBT process with $250\,\mathrm{nm}$ emitter width. To the authors best knowledge, the SSDA has the widest bandwidth for any single stage amplifier reported to date. Furthermore, the three tier M-SSDA has the highest bandwidth and gain-bandwidth product for any matrix amplifier reported to date.**

***Index Terms*—Distributed amplification, Single stage distributed amplifier, InP, MMIC, matrix amplifier, ultra-wideband amplifier.**

I. Introduction

Applications such as high resolution imaging, optoelectronic and instrumentation systems continue to drive demand for ultra-wideband integrated circuitry [2]. There are two key elements required to meet this demand: first is the availability of integrated circuit (IC) processes with ultra-wide bandwidth potential at appreciable gain, and the other is the development of circuit design techniques that maximise this potential. On the one hand, advancements in IC fabrication technology continue to deliver processes with increasingly higher gain-bandwidth potential, creating the enabling technology to meet ultra-wideband demands. On the other hand, however, there is the need for circuit design topologies and techniques that optimise these new generation devices and enable them to deliver maximum benefits in performance [2], [3]. For instance, an InP HBT process with 130 nm emitter width, developed by Teledyne Scientific Company (TSC), has an extrapolated f_T of 521 GHz and f_{max} of $1.15\,\mathrm{THz}$ at bias condition of $V_{CE} = 1.6$ V and $I_C = 6.9$ mA. At $600\,\mathrm{GHz}$, a single $130\,\mathrm{nm}$ HBT is expected to have approximately $6\,\mathrm{dB}$ gain [2], [3], however, realizable gain is expected to be much lower, as the matching network losses at hundreds of GHz frequencies are quite high, and transistors may only be practically operated at some fraction of their f_{max} [2], [4].

For over eighty years, the concept of distributed amplification, which allows the absorption of the bandwidth-limiting intrinsic capacitances of active devices into artificial transmission lines (ATLs) [5]–[7], has been employed in the design of amplifiers with bandwidth performance approaching the terahertz frequency bands (i.e. 0.3 - 3 THz) [1], [8], [9]. The conventional distributed amplifier (DA), as shown in Fig. 1, comprises of multiple gain cells with an additive gain mechanism. A signal applied at the input travels down the input ATL towards R_{TERM} where it is absorbed. The travelling voltage wave excites each transistor (Q_1 to Q_N), and transfers the signal to the output ATL through the transistor transconductance g_m. In the most commonly used scenarios, where the multistage amplifier is constructed from transistors of equal gains and the phase velocities of both lines are equal, the amplified signal from each of the transistors are all in phase and they add in the forward direction towards the output [6], [7], [10], [11]. It has also been shown that the input and output ATLs may also be purposively kept unequal, to provide specific gain [12] and filtering advantages [13], [14], with application in specialist communication systems.

More recently, in [15], the viability of a single stage distributed amplifier (SSDA) was demonstrated, showing that the distributed effect required to achieve the wideband performance in multistage DAs can also be observed in a SSDA. This was followed up by the introduction of the cascaded SSDA (C-SSDA), which improves the utility of the SSDA topology by providing additional gain at similar bandwidth, through a multiplicative gain mechanism [16]–[18]. The concept of the matrix SSDA (M-SSDA) was introduced in [19], as an alternative to the C-SSDA, with simulated results for an M-SSDA based on full foundry InP DHBT presented. The multiplicative gain mechanism of these topologies make them particularly attractive, as they make it possible to achieve significantly higher gain-bandwidth product performance, with fewer gain cells than the conventional, additive DA. Both derivative topologies of the SSDA have been described as *multiplicative DAs* in [1] due to their gain mechanism.

In this paper, we highlight the merits of the SSDA topology,

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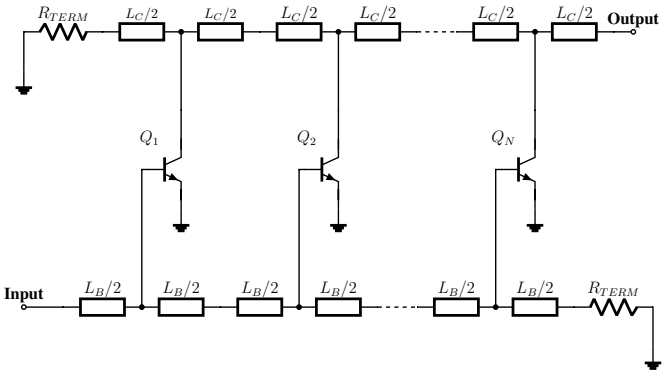
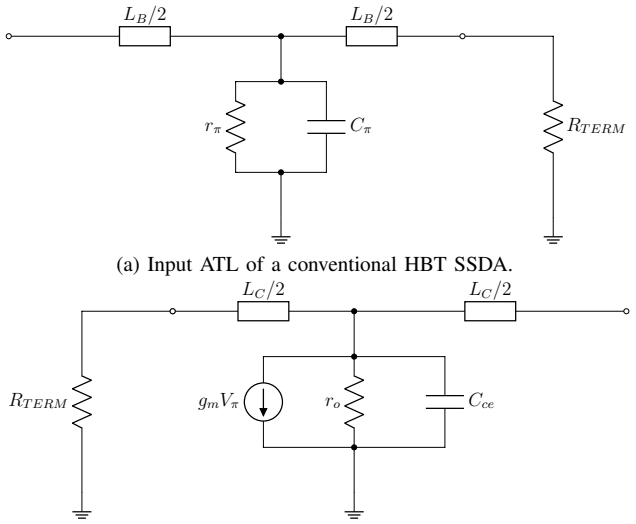


Fig. 1: Schematic diagram of the conventional bipolar DA, with N gain stages. L_B and L_C are the input and output inductances per gain stage, repectively, required to achieve distributed effect, and R_{TERM} is the terminating resistance of the input and output ATL.



(a) Input ATL of a conventional HBT SSDA.

(b) Output ATL of a conventional HBT SSDA.

Fig. 2: Simplified equivalent circuits of the input and output ATLs of the HBT SSDA. C_π and r_π are the capacitance and dynamic resistance, respectively, at the base-emitter junction; C_{ce} collector-emitter junction capacitance; and r_o is the output resistance of the HBT.

and its derivative M-SSDA, for the design of ultra-wideband amplifiers by considering its gain, bandwidth and noise potentials. We also report two new monolithic microwave integrated circuit (MMIC) amplifiers, based on an indium phosphide (InP) DHBT process with $250\,\mathrm{nm}$ emitter width: an SSDA MMIC with $7.1\,\mathrm{dB}$ gain and $200\,\mathrm{GHz}$ bandwidth, with a high frequency gain tuning range of $5\,\mathrm{dB}$ to $12\,\mathrm{dB}$; and the world's first M-SSDA, a three-tier device, with $12\,\mathrm{dB}$ gain and $170\,\mathrm{GHz}$ bandwidth. The outline of this paper is as follows: Section II discusses the merits of the SSDA and the M-SSDA for ultrawideband amplification, considering the gain, bandwidth and noise performance. In Section III, the design and measurement of the new SSDA and M-SSDA MMICs are presented. Section IV concludes the paper.

II. Merit of the SSDA and the M-SSDA for Ultra-wideband Amplification

A. The SSDA

The SSDA topology offers an advantage in achieving ultra-wideband performance, when compared to the conventional multi-stage DA. This advantage is attributed to the minimal high-frequency attenuative effects from the shorter lengths of transmission lines required in the SSDA. This merit is even more valuable in the design of DAs based on HBTs, as these have a forward biased PN junction between the base and the emitter, resulting in a complex characteristic impedance on the input ATL, as identified in [20], [21] and shown in Fig. 2 [11], [20], [22], [23]. This complex input nature of HBTs generally results in worse termination mismatch and higher input reflection with additional stages [9], [24]. Furthermore, the gentle frequency response roll-off of the single stage low-pass filters that make up the input and output ATLs of the SSDA is easily compensated for, using available attenuation compensation and bandwidth extension techniques, such as those presented in [24]–[27].

The SSDA, however, has two main limitations: limited gain from the single gain cell and lower signal to noise ratio compared to the conventional multi-stage DA. These limitations and how they may be addressed are discussed subsequently.

1) Gain limitation of SSDAs: The gain (G_{DA}) of the conventional DA is given by [6], [7], [11]

$$G_{DA} = \frac{1}{4} N^2 g_m^2 Z_{o-in} Z_{o-out}, \tag{1}$$

where N is the number of stages, g_m is the transconductance of the active device, and Z_{o-in} and Z_{o-out} are the image impedances of the input and output transmission lines, respectively.

$$Z_{o-in} = \sqrt{\frac{L_B}{C_\pi}\left(1 - \frac{\omega^2 L_B C_\pi}{4}\right)} \tag{2}$$

$$Z_{o-out} = \sqrt{\frac{L_C}{C_{ce}}\left(1 - \frac{\omega^2 L_C C_{ce}}{4}\right)} \tag{3}$$

with $L_B = R_{TERM}^2 C_\pi$ and $L_C = R_{TERM}^2 C_{ce}$.

For a $50\,\Omega$ SSDA (i.e. $N = 1$), G_{DA} is limited by g_m, which is quite low for high f_T devices. The issue of limited gain has been addressed through multiplicative DA topologies - formed from cascading or arranging SSDAs in a matrix [9], [10], [16], [19], [24], [28]–[30].

2) Noise performance limitation of SSDAs: While the SSDA topology presents notable advantages in wideband performance and design simplicity, with higher gain available from its multiplicative derivatives, it has a poorer signal-to-noise behaviour compared to multi-stage DAs. A notable merit of multi-stage DAs is that with each additional stage, the overall noise figure reduces in the amplifier passband, improving SNR at the output - a merit that the SSDA and its derivative amplifiers do not share [31]–[34]. However, the inherent flexibilities of the DA topology provide options for

noise performance optimisation based on available trade-offs. This may be observed by considering the noise factor (F) of a HBT-based SSDA which is derived as [30]

$$F = 2 + \frac{4}{g_m^2 Z_{\pi b} Z_{\pi c}} + Z_{\pi c}\left[\left(\frac{i_b g_m^2 Z_{\pi b}}{4}\right)^2 + \left(\frac{i_d}{2}\right)^2\right], \quad (4)$$

where $Z_{\pi b}$ and $Z_{\pi c}$ are the π-image impedances of the input and output transmission lines of the HBT SSDA; and i_b and i_c are the base and collector noise generators of the HBT, given respectively by [35], [36],

$$\overline{i_b^2} = 4kT_oBRe(Y_{ebp} - Y_{ce}) + 2kT_oBg_{be} \quad (5)$$

and

$$\overline{i_c^2} = 2kT_oBg_m \quad (6)$$

where $Y_{ebp} = gm\sqrt{2j\omega\tau_D}/\tanh\sqrt{2j\omega\tau_D}$ is the hole admittance of the emitter junction; $Y_{ce} = gm\sqrt{2j\omega\tau_D}/\sinh\sqrt{2j\omega\tau_D}$ is the transfer admittance of the transistor; τ_D is the diffusion time through the base region; and g_{be} is the total input conductance [35], [36]. It may be seen from (4), that F can be reduced by making $Z_{\pi b}$, larger. This would also increase the gain of the amplifier but the bandwidth would be reduced commensurately [30], [34]. A similar observation can be made for the FET-based SSDA, where F is derived as [32]

$$F = 2 + \frac{4}{g_m^2 Z_{\pi d} Z_{\pi g}} + \frac{Z_{\pi g}\omega^2 C_{gs}^2 R}{g_m} + \frac{4P}{g_m Z_{\pi g}}, \quad (7)$$

with C_{gs} being the input (gate-source) capacitance of the active device; R and P are dimensionless coefficients from Van der Ziel's FET noise behaviour model that depend on bias conditions, device geometry and other technological parameters [37]; and $Z_{\pi d}$ and $Z_{\pi g}$ being the π-image impedances of the input and output transmission lines of the SSDA. It is also observed that the overall noise factor can be reduced by making $Z_{\pi g}$, larger [32].

B. The M-SSDA

The M-SSDA is essentially two or more single stage distributed amplifiers (SSDA) connected by intermediate transmission lines, forming a *M* × *1* matrix structure. The schematic of an M-SSDA with *M* common-emitter gain tiers is shown in Fig. 3. The input and output transmission lines of the M-SSDA are the same as in the SSDA, shown in Fig. 2a and Fig. 2b, respectively. The simplified equivalent circuit of the intermediate transmission line is shown in Fig. 4, where L_{CB} is the inductance required to achieve distributed effect for the combined capacitance at the intermediate nodes of the matrix amplifier, with image impedance Z_{o-int} given by [19]

$$Z_{o-int} = \sqrt{\frac{L_{CB}}{C_\pi + C_{ce}}\left(1 - \frac{\omega^2 L_{CB}(C_\pi + C_{ce})}{4}\right)} \quad (8)$$

with $L_{CB} = R_{TERM}^2(C_\pi + C_{ce})$ [7], [38].

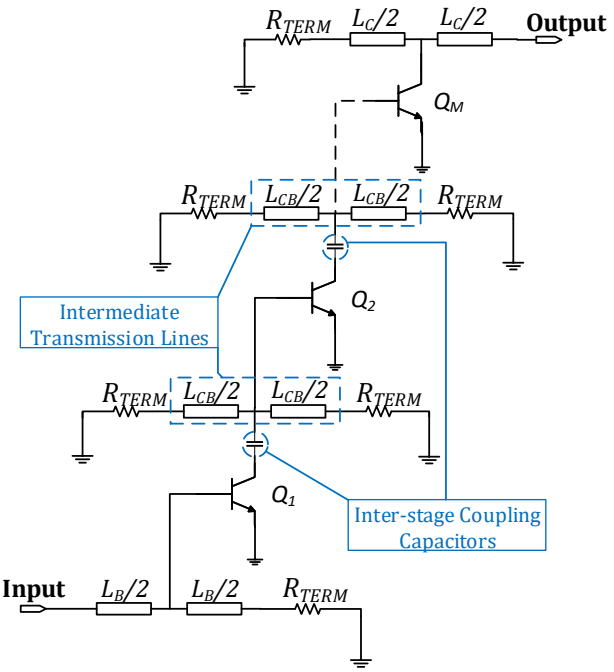


Fig. 3: Schematic diagram of a M-SSDA, with *M* gain tiers, forming an M × 1 matrix structure. L_{CB} is the inductance of the intermediate transmission line.

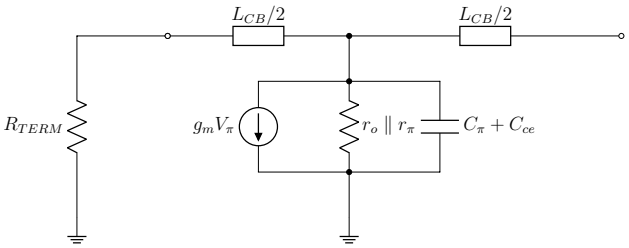


Fig. 4: Simplified equivalent circuits of the intermediate ATLs of the HBT M-SSDA.

The gain of the M-SSDA, G_M, given by [19]

$$G_M = \frac{1}{4} g_m^2 Z_{o-int}^{2(M-1)} Z_{o-in} Z_{o-out}, \quad (9)$$

The line impedances of the input (Z_{in}), intermediate (Z_{int}) and output (Z_{out}) transmission lines, are given by (10), (11) and (12), respectively, for the simplified CE M-SSDA:

$$Z_{in} = \frac{j\omega L_B}{2} + \frac{r_\pi\left(j\omega\frac{L_B}{2} + R_o\right)}{r_\pi + \left(R_o + j\omega\frac{L_B}{2}\right)(1 + j\omega r_\pi C_\pi)} \quad (10)$$

$$Z_{int} = \frac{j\omega L_{CB}}{2} + \frac{r_\pi \parallel r_o\left(j\omega\frac{L_{CB}}{2} + R_o\right)}{r_\pi \parallel r_o + \left(R_o + j\omega\frac{L_{CB}}{2}\right)(1 + j\omega\left(C_\pi + C_{ce}\right) r_\pi \parallel r_o)} \quad (11)$$

$$Z_{out} = \frac{j\omega L_C}{2} + \frac{r_o\left(j\omega\frac{L_C}{2} + R_o\right)}{r_o + \left(R_o + j\omega\frac{L_C}{2}\right)(1 + j\omega r_o C_{ce})} \quad (12)$$

The bandwidth of the M-SSDA is dominated by the cut-off frequency of the intermediate transmission line $f_{c(int)}$,

$$f_{c(int)} = \frac{1}{\pi\sqrt{L_{CB}\left(C_{\pi} + C_{ce}\right)}} \tag{13}$$

Both the C-SSDA and M-SSDA topologies make it possible to achieve significantly higher gain than is available from the conventional multi-stage DA, for the same number of active devices, while preserving the bandwidth advantage. The merit of the SSDA and its derivative multiplicative DA is highlighted by the fact that some of the DAs with the highest bandwidth and gain-bandwidth product (GBP) of any process technology and topology are based on the SSDA [9], [29], [39].

While the M-SSDA is a functional equivalent of the C-SSDA, in that they both share the same gain mechanism [19], there is a structural distinction. The C-SSDA consists of a number of unique SSDAs with the output of one connected to the input of the other (as shown in Fig. 5) [9], [16], [17]; while the M-SSDA is conventionally a multi-tier single structure, due to the presence of intermediate lines connecting the output of one tier to the input of the next tier [19]. In the design of cascaded DAs, it is essential that the individual amplifiers are designed to give a gain response as flat as possible up to the desired maximum frequency [40]. With matrix amplifiers, the fact that the output transmission line of a lower stage would form the input line of the stage above it, means that the stages cannot be individually optimised and then combined. Hence, these intermediate transmission lines must be designed to distribute the resultant capacitance of both stages that it connects.

The matrix topology, however, offers some advantages when compared to the cascaded topology, such as potentially higher gain, because both the forward and reverse waves on the intermediate transmission lines are amplified by the gain stage in the tier above them, whereas the reverse wave is absorbed by the drain line termination in the cascaded DA [10], [41], [42]; an inherent reverse isolation over wide bandwidths at reduced size [42]; better input and output matching with lower noise figure [33], [43]; reduced MMIC circuit footprint and, consequently, lower production cost [43]; and a potential for significantly less phase delay, when compared to the conventional distributed amplifier - an important feature for applications requiring good phase tracking [43].

In addition to the gain merit of multiplicative DAs, the topology also provides some noise optimisation potentials. The noise performance of the multiplicative DA is also limited by constraints similar to the SSDA, and overall noise marginally increases with additional stages, as opposed to multi-stage DAs. However, the multi-tier structure of multiplicative DAs present trade-offs that may be explored towards achieving gain/bandwidth/noise performance goals. For instance, in [34], it was established that multiplicative DAs follow the noise scaling mechanism of cascaded systems, such that the overall noise factor of the amplifier is primarily determined by the noise factor of the first gain stage. Hence, a viable design approach is to make the noise factor of the first stage of the multiplicative DA as low as possible, at appreciable single stage gain. This may be achieved by designing the input transmission line at a higher image impedance and by adopting a transistor with a wider bandwidth potential i.e lower input capacitance (and correspondingly lower g_m) in the first stage. With this approach, the loss in bandwidth from using a higher image impedance input line is offset by the inherent wider bandwidth of the transistor, while from (9), the gain is kept at an appreciable level by increasing Z_{o-in}.

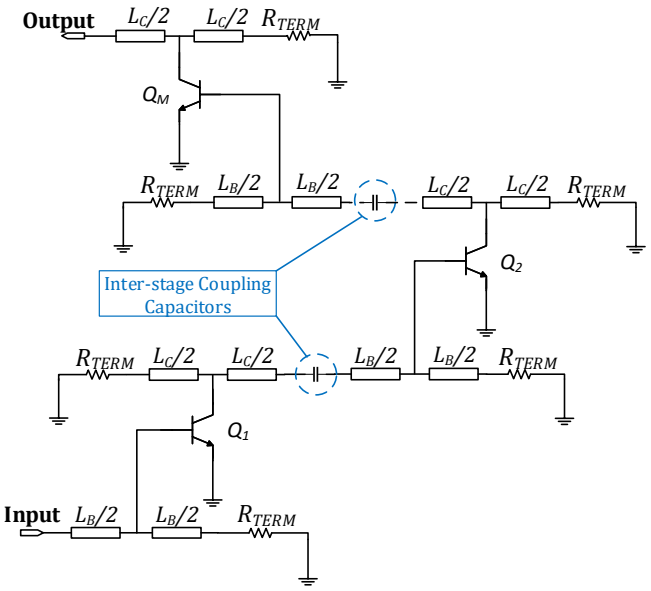


Fig. 5: Schematic diagram of a C-SSDA, with M gain tiers.

III. MMIC Amplifier Design and Measurement

We report the design and measurment of two amplifiers: an SSDA and an M-SSDA. Both amplifiers are based on an InP DHBT process with f_T/f_{max} of 350 GHz / 600 GHz [44], with a representative schematic shown in Fig. 6 [44].

A. SSDA with 7.1 dB Gain and 200 GHz Bandwidth

We report a SSDA which is suitable as a gain unit in a multiplicative DA topology. The amplifier features a cascode gain cell with two identical InP DHBTs, each with an emitter area of $0.25\,\mu\text{m} \times 6\,\mu\text{m}$. The cascode configuration is favoured for the high input-output isolation it offers, as well as the high output impedance which advantageously reduces the loading on the output transmission line of the DA [29], [46]. To improve bandwidth performance, the input transmission line is scaled down by a factor $\zeta \approx 0.5$ and peaked by a shunt capacitance $C_{peak} = \frac{1}{2}C_{\pi}$, where C_{π} is the input (base-emitter junction) capacitance of the active device [24], creating a similar effect to the application of a radial stub [47]. The loss compensation technique described in [24] was employed, involving the addition of peaking inductances L_{cc} and L_{ce} to the cascode gain cell, with L_{cb} added to maintain stability [24], [25]. Fig. 7a shows the SSDA schematic featuring the applied modifications. The fabricated MMIC occupies an area of $460\,\mu\text{m}$ x $620\,\mu\text{m}$ and is shown in Fig. 7b.

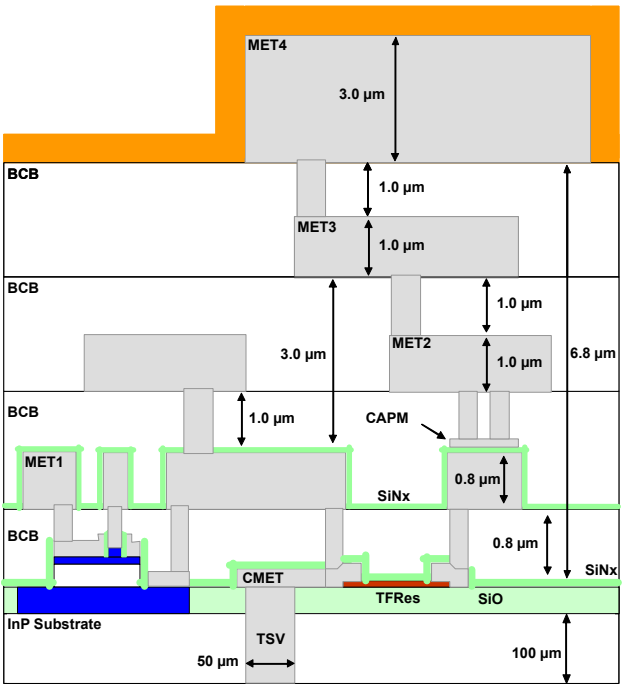
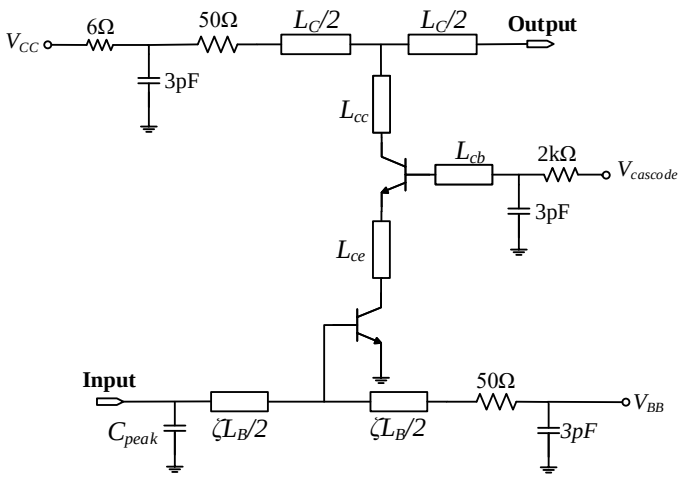
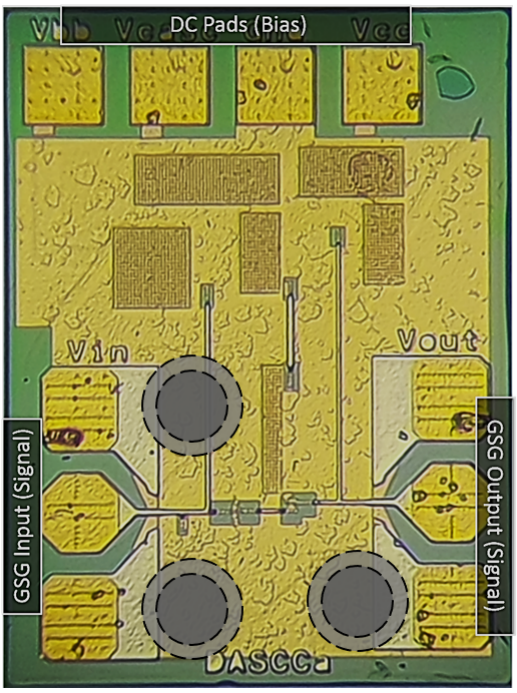


Fig. 6: IC interconnect cross-section showing low loss THz microstrip lines and high density thin-film interconnects [44], [45] and through-substrate vias (TSV).



(a) Schematic circuit of SSDA with scaled input line, shunt capacitance and adapted loss compensation.



(b) Microphoto of SSDA. Footprint: 460 µm x 620 µm. Dashed circles indicate location of through-substrate vias.

Fig. 7: SSDA: Circuit diagram and MMIC microphotograph

The verification of the amplifiers performance was done via small-signal on-probe measurements. Due to the wide bandwidth of the amplifier, two different measurement setups were required to characterize it. The low frequency response of the amplifier was measured on probe in the band 100 MHz – 120 GHz with the VectorStar ME7838A series broadband VNA by Anritsu via 75 µm 145 GHz Infinity probes. The input power was set to -20 dBm to avoid saturating the amplifier. The high frequency response in the band between 140 GHz – 220 GHz was measured with PNA-X N5247A by Keysight using VDI WR-5.1 frequency extenders and WR-5.1 waveguide probes. The input power was set and calibrated at -10 dBm to accommodate for the optimal operation of the frequency extenders. The limitations of the measurement equipment did not allow measurement in the 120 GHz – 140 GHz band. In both setups, the measurement reference plane was calibrated to the probe tips via certified calibration substrates. The SSDA was biased at I_B =0.63 mA, V_{CC} =5.2 V, $V_{cascode}$ =3.5 V and I_C =12.4 mA.

Fig. 8 shows the results of the two measurements along with the simulated performance of the amplifier. There is good agreement between the simulated and the measured forward gain $S21$ in terms of the bandwidth of 200 GHz (the bandwidth is defined as the -3 dB point below the average gain across the amplifier passband [48]). However, with average measured gain at 7.1 dB, there is an average shortfall in gain of $\sim$2.5 dB compared to the simulated response across the device bandwidth. The input and output reflection curves show good matching to the predicted results in the lower frequencies. There is also a high reverse isolation, $S12$, of less than -30 dB up to 120 GHz, and less than -15 dB in throughout the passband. In the higher frequency range, the measured results show some ripples on both input reflection ($S11$) and output reflection ($S22$) curves around 150 GHz and 200 GHz as seen in Fig. 8, that were not predicted in pre-fabrication simulations.

Post-measurement simulations were carried out to assess the effects of ground inductance, with results presented Fig. 9. It was observed that ground inductance (e.g from parasitics from DC bias probes) of $\geq$10 pH could result in $S22$ ripple between 160 GHz and 190 GHz, as reflected in the measured $S22$ (Fig. 8). Additionally, full EM simulations of the input and output GSG pads, substrate, ground plane slots, and through-substrate vias revealed that the substrate could sustain resonant modes at 170 GHz and 190 GHz, which also manifest as

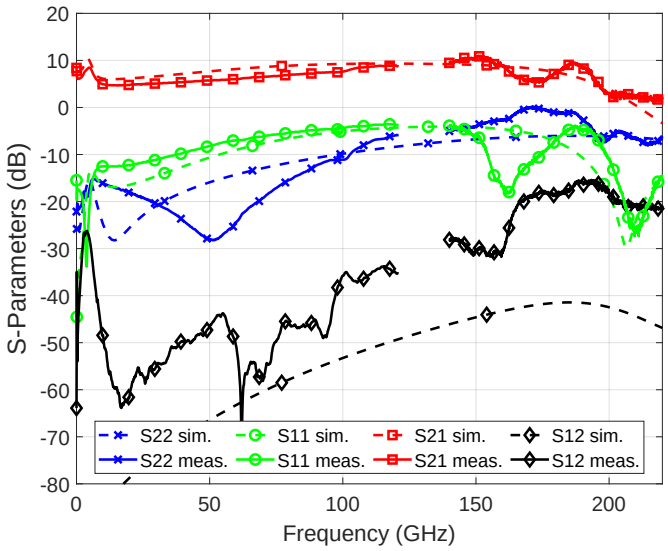


Fig. 8: Comparison of simulated and measured responses for the SSDA: simulated response - dashed lines; measured response - solid lines.

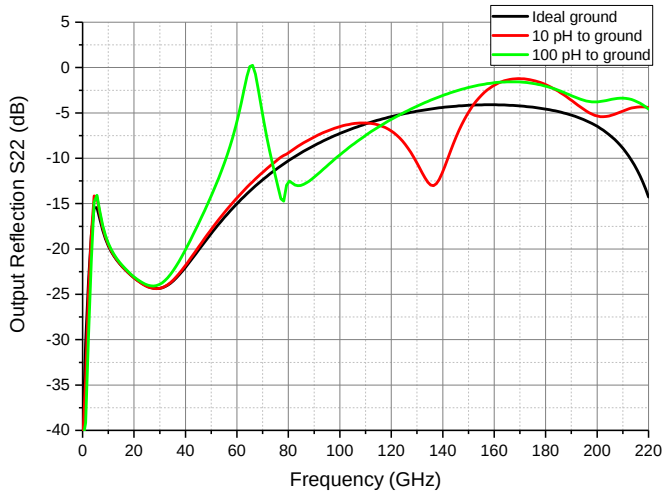


Fig. 9: Effects of ground inductance on output reflection coefficient.

dips in the forward gain curve. The substrate resonant modes resulted from the low density of through-substrate vias on the MMIC. The effect of these resonances in addition to the DC bias probe parasitics account for the output reflection coefficient approaching 0 dB. The Smith chart plot of $S11$ and $S22$ are presented in Fig. 10, and also show potential instability within this frequency range. This effect is in accordance to what has been shown in in [49], however due to the use of through-substrate vias and back-plane metallization in the proposed amplifier, it was not possible to use resistive silicon substrate, as prescribed in [49]. In line with design using similar processes, it is expected that both effects would be mitigated by packaging the MMIC, as this would improve both the decoupling and the grounding of the amplifier. A tricode gain cell could also be employed in place of the cascode gain cell, to increase maximum stable gain [50].

A comparison of the amplifier with state-of-the-art DAs in

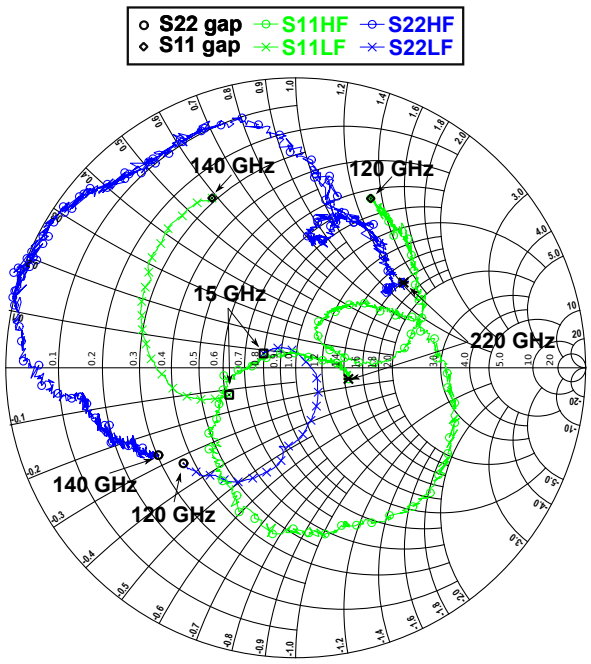


Fig. 10: Smith chart plot of $S11$ and $S22$ of the SSDA. The amplifier is potentially unstable in the upper frequency band, due to resonant modes at frequencies close to 160 GHz and 190 GHz. LF - Low frequency (100 MHz - 120 GHz); HF - High frequency (140 GHz - 220 GHz); "gap" is the frequency range from 120 GHz to 140 GHz, which is not covered in the measurement due to equipment limitations.

Table I. Particular focus is given to InP-based DAs; and SSDAs and multiplicative DAs to allow for like-for-like comparison. The bandwidth (BW), gain, GBP, DC power (P_{DC}), GBP/P_{DC} (a figure-of -merit that provides a measure of the DC power efficiency of wideband amplifiers), area of the MMIC chip and DA topology are compared. The SSDA reported in this paper has the highest bandwidth to date of reported single stage designs and is only outperformed by the 2-cascaded-SSDA in [9].

B. 3×1 M-SSDA with 12 dB gain and 170 GHz bandwidth

A three-tier M-SSDA has been designed and laid out as a MMIC. This amplifier is also based on the bandwidth optimisation technique adopted for the SSDA, and features an emitter follower (EF) input buffer [19]. A schematic of the 3-M-SSDA is presented in Fig. 11, with an inset showing the modified cascode gain cell. The design is also based on the same InP DHBT IC process used for the SSDA. Relatively large ($\sim$3 pF) inter-stage capacitors were used in the circuit to reduce the low-frequency cutoff and improve baseband operation.

Fig. 12 shows the microphotograph of the fabricated MMIC matrix-SSDA, with actual dimension of 770 µm $\times$ 800 µm. The verification of the amplifier performance was also done via small-signal on-wafer probe measurements using two measurement setups - 100 MHz - 120 GHz; and 140 GHz - 220 GHz, with the same vector network analyzer setups as described in Section III. The M-SSDA required eight voltage sources to bias its three stages: three base voltage sources

TABLE I: Comparison of SSDA with state-of-the-art DAs in literature.

Technology	**BW (GHz)**	**Gain (dB)**	**GBP (GHz)**	P_{DC} **(mW)**	**GBP/**P_{DC} **(GHz/mW)**	**Area (mm^2)**	**DA Topology**	**Ref.**
250 nm InP DHBT	241	$10 \pm 2^*$	762	387	2.00	0.82	6-stage Cascode	[8]
250 nm InP DHBT	207	13.5 ± 2	979	210	4.66	0.29	4-stage Cascode**	[51]
500 nm InP DHBT	175	$12 \pm 2^*$	697	180	3.87	0.975	5-stage tricode	[50]
250 nm InP DHBT	182	$10 \pm 2^*$	575	110	5.23	0.33	4-stage Cascode	[52]
250 nm InP DHBT	192	7.5 ± 1	455	40	11.38	0.24	SSDA	[9]
250 nm InP DHBT	235	16 ± 2	1480	117	12.65	0.41	2-Cascaded-SSDA	[9]
130 nm SiGe BiCMOS	170	$13 \pm 1^*$	759	74	10.26	0.22	4-Cascaded-SSDA	[53]
130 nm SiGe BiCMOS	175	16 ± 4	1102	360	3.06	0.38	2-Cascaded-SSDA	[28]
250 nm **InP DHBT**	**200**	**7.1 $\pm$ 3.5**	**455**	**67**	**6.79**	**0.28**	**SSDA**	**This Work**

* There were no comments on the gain ripple in these publications, so the gain ripple has been estimated from the s-parameter plot.
** CC: Common collector.

(V_{BB1}, V_{BB2} and V_{BB3}); three collector voltage sources V_{CC1}, V_{CC2} and V_{CC3}; one voltage source to bias the three common-base transistors forming the cascode of each gain cell (denoted by $V_{cascode}$); and one voltage source to bias the EF input buffer (denoted by V_{EF}). This required two additional DC power supply units compared to the measurement setup, used in characterising the SSDA, and an additional $150\,\mu\mathrm{m}$ pitch DC probe. For ease of tunability, two Keysight ES6312A triple output programmable DC power supply units were used to supply the base bias and cascode voltages, while the DC supply function of an Hewlett-Packard 4145B semiconductor parameter analyzer was used for collector and EF bias.

S-parameter measurements from the two measurement setups are presented as solid lines in Fig. 13, with the corresponding simulated curves presented as dashed lines. An average forward of gain of $12\,\mathrm{dB}$ and $170\,\mathrm{GHz}$ bandwidth was measured with good input and output matching of less than -$5\,\mathrm{dB}$ all through the measured bandwidth. The amplifier also has high reverse isolation $S12$ of less than $-40\,\mathrm{dB}$ up to $120\,\mathrm{GHz}$, and less than $-30\,\mathrm{dB}$ throughout the amplifier passband. A good degree of agreement between the simulated and measured responses may be observed in the $S21$ (dB), $S11$ (dB) and $S22$ (dB) up to $70\,\mathrm{GHz}$. A peaking in the $S21$ characterisation from $70\,\mathrm{GHz}$ to $120\,\mathrm{GHz}$ is attributed to the multiplicative effect of the peaking observed in the the same frequency range for the SSDA, as seen in Fig 8. However, for the higher frequency measurement, while the input and output reflection measurement closely matches prediction, the forward gain slightly deviates from the predicted profile, with a bandwidth-loss of $\sim 5\%$.

An electromagnetic (EM) simulation of the inter-stage coupling capacitors C_{BLOCK} and its peripherals presented in Fig. 14 (region enclosed with white dashed lines and labelled as 1, for tier 1 to tier 2 in Fig. 12) and EM coupling between transmission lines in the circuit revealed these as the main loss and bandwidth-limiting components. This observation is consistent with what is shown in [54]. Additionally, the large slots in the ground plane required by the inter-stage coupling capacitor structures resulted in significant crosstalk through the substrate which accounts for the gain peaking towards 110 GHz [55]. The region enclosed in black dashed lines (labelled as 2) in Fig. 12 indicates the location of the peaking inductances L_{ce} and L_{cc}; a region with relatively high EM coupling. These effects are shown in Fig. 15, which compares the simulated $S21$ gain without the EM simulation of the inter-stage capacitors with cases where either only the EM simulated capacitors are included or both the EM simulated capacitors and transmission line couplings are included. The Smith's chart plots of $S11$ and $S22$ are presented in Fig. 16, showing unconditional stability throughout the amplifier passband.

Table II presents a comparison of the new M-SSDA with the state-of-the-art matrix distributed amplifiers. The gain, BW, GBP, P_{DC}, GBP/P_{DC}, area of MMIC chip and the matrix configuration are compared. It is noted that the new M-SSDA has both the highest bandwidth and GBP of any matrix DA, albeit with a $10\,\mathrm{dB}$ mid-band peaking, due to parasitic effects from the large inter-stage capacitors.

IV. Conclusions

The peculiarities of the SSDA topology make it possible to operate new generation transistor processes close to their bandwidth limit and would be instrumental in making terahertz bandwidth amplification more practical. In this paper, we highlight the merits of the SSDA and its multiplicative derivatives in achieving ultra-wideband amplification, and we describe design approaches for gain, bandwidth and noise performance optimisation. We also present two new MMIC amplifiers: an SSDA and a three-tier M-SSDA. The SSDA amplifier has a measured gain of $7.1\,\mathrm{dB}$ and $200\,\mathrm{GHz}$ bandwidth and to the authors best knowledge, is the highest bandwidth reported for any SSDA. The three-tier M-SSDA measured a gain of $12\,\mathrm{dB}$

TABLE II: Comparison of the performance of new M-SSDA with other wideband matrix DAs.

Technology	Gain (dB)	Bandwidth (GHz)	GBP (GHz)	P_{DC} (mW)	GBP/P_{DC} (GHz/mW)	Area (mm^2)	Matrix Configuration	Ref.
0.18 µm CMOS	9.5 ± 1	50	149	420	0.35	1.54	2×4	[56]
0.18 µm CMOS	6.7 ± 3.5*	45.6	99	497	0.20	1.89	2×4	[57]
0.25 µm GaAs PHEMT	19 ± 1	19.5	174	270	0.644	7	2×4	[58]
0.25 µm GaAs PHEMT	18 ± 2	19.5	195	500	0.39	7	2×4	[58]
0.09 µm CMOS	15.4 ± 1	21	124	12.5	9.92	0.41	2×4	[59]
0.25 µm InP HBT	**12 ± 10**	**170**	**677**	**183**	**3.70**	**0.62**	**3 × 1**	**This Work**

*There were no comments on the gain ripple in this publication, so the gain ripple has been estimated from the s-parameter plot.

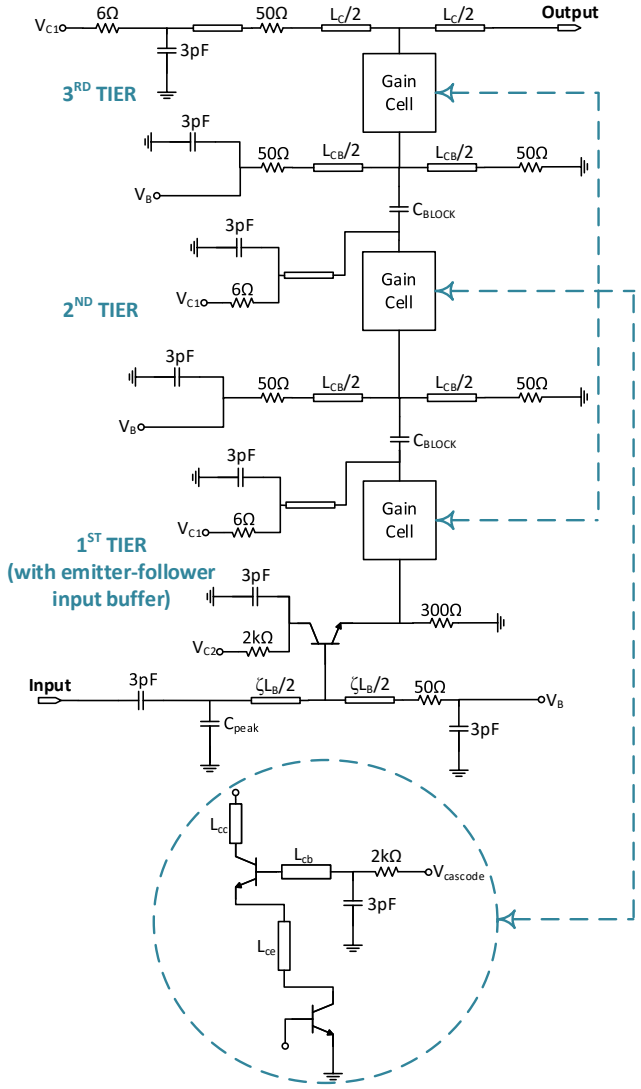


Fig. 11: Three-tier M-SSDA schematic with scaled input and intermediate transmission lines. Inset shows the modified gain cell. Modified from [19].

and 170 GHz bandwidth, which is the highest bandwidth and gain-bandwidth for any matrix amplifier reported in the literature. The M-SSDA results also underscore the critical compromise between achieving low and high frequency performance that arises from the size and the associated parasitic effects of the inter-stage coupling capacitances required in multiplicative DAs.

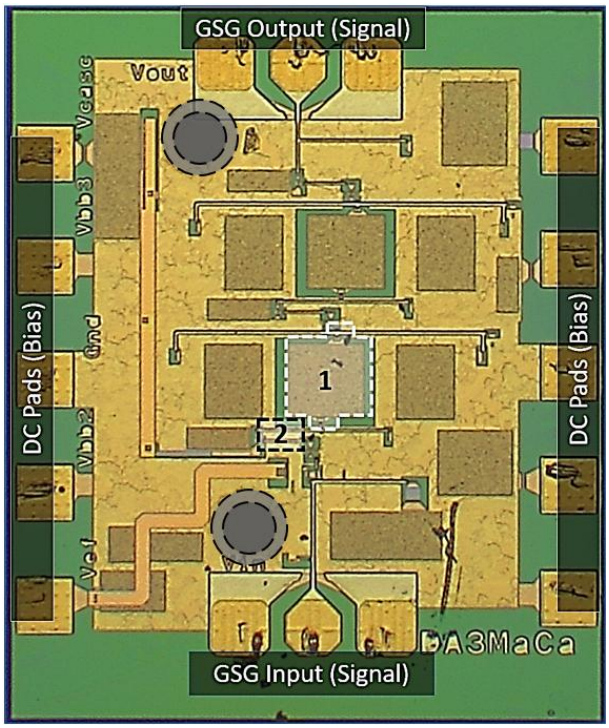


Fig. 12: Microphoto of the M-SSDA. Footprint: 770 µm × 800 µm. Region 1 (enclosed by white dashed lines) marks the location of the inter-stage capacitor C_{BLOCK} between tier 1 and tier 2, and the associated vias and metal connections; region 2 (enclosed by black dashed lines) marks the location of peaking inductances L_{ce} and L_{cc}. Dashed circles indicate location of through-substrate vias.

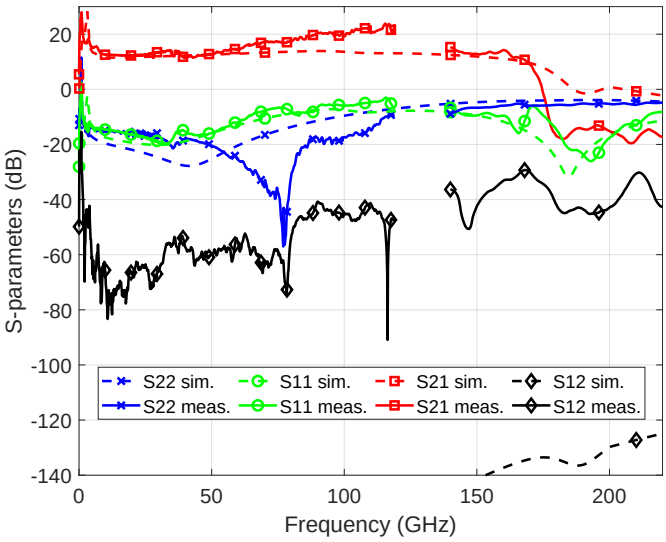


Fig. 13: Comparison of simulated and measured responses for the three-tier M-SSDA: simulated response - dashed lines; measured response - solid lines.

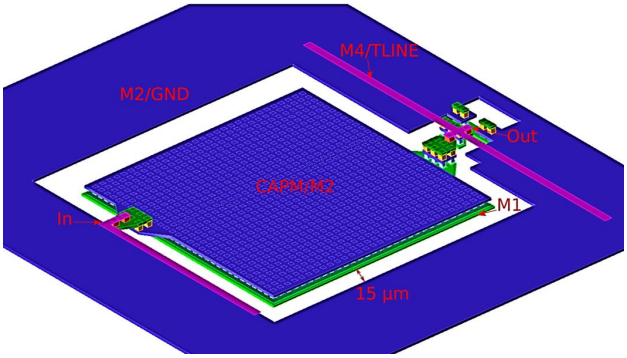


Fig. 14: Structure and interconnects of the inter-stage ac-coupling capacitors together with the input and output matching transmission lines, used in the E/M simulations.

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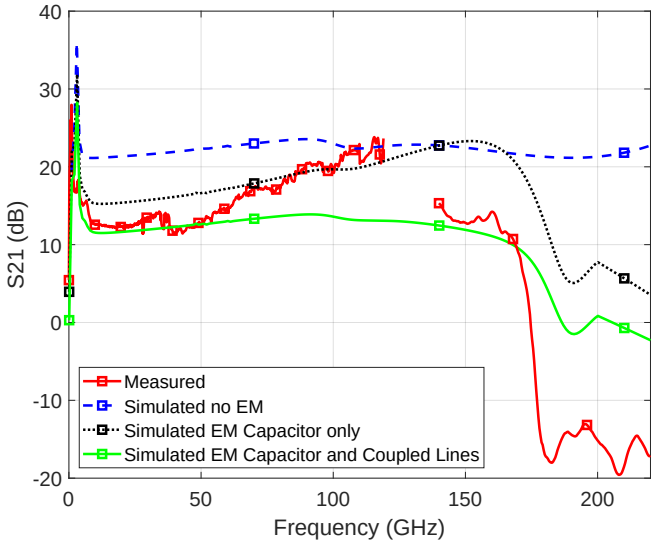

Fig. 15: Bandwidth-limiting effect of inter-stage coupling capacitors.

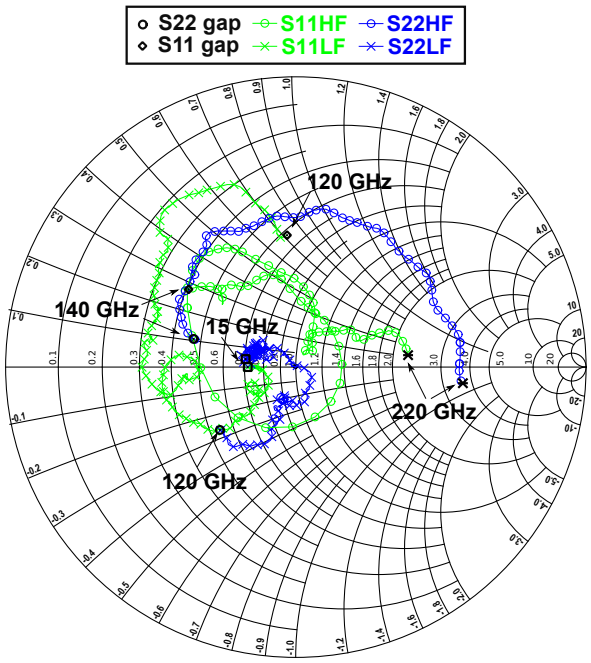

Fig. 16: Smith chart plot of S11 and S22 of the M-SSDA. The amplifier is unconditionally stable. LF - Low frequency (100 MHz - 120 GHz); HF - High frequency (140 GHz - 220 GHz); "gap" is the frequency range from 120 GHz to 140 GHz, which is not covered in the measurement due to equipment limitations.

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