Remote capacitive sensing in two-dimensional quantum-dot arrays

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Abstract

We investigate gate-induced quantum dots in silicon nanowire field-effect transistors fabricated using a foundry-compatible fully-depleted silicon-on-insulator (FD-SOI) process. A series of split gates wrapped over the silicon nanowire naturally produces a $2 \times n$ bilinear array of quantum dots along a single nanowire. We begin by studying the capacitive coupling of quantum dots within such a 2×2 array, and then show how such couplings can be extended across two parallel silicon nanowires coupled together by shared, electrically isolated, 'floating' electrodes. With one quantum dot operating as a single-electron-box sensor, the floating gate serves to enhance the charge sensitivity range, enabling it to detect charge state transitions in a separate silicon nanowire. By comparing measurements from multiple devices we illustrate the impact of the floating gate by quantifying both the charge sensitivity decay as a function of dot-sensor separation and configuration within the dual-nanowire structure.

Keywords: Quantum dots, Reflectometry, floating gate coupler, electrostatic coupling

Spin qubits in silicon demonstrate the fundamental properties required for scaled quantum computation, with state-of-the-art one- and two-qubit operations demonstrating control fidelities approaching the requirements for fault-tolerant quantum error correction.[1–4] While all control elements have been integrated into single devices with scalable readout mechanisms,[5] much effort is now being focused into developing these devices from simple laboratory prototype structures into scaled arrays of qubits capable of eventually yielding a quantum advantage.[6,7] The promise of a highly developed materials system and mature fabrication industry, together with the success of laboratory, and industry-grade prototype silicon-metal-oxide-semiconductor (SiMOS) quantum-dot based devices[8] has led to the proposition of several approaches to foundry-compatible scaling into grid-based architectures of quantum dot arrays. These approaches range from densely-packed qubits with next-nearest-neighbour couplings,[9] dot arrays partially-populated with qubits[10] and arrays with qubit sites linked via mediating structures for remote qubit-qubit coupling.[11]

SiMOS devices which form quantum dots in the corners of silicon nanowires naturally produce bilinear dot arrays,[12] which allow for proximal sensor integration for both charge[13–16] and spin states[17] through dispersive measurements using gate-based reflectometry. The advantages of these integrated sensors can be extended by mechanisms for *off-wire* coupling, to sense the state of dots located in remote locations within the quantum dot array. In order to enhance the capacitive coupling between spatially separated quantum dots, studies in planar GaAs/AlGaAs and Ge/Si heterostructures and carbon nanotubes have exploited a *floating gate*;[18–20] a metallic electrode which is galvanically isolated from, but capacitively coupled to, its immediate environment.

Here, utilising a single quantum dot sensor, we demonstrate a system capable of performing both proximal and remote capacitive charge sensing within a 2×4 array of quantum dots distributed across two parallel nanowires. We compare these results with geometrically identical single-wire variants, serving as an isolated 2×2 array. Each 2×2 array is formed on a single silicon nanowire (SiNW), and all devices described here are located in the same die, fabricated from a fully-depleted silicon-on-insulator (FD-SOI) process.[21] Our approach uses floating gate electrodes to capacitively couple a sensor dot to quantum dots on remote nanowires, whilst maintaining sensitivity to adjacent dots within the local nanowire. We quantify the sensitivity to charge movement within these two schemes by experimentally benchmarking the device capacitance matrix, supported by cryo-SiMOS simulations.

The scanning electron micrograph (SEM) image in Fig. 1(a) shows a device of the type

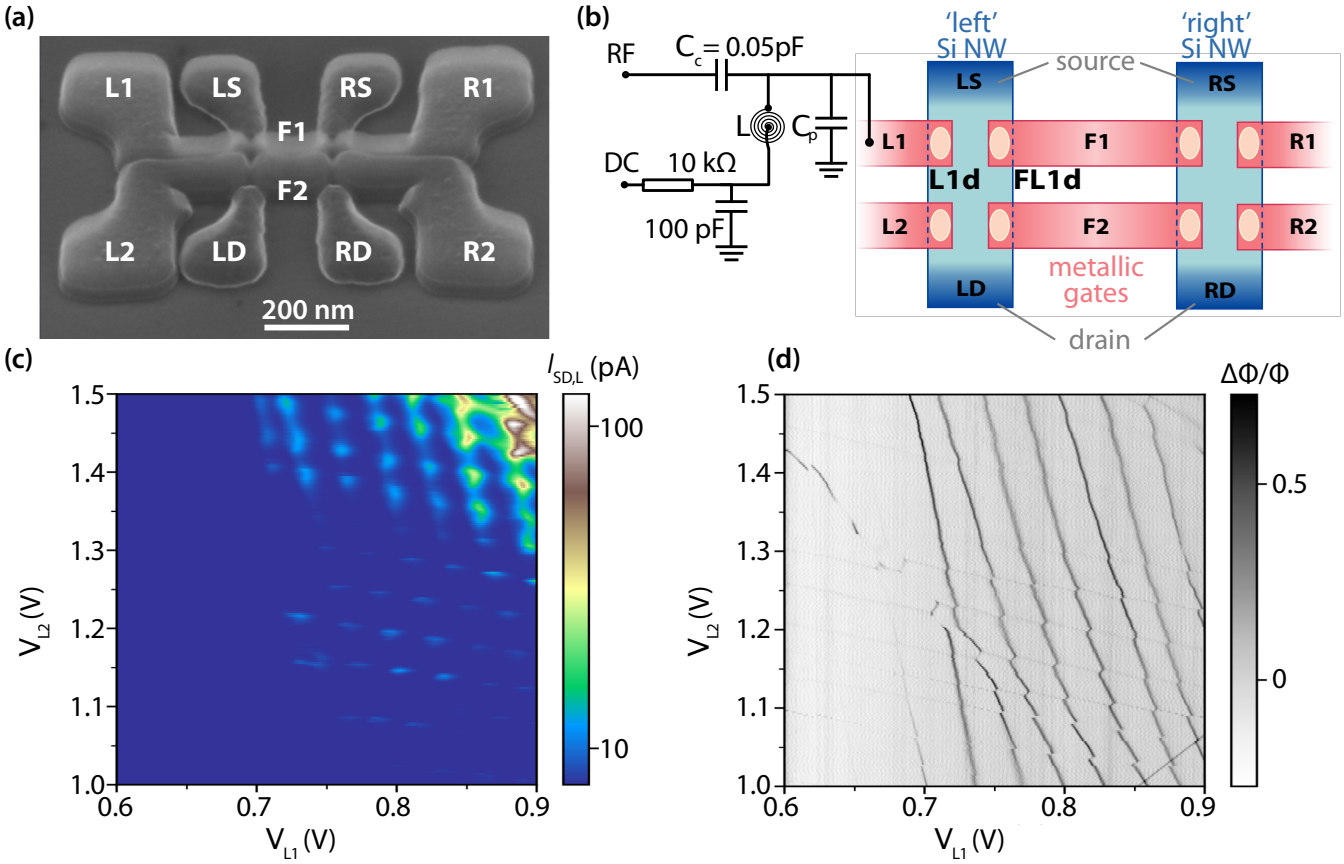

Figure 1: Device, measurement and configuration. (a) Oblique-angle Scanning Electron Micrograph illustrating the gate structure of the double-nanowire device coupled by two floating gates. (b) Cartoon of the gate structure and reflectometry circuit diagram. Charge transitions in a variety of quantum dots are detected by the 'single electron box' sensor under L1, including those in dots within the same (left, L) nanowire, or located remotely in an adjacent (right, R) nanowire, and detected capacitively through coupling facilitated by the floating gate. (c) Double-dot signatures within the left nanowire through a transport current map of gate L1 vs L2 voltage-space with a Source-Drain bias 4 mV. (d) A concurrent zero-biased reflectometry measurement illustrates dot-lead charge transitions of the L1 sensor dot and capacitive shifts due to addition of electrons to a local quantum dot defined under gate L2.

used in these remote sensing experiments. Two parallel nanowires, with centre-to-centre spacing of 200 nm, are fabricated with two central floating gates F1 and F2 wrapping the interior edges of both, spanning the gap between the two silicon structures. Gates F1 and F2 are capacitively coupled to the surrounding gates by proximity, but are otherwise electrically isolated. All gate structures are separated by a SiN spacer which increases cross capacitance. The device is further encapsulated by 300 nm of silicon oxide, above which an additional top gate T is deposited utilising a back-end metallisation layer (not shown). Full geometric details for the family of devices compared in this work can be found in Supplementary §I. The charge sensor for these experiments consists of a two-terminal structure in which a charge island is connected to single reservoir, known as a single electron box (SEB).[13–17] The sensor is configured under a single gate, L1, utilising the dot L1d, which is coupled to an electron reservoir and measured using the reflectometry circuit depicted in Fig. 1(b). With this configuration, the addition of electrons to the dots within the left nanowire can be inferred from either the transport current $I_{\mathrm{SD,L}}$ through the device with source-drain bias $V_{\mathrm{SD}} = 4$ mV, seen in Fig. 1(c), or the S_{11} reflectometry signal $\Delta\Phi/\Phi$ (measured at $V_{\mathrm{SD}} = 0$ V) seen in Fig. 1(d), which maps the same gate voltage space. Both measurements contain structure attributed to multiple dots within the 2×2 array of the left nanowire. Due to the low transport current through the device, discerning the occupancy of the dots via transport is a significant challenge, while the capacitive shifts due to the addition of an electron are readily detected in reflectometry, which can probe all proximal quantum dots down to the last electron transition (Supplementary §I). The SEB dot-lead transitions at lower SEB electron numbers are less visible due to the reduction in tunneling rates below the RF frequency of the reflectometry measurement.[22]

As the floating gates are galvanically isolated, we use the top metal gate T to assist in the accumulation of quantum dots under floating gates, primarily via the mutual capacitance between gates F1, F2 and T (see Supplementary §V). Simultaneously, both V_{L2} and V_{R2} are set to a depletion mode to avoid formation of quantum dots under gates L2, R2 and F2, to effectively 'shut-off' the lower half of the device by electron depletion. With the voltage sweep of V_{L1} and V_{R1} shown in Fig. 2(a), and noting the influence of the floating gate F1 which is capacitively coupled to both active gates, we can load electrons into dots L1d and R1d, as well as dots FL1d and FR1d, from their neighbouring reservoirs. Charge detection of these four distinct quantum dots is shown in the stability diagram measured in the reflectometry phase signal Fig. 2(a), and includes the remote sensing of dots FR1d and R1d, located in the 'right' SiNW, detected by the sensor dot L1d, located in the 'left' SiNW. The sensor dot L1d is estimated to hold ≈10 electrons in this voltage range, where dot-reservoir charge transitions can be observed directly as a phase peak. We can then identify the remaining three different quantum dots capacitively coupled to the sensor through two complementary approaches:

(1) Through the ratio of cross capacitance between the two active gate voltages V_{L1} and V_{R1} and the dot.

(2) Through direct charge detection by the sensor dot, assessing the magnitude of the capacitive shift upon the sensor.

For the voltage map between V_{L1} and V_{R1} shown in Fig. 2(a), each of the four dots capacitively couple to the L1 and R1 electrodes with differing strength, and we illustrate the four quantum dots present with reference to the colour code shown in the capacitance connectivity diagram of Fig. 2(c). In Figs. 2(a) and 2(b), the blue dashed line indicates dot-lead charge transition of the SEB, L1, which naturally has the highest lever arm to V_{L1}. The other three coloured dashed lines highlight each remaining variety of dot-lead charge transition. The floating-gate-induced quantum dot in the left SiNW FL1d (green) is more strongly coupled to the sensor gate L1 due to its proximity, while in the SiNW on the right, the other floating-gate-induced quantum dot FR1d (red) and gate-induced quantum dot R1d (yellow) are more

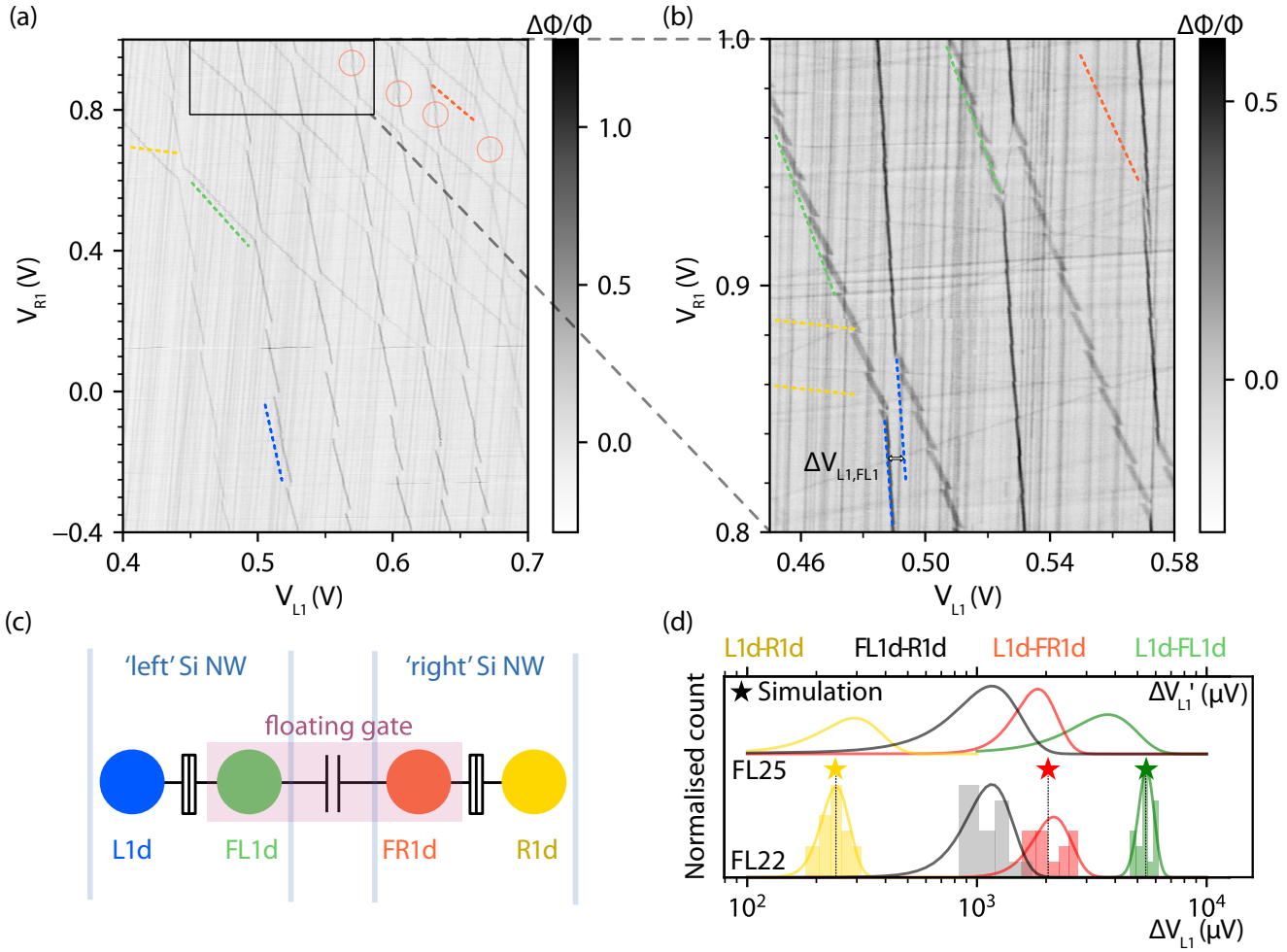

Figure 2: Remote sensing of quantum dot charge transitions in different silicon nanowires using the floating gate. (a) Charge stability map in the L1 and L2 gate-space (top gate T potential $V_{\mathrm{T}} = 4\mathrm{V}$; V_{L2} and $V_{\mathrm{R2}} = -1\mathrm{V}$). (b) Zoom-in of (a) illustrating the different capacitive shifts of the sensor dot-lead transition due to loading electrons into different quantum dots along the floating gate direction. (c) Schematic of the remote sensing showing quantum dots as a network of charge nodes and capacitors. Dot-lead transition in stability diagram are indicated by dashed line with corresponding quantum dot color. (d) Histogram of capacitive shifts induced on the sensor dot by a charge transition in another quantum dot measured at various anticrossings, following the colour-coding in (c), normalized as a dot L1 Coulomb peak shift ΔV. The coloured solid-line is the normalized fit to a Gaussian probability density function of histogram which attribute to the same quantum dot. (★) show calculated values from a COMSOL finite element simulation. Grey curves and histogram represent capacitive shifts from transitions in dot R1d measured using FL1d dot-lead transition. All data described above are from device 'FL22' — a normalized fit of the $\Delta V'$ histogram from a similar device 'FL25' is shown vertically offset above.

strongly coupled to gate R1. When quantum dot FL1d is sufficiently occupied, the increase in tunnel rates allows for FL1d dot-lead transitions to also be directly detected in the reflectometry phase shift signal. This signal allows us to trace back the number of electrons in sensor dot L1d (see Supplementary §I). This approach can be further quantified by comparing the cross-capacitance ratios $\alpha_{(i,j)}$ calculated as the degree to which gate L1 influences the other dot-lead transitions in voltage space. Assuming $\alpha_{(\mathrm{L1,L1})} = 1$, this method yields $\alpha_{(\mathrm{FL1,L1})} = 0.173$, $\alpha_{(\mathrm{FR1,L1})} = 0.124$, $\alpha_{(\mathrm{R1,L1})} = 0.005$. A significant drop in the cross-capacitance ratio is therefore apparent for groups of dots under spatially separated gates.

A second quantitative approach to distinguish the different quantum dots coupled to the sensor is to analyse the strength of the capacitive coupling between the sensor dot L1d and each of the remaining dots. In Fig. 2(d) we plot a histogram of the shifts $\Delta V_{(\mathrm{L1},i)}$, expressed in terms of the gate L1 voltage V_{L1}, arising from the capacitive shift in the sensor dot L1d due to the addition of an electron to some other dot i.[23] We use a peak-finding algorithm near a capacitive shift of interest in Fig. 2(b) and take the difference between the shifted dot-lead reflectometry peaks, extrapolated to the same value of V_{R1}. The capacitive shifts extracted in this way group naturally into three distinct sets, each corresponding to the transitions in another quantum dot indicated following the colour code in Fig. 2c). Being located in the same nanowire, FL1d (green) is the most strongly coupled to the sensor dot, while the other floating-gate-induced quantum dot FR1d (red), located in the remote nanowire, shows a slightly weaker coupling. The R1 gate-induced quantum dot R1d (yellow) in the remote nanowire shows the weakest coupling, but can still be detected. A normalized fit of the probability density function of each group provides the mean capacitive shift referenced against the sensor dot gate voltage: $\Delta\overline{V}_{(\mathrm{L1,FL1d})} = 5.47$ mV, $\Delta\overline{V}_{(\mathrm{L1,FR1d})} = 2.16$mV, $\Delta\overline{V}_{(\mathrm{L1,R1d})} = 0.243$ mV. These values show good agreement to simulations of the capacitance matrix for this device structure (see Supplementary §III).

As certain charge transitions FL1d are directly visible in the phase response, we can also extract a corresponding capacitive shift between dots FL1d and R1d, which is the symmetric analogue to the sensor dot coupling through the floating gate to FR2d. Data corresponding to such $\Delta V_{(\mathrm{L1d,FR1d})}$ shifts are shown in grey in Fig. 2d), and indeed fall within a similar range to $\Delta V_{(\mathrm{L1,FR1d})}$. This asymmetry is not captured in our simulations and is most likely due to finite lithographic misalignment between the patterns of the nanowire and the split between the gates. Based on automated overlay controls and tools specifications we estimate that the cuts, although centered on the nanowires by design, are probably shifted by 5-10nm on a typical device. In our case, this asymmetry translates into stronger lever-arm parameters for the dots defined along the right edges of the nanowires, and is systematically observed in other devices.[17,24] Finally, to show the consistency of these values across different devices of the fabricated on the same die, we performed the same set of measurements on a second device and plot the extracted Gaussian fits to $\Delta V_{(i,j)}$ for each pair of dots on the same axis in Fig. 2(d).

To demonstrate the enhancement of capacitive coupling arising from the floating gates, we compare results from floating gate devices with those from devices with similar dimensions containing only single, isolated silicon nanowires (see Supplementary §I). In order to facilitate the comparison of results from different devices, sensor dots and lever arms, we adopt a measure of the SEB sensitivity to the charge transitions in nearby quantum dots based on normalizing the voltage-referenced capacitive coupling by the addition voltage required to add an electron to the SEB: $\Delta q = \Delta V_{(\mathrm{L1},i)}/V_{\mathrm{C_{L1d}}}$, where $\Delta V_{(\mathrm{L1},i)}$ is the detected voltage shift in V_{L1} arising from coupling to dot i, $V_{\mathrm{C_{L1d}}}$ is the change in V_{L1} required to add an electron to the sensor dot L1d.

We first study the normalized SEB charge sensitivity within a 2×2 quantum dot array located in a single silicon nanowire. Here we can compare the capacitive coupling between dots formed on opposite edges of the nanowire,

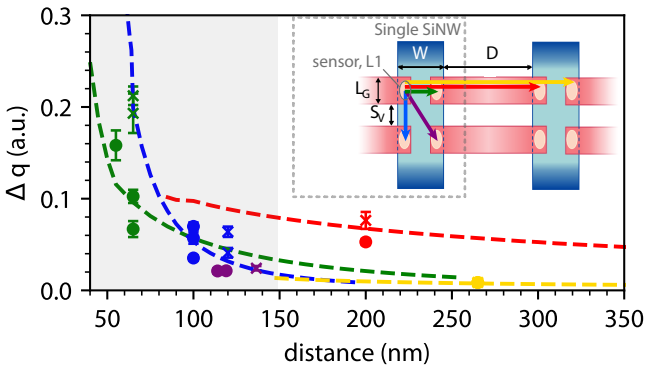

Figure 3: Normalized capacitive coupling as a function of distance. Voltage shifts in the sensor dot arising from capacitive coupling to other quantum dots are normalized against the addition voltage of the individual SEB to compare measurements from two floating gate devices and three single-nanowire devices (×, L_g = 60 nm; ●, L_g = 50 nm). Arrows in the inset illustrate the type of sensing: green, blue and purple data points relating to sensing within a single-nanowire and are obtained from both type of devices. Red and yellow data points required floating gate devices). COMSOL simulations are used to obtain parameter sweeps relating to each class of dot being sensed, following the colouring in the inset — a single normalisation is applied to all simulated curves. Error bars in the data include the uncertainties in both the capacitive voltage shifts and addition voltages.

between adjacent dots formed along a common SiNW edge, and also between diagonally coupled, next-nearest neighbour quantum dots. These configurations are shown in the inset of Fig. 3, which also illustrates configurations for sensing dots in a neighbouring SiNW, with coupling facilitated through the floating gate. The data in Fig. 3 compare three single-nanowire devices, each consisting a 2×2 quantum dot array, as well as the corresponding single-nanowire arrays within two floating-gate devices. The *intra-wire* normalised sensitivities Δq fall off quickly with increasing separation between the quantum dots, though a single power law cannot be used to describe the overall trend with distance for all couplings, due to the difference in mutual capacitance for dots located on the same or opposite edges of the nanowire.

Modelling the quantum dot as conducting ellipsoids we calculate the Maxwell capacitance matrix for varying center-to-center dot separation d, along with other nanowire design parameters (full details of the simulation method and relation to device dimensions are given in Supplementary §I–V). Each of the parametric sweeps from the simulations (dashed lines in Fig. 3) settles to a power law attributed to each sensor-dot configuration: nearest-neighbour couplings along the edge of the nanowire (L1d-L2d) or across the nanowire (L1d-FL1d) have couplings which decay approximately as $\Delta q \propto d^{-2.8}$ or $d^{-2.5}$ respectively, over the range of distances studied here. Data for a next-nearest neighbour configuration L1d-FL2d, where the dots are positioned diagonally across the wire, is shown for completeness but is not modelled. For the 'remote sensing' configuration where charge transitions are detected through the floating gate, the normalized capacitive coupling is sustained over a much greater distance, as reflected in the experimental data and simulations. By sweeping the floating gate length (approximated to be the SiNW separation, D) simulations show that the two dots under each corner of the floating gate have a coupling which is dominated by the second-order capacitive coupling via the floating gate at these distances, and decays only as $\propto D^{-0.4}$ (see Supplementary §VI). Combined with the

additional spacing of the nanowire width local to the SEB, this results in an coupling decay for the dot L1d-FR1d configuration which can be approximated as $\Delta q \propto d^{-0.6}$ in the range studied here. As a result, the mutual capacitive shift for dot L1d-FR1d remains relatively high, even at distances exceeding 300 nm, as shown in Fig. 3.

Coupling the sensor to dot R1d now involves three degrees of separation from the sensor, with a corresponding drop in sensitivity for short separations. However, the action of the floating gate leads to a much more gradual decay in sensitivity with distance that goes as $\Delta q \propto d^{-0.7}$ in our simulations. As a result, for distances above $d \approx 220$ nm, the floating gate mediated coupling between dots arranged on opposite edges of *different* nanowires exceeds that from two dots on opposite edges of the same silicon nanowire (see Supplementary §VI). Furthermore, the charge distribution due to floating gate geometry could be optimised to yield a stronger absolute coupling, while maintaining the much more gradual decay with distance .[25]

Our experimental measurements and simulations indicate decays in capacitive coupling strength which fall off more slowly than $\propto d^{-3}$, as previously observed within arrays of Si/SiGe planar quantum dots.[26,27] However, such measurements were made within planar quantum dot devices with a high density of metallic gate electrodes, expected to screen mutual capacitive coupling. Indeed, considering only the first-order approximations to capacitive couplings, our simulations also show decays that approach d^{-3} (see Supplementary §VI). In contrast, the devices studied here contained a relatively low density of metallic gate electrodes, and the fabrication of the split-gates involved etching of metal that was replaced by SiN. The result is a reduced decay rate in sensitivity as a function of dot-dot separation — most strikingly when facilitated by the capacitively coupled floating gate. Instead of screening charge movement, the floating gate propagates the effect of charge movement over a distance to be chosen as a design parameter, coupling charge between two otherwise separate silicon structures. While the simulations are able to capture well the trends in the different classes of coupling, the residual spread in experimental values across the measurements may be due to the asymmetry in realistic devices, not captured by the simulations, which can influence not only the dot to dot geometrical distance but also the device lever arms.

The capacitive shifts we measured between QDs, both locally and on distinct nanowires, are well above the full-width at half-maximum (FWHM) of the SEB dot-lead charge transition (see Supplementary §II). Assuming a Lorentzian lineshape for the measured SEB charge transition, any capacitive shift greater than twice the FWHM gives at least 94% of the maximum sensor contrast (e.g. for spin-dependent tunneling readout). Based on our simulations and the intrinsic FWHM of the sensor transition of 0.24 mV, dot L1d-FR1d type couplings mediated by the floating gate could be used to achieve spin readout for distances up to 500 nm without a reduction in readout contrast.

In addition to applications for sensing, capacitive coupling has been used to realise local multi-qubit interactions in a variety of systems, including singlet-triplet qubits[28] and charge qubits.[29,30] Meanwhile, several approaches to scaling quantum dot arrays pursue long-range coupling between qubits to facilitate the integration and fan-out of control electronics and suppress charge leakage[6,11]— solutions to realising such two-qubit gates include exploiting a RKKY mediating exchange interaction[11,31] or coupling via a superconducting resonator.[32] Multi-qubit operations utilising capacitive coupling via floating gates, coupling two singly-occupied planar dot structures, have been proposed to produce a spin-spin coupling Hamiltonian $H_{\mathrm{S-S}} \simeq J_{12}(\sigma_x^1\sigma_x^2 + \sigma_y^1\sigma_y^2)$ when the Zeeman energy $E_{\mathrm{Z}} \gg J_{12}$ and where $\sigma_{x,y,z}$ are the Pauli matrices in the relevant qubit basis,[25] which can be used to implement the iSWAP operation.[33] Combining the assumptions within Ref [25] with the parameters of the devices studied here and spin-orbit coupling strength for silicon,[34] we estimate a coupling of $H_{\mathrm{S-S}} \simeq 10^3$ Hz under realistic device operating condi-

tions between FL1d and FR1d with nanowire separation $\sim$ 200nm, which is too weak for practical applications. However, utilising the floating gate to couple two singlet-triplet qubits via $H_{\mathrm{ST-ST}} \simeq J_{12}/2((\sigma_z - I) \otimes (\sigma_z - I))$,[28] where I is the identity matrix, exploits the much stronger electric-dipole coupling to achieve the CZ operation. For the nanowire geometry presented here (i.e. with singlet-triplet qubits arranged on each nanowire and the nearest dots of each pair separated by $\sim$ 200nm) we estimate $H_{\mathrm{ST-ST}} \simeq 10^{12}$ Hz via the model in Ref. [25], made more favourable in this geometry due to reduced oxide thickness. In SiGe devices, coupling between charge qubits $H_{\mathrm{C-C}} \simeq g/4((I - \sigma_z) \otimes (I - \sigma_z))$ mediated by the mutual capacitance term[29,30] has been demonstrated with a strength of $\approx$15 GHz over dot separations of 130 nm,[30] while for the device geometry studied here our results predict $H_{\mathrm{C-C}} \simeq 10^{11}$ Hz for dots separated by 200 nm on different nanowires.

We have demonstrated through experiments and simulation the effect of integrating floating gate electrodes to extend the sensitivity range of a single capacitive sensor, highlighting in particular the potential to couple quantum dots located on distinct silicon nanowires. Our measurements made the use of a single electron box charge sensor, while we note that a parallel study on similar devices illustrates an alternative mode for charge detection in such structures, with one nanowire acting as a single electron transistor that remotely senses the charge occupancy of dots on the other nanowire.[35] In future devices with overlapping gate architecture,[3] a second layer of gate electrodes could be used independently tune the quantum dots confined under the floating gates and achieve remote interactions. Given the substantial promise of spin qubits formed along quasi-1D arrays, along the edges of silicon nanowires,[17] the enhanced capacitive couplings we measure using floating gates provide a potential route to couple qubits distributed across separate nanowires and thus for scaling in a second dimension.

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Supporting Information Available

Further information on the device, charge stability diagram of SiNW dot arrays; details of simulation and extraction of capacitance matrix

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