Implantable Analogue Circuits for Improved Methods of Nerve Signal Recording

By

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“All things must have a usefulness; that is certain. Since electricity must have a usefulness, and we have seen that it cannot be looked for either in theology or in jurisprudence, there is obviously nothing left but medicine.”

J. G. Krüger, Halle, 1743

Application of medical electricity.

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I am grateful that Mr. Iasonas Triantis took on the task of further developing the EMG cancellation system, allowing me to focus on the other aspects of ENG recording described in this thesis.

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TO JO
Abstract

Every year thousands of persons suffer injuries to the central nervous system with the permanent loss of sensation and voluntary motor functions. Functional electrical stimulation is a useful technique to restore some of these motor functions. However, the challenge remains to improve control of the stimulated muscle through provision of a feedback path. Biopotentials recorded from nerves (Electroneurogram, ENG) by means of cuff electrodes can provide the required feedback in a fully implantable system. The information and signal-to-noise ratio (SNR) obtainable from ENG recording can be increased by the use of multi-electrode cuffs (MECs). A MEC contains several electrode pairs embedded in the inside wall. The signal and noise performance of the MEC are discussed in this thesis. Typical signals recorded with this method are extremely small, on the order of 1μV and require amplification by a very low-noise, high-gain system providing multiple recording channels at very low power consumption.

This thesis is concerned with the design of a fully integrated analogue multi-channel ENG recording system, which due to its small size can be combined with the recording cuff to form a ‘smart electrode’, i.e. an electrode joined with active circuitry to provide additional functionality and higher signal quality. The specification of the system improves on previously reported designs for single tripole recordings making it suitable for MEC applications. Special attention is given to low-noise optimisation. The relevant noise equations are derived in this thesis, which leads to an optimum design strategy for very low-noise amplifiers. Due to the high gain of the system, AC-coupling of the gain stages is essential to preserve the available dynamic range. A suitable passive high-pass filter is
discussed, which removes DC offsets without degrading the noise performance. Furthermore, a micropower, continuous-time integrator with a very large time-constant is proposed. Such an integrator is a main building block in an ENG adaptive amplifier, which was proposed to reduce the effect of residual muscle signal interference on the recorded ENG. A recording system incorporating this integrator has the potential to further improve recording quality in a future design.

Measured results for all the proposed circuit blocks are presented as well as results for an 11-electrode ASIC combining the proposed circuits. Furthermore, in vitro tests with frog nerve show the feasibility of extracting parameters such as compound action potential propagation velocity and direction from the recorded multi-channel ENG.
# TABLE OF CONTENTS

## CHAPTER 1 – INTRODUCTION

1.1 Motivation for this Thesis ........................................ 18  
1.2 Thesis Contributions .............................................. 22  

## CHAPTER 2 – ENG RECORDING METHODS

2.1 ENG Properties ...................................................... 25  
2.2 ENG Recording Techniques ....................................... 27  
2.2.1 Monopole ......................................................... 30  
2.2.2 Bipole .......................................................... 30  
2.2.3 Quasi-Tripole ...................................................... 30  
2.2.4 True-Tripole ....................................................... 31  
2.2.5 Screened True-Tripole .......................................... 35  
2.2.6 MEC Overlapping True-Tripole ............................... 35  
2.3 Properties of the Multi-electrode Nerve Cuff .................... 36  
2.3.1 Principle of Velocity Selectivity ............................... 36  
2.3.2 MEC Signal Amplitude .......................................... 39  
2.3.3 MEC Noise and SNR .............................................. 43  
2.4 Noise Matching ..................................................... 50  
2.4.1 Noise-Matching to a Single Dipole ............................ 52  
2.4.2 Noise-Matching to an Array of Dipoles ....................... 52  
2.4.3 Noise-Matching to a Tripole and MEC ....................... 54  
2.5 MEC SNR Improvement Including Amplifier Noise ............ 57  
2.6 General System Specifications .................................... 58  
2.7 Conclusions ......................................................... 63
CHAPTER 3 – ELECTRONIC NOISE

3.1 Noise Mechanisms 65
   3.1.1 Thermal Noise 65
   3.1.2 Shot Noise 66
   3.1.3 Flicker Noise 68
3.2 Noise Models 69
   3.2.1 Noise in Resistors 70
   3.2.2 Noise in Vertical Bipolar Transistors 71
   3.2.3 Noise in Lateral Bipolar Transistors 73
   3.2.4 Noise in MOS Transistors 75
3.3 Conclusions 78

CHAPTER 4 – PREAMPLIFIERS

4.1 Design of a Low-Noise Preamplifier 79
   4.1.1 Noise Reduction Techniques 79
      4.1.1.1 Bias Switching 80
      4.1.1.2 Chopper Technique 81
      4.1.1.3 Autozeroing 82
   4.1.2 Preamplifier Specification 83
   4.1.3 Design Considerations 84
      4.1.3.1 Basis of Comparison 86
      4.1.3.2 Input-Refere ed Voltage Noise 87
   4.1.4 Simulated Results 91
   4.1.5 Measured Results 92
   4.1.6 Practical Considerations on Lateral BJT 95
   4.1.7 Lateral Preamplifier Design 99
   4.1.8 High-Pass Filter 99
   4.1.9 Simulated Results 101
   4.1.10 Measured Results 102
   4.1.11 Conclusions 103
CHAPTER 5- IMPROVED RECORDING METHODS

5.1 Experimental Determination of Compound A-P Direction and Propagation Velocity From Multi-Electrode Nerve Cuffs 106
   5.1.1 Introduction 106
   5.1.2 Experiment and Results 106
   5.1.3 Discussion and Conclusion 110
5.2 Measurement of MEC Noise 111
   5.2.1 Experiment 111
   5.2.2 Measured Results 113
   5.2.3 Discussion and Conclusions 113
5.3 Adaptive EMG Cancellation 116
   5.3.1 Introduction 116
   5.3.2 Very Large Time-Constant Low-Power CMOS Integrator 118
   5.3.3 Tuning a Very Large Time Constant 119
   5.3.4 Approaches for Realizing Large $C/G_m$ Ratios 121
   5.3.5 Circuit Description 124
   5.3.6 Measured Results 128
   5.3.7 Conclusion 131
5.4 Acquisition System - Measured Results 133

CHAPTER 6- CONCLUSIONS AND FUTURE DIRECTIONS

6.1 Conclusions 138
   6.1.1 MEC Signal and Noise 138
   6.1.2 Low-Noise Array of Amplifiers 139
   6.1.3 Adaptive EMG Cancellation 140
6.2 Future Directions 140

References 141
LIST OF TABLES

Table 1.1: Performance comparison between recording systems. 21
Table 2.1: Typical values of specific conductivity for various biological fluids. 33
Table 2.2: Matched noise resistance for various amplifier configurations. 57
Table 2.3: Areas sought to improve compared to other designs. 59
Table 2.4: Core system specification. 62
Table 3.1: Corner values for factor $\varepsilon$. 76
Table 3.2: Typical core parameters for noise modelling. 77
Table 4.1: Preamplifier Specification. 84
Table 4.2: Procedure for voltage noise reduction (constant $g_m$). 90
Table 4.3: Main parameters of the candidate OTAs. 91
Table 4.4: Measured Results. 95
Table 4.5: Amplifier specifications and measured results. 105
Table 5.1: Comparison of transconductance reduction approaches for realizing high $C/G_m$ ratios. 124
Table 5.2: Summary of performance. 130
Table 5.3: Comparison with other integrator designs. 131
Table 5.4: ASIC measured results. 136
LIST OF FIGURES

Fig. 1.1: Cross section of the spinal cord showing afferent and efferent nerves and their bundling. 19

Fig. 2.1: Local currents and membrane polarity during AP propagation. 25
Fig. 2.2: The components of a myelinated nerve fibre. 26
Fig. 2.3: Historical nerve cuff designs 28
Fig. 2.4: Impedance model of the cuff and idealized ENG and EMG potentials inside the cuff. 29
Fig. 2.5: Cuff Electrode Configurations. 30
Fig. 2.6: Monopolar recording of a potential difference between \( V_m \) and \( V_L \). 33
Fig. 2.7: Contribution of thermal noise sources to the true-tripole output noise. 35
Fig. 2.8: Histogram of fibre diameters in a human sural nerve. 36
Fig. 2.9: Cuff with overlapping true-tripole configuration (MEC). 37
Fig. 2.10: MEC arrangement for velocity selective recording. 38
Fig. 2.11: Frequencies of maximum signal amplitude vs. velocity. 42
Fig. 2.12: Gain in MEC signal amplitude compared to a single tripole. 43
Fig. 2.13.a: Noise contribution of the axonal resistance to amplifiers in the array.
   b: Noise sources associated with \( R_i \). 44
Fig. 2.14: Examples of spot noise density vs. artificial delay \( \tau \). 47
Fig. 2.15: Change in MEC noise with \( n \) (relative to a single tripole). 48
Fig. 2.16: SNR of the MEC relative to the SNR of a single tripole. 49
Fig. 2.17: Equivalent circuit for noise matching cuff and amplifier.

Fig. 2.18: Voltage noise sources in an overlapping array of dipoles.

Fig. 2.19: Amplifier current noise and resulting noise currents in the cuff.

Fig. 2.20: MEC noise due to amplifier noise sources – variation with $\tau$.

Fig. 2.21: SNR of the MEC compared to a single tripole considering both, thermal and amplifier noise.

Fig. 3.1: Thermal noise power spectrum.

Fig. 3.2: Shot-noise power spectrum.

Fig. 3.3: Flicker-noise power spectrum on a log-log scale.

Fig. 3.4: Flicker-noise voltage spectrum for 80k$\Omega$ POLY1 resistor.

Fig. 3.5: Wafer cross section through the npn-BJT with equivalent base spreading resistance.

Fig. 3.6: Schematic cross section through a reverse-biased n-well MOS with the schematic symbol to illustrate the location of the lateral BJT.

Fig. 3.7: Geometry of a lateral pnp-transistor.

Fig. 3.8: Simplified input-referred low-frequency noise models.

Fig. 4.1: Cycling of MOS gate bias (left) and application to an OTA.

Fig. 4.2: Block diagram of a chopper amplifier.

Fig. 4.3: Block diagram of autozero amplifier.

Fig. 4.4: Basic preamplifier architecture.

Fig. 4.5: Candidate OTA circuits.

Fig. 4.6: MOS and Bipolar OTA with noise sources.

Fig. 4.7: Simulated input-referred voltage noise densities of candidate OTAs.
Fig. 4.8: Final preamplifier schematic. 94
Fig. 4.9: Chip microphotograph. 94
Fig. 4.10: Comparison between simulated and measured voltage noise performance. 94
Fig. 4.11: Preamplifier schematic with lateral pnp-transistors. 97
Fig. 4.12: Comparison of amplifier noise performance using different manufacturing processes. 98
Fig. 4.13: Comparison of lateral amplifier gain in CMOS and BiCMOS process. 98
Fig. 4.14: Preamplifier architecture. 99
Fig. 4.15: High-pass RC-filter connected to preamplifier output. 100
Fig 4.16. Active 8.2MΩ resistor with improved linearity. 101
Fig. 4.16 Output noise PSD before and after RC-filter. The total noise remains the same. 104
Fig. 4.17: Percentage variation of resistance from nominal value with applied voltage. 104
Fig. 4.18: Measured output noise PSD before and after RC-filter. 105

Fig. 5.1: Cuff electrode before curling. 108
Fig. 5.2: Experiment setup. 109
Fig. 5.3: Action potential delayed by a constant time $T=50\mu$s between the traces ($d=1.8\text{mm}$). 109
Fig. 5.4.left: Signals produced after summation of the five tripole amplifier outputs with time delays. 110
right: The tuning curve, showing a peak at $r=52\mu$s. 112
Fig. 5.5: Cuff in saline.  
Fig. 5.6: Bench setup with amplifier ASIC.  
Fig. 5.7: Recording setup and likely entry points of interference.  
Fig. 5.8: Measured noise compared with expected results.  
Fig. 5.9: Simulation including interfering noise and noise equation.  
Fig. 5.10: Block diagram of the control system.  
Fig. 5.11: Adaptive system applied to a MEC.  
Fig. 5.12: $G_m C$ integrator with finite output impedance $R_o$.  
Fig. 5.13: Capacitance scaling. Simplified schematic and small-signal equivalent circuit.  
Fig. 5.14: Transconductance reduction by current division.  
Fig. 5.15: Current cancellation technique.  
Fig. 5.16: First four stages of the gm-1/gm chain.  
Fig. 5.17: Last stage of the $g_m^{-1}/g_m$ chain.  
Fig. 5.18: Chip microphotograph (core).  
Fig. 5.19: Transfer characteristics of the first $g_m/g_m^{-1}$ stage.  
Fig. 5.20: Integration of small sine waveform input.  
Fig. 5.21: Integration of small square waveform input.  
Fig. 5.22: Variation of the time-constant with external current source $I_{bias}$.  
Fig. 5.23: Transfer characteristics; open-loop and unity gain closed-loop.  
Fig. 5.24: Integration of a large square waveform.  
Fig. 5.25: Schematic of a possible implementation of the second-rank amplifier.
Fig. 5.26: Schematic of a possible implementation of the tripole amplifier. 135

Fig. 5.27: Measured voltage gain of a typical dipole channel and simulation result. 136

Fig. 5.28: Top: ASIC layout. 137

Bottom: Die mounted in PGA package for testing.
GLOSSARY OF TERMS

AP – ACTION POTENTIAL
ASIC – APPLICATION SPECIFIC INTEGRATED CIRCUIT
CAD – COMPUTER AIDED DESIGN
CAP – COMPOUND ACTION POTENTIAL
CNS – CENTRAL NERVOUS SYSTEM
ENG – ELECTRONEUROGRAM
EMG – ELECTROMYOGRAM
FES – FUNCTIONAL ELECTRICAL STIMULATION
MEC – MULTI ELECTRODE CUFF
MUX – MULTIPLEXER
OTA – OPERATIONAL TRANSCONDUCTANCE AMPLIFIER
SFAP – SINGLE FIBRE ACTION POTENTIAL
SNR – SIGNAL-TO-NOISE RATIO

FREQUENTLY USED CONSTANTS

$q$ – Electron charge $1.6 \times 10^{-19}$C
$k$ – Boltzmann constant $1.387 \times 10^{-23}$ VC/K
$U_{th}$ – Thermal Voltage at room temperature $=26$mV
SYMBOLS WITH ALTERNATIVE MEANINGS

$n$ – weak inversion slope factor (usually around unity).

$\text{number of dipoles in an MEC} = \text{number of electrodes minus 1.}$

$T$ - Temperature in °K.

$\tau$ - Artificial time delay of a MEC.

$\beta$ - Current gain of a bipolar transistor.

Feedback loop gain.
CHAPTER 1
INTRODUCTION

1.1 MOTIVATION FOR THIS THESIS

Injuries to the spine involving the central nervous system (CNS, nervous system comprising the brain and the spinal cord) are among the most devastating of all neurological disorders resulting in the permanent loss of sensation and voluntary motor functions. In most countries paralysis due to spinal cord injury occurs at an annual rate of 40 persons per million, which translates into many thousand cases per year in the European Union alone, predominantly among younger individuals. The cost of care approximates to about £1 million per individual in medical care and loss of earnings. In addition, permanent paralysis is accompanied by a drastic change in the individual’s life style and independence [1]. Especially focal spinal cord injuries lead to dramatic lower leg and bowel paralysis, whilst the peripheral nervous system behind the place of injury and the CNS before the injury are often still intact. In the absence of spinal cord regeneration, functional electrical stimulation (FES) aims at the full or partial restoration of lost function by stimulation of the intact nerves below the lesion with electrical impulses. As direct access to the spinal cord is associated with high risks of infection and traumatic surgical procedures, recent research focuses on the stimulation of and recording from peripheral nerves. Fig. 1.1 shows a cross section through the spinal cord with dorsal and ventral nerve bundles branching off the stem. Information is carried from receptors in the body via the dorsal root to the spine and information travels in the opposite direction to receptors in the
body via the ventral root. These two branches unite some distance away from the spine to form a peripheral nerve bundle, which carries information in both directions.

Devices for correcting drop-foot were the first and are still the most commonly used type of motor neuroprosthesis [2-4]. Other applications that have been investigated include the restoration of hand grasp in tetraplegic patients, and thumb force control [5-7].

![Cross section of the spinal cord showing afferent and efferent nerves and their bundling (modified from [2])]({})

However, the effectiveness of present FES prostheses remains unsatisfactory. One important reason for this is that most are pure feed forward systems, relying on an external feedback path, e.g. by voluntary operation of a control box by the patient. If feedback is available it is often insufficient, as the information obtainable with external sensors is not very detailed. This results in stimulation with little graduation, depending on visual feedback and experience [6]. Stimulation implants could be vastly improved if the loop is closed internally, reducing or even removing the need for external control. One promising approach is to make use of afferent nerve signals to provide feedback [8-10], which eliminates artificial sensors altogether. Recently Hansen et al. [11] showed that
the naturally-occurring neural signal (ENG) in a sensory nerve from the foot (sural nerve) could be used as the input source to a system that activates the tibialis anterior muscle via the peroneal nerve. Avoiding additional sensors is beneficial, because reduced wiring to external components increases the reliability of the system as well as patient's acceptance due to better cosmetic appearance and easier care.

Several recording techniques to obtain ENG have been introduced in the past and these are briefly discussed in Chapter 2. The challenge in recording useful signals with any practicable technique lies in the miniscule amplitude of the ENG, which is typically in the order of only a few microvolts, embedded in noise and interference in the millivolt range. Therefore, high quality amplification and signal conditioning must take place as close to the recording site as possible. Ideally, this functionality is placed immediately onto the recording nerve cuff, combining cuff and signal processing unit into one active, i.e. 'smart electrode'. The smart electrode also contains circuitry to add further functionality, such as a choice of recording methods, velocity selective recording, channel multiplexing etc., as discussed in the following chapters. This approach reduces the need for wiring and thereby keeps mechanical stress on the components to a minimum, limits interference pick-up and makes implantation easier and less invasive. The concept of a smart electrode places high demands on the active electronic circuitry, which has to be small enough to be mounted on the nerve cuff. Furthermore, the circuitry must consume little power, provide very low-noise operation, be fully integratable without external components and be cost-efficient. Key data of previously proposed recording arrangements are compared in Table 1.1 together with the performance of the system described in this thesis. The other
designs are intended for different applications and fall short of the requirements of the smart electrode, as indicated by the shaded areas. The system described in the following chapters improves on all the relevant measures to advance the state of the art in neuroprosthetic.

Power to the electrode is most conveniently supplied externally, e.g. by means of inductive coupling through the skin. Arrangements to facilitate power supply and signal transfer out of the body exist [12], allowing this thesis to focus on the cuff and associated electronics itself.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
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<tbody>
<tr>
<td>Target application</td>
<td>Recording from neurons</td>
<td>EEG recording</td>
<td>ENG experimentation</td>
<td>MEC ENG recording</td>
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<td>Number of channels</td>
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<td>16</td>
<td>16 Dipoles</td>
<td>10 Dipoles 9 Tripoles</td>
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<tr>
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<td>4.5mW</td>
<td>not stated</td>
<td>20mW</td>
</tr>
<tr>
<td>Gain</td>
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<td>500-5,000</td>
<td>65,000 – 200,000</td>
<td>10,000 Dipole 100,000 Tripole</td>
</tr>
<tr>
<td>Passband</td>
<td>15Hz-7kHz</td>
<td>0.3Hz-150Hz</td>
<td>20Hz-10kHz</td>
<td>300Hz – 10kHz</td>
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<tr>
<td>Input referred noise in passband</td>
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<td>1.4μVrms</td>
<td>7.4μVrms</td>
<td>0.3μVrms</td>
</tr>
<tr>
<td>Active Area</td>
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<td>24mm²</td>
<td>6.1mm²</td>
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<tr>
<td>CMOS Technology</td>
<td>3μm</td>
<td>2.4μm</td>
<td>0.7μm</td>
<td>0.8μm</td>
</tr>
</tbody>
</table>

Table 1.1: Performance comparison between recording systems.
Shaded fields identify shortcomings of existing designs.
1.2 Thesis Contributions
The following can be identified as major contributions of this thesis to the advance of nerve signal recording:

- The theory for velocity selective recording using a MEC is developed and its SNR characteristics in comparison to a conventional tripole are studied. The method allows to distinguish between signals from specific nerve fibre populations and to record from these selectively. Furthermore, the direction of AP propagation can be determined, so that signals from afferent and efferent fibres can be distinguished. It is shown that the SNR at low velocities, which yield a low SNR in the conventional tripole, is improved by using a MEC.

- A very low-noise, low-power amplifier interface suitable for use with the MEC is developed. The ideal amplifier for this purpose employs bipolar transistors as input devices. Two realizations are presented, one in a BiCMOS process and one in a CMOS process using lateral bipolar transistors.

- An acquisition system with a suitable high gain of around 10,000 is described and measured results are presented. Due to the high gain, AC-coupling between preamplifier and gain-amplifier is essential. The design of a low-power coupling stage is reported which does not degrade the noise performance of the system.

- The related topic of low-power, long time-constant integrators is examined and an integrator with a tunable time-constant of around 5s is proposed. The integrator is a key building block in an adaptive nerve signal amplifier being currently developed (not discussed in this thesis).
Measured results obtained from in-vivo experiments and fabricated test chips are presented for all the topics. A list of publications inspired by the work in this thesis is given below.


2.1 ENG PROPERTIES

The ENG recorded from a nerve bundle is a superposition of thousands of single fibre action potentials (AP) within the bundle [16]. An AP is initiated by depolarisation of the membrane above the activation threshold. The depolarisation is then passed on along the axon, giving rise to the flow of small local currents. Fig. 2.1.a illustrates the concept using a nerve model which treats the axon as if it were divided into separate cells. Each activated cell regenerates the depolarisation pulse to its full strength by triggering further current flow across the cell membrane, resulting in un-attenuated propagation. If the nerve is stimulated artificially, all APs are triggered by the same stimulus and start propagating at approximately the same time. The resulting multitude of APs is called the compound action potential (CAP).

Fig. 2.1: Local currents and membrane polarity during AP propagation.
The activation potential is built up by charging the capacitance associated with the cell membrane. As a result, large capacitance means slower conduction velocity. Therefore, a sheath of insulating myelin is wrapped around the fibres of fast mammalian nerves as shown in Fig. 2.2, which lowers its capacitance. The sheath is broken only at the *Nodes of Ranvier* and the flow of local currents across the *internode* passively conducts the AP (Fig. 2.1.b). This mode of conduction in myelinated fibres is called *saltatory conduction*, as the AP appears to jump from node to node. The propagation velocity is determined by a combination of the time delay introduced by active cell depolarisation (about 0.1ms at each node [17]) and the passive spread governed by basic cable equations (i.e. conduction along a lossy distributed conductor). For a detailed analysis of AP propagation see [18]. It has been shown that the propagation velocity in myelinated fibres scales approximately linear with the fibre diameter [19]. Propagation velocities in mammalian nerves span a wide range between around 5m/s and over 100m/s due to the large variation in fibre diameters. The frequency spectrum of ENG recorded by a tripolar cuff electrode as described in the following section typically shows a
peak at around 2kHz, with most power concentrated between 300Hz and 5kHz [20]. The amplitude is in the order of a few microvolts embedded in noise and interference, originating mainly from muscle activity near the electrode site (EMG) and thermal noise from the electrode-to-tissue interface. The EMG exhibits amplitudes in the millivolt range and is significantly larger than the ENG. The EMG spectrum shows a peak near 200Hz and contains most power below 1kHz.

2.2 ENG RECORDING TECHNIQUES

Over recent years many ENG recording techniques have been developed. The two most common techniques are intrafascicular electrodes and cuff electrodes. Intrafascicular electrodes are usually shaped either as needle or wedge and implanted to penetrate the nervous tissue itself, allowing for recordings at various depths within the tissue. Although this type of electrode produces a large ENG output, the likelihood of tissue damage during insertion of the electrode and its subsequent movement is high, which is the main reason why intrafascicular electrodes can only be implanted for limited periods.

Cuff electrodes are electrodes which are fitted around a nerve fascicle or a sub-set of nerves and do not penetrate the nerve itself. Contemporary cuff electrodes are 1-2 cm long with a maximum diameter of a few millimetres. A popular electrode shape is the spiral geometry, as its flexibility allows adaptation to changing tissue dimensions, e.g. occurring as a result of post-implantational swelling, whilst fitting snugly around the nerve with minimal compression. Other electrode geometries have been used for nerve stimulation in the past, some of which are shown in Fig. 2.3 (from [21, 22]). Safe implantation of nerve cuffs for
as long as 15 years has been reported [23], showing the suitability of cuff electrodes for chronic use.

As discussed in Section 2.1, APs propagate through the flow of small currents across the cell membranes into the extrafascicular medium. Inside a nerve cuff the fluid is confined to a limited space with a small cross-sectional area. Thus, a relatively high impedance is established around the bundle, ensuring that the local currents give rise to measurable potential differences between the electrodes. As the fluid outside the cuff provides a low-impedance connection between the ends of the cuff, potential differences such as EMG across the cuff are kept small. Furthermore, the potential gradient caused by such interference is nearly constant within the cuff due to its insulating property [24]. This linearisation effect is important in tripole recording as it helps to cancel EMG artefacts, as discussed below. The resulting potential distribution caused by

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Fig. 2.3: Historical nerve cuff designs.
external signals (EMG) and signals originating within the cuff (ENG) are shown diagrammatically in Fig. 2.4. While the EMG gradient is constant along the cuff, the ENG potential is largest at its point of origin within the cuff. Also shown are the nerve and cuff impedances lumped into equivalent devices [25, 26]. In this model, $Z_{a1}$ and $Z_{a2}$ (typically around 1kΩ) represent the axonal impedances inside the cuff, $Z_0$ (typically below 100Ω) is the tissue impedance outside the cuff, $Z_{11}$, $Z_{12}$ and $Z_{13}$ (a few hundred Ohms) are the electrode–tissue contact impedances, $I_{EMG}$ is the interfering EMG current that flows in the cuff, and $I_{ENG1}$, $I_{ENG2}$ are the ENG local currents. Different arrangements of electrodes inside the cuff are shown in Fig. 2.5 and Fig. 2.9 and these are briefly discussed below.

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Fig 2.4: Impedance model of the cuff and idealized ENG and EMG potentials inside the cuff.
2.2.1 Monopole
This method used in early experiments employs a single electrode located centrally inside the cuff. A second remote electrode is placed at a distance as reference. This monopolar arrangement produces large signal amplitudes, but the interference rejection is poor.

2.2.2 Bipole
Differential-, or bipolar recording decreases the electrode sensitivity to external signals. In the bipolar configuration two electrodes are embedded in the cuff and the ENG recorded is the potential difference between these electrodes. The amplitude of the recording depends strongly on the electrode separation, i.e. the enclosed impedance and also on the length of the insulating cuff.

2.2.3 Quasi-Tripole
An arrangement termed quasi-tripolar arrangement removes the cuff length dependency so that the signal amplitude depends on electrode separation alone [27]. The ENG is recorded between two shorted outer electrodes and a centre
electrode halfway between the outer electrodes as the reference. This arrangement yields the practical advantage of interference cancellation: Ideally, the shorted end electrodes force the potential at the cuff ends to the same potential, also forcing the centre electrode to assume this potential. However, this explanation is incomplete. The main reason for the success of the quasi-tripole is based on the linear gradient of the EMG potential inside the cuff. With equally-spaced electrodes, the potential of the centre electrode lies between those of the end electrodes (Fig. 2.4) resulting in cancellation in the differential amplifier. However, total cancellation only occurs in a perfectly symmetrical cuff of infinite length [24, 28]. Although the effect of limited cuff length is small, cuff impedances $Z_a$ and therefore symmetry are subject to significant variation. Variations occur with time due to tissue re-growth inside the cuff after implantation, due to manufacturing tolerances or an inhomogeneous nerve. Assuming $Z_{11}=Z_{12}=Z_{13}=Z_f$ and unity amplifier gain, the residual EMG at the output is approximated by [29]:

$$V_{EMG} = I_{EMG} \frac{Z_a (Z_{a2} - Z_{a1})}{2Z_o + 2(Z_{a1} + Z_{a2}) + (Z_{a1} + Z_{a2})/Z_f}$$ (2.1)

Unfortunately, the only way to restore symmetry of the pseudo-tripole (i.e. making the nominator of (2.1) zero) is by rebalancing the cuff impedances, which is impractical especially after implantation.

2.2.4 True-Tripole

It is the true-tripolar arrangement which implements additional trimming capability. In this configuration three amplifiers are used. The two first-rank amplifiers record differentially between the outer electrodes and the centre electrode as the reference. A third amplifier sums the output signals of the first-rank amplifiers. In this system the gains of the first-rank amplifiers ($G_1$ and $G_2$)
can be adjusted independently, which allows trimming of the structure. Assuming unity gain for the summing amplifier, the residual EMG voltage appearing at the summing output is given by [29]:

\[ V_{EMG} = I_{EMG} \frac{Z_0}{Z_0 + Z_{a1} + Z_{a2}} \left( G_1 Z_{a1} - G_2 Z_{a2} \right) \]  

(2.2)

Adjusting the amplifier gains thus compensates for relative mismatches between \( Z_{a1} \) and \( Z_{a2} \). Also the magnitude of the ENG signal is twice as large as in the pseudo-tripole and the SNR has been shown to improve slightly compared to the quasi tripole [30]. The extra-cellular potential recorded by the tripole can be derived from the monopolar signal \( V_{mono} \) recorded by an electrode located at distance \( z \) from one end of the cuff with respect to a remote reference (Fig. 2.6), which can be expressed in its most general form by [31]:

\[ V_{mono}(z,t) = A [V_m(z,t) - V_L(L,t)] \]  

(2.3)

where \( V_m(z,t) \) is the membrane potential at position \( z \) at time \( t \) \( V_L \) is the reference at position \( L \) and \( A \) is a scaling factor determined by the ratio between extracellular impedance \( R_e \) and intracellular impedance \( R_a \) along the direction of the fibre, given by [31]:

\[ A = \frac{R_e}{R_e + R_a} = \frac{R_e}{R_a} = \frac{\delta_e d_a^2}{\delta_a d_e^2} \]  

(2.4)

where \( \delta \) is the specific conductivity and \( d \) the diameter of the axon and cuff respectively. Typical values of specific conductivity for various biological fluids are given in Table 2.1 from which \( \delta_a=100\mu \) and \( \delta_e=350\mu \).
Table 2.1: Typical values of specific conductivity for various biological fluids [32].

<table>
<thead>
<tr>
<th>Substance</th>
<th>Conductivity $\delta ,[1/(\Omega \cdot m)]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physiological Saline</td>
<td>1.75</td>
</tr>
<tr>
<td>Human Spinal Fluid</td>
<td>1.55</td>
</tr>
<tr>
<td>Human blood</td>
<td>0.61</td>
</tr>
<tr>
<td>Interstitium (approximation)</td>
<td>2.5-5.0</td>
</tr>
<tr>
<td>Crayfish axoplasm</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Since the nerve diameter is proportional to its conduction velocity [33], the velocity dependence of $A$ can explicitly be expressed as:

$$A = K \frac{v^2 \delta_a}{d_e^2 \delta_e}$$

(2.5)

where $v$ is the AP propagation velocity, and $K$ is a constant of around $1.792 \times 10^7 \, s^{-2}$.

Applying equation (2.3) to the tripolar configuration results in:

$$V_m(z_1,z_2,z_3,t) = A[V_m(z_1,t) - 2V_m(z_2,t) + V_m(z_3,t)]$$

(2.6)

Note that this expression is independent of $V_L$ so that the recorded signal does not change with the tripole position within the cuff, which is the basis for the multi-electrode cuff described later. The membrane potential is a function identical for all the electrodes, however delayed by a time $T$ as the result of the finite propagation velocity $v$ of the AP and electrode distance $d$, which yields:
\[ T = \frac{d}{v} \tag{2.5} \]

where \( d \) relates to the electrode pitch \( z_2-z_1 \) and \( z_3-z_2 \), assuming a symmetrical tripole. In the frequency domain (2.4) can be rewritten as:

\[ V_{trip} = A\left(V_m - 2V_m e^{-j\omega T} + V_m e^{-2j\omega T}\right) \tag{2.6} \]

The magnitude of the recorded signal results from (2.6) as:

\[ |V_{trip}| = 4A\sin^2 \frac{\omega T}{2} |V_m| \tag{2.7} \]

The dominant components of noise recorded by the tripole originate from the resistance of the electrode leads and tissue interface and the axonal resistance between adjacent electrodes. The associated noise sources can be represented as shown in Fig. 2.7, where \( V_I \) includes thermal noise from the leads and electrode-to-tissue resistance and \( V_a \) is the thermal noise from the axonal resistance between any two electrodes. The low-impedance connection \( Z_0 \) is modelled by a short-circuit across \( V_{a1} \) and \( V_{a2} \). This connection allows currents to flow, generated by noise sources \( V_{a1} \) and \( V_{a2} \), so that each noise source \( V_a \) contributes to each dipole noise voltage \( V_{d1} \) and \( V_{d2} \). As the amplifier input impedance is high (see Sections 2.3.3 and Chapter 4 for more details), sources \( V_I \) do not cause significant current flow and each contributes to only one mesh in the circuit. The tripole output noise results from summation of \( V_{d1} \) and \( V_{d2} \). Assuming unity amplifier gains the contributions due to \( V_{a1} \) and \( V_{a2} \) partially cancel and the tripole noise voltage is given by:

\[ V_{trip\_noise} = V_{a1} - V_{a2} + V_{i1} - 2V_{i2} + V_{i3} \tag{2.8} \]

All these noise sources are uncorrelated, so that the noise powers add algebraically. The output r.m.s. noise voltage is therefore given by:
\[ |V_{\text{trip\_noise}}| = \sqrt{2V_p^2 + 6V_i^2} \]  

\[ V_{\text{trip\_noise}} = \frac{V_{p1}}{2} - \frac{V_{p2}}{2} + V_{i1} - V_{i2} \]
\[ V_{\text{trip\_noise}} = \frac{V_{p1}}{2} - \frac{V_{p2}}{2} + V_{i2} - V_{i3} \]

**Fig. 2.7: Contribution of thermal noise sources to the true-tripole output noise.**

### 2.2.5 Screened True-Tripole

The screened true-tripole is an extension of the true-tripole with two or more additional end electrodes. Shorting the end-electrodes reduces the potential difference between the cuff-ends, thus, also reducing the field inside the cuff. The principle is the same as described for the shorted ends of the quasi-tripole, but the end electrodes can be optimised to give maximum field reduction. The effectiveness mainly depends on the area of the end electrodes and SNR improvements varying between 18% and 73% were found in studies using a rabbit model [34].

### 2.2.6 MEC overlapping True-tripole

The MEC consists of multiple tripoles arranged in an overlapping configuration. This structure makes use of the fact, that a true-tripole recording is independent of the tripole position within the cuff. All tripoles within the cuff have the same transfer function and record the same ENG with a small time delay. This property enables velocity-selective recording and improved SNR as described next.
2.3 PROPERTIES OF THE MULTI-ELECTRODE NERVE CUFF

A typical distribution of fibre diameters in the human sural nerve is shown in Fig. 2.8. There is an approximately proportional relation between fibre diameter and propagation velocity, with a conversion factor on the order of 5 m/s per \( \mu \text{m} \) [35]. Therefore a wide distribution of velocities is encountered even within a single nerve. If naturally-occurring nerve signals are to be used for the detection of signals that are not dominant in the nerve traffic, it will be vital to discriminate between traffic with different propagation velocities and directions.

\[ T = \frac{d}{v} \]

2.3.1. Principle of Velocity Selectivity

It has been proposed that the MEC can be used for the purpose of discriminating between traffic with different propagation velocities and directions in the arrangement shown in Fig. 2.9 [36], similar to a technique used by Merletti et al. [37, 38]. However, Merletti used the array for surface EMG recording, which poses a very different set of requirements and challenges compared to this application. The MEC with equally spaced electrodes allows to obtain recordings of the same nerve signal, delayed in time. The definition of time delay \( T \) as given by expression (2.5) for a single tripole remains valid. In a cuff of length \( L \) with equidistant electrodes, the electrode pitch \( d \) is described by

\[ d = \frac{L}{n} \]  

(2.10)
where \( n \) is the number of electrodes. The time delay is visible in the recorded data as depicted in Fig. 2.9 for several overlapping true-tripole recording channels.

\[ \text{Fig. 2.9: Cuff with overlapping true-tripole configuration (MEC).} \]

A method for the measurement of propagation velocity is to sum the outputs of the tripole amplifiers after introducing artificial time shifts \( \tau \). When \( \tau \) matches \( T \) (as defined by (2.5)), the AP peaks add constructively to give the largest signal, since the correlation between the signals on the different channels is maximised. Conversely, when using mismatched delays \( \tau \), the correlation decreases and the amplitude remains smaller. The time shift that results in the maximal amplitude corresponds to \( T \) and the sign of \( \tau \) indicates the direction of propagation. Such an arrangement is, in effect, a velocity-selective filter since \( \tau \) tunes the arrangement to one matched velocity. Experimental evidence for the suitability of this method is reported in Chapter 5.

For any summation of two signals \( V_1 \) and \( V_2 \) the r.m.s. power \( P_{\text{rms}} \) is calculated as follows:
\[ P_{\text{rms}}(v_1+v_2) = \frac{1}{T} \int_0^T (V_1^2 + V_2^2) dt = \frac{1}{T} \int_0^T (V_1^2 + V_2^2) dt + \frac{2}{T} \int_0^T V_1 V_2 dt \] (2.11)

The second integrand \( V_1 V_2 \) describes the average correlation between the two signals during time interval \( T \). This term is zero for uncorrelated signals, as the contributions from \( V_1 \) and \( V_2 \) are random and cancel over time, and \( V^2 \) for fully correlated signals \( V_1=V_2=V \). Hence, the signal power available from the sum of two sources increases with the amount of correlation. This is the basis for velocity selective recording through variation of artificial MEC time-delays \( \tau \). The effect of tuning on the signal and noise is considered in more detail in the following sections.

---

**Fig. 2.10: MEC arrangement for velocity selective recording.**
2.3.2 MEC Signal Amplitude

The signal output from each tripole is given by (2.6). The artificial delays introduced by the delay blocks are multiples of \( \tau \) as shown in Fig. 2.10, so that the output of the MEC after summation of all the delayed tripole outputs is given by:

\[
V_{\text{MEC}} = V_{\text{trip}1} + V_{\text{trip}2}e^{-j\omega \tau} + V_{\text{trip}3}e^{-2j\omega \tau} + \ldots + V_{\text{trip}(n-1)}e^{-(n-2)j\omega \tau} \tag{2.12}
\]

Substituting (2.6) in (2.12) yields:

\[
V_{\text{MEC}} = AV_{m} \sum_{i=0}^{n-2} e^{-j\omega fi} \left( e^{-j\omega (i+1)} + e^{-j\omega (i+2)} \right)
\]

\[
= AV_{m} \sum_{i=0}^{n-2} e^{-j\omega (T+\tau)} \left( 1 - 2e^{-j\omega \tau} + e^{-2j\omega \tau} \right) \tag{2.13}
\]

The MEC output signal amplitude is the magnitude of (2.13), which by evaluation of the geometric progression and trigonometric substitutions is found to be [39]:

\[
|V_{\text{MEC}}| = AV_{m} \frac{\sin\left(\frac{\omega (T - \tau) (n-1)}{2}\right)}{\sin\left(\frac{\omega (T - \tau)}{2}\right)} \cdot 4 \sin^2 \frac{\omega \tau}{2} \tag{2.14}
\]

The expression has its first maximum where \( \tau = T \), i.e. when the artificial delay matches \( T \). Since (2.5) relates \( T \) to propagation velocity, the MEC with time-delays is a tunable velocity-selective filter, which can be used to selectively record APs with a propagation time matching a chosen \( \tau \). When tuned to a given velocity expression (2.14) reduces to

\[
|V_{\text{MEC}}| = 4AVA_{m} \frac{\sin\left(\frac{\omega (T - \tau) (n-1)}{2}\right)}{\sin\left(\frac{\omega (T - \tau)}{2}\right)} \cdot \frac{\omega T}{2} \tag{2.15}
\]

As \( T \) is given through (2.5) and (2.10) as \( \frac{L}{nv} \) equation (2.15) can be rewritten as:

\[
|V_{\text{MEC}}| = 4AVA_{m} \frac{\sin\left(\frac{\omega (n-1)}{2}\right)}{\sin\left(\frac{\omega n}{2}\right)} \cdot \frac{\omega L}{2nv} \tag{2.16}
\]

Note that for \( n=2 \), expression (2.16) reduces to (2.7), which describes the single tripole output amplitude. In comparison to the single tripole spanning a cuff of identical length \( L \), the MEC yields a signal gain of:
\[
\left| \frac{S_{\text{MEC}}}{S_{\text{trip}}} \right| = (n - 1) \left| \frac{V_{m,\text{MEC}}(\omega_{\text{MEC}})}{V_{m,\text{trip}}(\omega_{\text{trip}})} \right| \left( \frac{\sin \omega_{\text{MEC}} L}{2nv} \right) \left( \frac{\omega_{\text{MEC}} L}{\sin \frac{\omega_{\text{trip}} L}{4v}} \right)^2
\] (2.17)

Using (2.17) as a fair measure of practical signal gain requires comparison of the tripole and MEC amplitudes at their respective maxima, which occur at different matched frequencies \( \omega_m \) and depend on velocity \( v \). From (2.16) it is clear, that \( \omega_m \) also depends on the spectrum of \( V_m \). Thus, finding \( \omega_m \) requires a function to describe the membrane potential \( V_m \). An approximation for an SFAP is given in [40]:

\[
V_m(t) = Ct^2 e^{-Bt}
\] (2.18)

where constants \( B \) and \( C \) chosen to be \( 3 \times 10^4 \text{ s}^{-1} \) and \( 2 \times 10^{12} \text{ V} \) respectively so that the amplitude of the AP is 100mV and the duration about 0.3ms. The corresponding spectral magnitude is:

\[
|V_m| = \frac{6C}{(B^2 + \omega^2)^2}
\] (2.19)

After substituting this expression into (2.16), \( \omega_m \) is found as the frequency for which the resulting expression is maximised. This is equivalent to:

\[
\left| \frac{\sin \frac{\omega L}{2nv}}{B^2 + \omega^2} \right| \rightarrow \text{max}
\] (2.20)

Differentiating and equating to zero gives the solution:

\[
\phi(\tan 2\phi - \phi) = \frac{LB^2}{4nv}
\] (2.21)

where \( \phi = \frac{\omega L}{4nv} \). Since the equation is transcendental, no analytical solution can be found. Instead, solving (2.21) numerically yields the maximum frequencies
plotted in Fig. 2.11 versus velocity for various \( n \). The lowest trace for \( n=2 \) corresponds to the single tripole. For this case an approximately linear relation between \( \omega_m \) and \( v \) is found. A linear relationship for the tripole has also been reported by Struijk in [41]. For a 22mm long cuff he found:

\[
\omega_{m_{\text{trip}p}} = 250v
\]  

(2.21)

which is in good agreement with Fig. 2.11, also for a 22mm cuff. As the product of velocity and number of tripoles increases, the trigonometric term in (2.20) can be approximated by a first-order linear function and \( \omega_m \) is found from:

\[
\left| \frac{\omega L}{2nv(B^2 + \omega^2)} \right| \to \text{max}
\]  

(2.22)

The maximum can now be calculated by equating the first derivative to zero, which results in:

\[
\omega_{m_{\text{MEC}p}} = B
\]  

(2.23)

The asymptotical approach toward \( B \) is visible in Fig. 2.11 for \( n \) larger than about 4. It can be concluded, that in a MEC, where \( n \) is large and for velocities higher than around 40m/s, the frequency yielding the highest recording amplitude is nearly constant at \( \omega_{m_{\text{MEC}p}} = B \). For smaller velocities approximations (2.22) does not apply and \( \omega_m \) must be calculated in each case from (2.22) or can be taken from Fig. 2.11.
Fig. 2.11: Frequencies of maximum signal amplitude vs. velocity.

Using the matched frequencies obtained from (2.21), the signal ratio according to (2.17) is plotted in Fig. 2.12 for a 20mm long cuff. A striking feature of the graph is a peaking of the signal gain. The position of the peak is velocity dependent and occurs at lower velocities for higher numbers of \( n \). In a standard tripole, APs from slower fibres yield a smaller signal than those from faster fibres due to the velocity dependence of scaling factor \( A \) (Eqn. (2.5)), which makes it difficult to extract signals from slower fibres in naturally occurring ENG. As the MEC accentuates the small signals from slow fibres in favour of the large signals from fast fibres, a MEC should enable to record from a wider fibre population compared to the conventional tripole. To achieve optimum low-velocity gain, \( n \) is chosen near the low-velocity signal peak.
2.3.3 MEC Noise and SNR

As is the case for a single tripole, lead- and interface resistance produce thermal noise voltage $V_l$ and the resistive element $R_a$ produces thermal noise voltage $V_a$. Some of the noise sources $V_a$ and $V_l$ contribute noise to more than one tripole in the overlapping configuration. Furthermore, the voltage and current noise of each amplifier in the array affect the MEC noise. Also the amplifier input impedance has an effect, as finite impedance allows noise currents to flow. As the fundamental performance achievable by the MEC configuration is to be established first, the design dependent noise contributed by the amplifier array is considered separately in section 2.4. Furthermore, all amplifiers are assumed to have infinite input impedance, so that noise generators $V_l$ do not generate any current flow. This assumption is practical for cases where the input impedance is much bigger than the impedance present at the amplifier inputs due to the cuff, i.e.
for impedances above several kilo-ohms. Input impedance satisfying this requirement is readily available with MOS as well as bipolar input devices. The network representation of the nerve in Fig. 2.10 is linear so that the noise sources can be considered separately and superimposed later. Fig. 2.13a shows the network if only a single noise source is assumed active.

![Diagram showing noise contribution and noise sources](image)

*Fig. 2.13: a. Noise contribution of the axonal resistance to amplifiers in the array. b. Noise sources associated with $R_i$.*

Noise voltage source $V_{ai}$ associated with the $i$-th resistive element $R_{ai}$ appears across the input of amplifier $i$. In addition, $V_{ai}$ causes current $I_a = V_{ai}/(nR_{ai})$ to flow along the chain of resistances $R_a$ as shown. This current generates voltages $R_{ai}I_a = V_{ai}/n$ across the inputs of all amplifiers. This consideration is true for all noise sources $V_{ai}$ so that superposition yields the total voltage $V'_{ai}$ at amplifier $i$ as:

$$V'_{ai} = V_{ai} - \frac{1}{n} \sum_{j=1}^{n} V''_{aj}$$  \hspace{1cm} (2.24)

Assuming amplifier gains of unity dipole noise $V_{n_d,i}$ is identical with $V'_{ai}$. 

44
Noise sources \( V_i \) associated with \( R_i \) (Fig. 2.13b) do not cause any current flow as the amplifier input impedance is assumed infinite. These sources therefore contribute only to individual dipoles as:

\[
V'_i = V_i - V_{i+1}
\]  

(2.25)

The tripole noise for the \( i \)-th tripole in the MEC is given as the difference of adjacent dipoles, so that the sum terms from (2.24) cancel:

\[
V_{\text{trip noise}_i} = V_{a_i} - V_{a(i+1)} + V_i - 2V_{i(i+1)} + V_{i(i+2)}
\]  

(2.26)

As the network is linear, axonal and lead noise sources can be considered individually. Starting with \( V_i \) and using (2.12) and (2.26) the MEC output noise voltage can be written as:

\[
V_{\text{MEC}_i} = \left\{ V_{i_1} - 2V_{i_2} + V_{i_3} + V_{i'_2} - 2V_{i_3} - V_{i_4}' + V_{i_4}'' + V_{i_5}'' + \ldots \right\}
\]  

(2.27)

where each hyphen denotes a delay by time \( \tau \) introduced before summation to tune the MEC to the signal to be recorded as described in 2.3.2. To calculate the noise power, the square of (2.27) is formed as discussed in 2.3.1. It was shown that the squares of the uncorrelated signals, i.e. \( V_i \) with different indices, can immediately be summed, so that the r.m.s. noise power is:

\[
P_{\text{MEC}_i} = V_{i_1}^2 + (V_{i_2} - 2V_{i_2})^2 + (V_{i_3} - 2V_{i_3} + V_{i_3})^2 + (V_{i_4} - 2V_{i_4} + V_{i_4}^*)^2 + \ldots
\]  

(2.28)

Since in the frequency domain a time delay \( \tau \) is expressed as \( e^{j\omega \tau} \), (2.28) can be rewritten as:

\[
P_{\text{MEC}_i} = \left\{ V_{i_1}^2 + V_{i_2}^2 + V_{i_3}^2 \left| e^{-j\omega \tau} - 2 \right|^2 + \sum_{i=3}^{n} V_{i_1}^2 \left| e^{-j\omega \tau(i-3)} - 2e^{-j\omega \tau(i-2)} + e^{-j\omega \tau(i-1)} \right|^2 \right\}
\]  

(2.29)
The coefficients in (2.29) are evaluated individually and are then summed. The coefficient \(|e^{-j\omega r} - 2|^2\) for example yields \(5 - 4\cos\omega r\). In a symmetrical MEC and for a homogenous nerve all noise sources are of identical magnitude, so that (2.29) evaluates to:

\[
P_{\text{MEC}} = 4V_i^2 + V_f^2 \left[ 16\sin^2 \frac{\omega r}{2} + (16n - 48)\sin^4 \frac{\omega r}{2} \right]
\] (2.30)

This expression is valid for \(n>2\). The noise from the axonal resistance is calculated in a similar way, knowing that

\[
P_{\text{MEC},a} = V_a^2 + \sum_{n=2}^{n-1} \left| e^{-j\omega r(i-2)}(V_{an} - V_a) \right|^2 + \left| e^{-j\omega r(n-1)}V_{an} \right|^2
\] (2.31)

which for identical noise magnitudes yields:

\[
P_{\text{MEC},a} = 2V_a^2 + V_a^2 (4n - 8)\sin^2 \frac{\omega r}{2}
\] (2.32)

For comparison between arrangements with different numbers of section \(n\) in a cuff of constant length it is convenient to define a noise voltage \(\hat{V}_a\), representing the axial thermal noise produced across the entire length of the cuff. \(\hat{V}_a\) relates to the sectional noise as

\[
\hat{V}_a = \sqrt{n}V_a
\] (2.33)

The total noise power is the sum of the uncorrelated terms (2.30) and (2.32):

\[
P_{\text{MEC}} = \left\{ \begin{array}{l}
4V_i^2 + \frac{2\hat{V}_a^2}{n} \\
+ V_f^2 \left[ 16\sin^2 \frac{\omega r}{2} + (16n - 48)\sin^4 \frac{\omega r}{2} \right] + \hat{V}_a^2 (4 - \frac{8}{n})\sin^2 \frac{\omega r}{2} 
\end{array} \right\}
\] (2.34)

This expression is inconvenient due to the different orders of sine functions. However, by replacing all squares by the power of four and rearranging (2.34) to
the form \( P_{\text{MEC}} = P_{\text{max}} \sin^4 \frac{\omega \tau}{2} + P_{\text{min}} \cos^4 \frac{\omega \tau}{2} \) the following approximation is found:

\[
P_{\text{MEC}} = \left( \sqrt{(16n - 28)V_i^2 + (4 - \frac{6}{n} \hat{V}_a^2 \sin^2 \frac{\omega \tau}{2}} + \sqrt{4V_i^2 + \frac{2}{n} \hat{V}_a^2 \cos^2 \frac{\omega \tau}{2}} \right)^2
\]

(2.35)

The relative error made by a substitution of \( \sin^2 x \) with \( \sin^4 x \) is \((1-\sin^2 x)\). For the cosine substitution the relative error is \((1-\cos^2 x)\). Since \( P_{\text{max}} \) is larger than \( P_{\text{min}} \), the substitution of the sine function has a larger effect on the overall error. Therefore, the error is largest for arguments near zero and at periods of \( \pi \). In many practical cases the argument \( \omega \tau / 2 \) remains well between these extremes so that approximation (2.35) is applicable. Typical examples of the noise described by (2.35) are plotted in Fig. 2.14. The top six traces are for \( n \) ranging from 7 to 12 with a total axial resistance \( nR_a \) of 6kΩ, a lead/contact resistance of 1kΩ and a spot frequency \( \omega = 2\pi 1 \text{kHz} \). The lower trace is for \( n=7, nR_a=7 \text{kΩ}, R_f=200 \Omega \) and \( \omega=2\pi 3 \text{kHz} \). The markers show results obtained from simulation of the circuit of Fig. 2.10 using CADENCE design tools. For all examples expression (2.35) describes the simulated results closely with the expected deviations while (2.34) (not plotted) matches the simulation results precisely.

In analogy to the signal gain calculated in (2.17), the ratio of MEC noise to the noise of a single tripole \( G \) can be determined from (2.9) and (2.35):

\[
G = \frac{\text{SNR}_{\text{MEC}}}{\text{SNR}_{\text{trip}}} = \frac{(n-1)\sin^2 \frac{\omega_{\text{MEC}} L}{2nv} \sqrt{6V_i^2 + \hat{V}_a^2}}{\sqrt{(16n - 28)V_i^2 + (4 - \frac{6}{n} \hat{V}_a^2 \sin^2 \frac{\omega_{\text{MEC}} L}{2nv}} + \sqrt{4V_i^2 + \frac{2}{n} \hat{V}_a^2 \cos^2 \frac{\omega_{\text{MEC}} L}{2nv}} \right)^2 \frac{\sin^2 \frac{\omega_{\text{MEC}} L}{4v}}{4v}
\]

(2.36)
For a given cuff, $G$ is a function of $v$ and $n$. $G$ is shown in Fig. 2.15 evaluated at the frequencies of highest signal amplitude $\omega_m$. The plot reveals close resemblance to the behaviour of the signal ratios plotted in Fig. 2.12, which suggests that fixing the number of electrodes to maximise the signal gain for a given velocity comes at the expense of increased noise. However, for low velocities the gain in signal amplitude is larger than the increase in noise as the SNR improvement over the conventional tripole in Fig. 2.16 shows. For higher velocities the SNR compared to the tripole degrades. Fortunately, this degradation is small and occurs only for velocities, which already yield a comparably high SNR in the tripole.
Fig. 2.15: Change in MEC noise with n (relative to a single tripole).

Fig. 2.16: SNR of the MEC relative to the SNR of a single tripole.
2.4 NOISE MATCHING

So far only the noise produced by the MEG resistances has been considered, ignoring additional noise contributed by the array of amplifiers. In this section the effect of amplifier noise is examined when interfacing the amplifier with the nerve cuff. Noise figure $F$ is a commonly used measure of the degradation in noise performance due to the added circuitry. The general definition of the noise figure is [42]:

\[ F = \frac{\text{input SNR}}{\text{output SNR}} \]  
\[ (2.37) \]

The situation for a single electrode pair with resistance $R_{\text{cuff}}$ connecting to an amplifier is illustrated in Fig. 2.17 so that input and output refer to the amplifier terminals as shown. The noise voltage generated by the amplifier is represented by current and voltage sources $I_p$ and $V_p$ at the inputs. The noise generated by the cuff impedance alone is $V_{\text{cuff}}$. In this configuration $F$ expresses the percentage increase in recorded noise power due to the amplifier noise sources compared to the ideal case of a noiseless amplifier. Assuming uncorrelated noise sources, noise power $V_{\text{rec}}^2$ is the algebraic sum of all contributing effects:

\[ V_{\text{rec}}^2 = V_p^2 + V_{\text{cuff}}^2 + I_p R_{\text{cuff}}^2 \]  
\[ (2.38) \]

As any signal applied across $R_{\text{cuff}}$ appears unattenuated at the amplifier inputs the signal contents and amplifier gain in nominator and denominator of (2.37) cancel so that $F$ is given by:

\[ F = \frac{V_p^2 + V_{\text{cuff}}^2 + I_p R_{\text{cuff}}^2}{V_{\text{cuff}}^2} = 1 + \frac{V_p^2 + I_p R_{\text{cuff}}^2}{V_{\text{cuff}}^2} \]  
\[ (2.39) \]

Since the noise power $V_{\text{cuff}}^2$ produced by resistance $R_{\text{cuff}}$ is proportional to $R_{\text{cuff}}$ by a factor $4kTB$ (see Chapter 3 on noise) $F$ can be rewritten as:
This expression has a minimum where the derivation of $F$ by $R_{cuff}$ equals zero.

The minimum is found for:

$$ R_{cuff} \bigg|_{\text{minimum } F} = \frac{V_p}{I_p} $$

(2.41)

The ratio $V_p/I_p$ is termed the noise resistance of the amplifier. The noise figure is minimised under matching conditions, i.e. when the noise resistance equals the load resistance ($R_{cuff}$). In general, transformers can be used to match any given amplifier noise resistance to the cuff by impedance transformation [43]. However, transformers are bulky components and therefore not suitable for integration. Fortunately, with a fully customised recording system it is possible to design the noise resistance as required, which removes the need for transformers in most practical cases [44]. The noise recorded by the matched amplifier results from substitution of (2.41) into (2.38), which yields:

$$ V_{\text{ref}}^2 \bigg|_{\text{matched}} = 2V_p^2 + V_{cuff}^2 $$

(2.42)

It is clear that noise matching reduces the amplifier noise contribution to a minimum but does not make any statement about the total recorded noise or the SNR.

---

**Fig. 2.17: Equivalent circuit for noise matching cuff and amplifier.**
2.4.1 Noise-Matching to a single Dipole

Assuming a cuff resistance of $2k\Omega$ leads to the following requirement:

$$V_p < \frac{V_{cuff}}{2} = \sqrt{\frac{4kT \cdot 2k\Omega}{2}} = 4nV/\sqrt{Hz} \quad (2.43)$$

which shows that ideally the dipole amplifier voltage noise should be kept below $4nV/\sqrt{Hz}$ and the current noise evaluated from expression (2.41) around $2pA/\sqrt{Hz}$.

This result applies to a single dipole (i.e. monopolar recording) and has to be modified for an array of dipoles such as in a MEC configuration as due to the partial overlap between dipoles and the shorted end electrodes the current noise contributions differ.

2.4.2 Noise-Matching to an Array of Dipoles

The schematic diagram considering voltage noise in an array of dipoles is shown in Fig. 2.18. As the amplifiers are assumed to have infinite input impedance, the noise sources $V_{pi}$ appear across the input of the associated dipole amplifier. For the $i$-th dipole this is expressed as:

$$V_{dip,i} = V_{pi} \quad (2.44)$$

The effect of amplifier current noise $I_{pi}$ is more complicated, as $I_{pi}$ causes a current $I_{mi}$ to flow within mesh $i$ as well as a current $I_{xi}$ along the chain of $R_a$ (Fig. 2.19). The currents are found by network analysis as:

$$I_{xi} = I_{pi} \frac{1}{n}$$

$$I_{mi} = I_{pi} \frac{n-1}{n} \quad (2.45)$$

Superposition of all current sources $I_{pi}$ and addition of voltage noise contribution $V_{dipa,i}$ yields the total noise voltage at dipole $i$ due to the amplifier current and voltage noises:
In this expression all current sources are uncorrelated except for \( I_{pl} \), which appears in both terms of the sum. Taking these relations into account and assuming identical current noise amplitudes the power in \( V_{di} \) is given by:

\[
V_{di}^2 = I_p^2 \left[ (2R_f + R_a)^2 + 2R_f^2 + \frac{R_a^2}{n} - 2 \frac{R_a}{n} (2R_f + R_a) \right] + V_p^2 \tag{2.47}
\]

Choosing \( R_f = 400\Omega \) and \( R_a = 1.2k\Omega \), which would yield a cuff impedance of 2kΩ in (2.43), and with \( n = 10 \) \( V_{di}^2 \) evaluates to approximately \( (I_p 1.996k\Omega)^2 + V_p^2 \). This corresponds to expression (2.38), with \( (I_p 2k\Omega)^2 + V_p^2 \). Comparison shows that the coefficients are very similar, so that the matching noise resistance of the amplifiers whether used for a single dipole or an array structure remains approximately the same.

\[\text{Fig. 2.18: Voltage noise sources in an overlapping array of dipoles.}\]
2.4.3 Noise-Matching to a tripole and MEC

For each overlapping tripole in a MEC the output noise is calculated as the difference of two adjacent dipoles, where the dipole noise is given by (2.46). The sum terms cancel and the tripole noise due to the amplifier noise sources is given by:

\[ K_{i \text{ p amp i}} = (3 \beta + K) \left[ I_{p i} - I_{p M} \right] + V_{p i} - V_{p i+1} \]  

(2.48)

The noise of a single tripole in the array is calculated as discussed for dipole noise. However, the noise output is higher for tripoles in the centre of the cuff where all noise sources are present and lower for tripoles at the cuff ends (i.e. the index \( i \) in (2.48) is smaller than unity or exceeds \( n \)). If sources with invalid indices are assumed to be zero, expression (2.48) applies to all tripoles in an array and also for a single tripole.
As is the case for cuff thermal noise discussed in section 2.3, mutual
cancellation of parts of the tripole amplifier noise occurs after delay and
summation in a MEC. A variation between a minimum output noise, when no
correlation between the sources can be assumed, and a maximum with total
correlation is expected. Summation of all the tripole noise outputs with time delay
yields:

\[
V_{\text{trip}_{\text{amp}}} = \left\{ \begin{array}{l}
I_{n1}(\alpha - R_r e^{-j\omega t}) + I_{p2}(-\alpha + \alpha e^{-j\omega t} - R_r e^{-2j\omega t}) \\
+ \sum_{j=3}^{n-2} I_{n j}(R_i - \alpha e^{-j\omega t} + \alpha e^{-2j\omega t} - R_i e^{-3j\omega t}) e^{-j\omega t(j-3)} \\
+ I_{p1}(R_i - \alpha e^{-j\omega t} + \alpha e^{-2j\omega t}) e^{-j\omega t(n-4)} \\
+ I_{p}(R_i - \alpha e^{-j\omega t}) e^{-j\omega t(n-3)} \\
+ \sum_{j=1}^{n} (V_{p j} - V_{p j+1})
\end{array} \right. \quad (2.49)
\]

where \(\alpha = 3R_r + R_s\). Evaluation of the r.m.s. power in a 1Ω load is uncomplicated
assuming identical noise source amplitudes and following the procedure outlined
in section 2.3. However, the result is a lengthy expression. For \(n \geq 4\) it is:

\[
V^2_{\text{MEC}} = I_p^2 \left[ 6\alpha^2 - 8\alpha R_i \cos \omega t + 4R_i^2 - 4\alpha^2 \cos 2\omega t + 4\alpha R_i \cos 2\omega t \\
+ (n-4) \left( \left. 2(R_i^2 + \alpha^2) - (4\alpha R_i + 2\alpha^2) \cos \omega t \\
+ 4\alpha R_i \cos 2\omega t - 2R_i^2 \cos 3\omega t \right. \right) \right] + V_p^2 \left[ 2 + (4n-8) \sin^2 \frac{\omega t}{2} \right] \quad (2.50)
\]

and for \(n=3\):

\[
V^2_{\text{MEC}} = I_p^2 \left[ 5\alpha^2 + 3R_i^2 - (6\alpha R_i + 4\alpha^3) \cos \omega t + 4\alpha R_i \cos 2\omega t \right] + V_p^2 \left[ 2 + (4n-8) \sin^2 \frac{\omega t}{2} \right] \quad (2.51)
\]

These results are not very intuitive, but a plot for the typical parameters used
before \((R_i=400Ω\, \text{and} \, R_s=1.2kΩ)\) and an amplifier current and voltage noise of
2pA/√Hz and 4nV/√Hz respectively shows that the peak amplitude occurs for Ωτ=π and the minimum at τ=0 (Fig. 2.20).

![Fig. 2.20: MEC noise due to amplifier noise sources variation with τ.](image)

Evaluation of (2.50) with these arguments yields for n≥4:

\[
V_{\text{amp MEC}}|_{\omega\tau=0} = (2\alpha^2 - 4\alpha R + 4 R_i^2) I_p^2 + 2 V_p^2
\]

\[
V_{\text{amp MEC}}|_{\omega\tau=\pi/2} = \left[ 10\alpha^2 + 12\alpha R + 4 R_i^2 + (n-4)(4 R_i^2 + 8\alpha R + 4\alpha^2) \right] I_p^2 + (4n-6) V_p^2
\]

(2.52)

Using typical parameters results in:

\[
V_{\text{amp MEC}}|_{\omega\tau=0} = (2.88\text{kΩ}) I_p^2 + (1.41)^2 V_p^2
\]

\[
V_{\text{amp MEC}}|_{\omega\tau=\pi/2} = (16.06\text{kΩ}) I_p^2 + (5.83)^2 V_p^2
\]

(2.53)

which shows that the matching noise resistance varies with frequency and artificial time delay between a minimum of 2.0kΩ (2.88kΩ/1.41) and a maximum of 2.8kΩ (16.06kΩ/5.83). \(R_{\text{noise}}\) for different configurations including single tripoles and tripoles in an array without delay-and-add are compared in Table 2.2.
for the typical parameters used before. The table shows that the matched noise resistance is around 2kΩ for all the conventional dipole and tripole configurations. The MEC however yields a slightly higher noise resistance of around 2.5kΩ. The dependency on artificial time-delay and frequency is small.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>$R_{\text{noise}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single dipole</td>
<td>2.0kΩ</td>
</tr>
<tr>
<td>Dipole in array</td>
<td>2.1kΩ</td>
</tr>
<tr>
<td>Single tripole</td>
<td>2.4kΩ</td>
</tr>
<tr>
<td>Tripole in array (centre)</td>
<td>2.4kΩ</td>
</tr>
<tr>
<td>MEC, $n=10$</td>
<td>2.0kΩ-2.8kΩ</td>
</tr>
<tr>
<td></td>
<td>(depends on $\omega\tau$)</td>
</tr>
</tbody>
</table>

Table 2.2: Matched noise resistance for various amplifier configurations.

### 2.5 MEC SNR Improvement including Amplifier Noise

In section 2.4 the SNR of the MEC was compared to that of a single tripole, considering only cuff thermal noise. Fig. 2.16 showed that for low velocities a considerable improvement in SNR is achieved for a small loss at higher velocities. The amplifier noise contribution has been examined in the previous section, so that now the SNR including all noise sources can be calculated. Using $R_l=400\Omega$, $R_o=1.2k\Omega$ and amplifier noise sources of $V_n=4nV/\sqrt{\text{Hz}}$ and $I_n=2pA/\sqrt{\text{Hz}}$ yields the SNR improvement plotted in Fig. 2.21. As expected, comparison with Fig. 2.16 reveals that the maximum SNR improvement has decreased due to the additional noise sources. Fortunately, the MEC still performs almost 1.5 times better than a single tripole at low velocities. It is also clear from the figure that increasing the
number of electrodes above a certain value (around 10) decreases the MEC SNR for all velocities.

![SNR Comparison Graph](image)

**Fig. 2.21:** SNR of the MEC compared to a single tripole considering both, thermal and amplifier noise.

### 2.6 GENERAL SYSTEM SPECIFICATIONS

In the previous section it was shown that the matched amplifier noise resistance changes with the artificial delay introduced by the MEC. Furthermore, the proposed recording system is intended to provide dipole as well as MEC recording using the same input amplifiers:

- **Dipoles**, to be compatible with previous recording approaches but still improve on signal quality due to higher SNR.
- **Tripoles** in a MEC configuration to extract additional features from the ENG.
From the comparison in Table 2.2 it appears to be a suitable compromise to design the amplifiers with a noise resistance of around 2kΩ. This sufficiently matches the amplifier to all standard configurations and is the optimum noise resistance of the MEC without delays. The development of a very low-noise front-end, a high-gain system with high dynamic range and the option of making the dipole gains adaptable to cancel EMG are of further importance. A summary of these core requirements and associated challenges is given in Table 2.3. They set the framework for the discussions in the following chapters.

The dimension of practical nerve cuffs is limited by the anatomy of the nerve at the implantation site, restricting the length of the cuff to approximately 25mm. The physical length of the cuff also restricts the number of electrodes that can be embedded in its wall. For this application a cuff length of 18mm with an electrode pitch of 1.8mm and a width of around 0.8mm is chosen, yielding a maximum of 11 electrodes that can be placed inside the cuff. This results in 10 dipole recording channels and 9 true-tripole channels.

<table>
<thead>
<tr>
<th>Aim</th>
<th>Approach</th>
<th>Challenges</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Better SNR.</td>
<td>• Multi-electrode cuff with several recording channels.</td>
<td>• Combination of many channels on one chip with low power consumption and limited area.</td>
</tr>
<tr>
<td>• Determination of AP propagation velocity and direction</td>
<td>• Low-noise front-end.</td>
<td>• Experimental validation of information extraction capability.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Low-power, low-noise design.</td>
</tr>
<tr>
<td>• Improved interference rejection.</td>
<td>• Active electronics to increase signal quality.</td>
<td>• Low-noise design.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removal of residual EMG.</td>
</tr>
</tbody>
</table>

Table 2.3: Areas sought to improve compared to other designs.
To achieve low-noise operation, the first-rank amplifiers are further divided into a cascade of two amplifiers, so that the amplifier immediately connected to the cuff can be optimised for low-noise operation and the second amplifier boosts the gain and provides a well-controlled interface to the following stages (Fig. 2.22). To add flexibility to the system, the dipole-channels as well as tripole-channels are made accessible through a channel-switching multiplexer. The analogue signal at the multiplexer output is available for further processing, e.g. it can be converted into digital form to facilitate transmission out of the body. A diagram of the complete system is shown in Fig. 2.22.

Several of these electrode units can be combined with a controller unit to form a comprehensive and flexible nerve monitoring system. An example configuration with three electrodes and a control unit is shown in Fig. 2.23. The small electrode units are placed on the nerve, although the control unit may be located further away at a more convenient implantation site, as the ENG has already been amplified and multiplexed onto a single data wire by the cuff electronics.

![System diagram for one cuff](image-url)
Fig. 2.23: Example configuration of a monitoring system with three smart electrodes.

The core requirements for one electrode unit are summarized in Table 2.4. The pass-band of the recording system is matched to the properties of ENG and EMG: The cut-off frequencies of around 250Hz and 5kHz remove much of the EMG but pass the significant portion of the nerve signal. The voltage gain is not critical, but a magnitude between 10,000 and 50,000 seems adequate for signal amplitudes in the microvolt range.

Suitable manufacturing processes available at a low cost are the AMS 0.8μm CMOS and BiCMOS double-metal, double-poly processes by Austria-microsystems [45]. These processes are chosen as they are used by other parts of the recording system, are comparably cheap and comprehensive design kits are available. Both are 5V analogue processes, the choice of which sets the maximum supply voltage to ±2.5V.
Table 2.4: Core system specification.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pass-band</td>
<td>250Hz – 8kHz</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>10,000</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>±2.5V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt; 20mW</td>
</tr>
<tr>
<td>Input referred voltage noise in passband</td>
<td>&lt;400nVrms</td>
</tr>
<tr>
<td>Input referred current noise in passband</td>
<td>&lt;200pArms</td>
</tr>
<tr>
<td>Dipole channels</td>
<td>10</td>
</tr>
<tr>
<td>Tripole channels</td>
<td>9</td>
</tr>
<tr>
<td>active area</td>
<td>&lt;15mm$^2$</td>
</tr>
</tbody>
</table>

The noise performance of the system is determined by the input stage, so that low-noise design is critical at this stage. Chapter 3 is concerned with designing for optimum noise behaviour. The overall system gain is very high and is best achieved with a cascade of amplifiers. Two amplifiers with a gain of 100 provide the dipole gain of 10,000. After summation further amplification is possible, because EMG interference is cancelled to a high degree, i.e. the signal occupies less dynamic range. Offset voltages at the preamplifier outputs must be limited, as they are amplified by the following stages. Therefore, chapter 5 describes a filter arrangement to remove DC offsets before gain boosting. To achieve trimming of the differential tripole amplifier gains, automatic feedback control may used [46]. The approach takes advantage of the fact that over the dimensions of a typical cuff the EMG signal shows no significant phase variation. Therefore, the feedback control system is only required to adapt to amplitude variations in the EMG. Although the EMG cannot be completely eliminated by trimming the amplifier gains in this way, the requirement for post-filtering is reduced to manageable levels resulting in a system that is implantable. Increasing
the signal-to-interference (S/I) ratio of the ENG signal before digitisation increases the available dynamic range and relaxes the requirement on the resolution of the A/D. The practical implementation of the control circuits is still under investigation and will be part of a forthcoming Ph.D. thesis at the University College London by I. F. Triantis. The feasibility of implementing automatic gain control has been demonstrated with measured results in [47] and is discussed in chapter 5.

2.7 CONCLUSIONS

The signal amplitude of the MEC depends on the frequency, number of tripoles in the cuff and the artificial time delay. Choice of the introduced time delay allows recording from nerves with a specific conduction velocity. Having selected the velocity of interest, a frequency is found at which the recorded signal amplitude is highest. The recorded signal may be filtered around this frequency to immediately increase the SNR of the MEC. Furthermore, it is shown that an optimum number of tripoles exists, which yields maximum signal amplitudes and maximum SNR. The recording gain of low-velocity APs is higher than in a standard tripole, which is very advantageous as the signals from these fibres tend to be small when recorded with a tripole. Also the SNR at low velocities improves over the tripole. This should enable selective recording from a wide nerve population.

The effect of amplifier noise on the MEC performance was investigated and a specification for the required noise matching is derived. The SNR decreases when amplifier noise is considered. However, an improvement in the critical low-velocity region over the tripole is still given.
It can be concluded that the MEC yields several advantages over recording with a single tripole, and appears suitable to extract additional information from ENG to improve future neuroprostheses.
CHAPTER 3
ELECTRONIC NOISE

3.1 NOISE MECHANISMS

The smart electrode is required to amplify signals in the microvolt range with as little degradation in signal quality as possible. In contrast to interference which originates outside the circuit and must be prevented from entering the system, e.g. by the use of a tripole cuff, noise is produced within the circuit and therefore is a property inherent of a given design. Its reduction is achieved by low-noise circuit design techniques.

There are three main sources of noise that play a part in modern solid-state devices. These are referred to as thermal, shot- and flicker-noise. Other noise phenomena such as popcorn noise exist but are insignificant for this application compared to the major noise effects and are not treated in the following discussion.

3.1.1 THERMAL NOISE
Physical resistors and the resistances associated with active devices contribute to thermal noise (also known as resistor noise, Johnson noise or Nyquist noise). It is caused by the random collision of carriers with the atomic lattice and is characterised by a noise power, which is distributed equally over the whole frequency band up to the infrared spectrum. A typical noise energy spectrum is plotted diagrammatically in Fig. 3.1. The mean square of the thermal noise power \( P_\text{th} \) within a bandwidth \( \Delta f \) across the terminals of a resistive element is described by
where \( T \) is the absolute temperature in Kelvin, \( k \) is Boltzmann's constant and \( R \) is the ohmic resistance of the conductor [43]. The overbar represents an average value. The r.m.s. noise voltage \( \bar{v} \) relates to \( \overline{P_R} \) as:

\[
\bar{v}^2 = \overline{P_R}
\]

3.1.2 SHOT NOISE

The second noise source is shot-noise, caused by the random passage of charge carriers across a potential barrier such as in the \( pn \)-junctions of a diode or bipolar transistor. The shot-noise r.m.s. power for current \( I \) crossing the barrier is given by

\[
\overline{P_S} = 2qI\Delta f
\]

In general, the total current across a \( pn \)-junction is composed of electron-current \( I_n \) and hole-current \( I_p \). Furthermore, the current for each type of carrier is the sum of drift and diffusion components:

\[
I_p = I_{p,\text{drift}} + I_{p,\text{diffusion}}
\]

\[
I_n = I_{n,\text{drift}} + I_{n,\text{diffusion}}
\]

Since at equilibrium, i.e. without any voltage applied externally, drift and diffusion components for each carrier type are equal and opposite, so that they
balance. As expected, the net current flow in the device is zero under this condition.

The carriers contributing to drift-current are generated by thermal excitation. Some of the carriers are swept across the potential barrier at the junction, with the amount of crossing carriers proportional to the number of available carriers. The height of the potential barrier has no effect. Hence, drift current is proportional to the junction temperature and insensitive to the applied voltage. However, it can be shown that the diffusion component is increased from its equilibrium value by an applied voltage $V$ according to [48]:

$$I_{\text{diffusion}} = I_{\text{diff0}} e^{V/U_{th}}$$  \hspace{1cm} (3.5)

where $U_{th}$ is the thermal voltage and $I_{\text{diff0}}$ the equilibrium diffusion current.

The total junction current $I$ is therefore given by

$$I = (I_{p_{\text{diff0}}} - I_{n_{\text{diff0}}}) e^{V/U_{th}} - (I_{p_{\text{diff}}} - I_{n_{\text{diff}}})$$  \hspace{1cm} (3.6)

As at equilibrium diffusion and drift components are of equal magnitude the expression can be simplified to

$$I = (I_p - I_n) e^{V/U_{th}} - (I_p - I_n) = I_0 e^{V/U_{th}} - I_0$$  \hspace{1cm} (3.7)

All components are uncorrelated and show shot noise so that the resulting noise power is

$$P_{S_{\text{pm}}} = P_S[I_0 e^{V/U_{th}}] + P_S[I_0]$$  \hspace{1cm} (3.8)

Using expression (3.7) this is equivalent to [49]:

$$P_{S_{\text{pm}}} = P_S(I + I_0) + P_S(I_0) = P_S(I + 2I_0)$$  \hspace{1cm} (3.9)

The diffusion current $I_0$ is very small, in the range of femto-amperes [45, 50] and can be neglected in most common cases where the total bias current $I$ is much
larger than its component $I_0$. The shot-noise power spectrum exhibits the same
distribution as thermal noise (Fig. 3.2).

![Shot-noise power spectrum](image)

Fig. 3.2: Shot-noise power spectrum.

3.1.3 FLICKER NOISE
Due to its power distribution flicker noise (also known as 1/f-, excess-, pink-, contact-noise etc.) is important especially in low-frequency applications such as this. Its spot noise power is inversely proportional to frequency, so that its magnitude is largest at very low frequencies. In practical applications both, flicker-noise and noise with a flat spectral distribution are present. The point at which the two power contributions are equal is termed the flicker-noise corner frequency (Fig. 3.3). Several formal theories have been presented to describe the flicker-noise mechanism [51-55]. After some controversy [56] it is now widely accepted that a wide distribution in time constants is likely to be responsible for the 1/f spectrum [57]. The physical origin is described by the carrier number fluctuation theory also known as the trapping-detrapping model, originally proposed by McWorther [51]. He demonstrated that carriers communicating with trapping levels at some depth in the surface oxide of the device through tunnelling mechanism are a very likely cause for the 1/f noise power spectrum due to the characteristic distribution of the time intervals between trapping and release of the carrier. Trapping and release of carriers is observed as fluctuation in the currents of a transistor [58]. Flicker noise is prevalent in MOS transistors and in lateral
bipolar transistors using a base region covered by polysilicon, because both have a conduction area exposed to a region with high trap density (polysilicon). Polysilicon resistors also show potentially significant $1/f$-noise due to the presence of charge traps at the silicon grain boundaries [54]. In general, the flicker-noise power is described by the empirical model [59]:

$$\bar{P}_{1/f} = \frac{K_Y}{f^\gamma} \Delta f$$  \hspace{1cm} (3.10)

where $K_Y$ is a noise constant and exponent $\gamma$ is another constant typically close to unity.

\begin{figure}[h]
  \centering
  \includegraphics[width=\textwidth]{flicker_noise.png}
  \caption{Flicker noise power spectrum on a log-log scale.}
  \label{fig:flicker_noise}
\end{figure}

### 3.2 NOISE MODELS

In the design and analysis of low-noise circuits it is useful to work with standard noise models, which describe the noise behaviour of a device over its intended range of operation. Models for resistors, MOS- and bipolar transistors are described in this section. These models represent the noisy device by a combination of a noise source with an ideal noiseless component. Capacitors do not exhibit any noise except that associated with parasitic resistance. Due to the small size of this noise compared to the noise generated by other components it can be ignored in this application.
3.2.1 NOISE IN RESISTORS

The main source of noise in a poly-silicon resistor is thermal noise, which is related to the resistance as given by Eqn. (3.1). Additional flicker noise is present, caused by traps at the silicon grain boundaries [54]. The flicker-noise component can be modelled by [60]:

\[
\frac{P_{R,\text{f}}}{W L f} = K_R \frac{\Delta f}{W L f} 
\]

(3.11)

where \(W\) and \(L\) are the effective width and length of the resistor respectively and \(K_R\) is a noise constant. Note that standard models for circuit simulators do not include resistor flicker noise [61], and \(K_R\) is therefore not specified for the AMS processes. Reference [60] suggest \(K_R\) be in the range of \(10^{-22} (\text{Vm})^2\). This value has been confirmed by own measurements on an 80kΩ POLY1 resistor with width 5μm and length 18,971μm. The measured voltage noise spectrum is shown in Fig 3.4, from which a \(K_R\) of \(0.9 \times 10^{-22} (\text{Vm})^2\) was extracted.

![Fig. 3.4: Flicker-noise voltage spectrum for 80kΩ POLY1 resistor.](image)

A noisy resistor can hence be modelled by a noise-free resistor in series with a noise-source, which combines both thermal- and \(1/f\)-noise, as shown in Fig. 3.8.
3.2.2 NOISE IN VERTICAL BIPOLAR TRANSISTORS

The common bipolar transistor contains sources of thermal noise, 1/f-noise and shot-noise. In this section a noise model for the forward active bipolar junction transistor (BJT) is derived. Fig. 3.5 is a wafer cross-section through an npn-transistor available in the AMS 0.8μm BiCMOS process (not to scale) [45]. Indicated on the figure is also the base spreading resistance $r_{bb}$ between the base contacts and the emitter. This physical resistance gives rise to a thermal noise component. In most cases the base-spreading resistance is dominant over all other resistances in the transistor due to the light doping of the base area and its narrow cross section. Therefore, other resistances such as between base and collector are often ignored or lumped into the base resistance.

![Fig. 3.5: Wafer cross section through the npn-BJT with equivalent base spreading resistance $r_{bb}$ [45].](image)

The currents crossing the $pn$-junctions base-emitter and base-collector each give rise to shot-noise. The collector current is composed of the same charge carriers that constitute the emitter current. The currents are 100% correlated so that the total shot-noise powers add arithmetically and the equivalent noise generator in series with the collector terminal is given by

$$P_{S,BJT} = 2q(I_c + I_e) = 4qI_c$$

(3.12)
The portion of the shot-noise generated at the base-emitter junction is often referred to the base terminal, where it is represented by a noise source $2qI_E/\beta=2qI_B$ in series with the base, where $\beta$ is the forward current gain and $I_E$ and $I_B$ are the emitter and base current respectively.

Finally, the BJT also exhibits \textit{flicker}-noise, although this noise component is small (several orders of magnitude smaller than in MOS transistors [44]) due to conduction taking place deep within the structure (i.e. there is no oxide with high trap density near the current path). Elaborate studies are available, which trace the location of the noise sources within the transistor and study their physical origin [53, 62-64]. Many physical effects contribute to $1/f$-noise, but to simplify calculation and extraction of noise parameters a simplified empirical noise model is most commonly used. The model describes the \textit{flicker}-noise power as being proportional to the base current [65]:

$$P_{1/f-BJT} = \frac{K_B \cdot I_B^{AF}}{f} \Delta f$$  \hspace{1cm} (3.13)

with exponent $AF$ usually ranging between 1 and 2 [62]. Note that the flicker-noise power is proportional to the emitter area, but $K_B$ is a fixed value quoted for a given unity transistor. Hence, an increase in transistor area may be modelled by parallel connections of unity transistors.

In the noise-analysis of circuits it is often useful to refer all the noise sources back to the input terminal of the transistor, where it can be represented as an equivalent voltage source. Fig. 3.8 shows the input referred noise model for a load $R_S$ connected to the base, with noise contributions from $R_S$ not included [43].
3.2.3 NOISE IN LATERAL BIPOLAR TRANSISTORS

Although vertical BJTs are optimised devices, the advantage of lateral bipolar transistors is that they can be fabricated in a BiCMOS as well as CMOS process. Any MOS transistor can be operated in a lateral bipolar mode by reverse-biasing its gate [66]. By virtue of reverse bias it is ensured that no conducting channel is present between drain and source. Instead, drain and source are used as emitter and collector of the lateral BJT, while the conversely doped material previously forming the MOS channel region is used as the base (Fig. 3.6). In order to form isolated devices in a bulk process, the well is used as the base. Consequently, in an n-well process only pnp-lateral transistors are available as isolated devices and vice versa in a p-well process. Several problems arise from the horizontal structure, which are briefly discussed as they affect the noise performance. Firstly, not only the desired lateral pnp-transistor is formed, but also a parasitic vertical transistor between substrate, well and emitter. The emitter current is partially collected by the parasitic substrate collector and reduces the current gain of the lateral device. If a buried layer is available, it can be connected to the base, which establishes a conductive layer to decrease the flow of current towards the parasitic collector [66]. To increase the efficiency of the collector, a

![Fig. 3.6: Schematic cross section through a reverse-biased n-well MOS with the schematic symbol to illustrate the location of the lateral BJT.](image-url)
layout is used for the collector, in which the collector surrounds the emitter as shown in Fig 3.7.

The second disadvantage of the lateral transistor is, that the base region is wide compared to its vertical counterpart. In a self-aligning process the base is formed by the portion of well covered with gate-polysilicon. Therefore, the minimum base width is limited by the maximum definition of the polysilicon layer, typically in the micrometer range.

Finally, the doping levels are not optimised for bipolar operation, resulting in lower efficiency compared with the vertical BJT. It can be concluded that in terms of noise, a lateral BJT biased with the same collector current as a comparable vertical device performs worse. Degradation of noise performance is expected mainly due to three factors:

1. Gate polysilicon with associated charge traps is present over the active base region, giving rise to flicker-noise. However, the effect is smaller than in MOS devices, because conduction takes place at a depth within the well.

2. The effective forward current gain $\beta$ is smaller for the lateral device, so that for any given lateral collector current a higher base current results. This increases the flicker-noise according to relation (3.13).

3. The noise floor increases for a lateral device compared to the vertical transistor biased with the same emitter current, as the ratio of lateral collector current to emitter current $\alpha_{P,\text{effective}}$ is reduced to around 60% [66] due to the effects discussed. Hence, for a given lateral collector current, the shot noise of equation (3.12) increases by approximately $\sqrt{2}$.
\[
\overline{P_{sat}} = 2q(I_C + I_E) = 2qI_C + \frac{I_C}{\alpha_{F_{\text{effective}}}} = 5.3 \cdot qI_C \tag{3.14}
\]

3.2.4 NOISE IN MOS TRANSISTORS

Noise sources in MOS transistors include thermal-noise and flicker-noise. The resistive channel produces thermal noise, which is most conveniently expressed as a current noise source \( \overline{i_{th}} \) in series with the drain. Noise source \( \overline{i_{th}} \) is given by

\[
\overline{i_{th}} = \varepsilon 4kTg_{mn}
\tag{3.15}
\]

in analogy with Eqn. (3.1). Parameter \( \varepsilon \) is bias dependent and varies between the extremes given in Table 3.1, depending on the level of saturation and inversion [67-68]. For typical values of slope factor \( n \) of around 1.2, \( \varepsilon \) is approximately equal in weak and strong inversion. In the following sections on noise analysis, no distinction is therefore made between \( \varepsilon \) in weak and strong inversion. Note that in strong-inversion linear-operation transconductance parameter \( g_{mn} \) denotes channel...
transconductance $\delta I_d/\delta V_{ds}$, whereas under all other bias conditions $g_{mn}$ represents gate transconductance $\delta I_d/\delta V_{gs}$. The gate-referred voltage noise source shown in Fig. 3.8 is found under all bias conditions by dividing the r.m.s. current noise through the gate transconductance.

Flicker-noise in MOS has undergone extensive study [49, 58, 62, 69-70], suggesting that its origin is associated with the density of charge traps in the gate oxide. However, for analogue design, the empirical expression (3.10) is modified to describe the $1/f$-noise as a voltage noise power source at the gate:

$$
\frac{v_{1/f}^2}{v_{1/f}^2} = \frac{K_F}{C_{ox}W L f^{AF}}
$$

(3.16)

where $C_{ox}$ is the capacitance across the oxide layer between gate and channel. Exponent $AF$ is near unity and therefore not explicitly considered in the noise models of Fig. 3.8. Note that coefficient $K_F$ is bias dependent and different values apply for weak and strong inversion. However, $K_F$ is independent of drain-source voltage to a first approximation, so that it applies to the linear as well as saturated region [69]. Flicker-noise is smaller in a p-MOS transistor compared to the n-MOS, which is reflected in the value for $K_F$ (Table 3.2).

<table>
<thead>
<tr>
<th>Condition</th>
<th>strong inversion</th>
<th>weak inversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>saturation</td>
<td>2/3</td>
<td>$n/2$</td>
</tr>
<tr>
<td>ohmic</td>
<td>1</td>
<td>$n$</td>
</tr>
</tbody>
</table>

Table 3.1: Corner values for factor $\varepsilon$, where $n$ is the weak-inversion slope factor.
\[
\frac{v_n^2}{\Delta f} = 4kTR + \frac{K_S}{WLF_n}
\]

\[
\frac{v_n^2}{\Delta f} = \frac{e4kTg_m}{g_m^2} + \frac{KF_{si,wi}}{WLC_{ox}f}
\]

\[
\frac{v_n^2}{\Delta f} = 4kTb + \left(2qI_B + \frac{K_BI_B}{f}(R_s + R_i)^2 \right)
\]

\(R_S\) is the load resistance applied to the base.

**Figure 3.8:** Simplified input-referred low-frequency noise models.

<table>
<thead>
<tr>
<th>Bipolar Transistor:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>(R_b)</td>
</tr>
<tr>
<td>(I_0)</td>
</tr>
<tr>
<td>(\alpha_F)</td>
</tr>
<tr>
<td>(\beta_F)</td>
</tr>
<tr>
<td>(K_B)</td>
</tr>
<tr>
<td>(AF)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MOS Transistor:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>(K_{F_{si}})</td>
</tr>
<tr>
<td>(K_{F_{wi}})</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Polysilicon Resistor:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>(K_R)</td>
</tr>
</tbody>
</table>

*Table 3.2: Typical core parameters for noise modelling (from [65, 66] and own measurements).*
3.3 CONCLUSIONS

The relevant noise sources present in solid-state devices were discussed. From the physical causes for thermal, shot and flicker-noise, noise models for hand calculation are derived. For practical circuit analysis noise models for transistors and polysilicon resistor are presented, which express the noise in these components as equivalent noise sources connected to an otherwise noiseless device.

1/f-noise is high in MOS devices compared to bipolar transistors. Lateral BJTs are generally less efficient than their vertical counterparts which results in higher input referred noise. Flicker-noise in polysilicon resistors may be significant in some applications and is not included in models used as standard for CAD circuit simulators.
CHAPTER 4
PREAMPLIFIERS

4.1 DESIGN OF A LOW-NOISE PREAMPLIFIER

As shown in Chapter 2 the amplitude of the ENG signal recorded using tripodes depends to some extent on the dimensions of the nerve cuff but is typically on the order of $1\mu V$ r.m.s. with a broad, flat power spectral density centred at about 1-2kHz. Amplifiers contribute white noise and additionally, especially in the case of MOS-based circuits, flicker noise ($1/f$), which, because of its spectrum, can be harmful in a low frequency application such as this [65]. Each preamplifier is designed to provide optimum performance in terms of noise and power consumption and to have sufficient voltage gain so that noise is not an issue in the design of the subsequent stages. A nominal value of 100 was chosen as being adequate in this respect, but this is not by any means a critical parameter. Furthermore, if a feedback EMG cancellation system is applied, any residual differential gain errors between the channels are reduced. In addition, since a multi-electrode system requires arrays of 10 or more preamplifiers, circuit area is a significant design issue.

4.1.1 NOISE REDUCTION TECHNIQUES

Different approaches have been described to improve the performance of low-noise amplifiers. Noise reduction based on physical effects (bias switching), chopper- and autozero technique are reviewed in this section. All these techniques aim at the reduction of $1/f$-noise but do not improve on the white noise. These
techniques require clock generation circuitry and suffer from potential problems associated with high-frequency interference and clock-feedthrough. In addition, high switching circuits increase the power consumption of the design and increase its complexity. Low-noise design techniques as described in the following sections therefore remain a highly important prerequisite even when applying active reduction techniques.

4.1.1.1 Bias Switching

This technique aims at reducing the $1/f$-noise of a MOS transistor by cyclically increasing and decreasing its gate bias so that the device alternates between inversion and accumulation (Fig. 4.1). The transistor noise is modulated by the switching wave where the switching operation can be represented as a multiplication of the noise current with the switching signal $m(t)$. Using a square wave with 50% duty cycle as switching signal, $m(t)$ is approximated by its Fourier representation:

$$m(t) = \frac{1}{2} + \frac{2}{\pi} \sin(\omega_{sw} t) + \frac{2}{3\pi} \sin(3\omega_{sw} t) + \frac{2}{5\pi} \sin(5\omega_{sw} t) + \cdots \quad (4.1)$$

If the switching frequency $\omega_{sw}$ is chosen sufficiently high, the baseband noise reduces by half and any modulation effects represented by the sine terms in (4.1) remain outside the bandwidth of interest and can be removed by filtering. Note also that the baseband signal of interest is modulated so that the SNR remains unchanged. However, the reduction of $1/f$-noise achieved by switching is reported to be in excess of the effect expected from modulation theory [71]. It is instead explained by physical mechanisms, mainly a reduction in the time between carrier trapping and release due to cycling [72]. The maximum SNR improvement thus achieved is around 30% [71]. Hence, bias switching may improve noise performance at low frequencies, but requires a high speed clock.
applied to the gate or bulk of the transistor with potential problems due to charge feedthrough and additional noise originating from the driver circuit. Applying the clock to the backgate further introduces distortion due to the bulk-effect. Bias-switching therefore appears impractical in the targeted low-noise front-end.

![Fig. 4.1: Cycling of MOS gate bias (left) and application to an OTA.](image)

### 4.1.1.2 Chopper Technique

The chopper technique is also an approach based on signal modulation. Before amplification the amplifier input signal is modulated by a wave of frequency $\omega_{sw}$ much higher than the baseband frequencies of interest. The up-converted signal is then amplified and bandpass filtered. The modulated signal spectrum is located at frequencies higher than the $1/f$-noise corner, so that the amplifier noise floor alone determines the SNR. After amplification the signal is converted back to the baseband by multiplication with the same modulation waveform used for up-conversion [73]. Finally, low-pass filtering restores the desired signal. A block diagram of the chopper-amplifier is given in Fig. 4.2.
Although this technique reduces 1/f-noise and output offset voltages (DC), the noise performance is ultimately limited by the noise floor of the amplifier. Furthermore, non-idealities lead to signal distortion. Such non-idealities include the amplifier bandwidth, which must be at least twice the modulation frequency to satisfy the Nyquist criterion.

4.1.1.3 Autozeroing

The principle of the autozero technique is illustrated in Fig. 4.3. During sampling phase $\phi_1$, the amplifier is configured as a unity gain buffer and the input noise is sampled. During the amplification phase $\phi_2$, the noise sample is subtracted from the instantaneous amplifier input noise. As the sampling frequency is chosen higher than the 1/f-noise frequency the sample is highly correlated to the instantaneous noise, so that the low-frequency noise cancels. A detailed analysis of the autozero amplifier is complex and can be found in [74]. A major drawback of the autozero technique is that high frequency white noise is undersampled and folded back into the baseband where it increases the noise floor. In a continuous-time, low-noise system such as the ENG amplifier the continuous-time chopper technique seems better suited than autozeroing involving sample and hold.
However, in this thesis the simpler approach of low-noise design was adopted as described in the subsequent sections.

![Block diagram of autozero amplifier.](image)

**Fig. 4.3: Block diagram of autozero amplifier.**

### 4.1.2 PREAMPLIFIER SPECIFICATION

Although many integrated circuit amplifiers have been proposed for use with bioelectric signals [13-15, 75-80], existing circuits often exhibit excessive power consumption and, in particular, cannot meet the noise specification required for MEC nerve cuff recordings. Given the very small signal levels, a value of 300nV for the input-referred r.m.s. noise voltage in a bandwidth 1Hz-10kHz has initially been chosen to satisfy the specification drawn in Table 2.4.

This Section describes the design and evaluation of the preamplifiers. An outline specification is given in Table 4.1 in comparison with the specifications of the AMP01 instrumentation amplifier [81], which has been used frequently in biomedical recording experiments in the past. A comparison between three candidate designs is presented; two designs use MOS input stages and one has bipolar inputs. The thesis seeks to establish that in this application an optimum arrangement in terms of noise performance, size and power consumption employs bipolar input transistors. Although it has been suggested that MOS input stages operating in weak inversion can be used to advantage in this type of application [76], the comparison example presented shows that this can only be achieved at
the cost of increased power consumption and an unacceptably large increase in die area.

Note that although the preamplifier to be discussed in this thesis was designed for use in conjunction with a *true-tripolar* cuff or MEC, it can be seen as a generic very low noise interface to any configuration of *nerve cuff* electrodes.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Amp01 [81]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>±2.5 V</td>
<td>4.5 V min.</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt;2 mW</td>
<td>&gt;13.5mW</td>
</tr>
<tr>
<td>Circuit area</td>
<td>as small as possible</td>
<td>10.6 mm²</td>
</tr>
<tr>
<td>Gain</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>–3 dB frequency</td>
<td>15 kHz</td>
<td>≈50 kHz</td>
</tr>
<tr>
<td>CMRR @ 1KHz</td>
<td>100 dB</td>
<td>100 dB</td>
</tr>
<tr>
<td>PSRR @ 1KHz</td>
<td>&gt;40 dB</td>
<td>85 dB</td>
</tr>
<tr>
<td></td>
<td>&gt;40 dB</td>
<td>100 dB</td>
</tr>
<tr>
<td>Total input-referred voltage noise density @ 1Hz</td>
<td>&lt;20 nV/√Hz</td>
<td>30 nV/√Hz</td>
</tr>
<tr>
<td></td>
<td>&lt;4 nV/√Hz</td>
<td>10 nV/√Hz</td>
</tr>
<tr>
<td>Total input-referred current noise density @ 1Hz</td>
<td>&lt;20 pA/√Hz</td>
<td>≈0.3 pA/√Hz</td>
</tr>
<tr>
<td></td>
<td>&lt;2 pA/√Hz</td>
<td>0.3 pA/√Hz</td>
</tr>
<tr>
<td>Total input-referred r.m.s. voltage noise 1Hz-10KHz</td>
<td>300 nV</td>
<td>1000 nV</td>
</tr>
<tr>
<td>Residual input DC base current</td>
<td>as small as possible</td>
<td>2 nA</td>
</tr>
</tbody>
</table>

*Table 4.1: Preamplifier Specification*

**4.1.3 DESIGN CONSIDERATIONS**

In this application both very low noise and low power consumption are critical. In addition, since it is intended to use an array of preamplifiers in a MEC system, area is also significant, although no exact specification is given here. Bearing these factors in mind, a single-stage feedforward architecture was chosen. This was possible since the preamplifiers are AC coupled to the subsequent stages and so DC offsets occurring at the preamplifier outputs are not significant. In
addition, the *absolute* gain of each preamplifier is not critical for ENG recording [82] and the differential gains between the channels are likely to be small (e.g., the ratio of two polysilicon resistors on the same die is specified to +/-1% in the chosen process [45]).

The basic arrangement is shown in Fig. 4.4 and consists of an operational transconductance amplifier (OTA) terminated in a load resistor ($R_1$), a low-pass filter ($R_2$ and $C$) and an output buffer for testing purposes. Interference, especially at high frequencies, may couple into adjacent tracks and lead to oscillations due to parasitic feedback. Therefore, the combination of $R_2$ and $C$ is chosen to restrict the bandwidth to 15kHz to remove any such interfering signals. The candidate OTA circuits shown in Fig. 4.5 are conventional, consisting of a differential pair transconductance stage terminated in a current mirror.

---

*Fig. 4.4: Basic preamplifier architecture.*

---

*Fig. 4.5: Candidate OTA circuits.*
Three possible OTA architectures were considered: MOS transistors throughout, consisting of a p-MOS differential stage and n-MOS mirror using (a) weak inversion, (b) strong inversion and, finally, (c) a BiCMOS approach using npn bipolar transistors in the differential pair with p-MOS transistors in strong inversion for the current mirror. The input-referred noise was evaluated and simulated in each of these types of OTA. For the bipolar case, the input-referred current noise was taken into account by passing it through a noiseless 1kΩ resistance (representing the approximate ohmic resistance of the cuff electrodes in the relevant frequency band but noiseless to avoid including any source noise).

In addition to the OTA stages, the final BiCMOS preamplifier contains circuitry to cancel the base currents of the input transistors. Although primarily intended for AC coupling to the nerve tissue, a future application requires DC coupling and additional in-vitro experiments are needed to assess the optimum method to deal with any residual input currents.

4.1.3.1 Basis of Comparison

Since the maximum permitted DC dissipation is 2mW with ±2.5V power supplies, the maximum tail current ($I_S$) for the OTA is limited to 400μA. This immediately sets upper bounds on the transconductance gain ($g_m$) for the BiCMOS and weak inversion CMOS versions of the OTA of 15mA/V and 10mA/V, respectively (the transconductance gain for CMOS in strong inversion is a function of the device aspect ratio, W/L, in addition to the tail current). Also, since the nominal voltage gain is required to be 100, knowledge of $g_m$ fixes the value of the load resistor, $R_l$. Since the amplifier noise depends on $I_S$ (all cases) and $W/L$ (CMOS versions), knowledge of the maximum power dissipation, supply voltages, nominal voltage gain and target input-referred r.m.s. amplifier voltage noise sets the framework for the comparison discussed below.
4.1.3.2 Input-Referred Voltage Noise
The input-referred voltage noise of CMOS OTAs, first discussed by Bertails in 1979 [83], is dominated by flicker \((1/f)\) noise at low frequencies and thermal/shot noise at higher frequencies. By using the noise models given in Fig. 3.8 (Chapter 3), where the noise of each transistor is represented by a voltage source at its input, the total input-referred noise contribution can be calculated by considering the voltage gains from the device to the amplifier output. For the symmetrical OTA topology shown in Fig. 4.6, the input referred noise voltage is given for both, MOS and bipolar input, by

\[
\overline{V^2} = 2\overline{V^2_{n_{in}}} + 2\left(\frac{g_{m_m}}{g_{m_{in}}}\right)^2 \overline{V^2_{n_{m-m}}} \tag{4.2}
\]

where the subscripts ‘in’ and ‘m’ denote the input and mirror transistors, respectively. Note that the expression is independent of the output impedance of the OTA. Noise associated with tail current \(I_{tail}\) is small compared to the tail current and can be ignored for \(I_{tail}\) larger than a few microampere.
For both strong and weak inversion MOS transistors the input-referred flicker noise voltage model is given by Eqn. (3.16). Hence the total input-referred flicker noise power spectral density (PSD) for the weak inversion CMOS OTA is:

$$\frac{\overline{v^2_f}}{\Delta f} = \frac{2}{C_{ox} f} \left( \frac{K_{F_{in}}}{W_{in} L_{in}} + \frac{K_{F_{m}}}{W_{m} L_{m}} \right) \left( V^2/Hz \right)$$

(4.3)

and for the strong inversion CMOS OTA is:

$$\frac{\overline{v^2_f}}{\Delta f} = \frac{2}{C_{ox} f} \left( \frac{K_{F_{in}}}{W_{in} L_{in}} + \frac{K_{P_m} K_{F_{m}} L_{in}^2}{K_{P_m} W_{in}^2 L_{m}^2} \right) \left( V^2/Hz \right)$$

(4.4)

where $K_P$ is the transconductance parameter. In the case where the input MOS transistors are in strong inversion, but the mirror transistors are in weak inversion, the input-referred flicker noise PSD is:

$$\frac{\overline{v^2_f}}{\Delta f} = \frac{2}{C_{ox} f} \left( \frac{K_{F_{in}}}{W_{in} L_{in}} + \frac{K_{P_m} L_{in}}{2U_{th}^2 K_{P_m} W_{in}} \right) \left( V^2/Hz \right)$$

(4.5)

where $I_D$ is the drain current and $U_{th}$ is the thermal voltage. Equation (4.5) is similar to (4.3) but contains another factor, which modifies the mirror noise contribution. In order to determine, which bias condition results in the better noise performance, the definition of the weak- to strong inversion boundary has to be taken into account. With a 'safety-factor' $\alpha$ (around 8 to 10) to ensure a minimum distance from the idealized transition point, the boundary is given by [84]:

$$I_D \geq \alpha \frac{W_{in}}{L_{in}} K_{P_{in}} \cdot 2U_{th}^2; \quad \alpha >> 1$$

(4.6)

Assuming that the mixed inversion design described by Eqn. (4.5) is better, the additional factor must be smaller than unity, i.e.
\[
\frac{I_D L_{in}}{2U_{th} K P_{in} W_{in}} < 1 \tag{4.7}
\]

Solving (4.6) and (4.7) for \( \frac{W_{in}}{L_{in}} \) and combining yields

\[
\frac{W_{in}}{L_{in}} > \frac{I_D}{2U_{th}^2 K P_{in}} \geq \frac{\alpha I_D}{2U_{th}^2 K P_{in}} \tag{4.8}
\]

which is only true for \( \alpha \) smaller or equal to unity and contradicts the requirement of \( \alpha \) being large and positive. Thus, it can be concluded that the all weak inversion case is superior in terms of flicker noise performance. Similarly, in the case where the input transistors are in weak inversion, but the mirror transistors are in strong inversion, the input-referred flicker noise PSD is:

\[
\frac{\nu^2}{V f} = \frac{2}{C_{ox} f} \left( \frac{K F_{in}}{W_{in} L_{in}} + \frac{2K F_{m} K P_{m} U_{th}^2}{I_D L_{in}^2} \right) \left( V^2 / Hz \right) \tag{4.9}
\]

Again, the factor needed to transform (4.9) into (4.4) is never smaller than unity, resulting in an equal or higher flicker noise performance compared to the all-strong inversion case.

From Fig. 3.8, the input-referred flicker noise voltage model for bipolar transistors is

\[
\nu_f^2 = \left( r_b + r_s \right)^2 \frac{I_C K F}{\beta f} \Delta f \tag{4.10}
\]

where \( I_C \) is the collector current, \( \beta \) is the forward current gain, \( r_b \) is the base spreading resistance and \( r_s \) is the source (cuff) resistance. Using this model, the input-referred flicker noise PSD for the BiCMOS OTA is:

\[
\frac{\nu_f^2}{V f} = \frac{2}{f} \left( K F_{in} \frac{I_C}{\beta} (r_b + r_s)^2 + \frac{2K P_{m} K F_{m} U_{th}^2}{I_C L_{in}^2 C_{ox}} \right) \left( V^2 / Hz \right) \tag{4.11}
\]
At higher frequencies the input-referred noise voltage floor is dominated by white (thermal/shot noise). Using the input-referred MOS thermal voltage noise model for weak and strong inversion (3.15), the input-referred thermal noise PSD for the weak inversion CMOS OTA is:

\[
\frac{\nu_{th}^2}{\Delta f} = \frac{16}{3} \frac{2kT}{g_m(in)} \left( \text{V}^2/\text{Hz} \right)
\]  \hspace{1cm} (4.12)

and for the strong inversion CMOS OTA is:

\[
\frac{\nu_{th}^2}{\Delta f} = \frac{16}{3} kT \left( \frac{1}{g_m(in)} + \frac{g_m(m)}{g_m^2(in)} \right) \left( \text{V}^2/\text{Hz} \right)
\]  \hspace{1cm} (4.13)

The input-referred shot/thermal noise PSD for the BiCMOS OTA is:

\[
\frac{\nu_{s,th}^2}{\Delta f} = 4kT \left( 2r_b + \frac{g_m(in)}{\beta} (r_b + R_s)^2 + \frac{4 g_m(m)}{3 g_m^2(in)} \right) \left( \text{V}^2/\text{Hz} \right)
\]  \hspace{1cm} (4.14)

From these equations, straightforward procedures to minimize both the noise floor and the 1/f noise can be deduced and are summarized in Table 4.2. Notice that for the CMOS OTAs the noise floor is approximately inversely proportional to \(g_m\) whereas in the BiCMOS case the link with \(g_m\) is less direct, and contributions due to \(r_b\) and \(R_s\) can be significant. On the other hand, the 1/f components are dominated by the device geometries in all cases. Considering all these factors, the transistor dimensions shown in Table 4.3 were chosen.

<table>
<thead>
<tr>
<th>OTA circuit</th>
<th>Minimize noise floor</th>
<th>Minimize 1/f noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS weak inversion</td>
<td>Strong function of 1/g_m</td>
<td>maximize all transistor areas</td>
</tr>
<tr>
<td>CMOS strong inversion</td>
<td>Strong function of 1/g_m</td>
<td>maximize input transistor (W) maximize mirror transistor (L)</td>
</tr>
<tr>
<td>BiCMOS</td>
<td>reduce (r_b), also depends on (g_m)</td>
<td>maximize mirror transistor (L)</td>
</tr>
</tbody>
</table>

Table 4.2: Procedure for voltage noise reduction (constant \(g_m\)).
Finally, note that for weak inversion CMOS operation, the following inequality should be satisfied [84]:

$$\alpha L \leq \frac{W}{L} K P \cdot 2 U_{th}^2$$  \hspace{1cm} (4.15)

with large and positive 'safety factor' $\alpha$, which places a further constraint on the permissible values of $W$ and $L$.

### 4.1.4 SIMULATED RESULTS

In order to examine the noise performance of each configuration, a model of each OTA was simulated using the CADENCE design tools and the AMS 0.8µm BiCMOS (double metal, double poly) process parameters [45]. Using the principles outlined in Table 4.2, the tail currents, MOS aspect ratios and load resistors ($R_l$) were adjusted to meet the specified values of gain, power consumption and input referred r.m.s. noise specified in Table 4.1. The input-referred voltage noise PSDs are plotted in Fig. 4.7, together with the r.m.s. noise integrated across the bandwidth 1Hz-10KHz. All three designs meet the power/noise specifications, although the BiCMOS design achieves this with a DC dissipation of 1mW compared to 2mW for the CMOS designs.
The noise floors are quite similar for all designs, the BiCMOS having the lowest value at about 2.6nV/√Hz. This result is also found by equating the terms of Fig. 3.8 describing the noise floor of the MOS-FET and BJT. The BiCMOS case also has the best 1/f noise performance, followed by the strong inversion CMOS OTA. However, as Table 4.3 shows, in order to obtain this performance from the CMOS OTAs, the transistor dimensions must be made impractically large. This should be set against the extra cost of using a BiCMOS process. However, it was felt that the choice presented showed a reasonable compromise solution to the requirements of a preamplifier for an implantable neuroprosthetics system where nerve cuffs are used. The specified values of Common mode rejection ratio (CMRR) and Power supply rejection ratio (PSRR), measured at a spot frequency of 1kHz were achieved in all cases.

**Fig. 4.7: Simulated input-referred voltage noise densities of candidate OTAs.**
4.1.5 MEASURED RESULTS

The complete circuit schematic of the fabricated BiCMOS preamplifier is shown in Fig. 4.8 and Fig. 4.9 is a microphotograph of the chip (which includes two amplifiers). In addition to the components already discussed, circuitry was included to cancel the base currents of $Q_1$ and $Q_2$. This is important, as significant current flowing into the tissue cannot be permitted. The transistor $Q_8$ generates a replica of the base currents of $Q_1$ and $Q_2$, which is fed into the $pMOS$ current mirror $M_4$, $M_5$, $M_6$. The common base transistor $Q_9$ level shifts the current from $Q_8$ and ensures that its DC conditions match those of $Q_1$ and $Q_2$ as far as possible. The $pMOS$ mirror transistors $M_6$ and $M_5$ feed the bases of $Q_1$ and $Q_2$ respectively. The $nMOS$ source follower $M_3$ was included to enable the output to be measured off-chip. In a complete ENG amplifier where the output is AC coupled to the next (MOS) stage, this buffer would not be necessary.

Note that the base of $Q_9$ is connected to ground potential (i.e. half-way between the supplies) and that the inputs are also referenced to this level. In an implanted system, this ground potential would be defined by connection to an indifferent electrode.

A comparison between the simulated and measured voltage noise performance of the preamplifier is shown in Fig. 4.10. The measured results are summarised in Table 4.4 and these generally show good agreement with the simulation and the specification. The residual input DC base current could be further reduced by the use of longer transistors and/or cascoding for the DC sources ($M_4$-$M_6$, etc.).
Approximate transistor dimensions in µm (For BJT: emitter area in µm²).

Fig. 4.8: Final preamplifier schematic.

Fig. 4.9: Chip microphotograph.

Fig. 4.10: Comparison between simulated and measured voltage noise performance.
### Table 4.4: Measured Results.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>±2.5 V</td>
<td>±2.5V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt;2 mW</td>
<td>1.3 mW</td>
</tr>
<tr>
<td>Circuit area</td>
<td>0.3 mm²</td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>100</td>
<td>110</td>
</tr>
<tr>
<td>-3 dB frequency</td>
<td>15 kHz</td>
<td>14 kHz</td>
</tr>
<tr>
<td>CMRR @ 1KHz</td>
<td>100 dB</td>
<td>82 dB</td>
</tr>
<tr>
<td></td>
<td>(V_{DD}) &gt;40 dB</td>
<td>42 dB</td>
</tr>
<tr>
<td></td>
<td>(V_{SS}) &gt;40 dB</td>
<td>54 dB</td>
</tr>
<tr>
<td>Total input-referred voltage noise density @ 1Hz</td>
<td>&lt;20 nV/√Hz</td>
<td>11.5 nV/√Hz</td>
</tr>
<tr>
<td></td>
<td>&lt;4 nV/√Hz</td>
<td>3.3 nV/√Hz</td>
</tr>
<tr>
<td>Total input-referred current noise density @ 1Hz</td>
<td>&lt;20 pA/√Hz</td>
<td>17 pA/√Hz</td>
</tr>
<tr>
<td></td>
<td>&lt;2 pA/√Hz</td>
<td>1.5 pA/√Hz</td>
</tr>
<tr>
<td>Total input-referred r.m.s. voltage noise 1Hz-10KHz</td>
<td>300nV</td>
<td>290nV</td>
</tr>
<tr>
<td>Residual input DC base current</td>
<td>100 nA</td>
<td>120 nA</td>
</tr>
</tbody>
</table>

4.1.6 PRACTICAL CONSIDERATIONS ON LATERAL BJT

It is felt that the advantages of bipolar input transistors compared to MOS are very striking and fully justify the use of either the more expensive BiCMOS process in this application or the use of lateral devices in a CMOS process at the cost of increased power consumption. The white noise current spectral density in the channel of MOS and bipolar transistor (BJT) can be approximated by Eqn. (3.15). The noise current in the channels of the input transistors feeds into the load resistor and produces an output voltage noise density of

\[
\bar{v}_{\text{n-out}} = \varepsilon A \sqrt{\frac{8kT}{g_m}}
\]

(4.16)
where $A$ is the voltage gain of the amplifier. Since transconductance $g_m$ is typically larger in a vertical BJT compared to the lateral counterpart biased with the same current the noise performance of the vertical design is superior. Unfortunately, the ideal choice of an optimized BiCMOS process is more expensive than a pure CMOS realization. Although a more cost effective MOS process does not provide dedicated (vertical) BJTs, it has been suggested that lateral bipolar transistors can be used in low frequency applications with no significant loss in circuit performance [66, 85]. Assuming 50% efficiency, a tail current of $260\mu A$ is required to achieve less than $30\mu V$ output noise according to Eqn. (4.16). A current of this order is still within the given power budget, so that lateral devices can be used in this application to minimise chip cost. Since only $pnp$-transistors are available in the chosen process, $n$-mos mirrors are used so that the circuit schematic modifies to that given in Fig. 4.11. The efficiency relates to the gain that is achieved for a given bias current and therefore has an immediate effect on the input-referred noise. A wide variation of the efficiency between different processes is found, which has a dominant effect on the input-referred noise. A comparison of noise performances is given in Fig. 4.12 for amplifiers designed with a target gain of 100. The figure shows that the noise floor in the bandwidth of interest above 200Hz is nearly identical for both, the design using vertical BJTs and the design employing lateral input BJTs, manufactured in the same BiCMOS process. The measured results agree well with the simulation as shown for the vertical design in Fig. 4.10 and the lateral design in Fig. 4.12. However, the noise measured for the same topology using lateral transistors realised in a CMOS process is much higher, by about a factor of two. This is explained by lower efficiency of the device in the CMOS process due to the
absence of a buried layer. This also agrees with the lower gain measured (also a factor of two, Fig. 4.13). It can be concluded that the amplifier output noise is similar for all three implementations (vertical BJT, lateral BJT in a BiCMOS and in a CMOS process). However, this causes the input-referred noise to be higher in the pure CMOS process as the gain achieved with a given bias current is lower. Note that the simulation does not predict the measured differences. To effectively use the lateral approach in a CMOS process it appears essential to choose a manufacturing process which provides efficient devices, i.e. includes a buried layer and/or allows shorter base lengths. Under these conditions a performance can be achieved, which is comparable with a BiCMOS implementation. The area of the amplifier is in any case comparable to an implementation using vertical transistors as a comparison with Table 4.4 shows.

**Fig. 4.11: Preamplifier schematic with lateral pnp-transistors.**
Fig. 4.12: Comparison of amplifier noise performance using different manufacturing processes.

Fig. 4.13: Comparison of lateral amplifier gain in CMOS and BiCMOS process.
4.1.7 LATERAL PREAMPLIFIER DESIGN

In a complete recording channel the preamplifiers are followed by further high-gain stages with a total voltage amplification of at least 10,000. Therefore, output offset voltages are harmful as they are amplified and significantly reduce the output dynamic range of the system [86]. Previously reported biopotential amplifiers remove offsets with active filters [77, 86-88]. However, most of these rely on external components and are not suitable for integration. Furthermore, active circuitry increases power consumption and noise, and does not guarantee complete offset removal. Therefore, in Section 4.1.9 the design of a passive filter is discussed which, although it uses MOS transistors, does not increase the noise in the recording channel, i.e. has a unity noise factor, consumes no DC power and is fully integratable. Simulated results reported in Section 4.1.10 confirm the expected performance.

4.1.8 HIGH-PASS FILTER

Since absolute amplifier gain and linearity are not critical in biopotential recording [82], the feedforward architecture discussed in the previous sections is suitable and readily interfaces to a high-pass filter as shown in Fig. 4.13.

![Fig. 4.14: Preamplifier architecture.](image)

Resistor $R_2$ and the capacitor define the high-frequency cut-off around 35kHz, which is slightly higher than in the design of Fig. 4.8 to reduce the area consumed by $R_2$ and $C$. The cut-off frequency is lowered to the specified bandwidth by subsequent amplifiers in the system. The high-pass filter in addition
to removing the low frequency noise tail also eliminates DC offsets, which is important as the amplifier is followed by further gain stages. Ideally, the filter eliminates low frequencies below the ENG pass-band without increasing the noise in the recording channel. This is achieved as long as the filter noise power does not exceed the preamplifier low-frequency noise power. In this case, the total noise remains unchanged. As shown in the following analysis, a first-order RC filter (Fig. 4.15) provides the required performance and can be realized with minimum component count and no static power dissipation. This stage is added in cascade with the lowpass filter at the output of the preamplifier. Since the cutoff frequencies of the two sections are very different (300Hz, 35kHz), there is negligible interaction between them. The resulting filter noise power density \( P_{n_{filter}} \) at frequency \( f \) can therefore be approximated as follows:

\[
P_{n_{filter}} \approx \frac{4kTR_3}{\left(f/f_c\right)^2 + 1}
\]  

(4.17)

where \( f_c \) is the filter cut-off frequency given by

\[
f_c = \frac{1}{2\pi R_3 C}
\]  

(4.18)

Integration of (4.17) yields the total filter noise power below frequency \( f_p \):

Fig. 4.15: High-pass RC-filter connected to preamplifier output.
Fig 4.16. Active $8.2\,\text{M}\Omega$ resistor with improved linearity.

\[ \overline{P_{n_{\text{total}}}} \equiv \frac{4kT}{2\pi C} \arctan\left(\frac{f_p}{f_c}\right) \]  

(4.19)

Simulation of the preamplifier predicts that the total rms noise power below the cut-off frequency $f_c=300\,\text{Hz}$ is around 50pV^2 (Fig. 4.16). Choosing a matching filter noise contribution $\overline{P_{n_{\text{total}}}} = 50\,\text{pV}^2$ and solving eqn. (4.19) for $C$ allows calculation of the required capacitance. The magnitude of $R_3$ follows directly from eqn. (4.18), resulting in component values $C_3=65\,\text{pF}$ and $R_3=8.2\,\text{M}\Omega$. As a physical resistor $R_3$ of such magnitude would consume excessive chip area (around 2.5mm^2 when realised as a POLY1 resistor), a combination of MOS transistors biased in the ohmic region is chosen to implement $R_3$ as an active resistor. As Fig. 4.15 shows, two complementary devices are used in series connection. In addition to providing the required high resistance, this arrangement, given an appropriate choice of relative channel lengths, considerably improves linearity compared to a single MOS-FET.

4.1.9 SIMULATED RESULTS

The noise performance of the preamplifier alone and in combination with the RC-filter have been simulated using circuit parameters provided by the
foundry [45]. The noise before and after filtering are compared in Fig. 4.16. As expected, the preamplifier 1/f-noise tail (including the DC offset) is removed by the filter. Between 50Hz and 1kHz the noise increases slightly, due to the thermal noise contribution from the active resistor, so that the total output voltage noise in the bandwidth 1Hz-10kHz remains unchanged at 25μV as expected. Filter resistance \( R_j \) deviates by only 0.03% from its nominal value of 8.2MΩ over the operating voltage range of ±25mV as Fig. 4.17 shows. The preamplifier and filter have been laid out in a 0.8μm double-metal double-poly process, so that estimates on the silicon area consumption could be obtained. The results are included in the summary of simulated results in Table 4.5.

4.1.10 MEASURED RESULTS

The measured result of the voltage noise before and after filtering is shown in Fig. 4.18. A comparison with the specification is given in Table 4.5. The measured results are obtained from a filter and amplifier manufactured in the AMS 0.8μm BiCMOS process but using only devices also available in the compatible 0.8μm CMOS process (because a CMOS process including a buried layer was not available for this thesis). In comparison with the simulated results of Fig. 4.16 the shape of the noise spectrum does not show the downward drop in the passband visible in the simulated results. This is due to the measured noise floor of the preamplifier, which is higher than simulation predicts. Therefore the measured output noise is also higher than specified. Still as expected, the spot noise density in the passband after filtering approaches the preamplifier noise floor. It is also clear from Fig. 4.18 that the filter contributes no additional noise to the system.
4.1.11 CONCLUSIONS

The design, evaluation and fabrication of a preamplifier for an implantable ENG recording system using nerve cuffs has been presented. The preamplifier employs a simple OTA arrangement whose optimum realisation for this application in terms of noise performance, size and power consumption requires the use of bipolar input devices. Although it is possible to meet the power/noise specification using a CMOS approach (in weak or strong inversion) this solution requires impractically large transistors. It is proposed that lateral bipolar transistors can be used instead of vertical devices at the cost of increased power consumption. Although the noise performance of these devices is not as good as that of comparable vertical transistors, it is shown that very low-noise performance can still be achieved with reasonable bias currents. To remove output offset voltages the use of a passive $RC$-filter is proposed as a coupling stage between the preamplifier and further high-gain stages. The analysis presented shows how the filter can be designed with unity noise figure. In addition to low-noise performance the filter consumes no static power and is small enough to be fully integratable. Simulated results confirm the performance of the amplifier-filter combination.
Fig. 4.16: Simulated output noise PSD before and after RC-filter. The total noise remains the same.

Fig. 4.17: Percentage variation of resistance from nominal value with applied voltage.
Fig. 4.18: Measured output noise PSD before and after RC-filter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Target</th>
<th>Simulated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>±2.5V</td>
<td>±2.5V</td>
<td>±2.5V</td>
</tr>
<tr>
<td>Gain</td>
<td>~100</td>
<td>99</td>
<td>108</td>
</tr>
<tr>
<td>Passband</td>
<td>300Hz-35kHz</td>
<td>296Hz-37kHz</td>
<td>270Hz-30kHz</td>
</tr>
<tr>
<td>Output noise in BW 1Hz-10kHz</td>
<td>&lt;30μV</td>
<td>25μV</td>
<td>33μV</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt;2mW</td>
<td>1.9mW</td>
<td>1.8mW</td>
</tr>
<tr>
<td>Process</td>
<td>CMOS</td>
<td>0.8μm</td>
<td>0.8μm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMOS</td>
<td>BiCMOS</td>
</tr>
<tr>
<td>Area</td>
<td>&lt;1mm²</td>
<td>0.35mm²</td>
<td>0.35mm²</td>
</tr>
<tr>
<td>Preamplifier</td>
<td>--</td>
<td>0.3mm²</td>
<td>0.3mm²</td>
</tr>
<tr>
<td>Filter</td>
<td>--</td>
<td>0.05mm²</td>
<td>0.05mm²</td>
</tr>
</tbody>
</table>

Table 4.5: Amplifier specifications and simulation results.
CHAPTER 5
IMPROVED RECORDING METHODS

5.1 EXPERIMENTAL DETERMINATION OF COMPOUND A-P DIRECTION AND PROPAGATION VELOCITY FROM MULTI-ELECTRODE NERVE CUFFS

5.1.1 INTRODUCTION
In this section, experimental evidence for the feasibility of the idea of velocity selective recording using a MEC and the proposed array of amplifiers is presented.

A method for the measurement of propagation velocity is to sum the outputs of the tripole amplifiers after introducing artificial time shifts \( \tau \). When \( \tau \) matches \( T \), the AP peaks add constructively to give the largest signal. Conversely, when using mismatched delays \( \tau \), the amplitude remains smaller. The time shift that results in the maximal amplitude corresponds to \( T \) and the sign of \( \tau \) indicates the direction of propagation. Such an arrangement can be tuned to one matched velocity as shown in Chapter 2. This applies to an SFAP but, because the system is linear, the response to a compound action potential (CAP) will be the sum of the responses (SFAPs) of all the active fibres. Thus, it should be possible to record selectively from different fibre populations in a compound nerve by using several channels with different time shifts \( \tau \), each tuned to a specific population.

5.1.2 EXPERIMENT AND RESULTS
Experiments were performed in-vitro at room temperature on the sciatic nerve of a frog. The nerve of approximately 2.5 cm length is threaded into a specially-made polyimide 17-electrode spiral cuff of 3 cm length and inter-electrode pitch of 1.8 mm. The layout of the cuff electrodes is shown in Figure 106.
5.1. The flexible 25 μm thick plasma-modified polyimide substrate was e-beam evaporation coated with a 400 nm thick gold layer, which was subsequently patterned using UV photo lithography [6]. All exposed gold areas except the cuff electrodes and external electrical connections were insulated with a spin-coated polyimide encapsulation layer. Impedance reduction of the cuff electrodes was performed by electrochemical deposition of iridium oxide [7]. This process typically lowers the magnitude of the electrode impedance by a factor of around 15 for the frequency range of interest (1Hz to 10 kHz). The impedance value of each cuff electrode is estimated to be ~20 Ohms, which is negligible compared to the expected electrode-to-tissue impedance of up to 1kΩ. As the nerve was too short to extend all the way through the cuff, only recordings from the first 11 electrodes are considered, as indicated in Figure 5.2. The nerve was stimulated at some distance from the cuff (around 1cm) at the root end of the nerve with hook-electrodes, while recordings were taken after the first-rank of amplifiers, resulting in 10 dipole signals. The intensity was just above threshold so that only the larger fibres were stimulated. It is assumed that the range of velocity is small and therefore that the CAP is the sum of SFAPs from a similar group of fibres. The specially-designed low-noise amplifiers (Chapter 4), with a pass-band between 300 Hz and 10 kHz, amplified the signal with a gain of 3000. The amplified ENG was recorded with a DAT recorder\(^1\) and played back through a digitising oscilloscope for evaluation. The 9 tripolar channels shown in Figure 5.3 were obtained by subtraction of the channel pairs in MATLAB. The traces show a CAP shortly after stimulation, with the top trace corresponding to the tripole nearest to the stimulation site. The first negative spike is the stimulation artefact; the small

\(^{1}\) TEAC RD-145T
ripples before stimulation are artefacts due to the high-order filtering within the
DAT recorder and oscilloscope. Joining the first positive peak of the CAP on the
traces clearly shows the time delay $T$ between the CAP peaks. The delay is
constant between electrodes 2 to 8 with 50 µs/tripole (i.e. 50 µs / 1.8 mm)
calculated from the slope of the connecting line. Equation 2.5 relates $T$ to a
conduction velocity of $v = 36$ m/s, which is near the maximal velocity in frog
nerve of (5-37 m/s [89]), as expected.

Figure 5.1: Cuff electrode before curling.

Figure 5.4a shows the results of summation with delays between -50 µs and
150 µs. Ignoring the stimulus artefact, the maximum CAP amplitude between the
first negative and the next positive peak is plotted in Figure 5.4b for different time
delays. The result is a tuning curve with a signal amplitude at $\tau = 52$µs, which
confirms the observation above. Furthermore, the positive sign of $\tau$ indicates a
direction of CAP propagation away from the hook electrodes. The maximum error
introduced by digitising the recorded signals is approximately ±2µs, which
includes the channel skew introduced by the recorder.
Fig. 5.2: Experiment Setup.

Fig. 5.3: Action potential delayed by a constant time $T = 50 \mu s$ between the traces ($d=1.8\text{mm}$).
Fig. 5.4: Signals produced after summation of the five tripole amplifier outputs with time delays. On the right is the tuning curve, showing a peak at $\tau = 52 \mu$s.

5.1.3 DISCUSSION AND CONCLUSION

The recorded CAPs are marred by stimulus artefacts. Even allowing for their presence, the CAPs do not appear quite the same, which may be due to variation in the electrode impedance (per unit area) and the contact area between the nerve and the row of electrodes. Nevertheless, when the artificial delay is varied off-line (Fig. 5.4), there is, as expected, a peak when the propagation delay $T$ is matched by $\tau$.

Clearly very much better methods for reducing stimulus artefact are necessary before it will be worth comparing the shapes of the CAPs, seen after the tripole amplifiers, quantitatively. Such a comparison will be valuable because the method may be spoilt by many rather diverse factors:

- The uniformity of the nerve within the cuff: were any branches cut?
- The uniformity of the connective tissue that grows in the cuff.
• The ‘waviness’ of the nerve within the cuff.
• The ‘waviness’ of the axons within the nerve.
• Scaling factor $A$ may differ from Eqn. 2.6, e.g. due to cuff end effects.
• Dispersion of APs due to the stimulation of nerves with a spread of velocities.
• The noise from the electrodes, tissue resistance, and the amplifiers.

Gordon et al.[10] and Hoffer [11] have used cross-correlation to estimate propagation velocity between two tripoles. By using an MEC, an estimate of the velocity is found, based on many tripoles: it should therefore be less sensitive to irregularity due to these factors than correlation from two tripoles. Clearly new experiments and technical development will be necessary to see whether the method is practicable for naturally-occurring nerve signals.

In a neuroprosthetic device with velocity-selective neural inputs, the artificial delays and addition would be implemented in real time. For one value of $\tau$, the output would be maximal for one AP velocity, and this would have a filtering action when a multitude of single-fibre APs propagate, either in a compound AP or as randomly-timed APs in a natural neural signal. The delay-and-add structure of the signal processor can be repeated for several different matched velocities, over the positive and negative range, to give many channels from one cuff.

5.2 MEASUREMENT OF MEC NOISE

In Chapter 2 a theory to describe the noise performance of a MEC has been developed. In this section experimental results are presented, which yield a first confirmation of the theory.
5.2.1 Experiment

A polyimide cuff similar to the one used in the experiment on velocity selectivity described in the previous section has been used for the following measurements [90]. However, this cuff has a smaller diameter and was sealed along its side to limit current leakage. The cuff contains 11 electrodes on a length of 30mm. The noise between adjacent electrodes is recorded with the cuff immersed in a 0.9% physiological concentration of Saline (Fig. 5.5). As the cuff is filled with saline, $R_n$, representing lead- and tissue contact resistance in the cuff model, is very small. A value of around 20\(\Omega\) is assumed. The axial resistance between adjacent electrodes is measured while the cuff, is temporarily removed from the beaker to eliminate the short between the cuff ends. Care is taken to ensure that the saline inside the cuff remains. An impedance of around 500\(\Omega\) was measured at 1kHz. An ASIC containing an array of 10 of the low-noise lateral BJT amplifiers with a gain of approximately 100 as described in the previous chapter was connected to the cuff in the overlapping configuration (Fig. 5.6). Fig. 5.7 illustrates the setup but does not show the second rank amplifiers. The output voltage of the 10 dipole channels is recorded with a DAT recorder for off-line evaluation.

---

**Fig. 5.5:** Cuff in saline.  
**Fig. 5.6:** Bench setup with amplifier ASIC.
5.2.2 Measured Results
The recorded data is played back from the DAT recorder and 3 channels at a time are sampled on a digital storage oscilloscope. The sample frequency is 50kHz and 4096 samples are taken for each channel. The tripole responses were obtained by subtraction of the channel pairs in MATLAB. Thus, 9 channels of tripole data are available in the time domain, which are delayed by time τ ranging from zero to 1ms before addition to form the MEC output. A fast-fourier transform, also performed in MATLAB, yields the power spectral density of the MEC output. For n=10 the spectral density at frequencies 500Hz and 1kHz is plotted versus τ in Fig. 5.8. The theoretical noise (sum of (2.34) and (2.50)) is also plotted in the figure. Strikingly, the graph shows a high frequency waveform superimposed on the expected results. Except for this additional component the measured result closely agrees with the theory. Simulation of the experiment setup has been performed using CADENCE design tools in order to determine the cause for the unexpected variation. It is found that the measured result is consistent with a situation where additional noise is present on the dipole channels. Adding, for example, the same noise voltage of 5.75nV/√Hz to each of the preamplifier outputs as symbolised by the arrows in Fig. 5.7 yields the simulated result of Fig. 5.9. The noise expected from the theory is plotted for comparison. As in the measured results an additional high frequency wave is found superimposed on the expected noise component.

5.2.3 Discussion and Conclusions
The noise theoretically expected from superposition of cuff noise (2.34) and amplifier noise (2.50) agrees with the measured results except for an additional higher frequency component. Simulation suggests that this unexpected behaviour
is due to an additional noise source affecting all dipole channels. At least two possible sources causing the effect can be identified:

a) Interference pickup by the connective tracks on the ASIC, especially at high impedance nodes such as at the AC-coupling output.

b) A noise voltage appearing between the amplifier reference ground and the reference ground of the DAT recorder. Interference is again a likely source.

The latter source of noise would not be present in an implanted cuff, where the delay-and-add structure is implemented on the cuff. Noise pickup by the ASIC would also be reduced due to the shielding effect of the surrounding tissue. It may also be necessary to increase the power-supply rejection of the preamplifiers. Higher levels of interference reduction are possible by careful layout and on-chip shielding. Clearly, further experiments with a well-characterised experimental setup are necessary to establish the source of the additional noise. However, in principal the measured results confirm the theoretical considerations on MEC noise presented in Chapter 2. They are further evidence that the MEC can successfully be combined with the proposed amplifier array to advance the state-of-the-art in neuroprothetics, although a lot more research is required.
Fig. 5.7: Recording setup and likely entry points of interference (arrows).

Fig. 5.8: Measured noise compared with expected results.
5.3 ADAPTIVE EMG CANCELLATION

5.3.1 INTRODUCTION

A control system has been described recently in [91], which adaptively cancels interfering signals such as EMG by automatically adjusting the amplifier gains in a *true-tripolar* arrangement to restore signal symmetry (Fig. 2.5). Although the EMG is not completely eliminated using this approach, the requirement for post-filtering is much reduced resulting in a solution which is implantable.
A block diagram of such an adaptive amplifier is shown in Fig. 5.10. It consists of a true-tripole recording structure in which the gains of the input differential amplifiers, $G1$ and $G2$ have been made variable, controllable by the differential signals $V_{f+}$ and $V_{f-}$. The control system can be incorporated into the low-noise system described in the preceding chapters after the low-noise preamplifiers ($A1$ and $A2$). As the EMG appears linearly across the tripole as indicated in Fig. 5.10 and the cuff model in Fig. 2.4, voltages $V_1$ and $V_2$ are of identical amplitude (but inverted due to the polarity of the preamplifiers) in a fully balanced structure. Any imbalance results in either $V_1$ or $V_2$ being of larger amplitude, so that subtracting their moduli is a measure of magnitude and direction of the tripole imbalance. The subtraction is performed by the differential inputs of the integrator. A positive and negative copy of the integrated signal is fed back to the variable gain amplifiers to compensate for any imbalance. The loop gain of the system can be increased by adding two high-gain amplifiers into the circuit as indicated by the dashed structures in Fig. 5.10. The amplifiers are allowed to saturate, yielding a square waveform at their output (mark-space-ratio of the input signal). In this case the integrator is not required to be linear, which is discussed in Section 5.3.5. Adding further independent loops adopts the feedback
system to a multi-electrode cuff (Fig. 5.11). Further details about the adaptive system including simulated and measured results can be found in [46, 47, 92] and are subject of a forthcoming Ph.D. thesis at the University College London by I. F. Triantis. The integrator block can be identified as a key element of the system. Especially in a low-noise system as this, it is desirable to avoid the use of a clock with its associated interference, so that switched-capacitor integrators are not an optimum choice. A time-constant $\tau$ of at least 1 second is required, although the absolute value of the time-constant is not critical, allowing for an integrated solution [93]. Therefore, in the following sections the design and implementation of a continuous-time, very large time-constant integrator ($\tau$ around 5 seconds) suitable for the control system is discussed.

Fig. 5.11: Adaptive system applied to a MEC.

5.3.2 VERY LARGE TIME-CONSTANT LOW-POWER CMOS INTEGRATOR

Several approaches for the design of integrators with very large time constants have been reported [94-99]. In general, these are divided into switched-
capacitor (SC) techniques [99] and operational transconductance amplifier-capacitor (OTA-C) techniques with very small transconductances to allow the capacitance to be kept manageably low [94-98]. However, the use of SC techniques is not suitable for many biomedical applications because of its use of analogue data sampling. In the case of implantable devices for nerve signal recording where microvolt signals are involved, this can lead to clock feedthrough problems and reduce dynamic range. Furthermore, SC implementations for very large time constants tend to require large capacitor ratios [94]. For these reasons, the OTA-C approach is often preferred. However, the realization of OTAs with very small transconductances is not easy due to dynamic range, noise level, power dissipation and silicon area constraints [95]. Various topologies have been suggested to address this problem. Examples include the use of current division, current cancellation, current feedback and the cascading of transconductance-transimpedance \((g_m^{-1}/g_m)\) stages [94-98].

In the following sections, the design of a micropower CMOS OTA-C integrator with a tuneable, extremely large time constant (nominal value of 5 s) is presented. The integrator is based on the \(g_m^{-1}/g_m\) chain approach [101]. It is primarily intended for use in the adaptive recording system but is not restricted to this application. The integrator described here is superior to competing designs [94-99] in terms of the parameters relevant to this application.

5.3.3 TUNING A VERY LARGE TIME CONSTANT

The realisation of a very large time constant for implantable biomedical systems with an on-chip physical resistor and capacitor would require unrealistic chip area and would not be tuneable. In addition, component tolerance would make the resulting time constant very unpredictable. In an OTA-C integrator the
passive resistor is therefore replaced with an OTA having very small overall transconductance ($G_m$). In practical realisations the output impedance of the OTA-C integrator (Fig. 5.12) is finite, resulting in the transfer function

$$A(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G_m \cdot 1}{C \cdot s + \tau^{-1}}$$

(5.1)

where $s$ is the Laplace operator and $\tau = CR_o$ is the time constant given by the product of the capacitance $C$ and output impedance $R_o$. The resulting lossy integrator (Fig. 5.12) can be used directly as a first order filter or as a building block in the realisation of higher order filters. Tuning of the filter cut-off frequency is achieved by variation of $\tau$. In conventional $G_m$-$C$ filters, $\tau$ is usually controlled by the transconductance gain $G_m$. This is achieved by applying local negative feedback around the integrator [96, 101], where for a feedback factor $\beta$ the transfer function is given by:

$$A(s) = \frac{G_m}{C} \cdot \frac{1}{s + \frac{1}{CR_o} + \frac{\beta G_m}{C}}$$

(5.2)

so that $\tau$ becomes:

$$\tau = \left( \frac{1}{CR_o} + \frac{\beta G_m}{C} \right)^{-1}$$

(5.3)

The design goal is to make the second term in (5.3) dominant over the first term so that $\tau$ can be adjusted by choice of $G_m$ and $C$, as required. It is necessary,
therefore, that $\beta G_m >> 1/R_o$. However, when realising very large time constants, it is difficult to satisfy this condition, as $R_o$ cannot be increased without limit and increasing $\beta$ or $G_m$ would decrease the effective time constant. We therefore propose in this paper to operate the integrator without local feedback ($\beta=0$) and to trim $\tau$ by variation of $R_o$ instead of $G_m$. Note that although the dependency between time constant and $G_m$ is removed, linear operation of the integrator still requires a small transconductance.

### 5.3.4 APPROACHES FOR REALIZING LARGE $C/G_M$ RATIOS

Various circuit techniques have been proposed to achieve the effective large capacitances and/or small transconductances required for very large time constant integrators [100]. The capacitance scaling technique proposed in [99] can be used to multiply the physical capacitance $C$ present at a circuit high impedance node by feeding back a scaled-up copy (of factor $N$) of the current flowing through $C$ and subtracting it from the input current signal. Fig. 5.13 shows the schematic diagram of the scaling circuit and the small signal equivalent circuit without parasitic impedances. The scaled capacitance $C_s$ observed at node $C'$ is determined by physical capacitor $C$ and a current and transistor ratio $N$. The feedback current $g_{mN}v_{gs} = N \cdot i_c$ is subtracted from capacitor current $i_c$, resulting in an effective capacitance $C_s = (N+1) \cdot C$, i.e. an increase by a factor of $(N+1)$. In effect the circuit provides the Miller-Capacitance at node $C'$. With this technique scaling ratios on the order of 10 are achievable with practical current mirror transistor ratios [94].

In the technique of transconductance reduction by current division, the current generated by a fully-balanced OTA is further reduced by using current...
mirrors with large division factors $N$ (Fig. 5.14). The realisation of an integrator based on this technique with a time constant of 700 ms was reported, consuming an area of 0.5 mm$^2$ in a 3 μm CMOS process [98]. However, in order to decrease the transconductance further, the mirror transistor ratios have to be increased, which leads to large silicon area designs and sets a limit to the maximum practicable time constant.

![Figure 5.13: Capacitance scaling. Simplified schematic and small-signal equivalent circuit.](image)

Another popular technique to reduce the OTA transconductance is by current cancellation [102]. A small transconductance is achieved by cross-connecting segments of the input MOS transistor drains of a differential pair to reduce the effective signal currents as shown in Fig. 5.15. The reduction factor $N$ is determined by the proportion $n$ of cross-coupled transistor segments with $N = n + 1/n - 1$, with the highest cancellation for $n$ approaching unity. The circuit is ultimately limited by geometry mismatches, as $N$ is a strong function of $n$ near unity. As a result $n$ is limited to the range of 0.5 to 0.9 [102].

Cascading of basic transconductance and transimpedance ($g_m^{-1}/g_m$) elements to achieve a very small overall transconductance is proposed in [101]. The effective overall transconductance of the chain is the product of the transfer
functions of the single stages, which allows transconductance reduction to any desired level by adding more stages to the chain.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{transconductance_reduction.png}
\caption{Transconductance reduction by current division.}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{current_cancellation.png}
\caption{Current cancellation technique.}
\end{figure}

A comparison of the aforementioned approaches is given in Table 5.1 in terms of achievable scaling factor and design constraints. The cascade method was used for the integrator design in this paper as it offers a very high scaling
ratio on a small silicon area and high flexibility combined with the possibility of
low-power consumption by biasing all transistors in weak inversion.

<table>
<thead>
<tr>
<th>Technique</th>
<th>Max. scaling factor</th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance scaling</td>
<td>10</td>
<td>Used in addition to $G_m$ reduction</td>
<td>High current and transistor ratios</td>
</tr>
<tr>
<td>Current division</td>
<td>100</td>
<td>High voltage swing capability</td>
<td>Large transistor ratios required</td>
</tr>
<tr>
<td>Current cancellation</td>
<td>10</td>
<td>Small silicon area</td>
<td>Very sensitive to mismatch</td>
</tr>
<tr>
<td>Cascading ($g_m^{-1}/g_m$)</td>
<td>unlimited</td>
<td>Small silicon area, high flexibility</td>
<td>Offsets throughout the chain add</td>
</tr>
</tbody>
</table>

Table 5.1: Comparison of transconductance reduction approaches for realizing high C/$G_m$ ratios.

5.3.5 CIRCUIT DESCRIPTION

In the design of the integrator, each transconductance ($g_m$) stage was realized by a simple CMOS OTA with p-MOS inputs and each transimpedance ($1/g_m$) stage by a diode-connected n-MOS transistor. A total of three $g_m$ and two $1/g_m$ stages were cascaded. Given that in weak inversion the transconductance of an OTA and the resistance of a diode-connected transistor are [84]:

$$g_m = \frac{I_i}{nU_{th}}$$  \hspace{1cm} (5.4)

$$r = 1/g_m = \frac{nU_{th}}{I_i}$$  \hspace{1cm} (5.5)

respectively, the resulting overall transconductance of the $g_m$-$1/g_m$ chain is given by

$$G_m = g_m \left( \frac{I_5}{I_2I_4} \right)$$  \hspace{1cm} (5.6)
where $U_{th}$ is the thermal voltage, $n$ is the weak inversion slope factor which for simplicity is assumed to be identical for p-MOS and n-MOS devices, $g_{m1}$ is the transconductance of the first stage and $I_{1.5}$ is the total current in each stage.

The circuit schematic of the first four stages of the chain is shown in Fig. 5.16 and that of the last stage is shown in Fig. 5.17. Currents $I_1$ to $I_5$ are all in the nano-ampere range chosen to result in an overall $G_m$ value of 125 pA/V (nominal value). To achieve better-balanced DC conditions, an extra diode-connected n-MOS transistor $M10$ is connected at the inverting input of the second OTA as shown in Fig. 5.16. The last stage shown in Fig. 5.17 is a symmetrical OTA with regulated cascode n-MOS mirror transistors ($M16$-$M21$) biased by current sources $I_{reg}$. The integrating capacitor $C$ is connected across the low and high impedance output nodes, $V_{out1}$ and $V_{out2}$, respectively. Ideally, the DC voltages at these points are identical, resulting in minimum offsets (i.e. zero initial condition of the integrator) when the output voltage signal $V_{out} (= V_{out2} - V_{out1})$ is taken across the capacitor. For a maximum time constant of 10s a capacitance $C$ of 70pF was chosen according to (5.3).

---

*Fig. 5.16: First four stages of the gm-1/gm chain.*

125
A. Modes of Operation

If the input transistors of the first OTA \((M1\text{ and } M2, \text{ Fig. } 5.16)\) are to be kept in weak inversion, the input voltage must be restricted to \([84]\):

\[ V_{\text{in}} < 2nU_{\text{th}} \quad (5.7) \]

As \(V_{\text{in}}\) approaches \(2nU_{\text{th}}\), the output current of the first OTA increases asymptotically towards the common source current \(I_1\) and hence a further increase in \(V_{\text{in}}\) cannot increase the output current. The resulting non-linearity (i.e., saturated operation of the OTA) can be exploited very advantageously in applications such as this, where the mark-space ratio of a square waveform is converted into a proportional voltage (Fig. 5.10) so that the linearity of the integrator is not essential. In this mode of operation the drain current limitation effectively reduces the transconductance of the input OTA \(g_{m1}\).

\[ \text{Fig. 5.17: Last stage of the } g_{m1}/g_{m} \text{ chain.} \]
B. Offset Cancellation

Due to the very small $G_m$ value of 125 pA/V, the time constant of the integrator is ultimately limited by the charge leakage at the output node. The impedance of the output node must therefore be kept very high, which in turn dramatically increases the effect of offset currents in the output branch on the DC voltage level at this node. External trimming of the output stage is therefore necessary in most cases. Adjustment of the current source $I_{\text{offset}}$ in Fig. 5.16, allows for this trimming by altering the DC currents in the output branches of the OTA through adjustment of its gate bias to restore nominal conditions. The small transconductance of the output stage ($g_{m3}$) reduces the sensitivity of the output voltage to the trimming source compared to current trimming directly in the output branch, which relaxes the specification on the trimming current source.

C. Tuning the Time constant

Two values of bias current are used ($I_1 = I_3 = I_5$ and $I_2 = I_4$, with a ratio of around 10), which are generated on-chip by dividing an external 2.5 μA current source ($I_{\text{bias}}$) using simple current mirrors. Current $I_5$, which biases the output OTA (Fig. 5.17), varies proportionally with $I_{\text{bias}}$ and half of this current is mirrored into each of the output branches. The impedance at output node $V_{\text{out1}}$ is established by the diode-connected p-MOS mirror transistor $M22$ and is low compared with the impedance at $V_{\text{out2}}$, which is mainly determined by the drain-to-source resistance of the other p-MOS mirror transistor $M23$. Given that the drain-to-source resistance of a MOS transistor is approximated by [84]:

$$R_{ds} = \frac{1}{\lambda I_d}$$

(5.8)
where $\lambda$ is the channel length modulation parameter and $I_d$ is the drain current, variation of $I_{\text{bias}}$ is used to adjust the output impedance of the integrator and to tune the time constant according to (5.3), both in the linear and saturated modes of operation. Despite all currents $I_1-I_5$ being proportional to $I_{\text{bias}}$, eqn. (5.6) shows that only $g_m$ affects the overall transconductance, so that in this implementation $G_m$ varies inversely proportional with $R_o$. For applications where constant $G_m$ is required, bias current $I_1$ of the first OTA can be held constant by deriving it from a separate bias source. Considering that half the bias current $I_5$ is mirrored into the high-impedance output branch and using (5.3) and (5.8) the time constant can be expressed as

$$\tau = \frac{2C}{I_s \lambda}$$

(5.9)

Equation (10) is inversely proportional to the external bias current, i.e.,

$$\tau \propto \frac{1}{I_{\text{bias}}}$$

(5.10)

### 5.3.6 MEASURED RESULTS

The integrator was fabricated using the AMS 0.8μm double-metal, double poly CMOS technology. The simulations and layout were carried out using the CADENCE design kit provided by the foundry [45]. The microphotograph of the chip (core) is shown in Fig. 5.18. For testing purposes two on-board buffers were included. In total five chips were tested and all showed correct operation.

Firstly, the output voltage ($V_{o1}$ in Fig. 5.16) of the input OTA-diode combination was measured against the amplitude of the input voltage ($V_{in}$) to specify the exact regions of linear and saturated operation. As shown in Fig. 5.18 an input voltage smaller than about 200mV ensures linear operation and
amplitudes above about 380mV saturated operation. These values agree well with eqn. (5.7).

Fig. 5.18: Chip microphotograph (core).

A. Linear Operation

A sine wave of frequency 1 Hz and amplitude 200 mV (pk-pk) was applied to test the circuit at the limit of the linear region. The integrator output voltage ($V_{out}$) response is plotted in Fig. 5.20. The output signal shows only minor distortion and this confirms the linearity of the $g_m^{-1}/g_w$ chain. A square waveform of amplitude 120 mV (pk-pk) results in the triangular output waveform plotted in Fig. 5.21. The time constant of the integrator was varied by adjusting the external bias current ($I_{bias}$). In all five chips, the fall-time was found to be slightly longer than the rise-time. The time constant follows eqn. (5.10) as Fig. 5.22 shows, and is tuneable between 0.2 s and 10 s.

The integrator was then biased to have a time constant of approximately 2.5 s and its transfer characteristics were measured in open-loop as well as closed-loop configuration with a feedback gain of unity. The results are shown in Fig. 5.23 and agree with the simulated results also plotted in the figure. The $-3$dB cut-off frequency of the open-loop integrator is 66 mHz and increases to 220 mHz when the loop is closed, which corresponds to a more than threefold increase in time-constant over the conventional closed-loop $G_m$-$C$ approach.
B. Saturated Operation

To test the circuit in the saturated mode of operation, a square waveform of amplitude 600 mV (pk-pk) was applied. Figure 5.24 shows that the integrator works as predicted. The slope of the output signal is slightly higher than for the smaller square waveform (Fig. 5.21), but remains constant for any saturating input signal amplitude.

The integrator chip characteristics are summarized in Table 5.2, and these agree closely with simulations. Most of the power dissipation is due to the output buffers, but these were only included for testing purposes. Further measurement results with similar designs featuring an alternative biasing scheme suggest that the power dissipation of the bias circuitry may be reduced to 2 μW without any degradation in performance by using current splitting instead of current mirrors to divide the external bias current. A comparison with other integrated designs in terms of time constant, active area, and power dissipation is given in Table 5.3. The integrator offers superior performance in terms of power consumption, die area and time-constant when compared with previously published work.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.8 μm CMOS</td>
</tr>
<tr>
<td>Power supply</td>
<td>± 1.5 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td></td>
</tr>
<tr>
<td>integrator core</td>
<td>230 nW</td>
</tr>
<tr>
<td>bias circuitry</td>
<td>16.2 μW</td>
</tr>
<tr>
<td>output buffers</td>
<td>23.7 μW</td>
</tr>
<tr>
<td>Active area</td>
<td>0.1mm²</td>
</tr>
<tr>
<td>Time constant</td>
<td>0.8s - 10s</td>
</tr>
<tr>
<td>Input voltage range</td>
<td></td>
</tr>
<tr>
<td>linear operation</td>
<td>(V_{in} &lt; 200\text{mV})</td>
</tr>
<tr>
<td>saturated operation</td>
<td>(V_{in} &gt; 380\text{mV})</td>
</tr>
</tbody>
</table>

*Table 5.2: Summary of performance.*
### 5.3.7 CONCLUSION

A continuous-time CMOS integrator with an extremely large time constant has been presented. The circuit operates in weak inversion and allows both tuning of the time constant over a wide range and trimming of output offset voltages. Furthermore, it features lower power dissipation and smaller die area than previously reported designs. Its operation was verified by experimental measurements on fabricated samples using 0.8μm CMOS technology. Although the integrator presented was designed for use in an adaptive nerve signal amplifier, it may also be used in the design of very low power active filters with very low cut-off frequencies for other applications.

![Transfer characteristics of the first $g_m^{-1}/g_m$ stage.](image)

*Fig. 5.19: Transfer characteristics of the first $g_m^{-1}/g_m$ stage.*

---

<table>
<thead>
<tr>
<th>Reference</th>
<th>Time constant (ms)</th>
<th>Active area ($\text{mm}^2$)</th>
<th>Power consumption ($\mu\text{W}$)</th>
<th>CMOS Process ($\mu\text{m}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>~5000</td>
<td>0.1</td>
<td>0.23</td>
<td>0.8</td>
</tr>
<tr>
<td>[5]</td>
<td>690</td>
<td>0.5</td>
<td>not stated</td>
<td>3</td>
</tr>
<tr>
<td>[6]</td>
<td>70</td>
<td>0.8</td>
<td>500</td>
<td>5</td>
</tr>
<tr>
<td>[1]</td>
<td>66</td>
<td>1.0</td>
<td>10</td>
<td>0.8</td>
</tr>
</tbody>
</table>

*Table 5.3: Comparison with other integrator designs.*
Fig. 5.20: Integration of small sine waveform input.

Fig. 5.21: Integration of small square waveform input.

Fig. 5.22: Variation of the time constant with external current source $I_{bias}$. The measured values (markers) follow the ideal hyperbolic.
5.4 ACQUISITION SYSTEM - MEASURED RESULTS

An ASIC comprising the acquisition system as proposed in chapter 2 (Fig. 2.22) was designed in the AMS 0.8μm BiCMOS process. The chip contains the 10 low-noise preamplifiers using lateral bipolar input transistors presented in Chapter 4, 10 coupling filters, also discussed in Chapter 4, and the large time-constant integrator as a separate block for testing. In addition 10 second-rank amplifiers with a gain of 100, 9 summing amplifiers with a gain of 10 and the channel selection multiplexer (MUX) complete the system. These additional
circuits are not critical in terms of noise or power consumption, as the preamplifiers dominate these parameters, and can be implemented with standard designs [50, 66]. A possible configuration of the second-rank amplifier is shown in Fig. 5.25. The amplifier consists of a fully symmetrical OTA, where the output current feeds into the impedance provided by transistors $M6$ and $M8$ to achieve a high voltage gain. The gain stage is followed by an output stage $M9$-$M16$ as discussed in [50] to drive the resistive feedback network $R1$-$R2$, which by negative feedback sets the overall voltage gain to around 100. Capacitor $C$ is chosen to achieve the desired high-frequency cut-off of the recording channel at around 5kHz.

![Fig. 5.25: Schematic of a possible implementation of the second-rank amplifier.](image)

The differential amplifier which forms the tripole output can be implemented as a feed-forward stage, similar to the topology of the preamplifier. Figure 5.26 shows this arrangement, where an OTA identical to the one used for the second-rank amplifier feeds into resistor $R$ to produce the desired voltage gain.
As no feedback network is required, both positive and negative inputs are available as inputs to the ENG signal.

The voltage gain of a typical dipole channel using the proposed preamplifiers and the 2\textsuperscript{nd}-rank amplifier shown in Fig. 5.25 is graphed in Fig. 5.27. The low frequency cut-off is set by the AC-coupling stage to around 260 Hz. The high cut-off frequency of the preamplifiers is designed at above 10kHz as discussed in Chapter 4, so that the 2\textsuperscript{nd}-rank amplifier determines the overall cut-off of the recording channel. A frequency of around 6kHz was measured for the given design in agreement with simulation results, also shown in Fig. 5.27. As the preamplifier dominates the noise performance, the measured results presented in Chapter 4 equally apply for the system. The measured results are compiled in Table 5.4 and are in good agreement with the requirements of the recording system specified in Chapter 2 (Table 2.3). The layout of the ASIC and a photograph of the die under test are shown in Fig. 5.28.
Fig. 5.27: Measured voltage gain of a typical dipole channel (bold) and simulation result (dashed).

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pass-band</td>
<td>260Hz – 6kHz</td>
</tr>
<tr>
<td>Process</td>
<td>0.8μm BiCMOS</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>±2.5V</td>
</tr>
<tr>
<td>Dipole voltage gain</td>
<td>12,200</td>
</tr>
<tr>
<td>Power consumption</td>
<td>24mW</td>
</tr>
<tr>
<td>Input referred voltage noise in passband</td>
<td>291nV\text{rms}</td>
</tr>
<tr>
<td>Input referred current noise in passband</td>
<td>190pA\text{rms}</td>
</tr>
<tr>
<td>Dipole channels</td>
<td>10</td>
</tr>
<tr>
<td>Tripole channels</td>
<td>9</td>
</tr>
<tr>
<td>Active area</td>
<td>12mm\textsuperscript{2}</td>
</tr>
</tbody>
</table>

Table 5.4: ASIC measured results.
Fig. 5.28: Top: ASIC layout. Unidentified structures are additional test circuits.
Bottom: Die mounted in PGA package for testing.
CHAPTER 6
CONCLUSIONS AND FUTURE DIRECTIONS

6.1 CONCLUSIONS

The main purpose of the work presented in this thesis was to provide methods and circuits to enhance nerve cuff ENG recording with the intended use as control signal in neuroprostheses. If naturally-occurring nerve signals are to be used for the detection of signals that are not dominant in the nerve traffic, it will be vital to discriminate between traffic with different propagation velocities and directions. The MEC was proposed as a means to access these additional data. The use of a MEC entails the availability of an ASIC with a low-noise, high-gain array of amplifiers. Considering the practical requirements of such a system, this thesis addresses two main questions:

a) What is the MEC performance in terms of signal and noise compared to the conventional tripole?

b) What is the optimum solution in terms of noise, area and power consumption for a recording system in this application?

6.1.1 MEC Signal and Noise

First experimental evidence that the MEC may be used for velocity-selective recording using CAPs is reported in this thesis. The transfer function of the MEC is described in Chapter 2, which shows that the MEC behaves as a velocity-selective filter whose centre frequency is variable by introducing a time delay before summation of the individual tripole outputs. Comparison of the
signal amplitude with that of a single tripole of the same length shows that an optimum number of electrodes exists, which yields maximum output amplitude. Furthermore, partial cancellation of the MEC noise yields an improved SNR at low velocities. Noise matching between amplifiers and the cuff is discussed, leading to an optimum solution in terms of SNR. The analytical expressions derived in Chapter 2 give insight into the fundamental MEC performance, and lay the foundation for its practical application.

6.1.2 Low-noise array of amplifiers

Chapter 4 describes the design of a low-noise amplifier, which in terms of its relevant parameters including size, power consumption and noise is suitable for the application in a MEC recording array. It is shown that bipolar input transistors are required to achieve the specified low-noise operation. The feasibility of using lateral bipolar transistors in a cheaper CMOS process is examined. It is concluded that lateral transistors can be used in a design with performance comparable to the vertical BJT implementation, as long as the manufacturing process includes a buried layer or otherwise provides devices of high efficiency.

The proposed amplifier yields measured input referred voltage and current noise densities of $3\text{nV/\sqrt{Hz}}$ and around $2\text{pA/\sqrt{Hz}}$ respectively at $1\text{kHz}$. It is shown in Chapter 2 that this ratio of voltage to current noise matches the amplifiers well to both, the MEC and the dipole channels. As ENG recording requires signal amplification with very high gain, offset voltages become a limiting factor for the dynamic range of the system. This issue is addressed in Chapter 4, where an AC filter is proposed to remove DC offsets at the preamplifier output before further amplification. A multi-channel recording system based on the proposed circuit blocks has been designed and tested as presented in Chapter 5.
6.1.3 Adaptive EMG cancellation

A system to actively cancel the effect of EMG on ENG recordings has recently been proposed. Such a system includes a very long-time-constant integrator with a time constant in excess of 1 second. Such an integrator is difficult to implement without external components or high frequency clocks, whose interference may be harmful in this application. An integrator with the required time-constant is proposed in Chapter 5, performing better in terms of the relevant parameters compared to previously published designs.

6.2 FUTURE DIRECTIONS

The main focus of this thesis is on laying the foundation for the improvement of ENG recordings by proposing the MEC and a suitable recording interface. However, a large amount of work remains to be completed before such a cuff can successfully be used in conjunction with a neuroprosthesis in humans. The following points are issues that presently need to be addressed:

- Experiments are required to establish the magnitude of the offset voltage at the electrode-to-tissue interface of a MEC. Offset voltages of a few millivolts can be accommodated by the proposed acquisition system. However, larger offsets require additional reduction techniques.
- It has to be investigated how the MEC delay-and-add structure can most sensibly be integrated on the recording ASIC, using analogue or digital design techniques.
- The recording ASIC has not as yet been tested in vivo. Also the method of velocity-selective recording needs to prove its effectiveness with naturally-occurring ENG.
- Further experiments on the noise performance of the MEC need to be conducted to follow up on the initial results reported in this thesis.
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