GALLIUM ARSENIDE QUANTUM WELL MODULATORS GROWN ON SILICON SUBSTRATES

A thesis by

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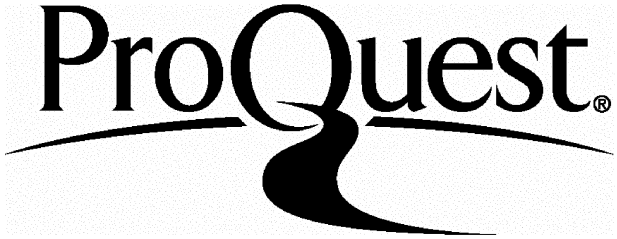


ABSTRACT

This thesis describes an investigation into GaAs/GaAlAs multiple quantum well (MQW) modulators grown on silicon substrates. The basic device consists of a *pin* diode containing quantum wells within the intrinsic region. Application of a reverse bias voltage to the device causes a change in the absorption of the MQWs. This change may be used to modulate a beam of light incident upon the modulator. By enclosing the device within a Fabry-Perot cavity, resonance effects can be used to enhance the degree of modulation. Such a device is known as an asymmetric Fabry-Perot modulator (AFPM).

The motivations for the integration of GaAs and Si are derived from an appreciation of the merits of the two different materials. For purely electronic systems there may be advantages, but most exciting are the possibilities for new systems using optics to enhance the capabilities of electronics. Chapter 1 introduces these issues and presents a discussion on possible future optoelectronic systems. Given that a high enough level of integration can be achieved, the AFPM is shown to be a promising device for use in such systems. The properties of MQW devices epitaxially grown on silicon have therefore been investigated.

A problem of GaAs on Si growth is the material mismatch, which results in a degree of strain in the epitaxial layer. The effect of this on MQW devices is discussed in Chapter 2. The material mismatch also creates a number of difficulties in the growth process and has an impact on material quality. These issues are discussed in Chapter 3, together with an outline of methods by which material quality could be improved. A study of the material quality of devices grown by both MOCVD and MBE is presented. Substrates used included plain, patterned, and GaAs pre-coated silicon. Material analysis was performed by electron microscopy, optical microscopy, photoluminescence, and optical beam induced current (OBIC) scanning optical microscopy.

Photocurrent and absorption measurements were made on a number of GaAs on Si MQW *pin* diode test structures and the results described in Chapter 4. Quarter-wave reflector stacks were also grown on silicon and their performance compared to similar devices grown on GaAs. The results of both these studies were used to model the performance of a complete AFPM structure. Experimental results for these modulators are presented in Chapter 5. These include both photocurrent and reflection spectra.

LIST OF CONTENTS

Chapter 1

An Introduction To Gallium Arsenide On Silicon Optoelectronic Devices

1.1 INTRODUCTION

The motivations for the integration of Gallium Arsenide and Silicon are derived from an appreciation of the merits of the two different materials. There are distinct advantages for purely electronic systems, but most exciting are the possibilities for new systems using optics to enhance the capabilities of electronics. For the latter application a solution combining the merits of both GaAs and silicon will be shown to be particularly powerful. Early work concerning GaAs on silicon recognized the optical properties of GaAs that silicon does not possess, however the implications were not considered in great depth. The motivations behind the work lay more in studying the potential for such growth, rather than particular devices or future systems. Therefore when this project began most studies reported in the literature were concerned with simple epitaxial test layers of GaAs on silicon only. Nevertheless, they did clearly recognize the different strengths and the weaknesses of the two material systems, and some of the benefits of combining the best points of each. We will thus start by looking at some of the physical properties of GaAs and silicon, and relating these to both their electronic performance and their benefits in optoelectronic systems.

1.2 MATERIALS COMPARISON BETWEEN GaAs AND SILICON

Presented below is a table showing the main physical properties of both GaAs and silicon, at 300K derivedfrom references [Sze], [Wright] and [Landolt&Bornstein]. An interesting point is the higher apparent mobility (about 5 times) of GaAs *vis-a-vis* silicon, however, a clearer view is obtained from looking at the figure of carrier drift velocity versus field, reproduced below in Fig 1.1. Although the mobility of GaAs is, indeed, five times greater than silicon at low field it reaches a peak value at a field strength of $0.3V\mu m^{-1}$, while that of silicon continues to increase monotonically. As devices continue to decrease in size the high field region becomes increasingly accessible; for example, a gate width of 0.5μm at 1V operation will exceed the field at which GaAs has its maximum carrier velocity. In fact, due to pinch effects, the localized peak field will be even greater, thereby reducing the likely advantage to about 1.1 times for GaAs [Saul].

Table 1.1 *The main physical properties of GaAs and Silicon at 300K.*

	GaAs	***Silicon***
linear thermal coefficient of expansion ($°C^{-1}$)	6.86×10^{-6}	2.6×10^{-6}
atoms/cm^3	4.42×10^{22}	5×10^{22}
atomic weight	144.63	28.09
breakdown field (Vcm^{-1})	4×10^5	3×10^5
crystal structure	zincblende (non-polar)	diamond (polar)
density (g/cm^3)	5.32	2.328
dielectric constant	13.1	11.9
effective density of states:		
in conduction band Nc (cm^{-3})	4.7×10^{17}	2.8×10^{19}
in valence band Nv (cm^{-3})	7.0×10^{18}	1.04×10^{19}
effective mass, m*/mo:		
electrons	0.067	$m_l^*=0.98$
		$m_t^*=0.19$
holes	$m_{lh}^*=0.082$	$m_{lh}^*=0.16$
	$m_{hh}^*=0.45$	$m_{hh}^*=0.49$
electron affinity (V)	4.07	4.05
energy gap (eV)	1.424 (direct)	1.12 (indirect)
intrinsic carrier concentration (cm^{-3})	1.79×10^6	1.45×10^{10}
intrinsic Debye length (μm)	2250	24
intrinsic resistivity (Ω-cm)	10^8	2.3×10^5
lattice constant	5.653Å	5.431Å
melting point (°C)	1238	1415
minority carrier lifetime (s)	$\approx 10^{-8}$	2.5×10^{-3}
mobility (drift) (cm^2 /Vs)	$\mu_n=8500$	$\mu_n=1500$
	$\mu_p=400$	$\mu_p=450$
optical phonon energy (eV)	0.035	0.063
phonon mean free path (Å)	58	76 (electron)
		55 (hole)
specific heat (J/g-°C)	0.35	0.7
thermal conductivity (W/cm-°C)	0.46	1.5
thermal diffusivity ($cm^2 s^{-1}$)	0.24	0.9

vapour pressure (Pa)	100 at 1050°C 1 at 900°C	1 at 1650°C 10^{-6} at 900°C
diffusion coefficient (m^2s^{-1})	D_n=0.0220 D_p=0.0010	D_n=0.0039 D_p=0.0012
maximum electron velocity (ms^{-1})	$2x10^5$ ($3x10^5Vm^{-1}$)	10^5 (at $5x10^6Vm^{-1}$)
bulk modulus (10^{10} dyne cm^{-2})	75.5	98
Young's modulus (100) (10^{10} dyne cm^{-2})	85.5	131
Shear modulus (100) (10^{10} dyne cm^{-2})	32.6	51
Poisson's ratio (100) (10^{10} dyne cm^{-2})	0.55	0.28
cleaving	easiest along {110} planes due to slight ionic component in bonds	easiest along {111} planes

The reason for the peak in GaAs can be seen from the band structure figures for GaAs and silicon shown in Fig 1.2. An upper valley exists for GaAs only 0.31eV above the direct band-gap, into which carriers may be excited by high fields. Here they have a higher effective mass and a correspondingly lower velocity.

The above description applies only to electrons, and in the case of holes the velocity in GaAs is actually lower than that for silicon. This explains the lack of an equivalent to CMOS in GaAs technology, for p-channel devices would be slower than in silicon.

As electronic circuits become ever more highly integrated, with a greater density of devices, the high field region will continue to favour silicon. For example, silicon bipolar devices with a base width of 0.2μm are likely to be competitive with any bulk GaAs devices, although the position is complicated by GaAs/GaAlAs and other compound semiconductor heterojunction devices, which are discussed later on. Silicon' s other physical properties also aid its greater capacity for increased levels of integration. For example, its thermal conductivity is, at 1.5W/cm °C, three times greater than GaAs. Consequently, heat dissipation is better, which is a significant factor in high density, high speed circuits. Although GaAs has a higher melting point of 1415°C compared to 1238°C for silicon, the latter is actually better suited to withstanding high temperatures, for GaAs begins to disassociate at well below its melting point, becoming highly toxic. This could potentially pose a

significant problem and is recognized in the stringent safety procedures in growth systems such as MOCVD.

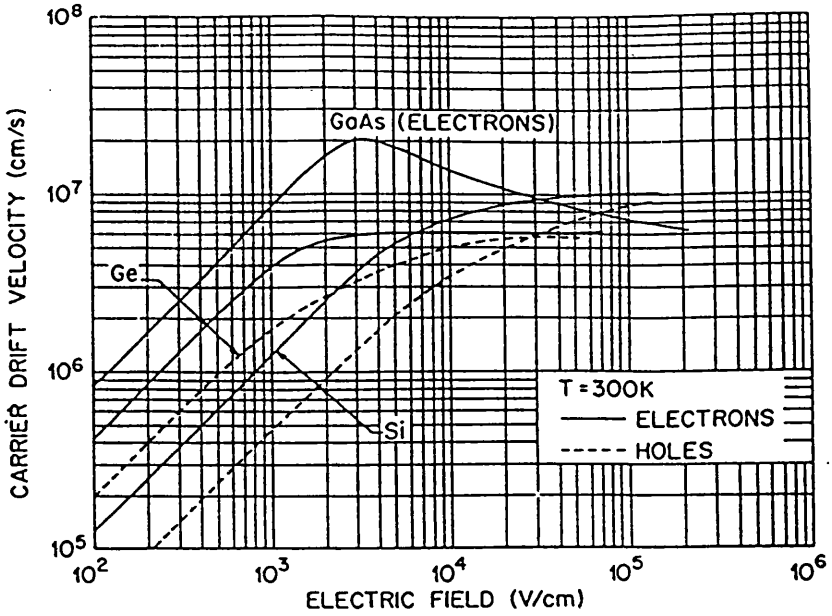


Figure 1.1 *Carrier drift velocity versus electric field for high purity GaAs, Si and Ge (after Sze)*

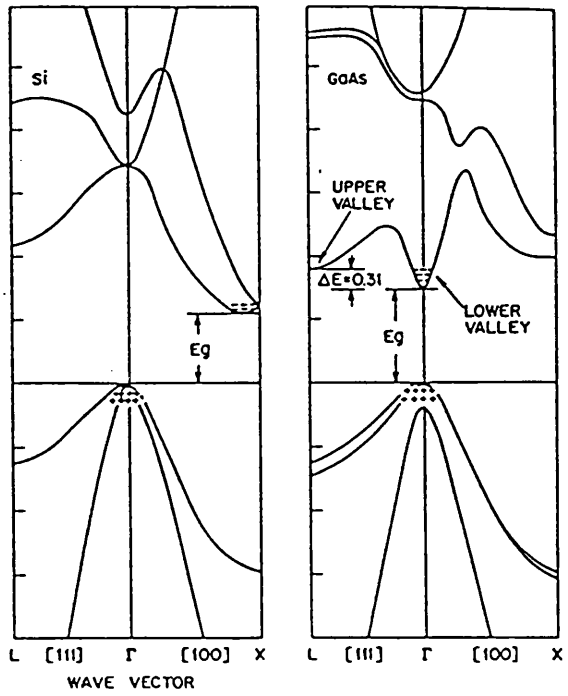


Figure 1.2 *Energy-band diagrams for GaAs and Si showing upper valley minimum for GaAs (after Sze)*

Also significant are the mechanical properties of the two semiconductors. Silicon, at 2.33g/cm^3, is less than half the density of GaAs (5.32g/cm^3). The advantages of reduced weight could extend from applications as diverse as space systems to highly portable microprocessors. The difference between the two is in fact further compounded by the greater strength of silicon, which allows thinner substrates to be used. This greater strength is also likely to maintain the current reliability advantage of silicon, particularly where large areas are required - either in the growth process, where large wafers can provide higher yields at reduced cost, or in increasingly large integrated circuits.

Whilst some of the advantages of silicon have been stressed, GaAs has the major benefit of a naturally occuring semi-insulating substrate, a corollary of its much lower intrinsic carrier concentration. The result is a reduction in parasitic capacitance, which increases speed and reduces power consumption. It has also made GaAs unsurpassed in its suitability for analogue RF applications, allowing propagation by low loss quasi-TEM mode rather than through the bulk of the 'lossy' semiconductor as would occur on silicon. The RF noise performance of GaAs is also significantly better than silicon. Furthermore, inductors can be fabricated and integrated onto GaAs, which is not possible on silicon. While much research has been directed towards the development of semi-insulating silicon substrates, through the implantation of insulating layers, or by deposition of silicon on sapphire, they are unlikely to become an alternative to GaAs in the RF analogue field. However, they could result in a useful reduction in parasitic capacitance for digital applications.

The greatest difference between GaAs and silicon is, of course, the nature of the energy-band structures, as shown in Fig 1.2 above. The valence band maxima for GaAs and silicon occur at the zero wave vector point (Γ), and the nature of the bands at this point control the simple hole conduction processes. The conduction band minimum also occurs at Γ for GaAs, but near the X point in silicon. Therefore the electron wave vector has finite magnitude and direction [100] for conduction electrons in silicon. The energy gap can be seen to be larger in GaAs than for silicon, therefore fewer carriers are thermally generated at room temperature, with the result that undoped GaAs is a better insulator than silicon. We have seen how this can reduce parasitic capacitance, but it also has the benefit of increasing the temperature at which thermally generated carriers exceed the intentional doping density, thereby increasing the operating range.

In silicon the difference in wave vector between the conduction band minimum and the valence band maximum means optical absorption and luminescence across the band-gap requires the participation of momentum conserving phonons. This process is thus intrinsically less efficient than it is in GaAs. For GaAs, three valence bands reach their maxima at Γ=0. Two are normally degenerate, and the third is split-off (Δ=0.34eV) to lower energy. The two degenerate bands have different curvature at Γ and therefore different masses, and are so known as the heavy hole and light hole bands.

The direct band-gap of GaAs, allowing efficient light emission, has opened up a whole host of optoelectronic applications unobtainable at present using silicon technology. Most dramatic of which has been the enormous success of GaAs-based semiconductor lasers. Recently there has been great interest in the strong photoluminescence shown by porous silicon, believed to be due to quantum confinement effects in the thin silicon wires. However, at this stage it is impossible to predict whether it can be used in practical devices, and so present an alternative to GaAs.

Another advantage of GaAs that attracted attention early on its development was its greater radiation hardness compared to silicon, although this would seem to be of minor importance in the great majority of applications.

In addition to considering GaAs and silicon in the context of discrete device performance it is important to look at their performance in large scale integrated circuits. It has become increasingly apparent that these are actually interconnection limited, and that the speed is largely independent of the basic transistor technology. Past performance projections based on straight-line log plots of packing density, speed, and processing power will cease to be valid. This is due to a number of inherent problems. Firstly, there is the physical problem of pin out, in which it becomes increasingly difficult to address with metal tracks all the required inputs and outputs on the chip. Successive generations of more and more complex ICs have attempted to ease this problem by combining the functions of several chips onto a single large one. However, these larger chips present their own problems of interconnectivity between different parts of the circuit within the chip itself, sometimes several centimetres in length. Considerable energy is spent charging and discharging these lines, whether inside or outside the chip, and as operating speeds are increased the problems of crosstalk and clockskew become severe. This may necessitate distribution of clock pulses by precise lengths of cable or

interconnect. The interconnects themselves may also be needed to support, cool, and provide power to devices. Interconnect performance depends on: the "connectivity", or ability to provide sufficient input and output connections; the propagation delay per unit length; and the bandwidth, sometimes specified as either the frequency bandwidth or the bit rate. Before showing how optoelectronic devices, in particular those using GaAs on silicon, will attempt to alleviate these problems it is worth concluding our comparison of the relative benefits of the two materials.

An engineering study should be almost by definition concerned with the most cost effective, efficient solution to a problem. But comparing the likely cost of future systems is notoriously difficult and unreliable. Nevertheless, a few useful comments can be made. Firstly, the inherent strength of silicon means larger wafers are always likely to be easier to fabricate than on GaAs. At present silicon wafers of up to 200mm diameter can be produced without reduction in quality, compared to a 100mm diameter maximum for GaAs. Larger areas result in greater yield and reduced costs. The expense of GaAs is further increased by raw material and refining costs - it being more difficult to produce. The difference in bulk material cost is presently about ten times. Even so, it could be argued that in either case the basic material cost is a minor factor in the cost of the finished product, particularly if one is concerned with highly complex circuits and systems.

Processing costs are difficult to compare due to both the far greater popularity of silicon, and its more advanced state of development. As packing densities continue to increase, costly precision techniques such as lithography have to be correspondingly advanced, whilst comparatively simple processing is used for GaAs where packing densities are generally lower. In the long term, processing complexities, and thus cost, are likely to be comparable. Probably the major factor in future cost is likely to remain the comparative market volumes, so that silicon is likely to have a significant advantage for a number of years to come.

We have so far only considered silicon and GaAs in their bulk forms, but a particularly powerful property of GaAs, and indeed most compound semiconductors, is the possibility of growing new materials combining more than one semiconductor in a series of heterogeneous junctions. Most important of these is the lattice matched growth of GaAs and $Ga_xAl_{1-x}As$. If the layers are thin enough it will result in important changes to the optical and electronic performance of the material due to quantum confinement

effects, these are described in more detail in Chapter 2. The result, however, is the ability to fabricate novel materials with the potential to develop new and exciting devices, such as the quantum well modulators described in this thesis.

That such structures can be grown is due to the advances in semiconductor growth techniques such as MBE [Cho] and MOCVD [Manasent] which were both employed for this research. The systems used are described in Chapter 3.2. The earliest observations of quantum confinement effects in semiconductors grown by these methods were in 1974 by [Esaki and Chang] and [Dingle *et al*].

The principle factors involved in matching different semiconductors together are illustrated in Fig 1.3 below. This shows the relationship between lattice spacing, band-gap and cut-off wavelength. The lines between points represent graduated compositions of ternary compounds. Similar lines between compounds without a shared element would represent quaternaries. Originally it was thought that only lattice matched materials were compatible, but it has been found that within certain limits strained layers can also be grown, indeed GaAs on silicon is one such strained material. Strained materials can further increase the range of materials available to the semiconductor designer, but there are also limitations, as discussed in Chapter 3.1.1.

It can be seen that both GaAs and AlAs have virtually the same lattice constant, so any combination of GaAs/ $Ga_xAl_{1-x}As$ can be grown. The corresponding range of cut-off wavelengths extends from about 590nm to 860nm. In order to access the wavelengths at which optical fibre systems are operated ($\approx$1.5μm) it would be necessary to use, for example, $In_{0.53}Ga_{0.47}As/InP$ [Chiu *et al*] [Geusic *et al*]. The lattice constants of these materials are too large to be grown on a silicon substrate, and they add a further level of complexity over and above that of GaAs/GaAlAs based materials. Their performance is also generally poorer. We can thus foresee a divergence in material systems. Firstly, those that are required for integration with long distance optical fibre communications, but not high levels of integration with conventional electronics; and secondly, those that may be used in free space, or short fibre-optic links, and which offer very high levels of integration when combined with silicon electronics.

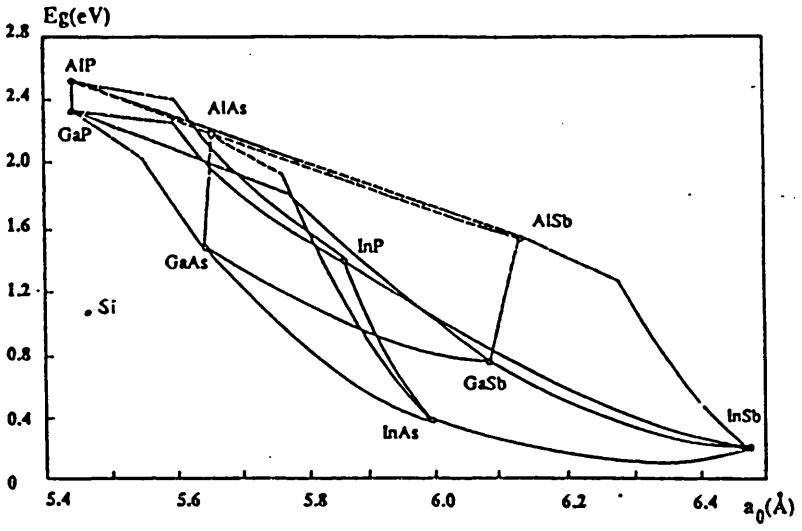


Figure 1.3 *Lattice constant v band-gap phase diagram*

Two types of devices employing ultrathin layers of more than one semiconductor have previously received the most attention - heterojunction transistors and semiconductor lasers. Quantum wells were incorporated in the active region of semiconductor lasers. Firstly, to provide a greater range of operating wavelengths, and secondly, to improve the efficiency by increasing the proportion of injected electrons and holes which occupy the lasing state. In a bulk laser there is an infinite continuum of energy levels with a parabolic density of states, therefore there is equal gain for both TE and TM modes. The lasing efficiency is not helped by the preponderance of injected carriers near the conduction and valence bands that do not actually contribute to the lasing wavelength, but serve only to increase the threshold current. By confining the electrons and holes in quantum wells they are restrained from having a wide range of momenta, since the band structure is divided into subbands with discrete energy levels. The heavy and light hole degenerate bands are also split, the heavy hole being predominantly TE, and the light hole primarily TM. This results in only the desired states being pumped, with a concomitant reduction in the threshold current. These improvements have been realised in commercial quantum well lasers both in the GaAs/GaAlAs material system and in $In_{0.53}Ga_{0.47}As/InP$ [Geusic *et al*]. It is important to note that there is actually a fourfold improvement from using quantum wells. Firstly, the *power* is increased due to the increased efficiency. Secondly, and for the same

reasons, the output will be more closely related to the drive current which means the *frequency response* or electrical bandwidth of the laser is improved. Thirdly, *chirp* which is caused by the modulating current, and is related to the ratio of change of refractive index to change of gain of the laser medium is reduced. Finally, the *linewidth* itself is reduced.

The problems with such lasers are in the thickness control of the layers and the growth difficulties, the sensitivity to temperature, and the reduction in saturation density caused by the wells. These have been largely overcome and the quantum well laser is likely to play an important part in many future optoelectronic systems.

Much interest in heterojunction transistors has been driven by a perceived weakness in the metal-semiconductor field effect transistor, or MESFET, which forms the basis of much GaAs electronics. This device relies on an n-doped GaAs channel, and, in order to increase the speed, this channel must be made as short as possible. Unfortunately, in addition to the reduction in mobility at high fields described in *Section 1.2*, the ionised impurities also begin to reduce the carrier mobility. The high electron mobility transistor (HEMT) [Drummond] addresses this problem by spatially separating the electron carrier supply region from the channel itself, which now need be only lightly doped. The carriers are provided from a highly doped GaAlAs layer which forms a heterojunction with the GaAs channel. The carriers from the doped layers fall into the potential well formed at the heterojunction interface, where are they free to move with very high electron velocities.

1.3 OPTICS AND ELECTRONICS

In this section it is shown how optics can be used to complement electronics, and that by the application of existing knowledge of the two technologies, a combination of the two should be able to exceed the limitations of either on its own.

1.3.1 Optics in Communications

In the comparison between Gallium Arsenide and silicon we mentioned some of the limitations found in electronic systems that were common to both

technologies, in particular the problems of interconnects. The optical properties of GaAs were also stressed, with the semiconductor laser being a particularly successful example of their application. It would thus seem worth examining the possible contribution optics could make to applications that are presently performed by predominantly electronic systems. Already optics are commonplace in telecommunications systems, for example in the use of lasers and optical fibres for transmitting data over long distances. Due to its almost unlimited bandwidth fibre has become the obvious choice transmission medium. Vast amounts of data can be transmitted in this way with very low loss, and with the introduction of fibre amplifiers, data can now be transmitted intercontinentally without conversion back to the electronic domain. Such an amplifier may consist of an Erbium doped fibre having an optical amplification window of around 30nm near the 1550nm minimum attenuation wavelength of the fibre. A 30nm optical window may appear quite small, but it is equivalent to 4000GHz or 13 times the whole electromagnetic spectrum from dc to mm wavelengths. At a lower level, fibres, or other optical waveguides, are already being used in rack-to-rack and board-to-board interconnects. These give sharper pulse edges than electrical interconnects, for there is very little degradation per unit length along the optical fibre, whilst in electrical interconnects resistance causes a risetime degradation that increases as the square of the linelength. An example of a waveguide interconnect is the 60GHz board-board optical interconnect of [Cheng *et al*]. This used polymer optical buses with microprism couplers between the GRIN waveguide buses and the boards. The S/N ratio was 22dB for an interconnect distance of 55cm. An advantage of using the polymer waveguide is that it can be laid down on any type of substrate e.g. either silicon or GaAs. The prisms allow coupling over a much larger wavelength range than, say, holographic elements - approximately 250nm compared to a few nm. However, a disadvantage is the precise adjustment of angle relative to the waveguide to achieve coupling. This is typical of the problems fibre or waveguide based systems have, and it is difficult to see how they could be more highly integrated - i.e. at the chip level. Alignment becomes increasingly tricky and the fibres themselves are too bulky, free space optics may therefore be able to contribute in this area. Nevertheless, the huge potential of fibres - or free space optical pathways - has yet to be fully tapped, for there exists no technology to switch or process the amount of data that could in principle be transmitted. Although currently optical communications are principally point-point, with a unidirectional signal from the transmitter to the receiver,

and at a single wavelength, this need not be true in the future. For example, by wavelength multiplexing (WDM) the amount of data presently transmitted could be increased by a factor of 1000 or more. Such a system could be unidirectional or bidirectional [Bornholdt *et al*] [Koch and Koren]. In the latter case different wavelengths, or groups of wavelengths, are used for the two directions. Bidirectional systems employing more than one wavelength offer the advantage of only requiring a single fibre whilst still providing low crosstalk between the receiver and transmitter. An optical grating would provide separation of the signals.

Coherent techniques used in radio communications could also be applied, but with a huge increase in bandwidth [Koch and Koren]. The system limitations then become not the fibre but the electronic network nodes and switches, it is thus worth considering whether optics can contribute to this area too.

1.3.2 Properties of Optics

In addition to the ability to transmit multiple wavelengths, or channels, simultaneously, light beams can also cross each other without the input and output beams being altered. This is in obvious contrast to the case of shorting two electrical conductors together. The result is to alleviate the restrictions on interconnect paths that are such a problem in integrated circuits. Furthermore, it opens up the possibility of new architectures, such as 2-d processing for which optics is particularly suitable, in applications such as image mapping and processing. Using the fact that light paths can crossover each other, their paths could be designed to be of equal length and thus eliminate clock-skew. This is helped by the theory which states that all paths in an optical imaging system (for example, in the simplest case, a single lens) have identical time delay or "timeskew". This feature could be used to provide an optical pulse for "clocking" purposes.

To utilize the instantaneous, wideband, 2-d input and output communications pathway conferred by optics would require imaging optics between the receiving and transmitting arrays. These could be provided by conventional lenses or, alternatively, holograms could be designed to perform the same function. There is however a limit to the number of interconnection patterns possible with such optics, and stray light could well be a problem. This would suggest a limit to the processing, rather than interconnect, role

optics could perform. Another limitation in terms of the potential for optical processing is that "light", or more accurately its wavelength, is actually quite large. This limits its potential for very high levels of integration even when compared to the best present day, sub-micron, electronic logic devices. Already 0.8μm CMOS electronics are commonplace, while feature sizes of 0.2μm are not far from the production process. Compare this to a focused optical beam which has a Gaussian spot of diameter 2w at its 1/e points, where $w=\lambda/\theta.\pi.n$ at far-field. If $\lambda/2$ optics are used to provide high quality images then θ is limited to 0.25rad [Midwinter 91]. Assuming the wavelength is 0.85μm and n is 1 (for free space) then w = 1.1μm, and the 1/e spot size is 2.2μm, already large compared to the feature size of conventional electronics. Moreover, if this spot was incident upon a receiver, it would be wise to double this to 4.4μm to ensure all the light was collected. Errors due to aberrations, alignment errors, and thermal changes may well require up to an order of magnitude increase in size to be certain of capturing the incident light, and to ensure that the light does not fall upon a neighbouring device. We are therefore presented with a much larger total device size than we are familiar with for individual electronic devices, although it remains small when compared with the conventional input and output bond pads currently employed for connecting chips. Clearly the extremely high levels of integration so common to us in electronics would be impossible in optics, thus if optics are to be of benefit it will not be by replicating electronic systems, but rather by complementing them or by bringing new functionality, perhaps by special architectures.

Essentially optics provide a transmission medium which, at the distances involved in electronic systems, is without loss, crosstalk, distortion and is speed independent. Optics also provide protection against electromagnetic interference, and isolation between different parts of the circuit. A feature that is already found to be useful in simple opto-isolators, stopping the load on one part of a circuit affecting the operation of another.

By comparison, electrical interconnects at high speed suffer from increased losses, pulses are distorted and may be reflected, and crosstalk and clock-skew become problems. At high speed the energy required to transmit data also increases, as the tracks have to be charged and discharged, which in itself requires the further complication of line drivers. An example of the methods one could use to alleviate these problems using conventional techniques is the Thermal Conduction Module [Arjavalingam & Rubin]. This provides interconnections for 100 chips, with 96 connections/chip, in a 90mm

square, 5.5mm thick device. Sixteen wiring layers are required, sandwiched by ceramic laminates, with a wiring density of 2/mm/layer. The module also provides fan-out, power supply distribution, and impedance and coupling control. The intention in such a design is to locate the chips close together, reducing the interconnect lines and propagation delay times. Although the multilayer wiring structure is unusual the interconnects themselves are conventional, giving a propagation delay of 10pS/mm and a risetime of ≈1nS. An alternative interconnect is high speed cable which, although too bulky at the required levels of integration, may be used between modules or cards. Typical performance would be a delay of 3.8pS/mm and a risetime of ≈200pS. Note that the delay is actually less than that for optical fibre having a refractive index of ≈1.5 which would result in a 5.0pS/mm delay, although with negligible rise time. The benefits of optics are not therefore related to the propagation delay itself. In fact comparable propagation delay can be achieved with electrical interconnects having linewidths of as little as 10μm, for instance copper microstrip insulated by a polymer having a low dielectric constant, such as polyimide, also has a propagation delay of 5pS/mm [Arjavalingam & Rubin].

Electrical reflections pose increasing problems as the demands on a system become more severe. These occur when the signal encounters a change in impedance or a discontinuity, for example signal line connected to cable, or the effect of nearby lines locally reducing the signal line's impedance. The discontinuities may be inductive or capacitive. The reflections themselves may be either positive or negative. If one succeeds in reducing the interconnect lengths by judicious redesign, it will as likely as not result in the problems of reflection becoming more severe due to the small delay. For example, consider a signal on a 50Ω transmission line encountering a 1pF shunt discontinuity. If it is a 1V signal with a 1nS risetime the reflected signal will be ≈25mV; with a risetime of 0.5nS this increases to 50mV. It can be seen that as the speeds increase reflections are likely to cause false switching. Coupled noise (unwanted signals from adjacent active interconnects) can also create similar problems. Compare this to the optical case in which light beams can cross each other without the outputs being affected.

Another form of noise that can cause problems is Delta-I noise. This is a voltage disturbance that occurs when numerous circuits switch simultaneously causing large changes in current, predominantly through the power distribution network. Because of the high currents required to drive transmission lines (20mA to drive a 1V signal in a 50Ω line) the simultaneous

switching of many drivers can cause amps of current to change direction in a few nS. With package inductances of tenths of nH, hundreds of mV of noise are possible, which could well cause false switching. Optical paths would act as isolators reducing the likelihood of switching errors.

We have seen how electronic devices have not been able to reach their full potential because of the problems of interconnectivity, both in terms of architecture and purely electrical limitations. It has also been discussed how optics is a particularly suitable transmission medium. It would thus seem sensible to examine in more detail what benefits a system of complementary technologies may have, and how such a system could be constructed. There are a number of factors involved in the performance of a processing system - the speed of the gates or devices themselves, the number of such devices required for a particular function, and the connectivity or processing algorithm. The basic measure of performance will be the cycle time necessary to perform fundamental operations. The interconnections have been seen to alter the cycle time, by preventing the devices operating at their maximum potential.

Although optical components could perform some useful processing functions, for example wavelength multiplexing and demultiplexing by gratings, or the use of couplers and conventional optics in routing data, there is no known way of performing the complex logic functions that are so familiar in electronic systems with anything like the same efficiency. Using electronic logic, discrete gates having switching energies of 10fJ to 1pJ, and speeds in the nS to low pS range, are familiar. Optical switches are by comparison very energy consumptive. An alternative is the use of an optoelectronic device such as the Multiple Quantum Well modulator which, for a 10μm diameter device, would have a capacitance of ≈0.01pF, giving at 3V Q=0.03pC. Assuming a responsivity of 1A/W, the device would require an optical input of 0.03pJ [Miller 87 & 89]. These devices will be discussed in more detail later on, the point to note here is that they require energies similar to electronic devices, because in essence their operation *is* electronic.

1.3.3 Energy Comparison of Electrical and Optical Interconnects

An interesting comparison has been made by [Hinton & Miller] with regard to the energy requirements of both electrical and optical interconnects

between electronic circuits. At the core of this comparison is the recognition of the essential duality of light. Its wave nature gives it the properties of an excellent transmission medium, and the ability to image and route two dimensionally. Conversely, its particle nature results in very efficient conversion between the optical and electronic domains. In fact, a single photon can optically excite and free an electron so that detection can fundamentally be with 100% efficiency. This has been termed Quantum Impedance Conversion, for reasons that are clearer when one compares the equivalent case for electrical transmission. Here the metal conductor appears as either a capacitance to be charged and discharged, with power consumption increasing with both modulation frequency and track length, or as a transmission line with a characteristic impedance. The first case requires that a wire or metal track be charged to the operating voltage every time a bit of data is transmitted, using total energy $E=CV^2$, or $1/2CV^2$ for the energy stored in the charged capacitor, and the same amount for dissipation in the resistance during discharging. In a lossy conductor signal diffusion along its length results in delay, typically 0.1nS/cm. To reduce time delay low impedance tracks are desirable, but the requirements of the electronic circuits dictate the use of low current, high impedance devices. Consequently, there exists an impedance mismatch between the tracks and the electronic devices. Note that even if a suitable superconductor existed capacitance would remain, the link looking like a stripline, and the connector would reflect unless matched. The use of an optical link would act like an impedance transformer, allowing very high impedance electronic devices to be used.

As an example Miller takes the charging of an electrical line of length 30cm to a voltage 1V. This would require approximately 20pJ, which is 1000 times greater than an electronic switch would require. On the other hand an optical path would not consume any measurable energy itself, although of course it is necessary to consider the whole interconnect, i.e. the additional requirements of the transmitter and the detector. In the case of the transmitter a low power light source is necessary. This could be either a low threshold microlaser which would operate as the transmitter itself, or an external laser could be used with a reflection modulator on the chip acting as the data transmitter. The detector could be a conventional *pin* diode or, as we shall see, a dual-purpose modulator that may operate as either transmitter or detector. The key issue is how much energy such an optoelectronic interconnect would use.

For a photodetector the minimum optical energy required to generate a voltage change V is [Miller 89]:-

$$E = \frac{\hbar\omega VC}{\beta e} \qquad \textbf{Eqn. 1.1}$$

where β is the quantum efficiency, C is the capacitance, e is the electronic charge and $\hbar\omega$ is the photon energy. Such a detector could operates at, or near, the quantum limit of one electron per incident photon. Similarly, an ideal emitter should emit one photon per excited electron. Lasers can operate very efficiently at high currents, but they first have to overcome the lasing threshold current. They must also be able to operate efficiently at low powers. This puts great demands on the laser design, and although microlasers are making great advances through the use of smaller gain volumes and higher reflectivities, it may be better to look to optical modulators to provide the required levels of integration, efficiency and energy consumption. These devices, which may also function as detectors, modulate an external light source by the absorption of photons. For each photon absorbed an electron flows, so we have exactly the same "quantum impedance conversion" as described for the photodiode. The energy required by such a device, if it was also in the form of a *pin* diode, would be the energy to charge the capacitance, CV^2; and the energy associated with the photocurrent generated, which is proportional to the incoming optical power.

Given that a high enough level of integration can be achieved, and if the device size is small enough (10 x 10μm), then Miller calculates that the breakeven point at which an optical interconnect would require less energy than an electrical one would be for distances greater than ≈1mm. Below this length metal tracks provide low energy, wide band communications; above it optical interconnects use less power and have a greater bandwidth. In both cases the *propagation* delay is similar, but signal diffusion proportional to the track length occurs for the electrical signal slowing the transmission rate. Because optics does away with the problem of impedance mismatch it would retain its advantage even if one had superconducting electrical lines. If the breakeven value can be achieved then the potential exists for use of optics on an intra-chip as well as an inter-chip level. At this level of integration one can imagine the optical interconnection of electronic islands, preferably utilising the advantages of two-dimensional architectures. The optical interconnects would release the full performance potential of electronic devices, whilst bringing greater flexibility in the ways they could be connected, the electronic

islands still performing the basic logic functions. Such a system is illustrated schematically in the figure below.

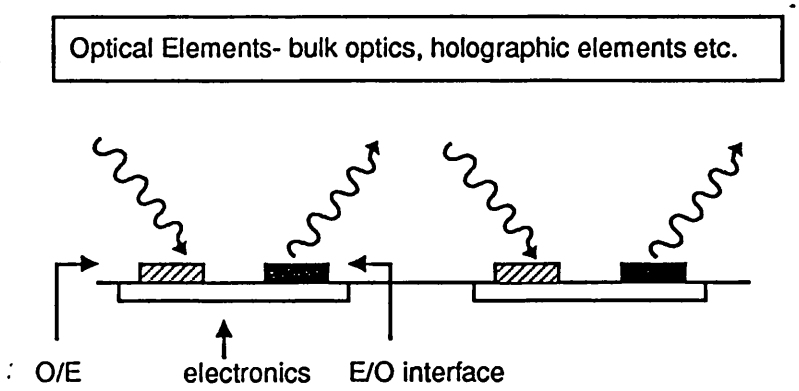


Figure 1.4 *Optically interconnected electronic islands.*

1.3.4 Potential Devices for Use in Electronic Islands with Optical Interconnects

Whether such a system as proposed above would be practicable is to a large extent dependent on a means of providing both the high levels of integration required and an adequate level of optical performance. The GaAs on Silicon asymmetric Fabry-Perot quantum well modulator would be a particularly attractive device for such an application for the following reasons:-

i) We have seen how silicon electronics are likely to remain the preferred choice in the majority of digital applications in the future;

ii) Electronic systems are presently limited by the interconnect technology and not the fundamental electronic device performance;

iii) GaAs based semiconductors have optical properties that silicon does not possess;

iv) The asymmetric Fabry-Perot modulator is a most promising device to provide both the necessary optical performance and the low energy requirements.

v) Growth of GaAs on Silicon modulators would satisfy the final requirement for high levels of integration, bringing optics into the intra- and inter-chip domains.

The basic properties of quantum wells and the operation of the asymmetric Fabry-Perot quantum well modulator (AFPM) are described in Chapter 2. It would be useful, however, to summarize the key points at this stage. For quantum wells the optical absorption spectrum shows a clear series of steps, resulting from the confinement of electrons and holes in GaAs "wells" by GaAlAs "barriers", with the layer thicknesses being ≈100Å. At the edges of the steps the absorption is enhanced by excitonic effects, which are observed at room temperature due to the confinement in the wells. Application of an electric field shifts the optical absorption edge, including the exciton absorption peaks, to longer wavelengths. As a result one can fabricate a semiconductor electroabsorption modulator. Furthermore, the performance of such a device can be enhanced by enclosing it in a Fabry-Perot resonator (see Chapter 2.4), resulting in a measured 20dB contrast ratio and a change in reflectivity of 43% at 9V [Whitehead *et al* 89(1)].

The electric field can be applied by locating the quantum wells in the intrinsic region of a *pin* diode which is then reverse biased. The energy required to modulate the light beam is $1/2\ CV^2$, where C is the device capacitance and V the operating voltage. This results in energies of $fJ/\mu m^2$ which are of the same order as electronic devices. Let us now consider the energies associated with the absorption process itself. The power dissipation in these absorptive modulators consists of *intrinsic* and *non-intrinsic* contributions [Woodward *et al*]. The first is simply the absorbed optical power. The second results from the work done in moving the photogenerated carriers through the applied electric field. This photocurrent is essentially a parasitic effect if one is interested only in optical absorption modulation. Minimizing the dissipation would result in a greater device packing density and maximize the allowed optical input power. For example, consider a MQW modulator operating at 5V absorbing a single photon. The intrinsic energy is approximately the band-gap energy (≈1.5eV), while the non-intrinsic energy is 5eV, the work done as the electron traverses the field. The latter thus dominates the dissipation at moderate values of bias, while the two are comparable in value even at zero applied bias due to the built-in field. The only way to reduce the dissipation is to prevent the carriers moving under the influence of the applied field. Even when no external field is applied the built-in field due to the MQW *pin* structure results in an electron velocity of about 10^7cm/s for a 1μm intrinsic region. It thus takes an electron about 10pS to traverse the intrinsic region and another 1-100pS to escape from the quantum well. This compares to a carrier lifetime in good material of >1nS which,

being much larger, means that the carriers will always manage to traverse the gap. One could increase the carrier escape time by deepening the wells, but this results in a reduced saturation intensity and slows the potential operating speed of the device. The other option may therefore be to reduce the carrier lifetime - for example by controlled proton implantation; deep level impurities, e.g. O; or the introduction in the growth process of excess As. The same effect is sometimes observed with GaAs on Si due to the dislocations found in this material, although this is often perceived as a disadvantage due to the adverse effect it has on laser performance. Consequently there is a performance trade-off between carrier lifetimes and optical performance. The same trade-off is observed for proton implantation - for a dose of $1x10^{13}cm^{-2}$ absorption modulation is maintained, with only a slight broadening of the exciton, beyond this the modulation performance is reduced [Woodward *et al*]. Of course proton implantation is a more flexible and selective method, and may be applied post-growth. Experimental results show that at 4V the quantum efficiency was ≈1 for unimplanted devices, but fell to 35% for a dose of $1x10^{13}cm^{-2}$ [Woodward *et al*]. The quantum efficiency is reduced due to a reduction in the carrier lifetime, which in turn results from the introduction of a large number of non-radiative recombination centres by the proton implantation. As the bias is increased the quantum well escape time and the traverse time are reduced, thereby reducing the likelihood of non-radiative recombination and increasing the quantum efficiency. What was previously seen as a detrimental quality, i.e. a low quantum efficiency, is thus observed to have some potential advantages and it is useful to keep this in mind when assessing the photocurrent spectra of MQW structures.

The reduction in energy dissipation is accompanied by an improvement in saturation intensity, for fewer carriers build-up across the device, reducing space-charge effects. By connecting two modulators in series, one implanted, the other unimplanted, optical gain has also been demonstrated [Woodward *et al*] which may prove useful for fanout and improved drive capacity.

The successful integration of an asymmetric Fabry-Perot quantum well modulator device with silicon would therefore represent a substantial step towards meeting the requirements for an optoelectronic interconnect described above.

1.3.5 Packaging Considerations

The trade-off distance at which optical interconnects would be favourable is clearly dependent on the size of the devices, which in turn requires a great deal of attention to be paid to the design and fabrication of the complete system.

The fabrication of a complete package would require additional optical components such as lasers, mirrors, lenses and holographic elements. It is worth looking at some of the progress that has been made in these areas, particularly the integration of various devices. Much of the motivation for research has come from the needs of long distance optical communications, rather than the possibilities for the future discussed above. This, however, is not unexpected as a more immediate need is being addressed, and it does not necessarily affect the conclusions that can be drawn. Indeed, processing the huge amounts of data that could be transmitted by fibre would be a key requirement of future systems. Whichever approach is taken the greater complexity of systems will demand higher levels of integration for reasons of cost, robustness, and isolation/coupling. We will now discuss some of the devices that may be used in such systems.

1.3.6 Characteristics of Modulators vis-a-vis Lasers

One example is that of the integrated laser and optical modulator. In a directly modulated laser chirp occurs, a wavelength shift causing dispersive signal distortions. This occurs to a lesser extent in quantum well modulators, therefore a combination of a constant power laser modulated by a quantum well device may have advantages. However, the modulator itself may create some degree of phase modulation. This is because it makes use of electroabsorption - the change in optical absorption coefficient α with electric field - which is related to the imaginary part of the index of refraction by:-

$$\alpha = \frac{4\pi\, n_{imag}}{\lambda} \qquad \textbf{Eqn. 1.2}$$

The Kramers-Kroenig relationship links n_{imag} and n_{real}, therefore a change in α results in an electrooptic effect. If Δn is large, phase modulation would occur in the modulator output, a similar effect to chirp in directly modulated lasers. Conversely, such an effect could be useful in constructing phase

modulators or couplers. In fact calculation of Δn by the Kramers-Kroenig relationship from MQW electroabsorption spectra show that the effect is relatively small in the region of high absorption changes, i.e. near the exciton peak, but larger at longer wavelength where the background absorption is smaller. Another parameter that concerns phase modulation is the linewidth enhancement factor, α_{LEF}, given by:-

$$\alpha_{LEF} = \frac{\Delta n_{real}}{\Delta n_{imag}} \qquad \textbf{Eqn. 1.3}$$

Which would be zero for a purely absorptive medium and infinite for a purely electrooptic one. Measured values have been reported as equal to 1 for MQW modulators, and 3-6 for directly modulated lasers [Wood]. This indicates that the modulator will show less phase modulation.

Chirp may not be of great importance over short distances but the use of a separate, single laser with a number of modulators is attractive for other reasons. This is an important issue on which there is at present no common consensus, for some would argue that thousands of microlasers would be more suitable in an optoelectronic system than would the MQW modulators. The laser is a low impedance, current driven device, the source being shunted by the laser's contact and substrate resistance, perhaps 3-10Ω. In a simple approximation it is this resistance that gives the R in the frequency response $1/2\pi RC$ [Wood]. On the other hand an MQW modulator is a high impedance, voltage driven device, and the R in the frequency response is that of the drive source, perhaps 50Ω. The effect of parasitic capacitances will thus in general be much less severe in the case of lasers. However, the capacitance itself may be less for modulators, because they can be more easily reduced in area (although the latest VCSEL microlasers may negate this advantage); and because they are operated in reverse bias. This effectively increases the "plate separation" in the parallel plate approximation of the device capacitance, due to the increased depletion width. A similar effect can be achieved by physically increasing the width of the intrinsic region, but this reduces the field and therefore involves a trade-off with increased operating voltage in order to maintain the same modulation performance.

The benefits of modulators are, however, significant. Firstly, integration of lasers on silicon is more difficult than modulators due to material problems discussed in Chapter 3. A laser of relatively high power could be mounted off-chip where its design need be less compromised. It could, for example, be a quantum well semiconductor laser operating well

above threshold, it would therefore be more efficient than thousands of microlasers on-chip, each with its own threshold current requirement. The off-chip laser could be of virtually any design or orientation, whilst those on-chip would need to be vertical cavity surface emitting lasers (VCSELs). The off-chip laser would also be operating at constant current, therefore without chirp, and would be able to dissipate heat away from the chip. Reliability would also be a major factor, a single off-chip laser operating at constant current is likely to be more reliable than thousands of microlasers operating at very high switching speeds. If a fault was to develop replacement may be possible with a single off-chip laser but would be impossible with integrated lasers.

Of interest to either approach may be the phase locking of two dimensional arrays of quantum well VCSELs, demonstrated in the InGaAs/GaAs system by [Orenstein *et al*]. A 27x27 array was fabricated by patterning the reflectivity of the laser back mirrors. This both defines the array elements and allows interelement coupling. This coupling phase-locks the lasers into a single coherent spatial mode, useful as a high brightness source or in beam steering applications. This may allow some degree of reconfigurability to the optics. The devices are similar in construction to the AFPM, having a quantum well region sandwiched between two epitaxially grown Bragg mirrors. The lower one containing 20 GaAs/AlAs layers, and the top reflector 12 periods plus the patterned metal layer.

An alternative approach to the AFPM, which uses absorption modulation, is to consider phase modulation in a MQW, this may also be useful in beam steering applications. The conventional approach is to operate well away from the band-gap, on the long wavelength side, so as to reduce absorption. Then the change in refractive index, linked to the change in absorption by the Kramers-Kroenig relationship, changes the path length and thus the phase of the optical beam. However, because one operates at a region of low absorption the changes in refractive index tend to be weak, this usually requires the use of waveguide geometries in order to obtain adequate modulation. A novel approach is to use the vertical geometry of an AFPM [Pezeshki *et al*]. The equation governing the total reflectivity of the AFPM at resonance is given by:-

$$R_T = \left[\frac{\left(\sqrt{R_f} - \sqrt{R_b} \right)}{\left(1 - \sqrt{R_f R_b} \right)} \right]^2 \qquad \textbf{Eqn. 1.4}$$

$$\text{where } R_{b'} = \text{effective back reflectivity}$$
$$= R_b e^{-2\alpha l}$$

The absorption is varied until R_T goes through a minimum equal to zero, at which point the front reflectivity equals the effective back reflectivity. On one side of the matching condition the loss due to absorption is too low to balance the equation, on the other too large. However, the reflected beams to the left and right of the matching condition differ in phase by 180°. This is because R_f and R_b are out of phase, and R_f dominates when the absorption is high and R_b dominates when the absorption is low. At a particular applied bias, and thus change in absorption, it is possible to change phase whilst maintaining a reflectivity of constant optical intensity. Large phase changes with low values of applied bias are thus possible. The disadvantage of this approach, using absorption changes to produce a phase change, is the insertion loss, although this will be comparable to AFPM absorption modulators. It is important to note that in a conventional AFPM there will also be some phase change, although as one is not *crossing* the matching point it will be greatly reduced. It has been estimated by [Pezeshki *et al*] to be ≈20°. This would still result in less chirp than waveguide devices.

We previously discussed how wavelength multiplexing could vastly increase the quantity of information transmitted. A step towards such a system is an integrated wavelength demultiplexer receiver, which has been demonstrated in GaInAsP/InP [Bornholdt *et al*]. This used two wavelengths routed by an integrated symmetric directional coupler. It may well be that the MQW could also be used as a wavelength demultiplexer since its responsivity is governed by the bias-dependent absorption spectra. One could then operate it as a voltage tuneable, wavelength dependent photodetector.

1.3.7 Integrated Waveguide Structures

While figure 1.4, above, shows free space optical interconnects, which would be in two dimensions, the use of optics could actually be extended into three dimensions by introducing optical waveguides in the plane of the electronic islands. These waveguides would be an almost direct optical analog to metal tracks. At present free-space optics and waveguided optics remain on the whole separate fields of research, this is, however, principally due to the

enormous amount of work still to be done in either area. In the future these technologies are likely to prove complementary, so it is worthwhile looking briefly at waveguide integrated optics and how they may relate to future optoelectronic systems.

The waveguide used may typically be a buried heterostructure in which the light is tightly confined by two semiconductors of different refractive index, and the dimensions may be ≈0.2x1μm wide. The loss per cm is only a few percent per centimetre of propagation distance, and would therefore not be a problem within an integrated circuit. The waveguide can also be absorbing, in which case it is termed active, and may then be used to form a modulator or laser within the plane of the chip. The use of corrugated waveguide gratings (or Distributed Bragg Reflectors) as laser cavity resonators eliminates the need for cleaved facets, and has led to the distributed feedback laser. The same type of gratings may also be used as filters in multiple-wavelength systems. By injecting a current across the DBR one can create a change ΔN which will change the reflectivity band.

An example of what can be achieved is the Multisection MQW-DBR laser [Koch and Koren] This has an output of 20-30mW, a minimum $\Delta\lambda$ of 1-2MHz, and allows 1GHz tuning (80Å) at 1.53μm. Such a device offers the potential for multichannel, coherent networks with quantum limited detection sensitivity. These channels could be detected, filtered and then routed to the processing optoelectronics, all by waveguide technology.

Integrated waveguide devices are now also being made using silicon technology. An example is the narrow band Bragg reflection grating made with phosphorus doped silica on silicon waveguides, demonstrated by AT&T [Adar *et al*]. This functions as a narrow band optical filter which may have applications in multichannel optics, for example wavelength division, optical feedback, and laser stabilization. If we return to the concept of electronic islands, located on silicon motherboards, and interconnected by 2d optical arrays, we may want to consider expansion and interconnectivity with other processor arrays. At this level fibres would be an obvious choice, and the silicon-based reflectors and waveguides can be matched to these, with reflectivities of up to 60% giving bidirectional links. Thus communications signals could be fed directly into the motherboards, distributed by silica waveguides, and processed by 2d optoelectronic arrays.

1.3.8 Self Electrooptic Effect Devices

To take a step nearer the system in Fig 1.4, consisting of two dimensional electronic arrays with free space interconnecting optics, it would be useful to first research the properties of two dimensional arrays. One approach is to build a 2-d array having optical inputs and outputs only, i.e. to dispense with the electronic processing stages. This brings the fabrication to within the limits of present day technology, and also allows the properties of 2-d arrays to be better understood, so that the appropriate electronics can then be designed. Such a system has been constructed using SEEDs (Self Electro-optic Effect Devices). The simplest form of such devices is shown below.

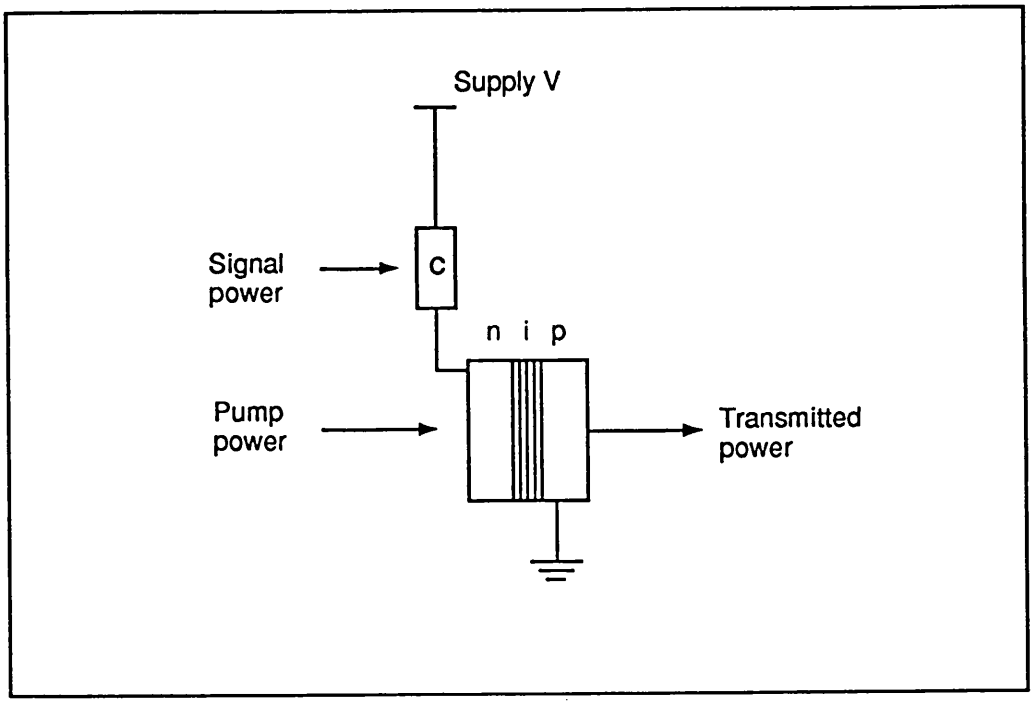


Figure 1.5 *Diagram showing the operation of a basic self electro-optic effect device (SEED).*

In the figure above C may be a photodiode, a phototranistor, another MQW modulator, a FET, or even simply a resistor. In the latter case there is no separate signal power beam, there being a single input beam incident on the *pin* MQW modulator and a single output. The wavelength chosen is that of the excitonic peak of the quantum well modulator in the unbiased state. Imagine that there is initially no light incident on the MQW diode, then all the supply voltage will appear across the diode as there is no current flowing in the circuit. When one begins to shine light on the diode a current will flow,

causing a voltage drop across the resistor, hence reducing the voltage across the diode. This leads to an increase in the absorption of the MQW diode, increased photocurrent, and so on, in a positive feedback loop until the voltage across the diode can get no smaller. We thus have switching into a high absorption (low transmission) state. The reverse process also occurs leading to a bistable device, having either low or high transmission. Choosing a photodiode instead of a resistor gives an extra degree of control *via* the second optical input beam, and results in improved performance [Miller 90].

A more sophisticated form of the device is the S-SEED, or symmetric-SEED, which consists of two MQW *pin* diodes connected in series, so that each node has two optical inputs and two optical outputs. When one diode is 'on' the other is forced 'off', i.e. one is absorbing and the other is transmitting. The device is bistable, and its state is changed by the ratio of the two input beams, and not by the absolute beam intensity. This is likely to result in more reliable operation as attenuation of the beam is less critical.

Although having both optical inputs and outputs these are still optoelectronic devices. SEEDs have been operated at 35pS switching times, and the limit is, perhaps, 1pS or less. They are far too energy consumptive at present for large systems, but they are ideal for exploring 2-d arrays, and have been used to demonstrate switching systems [1.106]. These could point the way forward in which a complete optoelectronic island array could be developed. For instance, by integrating a transistor to provide gain with the SEED device, the optical power required is reduced, and the benefits of electronics and optics demonstrated. In the future we can expect to see intense research into the exact types of architecture which would be most beneficial, and the optical devices that would be most appropriate. It seems likely, however, that an efficient optical modulator would play a key part in such a system and that integration on silicon would be a desirable option.

1.3.9 Optoelectronics in Switching Systems

We will now consider how optics and electronics may complement each other in the field of communication systems. In these, multistage networks are required to switch the transmitted data so that they are effectively routed from the sender to the addressee. Such a network is illustrated schematically in Fig 1.6, illustrating a generic network connecting N inputs to M output channels. This type of network would not only be used in

telecommunications but also in a parallel computer to link processors, memories, and I/O controllers. Multistage networks have been found to be best at reducing bottlenecks and prohibitive complexity (the other architectures that may be used are bus and crossbar). Some systems employ self-routing, by which the packets of data, each having an address header, can find their way through the network. These have the potential for both high throughput and rapid refiguring, but imply the use of distributed logic throughout the switching system. Each node of the network reads the address and sets its switch accordingly, either passing it straight through or "exchanging" it. Of course this must be done before the arrival of the data itself, or if not, at least a facility for buffering the data must be provided. The simplest 2x2 switch is illustrated in Fig 1.7. A row of such elements may form a stage, and a number of stages forms a network. The digital logic to perform the decoding and switching must therefore be very fast and efficient, which suggests the use of electronics. However, a number of problems are encountered in these systems: clockskew, limited pin-in/pin-out, physically large systems, and electrical signal crosstalk. The ideal transmission medium for such large quantities of data is optics, so once again the preferred solution may be an optoelectronic one consisting of electronic islands controlling the optical switching of data.

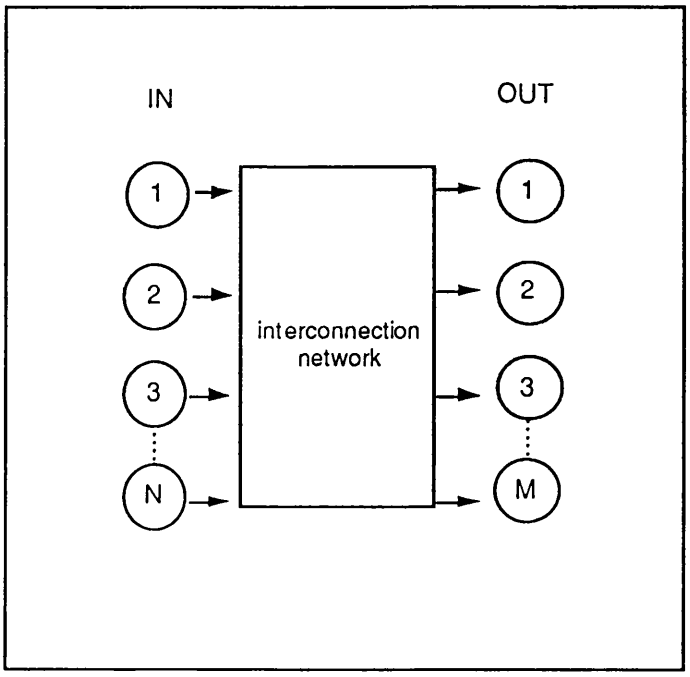


Figure 1.6 *NxM interconnection network*

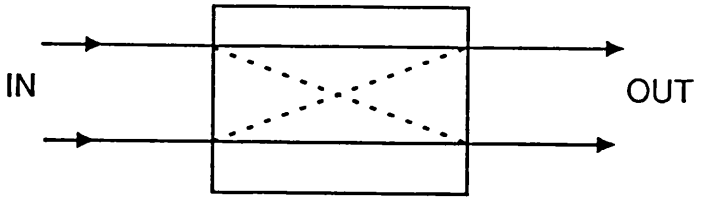


Figure 1.7 *2x2 switching element*

Various technologies have been proposed for the switching of optical data streams. For example, four port directional couplers have been demonstrated in Lithium Niobate, in which power crosses over depending on the phase relationship of the two waveguides, which is in turn controlled by voltage applied to two electrodes. These devices typically have large capacitance and require 5 to 20V to switch, the drive requirements therefore present a problem. Moreover, they also presently suffer from large attenuation, crosstalk, and are slow to reset, requiring 3 to 6 nS. Increasing the number of ports results in exceedingly complex devices to fabricate, the present state of the art being a 128x128 device built from 4x4 blocks [Burke *et al*]. Because such devices retain the data signal in the optical domain they have enormous potential throughput of data, but the reconfiguration times are slow. They would therefore seem more suited to routing large blocks of traffic, rather than sorting small packets of data.

An alternative technology is that using MQW modulators, which retains all the advantages of scale and integration provided by conventional semiconductor technology. The level of electronic intregration could range from a simple resistor if R-SEEDS were employed, in which the switching is a function of the incident optical power, to an electronic logic circuit decoding the address and hence controlling an AFPM modulator. Either approach would be ideal for 2-d arrays of sources and receivers, using microlenses and/or holographic lenses for the free space imaging.

A detailed comparison of two theoretical packet-switched synchronous multistage interconnection networks, one using optoelectronics, the other CMOS VLSI, is given in [Kiamilev *et al*]. It is worth highlighting the main findings here and comparing them to our previous discussion. The

optoelectronic system was designed along the lines described above, and assumed a high degree of integration between the MQW devices and the silicon electronics islands i.e. a GaAs/Si approach with transmitting and receiving modulators, and free space imaging optics. The key performance issues in such systems are the speed, the system throughput (the speed times the network size), the power consumption, and the floorprint area. The most appropriate, but functionally equivalent, topologies for the two technologies are the 2-d shuffle for optoelectronics, and the Banyan for electrical interconnects, which minimizes the number of wire crossovers, and is more efficient in terms of power consumption and footprint area.

An 8x8 Banyan switching network is shown in Fig 1.8. It is built from 2x2 switching elements, in three stages, each of which works on subsequent bits of the destination address. The data is routed to the upper output if the switching element sees a 0, and the lower output if it sees a 1. By following the paths through it can be seen that the data will find its destination regardless of the input it uses. A number of assumptions were made for the CMOS VLSI implementation.:- the elements would be arranged in rows; two layers of interconnect would be used, one for horizontal paths, the other for vertical paths; and all the elements would be integrated on one chip. In current systems many chips are often interconnected by transmission lines. These may have faster propagation rates, but have problems of ground loops, crosstalk, reflections, and high power consumption. The process assumed was 1.2μm 5V CMOS with a minimum feature size of 0.6μm, the wire pitch was taken as 2.4μm with a capacitance of 2pF/cm and a resistance of 375W/cm. The power consumption of the network envisaged is a function of the number of gates operating, the clock speed, and the energy charging and discharging the wires.

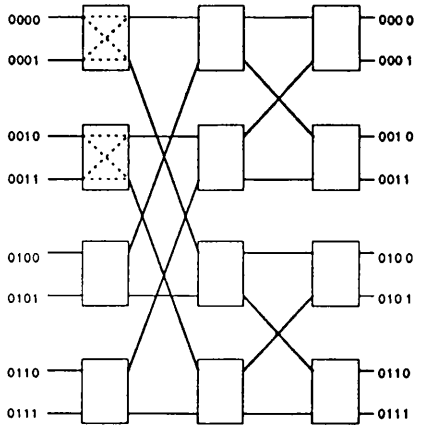


Figure 1.8 *8x8 Banyan interconnect*

The optoelectronic implementation assumed 5μm x 5μm MQW modulators integrated with Si CMOS electronics, operating at a wavelength of 850nm and with a 5V drive voltage. The modulator may appear optimistically small, given some of the problems of alignment we discussed earlier, but on the other hand the detector size was taken as a more generous 20μm x 20μm. The power consumption of the optoelectronic network would be a function of the electronic switches; the modulators and their drivers; and the detectors and their amplifiers.

Obviously in an exercise like this, where so many assumptions have to be made, it would be unwise to expect to derive definitive quantitative results as to the merits of both approaches. However, the general trends are certainly worthy of note. In terms of clock speed the VLSI implementation could be operated at high speed (100MHz) for small networks (N<256), but as the size increased the operating speed was found to be constrained because of delay in the longest wires, whilst the optoelectronic network speed was found to be independent of the network size. In terms of throughput the VLSI system reached a saturation point, for as the network size increased the clock speed had to be reduced. This restriction did not apply to the optoelectronic network so the throughput kept on increasing as the network was expanded. Power consumption for small networks was found to be similar, but comparison for larger networks was difficult. This was because the clock speed had to be reduced for the VLSI network, naturally resulting in reduced power consumption compared to the optoelectronic network. If, however, the VLSI network could be maintained at its original clock speed, its power consumption would be higher. This is a direct result of the factors discussed in the energy comparison between optical and electronic interconnects. As the network size is increased the scalability favours the optoelectronic network, because of its use of parallel inputs and outputs, while wiring of the electronic network becomes increasingly complex. This also means that the optoelectronic system will have a smaller footprint for large networks.

It is interesting that a detailed comparison of optoelectronic and electronic systems for a particular application should support the general conclusions made before. Principally, for small systems electronics have the advantage, but as the demands on the system size and speed increase an optoelectronic approach is shown to be of benefit. An important caveat is that the benefits optoelectronics can bestow is reliant on high levels of integration being obtained between the optical and electronic components, which favours

the use of GaAs on Si technology. Note that even if one was to make the comparison with 0.7μm CMOS and a reduction in supply voltage to 3.3V, the conclusions would not be radically different, but it would result in an increase in the critical point beyond which optoelectronics potentially outperforms VLSI by a factor of ≈2.

Chapter 2

The Effect of Strain in Gallium Arsenide On Silicon Quantum Well Devices

2.1 INTRODUCTION TO QUANTUM WELLS

To understand the effect of strain on the absorption spectra of the MQW structures, it is first necessary to introduce the basic theory that governs absorption in unstrained quantum wells. We start by ignoring the excitons themselves, which result from electron-hole coulomb interaction, and only consider the effect of confinement on free electrons and holes. These are normally described by the effective mass approximation, in which an effective mass is given to each particle according to its diffraction through the semiconductor lattice, due to the periodic potential of the unit cells. External potentials are ignored and the resulting band structure for bulk crystal can be used in the solution to the quantum well. The EMA has been found to be very successful in predicting the resulting absorption characteristics despite changes in the external potential occurring on an atomic scale in quantum well structures. The confinement due to the multilayer structure has the effect of firstly quantizing the motion of the electrons and holes perpendicular to the layers, and secondly introducing a different symmetry to that of the bulk material. This in turn results in new selection rules for optical transitions, and changes the hole masses, particularly for motion parallel to the layers.

In a real quantum well structure, for example GaAs/GaAlAs, there is a finite energy gap between the two materials that is shared between the conduction and valence bands such that:-

$$\Delta E_g = \Delta E_c + \Delta E_v \qquad \textbf{Eqn 2.1}$$

The ratio between ΔE_c and ΔE_v is known as the band offset ratio and is commonly quoted as 60:40. The real MQW structure will have a periodic sequence of wells and barriers of finite width. For wide wells the properties will tend towards those of bulk material, but as the thickness is reduced the allowed energy levels become governed by the effects of quantum confinement. When sufficiently wide barriers are used the wavefunctions between neighbouring wells do not overlap, however, when the barrier thickness is reduced interaction may occur between the adjacent well wavefunctions. This effect is known as coupling. A periodic structure of coupled wells is sometimes referred to as a superlattice, to distinguish it from the MQW. Some interesting possibilities are allowed by coupling effects, but

we shall primarily concern ourselves with the former case of non-interacting wells. The physics of which can be described by considering a single quantum well, and are not dependent on the number of wells present, these only serve to enhance the magnitude of the absorption or phase changes observed.

The real quantum well structures with finite barriers are rather difficult to analyse theoretically so it is instructive to first consider the example of a single, infinitely deep well for which a parabolic, non-degenerate band structure is assumed in the bulk material. For this model the important features resulting from quantum confinement can be deduced, and an exact solution to Schroedinger's equation calculated.

In the plane of the layers there is no confinement and so the electrons and holes can move freely with the usual dispersion laws:-

$$E_c(k) = E_g + \frac{\hbar^2}{2m_e}\left(k_x^2 + k_y^2\right) \qquad \textbf{Eqn 2.2a}$$

$$E_v(k) = -\frac{\hbar^2}{2m_h}\left(k_x^2 + k_y^2\right) \qquad \textbf{Eqn 2.2b}$$

Perpendicular to the layers the electrons and holes are confined, and since we have assumed an infinite well the amplitude of the envelope wave functions must be zero at the barrier walls. Therefore the wavefunctions become :-

$$\varsigma_j^{\infty}(z) = \left(\frac{2}{L_z}\right)^{\frac{1}{2}} \sin\left(\frac{j\pi z}{L_z}\right) \qquad \textbf{Eqn 2.3}$$

where L_z = the layer thickness, and (j-1) =0,1,2.. are the number of nodes of the wavefunctions. The Eigenenergies will be :-

$$E_j^{\infty} = \frac{\hbar^2}{2m_{e,h}}\left(\frac{j\pi}{L_z}\right)^2 \qquad \textbf{Eqn 2.4}$$

which result in a band structure like that shown below in Fig 2.1. A discrete set of energy levels is observed, rather than a single bandgap and a continuum as would be the case for bulk material. Only the first few levels are shown, although in theory there would be an infinite number.

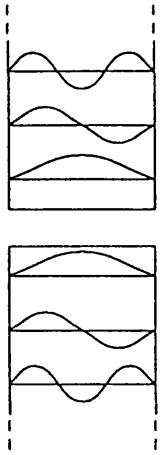


Figure 2.1 *Energy levels in an infinite quantum well*

The optical absorption will be governed by the above transition energies and the joint density of states. For the infinite well approximation this is given by [Chemla and Miller] :-

$$g_{2D}(E) = \frac{\mu}{\pi\hbar^2}\theta\left(E - E_{je}^{\infty} - E_{jh}^{\infty}\right) \qquad \text{Eqn 2.5}$$

where μ is the electron-hole reduced mass $\mu^{-1} = m_e^{-1} + m_h^{-1}$.
Therefore for an infinite well the absorption spectrum is a series of steps starting at $\Delta E = E_{je}^{\infty} - E_{jh}^{\infty}$, with the selection rule $\Delta j = j_e - j_h = 0$.

An example of a typical absorption spectrum for a MQW device is shown below in Fig 2.2. From the figure it can be seen that in addition to creating a step-like band structure the quantum confinement also allows significant excitonic effects to be observed at room temperature, and these must be included to describe the overall absorption characteristics of the quantum wells. In fact, for the modulators described in this thesis the excitonic absorption could be said to be of primary importance in determining the overall device performance. Excitons are loosely bound electron-hole pairs and require less energy for formation than a free electron and hole pair. However, in bulk semiconductors at room temperature the binding energy is

much smaller than the phonon energy, which results in their rapid thermal ionization. Lowering the temperature results in the observation of clear excitonic features.

The same result can be achieved through quantum confinement of the exciton, by which its binding energy is substantially increased. For while the exciton in bulk semiconductors is found to have a radius of 300Å and a binding energy of 4.2meV, the electron and hole will be forced closer together in the quantum well, resulting in an increase in binding energy up to a 2-d limit of ≈16meV. Although the exciton is still rapidly ionized at room temperature its lifetime is sufficiently increased for the exciton to be clearly visible in high quality material.

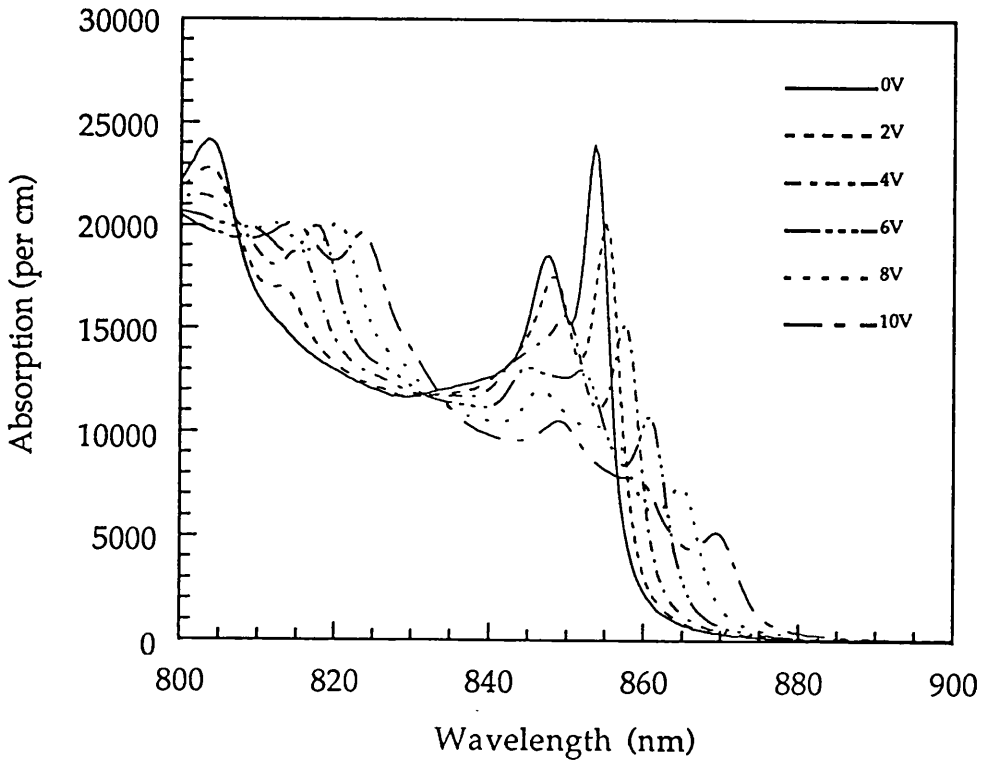


Figure 2.2 *Quantum Well Absorption Spectrum for a 100Å MQW*

The simplification that considers a single quantum well of infinite depth is very effective for interpreting the general characteristics of the band structure, but more accurate predictions require the modelling of wells with finite

depth. For such a well the envelope well function is no longer totally confined within the well but decays exponentially in the barriers so that:-

$$\varsigma_j(z) \propto \begin{cases} \sin(q_j W_z) & \text{inside the well} \\ \exp(-q_j B_z) & \text{outside the well} \end{cases} \qquad \textbf{Eqn 2.6}$$

The band structure then consists of a number of bound states and a continuum, as shown in the figure below.

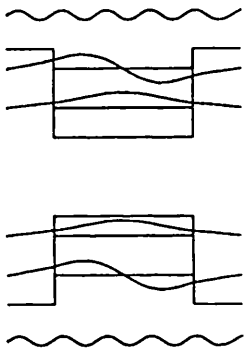


Figure 2.3 *Energy levels in a finite quantum well*

The energies may be found by a graphical solution to Schroedinger's equation and a number of features are worth noting:-

i) The energies depend on the effective masses both in the well and the barrier;
ii) there is always at least one bound state;
iii) the low lying energy levels are well confined in the wells, but as the energy level increases the exponential tails extend further into the barriers.

This last point is important because a limit is provided for the degree of possible confinement. As the well is narrowed the energy level of the lowest confinement state rises and extends further into the barriers, thereby limiting the confinement.

2.2 QUANTUM WELLS AND STRAIN

The influence of strain, due to GaAs on Si growth, on the absorption characteristics of quantum wells is best understood by first considering the simpler case of a single GaAs layer grown on silicon. Ideally, in order to minimize the dislocation density, the lattice mismatch between the two materials would be accommodated by strain in the epitaxial layer. The net strain in the layer plane can then be denoted by :-

$$\varepsilon_{\parallel} = \varepsilon_{xx} = \varepsilon_{yy} = \frac{(a_s - a_e)}{a_e} \qquad \textbf{Eqn 2.7}$$

Where a_s is the substrate lattice constant and a_e is the bulk lattice constant of the epitaxial material. This will only apply when the substrate thickness is much greater than the epitaxial layer thickness, and when no dislocations are generated in the epitaxial layer.

The co-ordinate system used is such that the x and y directions both lie in the epitaxial plane with z parallel to the growth direction, as shown in the figure below. The strain is biaxial, i.e. it is the same in both x and y directions, and induces a biaxial stress in the layer material. The lattice is therefore tetragonally distorted, so that if it is compressed in the x and y directions it will be expanded in the z direction. This relaxation along the growth direction is given by the following equation:-

$$\varepsilon_{\perp} = \varepsilon_{zz} = -\frac{2\sigma}{1-\sigma}\varepsilon_{\parallel} \qquad \sigma = \text{Poisson's ratio} \qquad \textbf{Eqn 2.8}$$

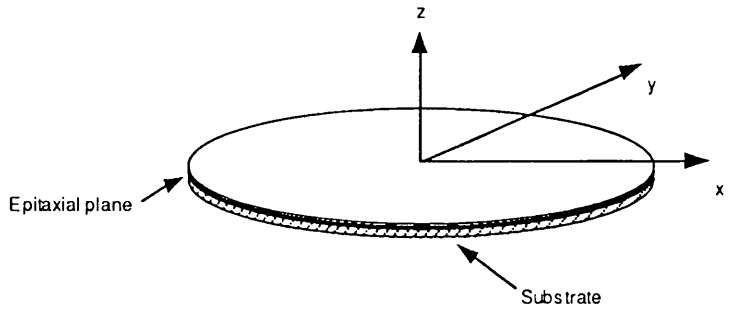


Figure 2.4 *Orientation of Co-ordinates*

For tetrahedral semiconductors $\sigma \approx 1/3$ so that $\varepsilon_{\perp} \approx -\varepsilon_{\parallel}$. It is often found useful to resolve the total strain into axial and hydrostatic components such that [O'Reilly] :-

$$\varepsilon_{ax} = \varepsilon_{\perp} - \varepsilon_{\parallel} \approx -2\varepsilon_{\parallel}$$

$$\text{and} \quad \varepsilon_{vol} = \frac{\Delta V}{V} \approx \varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz} \approx \varepsilon_{\parallel} \qquad \textbf{Eqns 2.9 a and b}$$

One might expect that since GaAs (a_e=5.653Å) has a larger lattice constant than Si (a_s=5.431Å) the epitaxial layer would experience a large compressive strain. Unfortunately, dislocations will be generated as the film thickness is increased, with a concomitant degradation in material quality. These aspects will be discussed in more detail in the next chapter. For the moment it is sufficient to note that for GaAs layers thicker than a few monolayers a high dislocation density will be present. The point at which this occurs is known as the critical thickness, h_c , and is defined as the layer thickness for which the stored strain energy exceeds that required for dislocation formation. This is shown schematically in Fig 2.5 below.

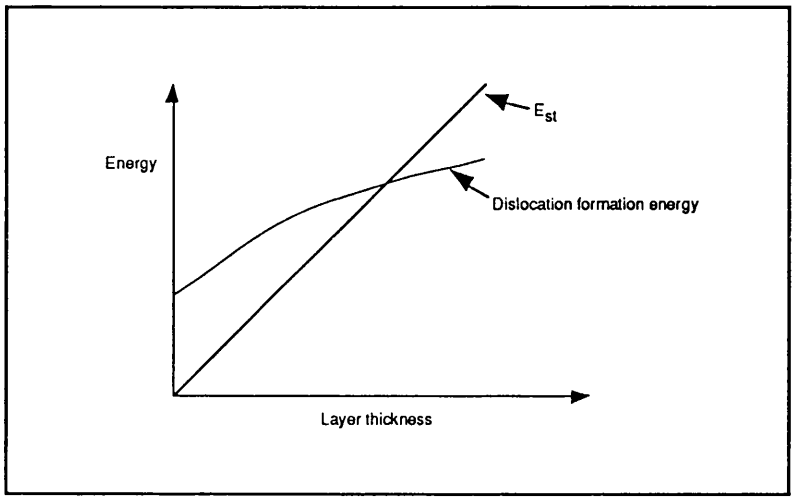


Figure 2.5 *Strain and Dislocation Energy v Layer Thickness*

The stored strain energy is given by the relationship:-

$$E_{st} = 2G\left(\frac{1+\sigma}{1-\sigma}\right)\varepsilon_{\parallel}^{2}h \qquad \textbf{Eqn 2.10}$$

where G is the shear modulus of the material and h is the layer thickness. Because the strain is so large for GaAs on Si (4.1%), the strain energy rapidly exceeds the dislocation formation energy. In fact the critical thickness is only a few monolayers for GaAs/Si, consequently any useful layer thicknesses will contain a large number of dislocations. These result in :

i) a large number of non-radiative recombination centres

ii) a reduction in the built-in strain

The latter effect is very important because it reduces, or eliminates, the compressive strain described above. However, upon cooling from the growth temperature a biaxial tension is created in the epitaxial layer due to the thermal mismatch of the two materials. The GaAs has a larger thermal coefficient of expansion than silicon and attempts to contract at this rate, but is constrained by the thicker substrate. The result is a slight concave bowing of the wafer, with the GaAs layer held in tension.

The strain is found not to drastically alter the shape of the conduction band, which is assumed to be parabolic for small k :-

$$E_c(k) = E_g + \frac{\hbar^2 k^2}{2m^*} \qquad \textbf{Eqn 2.11}$$

However, the strain can have a dramatic effect on the band gap and the valence band structure as illustrated schematically below [O'Reilly].

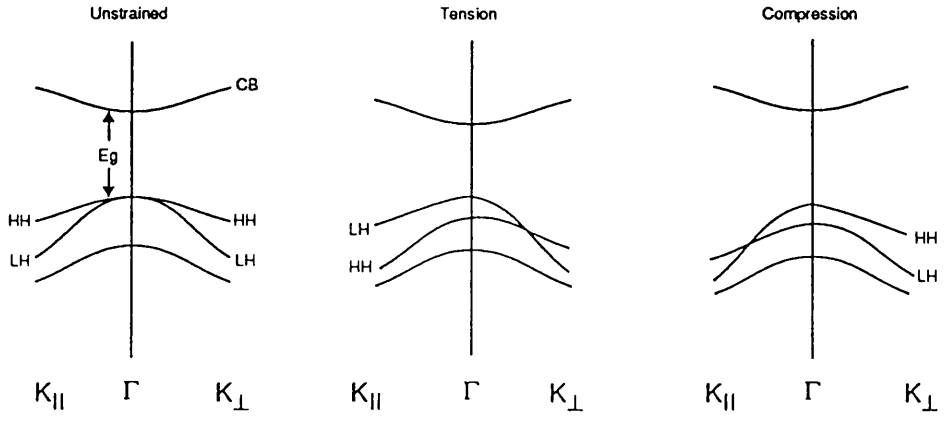


Figure 2.6 *Effect of tensile & compressive strain on the band structure*

The band structure is altered in the following ways:-

i) the hydrostatic component of strain changes the mean band gap, reducing it for tensile strain and increasing it for compressive strain.

ii) the axial component of strain lifts the valence band degeneracy at Γ, splitting the *hh* and *lh* bands. An anisotropy also occurs which makes description of the bands difficult, for in the case of biaxial tension the highest band is light along $k_{\perp}$ (the strain axis) but is heavy along $k_{||}$ (in the epitaxial plane). For biaxial compression the converse will be true.

In the unstrained state the heavy hole and light hole bands are degenerate at the valence band maximum due to the cubic symmetry of the lattice, while spin-orbit interaction results in a non-degenerate "split-off" band. When strain is applied the lattice is altered in the z direction with respect to the x and y directions, resulting in the heavy and light hole splitting.

These changes to the band structure can be used to advantage in many types of strained layer structures. For example, lifting of the lattice matching constraint means that a wider range of material combinations can be utilized, resulting in an increased choice of operating wavelengths. This is equally true whether for modulator structures or for lasers. In fact strained layer quantum well lasers also promise very low threshold currents, narrow linewidths, and lower chirp, as a result of the strain-induced changes to the band structure. One way in which this occurs is through reduced loss mechanisms. For example Auger recombination, in which an electron and hole recombine resulting in the excitation of another carrier rather than the emission of a photon. This is less likely to occur in a strained material due to the lifting of the valence band degeneracy. Similarly, inter-valence band absorption, in which a photon excites an electron from the split-off band into a hole state, is reduced. For modulator structures it is possible that in addition to increasing the range of operating wavelengths, strain could also be used to modify the absorption spectra. For example, in the case of GaAs-on-Si, the superposition of the heavy and light hole transitions. Alternatively strain could be used to modify the valence band structure so as to narrow the exciton absorption linewidths.

2.2.1 Calculation of Change in Band-gaps and Band-offsets

One can analyse quantitatively the effect of strain on the band gap and band splitting by using the model solid theory employed by [Van der Walle]. This provides a theoretical model by which the band structure of strained materials can be predicted. The results are expressed in terms of an absolute energy level for each semiconductor, and the hydrostatic and shear potentials that describe the effects of strain on the electronic bands. Although originally intended to describe lattice mismatched materials of less than the critical thickness, it has been adapted here to equally well describe thermally induced strain in GaAs on silicon structures.

A powerful feature of the model is the ability to predict the band offsets between two strained materials. We can thus analyse a strained GaAs/GaAlAs bilayer as would occur for growth of modulator structures on silicon. Both the strain induced shifts in the two materials and the band alignments can then be predicted. A comparison is presented below for three important cases: biaxial tensile strain; biaxial compressive strain; and unstrained material. In each case we consider a GaAs/GaAlAs heterojunction, giving an insight into both the band structure and the band offsets.

First let us consider the case of a GaAs on Si layer cooling from the growth temperature to room temperature. At 900°C the bulk GaAs lattice is 5.68Å [Landolt & Bornstein] which is reduced to 5.653Å at room temperature (300K). The GaAs will therefore attempt to contract to the smaller lattice constant, however it is constrained by the much thicker silicon substrate which has a slower rate of contraction. The GaAs epitaxial layer will therefore be under tensile strain. The value of strain will be dependent on the number of dislocations and the degree of wafer bending [Stoltz *et al*, Ueda *et al*]. For example, the maximum possible for a change in temperature from 900°C to room temperature would be a tensile strain of 0.0048. For the purpose of example we will estimate ε=0.002, which allows for some strain relief through dislocations and wafer bending, and use the parameters listed overleaf which have been derived from references [Van de Walle] and [Landolt and Bornstein].

	Δ_0	$E^0_{v,av}$	a_v	E_g^{dir}	E_c^{dir}	a_c^{dir}	a^{dir}	b	a_{semi}	c_{11}	c_{12}	D^{001}
GaAs	0.34	-6.830	1.37	1.426	-5.29	-8.43	-9.80	-2.00	5.653	11.8	5.37	0.910
$Ga_{0.7}Al_{0.3}As$	0.322	-6.982	1.83	1.853	-5.022	-7.90	-9.73	-1.95	5.655	11.9	5.27	0.886

Table 2.1 *Essential Parameters at 300K*

Notes on Parameters

i) Here $E_{v,av}$ is the average of the three uppermost bands at Γ, which are the *hh*, *lh*, and split-off bands. The model relates the strained energy levels to this average level, which does not have any physical significance of its own accord.

ii) The split-off energy is given by Δ_0 , which in the unstrained case is the difference in energy between the *hh* and *lh* at Γ and the split-off band. Like all other values of energy it is here given in eV.

iii) E_g^{dir}=the direct energy gap, and E_c^{dir}=the energy of the conduction band from which other energies are referred to.

iv) The hydrostatic deformation potential a^{dir} is split into conduction and valence band components so that

$$a^{dir} = a_c^{dir} - a_v$$

v) The shear deformation potential for a strain of tetragonal symmetry is given by b, in eV.

vi) The constant D, for the orientation considered here, depends on the elastic constants c_{11} and c_{12} which are given in units of 10^{11} dyn/cm^2.

vii) The bulk lattice constants of the materials are given by a_{semi} in Å.

The application of the model is best described by example. Here we consider a GaAs/GaAlAs bilayer under tensile strain, compressive strain and in the unstrained state.

2.2.1.1 Tensile Strain

We start by considering tensile strain as would occur for thermal mismatch with the silicon substrate. The strain is assumed to be equal in the two layers, the band structure can then be calculated using the following three steps.

i) Calculation of the strained valence bands

First consider the GaAs layer which, for a tensile strain of ε=0.002, will have $a_{\parallel}$ =5.6643 where $a_{\parallel}$ is the lattice constant in the growth plane. In the direction of growth the lattice constant is given by $a_{\perp}$:-

$$a_{\perp} = a_{GaAs}\left[1 - D^{001}_{GaAs}\left(\frac{a_{\parallel}}{a_{GaAs}} - 1\right)\right] \qquad \textbf{Eqn 2.12}$$

$$\text{giving } a_{\perp} = 5.6427\text{Å} \qquad \textbf{Eqn 2.12a}$$

therefore the strain along the z axis is $\varepsilon_{\perp}$ = -0.001822, where we have used the same co-ordinate system as shown in Fig 2.4. The strains are therefore:

$$\varepsilon_{XX} = \varepsilon_{yy} = 0.002 \text{ and } \varepsilon_{ZZ} = \varepsilon_{\perp} = -0.001822.$$

Leading to a volume change:

$$\Delta\Omega/\Omega \approx \varepsilon_{XX} + \varepsilon_{yy} + \varepsilon_{ZZ} = 0.002178.$$

$E_{v,av}$ is given by $E_{v,av} = E^{\circ}_{v,av} + a_v.\Delta\Omega/\Omega$ **Eqn 2.13**

$$= -6.83 + (1.37 \times 0.002178)$$
$$= -6.8270 \text{ eV}$$

For GaAlAs there is also a 0.002 tensile strain making $a_{\parallel}$ = 5.6663Å and $a_{\perp}$ = 5.6450Å therefore $\varepsilon_{\perp}$= -0.001768.
Similarly,

$$\Delta\Omega/\Omega = 0.002 + 0.002 - 0.001768 = 0.002232$$

$$\text{and } E_{v,av} = E^{\circ}_{v,av} + a_v.\Delta\Omega/\Omega = -6.9779 \text{ eV}$$

Finally, the average valence band offset is given by $\Delta E_{v,av}$ = 0.1509eV.

ii) Calculation of the strained conduction bands

for GaAs $E_c^{GaAs} = E_c^{dir} + a_c^{dir}.\Delta\Omega/\Omega = -5.3083eV$

and for GaAlAs $E_c^{GaAlAs} = -5.3096eV$

therefore $\Delta E_c = 0.2687eV$.

iii) Calculation of the valence band splitting

The splittings due to strain are given relative to $E_{v,av}$ as follows:-

heavy hole $\Delta E_{v,2} = \frac{1}{3}\Delta_0 - \frac{1}{2}\delta E_{001}$ **Eqn 2.14**

light hole $\Delta E_{v,1} = -\frac{1}{6}\Delta_0 + \frac{1}{4}\delta E_{001} + \frac{1}{2}[\Delta_0^2 + \Delta_0.\delta E_{001} + \frac{9}{4}(\delta E_{001})^2]^{\frac{1}{2}}$

split off $\Delta E_{v,3} = -\frac{1}{6}\Delta_0 + \frac{1}{4}\delta E_{001} - \frac{1}{2}[\Delta_0^2 + \Delta_0.\delta E_{001} + \frac{9}{4}(\delta E_{001})^2]^{\frac{1}{2}}$

where $\delta E_{001} = 2b\,(\varepsilon_{zz} - \varepsilon_{xx})$ **Eqns 2.15 a, b and c**

Therefore for GaAs we have	hh	$\Delta E_{v,2}$	= 0.10569eV
	lh	$\Delta E_{v,1}$	= 0.12131eV
	s.o.	$\Delta E_{v,3}$	= -0.22700eV
and for GaAlAs	hh	$\Delta E_{v,2}$	= 0.09999eV
	lh	$\Delta E_{v,1}$	= 0.11507eV
	s.o.	$\Delta E_{v,3}$	= -0.21493eV

From these results one can see that the *lh* and *hh* are no longer degenerate and that the *lh* is now the highest level. The valence band offset is therefore given for the *lh* by :-

$$\Delta E_v = \Delta E_{v,av} + \Delta E_{v,1}^{GaAs} - \Delta E_{v,1}^{GaAlAs} = 0.1571eV.$$

Steps *i)* to *iii)* can be repeated for unstrained GaAs/AlGaAs and for compressive strain with the following results.

2.2.1.2 Unstrained GaAs/GaAlAs

i) Valence Band

ε_{xx} =0, therefore $E_{v,av}^{GaAs}$ = -6.83 and $E_{v,av}^{GaAlAs}$ = -6.982eV.

ii) Conduction Band

$E_c = E_c^{dir}$ = -5.29eV for GaAs and -5.022eV for GaAlAs.

iii) Valence Band Splitting

For GaAs Δ_0 = 0.34eV and the lh and hh are degenerate so

$\Delta E_{v,1} = \Delta E_{v,2} = \frac{1}{3}\Delta_0 = 0.11333eV,$

and $\Delta E_{v,3} = -\frac{2}{3}\Delta_0 = -0.22667eV.$

For GaAlAs Δ_0 = 0.322eV and $\Delta E_{v,1} = \Delta E_{v,2} = \frac{1}{3}\Delta_0 = 0.10733eV$

and similarly $\Delta E_{v,3}$ = -0.21467eV.

2.2.1.3 Compressive Strain

Compressive strain would be expected due to lattice mismatch, but is normally relieved by dislocations. For comparison we consider a compressive strain of ε = -0.002. Using the same methodology the following results are obtained:-

i) Valence Band

For GaAs ε = -0.002 then $a_{\parallel}$ = 5.6417 and $a_{\perp}$ = 5.6633. Therefore it follows that $\varepsilon_{\perp}$ = 0.001822, $\Delta\Omega/\Omega \approx$ -0.002178 and $E_{v,av}$ = -6.8330eV. Similarly, for GaAlAs $a_{\parallel}$ = 5.6437, $\varepsilon_{\perp}$ = 0.001768, $\Delta\Omega/\Omega \approx$ -0.002232 and $E_{v,av}$ = -6.9861eV.

Therefore $\Delta E_{v,av}$ = 0.1531eV.

ii) Conduction Band

For GaAs $E_c^{GaAs} = E_c^{dir} + a_c^{dir}.\Delta\Omega/\Omega$ = -5.2717eV and for GaAlAs E_c^{GaAlAs} = -5.0044eV.

Therefore ΔE_c =0.2673eV.

iii) Valence Band Splitting

For GaAs	hh	$\Delta E_{v,2}$ = 0.12098eV
	lh	$\Delta E_{v,1}$ = 0.10604eV
	s.o.	$\Delta E_{v,3}$ = -0.22702eV
and for GaAlAs	hh	$\Delta E_{v,2}$ = 0.11468eV
	lh	$\Delta E_{v,1}$ = 0.10033eV
	s.o.	$\Delta E_{v,3}$ = -0.21501eV

The splitting for compressive strain is the opposite of that found for tensile strain. The degeneracy of the *hh* and *lh* bands is lifted, but the *hh* is now of highest energy. The valence band offset is then given by :-

$$\Delta E_v = \Delta E_{v,av} + \Delta E_{v,2}^{GaAs} - \Delta E_{v,2}^{GaAlAs} = 0.1594eV.$$

2.2.1.4 Band Structure Diagrams

The results can best be interpreted by reference to the band structure diagrams as shown overleaf:-

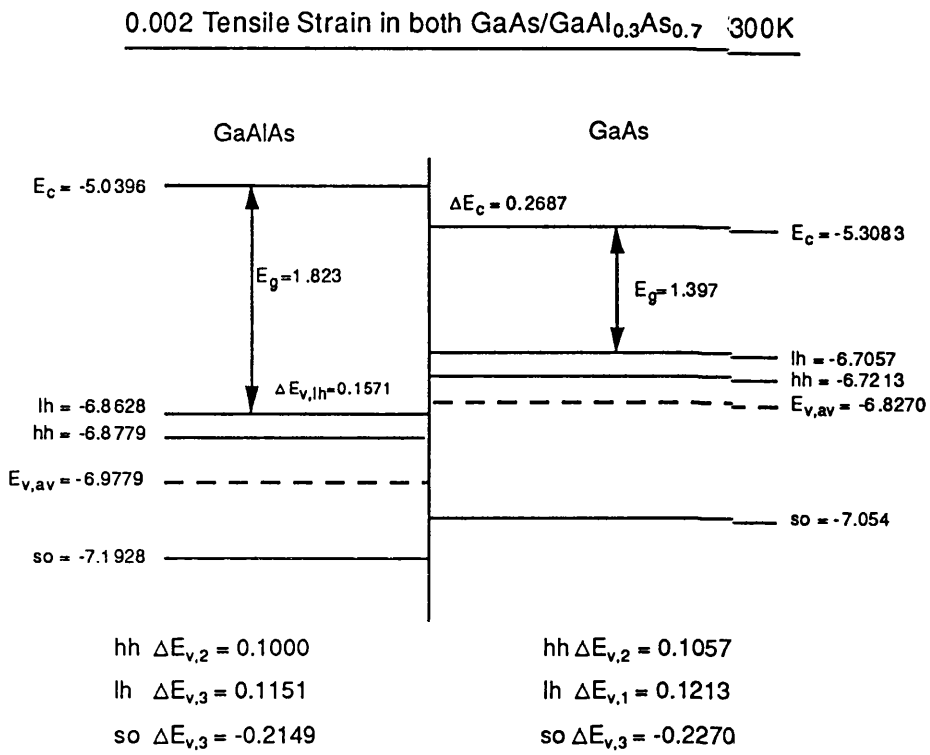


Figure 2.7 *Energy levels and band offsets for tensile strain.*

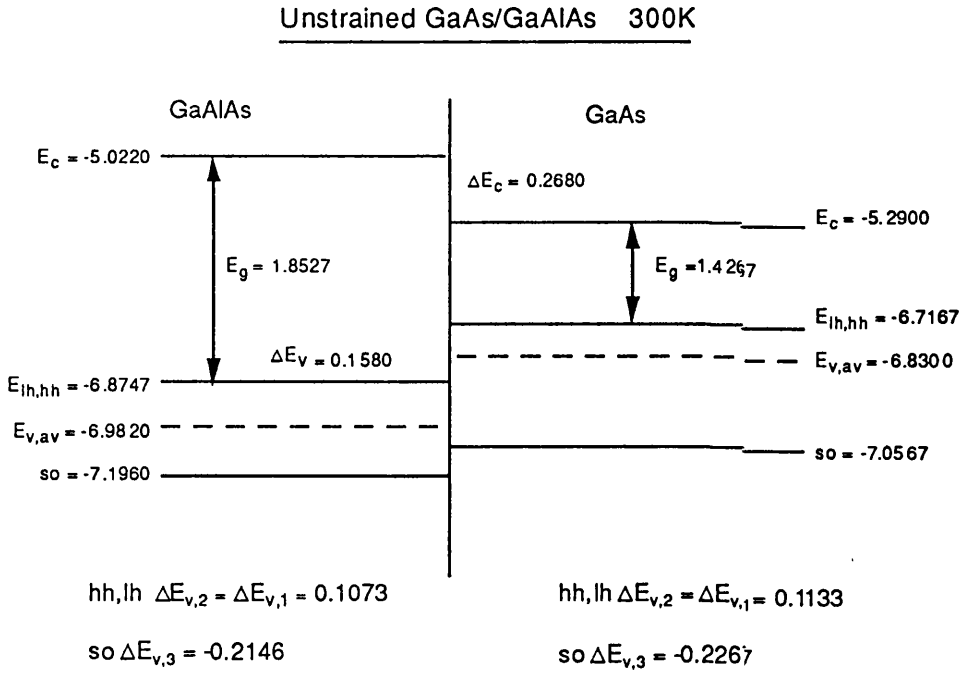


Figure 2.8 *Energy levels and band offsets for unstrained material.*

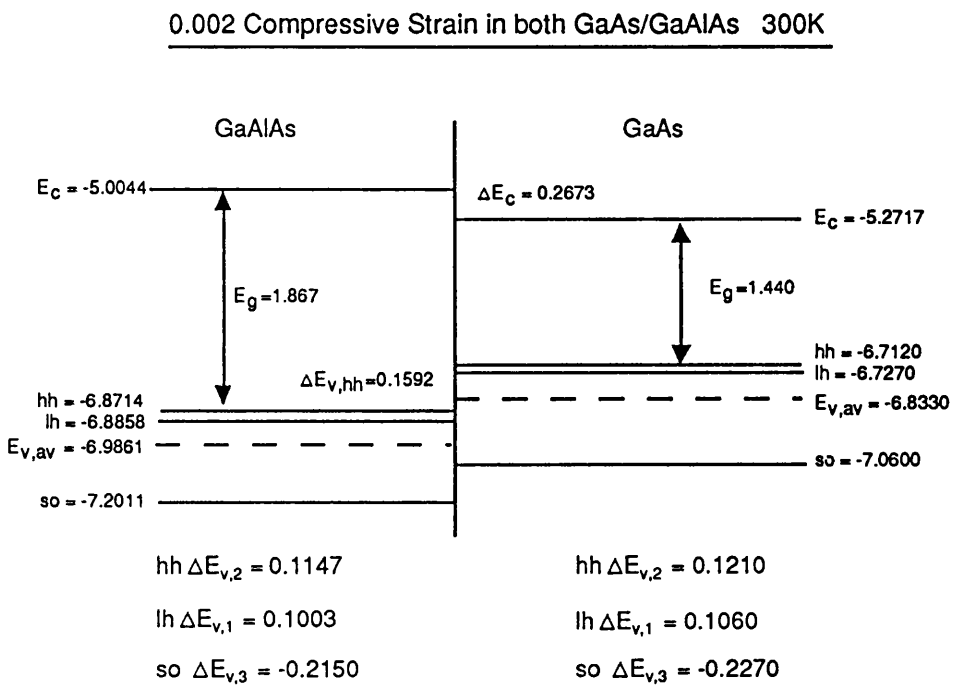


Figure 2.9 *Energy levels and band offsets for compressive strain.*

The band shifts can be equally well described in terms of stress rather than strain. These are related in the following manner :-

$$\varepsilon_{xx} = \varepsilon_{yy} = (S_{11} + S_{12}).X \quad \text{and} \quad \varepsilon_{zz} = 2S_{12}.X \qquad \textbf{Eqn 2.16 a and b}$$

Where S_{11} and S_{12} are the compliance coefficients and X is the stress magnitude, which is taken as positive for tensile stress. The splitting of the valence band is given by:-

$$E_S = 2b(S_{11} - S_{12}).X \qquad \textbf{Eqn 2.17}$$

and the change in the energy gap between the conduction band and $E_{v,av}$:-

$$E_H = 2a(S_{11} + 2S_{12}).X \qquad \textbf{Eqn 2.18}$$

The two can be added to give for the lh:-

$$\delta E_g^{lh} = [2a(S_{11} + 2S_{12}) + b(S_{11} - S_{12})].X \qquad \textbf{Eqn 2.19}$$

and for the hh:-

$$\delta E_g^{hh} = [2a(S_{11} + 2S_{12}) - b(S_{11} - S_{12})].X \qquad \textbf{Eqn 2.20}$$

The coefficients are given by [Freundlich *et al*] as S_{11} =1.16x10^{-6}bars^{-1} and S_{12} =-0.37x10^{-6}bars^{-1}. From the valence band splitting the stress at 1.8K was estimated as ≈3kbar.

In addition to lifting the degeneracy of the *lh* and *hh* bands the strain also changes the band-gap, which is reduced for tensile strain and enlarged for compressive strain. The band offsets predicted here between GaAs and GaAlAs, when both experience the same degree of strain, are equivalent to those that would be found in a MQW grown on silicon. We can therefore use these values in the solution of the quantum well so as to determine the combined effect of strain and quantum confinement on the observed energy levels. From the band structures shown in Fig 2.6 it can be observed that the band labelled *lh* is in fact light only perpendicular to the layer plane, while parallel to the epitaxial plane it is relatively heavy. Conversely, the *hh* is relatively light in the epitaxial plane. This crossover has been experimentally observed by [Freundlich *et al*]. Due to the uncertainty over which band is heavy and which is light the notation can become somewhat confusing. One can alternatively describe the effect of strain as splitting the J=3/2 valence band into a higher energy (for tensile strain) m_J=±1/2 band and a lower energy m_J=±3/2 band, or vice versa for compressive strain.

2.2.2 Change in Effective Masses Due to Strain

In addition to altering the band gaps and band offsets, the strain also changes the effective masses of the holes and electrons. These changes in effective mass in turn result in new transition energies for the quantum well structures *(Section 2.1)*. We must therefore calculate these new masses before tackling the problem of quantum confinement in the band-structures calculated above.

The following expressions were used to relate the changes in effective mass of the electron and light hole with strain, the heavy hole undergoing very little change, and were calculated using the **k.p** method [Kane, Stavrinou].

electron $$\frac{m_0}{m_e^*} = 1 + \frac{2m_0P^2}{\hbar}\left(\frac{E_{gs} + \frac{1}{3}\partial E_{001} - \frac{2}{3}E_{so}}{\left(E_{gs} - E_j^{lh}\right)\left(E_{gs} - E_j^{so}\right)}\right)$$ **Eqn 2.21**

light hole $$\frac{m_0}{m_{lh}^*} = 1 + \frac{2m_0P^2}{\hbar}\left(\frac{E_j^{lh} + \frac{1}{3}\partial E_{001} - \frac{2}{3}E_{so}}{\left(E_j^{lh} - E_j^{so}\right)\left(E_j^{lh} - E_{gs}\right)}\right)$$ **Eqn 2.22**

where $E_{so} = -\Delta_{so} + \frac{1}{2}\partial E_{001}$

E_{gs} = energy difference measured from hh level to electron level

E_j^{lh} = energy difference measured from hh level to lh level

E_j^{so} = energy difference measured from hh level to so level

and $E_p = \frac{2m_0P^2}{\hbar}$ is the valence to conduction band coupling energy

The values of $dE_{001} = 2b(\varepsilon_{zz} - \varepsilon_{xx})$ are the same as used in *Section 2.2.1* for the van der Walle model. Values for m_e^*, m_{lh}^*, E_g, E_p and Δ_{so} were taken or extrapolated from [Chemla and Miller], [Landolt and Bornstein], [Chemla *et al* (84)], [Stevens *et al*]. These are shown in the table below (energies in eV):-

	E_g	E_p(hh)	E_p(lh)	m_e^*	m_{lh}^*	Δ_{so}
GaAs	1.4267	21.4	20.61	0.0665	0.094	0.340
GaAlAs	1.8527	19.3	21.64	0.0917	0.114	0.322

Table 2.2 *Energies and effective masses for unstrained GaAs/GaAlAs*

First let us consider the change in effective mass of the electron due to tensile strain, which is governed by Eqn 2.21 above. Using Eqn 2.21 and the values given in the band structure diagrams and in Table 2.2, we obtain the following values:-

For GaAs

E_{gs} = energy difference from hh to e = 1.413

$\frac{\partial E_{001}}{3} = 0.00510$

$\frac{2}{3}E_{so} = -\Delta + \frac{1}{2}\partial E_{001} = -0.222$

E_j^{lh} = energy difference from hh to lh = 0.0156

E_j^{so} = energy difference from hh to so = –0.333

therefore $m_e^* = 0.065$

For GaAlAs

$E_{gs} = 1.838$

$\frac{\partial E_{001}}{3} = 0.00490$

$\frac{2}{3}E_{so} = -0.210$

$E_j^{lh} = 0.0151$

$E_j^{so} = -0.315$

therefore $m_e^* = 0.0902$

Similarly the light hole masses can be calculated for tensile strain giving the following results:-

GaAs $m_{lh}^* = 0.0888$ *GaAlAs* $m_{lh}^* = 0.1079$

The same procedure can be used for compressive strain giving the following values:-

GaAs $m_e^* = 0.0678$ (electron) and $m_{lh}^* = 0.100$ (light hole)

GaAlAs $m_e^* = 0.0933$ (electron) and $m_{lh}^* = 0.120$ (light hole)

The calculated effective masses, in terms of m_o, are summarized in the following table:-

		Tensile Strain	*Compressive Strain*	*Unstrained*
GaAs	m_e^*	0.0650	0.0678	0.0665
	m_{lh}^*	0.0888	0.1000	0.0940
GaAlAs	m_e^*	0.0902	0.0933	0.0917
	m_{lh}^*	0.1079	0.1200	0.1138

Table 2.3 *Effective masses, in terms of m_o, for strained and unstrained $GaAs/GaAl_{0.3}As_{0.7}$.*

2.2.3 *Transition Energies in Strained Quantum Wells*

Having calculated the band structures of strained GaAs and GaAlAs one can now introduce the additional effects caused by quantum confinement in the MQW structure. Using an existing computer model, which was developed for predicting the energy levels of an unstrained quantum well, we can insert the new values of band offsets for strained material, together with the new effective masses, and so predict the energy levels that result from a combination of strain and quantum confinement.

For a 95Å GaAs well with 60Å $Ga_{0.7}Al_{0.3}As$ barriers the results were as follows:-

	e1-hh	*e1-lh*	*(hh-lh)*
Unstrained	844.6	836.1	8.5
Tensile Strain	851.9	851.9	0.0
Compressive Strain	836.9	820.7	16.2

Table 2.4 *Transition wavelengths in nm for a 95Å GaAs well with 60Å $Ga_{0.7}Al_{0.3}As$ barriers with and without strain.*

To find the transition wavelengths of the excitonic transitions we need to subtract the *hh* and *lh* exciton binding energies. These are given by [Miller *et al* (85)] as 7.3meV for the heavy hole and 8.3meV for the light hole. The exciton transitions are then given as follows:-

	hh exciton	*lh exciton*	*splitting*
Unstrained	848.9	840.8	8.1
Tensile Strain	856.2	856.8	0.2
Compressive Strain	841.1	825.2	15.9

Table 2.5 *Exciton transitions wavelengths in nm for a 95Å GaAs well / 60Å $Ga_{0.7}Al_{0.3}As$ barriers with and without strain.*

The above results clearly demonstrate the effect of strain on the quantum well absorption characteristics. Firstly, there is a significant change in the band gap

(*hh* excitonic transition) from 841nm for a 0.2% compressive strain, to 849nm for the unstrained case, and 856nm for 0.2% tensile strain. This effect has actually been harnessed in a number of intentionally strained materials in order to increase the wavelength operating range of devices. Secondly, the *lh* excitonic transition is seen to shift with strain in a similar fashion, and finally the splitting between the *lh* and *hh* excitonic transitions changes. While compressive strain is seen to increase the splitting, application of a tensile strain reduces it to near zero. The two transitions thus become superimposed, and one would not expect to observe separate light and heavy hole transitions. The experimental results in Chapter 4 reveal this to be precisely the case, with only a single excitonic peak being observed. Of course, due to the exciton broadening it is impossible to say exactly how close the overlap is, it may well be that the transitions are 2-3nm apart, nevertheless the trend is clear. Certainly there exists the possibility of intentionally introducing strain into a material system, in order to benefit from the heavy and light hole excitonic superposition. The shift with strain of the band gap with strain is also evident from the experimental results, however it is rather less than that calculated for 0.2% strain. Although there is always a difficulty in obtaining a reliable control sample, the shift with strain appeared to be 4-5nm rather than the 7nm predicted above. This suggests the tensile strain in the samples was marginally less than 0.2% at room temperature.

2.3 APPLICATION OF ELECTRIC FIELD TO QUANTUM WELL STRUCTURES

Application of an electric field to the quantum well structures results in electro-optic effects that are not observed in the bulk material. If the field is applied parallel to the wells the exciton is ionized, resulting in the loss of the excitonic peak from the absorption spectrum, although in other respects there is little difference to the bulk material. However, if the field is applied perpendicular to the wells one observes the Quantum Confined Stark Effect. The field may be applied by growing the quantum wells in the intrinsic region of a *pin* diode which can then be reverse biased. The applied field shifts the excitonic peak to longer wavelength, and although reduced in magnitude excitonic features can still be observed at fields of up to fifty times

the classical limit. This is as a direct result of quantum confinement in the wells. Typical experimental electro-absorption spectra for quantum wells grown on GaAs are shown in Fig 2.2, while results for devices grown on silicon are described in the next chapter.

The applied field causes a tilting of the band structure of the quantum wells, shown in Fig 2.10. The energy levels that were calculated in the absence of reverse bias will therefore no longer be valid. This is as a result of the field providing a mechanism by which the electrons and holes can tunnel through the barriers. In fact, the new energy levels are calculated by considering the transmission of carriers through the barriers and determining the tunnelling resonances [Stevens *et al*].

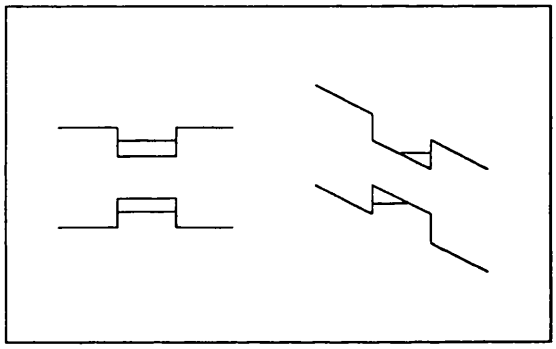


Figure 2.10 *Schematic representation of the effect of the application of an electric field on the band structure of a quantum well.*

One issue that is particularly significant for real *pin* devices is the doping levels in the individual layers. The doping density in the *p* and *n* layers needs to be high. Whether using MBE or MOCVD this is usually not a problem, however, obtaining a low background doping density in the intrinsic region can be difficult using the MOCVD system. The effect of the doping impurities is a variation in the field across the quantum wells in the intrinsic region, shown in the figure below. Each quantum well experiences a different applied field, and as the field governs the shift of the excitonic peak a broadening of the absorption spectrum will be observed. Assuming negligible voltage drop in the contact regions the average field in the intrinsic region will be:

$$E_{av} = (V+V_{bi})/L_i \qquad \textbf{Eqn 2.23}$$

where V is the applied bias, V_{bi} is the built-in voltage, and L_i is the length of the intrinsic region. The variation in the field across the intrinsic region is given by:

$$\Delta E = eN_bL_i/\varepsilon \qquad \textbf{Eqn 2.24}$$

where N_b is the background doping, e is the electronic charge, and ε is the dielectric constant of the intrinsic region. Therefore the field at any point x across the intrinsic region is given by:

$$E = (V+V_{bi})/L_i + (eN_b/e)(x-L_i/2) \qquad \textbf{Eqn 2.25}$$

The actual variation of the field across the intrinsic region is seen to be constant, so expressed as a fraction of the average field it will reduce as the bias is increased. However, the shift of the exciton peak with field is not constant, but increases as the field increases. Therefore the same variation in field results in a greater broadening of transition energies at high field than it does at low fields. The broadening is also accompanied by an apparent reduction in the shift of the exciton peak, for those wells that experience the least field will retain the maximum oscillator strength, and so dominate the absorption spectrum. The gradient at which the field varies is proportional to the background doping density, and if this value is high the field can reach a very high maximum value on one side of the intrinsic region while being close to zero on the other. For example, it was calculated in [Whitehead] that the field variation at 8V/μm would be ±72% of E_{av} for a background doping density of $1x10^{16}$, falling to ±7% of E_{av} at $1x10^{15}$. Clearly there is a significant advantage in obtaining a low background doping density, although theoretically derived absorption spectra quoted in the same reference suggest that there is little improvement to be had from reducing the doping density to below $1x10^{15}$. The large variations in field caused by high background doping also result in reduced breakdown voltages, due to the high maximum value on one side of the intrinsic region.

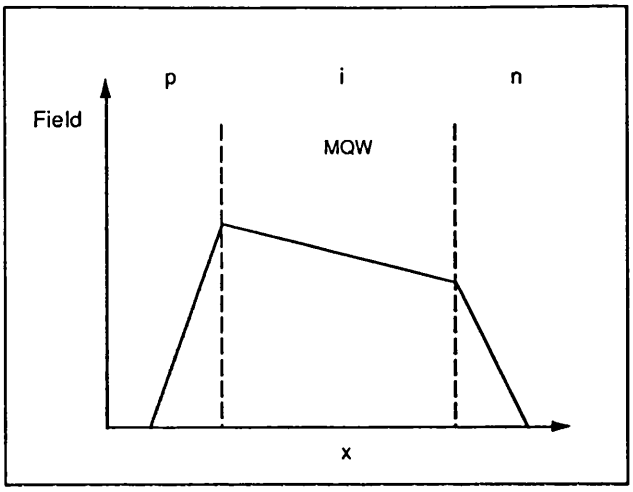


Figure 2.11 *Field variation across the pin diode.*

2.4 INTRODUCTION TO AFPMS

The Asymmetric Fabry-Perot Modulator was developed by [Whitehead *et al* 89(1) 89(2)] following research into the effects of Fabry-Perot resonances on quantum well modulators. Separately much work was done by [Yan *et al*] on a similar topic. Early studies concentrated on single pass transmission modulators, which had windows etched into the back of the GaAs substrate to allow light through. Because the interaction length was so short, of the order of a micron, rear reflectors were used to return light back through the quantum wells, forming a double pass device. In order to eliminate what were thought to be detrimental resonance effects the front surface was normally anti-reflection coated. These devices had the benefit of doubling the possible absorption change while maintaining the same operating voltage.

The device structure that was the inspiration for much of the work done in this thesis is shown schematically in Fig 2.13, and can be regarded as the original AFPM. The device consists of a *pin* diode which is integrated into a Fabry-Perot cavity, the front mirror of which is provided by the air-semiconductor interface, and the rear mirror by the quarter-wave stack.

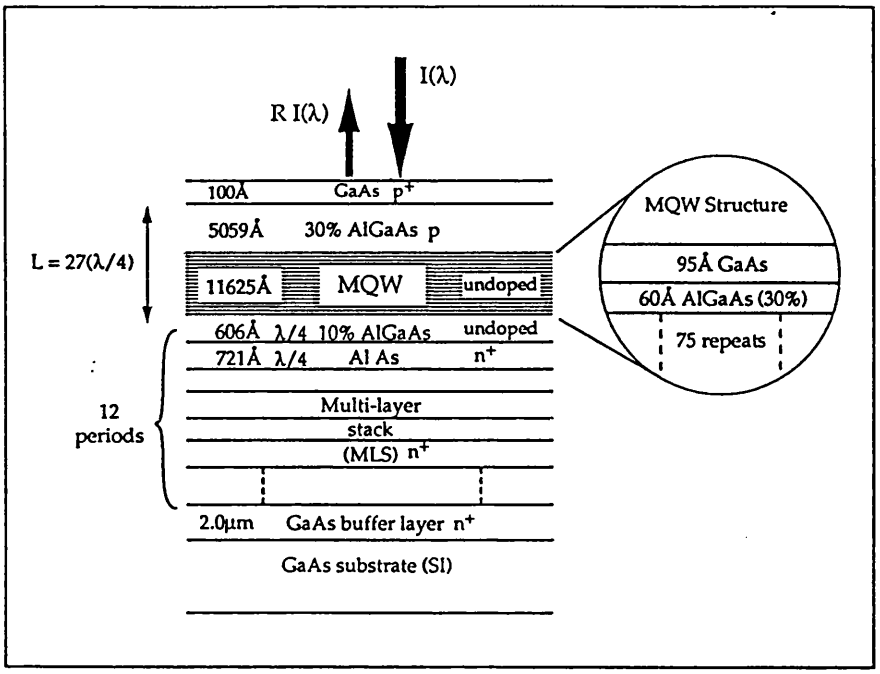


Figure 2.13 *Layer Structure of Original AFPM*

For light incident at a normal to the device the cavity has a number of resonances in the reflectivity (and transmission) spectrum, at which the waves reflected from the stack destructively interfere with those reflected from the front air-semiconductor interface. However, unlike a symmetric cavity, this will not normally result in zero reflection as the stack reflectivity (≈95%) is far greater than the front reflectivity (≈30%). This situation is altered when absorption is introduced into the cavity by means of the quantum wells. The waves reflected from the stack are attenuated, and given the correct amount of absorption, will be equal to those reflected from the front surface. If this is the case complete destructive interference occurs and the reflectivity falls to zero. Therefore, given a means of changing from a low value of absorption to a high value of absorption, a modulator with an extremely high contrast ratio is possible. Fortuitously, the shift of the excitonic peak, with applied electric field, provides an almost ideal mechanism for the required absorption change.

The Fabry-Perot effects of the cavity can be seen more clearly in the following simplified diagram.

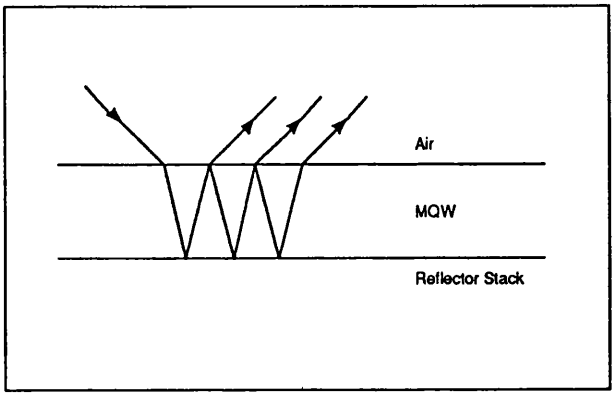


Figure 2.13 *Fabry-Perot etalon with MQW region*

The equations governing the reflectivity of the Fabry-Perot device can be derived either from considering the multiple reflections of individual waves, as shown in the figure above, or by using the wave matrix method as used for modelling the reflector stacks in Chapter 5. In either case the reflectivity at resonance is shown to be:-

$$R = \frac{R_f\left[1-\left(\frac{R_\alpha}{R_f}\right)\right]^2}{(1-R_\alpha)^2} \qquad \textbf{Eqn 2.26}$$

where

$$R_\alpha = (R_f)^{\frac{1}{2}}(R_b)^{\frac{1}{2}}e^{-\alpha d}$$

α = absorption coefficient of MQW

d = thickness of absorbing material (i.e. the wells)

Therefore the condition for zero reflectivity is $R_\alpha = R_f$ which is equivalent to $R_f = R_b e^{-2\alpha d}$. The front reflectivity is thus required to be equal to the effective rear reflectivity, which is that seen looking into the device from the external surface and including absorption in the cavity.

The above equations describe the reflectivity at resonance, but in order to account for the behaviour of the modulator over a wide range of wavelengths the following more general equations may be used :-

$$R = \frac{B + F\sin^2\delta}{1 + F\sin^2\delta} \qquad \text{where} \quad B = \frac{R_f\left[1 - \left(R_\alpha / R_f\right)\right]^2}{\left(1 - R_\alpha\right)^2}$$

$$\delta = \frac{2\pi nL}{\lambda} \quad \text{and} \; F = \frac{4R_\alpha}{\left(1 - R_\alpha\right)^2} \qquad \textbf{Eqn 2.27}$$

Here L is the length of the cavity from the front surface to the top of the reflector stack, and n is its average refractive index. The resonant condition is thus achieved at $\delta = 0$, $m\pi$ (m integer) and anti-resonance occurs for $\delta = m\pi/2$.

When considering a Fabry-Perot cavity formed with a quarter-wave reflector stack there is one small, but important, difference. Consider the simplest form of Fabry-Perot cavity, say, for example, a cleanly cleaved slab of semiconductor in air. In this case the front and rear amplitude reflectivities are given by the Fresnel equation:

$$r = \left(\frac{n_1 - n_2}{n_1 + n_2}\right) \qquad \textbf{Eqn 2.28}$$

Which will be negative for the front surface, implying a change of phase, but positive for the rear surface. Therefore, one would require the cavity thickness to be an integral number of half-wavelengths, i.e. an integral number of whole wavelengths for the round trip, in order for resonance and complete destructive interference to occur. This situation is altered for the modulator structure, for a π phase change also occurs at the reflector stack. The stack effectively has a large refractive index and so the Fresnel equation above becomes negative. With π phase change occurring at both reflectors it is necessary to make the cavity thickness an odd integral number of quarter-wavelengths, so that the interfering waves are half a wavelength (π) out of phase at resonance. The cavity length is then given by:

$$nL = (2m + 1)\frac{\lambda}{4} \qquad \textbf{Eqn 2.29}$$

where n is the refractive index in the cavity and m=(0,1,2...)

Further theoretical and experimental details of reflector stacks grown on GaAs-on-Si are discussed in Chapter 5, we have concentrated here on what is essential to understand the basic device operation.

We have seen how the first studies that considered integrating a quantum well modulator and a reflector were driven by the desire to increase the interaction length between the light beam and the quantum wells. This led to the incorporation of a reflector stack on the back of the device, which, with an anti-reflection coating on the front, resulted in a double pass device. The next step was to forego the anti-reflection coating and utilize what were up to then considered the undesirable Fabry-Perot effects. Both absorption and refractive index changes can be used, the two being linked by the Kramers-Kroenig transformation. Indeed, early studies tended to concentrate on index modulation - at energies below the band gap where index changes should dominate. Given an increase in the refractive index the path length in the cavity increases thus moving the resonance to longer wavelength. Therefore, at fixed wavelength a substantial change in reflection should be achievable. High finesse resonators were used to maximize the effect of index changes, but performance was limited due to background absorption. As a result the reflectivity did not fall to zero as intended. In order to optimize performance one can adjust the following variables: i) the cavity length, ii) the front and rear reflectivities, iii) the operating voltage, and iv) the properties of the active region. Moving the operating point to longer wavelength, by increasing the cavity length, moves the resonance further from the band-gap and so reduces background absorption. Unfortunately, the index changes are also diminished, requiring higher operating voltages to maintain the same performance.

The alternative to index modulation is absorption modulation, as exemplified by the AFPM device. Here the absorption is used to balance the mirror reflectivities and so create the condition of near zero reflectivity. Theoretical calculations predicted a contrast ratio of >23dB, with a 2.6dB insertion loss, for an operating voltage of 12V. In terms of operating bandwidth a contrast ratio of >10dB was claimed for less than 3dB loss over a 7nm range. The theoretical promise of such devices was borne out by the experimental results [Whitehead *et al* 89(1) and 89(2)]. A 20dB contrast ratio was measured at 860nm, for a 3.5db insertion loss, at 9V bias. At the same wavelength the reflection change was 42.6%, increasing to a maximum of 66.8%-13.1%=53.7%. The results for operating bandwidth were equally

successful with greater than 10dB measured over 4nm, and ΔR=40% over 7nm. The difficult task faced in this thesis was to combine GaAs on Si operation with comparable device performance.

2.5 STRAINED QUANTUM WELLS AND AFPMS

In *Section* 2.2 the effect of strain on the absorption spectra of GaAs on Si MQW structures was discussed. In order to assess the impact of these changes on the AFPM design and performance it was decided to model the complete structure. This was done by inputting measured absorption data into a model of the Fabry-Perot cavity. By the use of real experimental absorption spectra in the modelling process maximum accuracy could be obtained. Any number of absorption spectra could be input, so dependency on well width or field strength could be studied. However, the best results were obtained for a 95Å well thickness. The device used was CB306, a 50 period MQW with 95Å GaAs wells / 60Å $Ga_{0.7}Al_{0.3}As$ barriers. The full experimental results for this and other *pin* structures are presented in detail in Chapter 3, for convenience the absorption spectra for CB306 are reproduced below. The predicted superposition of the heavy and light hole excitonic transitions is clear, as is a small shift to longer wavelength of the exciton peak. Furthermore, some degree of broadening is apparent compared to the unstrained case.

In addition to being dependent on the absorption characteristics in the active region we previously stated that the AFPM was sensitive to the front and back reflectivities, the cavity length, and the operating voltage. All these parameters could be varied on the model and it is worth discussing some of the issues that arose in device design.

At resonance the reflectivity of the AFPM can be plotted against absorption in the cavity αd, as shown in Fig 2.15 [Whitehead *et al* 89(1)]. Where α is the absorption coefficient of the MQW material and d is the thickness of the absorbing material. For normally-on operation the absorption should be as low as possible in the unbiased state, such that insertion loss is minimized; this requires that the resonance be located several nanometres to the long wavelength side of the exciton peak. When a bias is applied the exciton shifts to longer wavelength, increasing the absorption at resonance,

and so producing a minimum in reflectivity. Further increasing the bias results in the effective rear reflectivity being so attenuated that it ceases to balance the front reflectivity, thereby resulting in an overall increase in reflection. The separation of the excitonic peak and the resonance in the unbiased state is of critical importance. If the gap is too large the required bias will be excessively high. This may in turn result in broadening of the excitonic peak, such that the required change in absorption is no longer possible. For too narrow a gap the background absorption in the unbiased state will be high, increasing the insertion loss and lowering the achievable contrast ratio. Unfortunately the GaAs-on-Si excitonic peak is slightly wider than on GaAs. Therefore for the same operating voltage the insertion loss will be higher, and vice versa. By adjusting the length of the cavity in the model the optimum separation could be achieved. In practice (see Chapter 5) the growth variations are such that obtaining the optimum performance is as much the selection of the best part of the wafer, since uniform growth to the desired thickness can not presently be achieved.

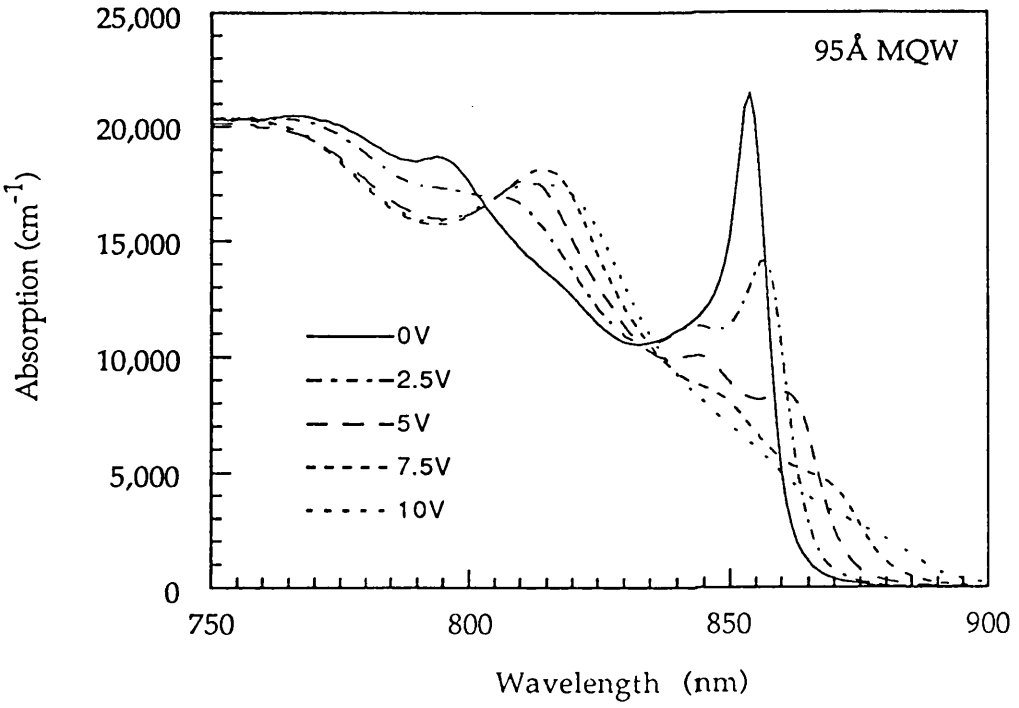


Figure 2.14 *Electro-absorption spectra for CB306, a 95Å well 60Å barrier MQW grown on a silicon substrate. Note the single excitonic peak at ≈ 855nm.*

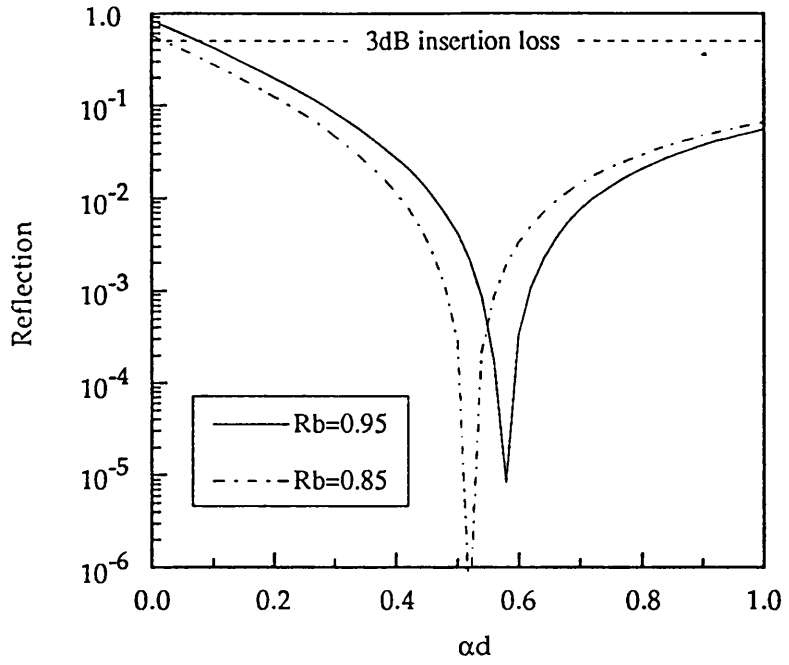


Figure 2.15 *AFPM reflection v absorption at resonance for two different values of stack reflectivity. Also shown is the 3dB insertion loss limit.*

Fig 2.15 also shows the effect of a change in the rear reflectivity. The higher the rear reflectivity the lower the insertion loss of the device will be. For this reason it was necessary to pay particular attention to the performance of GaAs-on-Si reflector stacks. Unless high reflectivity can be achieved a substantial insertion loss will result. The 95% reflectivity shown in the figure is readily attainable on GaAs substrates using a 12 period reflector stack, this was thus taken as a performance yardstick for comparison with stacks grown on silicon. A reflectivity of 85% results in a significant increase in insertion loss, and yet useful performance can still be obtained, therefore this represents a useful lower limit. Increasing the reflectivity beyond 95% would also be advantageous, since for $\alpha = 0$ the AFPM reflectivity becomes solely dependent on the stack reflectivity, rising to 100% as R_b becomes 100%. In modelling the AFPM on Silicon performance the front reflectivity was defined by the air-semiconductor interface, while the back reflectivity was derived from the 96% measured for a 15 period GaAs on Si reflector stack (see *Chapter*

5). Due to the close index match between the MQW and the stack this value falls to 86.5% within the cavity. By contrast a reflector stack measuring 98.5% in air would give 95% reflectivity within the cavity, as shown in Fig 2.15 above. The model showed that for the measured changes in absorption with applied field of CB306(95Å MQW), a reflection change of 40% and a contrast ratio of 10dB could be obtained for an applied bias of 5.7V. The modelled reflection spectra for this structure is shown in Fig 2.16 below.

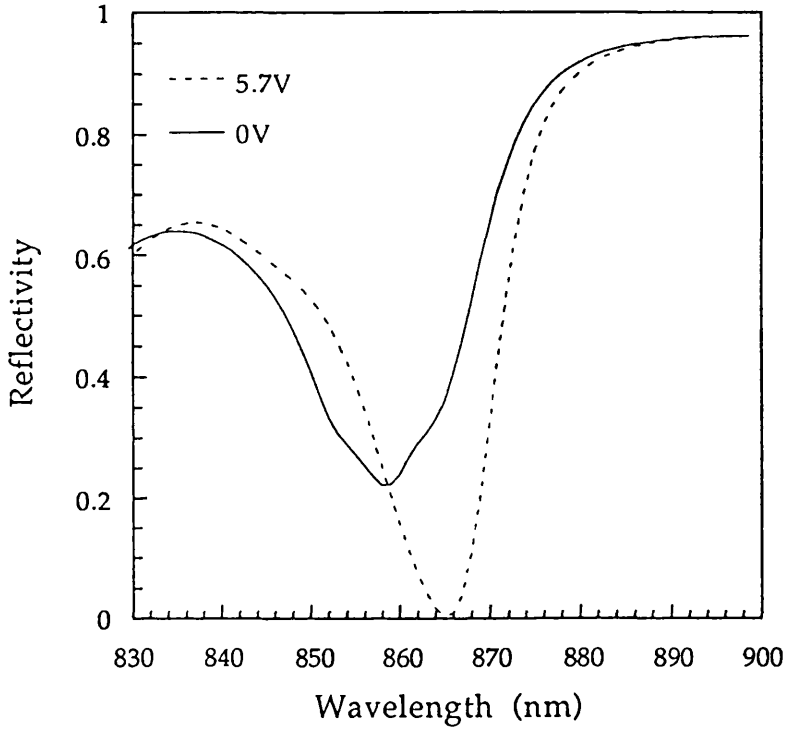


Figure 2.16 *Modelled reflection spectra for an AFPM on silicon using experimentally measured absorption data from CB306 (95Å MQW). The graph shows a 40% reflection change and a contrast ratio of 10dB.*

An interesting variant mentioned in the introduction is that of the normally-off device [Whitehead *et al* (90)]. In this configuration the exciton peak in the unbiased state is located at the resonance, such that the reflectivity falls close to zero. Upon application of a bias voltage the absorption falls, unbalancing the front and rear reflections, and so leading to an increase in reflectivity. To maximize the absorption change 150Å wells may be used. These are more

sensitive to the applied field, the reduced quantum confinement resulting in oscillator strength being lost more rapidly. With greater sensitivity to field lower voltage operation is possible. Experimental results demonstrate a contrast ratio of 6.7dB at 3.5V for an insertion loss of 3.2dB. A 3dB contrast ratio was also possible for only 1V bias. The significance of these results is not so much in the figures themselves, which in essence represent an alternative set of compromises, but in the manner of operation. By changing from a state of low reflectivity to high reflectivity, rather than *vice-versa*, a new functionality is bestowed upon the AFPM, allowing its use in SEED-type applications.

While all the modulators described in this thesis used the air-semiconductor interface to define the front reflectivity, it is possible to increase the reflectivity by the incorporation of a front reflector stack. The result of this is to increase the cavity finesse so that less absorber is required, leading to a reduction in the drive voltage. Such an approach has been demonstrated by [Yan *et al* (90)] and [Zouganeli *et al* (91)] the latter obtaining a contrast ratio of 15dB at only 2V. However, none of these devices demonstrate a clear all-round advantage over the design compromise utilized here. In addition to the extra complexity of such devices one also has to consider the reduced optical bandwidth, possibly higher insertion losses, and an increased sensitivity to both temperature and cavity length. These issues have been covered in some detail by references [Zouganeli et al (90), Yan and Coldren]. For the purpose of studying the application of microresonator devices grown on silicon, *vis-a-vis* GaAs, it was sensible to concentrate on one form of device so as not to cloud the comparison between the two. It is likely that the final choice of device parameters will rest on the precise application envisaged, requiring consideration of the relative importance of contrast ratio, reflection change, optical bandwidth, temperature and growth tolerance, and design complexity.

Chapter 3

Growth and Material Properties of Gallium Arsenide On Silicon Structures

3.1 GROWTH PROBLEMS AND DISLOCATIONS

In Chapter 1 the main problems associated with GaAs on Silicon growth were introduced, namely the 4.1% lattice mismatch between the two materials, the mismatch in the linear thermal coefficients of expansion, and the polar (GaAs zincblende lattice) on non-polar (Si diamond lattice) growth. The material outcome of these problems is the generation of dislocations, microcracks and anti-phase domains (APDs) in the epitaxial layer. The purpose of this chapter is to discuss these problems in more detail, and to outline various methods of improving epilayer quality. This is followed by an investigation of the material quality of the devices reported in this thesis, with particular reference to structural analysis and surface studies. The findings here mostly describe GaAs grown on (100) Si substrates, the standard orientation in the electronics industry, although growth on other substrates has been studied e.g. reference [Northrup]. There is not space here to describe in detail theoretical and experimental studies of the dynamics of growth initiation, but interested readers can refer to references [Northrup, Kaxiras *et al*, Fotiadis and Kaplan, Uneta *et al*, Maehashi *et al*, Lopez *et al*, Bringans *et al*, Soga *et al*, Woolf *et al*]

3.1.1 Lattice Mismatch

Bulk GaAs has a larger lattice constant (5.653Å) than Si (5.431Å) i.e. there are 25 atomic planes of Si for every 24 of GaAs. Therefore, when a GaAs epitaxial layer is deposited on Si, dislocation free growth would require that the GaAs lattice be compressed in the epitaxial plane, with a corresponding increase in the lattice dimension along the growth direction. The silicon, being much thicker, will be more resilient to changes in lattice dimension and will only expand a negligible amount. Unfortunately, the energy required to compress the lattice may exceed that required to form strain relieving dislocations. This is true for all strained layer epitaxial systems. Furthermore, it is found that the strain energy is proportional to epitaxial layer thickness, so that up to a certain "critical thickness" [Van der Merwe] the strain will be accommodated by lattice deformation, but beyond this point dislocations will be generated. For low

levels of strain this critical thickness can be several hundred Angstroms, enough for some devices to be made without significant dislocation densities. However, for GaAs/Si the lattice difference is so large that as soon as a uniform layer of GaAs is deposited on silicon it is likely to have exceeded the critical thickness, so that all device structures will contain a certain number of dislocations. Several models for the critical thickness have been developed, first by [Matthews and Blakeslee] giving t_c as 1.4nm. [People and Bean] estimated t_c as only 0.8nm. A later analysis by [Cammarata and Sieradzki] included the effect of surface stresses, in addition to those of in-plane elastic strain and interfacial dislocations. This predicted that larger critical thicknesses will be achieved when the stress-free lattice parameter of the film is greater than the lattice parameter of the substrate. Even so a figure of only 1.2nm was predicted for a 4.1% mismatch.

The difference between strain relief by dislocation and accommodation by lattice deformation is illustrated in Fig 3.1a and b. It is important to note that the dislocated structure is in a relaxed state, that is the strain has been relieved by the presence of the dislocation. In this state a dislocation will be required at least every 25 atomic planes. In the structure that is not dislocated the strain is accommodated in the lattice, thus altering the properties of the epitaxial layer. In reality one normally has a combination of the two cases, dislocations are generated but a residual strain remains in the epitaxial layer. The growth is then termed partially or completely incoherent, depending on how much of the strain is taken up by the dislocations. Reduction of the dislocation density to a level of ~$10^4 cm^{-2}$ remains an elusive goal, but much work has been done in progressing towards this objective.

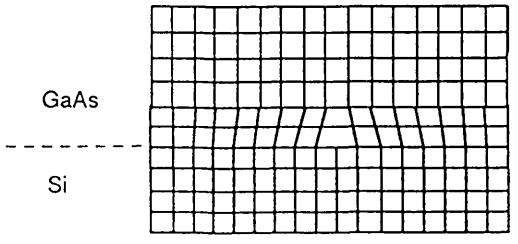


Figure 3.1 a *Schematic of GaAs on Si epitaxial growth showing dislocation relieving strain*

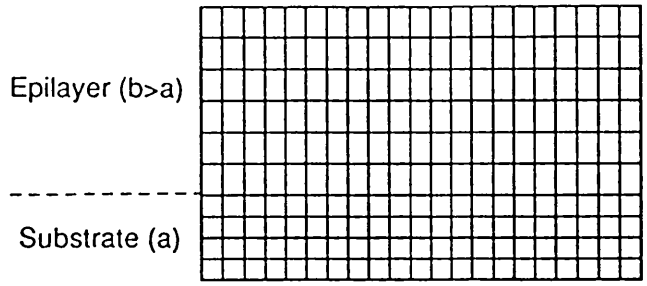


Figure 3.1 b *Schematic diagram showing deformation of the epilayer lattice by strain.*

The idealized GaAs/Si interface is shown in Fig 3.2, indicating the atomic arrangement when no dislocations are present. The figure shows growth on a (100) Si substrate viewed from the [011] direction. These directions can be more easily understood by reference to Fig 3.3, the (100) plane being that of the cube face parallel to both the y and z axes. The figure also shows an Anti-Phase Boundary (APD) which we will discuss in *Section 3.1.2.*

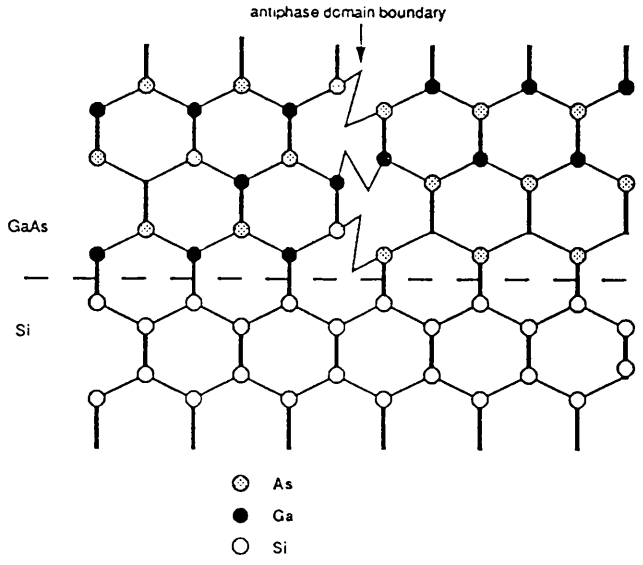


Figure 3.2 *Atomic arrangement of GaAs/Si showing an antiphase domain.*

Due to the lattice misfit, the ideal case shown in Fig 3.2 is disturbed by the formation of dislocations, generally classed as Type I and Type II and shown schematically in Fig 3.4 below. It can be seen that for the first case the Burgers vector b is parallel to the interface, while type II Burgers vectors are inclined to the interface [Fang *et al*]. The type I dislocations are screw type dislocations along the [001] growth direction. They are thus very efficient in accommodating the lattice mismatch, unlike type II which have a Burgers vector of b=±a/2<110>, at 45° to the plane of the substrate, therefore requiring a greater number to accommodate the same lattice mismatch. Identification of the different dislocations is not easy, for when viewed from the (110) projection all dislocations along, for example, [011], [10$\bar{1}$] and [$\bar{1}$12] will appear the same, in this case running at ~55° to the interface. This can be observed in the TEM photographs of MOCVD grown structures that are discussed in *Section 3.4.2*. By using several different viewing angles during TEM the nature of the dislocations can be analysed in greater detail [Tamura *et al*].

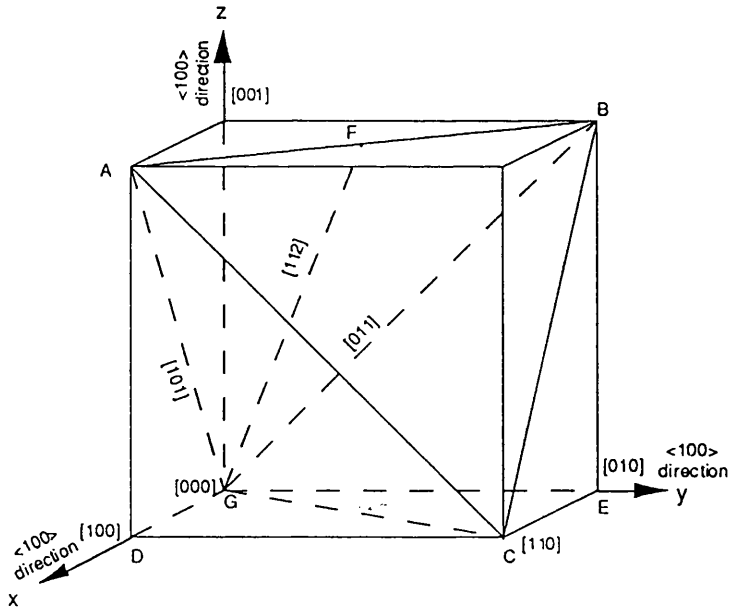


Figure 3.3 *Diagram showing lattice directions. Families of directions are labelled by angular brackets e.g. <100> denotes a family of directions which includes [100], [010], [001] etc.*

At present no significant difference in the effect of the various type II dislocations has been observed. On the other hand type I and type II

dislocations affect the material quality to different degrees. While type I will not propagate far into the epitaxial layer, the type II dislocations thread their way upwards because the GaAs (111) planes slip easily. The latter are therefore more detrimental to the material quality and are mainly responsible for device degradation. As well as providing non-radiative recombination centres, they can act as possible shorts and cause enhanced impurity into the active region. These two types of dislocation have been directly observed using high resolution electron microscopy [Tamura *et al*]. Material quality will be improved if type I dislocations can be encouraged at the expense of type II, and this is found to occur when a tilted substrate is used which has a series of atomic steps across the surface. These steps encourage the formation of type I dislocations, and also, as will be discussed later, discourage the formation of APDs.

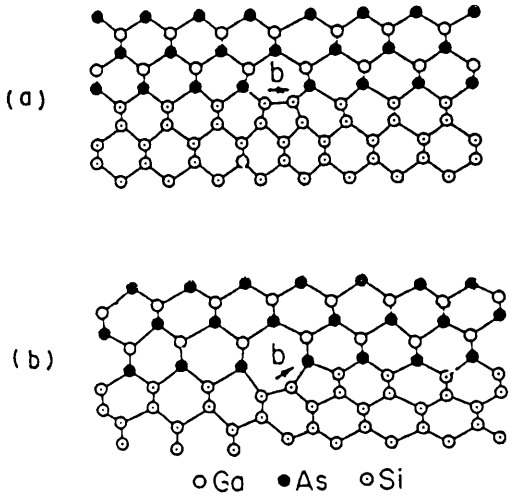


Figure 3.4 *Type I and Type II GaAs on Si Dislocations (after [Fang])*

3.1.2 Anti-Phase Domains (APDs) and the Problems of Polar on Non-Polar Growth

One of the early problems found with GaAs/Si growth was that neither the Ga nor the As has a particular preference for bonding to the silicon substrate. This results in the formation of Anti-Phase Domains (APDs), areas in which the atomic arrangement at the interface changes from Ga nucleation on the Si substrate to As nucleation. These are illustrated in Fig 3.2. The APDs can be revealed by preferential etching, using molten KOH

[Noge], and result in surface roughness and a deterioration of material quality. It was obvious that a means of eliminating the APDs had to be developed, but the solution was not as straightforward as simply introducing one of the constituents before the other, in the form of a "prelayer". Although this helped, it did not entirely remove the problem as the process was likely to encourage three dimensional island growth, rather than uniform two dimensional planar growth. However, the solution to the problem has been widely acknowledged as the utilization of an off-oriented silicon (100) substrate. Growth on oriented and off-oriented substrates are shown schematically in Fig 3.5 below, after [Mizuguchi]. The substrate is cut at a slight angle, usually a few degrees off (100) towards [110], leaving a regular series of atomic steps across the surface. These are believed to encourage uniform single phase nucleation of GaAs.

While there is general agreement that an off-oriented substrate helps reduce APDs [Fan] [Morkoc *et al*] [Woodbridge], and improves surface quality, the nature of the mechanism is not clear. Full investigation and understanding of the effect is unfortunately beyond the scope of this thesis, requiring as it does an intimate knowledge of the surface structure, the kinetics of growth nucleation, the surface energies and the material differences. However we can consider two alternative views as put forward by [Mizuguchi] and [Fang].

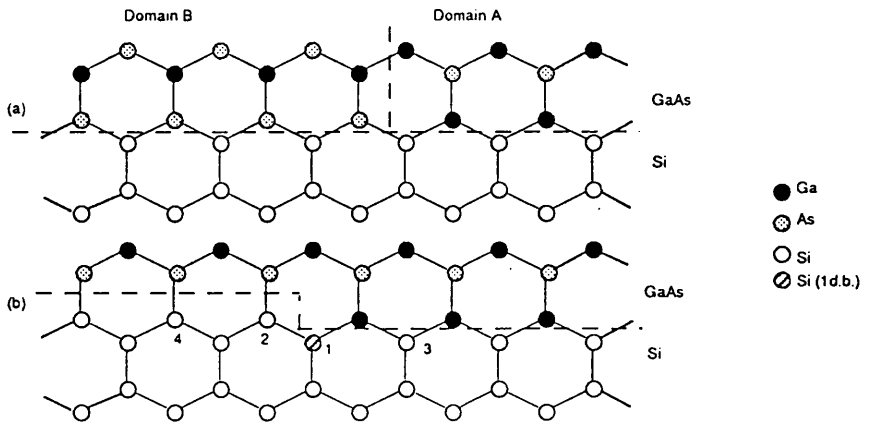


Figure 3.5 *Oriented and Off-oriented GaAs on Si Nucleation (after Mizuguchi)*

Mizuguchi uses Fig 3.5 as the basis of his argument, in which site 1 has one dangling bond, while site 2 has two dangling bonds. Ga atoms have a

tendency to attach to the single dangling bond, while As tends to attach to the double dangling bond, thus eliminating the APDs and resulting in single phase growth. The uniform series of steps have another advantage in that they provide a high density of nucleation points, increasing the tendency to two dimensional growth, rather than 3-d growth followed by island coalescence [Morkoc *et al*]. Note that the series of steps is important in order to conserve the pattern of growth; a step down followed by a step up, as found on a nominally flat Si surface, will result in the formation of APDs [Morkoc *et al*]. Step formation on Si surfaces has been studied by Scanning Tunneling Microscopy in reference.[Schwartzentruber *et al*]. Of particular importance was the formation of double atomic steps, and the relative densities of single and double steps, with the latter believed to encourage the formation of APDs.

The above argument is at odds with that of [Fang (90) *et al*] and [Demeester *et al*]. Here the presence of single atomic steps is believed to be a disadvantage likely to cause APDs. Instead, double atomic steps are proposed for their elimination. These double steps are energetically favourable on substrates misoriented by ≥1.6°, although 2° is preferable to reduce the number of monosteps to a minimum. Once more it is the action of the Si dangling bonds that is of key importance. What happens to these is, unfortunately, a very complex issue, but most probably they are used to form covalent or ionic bonds between adjacent atoms. This process is called dimerization, and covalent bonded dimers are known as symmetric dimers. Ionic bonding is equivalent to asymmetric dimerization and leads to an orthogonal 2x1 unit cell reconstruction as found on Si. The ionic bonding is elastic and requires charge transfer and both lateral and vertical atomic movement. Thus at steps in the Si surface the dimerization will alter the nature of the dangling bonds and influence nucleation. The steps can then be classified according to :-

1) single or double atomic step

2) edge parallel or perpendicular to surface dimerization

It is believed that APDs are energetically unfavourable on double atomic steps perpendicular to surface dimerization, while they are aided by monolayer high steps. These two situations can be observed in figure 6 below. Pre-exposure to either Ga or As has been proposed as a means of reducing APD formation [Bringans *et al*] [Masselink *et al*], although As is usually preferred as it has a reduced tendency to cling together, so avoiding more than a single layer being deposited. If Ga is used care has to

be taken over the deposition temperature, and uniformity of the substrate heating is critical.

It is worth noting at this stage that an alternative to using a Si (100) substrate off-oriented ~2° towards [011] is to employ a (211) substrate as proposed by Kroemer [Wright *et al*] [Demeester *et al*]. On this surface the Ga and As atoms have preferential bonding sites, with the latter bonding to lattice sites with double dangling bonds, and so APDs are avoided. Another advantage is the higher density of nucleation sites compared to off-oriented Si [Fotiadis and Kaplan], resulting in two dimensional growth occuring at an earlier stage. Nevertheless, due to the incompatability between this substrate and present commercial Si processing this solution has not been studied very intensively. Research is also handicapped by the immaturity of knowledge in (211) preparation and processing. Other substrates that have been studied include Si(111) [Maehashi *et al*], Si(110) [Lopez *et al*], and Si(100) misoriented towards [001] ([Adomi *et al*]). The issue of initial growth nucleation has also been studied theoretically with the intention of encouraging two dimensional growth [Kaxiras *et al*] [Uneta *et al*].

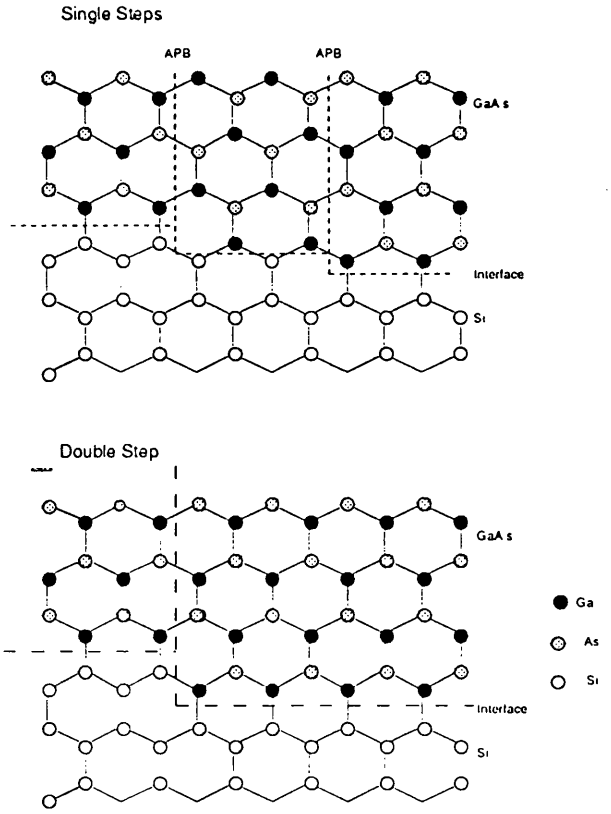


Figure 3.6 *Growth of GaAs on single and double stepped silicon, after [Demeester et al].*

APDs can be described as charged structural defects [Fang (90) *et al*]. Ga-Ga bonds have an electron deficiency and so act as acceptors. As-As bonds have excess electrons and act as donors. Thus both combined will act as a compensated semiconductor. The dislocation running along the boundary will also act as a non-radiative recombination centre, and will adversely affect leakage currents.

So far we have assumed the deposition of GaAs, in some cases with a pre-layer of Ga or As, on pure Si substrates. This need not always be the case, but it does provide a situation that we can at least begin to understand. However, in order to make progress it is essential to be able to provide a clean Si surface, which in itself is not trivial. Contaminants on the surface will obviously affect nucleation so the clean-up stage is very important otherwise rough, three dimensional growth will ensue. Of critical importance is the removal of the oxide layer (SiO_x) and any other oxygen/carbon contaminants. Removal of the oxide is usually done by thermal desorption at ~1000°C, although this is not practical if one is hoping to grow on processed Si substrates, as the devices are likely to be damaged by such high temperatures. For this reason chemical etches have been used as an alternative, followed by thermal desorption at a lower temperature. One possibility is the use of an HF treatment [Soga *et al*], which removes the oxide layer and instead terminates the Si dangling bonds with H, which can then be removed at medium temperatures (≈500°C). The use of Laser Assisted MBE has also been proposed as a means of reducing the APD density [Christou *et al*], using this scheme heat can be applied selectively and two dimensional growth encouraged rather than island growth. This reduces APD density and also results in a reduction of the dislocation density. This is because it is suggested that most of the Type II dislocations, with a/2 <110> Burgers vectors, are created at the island concrescences. A more radical approach still is to nucleate growth with AlAs [Kobayashi and Kawabe] or AlGaAs [Soga *et al*], both of which are claimed to encourage two dimensional rather than three dimensional growth.

While most studies have dealt with the elimination of APDs at the nucleation stage, another mechanism for APD reduction is their self-annihilation with increasing layer thickness [Christou *et al*, O.Ueda (89) *et al*]. In particular, Ueda has studied APDs in the presence of GaP, GaP/GaAsP, and GaAsP/GaAs strained layer superlattices, using (001) substrates off-oriented by 0.4° and 2° towards [110]. It was found that the

size of APDs depended on offset, 0.5-2μm for 0.4° and 10-20nm for 2°. The improvement for the larger offset is consistent with double atomic steps progressively replacing monatomic steps as the off-orientation is increased. The APDs were found to occur when islands coalesced, but were reduced in size as the layer thickness increased, finally self-annihilating. It is not known whether the APDs were all initiated at remaining unwanted monatomic steps, or whether they could also begin at diatomic steps, but had been previously unnoticed due to their small size which was not detectable by conventional etching techniques.

3.1.3 Thermal Mismatch

Due to the difference in the linear thermal coefficients of expansion of GaAs and Si, large tensile stresses are introduced into the GaAs epilayer when the wafer is cooled from the growth temperature to room temperature. This situation is normally assumed to be like that of a bimetal model, so that the biaxial tensile strain, introduced upon cooling, will be given by :-

$$\varepsilon = \Delta\alpha\,\Delta T = \left(\alpha_{GaAs} - \alpha_{Si}\right)\left(T_g - T_r\right) \qquad \textbf{Eqn 3.1}$$

where T_g=growth temperature, T_r=room temperature, and α=the linear thermal coefficient of expansion. However, α is a function of temperature so we have [27]:-

$$\varepsilon = \int_{\Delta T} \Delta\alpha\, dT \qquad \textbf{Eqn 3.2}$$

The above equation assumes that the epitaxial layer is unstrained at the growth temperature. This requires that the compressive lattice misfit strain is completely relieved by dislocation generation, and that all the tensile strain is thermally induced during the cooling stage. These dislocations are free to move at temperatures above their freeze-in point, and thus may relieve some of the strain during cooling, a point that is discussed below.

The changes in α_{GaAs} and α_{Si} with temperature are difficult to measure and different values are reported in the literature [Landolt and Bornstein], however examples are given in Fig 3.7 below.

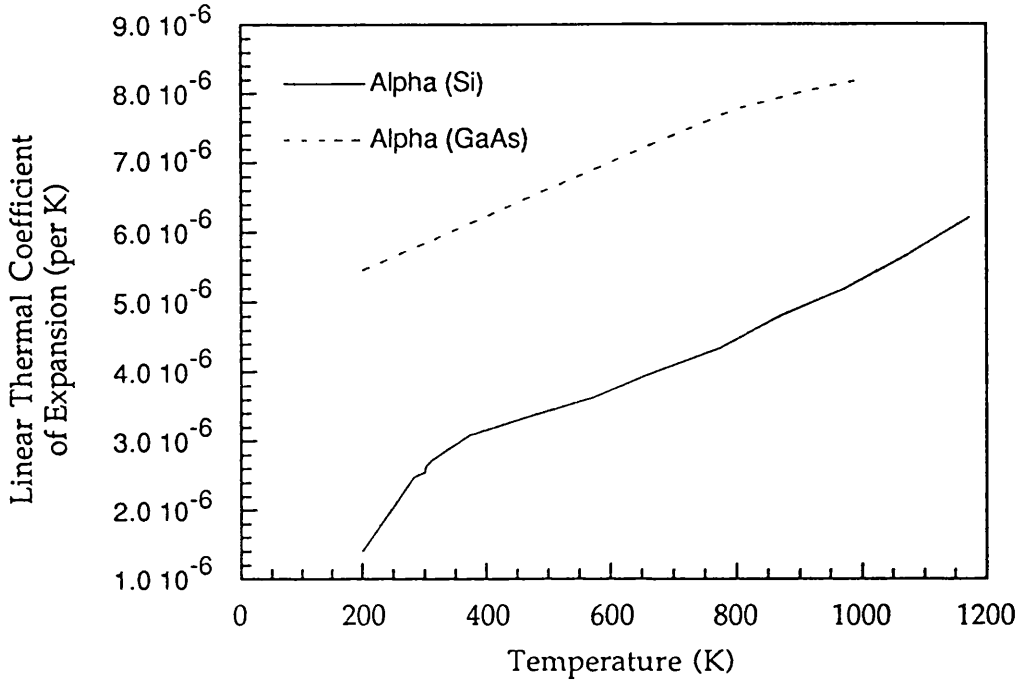


Figure 3.7 *Graph showing the change in the linear thermal coefficients of expansion α_{GaAs} and α_{Si} against temperature.*

Often used are the room temperature coefficients of $\alpha_{GaAs}=6.0\times10^{-6}/K$ and $\alpha_{Si}=2.3\times10^{-6}/K$. The GaAs epilayer attempts to contract at this rate but is confined by the slower rate of the Si substrate, which being much thicker dictates the rate of thermal contraction. The result of this is a large biaxial tensile strain and a distortion of the GaAs lattice. Although the epilayer is typically only a few microns, compared to 0.5mm for the Si substrate, the stresses (up to 1.5×10^{9} dyn/cm^2 [Ueda *et al* (88)] are such that concave bowing or warpage of the wafer will occur.

Layers thicker than ≈4μm normally display a large number of microcracks, due to the thermal stress, running from the surface to the GaAs/Si interface. The wafer warpage can be related to the stress as follows [Demeester *et al*]:-

$$\sigma = \frac{1}{6}\left(\frac{E_s}{1-\nu_s}\right)\frac{D^2}{tR} \qquad (t << D << R)$$

$$= \frac{1}{3}\left(\frac{E_s}{1-\nu_s}\right)\frac{D^2}{r^2}\frac{\Delta z}{t} \qquad (\Delta z << r)$$

Eqn 3.3

where σ = stress of GaAs layer
E_s = Young's modulus for silicon
ν_s = Poisson's ratio for silicon
D = thickness of substrate
t = thickness of epilayer
R = radius of curvature of wafer
r = radius of silicon substrate

The stress can be related to the bimetal model such that

$$\sigma = \frac{E_f}{1 - \nu_f}(a_{GaAs} - a_{Si})\Delta T \qquad \textbf{Eqn 3.4}$$

and then

$$\Delta z = \frac{3(E_f/1-\nu_f)}{(E_s/1-\nu_s)} r^2(\alpha_{GaAs} - \alpha_{Si})\Delta T \frac{k}{D^2} \qquad \textbf{Eqn 3.5}$$

where E_f = Young's modulus for GaAs
ν_f = Poisson's ratio for GaAs

Therefore one would expect that if the stress in the epilayer is accounted for only by the difference in thermal expansion the wafer warpage should be proportional to both ΔT and the epilayer thickness, while it should be inversely proportional to the square of the substrate thickness. The extent to which experimental observation mirrors the predictions of the model, and the means of reducing the strain are a matter of dispute. For instance [T.Ueda *et al*] examined the wafer warpage using a laser scanning flatness tester and found that the bimetal model gave very close agreement. It was observed that wafer warpage increased linearly with epilayer thickness for test layers of 1-4μm as predicted. The use of thicker (1mm) substrates reduced warpage to <10μm for a 4μm layer, again fitting the theoretical predictions. More surprisingly a growth temperature dependence of stress was not observed, the warpage remaining at a constant, and less than estimated, value for growth temperatures of between 600°C and 800°C. Even samples annealed at up to 900°C showed no greater warpage. From these observations it is concluded that the misfit dislocations are responsible for some degree of strain relief, and that these dislocations are mobile down to about 350°C, thus they are able to move in such a way as

to accommodate some of the strain. If this is correct it would make reduction of the strain by growth at lower temperatures difficult, as no advantage would be gained unless a temperature of <350°C could be achieved.

A common outcome of the wafer warpage is microcracking and it might be thought that the lower than expected warpage was due to stress relief by the cracks, however in this case the layers were of <4μm and no cracking was observed.

Like Ueda several other authors [Stolz (91) *et al*], [Neumann *et al*], and [Harris *et al*] only consider the thermal strain, but compressive strain due to the lattice mismatch has been observed. For instance [Yeo *et al*] has shown that for a <0.3μm layer compressive lattice strain exists, although for >0.8μm thermal strain (tensile) is dominant.

3.2 EPITAXIAL GROWTH OF GALLIUM ARSENIDE ON SI

3.2.1 Introduction

The fabrication of complex optoelectronic devices employing quantum wells is only possible due to recent advances in epitaxial growth systems. The most significant of these are molecular beam epitaxy (MBE), and metal-organic chemical vapour deposition (MOCVD), also known as metal-organic vapour phase epitaxy (MOVPE). We have been able to compare both systems in this study, for which device results are presented in Chapters 4 and 5, while in this chapter we concentrate on the material quality of the epitaxial layers grown by the two methods. The particular problems associated with epitaxial growth of GaAs on a Si substrate, as opposed to a GaAs substrate, have demanded alterations in the growth conditions so as to attain a reasonable standard of material quality. Some of these can be classified as optimization of conventional methods, while others have taken a more radical approach. All, however, demand a knowledge of the basic methods of epitaxial growth.

At the simplest level one requires that the desired epitaxial material is deposited on the substrate, and that this growth should be coherent i.e. the deposited atoms should form a regular arrangement that mimics that of the substrate. The nucleation stage is critical and the ideal is normally a monolayer, in which a single layer of atoms is deposited over the entire

surface, a condition that requires the deposited atoms to bind more strongly to the substrate than to each other. Growth of complete layers one at a time does not in fact occur, even when the growth is nominally two dimensional, at least in studies of MBE growth [Joyce]. These found that growth of the second layer starts before the previous one is finished. If, however, growth is interrupted an atomically flat surface is achieved due to dissociation of the upper two- dimensional islands, followed by surface diffusion and reformation. This observation has helped introduce the concept of Atomic Layer Epitaxy (ALE) or Migration Enhanced Epitaxy (MEE) in which the growth is interrupted regularly in an attempt to improve material quality, especially at low temperature. This could be particularly useful for GaAs on Si growth for which thermal strain is of such importance. More typically nucleated growth will occur, in which three dimensional islands form on the surface, these then coalesce to form a two dimensional layer. Much work has been targeted at achieving two dimensional (monolayer) nucleation, in the hope that the lattice mismatch would then be taken up by dislocations at, and parallel to, the interface. These are the most efficient form of dislocations and do not travel through the epitaxial layer, which would then be essentially dislocation free. However, 3-d island growth normally occurs and dislocations are likely to form at the point where two islands coalesce. These dislocations are most often Type II and thus likely to thread their way through the epitaxial layer. Stacking faults and microtwins are also commonplace.

Island growth is more apparent for epitaxy on Si rather than GaAs substrates. This is a result of a combination of factors, namely, contamination of the Si surface, steps on the surface, and strain effects at the interface due to lattice mismatch. The first of these is usually due to the formation of silicon oxides, these are particularly difficult to remove and will seriously disrupt growth. Scanning tunnelling microscopy has shown the difficulty of obtaining an atomically flat Si surface, a number of mono or diatomic steps normally being found. These act as nucleation sites with differing sticking coefficients, causing 3-d island growth and APDs. As has been discussed the intentional introduction of a series of steps, by off-orientation of the substrate, can lead to the elimination of the latter. An additional benefit is that nucleation will be encouraged at a regular array of sites. Nevertheless, this is perhaps a second best solution to the problem as nucleation still retains a 3-d nature. Even in lattice

matched epitaxy the condition of the substrate is critical as, by the nature of epitaxial growth, any defects on the surface will be copied by the epitaxial layer. This will not always be true for strained layer growth as the deposited atoms interact and affect the position of others. Lattice mismatch itself is however the most fundamental drawback to two dimensional nucleation of growth. The first isolated atoms deposited on the surface will bond normally, but the formation of a continuous layer of GaAs is likely to be energetically unfavourable, as it requires the atoms to be confined to the dimensions of the Si lattice. This restriction is lifted for 3-d island growth and thus this form of nucleation is more probable. The point at which island growth becomes energetically favourable was first considered by [Franck and van de Merwe (1949)] in their studies of strained layer growth and is dependent on lattice misfit, such that for small degrees of misfit a strained lattice monolayer would be possible. This was for a time considered the necessary condition for epitaxial growth. In order to ascertain which material combinations were possible reference was made to a phase diagram such as Fig 1.3. The diagram shows the energy gap and the lattice constants for a variety of materials, the lines between points representing the different compositions of ternary or quaternary compounds, for instance $Ga_xAl_{1-x}As$. For any particular lattice constant a vertical line can be drawn intersecting all those material combinations that can be grown, together with their energy gaps. The enormous developments in strained layer systems in recent years have proved that a greater variety of materials can actually be grown. In fact perfectly coherent growth can result for relatively high values of strain (e.g. InGaAs/GaAs etc.) but a new limiting condition applies and that is the maximum thickness of the epitaxial layer that can be grown. Above this limit, known as the critical thickness, misfit dislocations will be generated *(see Section 3.1.1)*. Whether employing MOCVD, MBE or any other form of epitaxy all the above will be critical in determining the final material quality.

3.2.2 MBE Growth of GaAs on Silicon Structures

All the MBE grown structures were grown in collaboration with Philips Research Laboratories by Dr.Karl Woodbridge. The machine used was of a very high specification and is typical of what is now considered a conventional MBE system. The basic principle of which is the vacuum

evaporation of heated solids or liquids in crucibles onto a heated substrate. In order to obtain an even, collision free flow of particles, and a low impurity density it is necessary that the growth should take place under UHV conditions. This has the additional benefit of allowing *in situ* monitoring by RHEED and/or Auger Electron Spectroscopy, a significant advantage over MOCVD which takes place at or near atmospheric pressure, thereby making such monitoring impossible at present. The pressure obtained in the chamber is about 10^{-11} Torr, and an average growth rate of 1μm/hr or approximately 1ML/s, equivalent to 10^{-6} Torr, is typical. The evaporation sources are placed in what are sometimes referred to as Knudsen cells. These basically consist of a crucible, a heater, and a thermocouple. The detail design is critical so as to avoid contamination, produce a stable flux, and allow accurate control of the flow rate. The crucible is normally made from Boron Nitride while the whole is enclosed by a Ta radiation shield. There is a difficult compromise between keeping the temperature down so as not to release impurities while still meeting the flow requirements. This usually leads to modification of the crucible shape and aperture size so that most can no longer be called true Knudsen cells.

The MBE geometry results in growth that is inherently non-uniform, and this requires the use of a rotating substrate. Nevertheless, the question of wafer uniformity is an important one, particularly for AFPMs, and has been investigated in much detail in Chapter 5. For small wafers (2") there is very little variation, but as wafer size increases the non-uniformity becomes significant. On the other hand the non-uniformity is very predictable, the layers being thickest in the middle with a gradual and continuous reduction towards the edge. In principle MOCVD may have the potential for more uniform growth over larger areas, but at present the difficulties in controlling the gas flow exceed the advantages of simpler geometry. This leads to a comparable variation in layer thickness, but unfortunately of a much less predictable nature.

The alternative sources can be introduced by the use of mechanical shutters which take ~0.1 to 0.3s to open and close. This allows single atomic layers to be grown of a particular material, although it becomes difficult to produce very short period superlattices simply because of all the mechanical switching that has to occur. It is possible to use either an As_2 or an As_4 flux. The former can have a sticking coefficient of 1, but the latter is believed never to exceed 0.5. This is because for every two As_4

molecules two atoms from each will stick to the substrate, whilst the other two from each form a new As_4 molecule that desorbs.

The presence of *in situ* RHEED is very useful for monitoring the surface reconstruction during growth. Ideally, the surface should be terminated by a complete layer of either Ga or As but different structures are possible e.g. 4x2, 3x1, 2x4. The RHEED signal is found to oscillate as each layer is deposited so it is actually possible to monitor single layer growth, allowing extraordinarily high control of the device structure. The interface roughness in a high quality system has been estimated to be no more than a single monolayer.

The choice of dopants is to a large extent dictated by the temperatures used during growth as re-evaporation can be a problem. For this reason Be (Gp II) is almost universally used as the *p* dopant, while the same is true of Si (Gp IV) for *n* doping. Enhanced diffusivity of both of these at high doping levels can sometimes be a problem leading to disordering of structures such as MQWs. An answer to this may be in the use of carbon as a p-dopant [Wang *et al*] which can provide very high doping levels combined with low diffusivity.

The MBE system used for the growth of devices in this project was a Varian Modular GEN11. This has full computer control of all furnace temperatures and shutter operations and is capable of growing 3" wafers on a non-bonded substrate stage [Woodbridge]. Two separate Al sources are provided allowing two different rates of flow and thus compositions of GaAlAs. Thermal cleaning of the substrates was carried out in a separate chamber designed so as to avoid contamination of the growth chamber.

3.2.3 MOCVD Growth of GaAs on Silicon Structures

As an alternative to MBE we were able to grow devices using the MOCVD system installed at the SERC Central Facility at the University of Sheffield. Differing in nearly all respects to MBE, this form of growth is nevertheless an accepted production technique, and has been developed equally intensely during recent years. Although at present perhaps less predictable than MBE, the best results are the equal of those obtained on any other system. A particular advantage is in the growth of semiconductors involving phosphorus - a problem with MBE systems. In fact the

possibility of using a wide variety of precursor compounds rather than high purity solid or liquid elements as in MBE is a significant point in favour of MOCVD. This flexibility allows a huge variety of materials to be grown. A downside to this is the difficulty of preparing pure, safe sources. Many of the gases used are extremely toxic requiring a high level of safety measures. The difficulties imposed on the handling of these sources also hinder purification, so that impurities tend to be more unpredictable than is the case for MBE.

The basic principles involved are illustrated in Fig 3.8. Gases are introduced at or near atmospheric pressure into the growth chamber where a thermally driven reaction occurs resulting in deposition of, in this case, GaAs. Alternative precursors can be used for the growth of GaAs, but the most common are Trimethyl Gallium and Arsine.

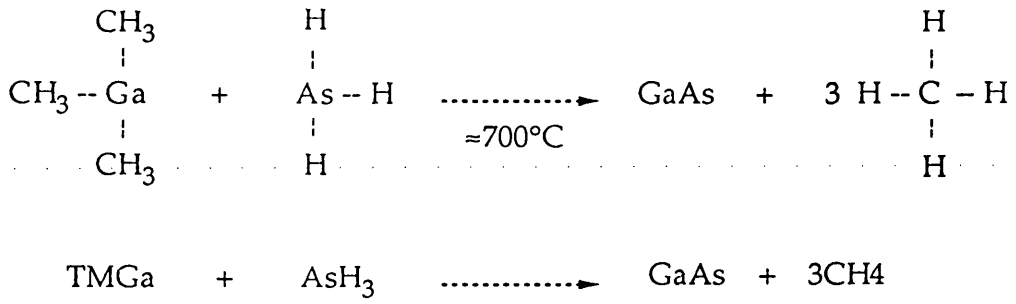


Figure 3.8 *MOCVD growth equations.*

Studies of growth rate against temperature and Gp.III and Gp.V concentration reveal some interesting results [Stradling and Klipstein]. Principally, that the growth rate is more or less independent of excess concentrations of arsine. This is useful as it allows an extra degree of freedom in the growth process, which we found to be helpful in the renucleation of GaAs on Si. The introduction of an excess of Arsine is known to eliminate carbon, a common impurity, from Gp.V lattice sites.

The growth rate is found to be critically dependent on temperature and normally the best morphology is expected in the plateau region, for which the growth rate is also at a maximum. In terms of arsine concentration the temperature can be used to fine tune the growth process. This can be useful for optimization of the different stages of growth, such as nucleation, buffer layers, and device layers.

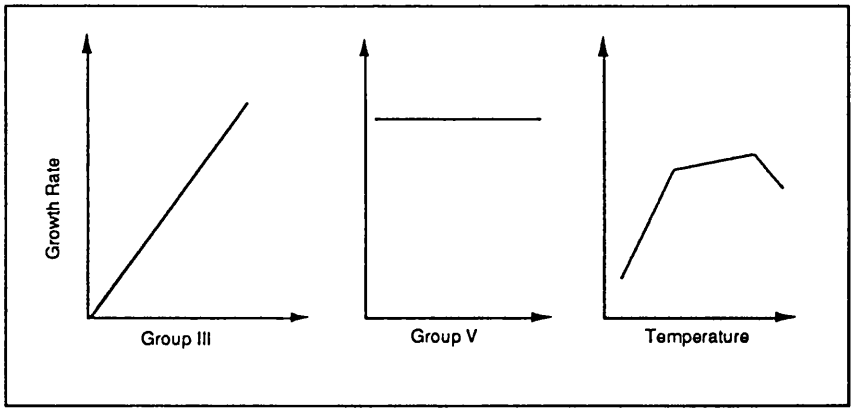


Figure 3.9 *Schematic diagram showing growth rate dependencies in MOCVD on Group III, Group V, and temperature.*

Dopants normally used are Si (*n*-type) and Zn (*p*-type) which are introduced by specially prepared precursors such as disilane and DMZ or DEZ. Unfortunately both Si and Zn are commonly found in the Ga precursor, TMGa, and are difficult to eliminate. This often leads to variations in material quality from batch to batch depending on the precursor quality provided. Another source of unwanted Si during GaAs on Si growth can be the substrate itself [Nozaki *et al* (89) and (90)]. This involves gas phase transport of the Si to the epitaxial layers during growth. Silicon can also be incorporated through diffusion across the GaAs/Si interface, enhanced by defects in the GaAs. A solution to the former problem is to coat the back and sides of the Si substrate with SiO_2 prior to epitaxy [Nozaki *et al* (90), Egawa *et al*], resulting in a background doping of only $3x10^{14}cm^{-3}$. Oxygen is another impurity that can present problems [Goorsky]. It incorporates more easily into GaAlAs than GaAs, in which it is difficult to exceed 10^{15}. The result is a reduction in photoluminescence with a dominant trap at E_c-0.41eV. Other effects are the compensation of Si doping, sometimes leading to misleading measurements of doping level, and an increase in surface roughness. Intentional oxygen doping could be useful for making high resistivity materials.

The dangerously high toxic level of Arsine has encouraged much research into alternative precursors, for example TMA and TEA, but the density of impurities has been too great. However, a safer precursor certainly remains a highly desirable objective and would surely encourage

further development of MOCVD systems. Other research has been directed at the realization of selective growth, in which material is deposited only on certain parts of the wafer. This could be useful in the simplification of device processing and in the development of novel optoelectronic devices. One approach has been by photo-assisted deposition in which laser radiation is used to drive the reaction, another is the development of special precursors sensitive to the surface condition. This could be varied via its structure, composition or crystallography, perhaps by etched channels or mesa areas.

The advantages of MOCVD *vis-a-vis* MBE thus lie in its extra versatility, achieved through more flexible chemistry. It has the potential for a high throughput of a wide combination of materials, and does not require an UHV system, growth taking place at or near atmospheric pressure. This has however hindered the development of *in-situ* monitoring. An advantage may be gained by moving to MOCVD operating at lower pressures (50-100 Torr) in which fewer by-products are present in the system [Sato and Togura]. A common feature of MBE grown epitaxial layers is the number of surface defects. These are often oval defects due to "spitting" of the solid sources and are an order of magnitude higher than for MOCVD.

The structures grown by MOCVD utilized commercially supplied (Kopin, U.S.A.) GaAs coated 3" Si wafers. The growth was therefore not directly concerned with GaAs nucleation on Si, but neither was it simply a matter of proceeding as for normal GaAs lattice matched epitaxy. The supplied substrates were, of course, still under a significant amount of thermal strain and residual lattice strain They also contained a high density of dislocations and were not of a perfectly mirror-type appearance. The problems therefore remained those of nucleation and accommodation of thermal and lattice mismatch. The coated substrates were themselves prepared by MOCVD, and were claimed to contain a defect confinement region although no details were provided of the mechanisms involved. The specification of the wafer was otherwise as follows:

Kopin Wafer Specification

Lot Number:1255 Wafer Number:1-4 Boule Number:9117

Substrate	Si 0.01 to 0.02 ohm-cm *n*-type
Thickness	635μm
Diameter	3"
Orientation	(100) 2°-4° off toward the (011)
Flat Orientation	Primary flat (01 $\bar{1}$) secondary 90° clockwise (011)
Layer	GaAs *n*-type Si doped at $1x10^{18}cm^{-3}$
Thickness	2.8μm
Surface Defects	$<100cm^{-2}$ ($1\mu m^2$ or greater)
Surface Haze	<2000ppm over ≥ 90% of the wafer surface

The MOCVD system used at Sheffield was a MR Semicon 2 x 2 horizontal reactor operating at 900 Torr. The matrix reagents consisted of adduct purified TMG and TMA together with AlGaIn dried 100% AsH_3. The dopant sources comprised 5000ppm DMZ/H_2 and 10ppm SiH_4/H_2. The possible *n* dopants in the system are Ge in Arsine and Germane, and oxygen in TMA - the aluminium source. *P* doping can come from silicon in both the TMA and TMG, and from carbon, mostly in TMA. A poor source of TMA could result in unintentional carbon doping of 2×10^{16}. Carbon and oxygen are mostly found in the AlGaAs or AlAs layers and do not diffuse much so they rarely appear in GaAs. Oxygen creates recombination centres which can be a problem in the AlGaAs barriers. One problem we found was that the C and Si *p* dopants can be compensated by *n* impurities (Ge and O) and thus form what appear to be low doped intrinsic regions when measured by C-V profiling. In fact these layers were highly compensated resulting in poor material quality with low quantum efficiency and even roughening of the surfaces. In the worst cases oxygen doping could reach 10^{17} in 30% AlGaAs, rising to 10^{19} in AlAs. This problem was solved at the expense of a higher *measured* doping level due to reduced compensation.

The Kopin wafers were first cleaved into 3-4cm^2 pieces and blown with antistatic nitrogen before being loaded into the growth chamber. Substrate clean up was performed at 700°C followed by deposition of a 0.1μm GaAs buffer layer at 1.24μm/hr and *n* doping of $1.2x10^{18}$. A high

V/III ratio of 71:1 was used to increase the Ga precursor mobility and therefore obtain a more coherent, smoother renucleation interface.

3.3 IMPROVEMENT OF GALLIUM ARSENIDE ON SI MATERIAL QUALITY

3.3.1 Introduction

In the previous sections we explored the difficulties facing GaAs on Si epitaxy, the basic methods of growth that are employed, and described some of the techniques and processes used in this project. However, it is clear that the straight forward application of conventional methods developed for lattice matched epitaxy can not fully satisfy the requirement for high quality GaAs on Si material. We must thus address the key issue of how material quality can be improved. In addition to our own work in this area there has been a considerable effort by a number of other groups. From these it is possible to discern a number of different approaches which can be classified as follows:-

1) Optimization of conventional techniques
This refers to system such as MBE and MOCVD and includes such concerns as substrate choice and preparation, nucleation procedure, prelayers, growth temperature and pressure, and annealing.

2) Epitaxial layer design
Investigation of the dependence of material quality on layer thickness, buffers, strained layer superlattices, doping planes etc.

3) Selective area GaAs on Si
Under this title we group patterned growth, post-growth patterning, and undercut epitaxy.

4) Alternative epitaxial systems
For example Metal-Organic MBE and Atomic Layer Epitaxy.

5) Novel growth techniques
This includes methods such as epitaxial lift off, overgrowth, and conformal growth.

In practice these approaches are usually mixed, making it difficult to evaluate the true importance of any single change. The results presented in this chapter are a result of research into three of these areas, namely optimized growth, layer design, and selective growth. A summary of developments into novel growth techniques is also presented.

Characterization of GaAs on Si epitaxial layers has involved an enormous number of different techniques. Among these are surface inspection by optical and Scanning Electron Microscopy (SEM), and cross sectional analysis by Transverse Electron Microscopy (TEM). These are on the whole qualitative methods although TEM can be used to measure the dislocation density. An alternative method is to use a defect revealing etch, such as molten KOH, and then count the Etch Pit Density. Comparison between the two methods has revealed a significant discrepancy [Ishida *et al*, Stirland] in the number of dislocations recorded. The EPD figure is usually found to be lower than that measured by TEM, varying from 2/3 to an order of magnitude less. This variability makes it difficult to compare the dislocation densities published by different groups. However, there is no reason to doubt the comparative dislocation densities for results published by the same group. An indication of the difficulty is the withdrawal of early claims for dislocation densities in the $\approx 10^5 cm^{-2}$ range. Later results reverted to a figure of $\approx 10^8 cm^{-2}$ while the best material is now probably in the $10^6 cm^{-2}$ range.

Some methods of characterization have been directly concerned with the crystallinity of the epitaxial layers. These include RHEED and Auger spectroscopy, Rutherford Back Scattering, and X-ray diffraction. Others have concentrated on analysis of the optical quality such as cathodoluminescence, PL and PLE. Investigation of electrical properties has been variously performed by C-V profiling, Deep Level Transient Spectroscopy, and measurement of the implant activation efficiency of low dose, low energy ^{29}Si ions following rapid thermal annealing. This list excludes indirect testing of material quality through device fabrication, which is an area we have been particularly concerned with and for which results are presented in Chapters 4 and 5. As the majority of groups have concentrated on only a few of these many methods comparison of results

is difficult, nevertheless a number of key issues emerge together with some shared conclusions.

3.3.2 *Optimization of Conventional Growth*

The obvious starting point when considering how improved material quality can be achieved is in the choice and preparation of the substrate. One of the most widely used developments has been the use of a misoriented substrate, usually cut 2-4° off (100) towards [011] [Fischer *et al*, Mizuguchi *et al*, T.Ueda *et al* , Stolz (88) *et al*, Bringans *et al*, Pearton *et al*]. This has resulted in the elimination of APDs as described in *Section 3.1.2*. Other substrates have been tried, among them Si(111) [Sobiesierski (91)*et al*, Radhakrishnan *et al*]; Si(110) [Lopez *et al*]; Si(211) [Fotiadis and Kaplan]; and Si(100) on Sapphire [Humphreys *et al*]. Growth on Si(111) is shown to increase the *hh* and *lh* splitting indicating a greater built-in strain, in this case from 2.8kbar measured on (100) to 3.9kbar. A faster transfer to two dimensional growth was reported for Si(110) but at the expense of APDs. The use of a silicon-on-sapphire substrate reduced thermal strain by 50%, but material quality was poor due to dislocations in silicon itself threading into the GaAs. Probably the best alternative from the point of view of material quality remains the (211) orientation. Two dimensional nucleation occurred faster than for (100) presumably due to the greater nucleation site density as predicted by Kroemer. Using this orientation APDs are also eliminated due to the preferential bonding sites for Ga and As atoms. The major drawback to this substrate is its incompatibility with current silicon processing. We therefore decided to opt for off-oriented Si(100) substrates.

Having made a choice of substrate the next critical stage is its preparation for growth. Any contamination on the surface will cause uneven nucleation, resulting in poor morphology of the epitaxial layers. The cleaning of the wafer is an important step in any type of epitaxial growth but it is critical for GaAs on Si. This may be because the type of dislocation is as significant as their number. The basic principle in most surface preparations is the removal of all contaminants, except oxygen, by first degreasing and then proceeding with a series of wet chemical etches. A thin SiO_2 layer is left on the surface which is removed by high temperature thermal desorption in the growth chamber. This approach is

something of a compromise since one would not normally want to oxidize the surface, nor is the high temperature desorption desirable. Furthermore any etchant is in itself likely to leave the surface terminated with some element or other, and these will not necessarily be any easier to desorb. SiC, for example, is very difficult to remove thermally. What is more these etchants can not guarantee the removal of all other contaminants. The aim therefore is to remove such contamination before loading into the growth chamber, which is done at the expense of forming an oxide layer. The presence of the oxide layer is turned to advantage as it can be used as a protective coating, preventing other contaminants bonding to the surface. Removal of the oxide layer need not necessarily be carried out thermally, a Si or Gp.III flux can be introduced [Castagne (1,2) *et al*] to reduce SiO_2 to SiO which is more volatile and will desorb at lower temperature. Another possibility is the use of ion sputtering. Nevertheless, thermal desorption is most common, usually at 850°C to 1000°C for MBE in UHV [Bringas *et al*, Rossow *et al*, Lopez *et al*, Stolz (88) *et al*, Sobiesierski (90)*et al*] or MOCVD in an H_2 or AsH_3 ambience [Pearton *et al*, Goga *et al*, Sato and Togura, O.Ueda (90) *et al*, Suzuki and Chikaura, Mizuguchi *et al*].

The etching procedure is normally a series of oxidation and reoxidation steps, with a final oxidation stage to form the thin protective oxide layer. The MBE preparation procedure was therefore as follows:-

MBE Substrate Preparation

i) *Degreasing of surface (ethanol, IPA etc)*
ii) *Shiraki etch*
iii) *Final oxidation etch*
iv) *Thermal desorption at 900°C*

Most other groups have used either the Shiraki etch or variants upon it [Pearton *et al*, Woolf *et al* (89), Demeester *et al*, Castagne (1) *et al*.] In [Sobiesierski (90)*et al*]a comparison was made between etches with and without the final oxidation step, but better results were obtained upon its conclusion. Alternative approaches have involved the use of a final HF etch to leave a hydrogen passivated surface [Demeester *et al*, Woolf *et al* (89), Castagne (1) *et al*, Fang *et al* (91)] which is then thermally desorbed; a UV-ozone cleaning step [Bringans *et al*]; and the use of low temperature hydrogen/arsine plasma cleaning [Yoon and Reif].

3.3.2.1 Nucleation Procedures

Almost every group utilizes a different nucleation procedure to all the others. In some cases this may be a slight change in the temperature at which growth is initiated, while in others a different material may be used altogether. Nonetheless, some degree of consensus has emerged over the last few years, and that is the widespread application of a two step growth procedure [Sobiesierski (90) *et al*, Masselink *et al*, Yamaguchi(91), Mizuguchi *et al*, Suzuki and Chikaura, Stolz (88) *et al*, Rossow *et al*, Radhakrishnan *et al*, Yamagushi *et al*, Goga *et al*, Yoon and Reif]. This separates the growth conditions of the nucleation from that of the rest of the epitaxial layer, and is normally an attempt to encourage two dimensional growth faster than would otherwise be the case. The first step takes place at lower than normal temperature (300-450°C) and at a reduced growth rate, typically 0.1μm/hr. Once the layer has been deposited the temperature is ramped up to ≈700°C for deposition of the buffer layers. At this point the growth rate is increased to 1-2μm/hr. The importance of the final temperature has been studied in [Goga *et al*]. This procedure is equally successful whether MBE or MOCVD is used. An exception was reported using low pressure MOCVD [Sato and Togura], operating at 3-4 Torr with TEG and AsH_3 precursors. The two step method found to be unnecessary and initial AsH_3 exposure was simply followed by growth at 600°C and 3μm/hr. When using MOCVD another variable is the V/III ratio. We have found an excess of arsine in the ratio 71:1 advantageous [Barnes *et al*]. Others have favoured 50:1 [Suzuki and Chikaura], 40:1 [Soga *et al*]and 20:1 [Sato and Togura]. The variation could be due to the quality of the source used. A high overpressure should inhibit carbon impurities from occupying arsenic lattice sites, but in some cases the large throughput of arsine may be responsible for bringing other impurities into the system. The arsine pressure is also important during nucleation. Often AsH_3 is introduced before the Ga precursor in order to terminate the surface with As, thereby discouraging APD formation. Arsenic pre-exposure has also been used in MBE [Won et al, Radhakrishnan et al, Masselink et al]. Alternatively a Ga prelayer can be used, again with the same intention of discouraging APDs and improving two dimensional nucleation [Bringans *et al*] [Yamaguchi]. Other possibilities are nucleation by AlAs [Kobayashi and Kawabe] or AlGaAs [Soga *et al*]. In the case of AlAs an Al monolayer

was deposited followed by 35 monolayers of AlAs, before the GaAs growth was initiated. The use of an AlAs layer was claimed to reduce the dislocation density by an order of magnitude from 10^8 to 10^7. RHEED studies also indicated that the AlAs was two dimensional. Similar results were reported for a 22.5nm $Al_{0.5}Ga_{0.5}As$ nucleation layer and GaAs epitaxial layer. The Al content allowed the lattice of the nucleation layer to relax at a slower rate than GaAs i.e. it appeared more elastic. In contrast GaAs relaxed to near its bulk value within a few monolayers of growth, thereby forming a larger number of dislocations.

Thermal annealing has been used as a means of reducing the density of dislocations [Yamaguchi (2,3) *et al*] [Tachikawa and Mori] The wafer is heated *in situ* to T_{max}, normally about 900°C, then cooled to T_{min}, which may be as low as room temperature. Finally it is returned to the growth temperature. This cycle may be repeated any number of times. Most studies have found that the dislocation density reduces as the number of cycles is increased. Beyond a certain number of cycles the rate of reduction slows down, and in some cases may actually begin to increase. Dislocation densities of as low as $2x10^6cm^{-2}$ have been reported using these techniques [Yamaguchi, Yamaguchi (1,2,3) *et al*] for layers of ≈4μm. The reduction is assumed to be a result of dislocation annihilation and conversion. Threading dislocations that have travelled beyond the buffer layer region are annihilated, a condition that can be conserved as the GaAs is close to being fully relaxed. The type II dislocations that are closer to the interface are converted to type I edge dislocations by dislocation movement that is driven by the thermal annealing. These can better accommodate the lattice mismatch between the highly strained GaAs at the interface and the Si.

3.3.2.2 Effect of Layer Thickness on Material Quality

Several studies have investigated the relationship between epitaxial layer thickness and material quality [Pearton *et al*, O.Ueda (90) *et al*, Rossow *et al*, Tachikawa and Yamaguchi, Sobisierski *et al*, Woolf *et al*. (90)]. Characterization has employed almost all the techniques described above. From these results one can draw the following conclusions:-

i) Almost all the methods indicate that material quality improves with layer thickness. The improvement is drastic over the first few μm but continues up to 180μm, the thickest that have been grown [Tachikawa and Yamaguchi]. There are two clear exceptions to this rule as follows:-

ii) For layers thicker than ≈4μm microcracks normally appear. Sometimes they may be clearly visible, at others they are difficult to observe without first etching the surface.

iii) The wafer warpage is approximately proportional to epitaxial layer thickness, and is a result of thermal mismatch between the two materials.

The effect of microcracking on the modulator structures is discussed in the next two chapters, and is rather less than may have been expected. The problems become more severe if the surface has been etched as the etchant attacks and widens the microcracks. This can drastically affect the electrical characteristics of the layers [Sobiesierski (90)*et al*]. Interestingly, once the cracks have developed there is very little change in their density with increasing layer thickness. The intercrack spacing was measured as 100-300μm for 10μm layers and for 180μm layers [Tachikawa and Yamaguchi]. The most detailed study has been [Pearton *et al*]. in which particular attention was paid to the Si implant activation energy efficiency. This was found to match that of GaAs on GaAs epitaxy for a 4μm layer thickness, just below the onset of microcracking. However, at this thickness the dislocation density was felt to be too high for the fabrication of minority carrier devices.

3.3.2.3 Effect of Growth Temperature on Material Quality

Due to the problem of wafer warpage attempts have been made to reduce the growth temperature. If this could be achieved the thermal strain upon cooling to room temperature should be substantially reduced. However, comparison of equal thickness wafers grown at both 800°C and 600°C [T.Ueda *et al*] showed little reduction in warpage. In fact, annealing of the wafer at temperatures of up to 900°C made little difference. There is thus a

divergence between the bimetallic model and what is actually observed. The warpage was found to be less than one would expect using that model. One can surmise that some warpage is relieved at high temperature through the movement of dislocations, and therefore the warpage is less than it would be if the dislocations were not free to move. Beyond a certain temperature the extra thermal strain would thus appear to be compensated by dislocation movement, and this temperature was calculated as 350°C. It was concluded that further reduction in warpage would require growth at temperatures below this.

Some progress towards this target has been achieved, but up to now has been mostly on GaAs substrates. GaAs/$Al_{0.5}Ga_{0.5}As$ quantum wells were grown at 350°C [Sekiguchi *et al*] and demonstrated narrower PL FWHM (9.4meV) than at 620°C (16.8meV) indicating smoother interfaces. Unfortunately PL intensity was reduced as a result of higher non-radiative recombination. Growth at even lower temperatures has been reported by AT&T [Eaglesham *et al*] in which limited thickness epitaxy (5500Å) was possible at 240°C. Beyond this thickness growth became amorphous. In fact, no limiting temperature for epitaxy was found *per se*, rather a limiting thickness for any particular temperature. Even if thicker layers can not be achieved this result could be very significant for GaAs on Si nucleation and prelayer formation.

3.3.3 Improvement of Material Quality by Layer Design

Despite significant progress in nucleation and growth processes it is presently still accepted that a great number of dislocations will be generated at the GaAs on Si interface. The purpose of most layer designs therefore is to minimize the number that penetrate the active region. One method of doing this is to introduce a Strained Layer Superlattice (SLS) into the buffer. This consists of a number of alternating layers of two slightly lattice mismatched materials. Each layer is less than the critical thickness of the material combination being used, therefore no new dislocations will be introduced by the superlattice itself. One common combination is InGaAs/GaAs [Woodbridge *et al*, Nichimura *et al*, Nozawa and Horikoshi (91)]. Investigation by TEM has revealed that a number of threading dislocations and microtwins are bent at the interface between the buffer material and the SLS. These then travel harmlessly along the

direction parallel to the interface, are annihilated, or are converted to the more desirable Type I pure edge dislocations. There is a strong strain field associated with the SLS and this is assumed to be responsible for bending out the dislocations. We were able to observe a similar, although reduced, effect with GaAs/GaAlAs reflector stacks, see also [Yamaguchi (2) *et al*]. These do not themselves introduce any strain, but they will be strained due to thermal effects, and so the mechanism is presumed to be similar to that of SLS. The results of TEM analysis on these samples is given in *Section 3.4.2*.

Much experimentation has been carried out with the intention of discovering the ideal compositions, layer thicknesses, and position of the superlattices. Unfortunately this has resulted in little common agreement, for example, preferred Indium compositions have varied between 6% [Nishimura *et al*], and 30% [Nozawa and Horikoshi (91)]. Other material combinations have been InGaAs/GaAsP [Nishimura *et al*, Yamagushi *et al*, El-Masry *et al*], GaAsP/GaP, GaAs/GaAsP [O.Ueda (90) *et al*, Whelan et *al*] and multiple In planes or doping [Tamura *et al*, Watanabe *et al*] The bending of dislocations is often helped by thermal annealing which enhances their mobilization and subsequent interaction. It has to be said that there is some dispute as to the actual value of strained layer superlattices, one view being that deflection of dislocations is usually followed by their reemergence higher up in the epitaxial layer [Woodbridge *et al*] and that buffer thickness is of primary importance. Certainly there is no disagreement that the one sure way of improving material quality is increasing GaAs thickness, excepting the problem of microcracking. Some claims for dislocation density reduction by the use of SLS are impressive, for example in [Nozawa and Horikoshi (91)] a figure of $<1x10^5cm^{-2}$ is quoted for a total epilayer thickness of only 3.5μm. It is interesting to note that this sample was grown by MEE, allowing a temperature of only 300°C to be used for deposition of the strained layer superlattice. It is claimed that at this low temperature misfit dislocations cannot be easily generated, nor are they so mobile. For this reason more strain can be stored in the SL and fewer dislocations propagate into the upper GaAs layer.

Interesting alternatives to strained layer superlattices have included Si interlayers of 2-3 monolayers thickness and ZnSe buffer layers. Some dislocation bending was observed for the Si layers, which are assumed to block dislocations due to the strong Si-Si covalent bonds. In addition, the

high stress required to create new dislocations in Si makes their formation unlikely. The purpose of the ZnSe buffer layer is to take advantage of its lattice and thermal matching to GaAs, combined with its insulating properties - an important issue for GaAs on Si. The linear coefficient of thermal expansion for ZnSe is $7x10^{-6}°C^{-1}$ compared to 5.8 for GaAs and 2.3 for Si. The thermal strain was found to be largely confined to the ZnSe buffer layer, resulting in an order of magnitude reduction in the GaAs.

3.3.4 Selective Growth

Disregarding the benefits to GaAs on Si growth, the motivations for developing selective growth are still strong. For instance there is the extra flexibility it provides for optoelectronic chip design, allowing different types of devices to be fabricated on the same wafer. Such an approach could combine lasers, modulators, and high speed electronic devices all in the same integrated structure. In fact much work has been done in this area using GaAs substrates. To these advantages one can further add the possible reduction in strain of GaAs on Si epitaxy. By growing GaAs selectively on Si one would hope to meet the requirements of both improved material quality, and novel optoelectronic chip design. The methods used to provide selective GaAs on Si fall into two categories, those in which a patterned substrate is used and selective epitaxy occurs, and those in which some form of post growth patterning occurs.

3.3.4.1 Patterned Substrates

By using a combination of masking and etching techniques the silicon substrate is patterned so that GaAs epitaxial growth only occurs on spatially separated areas. This may be done by growing over a masked area (e.g. Si_3N_4) which has had windows opened in it [Chand *et al*], or by etching islands into the Si substrate [De Boeck (1)*et al*, Hashimoto (89) *et al*] followed by epitaxial deposition. In the latter case it was found that the GaAs grows only on the {100} planes and not the {111} sidewalls. Further possibilities for masked growth are studied in [Azoulay and Dugrand] for an MOCVD system using TMGa, AsH_3 and $AsCl_3$. No growth was found on Si_3N_4 or W masks, a fact attributed to HCl adsorption blocking GaAs

deposition. Another approach is the etching of wells into the Si surface [Liang *et al*, Kao *et al*, Charasse *et al*]for which the motivation is planarized monolithic co-integration of GaAs and Si devices. These have been on the whole less successful as regards material quality, the problem being the roughness of the etched well bottom and sides, this in turn promotes dislocation generation and some polycrystalline growth.

A significant advantage of the patterned substrates is in the reduction of wafer bending. For example, a comparison between patterned and unpatterned substrates for a 2.7μm GaAs layer showed wafer warpage to be reduced by half. This despite the patterned Si substrate used being only half the thickness of the unpatterned substrate [Chand *et al*]. On the other hand the GaAs coverage ratio was reduced to 1/6 of the wafer in the case of the unpatterned substrate.

Observation of the variation of strain across individual patterned squares and islands[De Boeck (1)*et al*] has shown that the biaxial strain field normally found is reduced. Moreover, as the stripe width is narrowed the strain becomes non-uniform with a dominant longitudinal component. This was measured by the shift in optical transitions by PL due to strain relaxation. The use of selective area growth has been found to reduce the dislocation density as well as the residual stress [Yamaguchi], with a claim of $<1x10^6cm^{-2}$. The reduction in stress is thought to prevent dislocation generation, a claim that is consistent with results that show most dislocations are generated in the cooling stage of GaAs growth [Tachikawa and Mori] and not in the epitaxy itself. Narrower stripes, with reduced stress, were found to have fewer dislocations.

Most of the work done by other groups has been concerned with relatively thin layers, and therefore have not observed the effect of patterning on microcracking. This is an area we have studied with some very promising results, the details of which are given in the next section. In summary, a large percentage of microcracks were eliminated in layers as thick as 8μm. An alternative approach has been the deposition of small SiO_2 wedge shape islands on the Si surface [Ackaert *et al*] which were found to induce cracks at specific dislocations. Although the total number of cracks was not reduced the ability to control their position could be very useful for the fabrication of devices on Si.

3.3.4.2 Post Growth Patterning

A simpler alternative for producing selective GaAs on Si is to use conventional growth followed by patterning of the as-grown wafer. This is achieved by etching of the epitaxial layer into islands similar to the mesa structures used for the devices discussed in Chapters 4 and 5. The resulting reduction in stress is reported to be comparable to that achieved by substrate patterning. In [Van der Ziel *et al*] as-grown stress was measured at 2.65kbar, but this was reduced to 0.5kbar for a 9 x 12 μm^2 island. Again the strain was found to be largely uniaxial in narrow stripes [Lee *et al*], with strain relief normal to the stripe direction. These changes are detected by low temperature photoluminescence in which the excitonic *hh* and *lh* splitting as well as the band gap change with strain. In particular, the ratio of splitting to the average shift varies according to the type of strain, so that for uniform biaxial it measured 0.757, and for uniaxial strain 1.3. More generally, as the strain increases the band gap is reduced but the splitting becomes greater.

Despite these improvements the major drawback to post-growth patterning is that the initial layers are grown under highly stressed conditions. One would therefore expect a correspondingly high dislocation density, however, this may be partially alleviated by post-growth annealing [Chand and Chu]. By heating to 850°C for 15 minutes a large proportion of dark line (non-photoluminescent) defects were eliminated. The small islands allow dislocations to migrate laterally out of the crystal, activated by the thermal energy.

A different approach altogether is undercut GaAs/Si (3.202, 3.204). Here GaAs is grown conventionally on Si but a special $Al_{0.7}Ga_{0.3}As$ selective etch layer is incorporated at or close to the GaAs/Si interface. This is then almost completely etched away leaving the device layer supported on stilts. Following thermal annealing the dislocation density is found to be substantially reduced. The reason is that the undercut GaAs is no longer lattice constrained to silicon and so is restored to its bulk condition by dislocation movement and annihilation. Despite these benefits this approach would appear to have significant drawbacks when one considers device design, reliability, uniformity and mass production.

3.3.4.3 M488 Patterned Substrate

We chose to investigate patterned Si substrates, this method being particularly suitable for the realization of novel optoelectronic structures. Unlike the examples described above we grew a device structure, in this instance a 50 period MQW pin diode, the first time this has been attempted. The layers were grown on the Philips MBE system by Dr.K.Woodbridge. The substrate used was boron doped Si(100) misoriented 3° towards [110]. Patterning was done through a 2000Å thick oxide layer using IPA:KOH:H_2O (20:60:190), resulting in an array of islands. These were grouped into sets of four islands with sizes in microns, measured by SEM, of 266x461, 259x207, 195x58 and 154x29. The patterned area covered an area of about 3x3cm in the centre of a 2" wafer allowing growth on both plain and patterned regions simultaneously. The layout of the wafer is shown in Fig 3.11 below. After the etch procedure described in *Section 3.3.2* the substrates were loaded into a separate UHV chamber and thermally cleaned at 850°C for 20 minutes. After transfer into the growth chamber RHEED showed a strong 2x2 reconstruction and growth was initiated with 500Å of GaAs grown at 350°C before the temperature was raised to 580°C for growth of a 6μm GaAs *n* doped buffer layer. Prior to the end of this buffer layer, the substrate temperature was further raised to 630°C for growth of the pin MQW structure. This consisted of a 50 period 95Å/60Å GaAs/$Al_{0.3}Ga_{0.7}As$ intrinsic region clad by *n* and *p* doped $Al_{0.3}Ga_{0.7}As$ on the substrate and air sides respectively. A 100Å *p* doped GaAs contact layer was deposited on the top of the structure and 200Å of the AlGaAs cladding region immediately adjacent to each side of the MQW were undoped to prevent dopant diffusion into the intrinsic region. The Si and Be *n* and *p* doping levels were set from previous calibrations to be about $1x10^{18}cm^{-3}$. The GaAs growth rate was set from RHEED oscillations to be 1μm/hr while the V/III beam flux ratio was set at 20/1. The structural assessment of these layers, like the others, is given in *Section 3.4.*

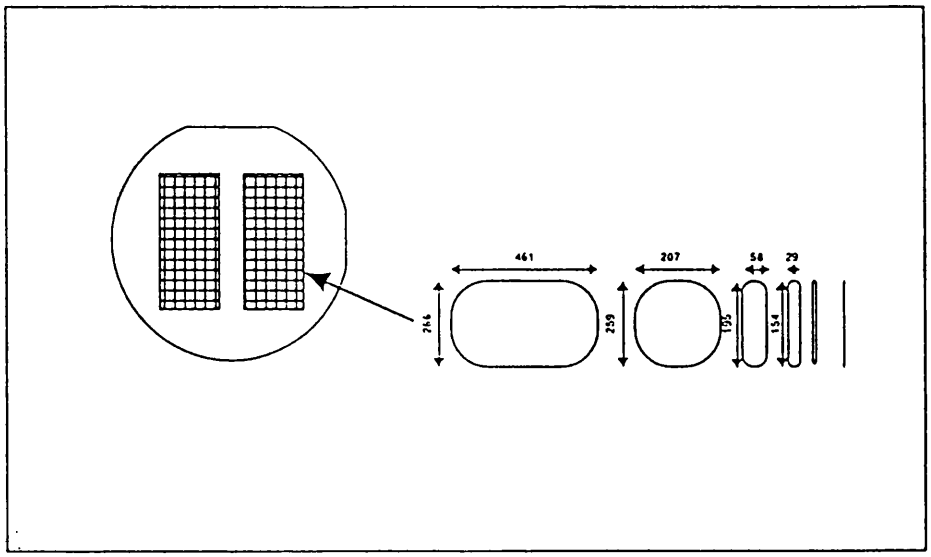


Figure 3.10 *Layout of M488 patterned wafer showing island sizes in μm. These patterns were etched into the silicon substrate prior to growth.*

3.3.5 Alternative Epitaxial Systems

Various alternatives to conventional MBE and MOCVD systems have been used in attempts to improve material quality. One of the most promising has been Migration Enhanced Epitaxy (MEE) also known as Atomic Layer Epitaxy (ALE) [Nozawa and Horikoshi (89), Nozawa and Horikoshi(91)] The basic principle of which is that the Ga and As atoms are supplied separately by means of shutters. The mobility of Ga atoms is found to increase in the absence of As, leading to smoother interfaces and encouraging two dimensional growth. This in itself is thought to reduce microtwins and stacking faults, but the enhanced mobility also allows a reduction in the growth temperature. This in turn reduces thermal stress and associated dislocations. However, there is a compromise to be reached as annealing is often found to improve material quality, presumably through dislocation annihilation and Type II to Type I conversion. Often a two step procedure is used in which nucleation and the initial buffer layer are deposited at ~300°C and then annealed at ~600°C. The remaining layers are then grown at 300°C if MEE is continued or at ~600°C if MBE is used.

The availability of a low temperature growth method has made the elimination of the high temperature oxide desorption step even more desirable. Although this takes place before deposition of the GaAs layers

one would prefer to avoid it so as to allow the possibility of growth on processed Si wafers. One suggestion is to use a hydrogen rather than an oxide terminated surface [Sudersena Rao *et al*], which can be achieved by treatment of the substrate with an HF etch. The hydrogen can easily be desorbed at 400°C. In fact higher temperatures would be undesirable as they are likely to promote surface reactions with any impurities in the growth chamber.

While we have treated MBE and MOCVD as separate systems others have sought to combine the best of both into a single system known as Metal Organic MBE [Watanabe *et al*(89), Watanabe *et al*(90), Ueneta *et al*]. Like MOCVD the Gallium source is provided by TEGa but a solid arsenic source is used in place of arsine. The growth chamber has a background pressure of typically ~10^{-10} Torr to which TEGa is introduced, without a carrier gas, via a group III cell. MOMBE is intended to combine the flexibility of MOCVD chemistry with the control and reproducibility of MBE. Unfortunately some critics have labelled it the worst of both worlds. Certainly an increased carbon impurity problem has been observed by [Watanabe *et al*] from the TEGa despite a high As overpressure. It is possible that the migration of Ga may be enhanced by the gas phase but results at present are inconclusive.

MBE has also been combined with other technologies, such as in Laser Assisted MBE (LAMBE) [Christou *et al*]. Again the intention has been to promote a grid of pure edge type dislocations with a/2 <110> Burgers vectors, rather than the less efficient threading dislocations. A short wavelength excimer laser (308nm) is used to heat the substrate to 850°C in order to clean the surface, particularly from carbon contamination. It is then used to form a sequence of double steps in the silicon surface so as to prevent APDs and enhance two dimensional growth. Finally the laser can be used to thermally anneal the grown layers. In future LAMBE may prove to be a useful tool in selective area epitaxy, with a scanning laser being used to preferentially treat particular parts of the wafer.

Growth has also been attempted by a combination of MBE and LPE [Yasawa *et al*],low energy ion beams [Haynes *et al*], and chemical beam epitaxy [Xing *et al*]. The last is interesting not only for the growth techniques involved, but also for some interesting TEM observations. It was noticed that some areas of the silicon substrate appeared to be covered with amorphous growth, and, more surprisingly, areas of perfect GaAs

crystallinity sometimes occurred above them. These amorphous areas were confirmed as remnants of SiO_2 that had not been fully desorbed. Normally these are considered undesirable and likely to cause dislocations and incoherent growth, indeed that was sometimes the case here. However, the observation of perfectly crystalline areas suggests seed growth occurs at clean silicon, followed by the overlay of SiO_2 by lateral growth. The SiO_2 had thus lifted in some way the lattice matching conditions. This is in agreement with observations made for conformal growth, lateral overgrowth, and epitaxial lift off methods that are summarized in the next section. The possibility that SiO_2 may actually be useful in producing dislocation free GaAs on Si layers is an exciting and significant development.

3.3.6 Novel Growth Techniques

An interesting recent development that confirms the above is conformal growth [Pribat *et al*]. Initially a seed layer of GaAs is grown conventionally on Si followed by a Si_3N_4 capping layer. Most of the GaAs is then etched away leaving the Si_3N_4 layer supported by GaAs pillars on the silicon substrate. The etching process also leaves an ~30Å SiO_2 layer on the silicon surface. Vapour Phase Epitaxy is then begun and GaAs growth is found to seed from the GaAs pillars and extend laterally over the SiO_2 layers. Dislocations in the seed pillars are found not to extend laterally, and new dislocations are not generated as the growth is now essentially lattice matched. In fact TEM has revealed truly dislocation free growth over the SiO_2 layer. No dislocations were apparent in a 0.65μm thick GaAs layer of 200μm^2 area. Furthermore PL was intense from the conformal layer but close to zero above the seed pillars. Although at a very early stage of development, and a somewhat involved procedure at present, there is little doubt that close to dislocation free GaAs on Si has been observed.

A similar idea has been tried by a mix of LPE and MBE [Ujiie and Nishinaga, Sakai *et al*]. The starting point is a GaAs coated Si layer onto which a SiO_2 mask with windows (line seeds) is deposited. Growth was then recommenced using LPE, the GaAs growing laterally over the SiO_2 from the window seeds. Early efforts had limited success but growth has been enhanced by passing a DC current from the substrate to the GaAs

melt, this improves lateral growth by electromigration which helps the transport of species across the wafer.

Finally we shall consider Epitaxial Lift Off and Deposition (ELO) sometimes known as CLEFT [Yablonovitch *et al*, Pollentier et al, de Boeck (2,3) *et al*]. Using this method the device structure is first grown on a GaAs or other lattice matched substrate then, by the inclusion of a selective etch layer, it can be lifted off and deposited on a silicon substrate on which molecular bonding is found to occur upon contact. Thus one avoids the growth problems of lattice and thermal expansion mismatch. Potentially it would even be possible to re-use the GaAs substrate, thereby obtaining perhaps the first recyclable epitaxy! Examination of the GaAs/Si interface by TEM reveals an amorphous layer, very similar to that found in conformal growth, and also believed to consist of oxides [Yablonovitch *et al*]. The microscopic quality of such layers is reported to be very high with dislocation densities little higher than on GaAs substrates. However the epitaxial films are very fragile when being transferred and cracking of the layers is commonplace. Fabrication of monolithic integrated devices is also likely to create alignment problems. It may well be that improved handling procedures can solve these problems but a number of alternatives have been suggested. One is growth of the device structure on a Ge substrate which is lattice matched to GaAs. The whole wafer is then inverted and bonded to a Si substrate so that the Ge is now the top layer, this can then be selectively etched off. The handling and alignment problems are therefore eliminated at the expense of a rather wasteful procedure. A second possibility is the growth of GaAs directly on Si but with the incorporation of a selective etch layer. A photoresist clamp holds the device layers in position while the etch layer is removed. Self-aligned redeposition of the device layers follows. The result of this is to eliminate thermal strain from the layers as measured by PL while avoiding the problems of transportation and alignment. Of course the dislocations originally generated in epitaxial growth remain.

While no perfect solution has yet been found to the problems of GaAs on Si epitaxy some of these alternative modes of growth have demonstrated dislocation free GaAs on Si. It is hoped that these demonstrations will provide further impetus for the improvement of more conventional methods of epitaxy, so that a wide variety of structures can benefit from high quality, dislocation free GaAs on Si.

3.4 MATERIAL ANALYSIS

3.4.1 Introduction

Results are presented for the characterization and structural analysis of the GaAs on Si epitaxial layers. The methods primarily used included transverse and scanning electron microscopy; conventional and Nomarski optical microscopy; photoluminescence; and optical beam induced current (OBIC) images. It was felt that comparison of different structures would be easier if the results were presented according to measurement type, and that is what has been done on the whole. An exception is the patterned substrate device M488 which is discussed separately.

3.4.2 Transverse Electron Microscopy

From the photocurrent spectra for device structure CB252 it was apparent that a miscalibration in growth had occurred. An excitonic peak at around 850nm had been expected but instead a wavelength of 807nm was measured. From the TEM image in Fig 3.11 we can see that the GaAs wells are in fact 40Å, and the $Al_{0.3}Ga_{0.7}As$ barriers are 60Å. The image is a highly magnified (x100K) view of the MQW region with the GaAs wells appearing dark and the AlGaAs light. The high quality of the material is evident with very smooth interfaces between wells. A cross-section of the entire epitaxial structure is shown in Fig 3.12. A high dislocation density is evident at the interface, however there is a substantial reduction in the first 2μm of the GaAs buffer. The MQW region is just visible as a slightly darker band between the lighter cladding layers of AlGaAs. A microcrack is visible at the extreme left and appears to run from the GaAs/Si interface through the epilayers. The narrowness of the microcrack is evident and shows why they are often difficult to observe on the surface unless the sample has been etched. The etching process widens the crack causing obvious damage to the device structure. Over a 50μm wide cross section the average dislocation density was estimated as $7.4x10^7cm^{-2}$ at the interface between the GaAs buffer and the lower AlGaAs cladding layer, $4.2x10^7cm^{-2}$ at the AlGaAs/MQW interface and $3.6x10^7cm^{-2}$ at the MQW/AlGaAs interface. Some dislocations are visible in the MQW

region and a close-up of one of these is given in Fig 3.13. The dislocation is seen to distort the lattice causing a variation in the well width which will result in broadening of the excitonic lineshape.

A rough polycrystalline GaAs capping layer can be observed. Initially this was thought possibly to be the cause of the slightly specular surface appearance typical of GaAs/Si wafers. The roughness is somewhat surprising when one considers the smoothness of the MQW layer. TEM of later samples had smooth surfaces, so it is assumed that the roughness observed here is either a result of damage in the preparation or is confined to this particular sample.

Two reflector stacks were studied by TEM to assess their material quality [Fig 3.14]. The slight scattering that was apparent when viewing GaAs on Si wafers was thought perhaps to be a result of the GaAs or $Al_{0.1}Ga_{0.9}As$ layers not terminating growth completely evenly. To investigate this an extra AlAs capping layer was grown on one reflector stack (QT145). This was then etched off immediately after removal of the wafer from the growth chamber. The final layer structure was identical to QT105 and was a 15 period, 723Å AlAs/609Å $Al_{0.1}Ga_{0.9}As$ Bragg stack, *n*-doped with Si($2x10^{18}$). Comparison of the two stacks by TEM revealed both to have perfectly smooth surface layers. This is slightly surprising given that the surface scattering is visible to the naked eye. Without access to higher resolution TEM it is assumed that the scattering must be due to either a slight 'waviness' in the surface layer, or dislocation scattering within the epitaxial layer. A cross section of the complete reflector stack is shown in Fig 3.15 (AB1247). A microcrack is visible on the far right, while some dislocation bending is seen at the buffer/stack interface. The stack appears to act as a dislocation filter, only allowing certain orientations through. The mechanism is assumed to be similar to that obtained using intentionally strained superlattices, the strain field bending the dislocations.

A number of MBE samples previously grown by Philips were analysed by TEM and their dislocation densities measured. That of M200, a reflection modulator containing a 12 period stack, is compared to structures without stacks in Fig 3.16. For the same total distance from the interface the reduction in dislocation density with the reflector stack is clear. The improvement is confirmed by I-V measurements on devices containing stacks given in Chapter 5.

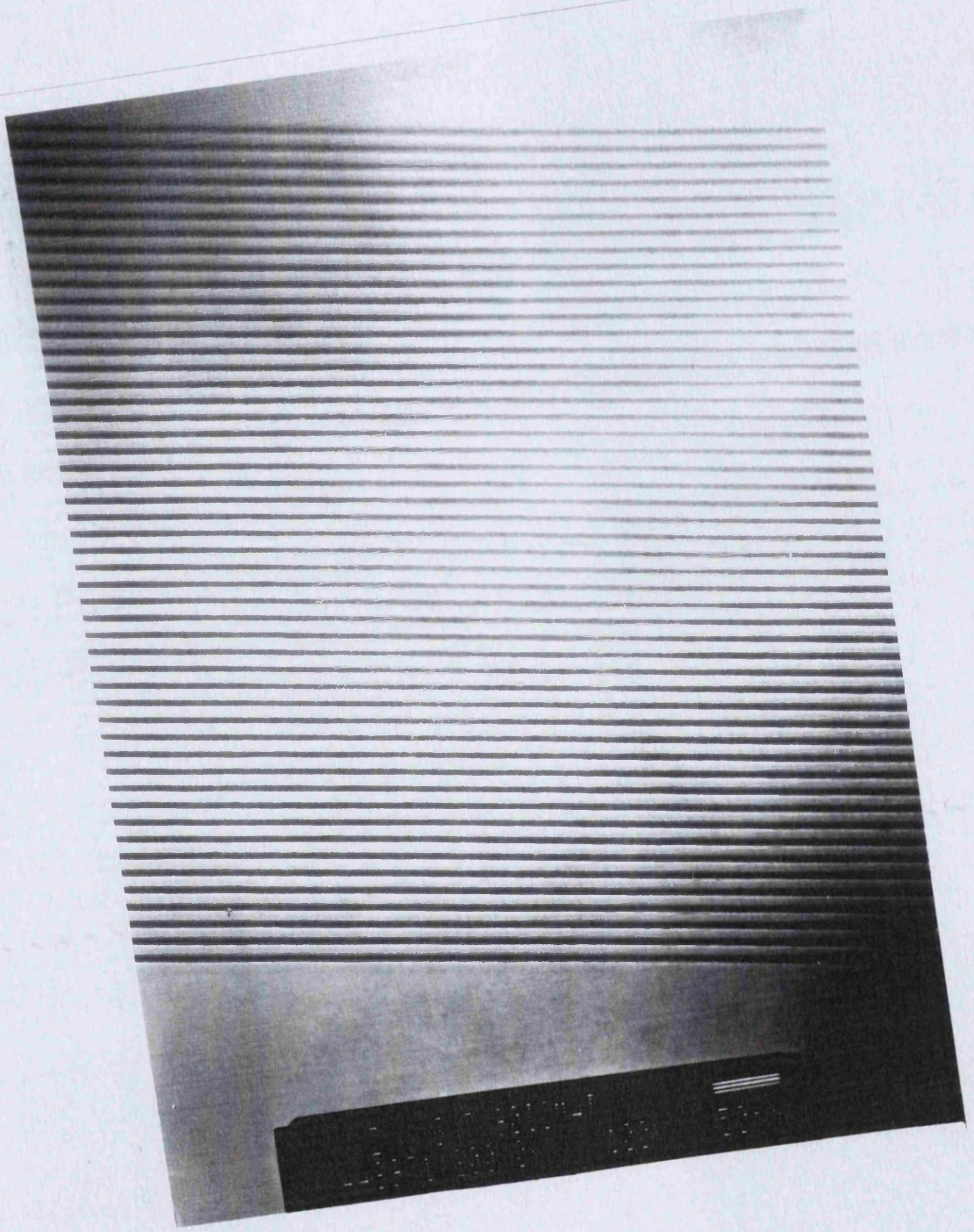
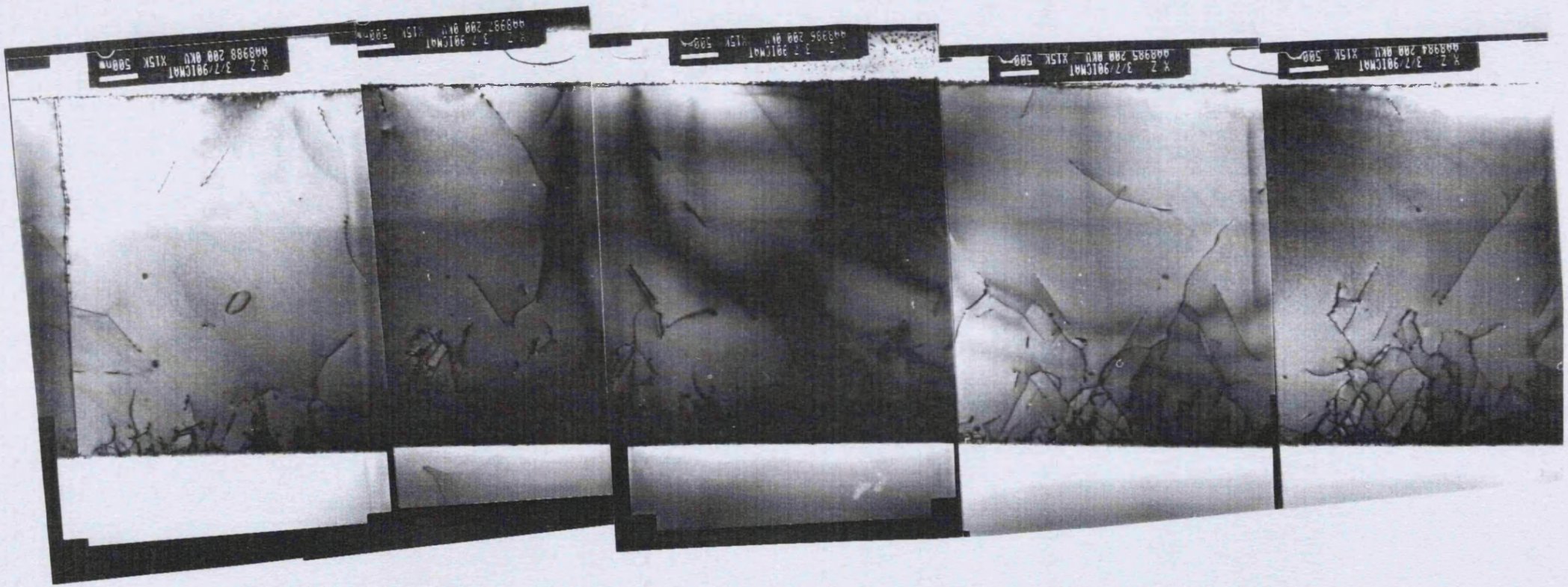


Figure 3.11 TEM of CB252 (8971). The GaAs wells are 40Å, and the $Al_{0.3}Ga_{0.7}As$ barriers are 60Å. The image is a highly magnified (x100K) view of the MQW region with the GaAs wells appearing dark and the AlGaAs light. The high quality of the material is evident with very smooth interfaces between wells.

Figure 3.12 *A TEM cross section of the entire epitaxial structure of wafer CB252. A high dislocation density is evident at the interface, however there is a substantial reduction in the first 2μm of the GaAs buffer. The MQW region is just visible as a slightly darker band between the lighter cladding layers of AlGaAs. A microcrack is visible at the extreme left and appears to run from the GaAs/Si interface through the epilayers.*



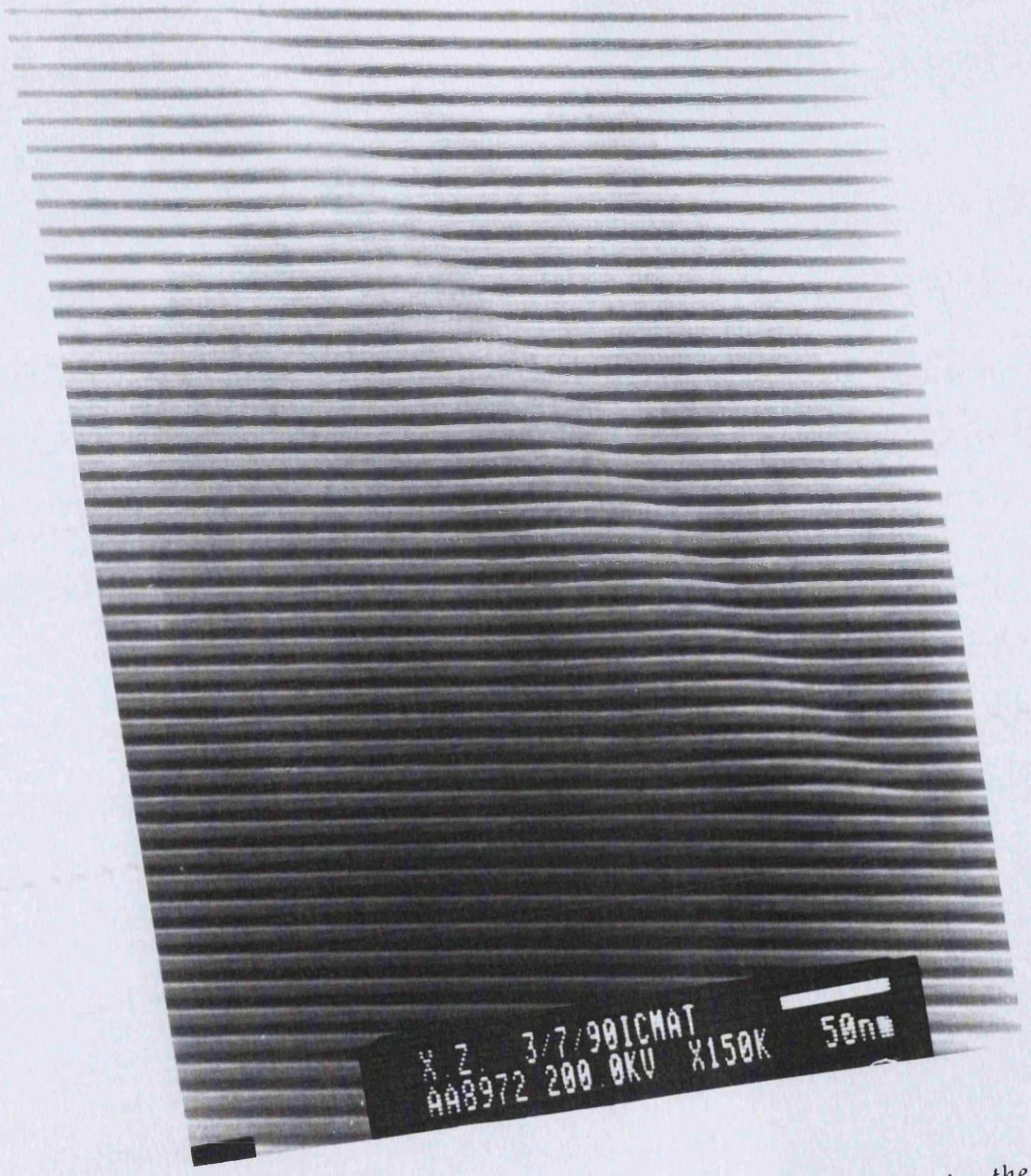


Figure 3.13 TEM of CB252(8972) showing a dislocation in the MQW region. The dislocation is seen to distort the lattice causing a variation in the well width which will result in broadening of the excitonic lineshape.

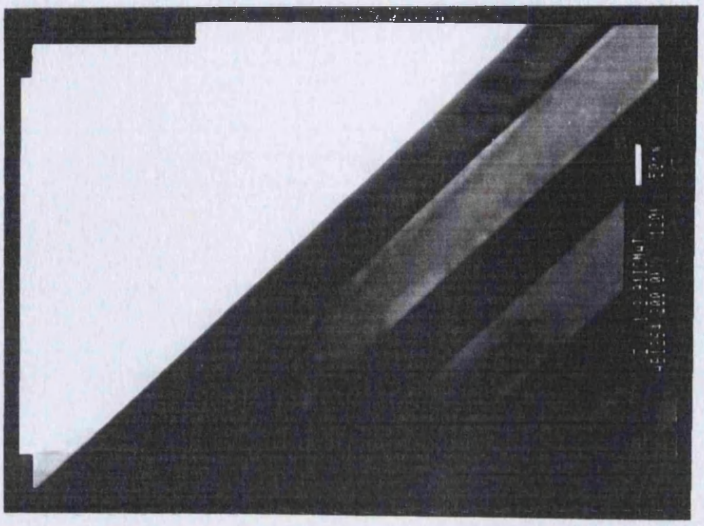


Figure 3.14 *Figure 3.14 (AB1264) shows the surface of a reflector stack grown on silicon (QT105). The layer structure was a 15 period, 723Å AlAs/609Å $Al_{0.1}Ga_{0.9}As$ Bragg stack, n-doped with Si($2x10^{18}$). The perfectly smooth surface layer is slightly surprising given that the surface scattering is visible to the naked eye. Without access to higher resolution TEM it is assumed that the scattering must be due to either a slight 'waviness' in the surface layer, or dislocation scattering within the epitaxial layer.*

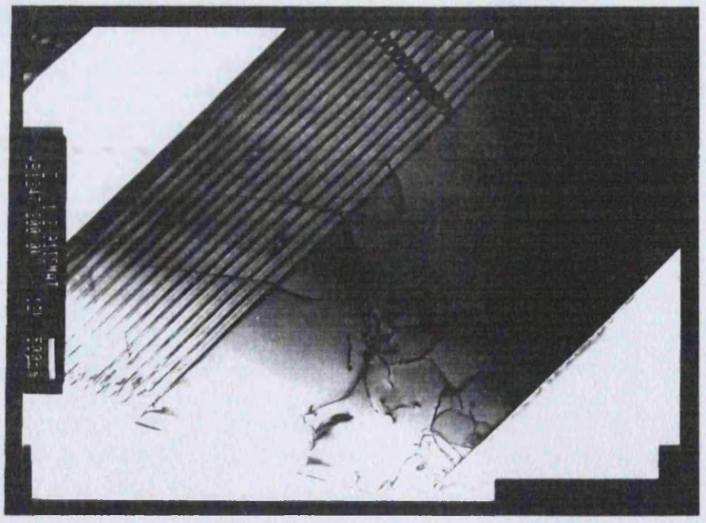


Figure 3.15 *Figure 3.15 (AB 1247) shows a cross section of the complete reflector stack. A microcrack is visible on the far right, while some dislocation bending is seen at the buffer/stack interface. The stack appears to act as a dislocation filter, only allowing certain orientations through. The mechanism is assumed to be similar to that obtained using intentionally strained superlattices, the strain field bending the dislocations.*

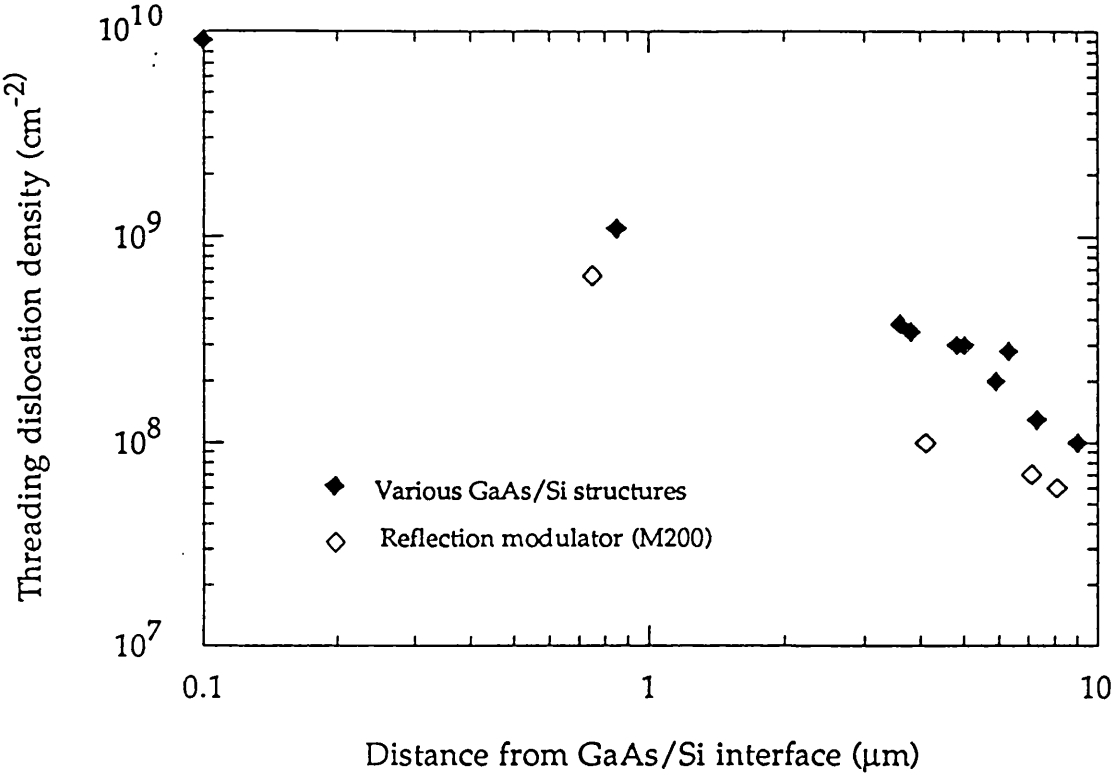


Figure 3.16 *Dislocation density v distance from GaAs/Si interface for a number of MBE grown structures. The M200 modulator structure that utilizes a GaAs/GaAlAs reflector stack has a significantly lower dislocation density.*

3.4.3 Surface Microscopy: SEM and Optical Microscopy

A number of samples were examined using Scanning Electron Microscopy and Nomarski phase contrast microscopy. In addition to the quality of the material within the epitaxial layer the surface characteristics are particularly important for optical devices. This is even more true for the AFPM which relies on reflectivity resonances for its operation. For this reason we were particularly interested in the surface quality of the MBE and MOCVD grown structures and a comparison between the two. The appearance of GaAs on Si wafers is often characterized by a slightly "milky" surface visible to the naked eye, and resulting in a degree of optical microscopy. Figure 3.17 is an electron micrograph showing a number of *pin* modulators fabricated on the CB306 wafer. These have a MQW region containing 50 95Å GaAs wells with 60Å $Ga_{0.7}Al_{0.3}As$ barriers with a total thickness of 3.2μm between the quantum wells and the

GaAs/Si interface. The dark regions are the optical windows of the modulators and are surrounded by a gold contact layer. Microcracks can be seen running along the length of the devices. These have been enlarged by the etching processes required during fabrication. A number of devices and wafers were examined by SEM and a difference in the surface characteristics of MBE and MOCVD grown structures was observed. The MBE wafers appearing to have a coarser surface texture. These differences were, however, more easily visible using Nomarski microscopy and can be observed in Fig 3.18a and b. Given the previous TEM results, in which the surfaces appeared to be extremely smooth, it is unclear whether the surfaces themselves are textured or whether the appearance is due to some other form of scattering.

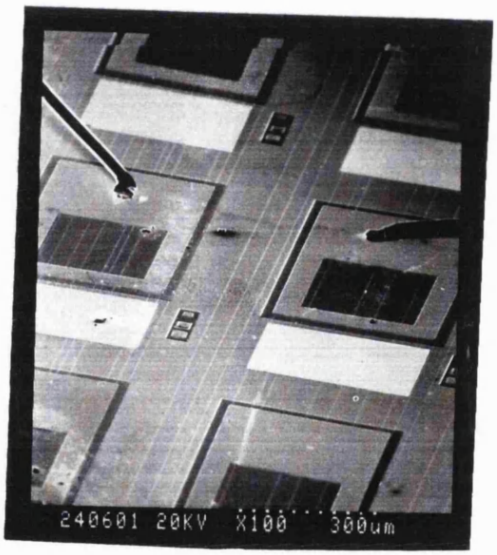


Figure 3.17 *SEM image showing pin modulators fabricated on the CB306 wafer. Each device has a MQW region containing 50 95Å GaAs wells/60Å* $Ga_{0.7}Al_{0.3}As$ *barriers.*

Figure 3.18a shows a Nomarski optical micrograph of the QT105 reflector stack. This structure was grown by MOCVD on a GaAs-coated silicon substrate. A magnification of 256x was used, and the photograph represents an area approximately 250μm x 360μm. An apparent surface texture can be observed and a number of microcracks are visible.

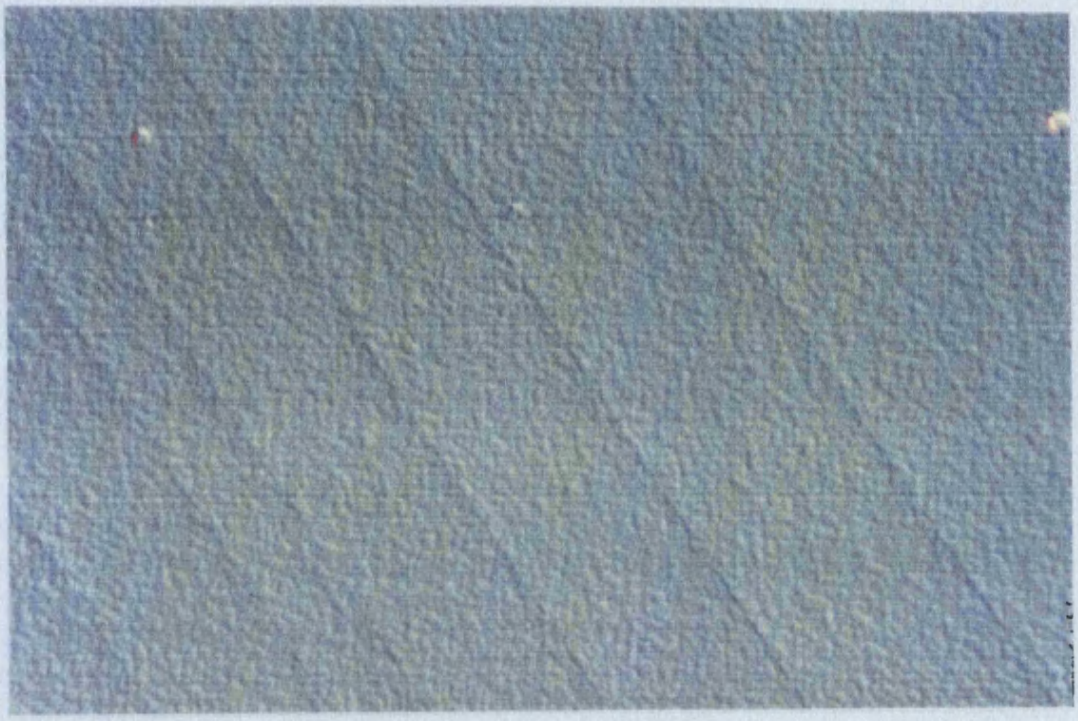


Figure 3.18a *Nomarski optical micrograph of the QT105 reflector stack grown by MOCVD on a GaAs coated silicon substrate. A magnification of 256x was used, and the photograph represents an area approximately 250μm x 360μm.*

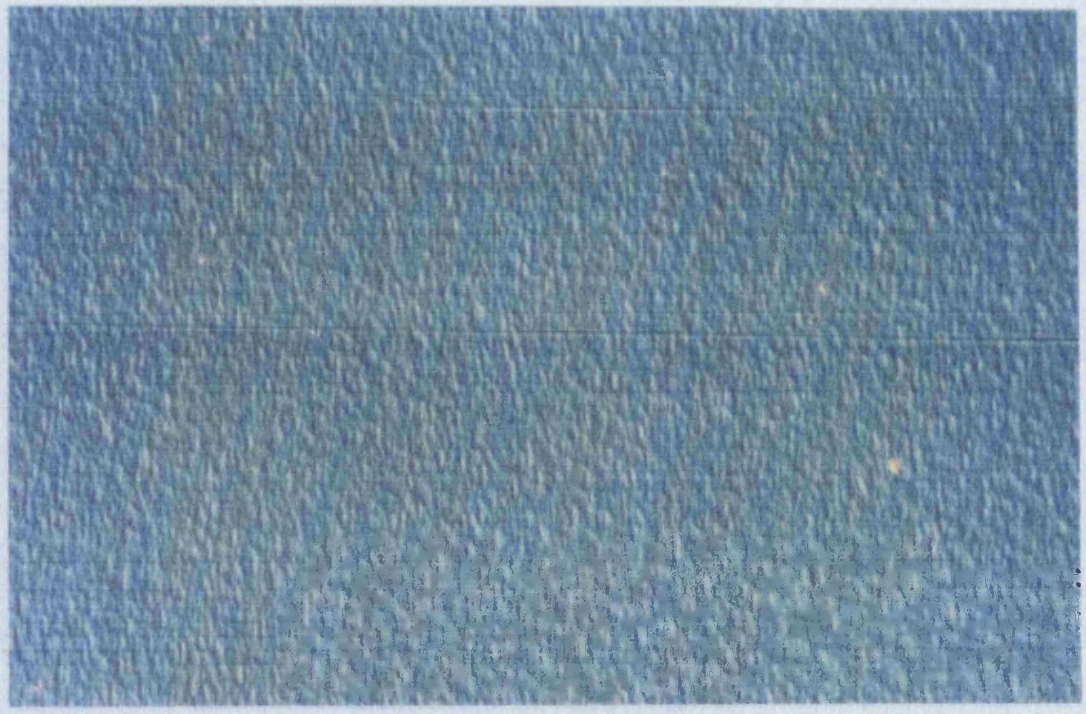


Figure 3.18b *Nomarski optical micrograph of the M199 reflector stack, grown on silicon by MBE. The magnification and surface area are as above. A slightly coarser texture can be observed, and this is believed to be responsible for the lower reflectivity measured on this wafer (Chapter 5).*

The photograph was chosen to show these and does not give an indication of the average microcrack density. Figure 3.18b shows the M199 reflector stack, grown on silicon by MBE. The magnification and surface area are as above. A slightly coarser texture can be observed, and this is believed to be responsible for the lower reflectivity measured on this wafer, see Chapter 5.

3.4.4 Material Analysis of the M488 Patterned Substrates

Growth on a patterned silicon substrate was investigated in order to ascertain whether this would be beneficial in relieving stress and reducing microcracking in the GaAs epitaxial layers. This technique may be especially suitable for direct growth of MQW devices and arrays which are frequently of the same order of size as the features on the substrates. MQW structures were grown on pre-patterned Si substrates with islands of varying sizes, and the structural and optical properties of the epitaxial layers were examined. This is believed to be the first time MQW structures have been demonstrated on Si islands. The growth details and a diagram showing the layout of the patterned wafer were given in *Section 3.3.4.3*.

3.4.4.1 Optical Assessment

Photoluminescence measurements were made at 10K using the 514.5nm line of an Ar^+ laser with the beam focused down to around 50μm diameter. Figure 3.19 shows PL spectra of the four island sizes in one set. Each spectrum shows a lower energy peak originating from the GaAs buffer layer and a higher energy peak assigned to the *e1-hh1* transition from the MQW. PL intensity shows little decrease with island size although there is some broadening which may be related to non-uniform strain. There is a marked blue shift of the QW emission of about 10meV as island size is decreased. This indicates a reduction in tensile strain as island size is reduced. The hh emission from adjacent plain areas away from microcracks was at about the same energy as the largest island so that significant strain relief is only apparent on the smaller islands. If we assume a tensile stress of magnitude X, then the change in energy of the *e1-hh1* transition is given by Eqn 2.20:-

$$\delta E_g^{hh} = [2a(S_{11} + 2S_{12}) - b(S_{11} - S_{12})].X$$

The compliance coefficients are given by [Freundlich *et al*] as S_{11} =1.16x10^{-6}bars^{-1} and S_{12} =-0.37x10^{-6}bars^{-1}. The hydrostatic and shear deformation potentials are a=-9.8eV and b=-2.0eV and are taken from Table 2.1. The observed shift of 10meV then corresponds to a reduction in strain of 1.95kbar. Freundlich reported a strain of 3kbar for unpatterned GaAs on Si at 1.8K, therefore the strain in the smallest islands has been reduced to ≈1kbar. Figure 3.19 also shows an energy shift in both buffer and MQW emission across the wafer on the largest islands. This suggests a growth induced underlying strain variation of about 0.4kbar/mm. This may be due to non-uniform thermal characteristics during growth related to substrate heating or wafer mounting but the relative shift of PL peaks with island is maintained regardless of position on the wafer. A few of these islands had microcracks (indicated) although these did not appear to shift the MQW peak position. These results clearly show that MQW devices can be grown on silicon with much reduced stress.

3.4.4.2 Structural Assessment

After a light peroxide etch, areas of both plain and patterned substrates were examined by SEM and representative images can be seen in Figs 3.19 a to f. Figs 3.19a, c and e show parts of the unpatterned area at three different magnifications. Arrays of microcracks in the <110> directions are apparent with an average density of around 60 per mm and 15 per mm in the two directions. Across the whole of the wafer no clear preference was found for microcracking in either <110> direction. Figs 3.19b, d and e show parts of the patterned area. Surface morphology on the islands is good with some polycrystalline growth at the edge and in the trenches. There is a complete absence of microcracks in either direction. Some areas of the patterned substrate did show an occasional microcrack but average spacing was at least an order of magnitude higher than on the plain areas. A side by side comparison of the unpatterned and patterned areas of the wafer can be observed in Fig 3.19e. In addition it was observed that in some cases microcracks that were present did not propagate across the wafer but were stopped at an island edge. Fig 3.19f is a highly magnified view (7000x) of a

microcrack, note that this will have been enlarged due to the etching process. By comparison an unetched microcrack can be observed in the TEM image of Fig 3.12. Fig 3.19f also shows a slight surface texture, with a similar appearance to the SEM and Nomarski micrographs in the previous section. These results indicate a significant reduction in strain in the patterned areas. It is also believed to be the first time that this has been shown to result in a large reduction in microcrack density. This may have important implications for device integration in the future.

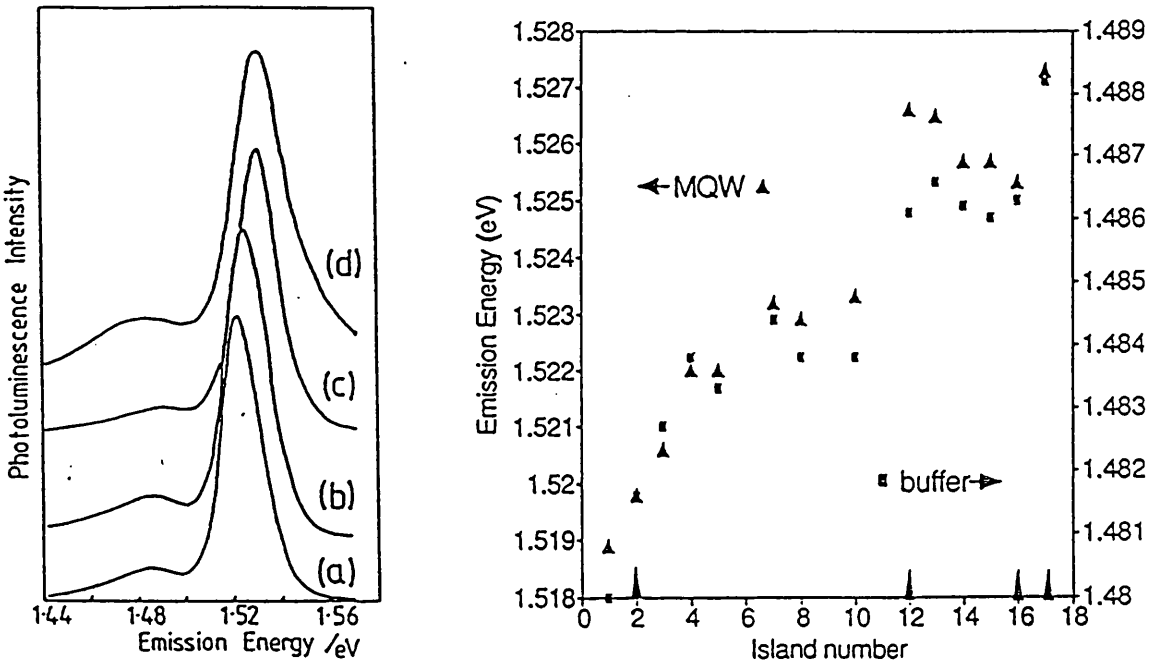


Figure 3.19 *The plot on the left shows PL spectra from different island sizes, (a) 266x461μm, (b) 259x207μm, (c) 195x58μm and (d) 154x29μm. The emission moves to higher energy with decreasing island size because of reduced strain. Etching away the MQW leaves the emission at 1.458eV from the GaAs buffer. The plot on the right shows the variation in emission energy from the 266x461μm island across a 1cm section of the wafer. Arrows indicate islands in which one or more microcracks were present.*

3.4.5 Characterization of GaAs on Si Growth by Scanning Optical Microscopy

A GaAs on Si test structure was grown for characterization by Optical Beam Induced Current (OBIC) imaging using a scanning optical microscope [Wilson] [Wilson *et al*] and [Wilson and McCabe]. OBIC imaging was developed partly because of some of the drawbacks to electron beam induced current (EBIC). One such problem is the need to use very energetic electrons, typically 10-30keV, to allow high resolution and adequate penetration of the semiconductor under test. These can result in damage to the sample and so alter the electrical properties of the device under test. Another problem can be the charging up of the surface of the device, which destroys the image. This occurs for samples that are not fully conducting, for example, they may have a polyimide coating or some other passivating surface layer. Scanning electron microscopes also require operation under vacuum conditions, making them bulky, expensive, and unsuitable for high throughput. The use of a scanning optical microscope and OBIC imaging overcome these problems, while exhibiting a form of super-resolution [Wilson] that in a direct comparison of OBIC and EBIC images allows the former to have essentially identical contrast and resolution. The use of a laser beam rather than an electron beam provides this performance while at the same time ensuring freedom from charging problems, therefore devices coated with silicon dioxide, silicon nitride, or polyimide may all be examined.

In the confocal scanning microscope both a point source and a point detector are used. Similarly, both objective and collector lenses are focused onto the object. Illumination of a device is achieved by relative motion of the object and the optics. The system at the University of Oxford, which was used to test the GaAs on Si devices, moved the object by electro-mechanical vibrators, which were attached to the device platform by taut wires. The detailed design of such a system is critical in order that the device scans accurately in the focal plane. By scanning the device across the focused laser beam two images can be built up. The first is made up from the OBIC contribution from each point on the device. The result is a "map" that indicates the photocurrent generated at each point across the device. This in contrast to the normal photocurrent measurement that effectively gives the sum of all such contributions.

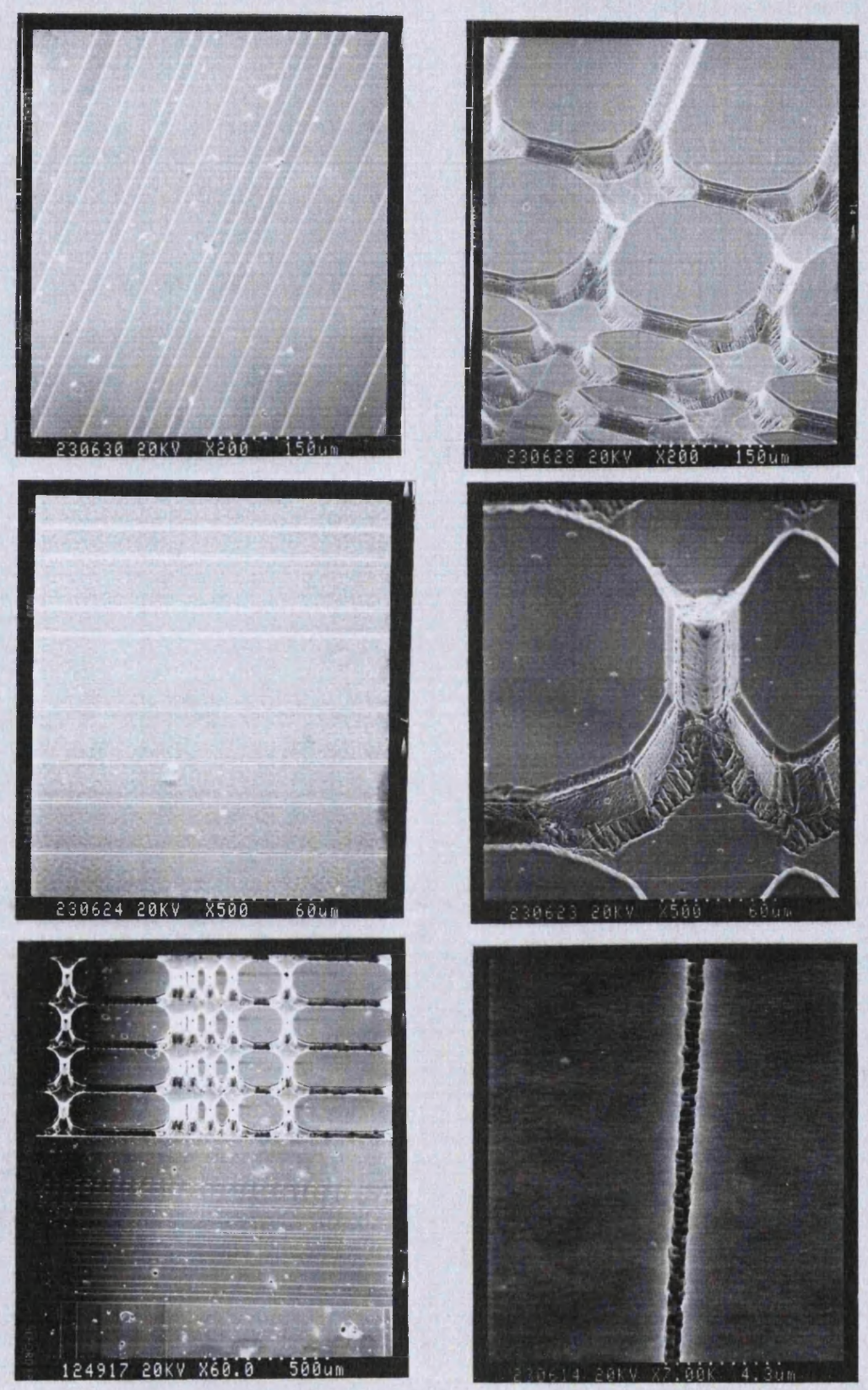


Figure 3.19 *a, b, c, d, e and f SEM images of the M488 patterned substrate wafer. The difference in the microcrack density between the patterned and unpatterned areas of the wafer can be clearly observed.*

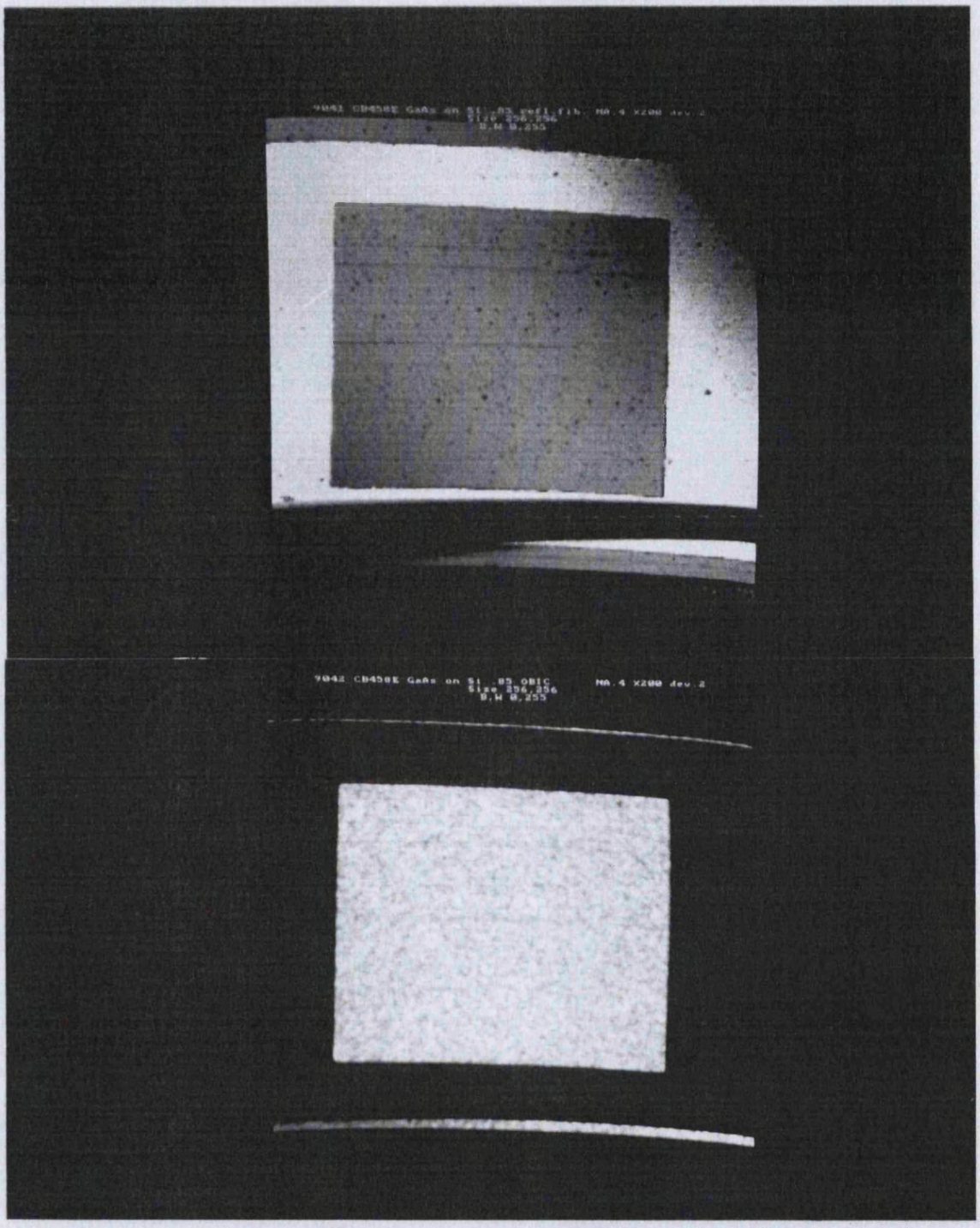


Figure 3.20 ***a and b*** *Figure a, upper, shows a scanning optical microscope image of a GaAs on Si pn junction device mesa. The optical window is 250μm. Bright areas correspond to regions of high reflectivity. A number of microcracks can be seen running from left to right across the image. Figure b, lower, shows the corresponding OBIC image. Bright areas correspond to regions of high photocurrent generation. The microcracks can be seen to have very little effect on the photocurrent performance, but clusters of dislocations , of size 1 to 5μm, create a speckled appearance.*

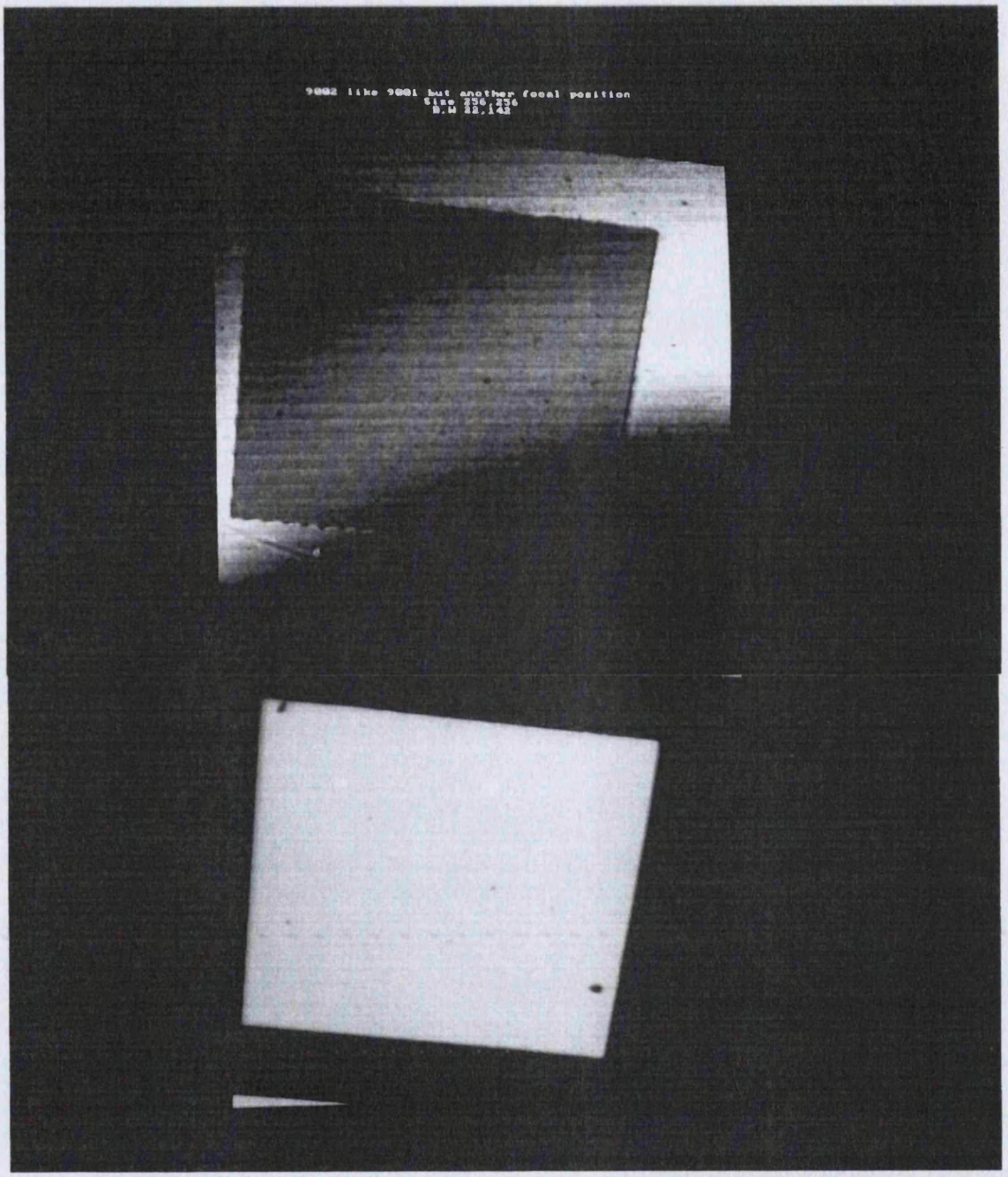


Figure 3.21 ***a and b*** *Figure a, upper, shows a scanning optical microscope image of a GaAs pn junction device mesa grown on a GaAs substrate. The optical window is 250μm. Bright areas correspond to regions of high reflectivity. The horizontal lines are a result of the rastering used in collecting the image. Figure b, lower, shows the corresponding OBIC image. Photocurrent generation is extremely uniform across the device indicating very few dislocations. The bright spots result from photoresist remnants acting as anti-reflection coatings, the dark spots from contamination on the surface.*

Figure 3.22 *a and b Figure a, upper, is a scanning optical microscope image showing a detail of two microcracks running horizontally across the image and a number of surface defects. The device is a GaAs on Si pn junction. Figure b, lower, is the corresponding OBIC image and shows the diagnostic value of this technique. The microcracks have little effect on the photocurrent but a defect running vertically has a dramatic impact on the OBIC image. The size of the image is approximately 20μmx20μm.*

The second image is the reflected optical image of the device. The two images can be compared side by side so that the effect of visible imperfections on the electrical performance can be assessed. Conversely, the OBIC images may reveal defects that are not visible on the surface. For example, dislocations or cracks in the epitaxial layer are likely to result in reduced photocurrent generation at those points. Depending on the choice of laser wavelength and the device structure the properties at different depths or growth thicknesses may be probed. For example an absorbing layer, at the test wavelength, could be grown at various distances from the interface.

A test structure, CB458, was grown by MOCVD specifically for analysis by OBIC imaging. This was a *pn* junction grown on GaAs coated silicon substrate. The device structure was as follows: a 100Å GaAs p^+ capping layer, a 0.5μm GaAs p layer doped at 8-9x10^{17}, a 0.5μm GaAs n layer doped at 3-5x10^{17}, and a 2.7μm GaAs n^+ buffer layer. The buffer layer was part of the GaAs coated silicon substrate (supplied by Kopin). Mesa structures were fabricated with both 100μm and 250μm windows. The devices demonstrated diode characteristics with turn-on and breakdown voltages of 0.9 and -12V respectively. Leakage currents were of the order of 10μA at 10V reverse bias. Monitor devices were grown and fabricated with the same device structure on GaAs substrates, and these had similar electrical characteristics.

The OBIC and optical reflection images for both the GaAs on silicon test structure and the GaAs substrate monitor can be seen in Figs 3.20, 3.21 and 3.22. Figure 3.20a shows the optical reflection image of the GaAs on Si structure. The device window is 250μm wide. The surrounding brighter area is the gold contact layer. A contact wire can be seen running from left to right across the bottom of the image. Within the darker device window can be seen a number of microcracks, again running from left to right of the picture. A slight surface texture can be observed together with a number of small black dots. The former is due to the GaAs on Si growth but the latter are either remnants of photoresist or contaminating particles. Although unwanted these do serve to indicate the level of resolution that can be achieved. The corresponding OBIC image can be observed in Fig 3.20b. The surprising and encouraging thing from this image is the relative lack of effect of the microcracks. They are still just evident, appearing as faint lines across the image, but do not appear to have a dramatic effect on the photocurrent. This corresponds with our

findings for the electrical and optical performance of modulators given in Chapter 4. On the other hand, if the structure had been thicker, increasing the thermal strain and thus the cracking, or if the processing had widened the cracks, then their effect may have been more significant. The OBIC image is characterized by a mottled appearance, however, this does not appear to have any direct relation to that of the surface texture. The image is therefore an indication of the variation in dislocation density across the device. Where dislocations cluster together there is greater non-radiative recombination and the measured photocurrent is reduced, resulting in dark regions on the OBIC image. These regions are typically of length 1-3μm and appear to be distributed randomly across the device. It would thus be possible to reduce the size of the device, or modulator, by approximately two orders of magnitude before the clustering created a significant variation in performance between devices. This would satisfy the constraints on the maximum size of such devices if they were to satisfy the requirements for an optical interconnect discussed in Chapter 1.

Figures 3.21a and b show the equivalent images for the GaAs substrate monitor device. The horizontal lines in Fig 3.21a are a result of the rastering used in collecting the image. Figure 3.21b shows the corresponding OBIC image. Photocurrent generation is extremely uniform across the device indicating very few dislocations as one would expect. The bright spots result from photoresist remnants acting as anti-reflection coatings, the dark spots from contamination on the surface. Figures 3.22a and b show the optical reflected image and the OBIC image at a higher magnification of a number of defects in another GaAs/Si test device. In the optical image of Fig 3.22a two microcracks can be seen running from left to right across the picture. Another line defect can be seen crossing the microcrack, while just above and to the right of this is another apparent surface defect. These defects are not believed to be characteristic of GaAs on Si growth but were particular to this sample; the image was chosen to show the value of the technique and the relative importance of different types of defects. The microcracks can be seen to have little effect on the photocurrent but the defect running vertically has a dramatic impact on the OBIC image. The resolution provided by this technique is evident from the fact that the image represents an area approximately 20μmx20μm in size. Note that the two images have become slightly displaced from each other at this magnification (x2k). The horizontal line in the top half of the OBIC image is due to rastering and is not the microcrack. Again, the

dark spots on the optical image are due to remnants of photoresist or to surface contamination, which appear as bright spots and dark spots respectively on the OBIC image.

The *pn* junction device used here was a very demanding test structure, for the active region was only ≈3μm from the GaAs/Si interface. Despite this we can conclude that the microcracks only had a minor effect on device performance, and that the dislocation density was very even across the device, with clustering only appearing at sizes of 1-3μm. It would therefore be possible to substantially reduce device size before non-uniformity became a problem, thereby satisfying one of the requirements for optoelectronic integration.

Chapter 4

Device Results for GaAs on Silicon MQW *pin* Diode Structures

4.1 INTRODUCTION

Before designing a complete microresonator structure it was first necessary to investigate the properties of the quantum well structures themselves. It was clear from early on that the properties were modified by the GaAs on Si growth process, thus the first task was to characterize and interpret these differences. The results could then be used to model the performance of a complete modulator structure, enabling explanation of any observed changes in performance when compared to structures grown on GaAs.

Growth of devices was carried out both by Molecular Beam Epitaxy (MBE) and Metal-Organic Vapour Phase Epitaxy (MOVPE). The MBE structures were grown at Philips Research Laboratories by Dr. Karl Woodbridge, now of University College London. Due to financial restraints at Philips this machine was scheduled to be decommissioned thus, unfortunately, limiting the duration of the growth programme. It was therefore decided to concentrate on microresonator structures at the expense of *pin* diodes. The MOVPE growth was performed by Dr. John Roberts and Chris Button at the SERC III-V facility at the University of Sheffield. Using MOVPE we were able to proceed with a continuous programme of assessment of the *pin* diodes, and were able to characterize their performance due to changes in device design (e.g. number and width of quantum wells) and growth parameters (e.g. buffer layer, growth conditions).

This chapter concentrates on this characterization and I have indicated which factors are responsible for the observed differences when compared to similar structures grown on GaAs substrates. Detailed explanations of the effects of strain and dislocations are given in Chapter 2 while technical details of the growth, together with structural studies, have been given in Chapter 3. The conclusion makes a value judgement of the device performance and discusses any limitations *vis-a-vis* similar structures grown on GaAs.

4.2 STRUCTURES TESTED

In order to design the full microresonator structure the following issues associated with the *pin* diodes need to be considered:-

i) The excitonic absorption in the MQW.

ii) The Stark shift of this absorption when an electric field is applied.

iii) The I-V characteristics of the *pin* diodes.

The rest of this chapter considers these in detail and presents results and analysis for various structures. This required the testing of a number of different MQW *pin* diodes. MOVPE structures were grown with well widths ranging from 40Å to 95Å under different growth conditions. Two MBE *pin* samples were grown, the first was an early 95Å MQW and is included here mainly to demonstrate the progress made with later devices. The second was grown on a patterned silicon substrate in an attempt to relieve the strain in the epitaxial layer. A summary of the device structures is given in Table 4.1 while a typical test structure is shown below.

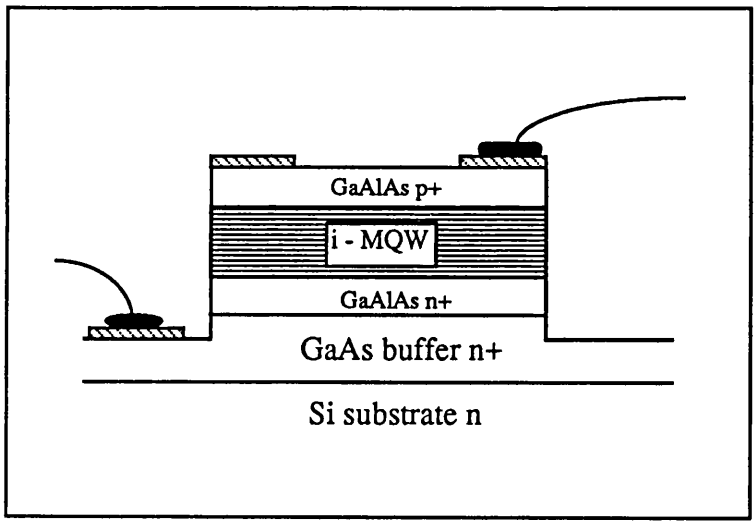


Figure 4.1 *Figure of a typical GaAs on Si MQW test structure. The p and n GaAlAs regions would be about 0.5μm, and the buffer about 3μm. Bond wires provide electrical connection to the p and n layers.*

The thickness of the transparent AlGaAs *p* and *n* regions is fairly arbitrary but they were chosen as above so as to aid comparison with devices previously grown on GaAs substrates. A GaAs *p+* capping layer provides an ohmic contact whilst being thin enough to absorb only a negligible amount (≈1%) of the incoming light. A thin (0.04μm) region is grown between the heavily doped *p*-AlGaAs layer and the MQW in order to prevent any dopants diffusing into the quantum wells. On some samples an equivalent undoped layer was grown to separate the MQW and the *n*-AlGaAs layer.

4.3 FABRICATION

The planar as-grown structures were made into mesa devices, as shown in Fig 4.1, using what are now well documented photolithographic, wet-etching and metallization techniques [Whitehead]. The mesa diodes were fabricated in various sizes ranging from $7.35 \times 10^3 \mu m^2$ to $291.6 \times 10^3 \mu m^2$. The *p* contacts were provided by a thin film of evaporated Cr/Au, while the *n* contacts used Sn/Au. These contacts did not always have low resistances. A problem that was not just confined to devices used in this project, and the variation in quality is the subject of ongoing research. Typically, the chip size taken from each wafer for fabrication would be up to $\approx 40 mm^2$, and, depending on the mask set used, the processed chip would contain from a dozen or so devices to over a hundred.

Layer No.	MQW (well/barr Å)	Periods	Lower Layer	Buffer	Growth
M121	95/60	75	0.5μm GaAlAs	6μm GaAs	MBE
M488	95/60	50	0.5μm GaAlAs	6μm GaAs	MBE(patt sub)
CB252	40/60	50	0.5μm GaAlAs	2.8μm GaAs	MOCVD
CB305	54/60	50	0.5μm GaAlAs	2.8μm GaAs	MOCVD
CB306	95/60	50	0.5μm GaAlAs	2.8μm GaAs	MOCVD
CB504	41/60	50	0.5μm GaAlAs	2.8μm GaAs	MOCVD
CB505	56/60	50	0.5μm GaAlAs	2.8μm GaAs	MOCVD

Table 4.1 *Table of GaAs on Si MQW pin diode test structures.*

4.4 ELECTRICAL ASSESSMENT

Before mounting on a header convenient for use in optical testing the devices were tested on wafer using micropositional electrical probes and an I-V curve tracer. The results here detail only *pin* diode structures, but these are tabulated and compared to modulator structures incorporating reflector stacks in Chapter 5.

In assessing the I-V characteristics we were primarily interested in the reverse bias leakage currents. If these values are too high it becomes more difficult to detect the photocurrent produced by an incident light signal. This is important in the envisaged application of an intra-chip optical interconnect where the modulator has a dual function as a high efficiency detector, for which one would require minimal dark current. Excessive leakage current will also result in increased power consumption and thermal heating of the device, again one would prefer this to be negligible in comparison to the effects of the photocurrent. A value of 10nA was chosen as a preferred upper limit to the reverse bias leakage current and the voltage noted at this value. This was the standard previously used for devices grown on GaAs substrates and so allowed easy comparison. Typically the dark current was also measured at 5V and 10V. The former represents a desirable operating voltage, being within CMOS limits, while the latter was considered to be the maximum practical operating voltage. The current in forward bias was also monitored giving an indication of the series resistance. High resistance was most commonly due to variable contact quality or, in the microresonator structures, to the resistance of the reflector stack. This resistance is troublesome in a number of ways. Firstly, it reduces the measured dark current to a value it would not otherwise be; secondly, if a large photocurrent passes through it the subsequent voltage drop will lower the bias applied to the MQW; and thirdly, the ultimate speed of the device will be limited due to the RC time constant.

Transfer of the devices, from the wafer to the headers used for optical measurements, can sometimes be difficult, resulting in damage to the devices. This is particularly true for GaAs on Si wafers, in which the silicon is both significantly stronger than the GaAs and has a different preferred cleavage plane. Despite this it was found that by first thinning the silicon substrate, and then cutting the wafer with a low damage

inducing diamond saw, devices could be transferred without any observed degradation in performance, although the yield in this process is low. Ideally one would prefer to cut the wafers from the stronger, silicon (back) surface but this presents one with the problem of how to view the devices. If one wished to fabricate large numbers of devices this would be a small problem to solve as some system of alignment could be devised, but in our case the required number of devices was comparatively small and this would have introduced unnecessary complication.

4.4.1 MBE Grown Structures

4.4.1.1 M121: a 75 period 95Å well MQW diode

The earliest device was M121, a 75 period 95Å MQW similar to the test structure shown in Fig 4.1 but incorporating a 6μm buffer layer between the *n*-AlGaAs layer and the Si substrate. Initially two mesa sizes were fabricated having optical windows of 400x400μm and 800x800μm, with mesa areas of 0.36mm^2 and 1.17mm^2 respectively. Leakage currents were found to be in the mA range for only 3-4V applied reverse bias with very soft diode characteristics. These large areas were thus not usable and a switch was made to an alternative mask set using a range of smaller mesa sizes. The results are shown in Table 4.2 and as expected the smaller areas show reduced leakage currents. This is primarily a result of the reduced number of dislocations within the devices, assuming the dislocation density per unit area is relatively constant across the wafer. In fact some smaller devices showed a greater reduction in leakage current than would be associated with simple scaling with area. This is partly due to a variation in quality across the chip, suggesting an uneven dislocation distribution, but may also be in part due to post growth stress relief with dislocations moving to the edge of the mesas, the edge:area ratio of which is proportionately greater for the smaller devices.

With a 6μm buffer layer there is, unsurprisingly, a high density of microcracks. However, where these run parallel to the devices they do not appear to affect the leakage current. This conclusion is based on the fact that there is no discernible relationship between the density of cracks in the devices and their respective performance.

4.4.1.2 M488: A 50 period 95Å well MQW diode grown on patterned and unpatterned substrates

The M488 structure was grown on a patterned silicon substrate with arrays of islands of five different sizes etched into its surface. These island patterns are repeated over the majority of the wafer surface with the outer areas left unpatterned. The island sizes were measured post growth by optical microscopy and SEM and are shown in Fig 3.10.

Fabrication of devices on the patterned substrates was very much a trial procedure involving a number of limitations. For example, the standard mask set was used for device fabrication but this had a different repeat period to that of the islands, therefore only a few of the mesas were aligned with the islands. A second major problem was that the fabrication procedure assumed that one starts with a flat, planar surface. Unfortunately, the steps in the wafer, of up to ≈10μm, were such that the photolithographic masks were unstable and liable to lift off prematurely. This resulted in misalignment between the mesas and the contact metallizations, many of which were missing. Consequently, the yield was lower than one would normally expect. It was initially hoped that devices could be fabricated on all the island sizes, however, the mask set was too large for all but the two largest island sizes. In the event, due to the aforementioned processing problems, only a few devices could be fabricated on the second largest island and most of the devices reported here are from the largest island size. Inspection of the wafers by optical microscopy revealed a very low density of microcracks, in fact most of the smaller islands were crack free with only a few cracks penetrating the largest islands. This is in contrast to the unpatterned part of the wafer which was severely cracked. It was observed that the cracks in the unpatterned part of the wafer ceased to propagate when they reached the patterned area. Discussion of the structural quality and in particular the microcracks has been given in *Section 3.4.4*. Nevertheless, it is worth reiterating at this point that the microcracks do not seem to have any relation to the observed electrical characteristics.

The structure grown on the patterned substrate was a 50 period 95Å MQW with a 6μm buffer region as for M121. Undoped AlGaAs regions of 200Å were incorporated on each side of the MQW to minimize background doping. The *p* and *n* regions were again 0.5μm and a 100Å GaAs *p*+ capping layer was used for contacting. The intrinsic region was

narrower than for M121, so as to increase the built-in electric field such that the greatest number of carriers are swept out. However, this reduces the expected breakdown voltage which is approximately proportional to the intrinsic region thickness. The growth temperature was 630°C except for the deposition of the capping layer which took place at 500°C.

The fabricated devices had optical windows of 20x20μm or 50x50μm with respective mesa areas of $7.35x10^3\mu m^2$ and $21.6x10^3\mu m^2$. The improvement in quality in either case compared to M121 is immediately apparent from Table 4.2.

With the limited data one can not draw any definitive conclusions other than the all round improvement over M121. This applies to devices fabricated on the unpatterned areas as well as those on islands, however it must be remembered that the properties of the whole wafer will be influenced by the large patterned area which will result in reduced strain across the wafer. Overall, these results, taken together with the material analysis in Chapter 3, suggest strong potential for the improvement of device quality by the use of patterned wafers.

Device	Buffer Layer	Area	Voltage	Dark Current	
		($10^3\mu m^2$)	at 10nA	Vr=5V	Vr=10V
M121	6μm	7.35	-	64μA	285μA
		21.6	-	96μA	355μA
M488 patterned	6μm	7.35	12V	2nA	7nA
		21.6	6V	8nA	130nA
unpatterned	6μm	7.35	2.5V	-	-
		21.6	-	-	-
CB252/GaAs	-	21.6	8V	2nA	13nA
		113.4	8V	3nA	16nA
		175	6.5V	4nA	44nA
CB252/Si	2.8μm	175	6V	6nA	50nA
CB305/GaAs	-	7.35	17V	<1nA	1nA
		21.6	17V	3nA	5.5nA
		113.4	13V	4nA	7nA
		175	6V	8nA	14nA
CB305/Si	2.8μm	7.35	18V	1nA	3nA
		21.6	10V	3nA	10nA
		113.4	3V	20nA	170nA
		291.6	6V	14nA	100nA
CB306/GaAs	-	21.6	20V	<1nA	1nA
		113.4	18V	1nA	4nA
		175	6V	7nA	13nA
CB306/Si	2.8μm	21.6	13V	<1nA	3nA
		113.4	9.5V	5nA	11nA
		175	5V	9nA	800nA
		291.6	5V	10nA	70nA
CB504/GaAs	-	113.4	12.5V	1nA	9nA
		175	10.5V	2nA	9nA
CB504/Si	2.8μm	113.4	11.8V	1nA	7nA
		175	9.5V	2nA	13nA
CB505/GaAs	-	113.4	13V	<1nA	2nA
		175	10V	<1nA	10nA
CB505/Si	2.8μm	113.4	10.5V	<1nA	7nA
		175	9.5V	2nA	14nA

Table 4.2 *Leakage currents of device structures.*

4.4.2 MOVPE Grown Structures

For the purpose of assessing their optical properties a number of test structures were grown with well widths ranging from 40Å to 95Å, and it is these that are reported here.

4.4.2.1 CB252: A 50 period 40Å well MQW diode grown on Si and GaAs substrates

This structure was mistakenly grown as a *nip* , rather than a *pin*, diode on an *n* substrate. Due to the thinness of the *p* region the mesa etch penetrated the substrate so that the fabricated device was actually *nipn*. Essentially this is a rather complicated phototransistor structure, with the base region being formed by the 0.5μm *p*+ AlGaAs layer and the adjoining 0.1μm *p*+ GaAs buffer layer. The devices turned on with about 5V forward bias, and breakdown occurred at ≈19V reverse bias for both substrates.

Although not directly comparable to the previously discussed devices due to the double junction within the device the electrical characteristics for CB252 were very promising. The low leakage currents are evident from Table 4.2. Also significant is the similarity between the performance of the modulator grown on Si and its monitor on GaAs.

4.4.2.2 CB305 and CB306: 50 period 54Å well & 95Å well MQW diodes grown on Si and GaAs substrates

These two samples were grown one after the other in the same growth run. CB305 had a nominal well width of 40Å and was intended as a regrowth of CB252, but with the correct *pin* structure on an *n* substrate. In the event, photovoltage spectroscopy and subsequent photocurrent spectra indicated that the well width was in fact 54Å. This was not important as the 54Å MQW made an interesting comparison with the 40Å and 95Å MQW structures, and the intention had been to grow a 60Å MQW for this purpose. Unfortunately, CB305 was found to have a high background doping level in the intrinsic region, resulting in poor electro-absorption characteristics and requiring a regrowth. Both wafers were grown with GaAs substrate monitors *in situ*, however, one has to be careful when

comparing the sample and the monitor as the position in the growth chamber is critical when using MOVPE and can be responsible for some of the observed differences. Furthermore, the ideal growth conditions and temperatures will not necessarily be the same for both devices. The alternative approach to monitoring the material quality *in situ* is to have a separate growth run which is optimized for the GaAs substrate, but then of course one can not be 100% certain that any of the growth parameters (source quality, gas flows, impurity concentrations etc.) are the same. For the growth of these structures the Arsine source was reported to be of high purity (20% AsH_3) and the GaAs nucleation on the GaAs on Si substrate was improved. The temperature was slowly increased to 700°C in a high Arsine ambience, with growth being initiated at a slow rate before being ramped up to the normal value.

Despite the fact that the two wafers were grown one after the other a number of significant differences became apparent. In addition to the higher intrinsic doping level, CB305 also had a higher density of microcracks and, unlike CB306 and previous devices, these had a detrimental effect on device quality. Mesas which contained a high density of microcracks behaved as electrical shorts when tested. The yield for CB305 was low, both for the monitor and the test structure. In fact the yield (≈25%) and the variability of the monitor were little better than for the silicon substrate. Of course, this highlights a weakness in the device processing and fabrication as much as any problems with the epitaxial material quality. Notwithstanding these problems the leakage currents of the working devices are low and forward currents high, suggesting low contact resistances. Particularly notable is the similarity in performance of the devices grown on Si and those grown on GaAs, and that just 10nA leakage current has been obtained at 10V reverse bias for a 50μm window ($21.6x10^3\mu m^2$) device on silicon.

In comparison with CB305, cracking on CB306 was less significant and did not affect device performance, while the yield was also improved. The variability and yield still remained poor both for the control and the test structure, again raising the problem of control in the fabrication process. With an increase in intrinsic region from ≈0.5μm to ≈0.775μm one would expect CB306 to have reduced dark currents and this is indeed the case. Table 4.2 shows that for a 100μm window device ($113.4x103\mu m^2$) 11nA dark current is seen at 10V bias, dropping to 5nA at 5V. Forward currents are again good for the size of device with 3μA at 1V.

4.4.2.3 CB504 and CB505 50 Periods 41Å well/60Å barrier and 56Å well/60Å barrier

The 41Å MQW *pin* diode was effectively a regrowth of CB252, while the 56Å MQW was a regrowth of CB305. In both cases GaAs *n*+ substrate monitors were grown *in situ*. The *p*+ doping was set at $1x10^{18}cm^{-3}$ and the *n*+ at $2x10^{18}cm^{-3}$. The growth control shows improvement in these later wafers, for the quantum well thicknesses, as inferred from photovoltage spectroscopy, are within a monolayer of the design specification. Unfortunately, like device CB305, doping control in the intrinsic region was poor leading to disappointing electroabsorption performance, see *Section 4.5*. The leakage currents were, however, extremely low for all the devices, both those grown on GaAs substrates and those grown on silicon substrates, see Table 4.2. The characteristics of the diodes grown on silicon were virtually identical to the control devices grown on GaAs. Both sets had strong turn-on performance and sharp breakdown voltages. These results were even more encouraging than those previously discussed, for the behaviour of the devices and the control samples were so similar.

4.5 PHOTOCURRENT AND ABSORPTION

4.5.1 Photocurrent Measurement

Photocurrent spectra were recorded for the *pin* diodes using a computer controlled data acquisition system. This is shown in the Fig 4.2 below.

The tungsten halogen source is connected to a high stability, constant current (≈9A) supply. The emitted light is a stable, broadband source which passes through an optical chopper and thence onto the monochromator which has an adjustable grating to control the wavelength of the output light. The output is of narrow bandwidth (≈<1nm) the exact figure being dependent on the width of the input and output slits. The monochromatic light then passes through a variable aperture, used to limit the spot size, and a high pass filter with λc=750nm, chosen to eliminate second order diffraction wavelengths. The diverging beam is collimated and then focused onto the device.

The photocurrent generated in the sample under test will consist of a square wave of the frequency set by the optical chopper, plus any

contributions from stray light and dark current. The signal is amplified and the peak level of the square wave component detected by the lock-in amplifier, which uses the frequency of the optical chopper as a reference. In addition to recording the *dc* output of the lock-in amplifier/detector, the computer controls, by means of an *IEEE* interface, the output wavelength of the monochromator and the bias applied to the device by an *H-P* programmable voltage source.

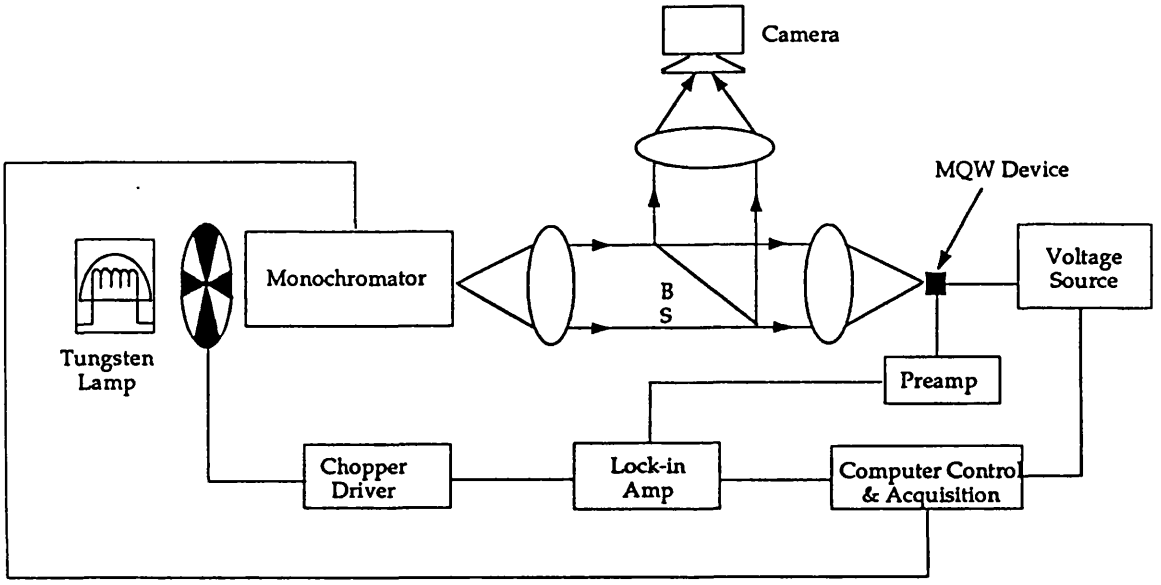


Figure 4.2 *Diagram showing the monochromator set-up used for measuring photocurrent of MQW devices.*

In normal operation the computer software will run a looped series of scans, with the wavelength stepping from say 750nm to 900nm in 1nm steps, for each value of applied bias. The photocurrent is recorded at each point and may be normalized to account for the variation of incident power with wavelength. This is done by first making a calibration curve of the monochromator output using a detector with a known response curve. The optics also include a beam splitter and focusing elements for detection of a reflected signal which is recorded in a similar manner to the photocurrent.

The actual signal input to the lock-in amplifier is the voltage generated across a series resistor by the photocurrent. The value of this can be adjusted depending on the required signal level, but would typically be 100kΩ. For large current levels, e.g. for high incident powers or poor leakage characteristics, an excessively large resistor will result in some of

the applied voltage being dropped across the resistor. For example a 1μA current with a 1MΩ resistor will result in a 1V drop across the resistor, therefore some care has to be taken with the choice of resistor and photocurrent level.

In the case of extremely low signal levels an external current pre-amplifier can be used instead of the resistor and the output fed to the lock-in amplifier.

The photocurrent generated by a MQW *pin* diode is itself an important characteristic of the modulator. Indeed some devices derived from it, such as the Self-Electro-optic Effect Device, use it as the principle of operation. The photocurrent is also of prime consideration when the microresonator devices are used in their complementary function of detector rather than modulator. However, the real power of photocurrent spectroscopy as far as this chapter is concerned resides in the intimate relation of photocurrent and absorption. The photocurrent spectra are seen to be very close to the absorption spectra, and this allows relatively easy study of such interesting phenomena as heavy and light hole excitonic transitions.

4.5.2 *Measurement of Absorption*

For the case of light incident normally on a simple MQW *pin* diode the photocurrent generated is given by :-

$$I_{ph} = P_{in}(1-R_f)(1-e^{-\alpha d})\eta\, e\frac{\lambda}{hc}$$

where P_{in} = the power of the incident beam falling on the device
R_f = reflectivity of front surface
α = the absorption coefficient
d = thickness of the absorbing region
e = electronic charge
λ = wavelength of incident light in air
c = speed of light in air
h = Planck's constant
η = quantum efficiency of device i.e. the percentage of the photogenerated carriers that are actually collected **Eqn 4.1**

This equation can be rewritten as :-

$$\alpha = -\frac{1}{d}\ln\left(1-\frac{I_{pc}}{P_{in}}.\frac{hc}{\lambda\eta e}.\frac{1}{1-R_f}\right)$$

$$\text{or } \alpha \approx -\frac{1}{d}\left(-\frac{I_{pc}}{P_{in}}.\frac{hc}{\lambda\eta e}.\frac{1}{1-R_f}\right) \textit{ to the 1st approximation}$$

$$= I_{pc}.\frac{hc}{dP_{in}\lambda\eta e}.\frac{1}{1-R_f}$$

$$= const.\frac{I_{pc}}{P_{in}} \qquad \textbf{Eqn 4.2}$$

Therefore α is proportional to I_{pc} if the variation of P_{in} with λ is taken into account. This approximation turns out to be a good one as can be seen from the plots of photocurrent and absorption spectra, and in most cases we observe and discuss excitonic features with the use of photocurrent spectra. The reason for this is that although the above relationship between absorption and photocurrent is mathematically simple, accurate measurement of all the variables is considerably more difficult. The first consideration is measurement of the incident power. On the monochromator set-up this is particularly difficult since one has to be certain that all the measured power actually falls within the device window, for this reason a laser system was preferred for more accurate measurements. The set-up was very similar to that of the monochromator except that the light source consisted of a tuneable Ti:Sapphire laser pumped by an Argon ion laser. An extra lock-in amplifier was also required to measure the laser output, since this was far less stable than the tungsten source, with variation over both time and wavelength. The measured photocurrent signal was then normalized to take account of the fluctuating laser power output. A third lock-in was used to measure reflected signals. All three were tied to the same optical chopper reference.

The laser spot size is much smaller than that which can be obtained by focusing the monochromator output. By viewing the device on a CCTV monitor the spot could be observed to be well within the optical window. Due to the higher power levels involved, measurement of the incident power was both easier and more accurate than could be achieved for the monochromator.

In calculating α the remaining difficulties are with η and R_f. If at short λ (away from the band-edge) the photocurrent saturates at a certain

bias voltage, and any increase in voltage does not change the value of the photocurrent, then it was assumed the quantum efficiency η at that point was 1. Whether the photocurrent saturates, and at what voltage, is dependent on material quality and the design of the structure. It was further assumed that the quantum efficiency is independent of λ. The front face reflectivity was also assumed to be independent of wavelength and ≈32% for an air-GaAs interface. In reality there is a small change in value of the refractive index of GaAs [Landolt & Bornstein] but between 800nm and 900nm this results in only a 0.7% change in R_f. This situation is very different to that of the microresonator structure, in which light is reflected after passing through the MQW, thus traversing the absorbing region a large number of times. For the microresonator structure it is not easy to derive the absorption from the measured values of photocurrent.

Normally, accurate measurement of the absorption was made at two or three points using the laser set-up, and the remaining values fitted using Eqns 4.2 and the assumptions discussed above.

In the next two sections a chronological presentation of the structures grown and tested is presented. Some of these were not of high quality but are included both for completeness and to show the progress that has been made.

4.5.3 MBE Structures

4.5.3.1 M121: a 75 period 95Å well / 60Å barrier MQW

This was the first structure grown and was generally of poor material quality. The "raw" photocurrent data is shown in Fig 4.3. With these plots the photocurrent is corrected for changes in the incident power against wavelength, but is otherwise an exact representation of the measured photocurrent.

The order of magnitude increase in photocurrent at 2V applied bias indicates that the quantum efficiency is very low in the unbiased state. The photocurrent does not saturate with applied bias since the leakage currents become very large and the diode breakdowns before this happens. As the

bias is applied measurement of the photocurrent becomes difficult because of the high background signal. One cause of poor quantum efficiency is a high level of unintentional doping in the intrinsic region, this causes a drop off in the field across the MQW reducing the probability of carriers being swept out before recombination. However, MBE growth in general, and the Philips system in particular, maintain a high level of control of the dopants and unintentional doping was not the problem in this case. More important was the material quality in the intrinsic region, where defects and dislocations act as non-radiative recombination centres to trap the carriers before they escape. Increasing the field increases the velocity of the carriers, and so they are more likely to escape before recombination thus increasing the photocurrent.

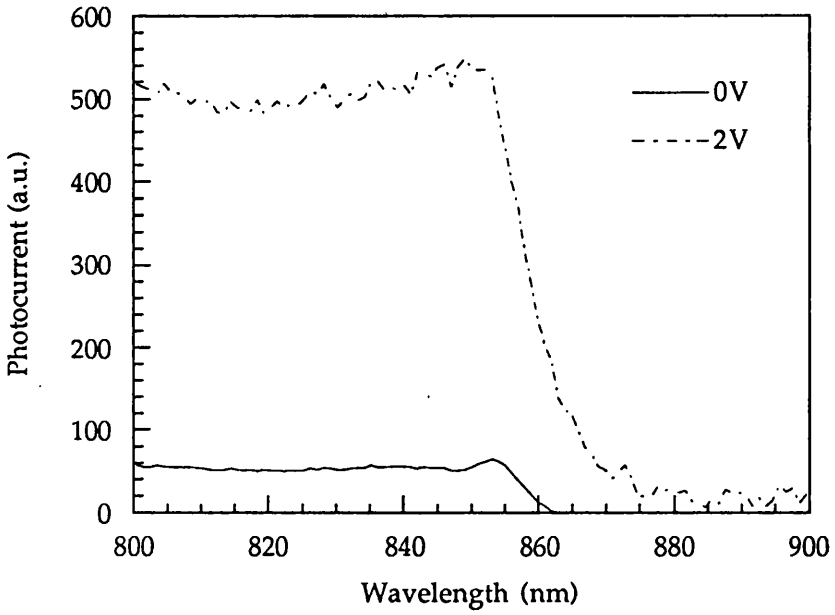


Figure 4.3 *The figure shows the photocurrent spectra for M121, a 95Å MQW that was the first to be grown on silicon. The poor photocurrent characteristics are evident in this early sample. Nevertheless, an excitonic peak can be clearly observed.*

One encouraging feature on the spectra is the clear excitonic peak on the 0V plot, and to a lesser extent on the 2V plot. The presence of a single excitonic peak, rather than the more commonly observed *hh* and *lh* transitions, is the most significant difference between QWs grown on Si and those on GaAs. This was the first manifestation of the strain effects

discussed in Chapter 2, and is an indication of the overlap between the two transitions.

A useful way of displaying the photocurrent spectra is to equate the levels at short wavelength, by means of a multiplicative constant, as shown by Fig 4.4. By doing this we eliminate the effect of changes in η with applied bias, so the spectra reveal more clearly the changes in absorption. We will call these plots *normalized* photocurrent spectra. In this case only a low voltage could be applied due to the poor electrical properties and the exciton peak is seen to broaden rather than shift, nevertheless this was our first demonstration of an electroabsorptive change in MQWs grown on silicon substrates.

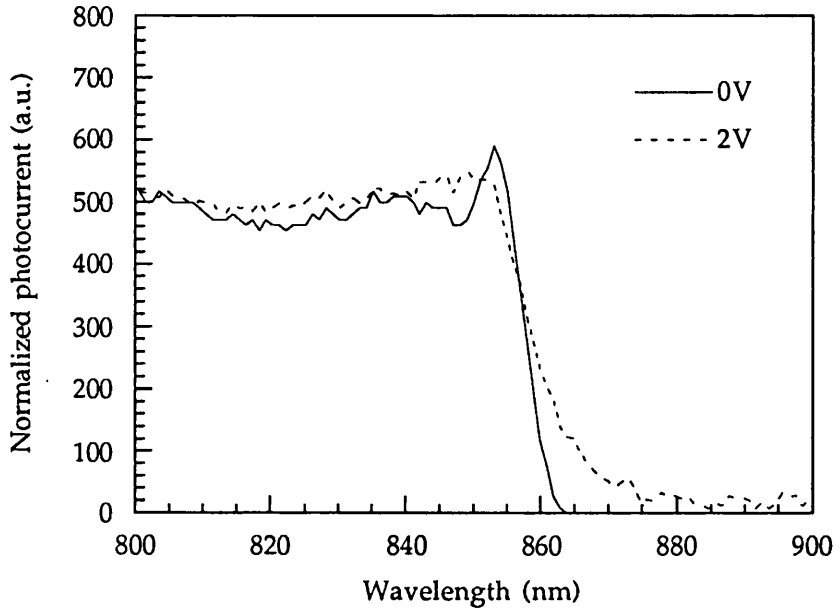


Figure 4.4 *Figure showing the normalized photocurrent spectra for M121 (95Å MQW). Only a small voltage could be applied due to the poor electrical characteristics of the device. The exciton peak is seen to broaden rather than shift, however, this was our first demonstration of an electroabsorptive change in an MQW on silicon.*

4.5.4 MOVPE Structures

4.5.4.1 CB252: a 50 period 40Å well / 60Å barrier MQW

As discussed in *Section 4.4.2* this structure was mistakenly grown as an *nip* structure on a *n* substrate, rather than a *pin*. The *p*+ GaAs contact layer was only 0.1μm and, as a result of over etching, the final device structure was actually *nipn*, both for the test structure and its monitor. This resulted in the unusual spectra seen in Fig 4.5a and b. Noticeable is the negative photocurrent from approximately 810nm to 900nm. This is a result of absorption in the accidental GaAs *p-n* junction, with the photocurrent flowing in the opposite direction to that generated in the MQW. Therefore, for any particular applied bias, there is a point at which the two contributions are equal and cancel out giving zero photocurrent. At shorter wavelengths the MQW absorbs most of the light (≈75%) and so the photocurrent from this region dominates. The steep band edge of the MQW absorption is in contrast to the long tail of the bulk absorption and emphasises one of the advantages of quantum well devices.

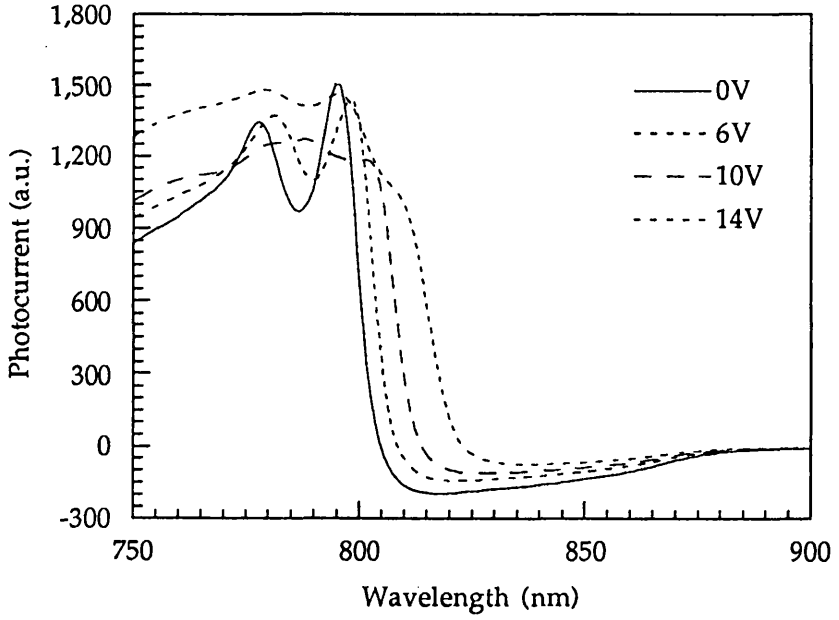


Figure 4.5a *Photocurrent spectra for the CB252 40Å MQW monitor device grown on a GaAs substrate. This was mistakenly fabricated as a nipn device resulting in the negative photocurrent from the bulk GaAs.*

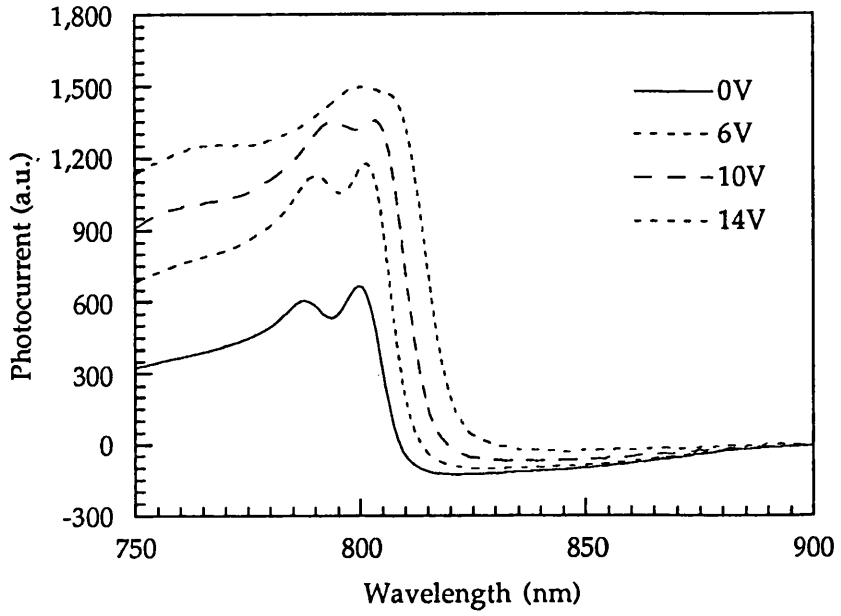


Figure 4.5b *Photocurrent spectra for the CB252 40Å MQW device grown on a silicon substrate. At this well width both the hh and lh excitonic peaks are resolved due to the confinement splitting exceeding the strain splitting.*

A noticeable feature of the photocurrent spectra is that the increased confinement of the 40Å well results in the *hh* and *lh* transitions becoming once more resolvable. For a 95Å well the strain splitting and the confinement splitting cancel each other out, here the latter dominates. By comparison to the monitor the *hh* and *lh* separation is reduced to 6nm from 11nm, the difference being attributable to the strain in the quantum wells. The monitor only experiences a small change in the photocurrent level when a bias of up to 12V is applied, this suggests very good quantum efficiency in the unbiased case. The narrow intrinsic region helps here as the transit time is reduced and the probability of detection increased. A corollary of the thin intrinsic region is the avalanching at 16V or more, at which point the field in the sample reaches 32kV/cm and photogenerated carriers have enough energy to excite other free carriers.

In the test structure the quantum efficiency is also good at 0V bias, but some improvement is seen as a bias is applied, there being about a factor of three change. The difference between the monitor and the test structure is a measure of the material quality of the latter, since the

reduced quantum efficiency at zero bias is a measure of recombination in the MQW due to defects.

4.5.4.2 CB305: a 50 period 54Å well / 60Å barrier MQW

The CB305 on silicon wafer was unusual in exhibiting a greater than normal degree of microcracking. The microcracks appeared to be both more numerous and wider than had been previously observed. The problem was confined to this growth run and is thus not felt to be representative of GaAs on silicon growth in general. Unfortunately, the devices seemed to further deteriorate when transferred from the processed wafer onto headers. This was probably due to the strain applied when cutting the wafer up. For this reason it was not possible to test any samples that had reasonable breakdown voltages. Figure 4.6 therefore shows only the photocurrent at 0V applied bias. The *hh* exciton peak is clearly resolved and has been shifted to shorter wavelength when compared to the 95Å well devices. The *lh* excitonic peak can be observed on the shoulder of the *hh* peak.

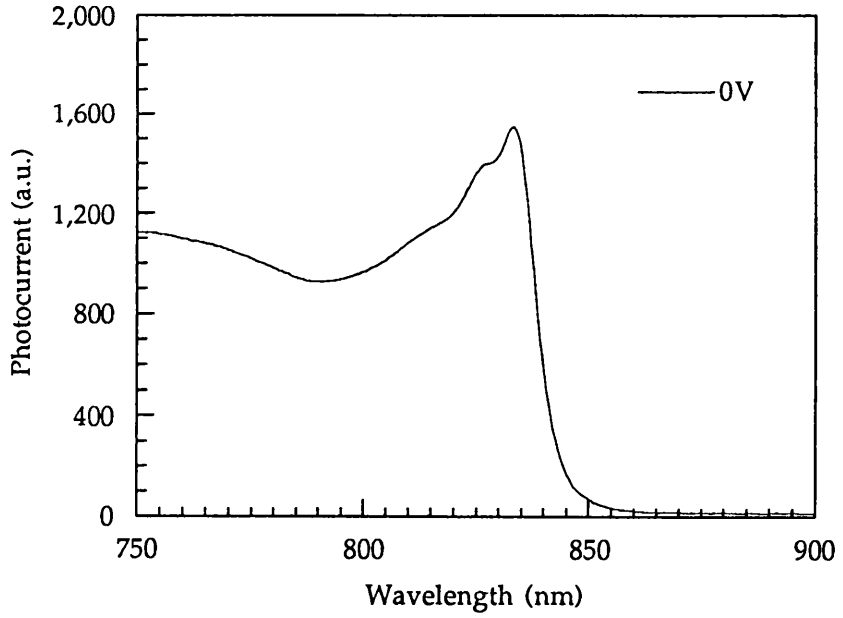


Figure 4.6 *Photocurrent plot for the CB305 54Å MQW diode grown on a Si substrate. The lh excitonic peak can be observed on the shoulder of the hh peak.*

4.5.4.3 CB306: a 50 period 95Å well / 60Å barrier MQW

The unnormalized photocurrent spectra for this sample indicate the high quality of this device, see Fig 4.7a. The saturation of quantum efficiency required only 4V applied bias and resulted in an overall increase of photocurrent of only ≈10%. This compares to the monitor where the increase is 2.5% for a 3V saturation voltage, see Fig 4.7b. The samples had a 50 period 95Å well / 60Å barrier MQW with an additional 0.04μm undoped buffer region, thus making the total intrinsic region thickness 0.815μm. For this thickness and the material quality of this wafer it is apparent that the built-in field is such that efficient carrier sweep-out occurs.

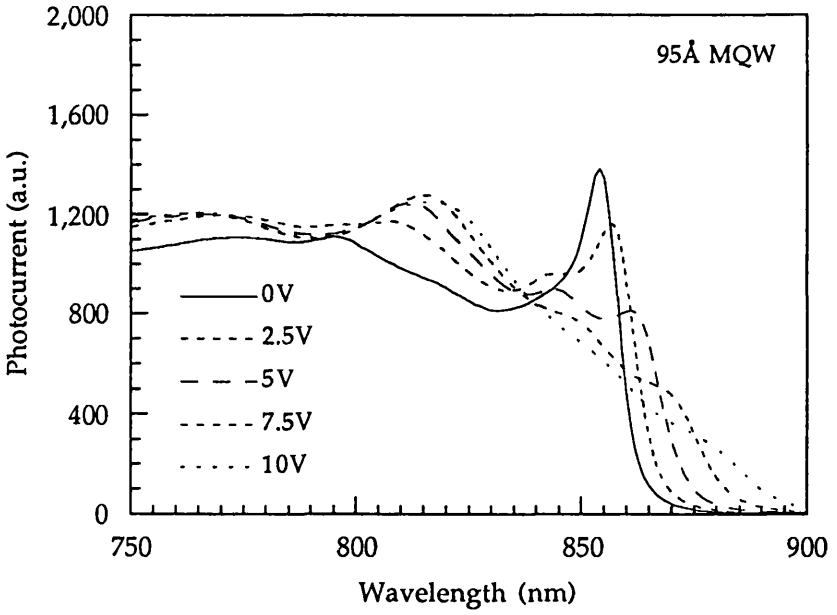


Figure 4.7a *The figure shows the unnormalized photocurrent spectra for CB306, a 95Å MQW grown on a Si substrate. The most noticeable feature is the lack of a resolved light hole, leaving a single excitonic peak. The Stark shifts of the excitonic peak are clear. Also note the small increase in signal level with bias at short wavelength, indicating a high quantum efficiency.*

In most respects the performance of the GaAs/Si *pin* is significantly better than that of the monitor. The exciton peak is stronger and the shifts with field more pronounced. Although grown simultaneously it appears that the monitor's quality is not particularly good, and may have been affected

by either its position in the chamber or the particular growth conditions. The former seems more likely as high quality growth was reported independently at about the time of this device, partly due to a high purity batch of 20% AsH_3. In the case of the monitor the *hh* and *lh* excitons are not as well resolved as for the best quality devices grown on GaAs. The *hh* excitonic peak loses strength rapidly when a field is applied and the QCSE shift is small. Background doping in the intrinsic region will cause this, producing a non-uniform field across the quantum wells.

The clearest difference in the photocurrent spectra is the large single excitonic peak for the device grown on silicon, compared to the usual *hh* and *lh* transitions observed on GaAs. In the former case strain changes the splitting and results in the superposition of the two transitions. Also apparent is the shift in the *hh* excitonic peak from 849nm to 853.5nm, again due to the strain. The accuracy of the growth calibration is confirmed by modelling the unstrained quantum well, this predicts a *hh*-exciton transition at 850nm, and a *lh*-exciton transition at 842nm, where as for our monitor we record 849nm and 843nm respectively.

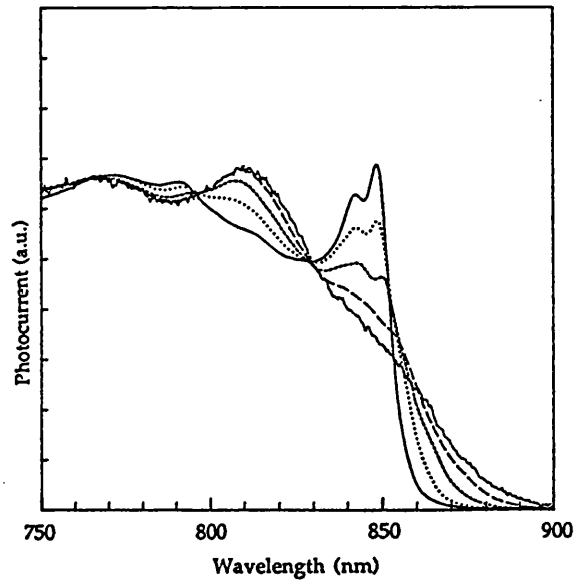


Figure 4.7b *Photocurrent spectra for the CB306 monitor grown on a GaAs substrate. The curves shown are for 0V(solid), 2.5V(dotted), 5V(dashed), 7.5V(long dashes) and 10V(dash-dot). The hh and lh excitons are not as well resolved as is normal for devices grown on GaAs. The hh excitonic peak loses strength rapidly when a field is applied and the QCSE shift is small, indicating a high level of unintentional doping in the intrinsic region.*

Since the monitor was not of particularly high quality, comparison was made with two structures previously grown on GaAs. These had similar structures to CB306 and were found to be of very high quality. The devices used were KLB461 and M33. The former was estimated to have a quantum well thickness of 98Å, while that for M33 was 97Å, these are of course within a monolayer of that of CB306. The *hh* excitonic peak was measured at 853.5nm for M33, while it was almost exactly 850nm for KLB461. Where these structures differed from CB306 was in the thickness of the barriers. These being 111Å for KLB461 and 100Å for M33, with Aluminium concentrations of 40% and 30% respectively.

	KLB461	*M33*	*CB306*
well	98Å	97Å	95Å
barrier	111Å	100Å	60Å
periods	25	20	50
i region	0.622μm	0.984μm	0.815μm
Al%	40	30	30
i doping	$5.5x10^{15}$	$6x10^{14}$	$1x10^{16}$

Table 4.3 *Details of MQW structures grown on GaAs (KLB461 and M33) that were used to compare the performance of CB306, a 95Å MQW grown on silicon.*

Previous studies [Whitehead] have shown that the barrier thickness can be reduced to 60Å without any appreciable coupling, and thus little change in the electroabsorption, the comparison is therefore valid. Although one would ideally like to use an identical sample, such as the monitor, the prime consideration was to compare the performance of CB306 against the best available samples grown on GaAs and this dictated the choice above.

In Fig 4.8 the *hh* excitonic peak shift versus applied field is plotted for all three device structures. The applied field is here simply defined as the applied voltage / intrinsic region thickness. The shift can be seen to be identical for either substrate and is a clear indication of the device quality. Another important aspect of the MQW *pin* diode performance is the rate at which the oscillator strength of the exciton transition is lost when a field is applied across the quantum wells. In Fig 4.9 we plot the absorption at the excitonic peak normalized against its maximum value at 0V for all

three devices. Again the change in CB306 is similar to the best devices on GaAs.

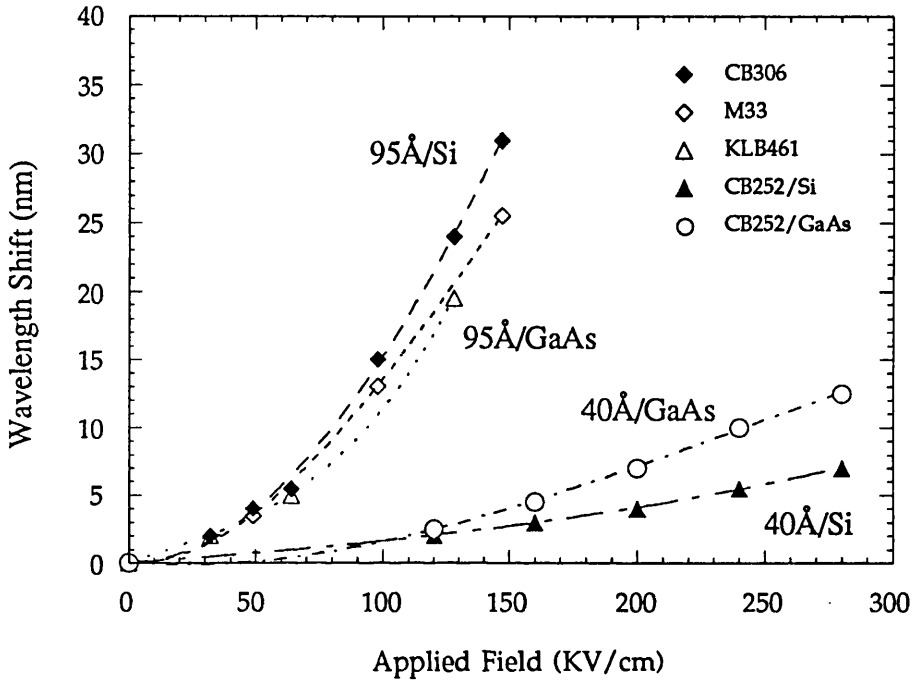


Figure 4.8 *Wavelength shift of the hh excitonic peak versus applied field for MQWs grown on both GaAs and Si substrates. The 95Å wells grown on Si shift as far, if not further, than high quality devices grown on GaAs. The 40Å wells lag behind the GaAs substrate control structures.*

Comparison of the photocurrent spectra for CB306 and its monitor shows a higher value for the excitonic peak relative to the continuum for the device on Si. We were therefore excited to see if the superposition of the *hh* and *lh* transitions had actually resulted in an enhancement of absorption at the excitonic peak. The absorption spectra were derived from the measured photocurrent as described in *Section 4.5.2*. The results are shown below, in Fig 4.10 a and b, where we plot absorption versus wavelength as well as change in absorption versus wavelength.

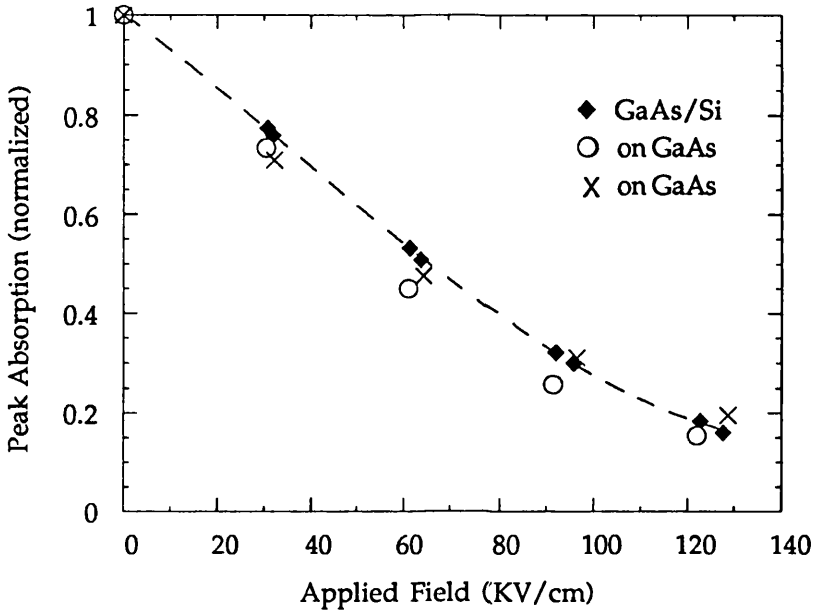


Figure 4.9 *Peak absorption versus applied field for devices grown on Si and GaAs substrates. The loss of oscillator strength is shown to occur at the same rate regardless of the substrate material used.*

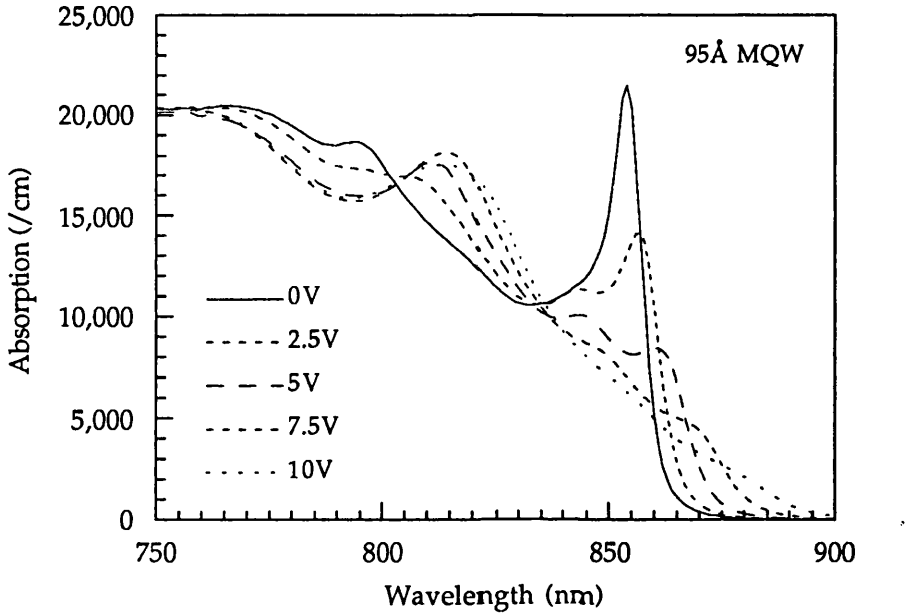


Figure 4.10a *Absorption versus wavelength for CB306, a 95Å MQW grown on a Si substrate. The absorption at the excitonic peak is 21,500cm^{-1}.*

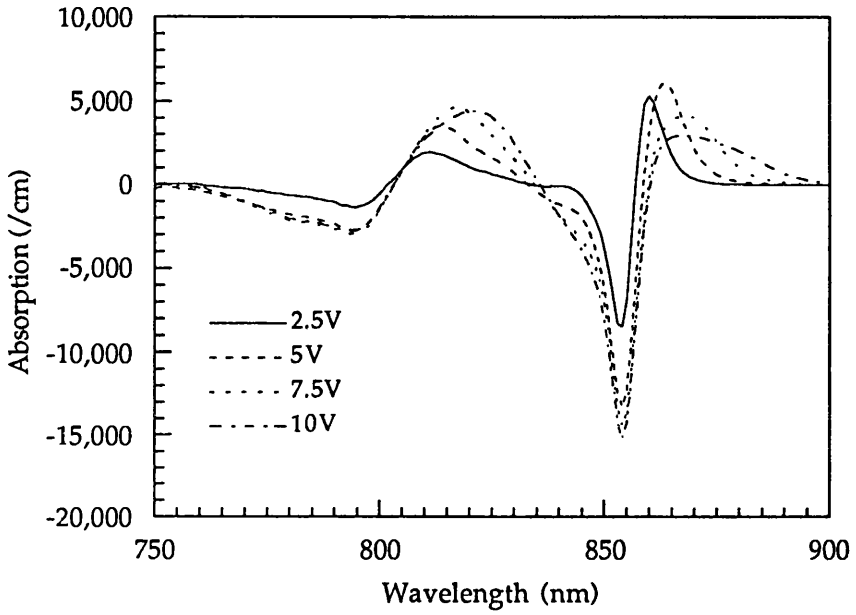


Figure 4.10b *Plot showing the change in absorption versus wavelength for CB306, a 95Å MQW grown on Si.*

Detailed comparisons were made of the absorption spectra of CB306 and its monitor, together with M33 and KLB461 from which we draw the following conclusions.

The peak absorption for CB306 is 21,500cm^{-1}, close to the expected value for a 95Å MQW on GaAs of 22,500^{-1}. It would appear from this fact that we have no enhancement, however, comparison to the monitor shows the structure grown on silicon has an exciton peak ≈10% higher. This would indicate that the monitor has lower than expected peak absorption, a problem that is most likely related to the small degree of broadening seen in the photocurrent spectra. It is impossible to say whether CB306 itself is similarly affected, so one can not tell from this single case whether the higher peak is a direct result of the growth on silicon. KLB461 has a maximum absorption of ≈23,000cm^{-1} in line with the expected value, while M33 shows an exceptionally high maximum of 26,000cm^{-1}, probably due to the very low background doping and small number of wells (20) reducing broadening. Measurement of the FWHM of the exciton peak for CB306 gave a figure of 13.1meV, while that of KLB461 was 9.9meV, and 7.7meV for M33. Although the latter two structures have fewer wells, it would appear that there is a degree of broadening in CB306

when compared to the best samples grown on GaAs. In terms of absorption it seems that the *hh* and *lh* superposition effectively compensates for this broadening. Therefore the peak absorption is not reduced despite the presence of broadening.

4.5.5 Discussion

The purpose of the test structures described in the previous section was to investigate whether the problems associated with GaAs on silicon growth had any effect on the optical properties of the quantum wells, and if so in what manner and to what extent. The specific considerations were:

i) the excitonic absorption in the MQW

ii) the Stark shift of this absorption when an electric field is applied

The most commonly observed change in the absorption spectra of GaAs on Si MQW structures is the disappearance of a resolved light hole to conduction band transition, and a slight shift (~2nm for a 95Å well) of the peak exciton absorption to higher wavelength [Goossen *et al*]. This is generally attributed to residual strain in the wafer causing a splitting in the heavy hole and light hole transitions that is in direct opposition to the splitting created by the confinement of the exciton in the quantum well. The net result is that the *lh* and *hh* transitions coincide, and are no longer resolvable.

This was confirmed by growing MQW structures with well thicknesses of 54Å (CB305) and 40Å (CB252). Decreasing the well thickness to 54Å increases the confinement and, as one would expect, the *lh* and *hh* splitting. The strain splitting does not change greatly (provided growth temperatures are the same for both structures), with the result that the *lh* transition should once more become visible. This is indeed the case as can be seen in Fig 4.6 where the *lh* is clearly visible as a shoulder on the *hh* excitonic peak. Increasing the confinement further, by reducing the well thickness to 40Å, results in completely resolved light and heavy holes, but with a smaller separation than is found when grown unstrained on a GaAs substrate (Fig 4.5a and b). The fact that the light hole moves to longer wavelength indicates that there is a tensile strain in the quantum well

in GaAs, suggesting that any broadening and loss of exciton strength due to the strain is compensated by the *hh* and *lh* overlap.

The Stark shift is seen to be very similar for the 95Å MQW whether grown on Si or GaAs, as is the loss of exciton strength. At a field strength of 150kV/cm the Stark shift on the Si substrate is in fact slightly larger, although with this field the exciton absorption is significantly broadened, making exact measurement difficult. For the 40Å device (CB252) the Stark shift was reduced and at high field strength (250kV/cm) is only about 55% of a control grown on GaAs. It is not clear why this occurred, or indeed, whether it is a reproducible difference.

Chapter 5

Results for Gallium Arsenide on Silicon Reflector Stacks and Modulator Structures

5.1 INTRODUCTION

In the previous chapter we investigated the properties of MQW *pin* diodes grown on silicon and compared them to similar devices grown on GaAs substrates. The results were extremely encouraging and showed that the excitonic absorption and electroabsorptive properties were such that a good modulator could be developed. To complete the integrated AFPM structure one requires a reflector stack, and we start by investigating the properties of such stacks grown on silicon. Growth of the stacks was performed by both MBE and MOCVD, and the results are compared to similar structures grown on GaAs and to modelled spectra.

5.2 DESIGN OF REFLECTOR STACKS

5.2.1 Introduction

The principle exploited in the multilayer reflector stack is an old one, for example see [Born and Wolf]. The stack consists of alternating layers of two dielectric materials with differing refractive indices, the optical thickness of each layer being a quarter wave at the required operating wavelength. The result is a mirror with a high reflectance band at the design wavelength.

With the development of growth systems such as MBE the principle could be applied to high quality, single crystal, semiconductor structures [Van der Ziel *et al*, Gourley *et al*]. The quality and control of the semiconductor growth is such that very high reflectivity mirrors can be achieved, even when the difference in refractive index between the two materials is small. The actual reflectivity attained is dependent on the number of periods in the stack and is given by :-

$$R_{max} = \left[\frac{\left(\frac{n_{inc}}{n_s}\right) - \left(\frac{n_A}{n_B}\right)^{2N}}{\left(\frac{n_{inc}}{n_s}\right) + \left(\frac{n_A}{n_B}\right)^{2N}} \right]^2 \qquad \textbf{Eqn 5.1}$$

where N is the number of periods, n_s=refractive index of the substrate, n_{inc}=refractive index of the medium from which the light is incident, and n_A and n_B are the indices of the alternating refractive index layers. The width of the high reflectance band is given by :-

$$\frac{\Delta\lambda}{\lambda_0} = \frac{4}{\pi}\sin^{-1}\left(\frac{|n_B - n_A|}{n_B + n_A}\right) \qquad \text{Eqn 5.2}$$

From these two equations one can draw the following conclusions. The maximum reflectivity increases with the number of periods and as ΔN between the two materials increases. A large difference between n_{inc} and n_s will also increase the measured reflectivity, for example a stack measured in air will have a higher reflectivity than would occur if the incident material is GaAs. The choice of materials must be such that neither is absorbing at the intended wavelength, this dictates the selection of $Ga_{0.9}Al_{0.1}As$/AlAs reflector stacks in the modulator structures rather than the otherwise more desirable GaAs/AlAs combination. The high reflectance bandwidth $\Delta\lambda$ is only dependent on Δn between the two materials forming the stack. In the case of the AFPM we would prefer as wide a bandwidth as possible in order to reduce the required growth tolerance.

In an actual AFPM the light is incident on the stack from the MQW region rather than from air, however, the test reflector stacks are measured in air. It is thus useful to define an effective refractive index for the stack so that the measured value of reflectivity can be easily converted to the value it will be within the AFPM cavity.

The measured reflectivity in air is R_{air} such that

$$R_{air} = \left(\frac{n_1 - n_{eff}}{n_1 + n_{eff}}\right)^2 \qquad \text{Eqn 5.3}$$

$$\text{then} \quad n_{eff} = \frac{\left(1+\sqrt{R_{air}}\right)n_1}{\left(1-\sqrt{R_{air}}\right)} \qquad \text{Eqn 5.4}$$

$$\text{and} \quad R_{semi} = \left(\frac{n_{semi} - n_{eff}}{n_{semi} - n_{eff}}\right)^2 \qquad \text{Eqn 5.5}$$

Where n_1 = the refractive index of air (1), and n_{semi} = the refractive index of the medium in the AFPM from which light is incident onto the reflector stack. For the typical case of a 12 period reflector stack with n_A=3.54 ($Ga_{0.9}Al_{0.1}As$), n_B=2.98 (AlAs), n_s=3.62 and n_{semi}=3.54, the maximum reflectivity in air would be 98.24%, this is reduced to 93.9% inside the semiconductor cavity. One can also work backwards so that, for example, 95% reflectivity in the cavity requires a measured value of reflectivity of 98.6% in air.

The stacks themselves are relatively insensitive to variations in growth, partly due to the wide high reflectance band. These changes can be easily modelled by considering a matrix representation of a general multilayer structure.

Consider the reflected and transmitted waves for light incident upon a single layer as shown below:-

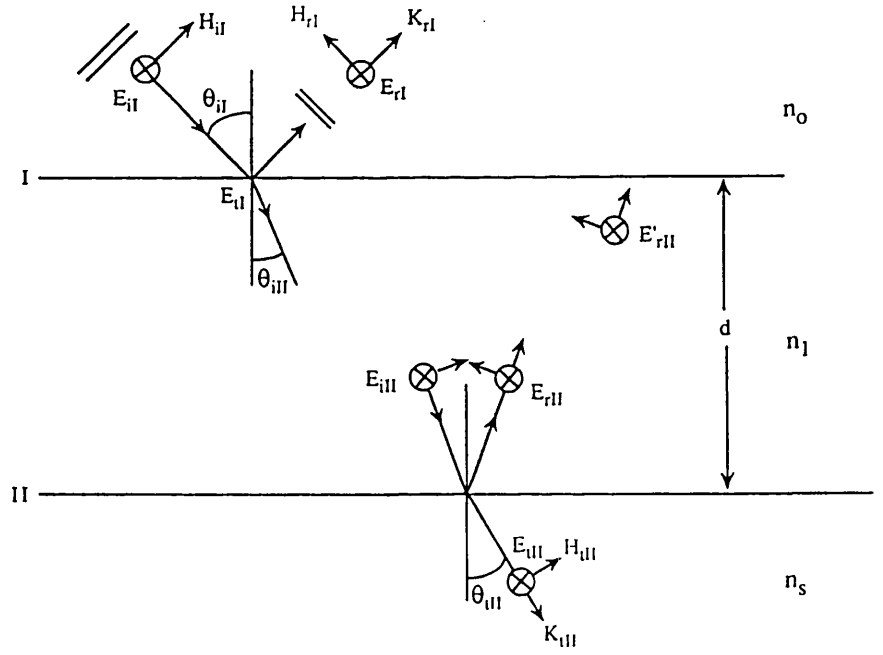


Figure 5.1 *Reflected and transmitted waves for light incident upon a single layer.*

The model assumes the summation of waves, i.e. each wave equation is the summation of all waves in that direction. In this case there are just two defined directions - incident and reflected at each interface. Tangential components of E and H fields must be continuous at the boundaries, so one can equate the incident, transmitted, and reflected waves.

From the above considerations it can be shown that, in matrix notation, the tangential components of the E and H fields at the boundaries are:-

$$\begin{bmatrix} E_I \\ H_I \end{bmatrix} = \begin{bmatrix} \cos(k_0 h - i\gamma x) & \left(i\sin(k_0 h - i\gamma x)\right)/Y_1 \\ Y_1 i\sin(k_0 h - i\gamma x) & \cos(k_0 h - i\gamma x) \end{bmatrix} \begin{bmatrix} E_{II} \\ H_{II} \end{bmatrix} \qquad \textbf{Eqn 5.6}$$

where h = $n_1 d\cos\theta_{iII}$, d = the thickness of the layer, θ_{iII} = angle of wave through medium, and γ = the amplitude absorption coefficient = 0.5α.

Each layer has such a matrix and by multiplying these together so that:-

$$M_t = [M_1 \times M_2 \times \ldots\ldots M_n] \qquad \textbf{Eqn 5.7}$$

$$\text{then} \quad \begin{bmatrix} E_I \\ H_I \end{bmatrix} = M_t \begin{bmatrix} E_{II} \\ H_{II} \end{bmatrix} \qquad \textbf{Eqn 5.8}$$

The reflectivity is given by R = r*conj(r), which for a stack consisting of two alternating media can be calculated from:-

$$r = \frac{\left(Y_0 * M_t(1,1) + Y_0 * Y_s * M_t(1,2) - M_t(2,1) - Y_s * M_t(2,2)\right)}{\left(Y_0 * M_t(1,1) + Y_0 * Y_s * M_t(1,2) + M_t(2,1) + Y_s * M_t(2,2)\right)} \qquad \textbf{Eqn 5.9}$$

$$\begin{aligned} Y_0 &= c_0 * n_0 * \cos(\theta_i) && \text{for the incident medium} \\ Y_1 &= c_0 * n_1 * \cos(\theta_{il}) && \text{for the first medium} \\ Y_2 &= c_0 * n_2 * \cos(\theta_{iII}) && \text{for the second medium} \\ Y_s &= c_0 * n_s * \cos(\theta_t) && \text{for the exit medium} \end{aligned} \qquad \textbf{Eqn 5.10}$$

For any combination of layers we can multiply the appropriate matrices together and thus calculate the resultant reflectivity. The model is also applicable to absorbing media and different incident angles.

In order to simplify the modelling of the reflector stacks a constant refractive index with wavelength is assumed. In fact for $Ga_xAl_{1-x}As$ the refractive index drops slightly as the wavelength increases. This will cause a slight asymmetry in the actual reflection spectra but is of little importance. Figures 5.2 a and b show modelled spectra demonstrating the effect of increasing the number of periods in the reflector stack. The former shows the reflectivity for light incident from air, the latter for an incident medium with refractive index n=3.62 as would be the case for an

AFPM. This results in a reduction in the peak reflectivity for a 12 period stack from ≈98% to 94%, which we will see later to have an adverse effect on the AFPM insertion loss. Measurement of the reflectivity of the test stacks in air actually presents a significant problem, since high reflectivities (>95%) are achieved relatively easily. Distinguishing between reflectivities of 95% to 100% becomes extremely difficult, and yet these differences can become significant once the stack is inserted into the AFPM cavity. Measurement was actually done by reference to a freshly deposited gold film, which has a reflectivity of ≈97% at 850nm.

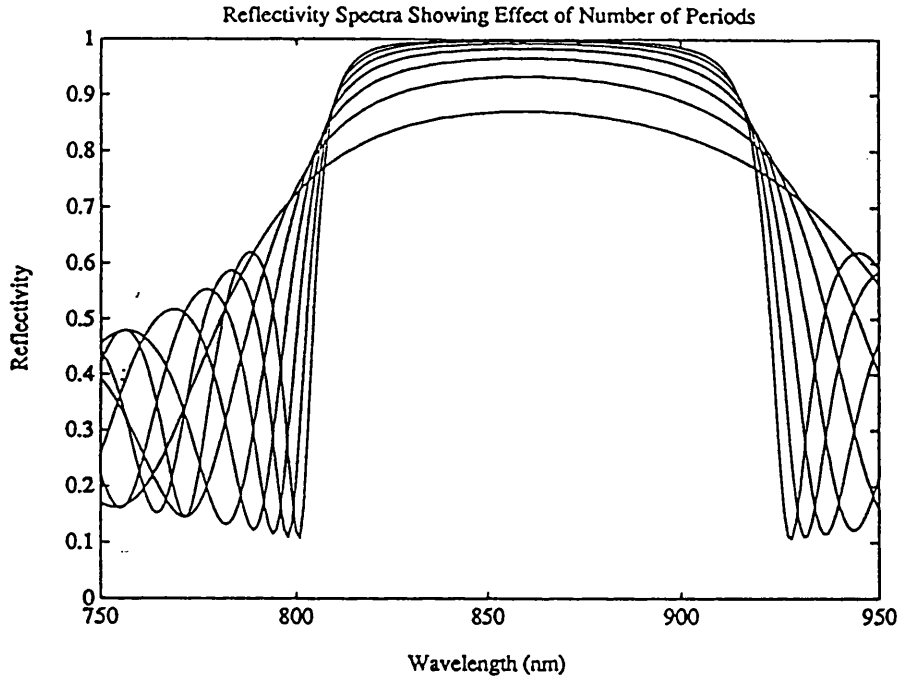


Figure 5.2a *Modelled reflection spectra for reflector stacks in air having 6, 8, 10, 12, 14, 16 and 18 periods of* $AlAs/Ga_{0.9}Al_{0.1}As$. *Increasing the number of periods can be seen to increase the maximum reflectivity.*

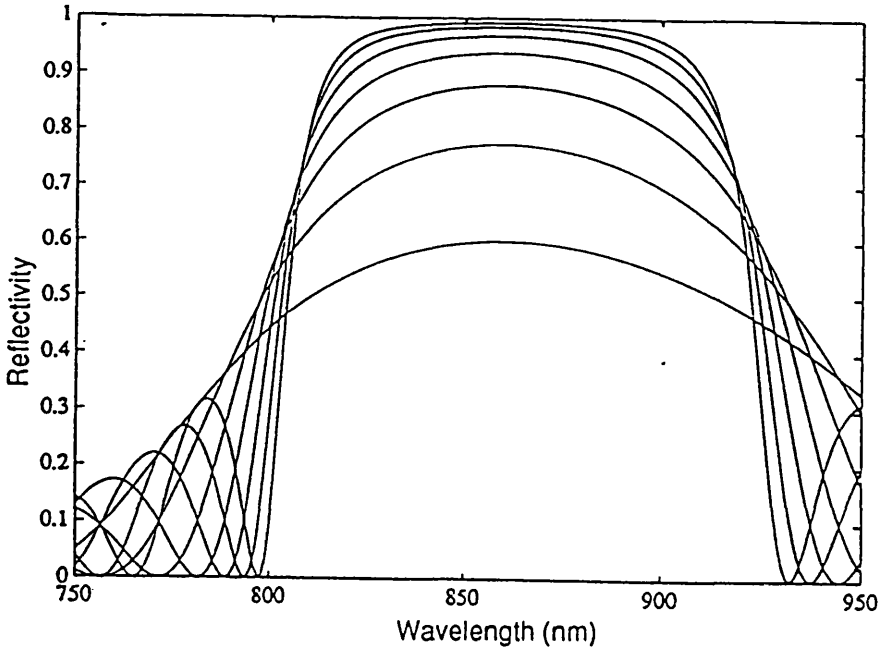


Figure 5.2b *Modelled reflection spectra for reflector stacks embedded in a modulator structure having 6, 8, 10, 12, 14, 16 and 18 periods of $AlAs/Ga_{0.9}Al_{0.1}As$. The reflectivity is reduced due to the small index change between the cavity and the reflector stack.*

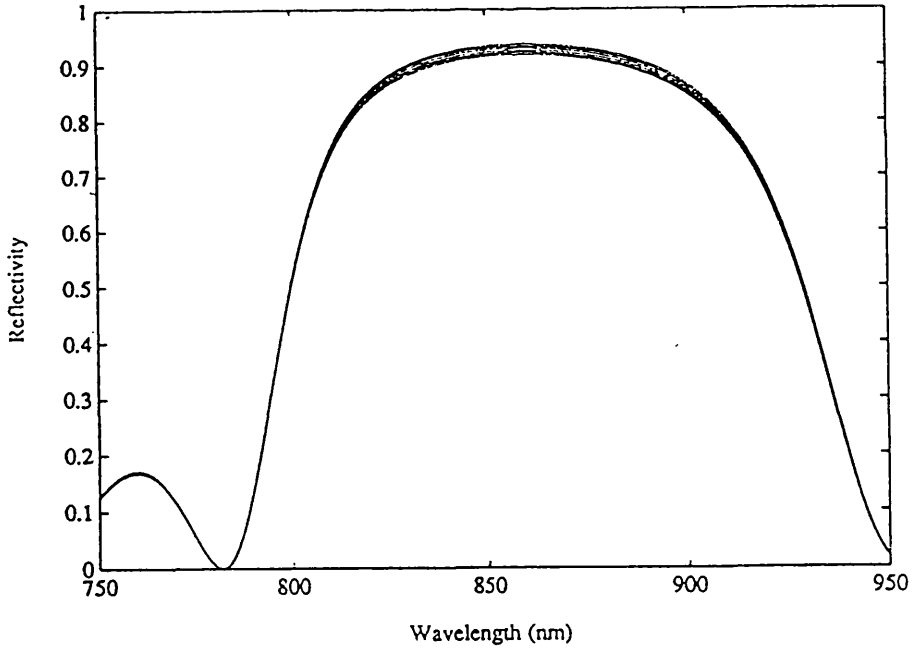


Figure 5.2c *Effect of a small amount of band-tail absorption on the reflectivity of a 12 period stack in a semiconductor cavity, α=0 to 500cm^{-1}*

We previously stated that to achieve the highest reflectivity over the widest bandwidth it was desirable to have Δn between the layers as large as

possible. However, this is constrained by the need to have both layers transparent at the required operating wavelength. Fig 5.2c shows the effect of a small degree of band-tail absorption in the $Ga_{0.9}Al_{0.1}As$ layer of a 12 period reflector stack. The figure plots reflectivity in the cavity against wavelength for absorption coefficients ranging from $\alpha=0$ to $\alpha=500cm^{-1}$. The result is a reduction in the peak reflectivity from 93.79% to 91.86%.

In assessing the operation of AFPMs integrated with silicon one point of consideration will be the sensitivity to input angle. In Figure 5.3a, below, the reflectivity of a 12 period stack is plotted against wavelength as the angle of the incident light is varied from 0 to 89.9%. It can be seen that, although the central wavelength of the high reflectivity band shifts, the overall outcome is a progressive increase in reflectivity towards 100% over the whole wavelength range. The increase is such that at the design wavelength of 860nm the reflectivity is actually enhanced, despite the shift of the high reflectance band.

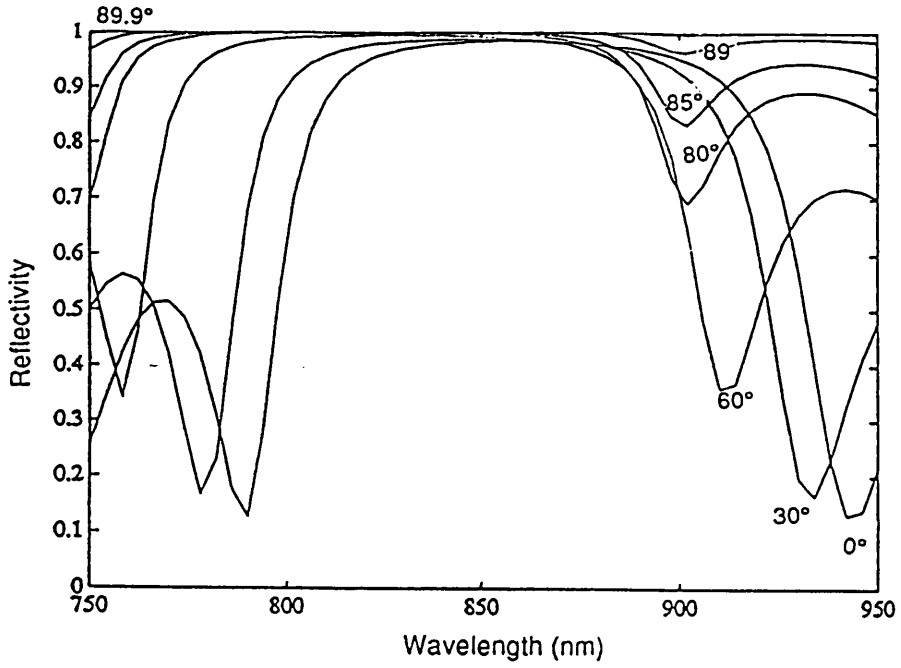


Figure 5.3a *Reflectivity of a 12 period stack in air as the incident angle is varied from 0° to 89.9°. At the centre wavelength, 860nm, the reflectivity increases despite the shift in wavelength of the high reflectivity band.*

The above situation relates to the case of a reflector stack in air, more important, however, is the case in which is light is incident from a semiconductor and this is shown in Figs 5.3b and c. For angles of 0 to 16° a similar effect is observed as before, with the reflectance band shifting in

wavelength, although in this case there is only a marginal increase in the peak reflectivity. In fact at the design wavelength of 860nm a slight decrease in reflectivity is observed from 93.8% to 92.95% at 12°, falling to 88.7% at 16°. An interesting case is that for light incident at 12°, corresponding to an incoming beam at 48.8° for the geometry shown below.

This is typical of a possible interconnect scheme in which the signal is passed along an array of electronic islands. Note how strongly the beam is refracted within the semiconductor, due to the large difference in refractive index. In fact 16° is the maximum angle possible for the case shown on the left, corresponding to light incident from air at 89°. As the incident angle within the semiconductor is increased further one approaches an angle at which total reflection occurs, this is equivalent to total internal reflection in a waveguide, for example. However there is a significant difference in that this occurs at a more acute angle, ≈42.7°, compared to 63.5° one would expect for two layers of n1=3.62 and n2=3.24, the latter being the average value for the reflector stack.

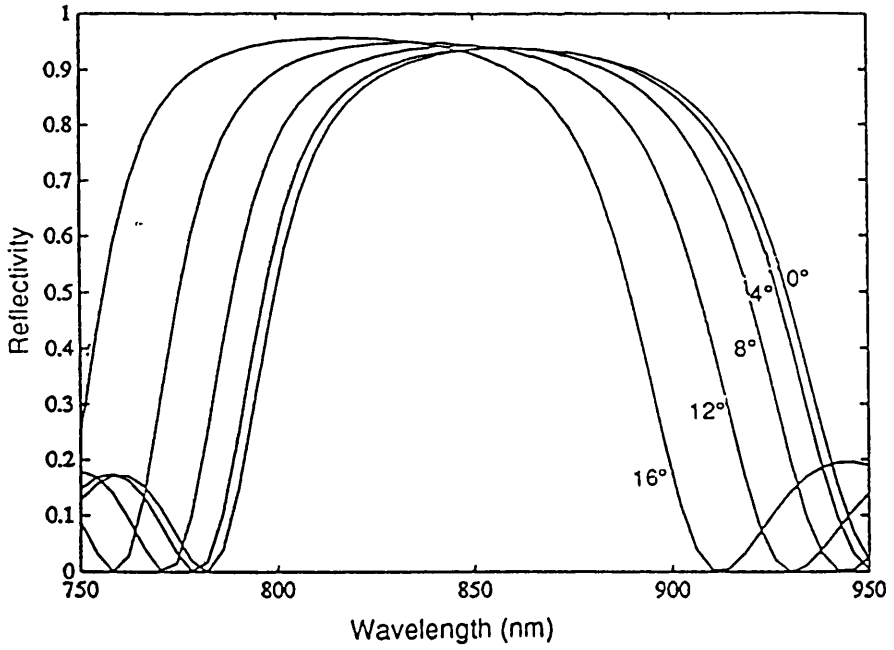


Figure 5.3b *Reflectivity of a 12 period stack in semiconductor as the incident angle is varied from 0° to 16°. At the centre wavelength, 860nm, the reflectivity decreases from 93.8% to 88.7%.*

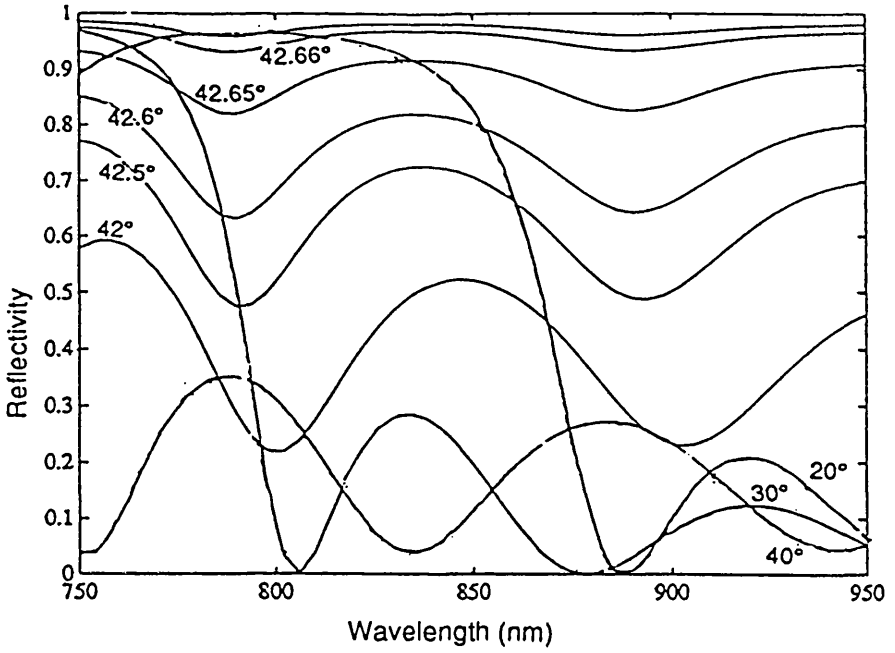


Figure 5.3c *Reflectivity of a 12 period stack in a semiconductor cavity as the incident angle is varied from 20° to 43°. Total internal reflection occurs at 42.7°.*

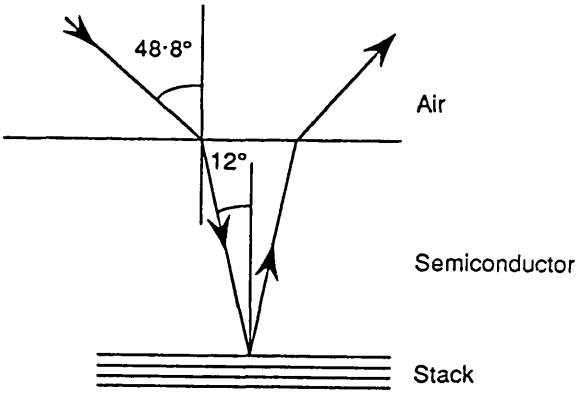


Figure 5.4 *Schematic diagram showing the geometry for light incident at an angle to an AFPM modulator structure. The large refractive index difference between air and semiconductor ensures that light is always incident near to the normal on the reflector stack.*

Even with a cladding layer of AlAs (n=2.98) total internal reflection does not occur until an angle of 55° is reached. A comparison is made below of the possible alternatives :-

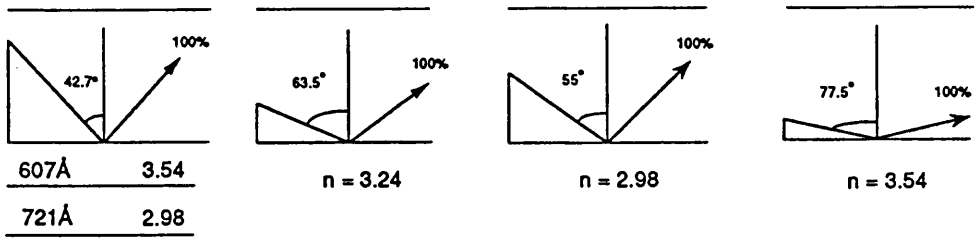


Figure 5.5 *By using a multilayer structure the angle of incidence at which total internal reflection occurs can be reduced. The refractive index of the incident medium was assumed to be n=3.62.*

The effect only requires a single period and could be used to improve guiding and launching into waveguide structures.

Because the insertion loss of the AFPM structure is dependent on the stack reflectivity, it is worth considering the effect of increasing the number of periods to 18. For any possible angle of light incident from free space it was found that the reflectivity seen inside the cavity, at the design wavelength, will never fall below 96.5%. Thus increasing the number of periods is also advantageous in increasing the operating tolerance.

5.2.2 Problems of Growth Tolerance

In addition to considering the sensitivity to operating conditions it is also useful to model the tolerance of the stack to growth variation. Figures 5.6a and b show the reflectivity spectra for stacks with ±5% and ±10% error respectively. The error is presumed to be the same in both layers and gives, as one would expect, a simple shift in the reflectance band. Both spectra are for light incident from free space and show that for even a 5% growth error the reduction in reflectivity would be unacceptable. Although such calibration errors do occur in growth, most often in MOCVD rather than MBE systems, the required tolerance is less severe than that governing the Fabry-Perot cavity itself. One final consideration is

when the thickness increase in one layer is offset by a reduction in another. Although there is some asymmetry, with a reduction in the peak reflectivity, it was found that the layers need not be precisely $\lambda/4$ thick. For any periodic structure, with layer thicknesses A and B, there will be a high reflectivity at the wavelength:-

$$\lambda=2(n_1A+n_2B) \qquad \text{Eqn 5.11}$$

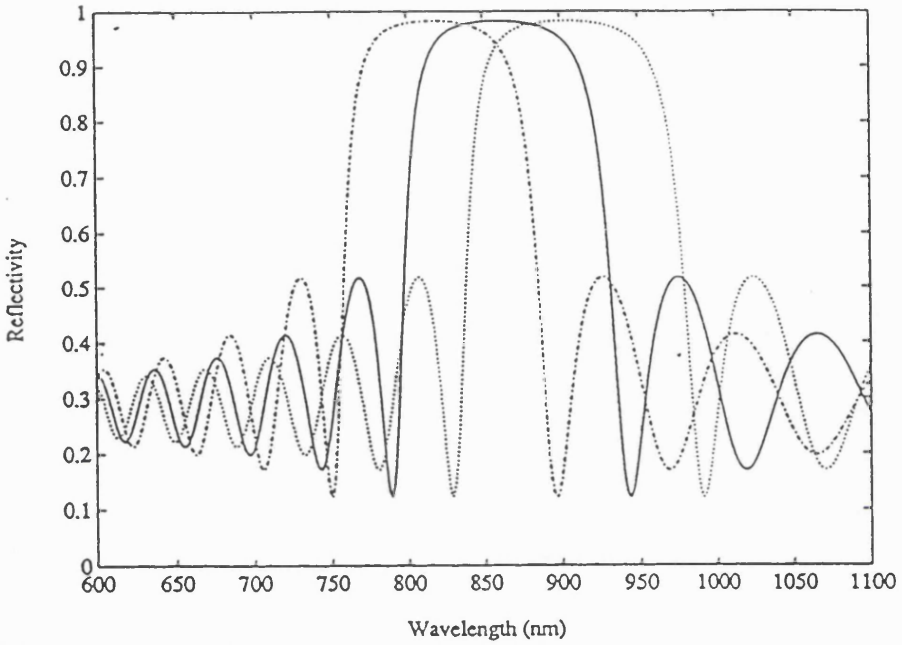


Figure 5.6a *Reflector stack with 0,±5% growth error*

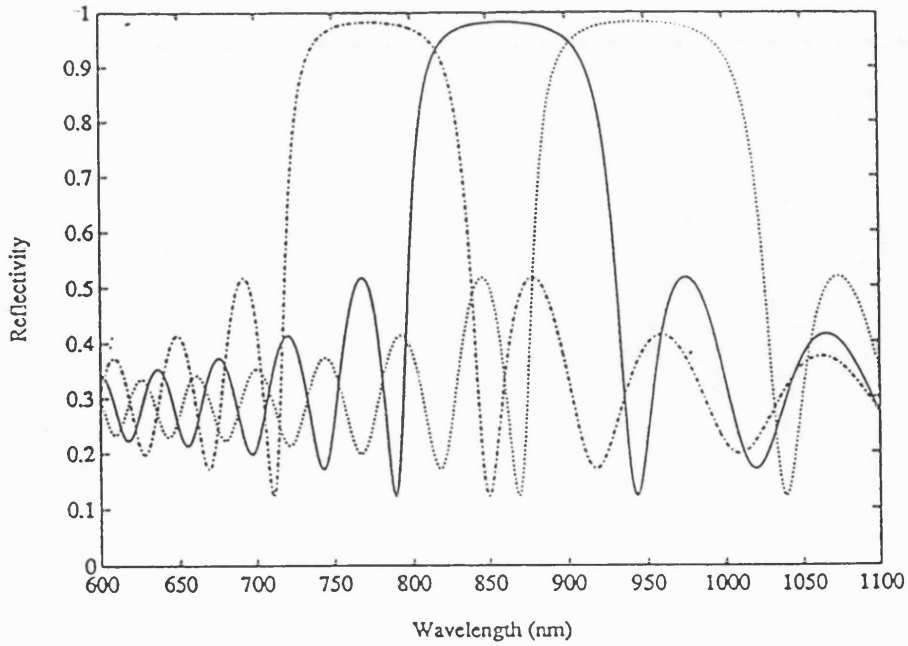


Figure 5.6b *Reflector stack with 0,±10% growth error*

5.3 PERFORMANCE OF REFLECTOR STACKS GROWN ON SILICON

5.3.1 MBE Grown Stacks

5.3.1.1 M199: A 12 period reflector stack grown on silicon by MBE

A promising start was provided by the growth of a reflector stack on silicon using the MBE process. The structure consisted of 11 periods of n^+ 606Å $Ga_{0.9}Al_{0.1}As$ / 721Å AlAs and a twelfth period of 594Å GaAs / 721Å AlAs, the GaAs providing a capping layer. The refractive indices were assumed to be 2.98, 3.54 and 3.62 for AlAs, $Ga_{0.9}Al_{0.1}As$, and GaAs respectively, at the design wavelength of 860nm. The top layer of GaAs was provided to ensure no surface oxidization would occur, and to provide the possibility of contacting. However, this layer does reduce the reflectivity slightly. Assuming an absorption of 10,000 cm^{-1} we can model this structure, and thus predict a maximum reflectivity of 94.9%, slightly less than the 98.2% expected for 12 periods of $Ga_{0.9}Al_{0.1}As$/AlAs. A 6μm n^+ GaAs buffer region separated the device layer from a low p silicon substrate.

Material studies of the reflector stacks are presented more fully in Chapter 3, here we limit ourselves to a brief description of the appearance, and a discussion of the device performance. Reflection spectra for different points across the wafer are shown in Fig 5.7 below.

The high reflectance band can be clearly observed and is centred around 840nm rather than 860nm, suggesting that the layers are somewhat thinner than desired. The maximum reflectivity was ≈86% when compared to a gold reference of 97%. Detection of the reflected signal was made using the computer controlled monochromator and data acquisition system, with the recorded data being normalized with respect to the reflectivity of a freshly deposited gold mirror. The spectra for plot D was intentionally taken from a particularly poor part of the wafer for comparative purposes. Across the whole surface of the wafer the reflectivity seemed slightly hazy, or milky, with a patchy appearance. Nevertheless these initial results were very encouraging, in fact their promise was confirmed by the high quality reflector stacks reported later.

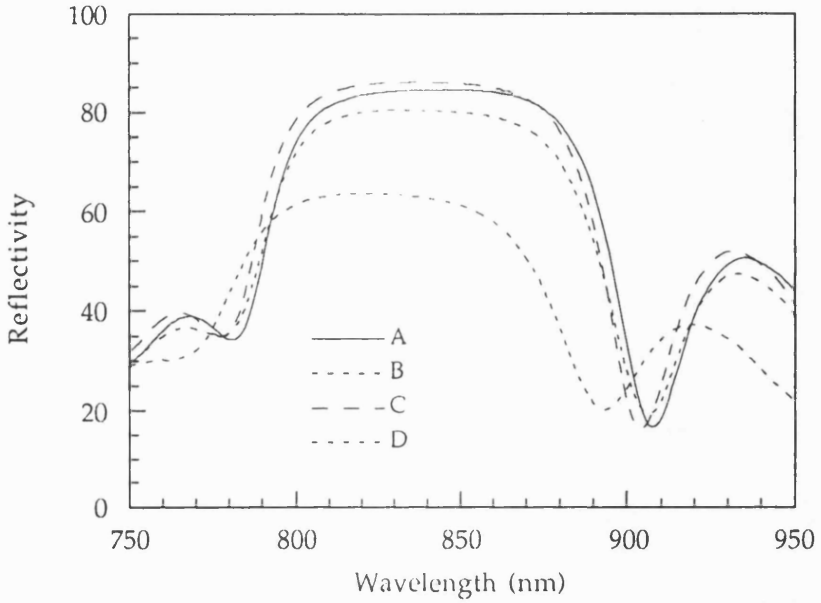


Figure 5.7 *Reflection spectra for M199, a 12 period stack grown on silicon by MBE. The plots A, B, C and D were taken from different parts of the wafer. Plot D was intentionally taken from a poor looking part of the wafer for comparative purposes. The maximum reflectivity is ≈ 86%.*

5.3.2 MOCVD Grown Stacks

5.3.2.1 QT105 and QT145: 15 period stacks grown on silicon by MOCVD

The MOCVD grown reflector stacks differed from those grown by MBE in that they employed a commercially supplied (Kopin) GaAs coated silicon substrate. The thickness of the pre-supplied GaAs epitaxial layer was 2.7μm, also deposited using the MOCVD process. Inspection of these substrates revealed a high quality surface, although still retaining a slight graininess. In the case of QT145 a GaAs control wafer was also placed in the growth chamber, allowing direct comparison to be made of the respective performance. The clean up procedure and renucleation still proved critical, as for the case of growing directly on the silicon substrate. The reason for this is that the GaAs coating is clearly highly strained, with

a high density of dislocations, and in order to realize a structure with good morphology the growth process had to be adjusted accordingly. These issues have been discussed more fully in Chapter 3. Following renucleation, a 15 period reflector stack was deposited. The increase in number of periods was chosen so as to improve reflectivity, but at the same time restricting the electrical resistance of the stack and the total epitaxial thickness. Reflector stacks with large numbers of periods are known to be of high resistance, an undesirable effect that is particularly problematic when designing VCSELs (Vertical Cavity Surface Emitting Lasers). We were perhaps over-cautious in this respect as the optical properties are more important at this stage of development, indeed studies reveal that resistance can be substantially reduced by grading of the reflector stack layers, a modification that has little effect on the reflectivity. Nevertheless, minimization of the total epitaxial thickness is desirable in order to reduce microcracking, this is found to occur if the epitaxial layer is >2.7μm, and increases with layer thickness. In our samples the coated substrates did not show any signs of microcracks, and the hope was that by minimizing the layer thickness, the probability of microcracks occurring would be reduced. Theoretical calculations showed that the reflectivity should increase from 98.24% for a 12 period stack, to 99.37% for a 15 period stack.

Inspection of the wafer after growth showed that deposition of the extra ≈2μm epitaxial layer had resulted in the usual degree of microcracking. Nevertheless, the surface appearance was greatly improved over M199, with only a slight haziness remaining. The reflectivity spectrum for QT105 is shown in Fig 5.8, normalized to the reflectivity spectrum of a gold plate mirror. The performance of the stack is exceptionally good and a peak reflectivity of 96% was measured. This is only ≈3.3% less than that expected for a similar stack grown on GaAs, although it has to be remembered that this difference becomes more significant once the stack is placed in a semiconductor cavity. A shift in the high reflectance band to longer wavelength is observed, indicating that the growth erred on the generous side.

It was thought at this point that the slight surface haziness or scattering could be due to the final epitaxial layer, in this case $Ga_{0.9}Al_{0.1}As$, not terminating growth completely evenly. To investigate this, a second reflector stack, QT145, was grown in which an additional AlAs layer was grown as a final capping layer, this was then etched back to reveal the

surface underneath. In all other respects the structure was identical to QT105. After etching, visual inspection revealed no apparent improvement in the surface quality, and the reflectivity spectrum reveals almost identical performance to QT105, Fig 5.8. TEM studies failed to reveal any surface roughness in either structure, so the scattering mechanism remains unclear. Fig 5.8 also shows the reflectivity spectra for the QT145 stack grown on the GaAs control wafer. The reflection band is shifted to shorter wavelength, suggesting that the growth rate in this part of the chamber is reduced. Most noticeably, however, the maximum reflection is substantially reduced. This is due to the difference in gas flow and vapour composition at the position in the MOCVD growth chamber where the monitor was grown. Because of the poor quality of the control stack, comparison was made with a previously grown stack on GaAs having the same layer structure (QT5). The reflectivity for this stack is also plotted in Fig 5.8, and the comparison confirms the high quality of the stacks grown on silicon. Nevertheless, the stack grown on silicon demonstrate a drop in maximum reflectivity of ≈2% when compared to the QT5 structure grown on GaAs.

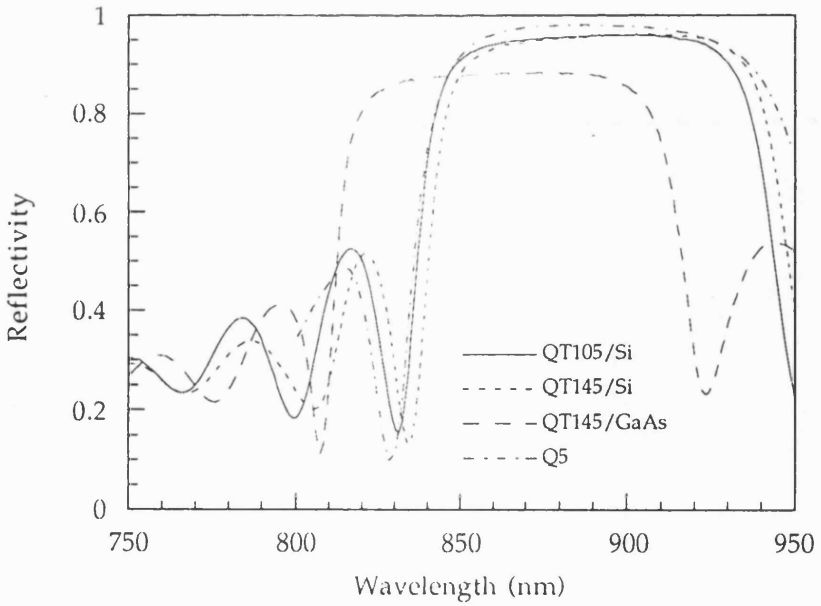


Figure 5.8 *Reflectivity spectra for QT105 and QT145, both 15 period stacks grown on silicon. The QT145 control stack grown on GaAs had poor performance so comparison is made with a previously grown stack on GaAs. The high quality of the GaAs/Si stacks is evident, with max R=96%.*

5.4 RESULTS FOR MODULATOR STRUCTURES GROWN ON SILICON

From the initial stages of the project modulator structures were grown that incorporated reflector stacks, designed to enhance the modulation characteristics. The intention was to make an initial assessment of device performance, and thus define the key areas of necessary improvement. At the same time, research was conducted into the nature of the quantum well electroabsorption, and the reflectivity of the quarter-wave stacks. These results could then be used, first to interpret the modulator characteristics, and second to suggest means of improvement which could be subsequently incorporated. The earliest modulators were grown by MBE and began with M130. This was grown before much was known about the specific problems associated with the growth of GaAs on silicon for modulator devices, and the performance is predictably limited. In the next section the development of the modulators is traced, leading up to the more recent MOCVD grown devices, designed using experimental results for electroabsorption and stack reflectivity. These demonstrate reflectivity changes of 51%, and contrast ratios of up to 9.3dB.

Results are presented for the electrical performance of the devices, photocurrent spectra, and reflection spectra. Two systems were used for the optical measurements, the first was the monochromator system previously described, allowing a wide range of wavelengths to be scanned with very low noise, but with a limited minimum spot size. This system was thus particularly suitable for photocurrent measurements. For testing the smallest devices a laser source was necessary, this was initially provided by a tuneable dye laser pumped by an argon ion laser, allowing scans to be made in the range 800-900nm. This was later upgraded to a Ti-Sapphire tuneable laser giving an extended wavelength range, lower noise and simpler operation. The smaller spot size possible with the laser provided a means of measuring reflectivity spectra for devices with windows of as little as 50μm x 50μm, impossible with the monochromator.

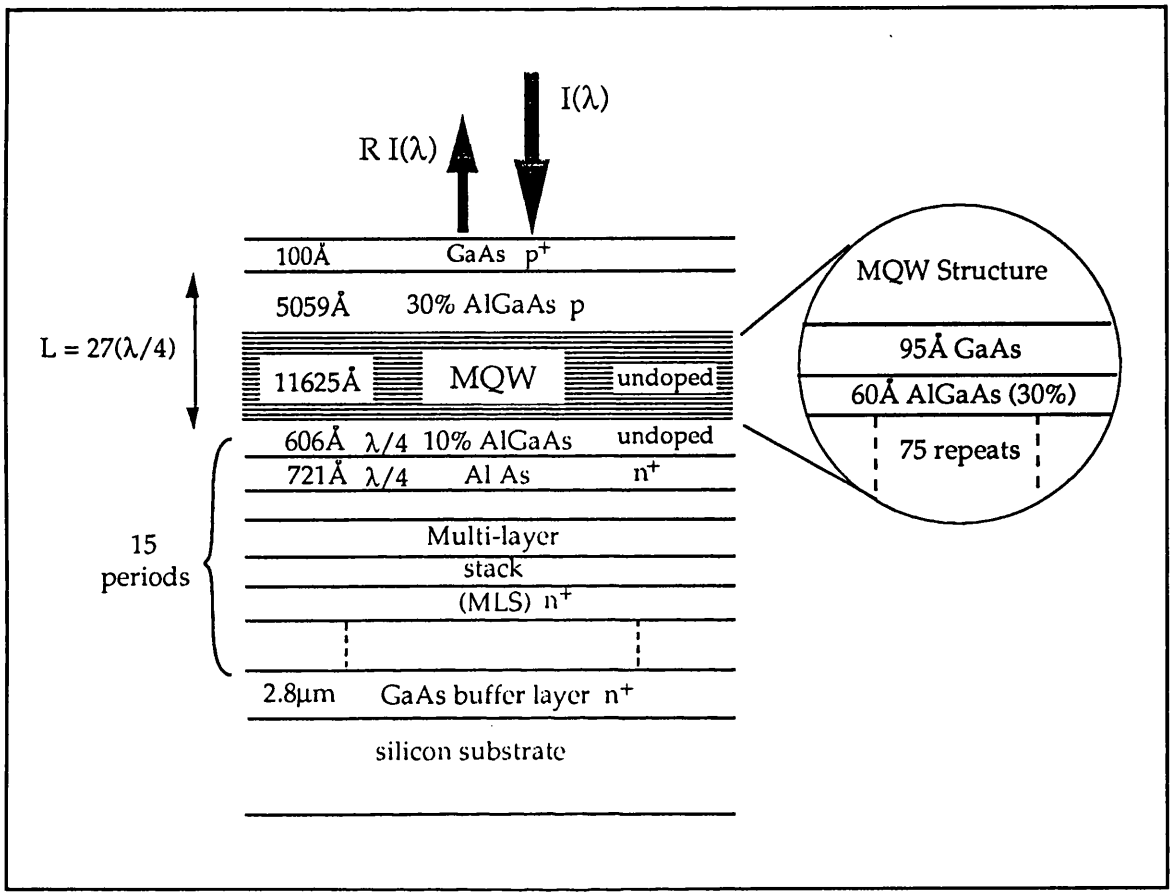


Figure 5.9 *Schematic diagram of a typical microresonator reflection modulator using an asymmetric Fabry-Perot modulator. The number of layers in the quarter-wave multilayer stack can be varied to adjust the back reflectivity, while the front reflectivity is provided by the air-semiconductor interface.*

5.4.1 Electrical Performance of Modulator Structures

The AFPM modulator structures were fabricated into *pin* diodes similar to the devices described in the preceding chapter. The I-V characteristics were then assessed, and we compare here the results for devices grown on both MBE and MOCVD. A summary of the different devices is given in Table 5.1, and the modulator structure is illustrated in Fig 5.9. The devices were grown over a period extending from almost the beginning to close to the end of the project, and thus provide a measure of the improvement attained. In the case of the most recent MOCVD structures a GaAs substrate was placed next to the silicon substrate, so that a control structure could be grown simultaneously. Devices were then fabricated in the same processing run using both substrates, allowing the direct comparison

presented here to be made. Unfortunately, due to the heavy demands on the growth systems, and indeed on the clean room time, it was not always possible to make this direct comparison. However, a large store of similar structures grown on GaAs substrates had been built-up previously, and these were used to give a measure of the relative performance of devices grown on silicon.

Layer No.	MQW (well/barr Å)	Periods	Reflector Stack Buffer	Growth
M130	95/60	75	12x(721Å/607Å) 6μm GaAs	MBE
M200	95/60	75	12x(721Å/607Å) 6μm GaAs	MBE
QT183	95/60	75	15x(721Å/607Å) 2.8μm GaAs	MOCVD
QT253	95/60	75	15x(721Å/607Å) 2.8μm GaAs	MOCVD

Table 5.1 *Table of GaAs on Si MQW AFPM modulator structures.*

Experience from fabricating MQW diodes on GaAs substrates had shown that a dark current of 10nA or less, at 10V, represented a "good" device. This figure applied for whatever size of device was chosen from the mask set employed. In most cases this was a set that consisted of four mesa sizes, generally referred to by their square window dimensions of 20μm, 50μm, 100μm and 250μm. The total active areas for these devices are, respectively, $7.35x10^3\mu m^2$, $21.6x10^3\mu m^2$, $113.4x10^3\mu m^2$ and $175x10^3\mu m^2$. In addition a second mask set was available with windows of 400μm and 800μm and active areas of $291.6x10^3\mu m^2$ and $1.17mm^2$. Reference was also made to devices grown on GaAs for comparison of forward bias characteristics. This was done firstly because these represented a known standard that included both device and processing quality, and secondly because of the difficulties of measuring a specific forward resistance. High forward biases were liable to damage the devices and result in excessive heat build-up, which would in itself cause a change in the measured resistance. The relative contributions of contact resistance and device resistance are also difficult to ascertain, and were extremely variable. It was thus decided to measure the current up to 1V forward bias, which gave a measure of the steepness of the device turn-on, to ensure that high resistivity was not a cause of low measured dark current. The results of the I-V characterization are listed in Table 5.2 below.

Device	Buffer Layer	Area ($10^3\mu m^2$)	Voltage at 10nA	Dark Current Vr=5V	Dark Current Vr=10V
M130	6μm	21.6	2V	25nA	45nA
		113.4	-	0.85μA	7μA
M200	6μm	21.6	14V	<1nA	4nA
M490	6μm	113.4	3.7V	10nA	170nA
QT183	2.8μm	113.4	17V	1.5nA	3nA
QT253	2.8μm	113.4	26V	<1nA	1nA
		291.6	18V	2nA	4nA
QT253/GaAs	-	291.6	25V	<1nA	2nA

Table 5.2 *Table showing dark currents for modulator structures. The presence of reflector stacks was found to greatly improve the quality and uniformity of the devices. For the small sizes most suitable for systems applications leakage currents at an operating voltage of 5V are <1nA.*

An interesting comparison can be made with the results for the simple *pin* devices given in Chapter 4.4. The structure M130 differs from M121 only in having a built-in reflector stack, however, the I-V characteristics are much improved. The reasons for this improvement were not immediately clear but the following possibilities were considered:-

i) The design of the reflector stack may inhibit dislocation movement into the diode region.
ii) The extra thickness between the GaAs/Si interface and the active region of about 1μm.
iii) Increased resistance due to the reflector stack will reduce the overall magnitude of the leakage currents.
iv) A change in the growth conditions.

No intentional changes were made to the growth conditions, although even with MBE there is a certain degree of variation between growth runs. Results from the other modulator structures (grown by both MBE and MOCVD) also show a substantial reduction in leakage current, and a consistent pattern started to develop. It is therefore believed that the improvement is due to a combination of the first three factors mentioned

above. Devices grown on reflector stacks also showed improved uniformity in electrical characteristics across the wafer. It is well known that reflector stacks incorporating AlAs can have significant resistance and it is clear that this would result in reduced measured values of dark current. To check this, reference was made to the forward bias currents, however, we noted a much larger improvement at reverse biases than was accounted for by any increased resistance. (An exception was an MBE grown structure which incorporated a 16 period reflector stack, not listed above, for which the resistance also reduced the current in forward bias). This general improvement cannot be accounted for simply by an increase in the effective buffer layer thickness, and a consequent improvement in material quality. The benefit arises as a result of the filtering of threading dislocations by the reflector stacks themselves. The plots in Fig 3.16 provide evidence of this. They show the threading dislocation density as a function of epitaxial layer thickness for a number of structures grown with and without reflector stacks, the former showing a reduction on average of a factor of two. It is this reduction that is most likely responsible for the improved device quality.

Further evidence is obtained from a TEM analysis of a reflector stack structure grown by MOCVD, as shown in Fig 3.15. It is apparent that most of the dislocations stay within the first 2μm of GaAs buffer layer, and, of those that do penetrate further, some of the stacking faults and microtwins are observed to be bent out by the reflector stack. It is not clear what the precise mechanism is that improves the performance of devices incorporating reflector stacks, although the use of multiple strained layers has been shown to improve GaAs on Si material quality (see Chapter 3.3.3). The reflector stack layers used here are themselves unstrained, although the complete structure is under thermal strain, but we appear to obtain similar improvements.

Table 5.2 also shows the expected improvement in leakage currents with decreasing mesa size. The smaller sized mesa would be most appropriate for applications involving optical interconnects since they would be required from device speed considerations. A combination of small mesa size and the use of reflector stacks results in measured dark currents of the order of 1nA at 10V applied reverse bias; even devices of area $113.4 \times 10^3 \mu m^2$ show only 3nA at the same bias. Note that this compares well with the figure of 10nA dark current at 10V we set as a target based on experience with devices grown on GaAs. The dark current

for some smaller devices can be seen to reduce at a faster rate than a simple scaling to area, the reason for this is not clear but it could indicate a statistical variation in dislocation density across the wafer.

It is interesting to compare M130 with the later M200. Despite sharing the same design structure, comparison of their I-V characteristics shows the latter device is significantly improved:-

Applied Bias	*M130*	*M200*
-10V	-45nA	-4nA
-15V	-55nA	-12nA
-20V	-75nA	-32nA
-25V	-210nA	-120nA
-30V	-1.3μA	-1.1μA
-35V	-8.4μA	sharp bdown
-40V	-35μA	
+0.5V	5nA	4nA
+0.6V	26nA	30nA
+0.7V	70nA	300nA
+0.8V	144nA	2μA
+0.9V	210nA	8μA
+1.0V	+300nA	18μA
+2.0V	1.4μA	-

Table 5.3 *The table shows I-V characteristics for M130 and M200, two devices with identical layer structures. Improvements in the growth resulted in substantially improved performance for the later device. In addition to lower dark currents M200 has more rapid turn-on indicating reduced resistance in the stack.*

While matching the figures for M130 as regards leakage current, M200 has a much steeper breakdown indicating better diode performance, it also has much more rapid turn-on characteristics suggesting a smaller inherent resistance. Devices grown by MOCVD also show that the use of reflector stacks can be used to reduce dark currents, while maintaining excellent diode properties. Complete I-V curves for a number of devices are shown in Fig 5.10.

The consistency and reliability of devices is obviously an issue of major concern. We have stated that operating devices at large forward biases results in reduced lifetimes and eventual failure. However, the devices are intended to operate at moderate reverse biases, and in this mode reliability has been extremely high. Restricted to operation between 0 and -10V, no deterioration in devices more than two years old has been observed. Another area of possible concern is that of the microcracking in devices. Contrary to expectations there was usually no correlation between the density of microcracks and device performance. An exception was that of M490, this thick structure had areas of heavy cracking which had an adverse effect on device performance. Damaged devices typically had the characteristics of an electrical short, or showed large leakage currents and poor breakdown voltages. Inspection of M490 revealed that the perpendicular microcracks would on occasion cross over each other, the frequency of which had a strong correlation with device performance. In all other devices a microcrack travelling in one direction would be terminated if it intersected another travelling in the perpendicular direction, giving the appearance of a "T-junction". The density of microcracks was therefore usually restricted in this way, and the strain in the layers relaxed. It appears that in M490 the strain was such that microcracks could propagate across each other, resulting in damage to the devices.

A more typical sample was QT183. Again the layer structure is thicker than for a simple *pin* diode, and, as expected, the microcracking was proportionately greater. However no adverse effects of the cracks could be detected. In some cases those areas of the wafer which were most heavily cracked subsequently produced some of the best performing devices. Compared to the thinner *pin* diodes the electrical uniformity was also improved, indicating that the reduction in dislocation density was of more importance than the concomitant increase in microcrack density. Comparisons were also made between the same devices before and after thinning, cleaving, and mounting on headers. It was feared that due to the strain in the layers the devices might be damaged during this process, but they turned out to be remarkably resilient. For example, at 10V reverse bias QT183 showed 2nA leakage before mounting and just 3nA afterwards. Initially there were problems due to the inherent strength of the silicon substrate, and the fact that it tends to cleave along a different axis to GaAs. But it was found that by greater than normal thinning of the substrate, and

by use of a low damage inducing diamond saw, the above results could be achieved. These represented a significant improvement over earlier reported results where the above operations typically increased leakage currents by about 20%. Cutting out very small pieces of the wafer still remains a problem, but one that is perhaps unlikely to occur in device applications where large integrated structures are preferable to small discrete packages.

In the previously described devices the microcracks tended to be parallel or perpendicular to the mesas. To investigate whether the crack orientation was significant, devices were fabricated using the QT253 wafer with the microcracks running at 45° to the mesas. Testing of these devices did not reveal any measurable difference in the I-V characteristics.

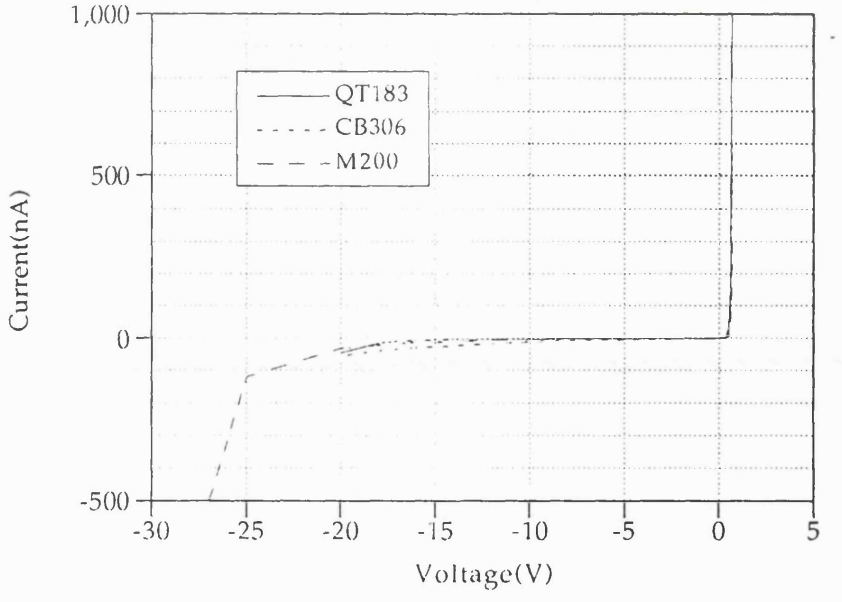


Figure 5.10 *I-V characteristics for GaAs on Si mesa pin diodes showing high breakdown voltages and low leakage currents. QT183, MOCVD grown reflection modulator; CB306, MOCVD grown pin diode test structure; M200, MBE grown reflection modulator.*

It was impossible to come to any definitive conclusions as to the relative yield of devices grown on silicon substrates as opposed to those on GaAs. This was due to the variability of the control devices themselves. Although GaAs devices in general have a lower yield and are not as

durable as their silicon counterparts there seem to be no fundamental problems in commercial manufacture. Nevertheless, in the devices reported here the yield of those grown on GaAs could be as low as 25%. There are a number of possibilities why this may occur:-

i) Defects in the material could be introduced during growth. A common example would be that of oval defects in MBE. This is due to "spitting" of the source elements, resulting in large "lumps" of material falling on the wafer surface, rather than a smooth stream of atoms. These inhibit growth, causing pits in the epitaxial layer. If a layer of gold is then deposited it is possible to short out the top and bottom layers of the structure, causing failure of the device. In the case of MOCVD this type of defect should not occur, as a gas phase is employed. However, this brings with it greater possibilities for contamination.

ii) Contamination of the wafers between growth and processing. In all cases the wafers were remotely sourced, whether from Philips or the University of Sheffield, and had to be sent on to UCL. In most instances these were then inspected for visual imperfections, and in the case of the AFPM structures had to be optically scanned to select the appropriate part of the wafer before processing. Pressure on clean room facilities also resulted in not inconsiderable delay between receipt of the wafers and their subsequent processing. There was thus ample opportunity for all sorts of undesirable impurities to contaminate the wafer surface, not all of which can be removed however thorough the clean-up procedure

iii) Problems in the processing and fabrication steps. These are optimized for flexibility and small volumes rather than large production runs. This results in a trade-off between the versatility gained and consistency. On some occasions the appearance of the processing would be poor, with stray deposits remaining on the surface, or variable metallization, with contacts sometimes missing.

It was thus very difficult to ascertain the underlying material quality, hidden as it was by so many variables. Making a qualitative judgement one could say that the modulators on GaAs substrates were of more

consistent quality than those on silicon, while both were improvements over *pin* diodes grown on silicon.

5.4.2 *Photocurrent and Reflection Measurements of AFPM Modulator Structures*

While the devices described in this chapter were primarily designed to operate as reflection modulators, it is also important to realise that they are also very effective photodetectors. Measurement of photocurrent spectra therefore provides many useful functions, both revealing information about the fundamental nature of the device and giving a view of the detector performance. From the photocurrent spectra we can get some idea of the excitonic absorption characteristics, and the effect of the resonant cavity on the total absorption. By applying a bias to the device we can observe the change in photocurrent level, which gives a measure of the quantum efficiency.

5.4.2.1 *MBE Grown Modulator Structures*

The first modulator structure grown on silicon, M130, makes an interesting comparison with its companion *pin* diode M121. The latter, described more fully in the preceding chapter, had low quantum efficiency with a reverse bias of 2V causing a ten fold increase in photocurrent. This is due to dislocations trapping the free carriers before they can be swept out of the device; in the presence of an applied field they are accelerated and so have a greater chance of being collected. Unfortunately, increasing reverse bias increases the leakage current and so makes detection of the photocurrent more and more difficult. Unlike the better MOCVD *pin* diodes, the photocurrent level of M121, and therefore the quantum efficiency, does not saturate with increasing reverse bias. Before this point is reached the leakage current becomes dominant, and measurement of the photocurrent becomes impossible. Similarly, no saturation is observed for in the case of M130. Nevertheless, a substantial improvement is observed, the photocurrent being of the same order of magnitude for both

the 0V and 6V plots. This suggests the quantum efficiency of M130 with zero applied bias is higher than that of M121. Alternatively, if the device has higher resistance some of the applied bias may be dropped across the reflector stack, reducing the effective bias across the device and thus the measured photocurrent. This may be partly true but interpretation of the photocurrent spectra with and without applied bias, in Fig 5.8 below, suggests that most of the bias is in fact being dropped across the intrinsic region.

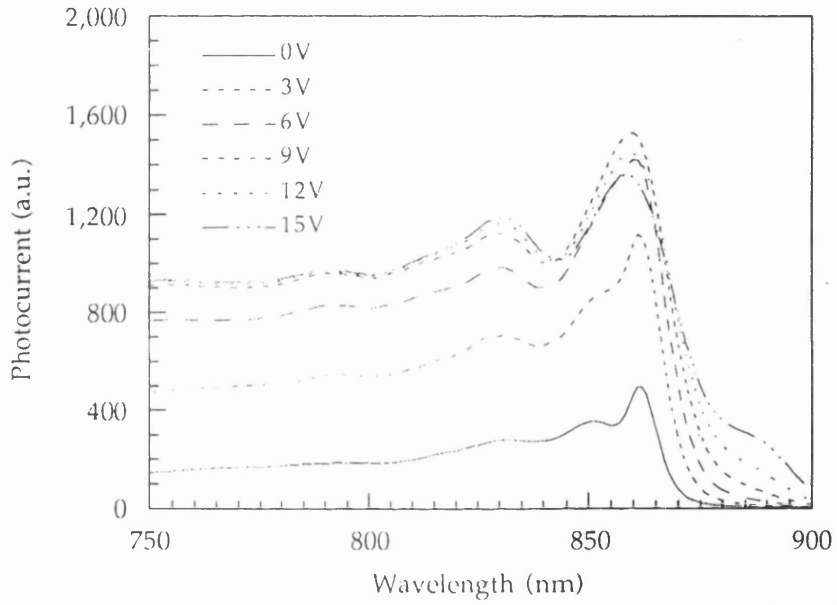


Figure 5.10 *Photocurrent Spectra for M130. A single excitonic peak can be seen at about 850nm, and a larger peak at 860nm due to resonant enhancement by the Fabry-Perot cavity.*

Consider the spectrum for zero bias where the large resonant peak at about 860nm is believed to be due to Fabry-Perot enhancement, and the small peak at 851nm due to the heavy hole excitonic transition. Now when a bias is applied the resonant peak is enhanced, and a trough develops just short of 850nm. We can interpret this as a slight shift of the excitonic peak into the resonant region, thus enhancing the photocurrent, this shift would only occur if the voltage was actually being dropped across the intrinsic region. When compared to what one might expect on a GaAs substrate the excitonic and resonant features are less well resolved and, as for the *pin* diodes, no separate light hole transition is visible.

As expected from the absorption spectra of MQW *pin* diodes on silicon the excitonic peak is slightly broader and less resolved than is typical on GaAs. In the case of the modulator structure this effect is further exaggerated by the influence of the resonant cavity. When the resonance is situated in the band-tail, to the long wavelength side of the excitonic peak, its effect will be to increase the photocurrent at this point - since the light is reflected back and forth within the cavity. This increase in magnitude will thus obscure the actual excitonic absorption peak. Further broadening occurs as the excitonic peak, itself already broadened due to strain, will now extend further into the resonance. At the peak itself the contribution from the resonance will be small, but the magnitude of the absorption edge will be magnified by its proximity to the resonance. Given these difficulties M130 presented a promising first step. We could observe both excitonic and resonant effects, and the reverse bias characteristics were such as to allow reasonable modulation voltages to be applied. It will be noted that at shorter wavelengths the resonant peaks are less pronounced, a corollary of reduced cavity finesse due to the increased absorption.

Optical measurements were made on several devices using a dye laser source, tuneable over the wavelength range 800-870nm, with the beam focused down onto the device windows by means of a microscope objective. It was not possible to use the monochromator to measure the reflection of these devices, due to their small size, with optical windows of only 50μm. Figure 5.11 shows the reflection spectra for a $21.6x10^3\mu m^2$ device. With 8V applied bias 31% modulation is achieved at 865nm, corresponding to a reflectivity change of 42.5% to 55.5%. Alternatively the device can be operated in low-loss mode at a wavelength of 870nm, where modulation of 24% is still possible but with the 0V state giving 72.5% reflection.

Interpretation of the reflection spectrum is complicated by the precise characteristics of the reflector stack and the Fabry-Perot cavity. However, it is clear that the quantum confined Stark effect shifts the excitonic peak to a longer wavelength, and in particular into the Fabry-Perot resonance, thus enhancing the change in reflection. This is the same effect that can be observed in the photocurrent spectra of Fig 5.10. This device was the first multiple quantum well optical modulator incorporating a quarter-wave reflector stack to be grown on silicon. At the time, the modulation of 31% relative change in reflectivity with 8V

applied bias was the best reported for a reflection modulator grown on silicon.

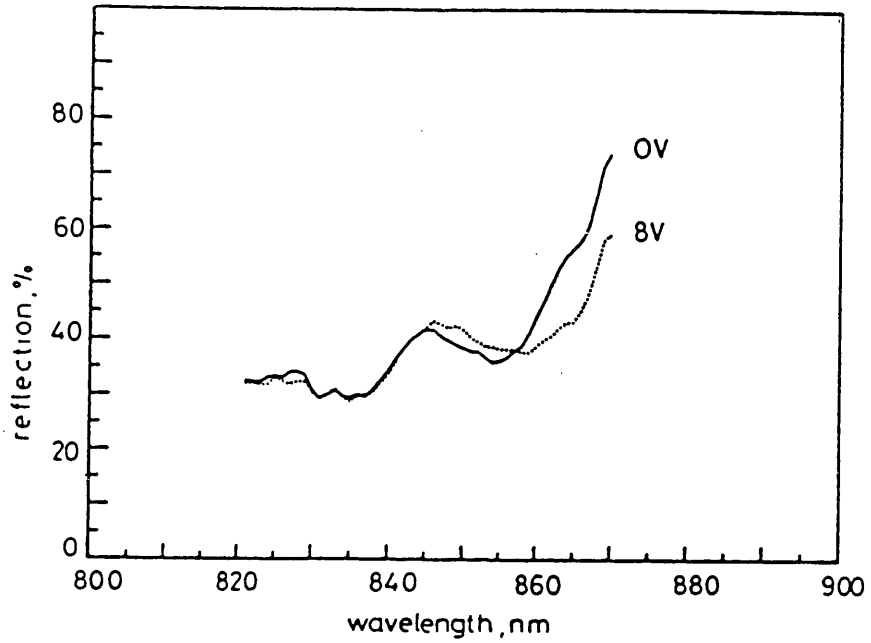


Figure 5.11 *Room temperature reflection spectra for M130, the first GaAs on Si MQW reflection modulator. A 31% relative change in reflectivity was achieved at 865nm for 8V applied bias.*

The M200 devices had a similar structure to M130, but initially looked unpromising due to a large area of the wafer having a poor appearance. In the event, those parts of the wafer that were suitable for making devices actually showed a marked improvement over the previous structure. Modulators were fabricated in the 50μm window size, and the photocurrent spectra illustrated below, in Fig 5.12. The excitonic peak and the resonant wavelength appear to be too close together, resulting in one main combined peak, with a shoulder at 850nm due to excitonic absorption. As a voltage is applied the exciton shifts to slightly longer wavelength, enhancing the natural Fabry-Perot resonance at 857nm. This is about 5nm lower than the design wavelength and accounts for the exciton peak being obscured, limiting the potential modulation performance.

Due to the proximity of the resonant wavelength to the exciton peak it was interesting to measure the photocurrent at a lower temperature. The reasons for this were twofold, firstly the exciton peak

shifts to shorter wavelengths more rapidly than does the Fabry-Perot resonance, and secondly reducing the temperature reduces the broadening. The result of both of these should be to resolve the single peak at room temperature into separate excitonic and resonance features, making interpretation of the spectra easier. This was indeed the case as can be seen from the photocurrent spectra in Fig 5.13, recorded at 263K.

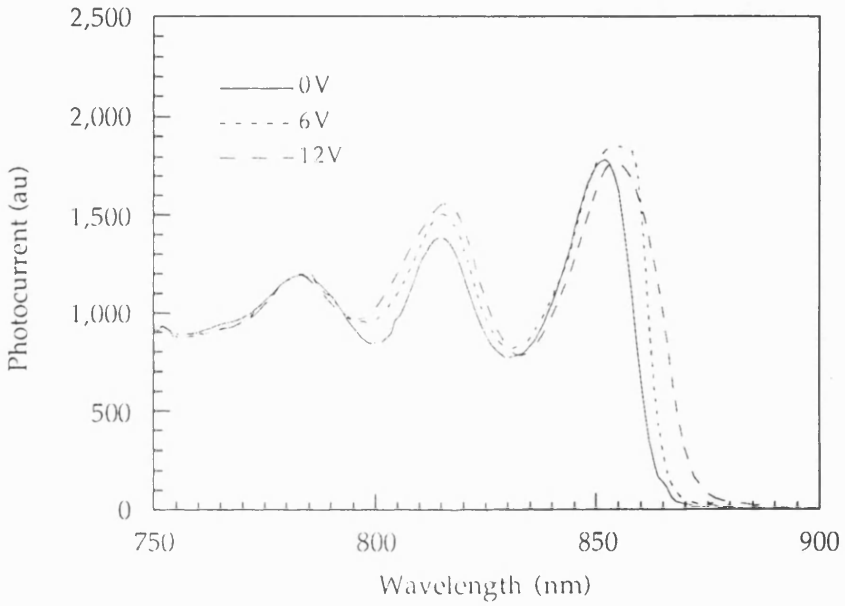


Figure 5.12 *Normalized photocurrent spectra for the M200 GaAs on Si reflection modulator. The exciton peak and the resonant wavelength are too close together and are therefore difficult to resolve. Nevertheless, a small increase in signal is observed at 6V applied bias as the exciton is shifted into the resonance.*

Another important difference between M130 and M200 is the relative quantum efficiencies. In the case of M130 the level of photocurrent increases by a factor of six as bias is applied to the device, saturation occurring at about 9V. For M200 the level only increases by a factor of two and saturation occurs at about 6V. The maximum photocurrent at 750nm is similar in both cases so it seems that the quantum efficiency of M130 at 0V is lower than for M200. The improvement is a sign of the increased device quality of M200, with a reduced probability of electron trapping in the intrinsic region.

To observe in more detail the changes to the exciton absorption, and the resonant cavity characteristics, photocurrent spectra were taken over a range of temperatures from 77K to 373K. Examples of the measured spectra are shown in Figs 5.14a and b, which were taken between 77K and 223K. The exciton peak can be seen to shift at a faster rate than does the resonance. At 77K the exciton and the resonance are superimposed, but as the temperature increases the exciton becomes resolved, and moves to longer wavelength than the resonance. As the temperature is further increased to 273K, the next resonance becomes visible on the shoulder of the exciton peak. The two become superimposed at 353K, before the exciton is resolved once more at 373K. The exciton peak actually shifts from ≈809nm at 77K to ≈870nm at 373K, or an average shift of 0.206nm/°C. The equivalent shift for the resonance is from ≈809nm to 822nm, at an average rate of 0.044nm/°C. The exciton shift is governed by the band-gap change with temperature, while the resonance is affected by both thermal expansion and the change in refractive index.

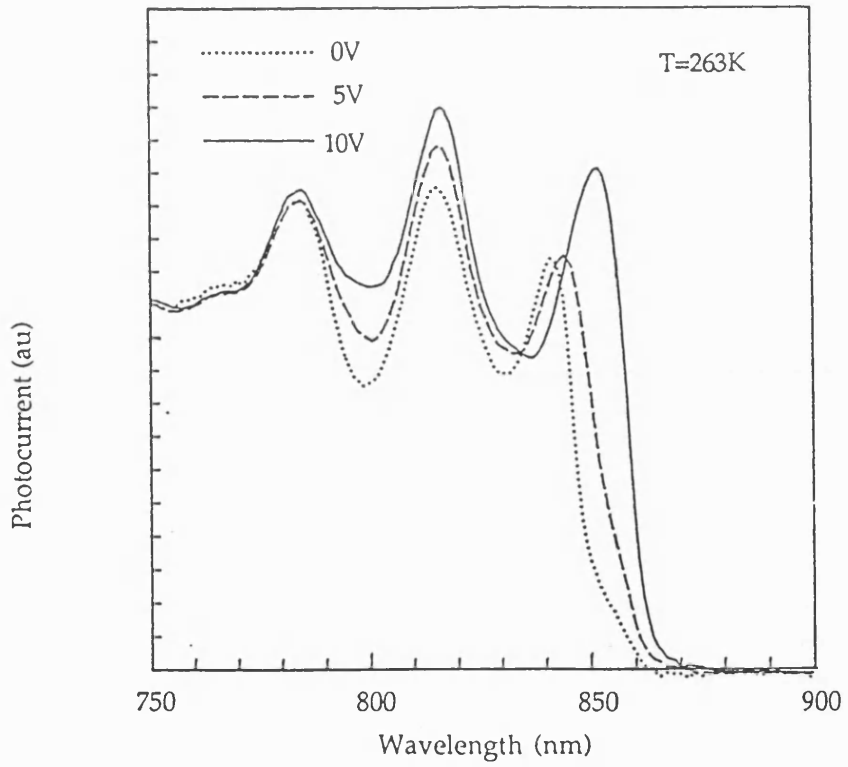


Figure 5.13 *Normalized photocurrent spectra for M200 at 263K showing resolved excitonic and resonant peaks. As a bias is applied the exciton is shifted into the resonance, resulting in a large increase in absorption and thus photocurrent.*

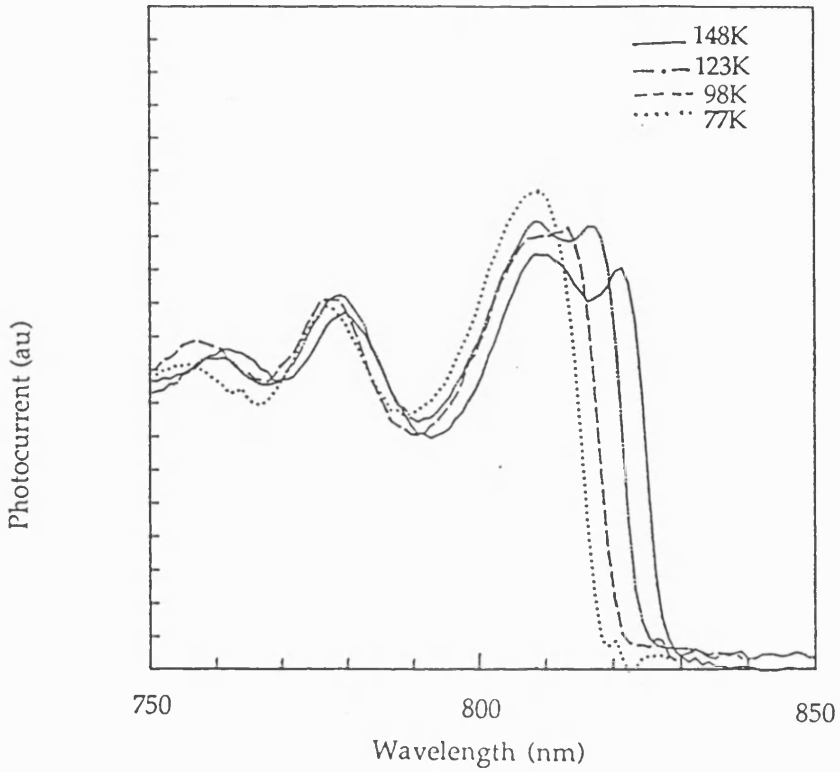


Figure 5.14a *Normalized photocurrent spectra for M200 measured at 77K, 98K, 123K and 148K. At 77K the exciton and the resonance are superimposed, but as the temperature increases the exciton becomes resolved, and moves to longer wavelength than the resonance.*

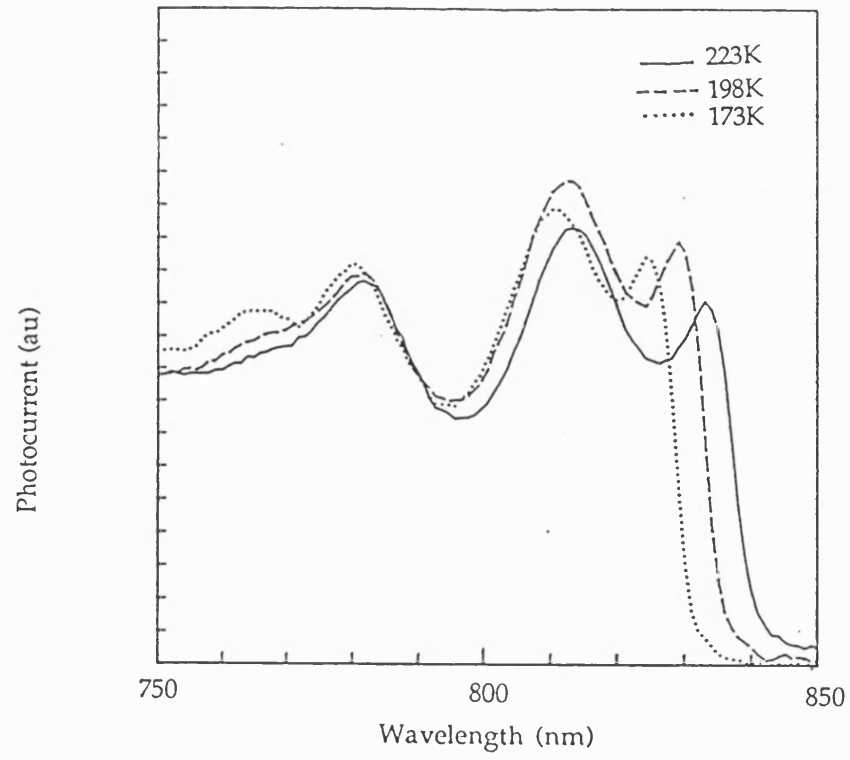


Figure 5.14b *Normalized photocurrent spectra for M200 measured at 173K, 198K and 223K. The exciton continues to shift faster than the resonance and is clearly resolved.*

Reflection spectra for the M200 modulator are shown in Fig 5.15. A contrast ratio of 6.4:1 was achieved at 14V bias and at a wavelength of 856nm. Reflection changes of 22% were achieved with a number of devices and typically with voltages of 12V. Temperature tuning of the device, in order to attain the ideal separation between the excitonic peak and the Fabry-Perot resonance, resulted in an increase in the maximum reflectivity change to 27% at 5°C for 12V bias. Although these results represented the best performance at the time of modulators on silicon, they are not as good as those achieved with GaAs substrates. The reason for this is that the reflectivity of the Fabry-Perot resonance at 861nm is low, due to reduced reflectivity of the stack.

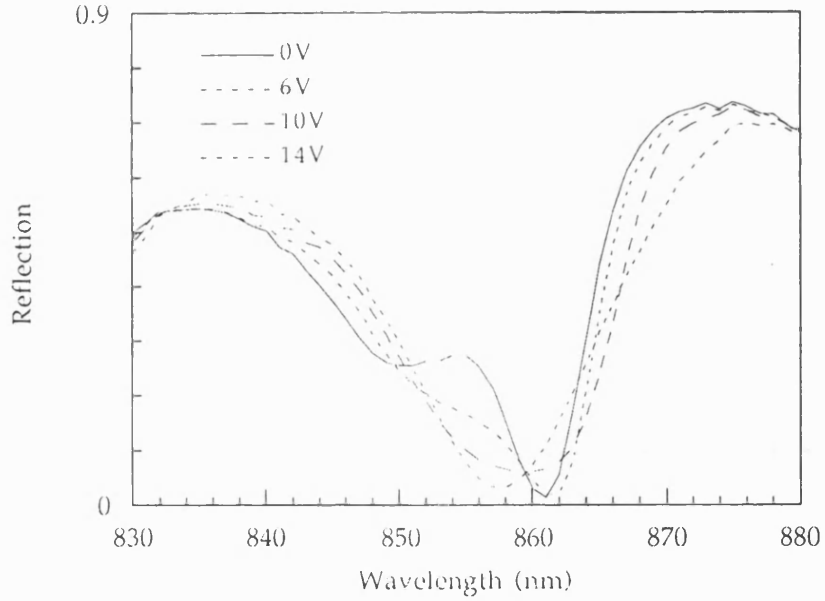


Figure 5.15 *Reflection spectra for the M200 modulator. A maximum reflection change of 22% was measured and a contrast ratio of 6.4:1 was achieved at 14V bias and at 856nm. The low value of reflectivity at the 861nm resonance was caused by a lower than desired back reflectivity.*

A number of other modulator structures were grown by MBE. However, these did not improve on the performance of M200 due to a number of problems relating to the growth. These were one or more of the following: poor material quality affecting the reflectivity; location of the Fabry-Perot resonance at the wrong wavelength; incorrect quantum well thickness; poor electrical characteristics due to severe cracking in devices with large

buffer layers and 16 period reflector stacks. The ability to grow the Fabry-Perot cavity at the right thickness and with acceptable uniformity is an important issue. Without it there will naturally be doubts about practical applications due to poor yields and low reproducibility. Normal practice for fabricating test devices was to optically scan the as-grown wafer in order to select the most suitable part, at which the cavity wavelength and the reflector stack meet the design criteria. Although none of the subsequent MBE grown modulator structures were able to improve on the modulation performance of M200, optically scanning suggested a high degree of uniformity across the wafer. Combined with the asymmetric Fabry-Perot cavity modulator's relative insensitivity to wavelength change this should give higher than expected yields. To quantify this the Fabry-Perot resonance for an MBE grown structure was recorded over the extent of the wafer. To carry out the mapping a tungsten source was focused onto the wafer and the reflectivity spectrum recorded by an optical multichannel analyser. A plot of the resonant wavelength against wafer position is shown in Fig 5.16. Although the central part of the wafer was incorrectly calibrated we can observe the high degree of uniformity. For this 3" wafer the epitaxial growth area is $\approx 40.7 cm^2$ which means that >60% of the wafer has a cavity resonance of 856±5nm. From the results for the AFPM reported in [Whitehead *et al*] we can see that a ±2.5nm deviation around the design wavelength still results in a 10dB contrast ratio, adequate for an optical interconnect. Using this criterion gives a usable area of $11.7 cm^2$ or >28% of the wafer surface, provided the centre of the wafer is calibrated accordingly. This yield could be further increased by post growth tailoring of the excitonic wavelength by such means as impurity free vacancy diffusion [Ghisoni *et al*], in which the absorption peak can be matched to the existing resonant cavity wavelength.

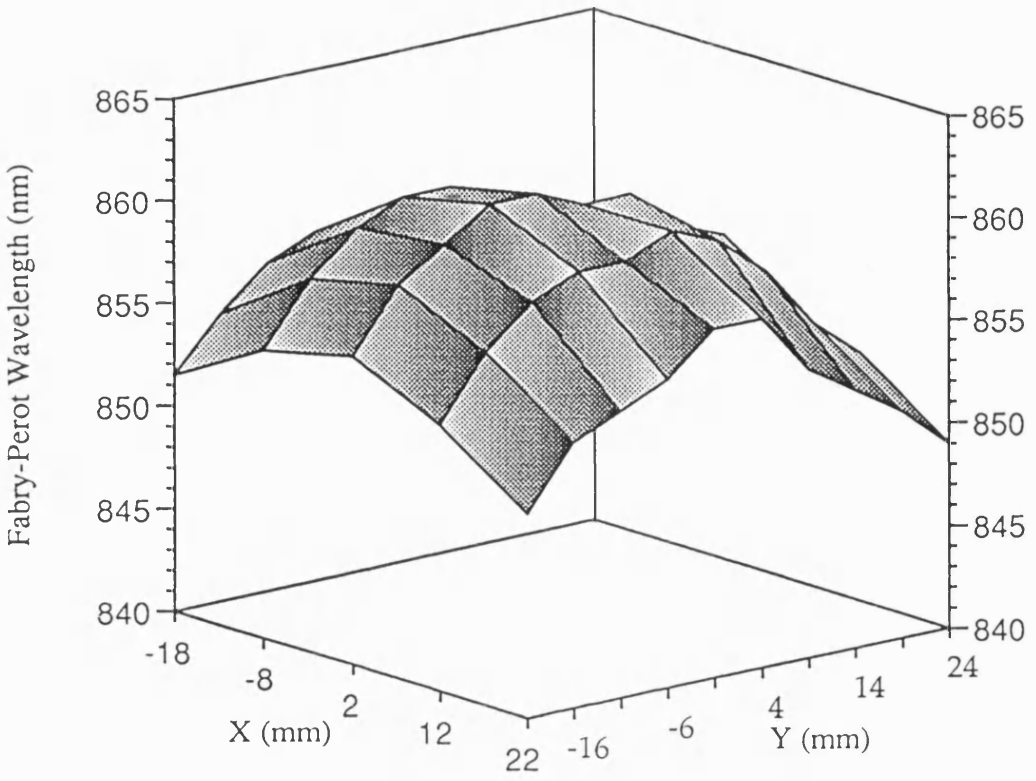


Figure 5.16 *3-D plot of the Fabry-Perot resonance wavelength over the surface of a microresonator modulator grown by MBE on a Si substrate, showing the high uniformity across the wafer. For a 3" wafer >60% of the wafer area had a cavity resonance of 856nm±5.*

5.4.2.2 MOCVD Grown Modulator Structures

It was possible to model a resonant modulator structure by using a program that allowed entry of the measured absorption data from the 95Å MQW grown by MOCVD on silicon (CB306) reported in Chapter 4. The front reflectivity was defined by the air-semiconductor interface, while the back reflectivity was derived from the 96% measured for the MOCVD-grown GaAs on Si reflector stack (QT105/QT145) described in *Section 5.3.2.1*. The model showed that for the measured changes in absorption with applied field, a maximum reflection change of 40%, and a contrast ratio of 10dB, could be achieved with an applied bias of 5.7V. A plot of the calculated reflection spectra for 0V and 5.7V is shown in Fig 5.17. We can now compare the theoretical results with those achieved for modulator structures grown by MOCVD on silicon.

change of 40%, and a contrast ratio of 10dB, could be achieved with an applied bias of 5.7V. A plot of the calculated reflection spectra for 0V and 5.7V is shown in Fig 5.17. We can now compare the theoretical results with those achieved for modulator structures grown by MOCVD on silicon.

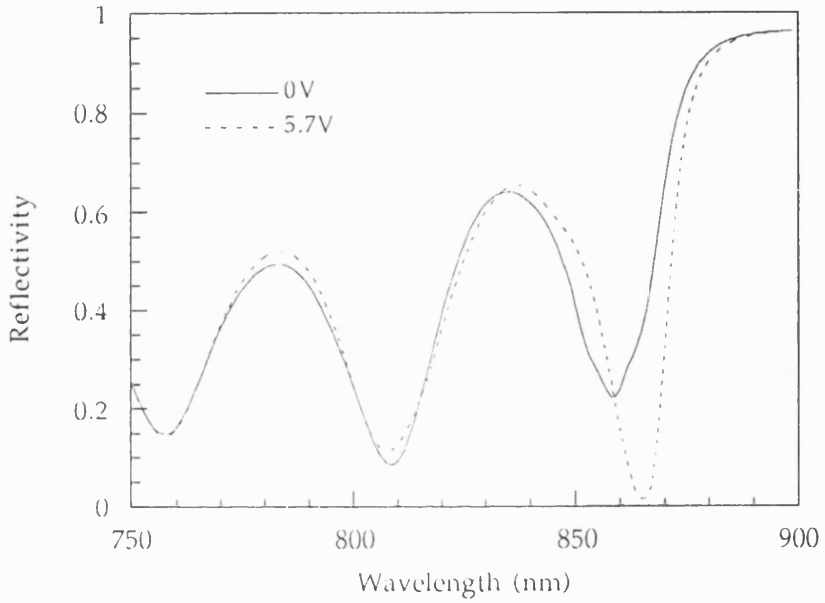


Figure 5.17 *Modelled reflectivity spectra for a GaAs on Si AFPM. The model allowed entry of the measured electro-absorption spectra for a 95Å MQW grown on Si (CB306). The stack reflectivity was derived from that measured for a 15 period stack grown on Si (QT105/145).*

The first AFPM structure grown on silicon by MOCVD was QT183 (see Table 5.1), which used a 95Å MQW region and a 15 period reflector stack. Normalized photocurrent spectra are plotted in Fig 5.18. The resonance is slightly too close to the excitonic peak at zero bias, so that the excitonic peak and the Fabry-Perot resonance cannot be clearly resolved. The latter is seen as a shoulder to the long wavelength side of the excitonic peak. Nevertheless, as a bias is applied the exciton can be seen to shift into the resonance, resulting in an increase in the peak signal. The maximum is reached for 6V, after which the exciton moves through to the long wavelength side of the resonance, and the peak signal falls. Although the normalized photocurrent spectra are shown here, the unnormalized plots showed that these devices had good quantum efficiency. An increase of

only 1.8x was observed in the short wavelength photocurrent level when the bias was increased from 0V to 8V, with saturation occurring at 8V. The corresponding reflection spectra are plotted in Fig 5.19. The closeness of the resonance to the excitonic peak at zero bias results in greater absorption, and thus lower reflectivity, at the resonant wavelength.

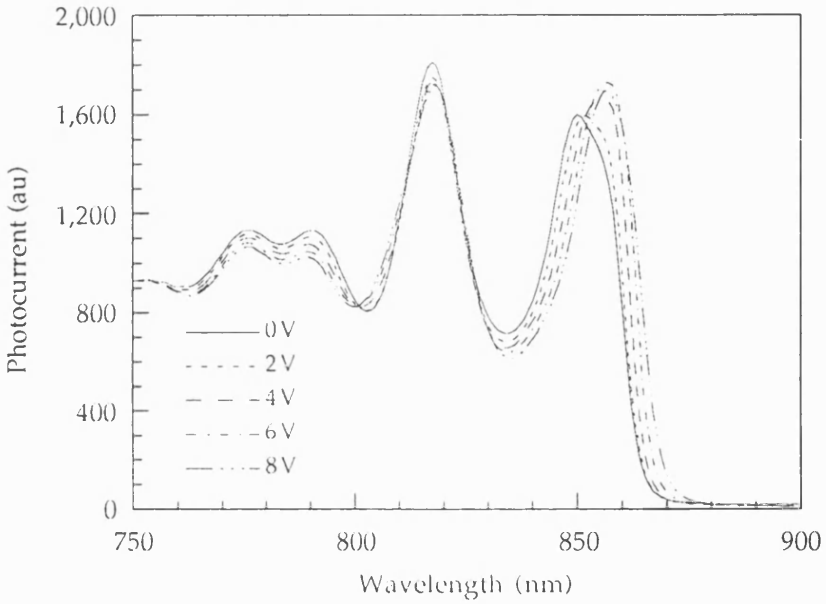


Figure 5.18 *Normalized photocurrent spectra for the QT183 GaAs on Si reflection modulator grown by MOCVD. The Fabry-Perot resonance is slightly too close to the exciton peak at 0V, so that the two cannot be clearly resolved.*

Conversely, the close proximity of the resonance to the resonance does, usefully, result in a lower operating voltage, in this case of 5V. Using the data from Fig 5.19, the contrast and reflection change induced by a 5V signal across the device are plotted in Fig 5.20. A contrast ratio of 7.4dB at 858nm was obtained, with better than 3dB being maintained over 10nm. A maximum reflection change of 40% was measured at 862nm. Figure 5.20 shows the full spectral dependence of the contrast and reflection changes. The maximum values are close to the predicted values above. A slight reduction is observed due to the closeness of the exciton and Fabry-Perot resonance. The voltage used falls within the operating limits of CMOS

circuits and so opens up the possibility of highly integrated optical interconnects.

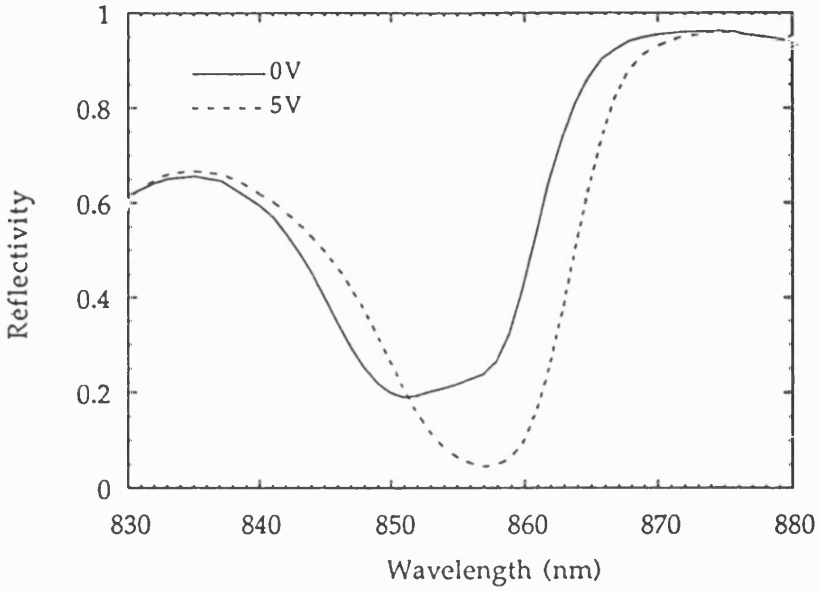


Figure 5.19 *Reflectivity spectra versus wavelength for the QT183 reflection modulator at 0 and 5V applied bias. A maximum reflection change of 40% is achieved at 862nm, and a contrast ratio of 7.4dB at 858nm.*

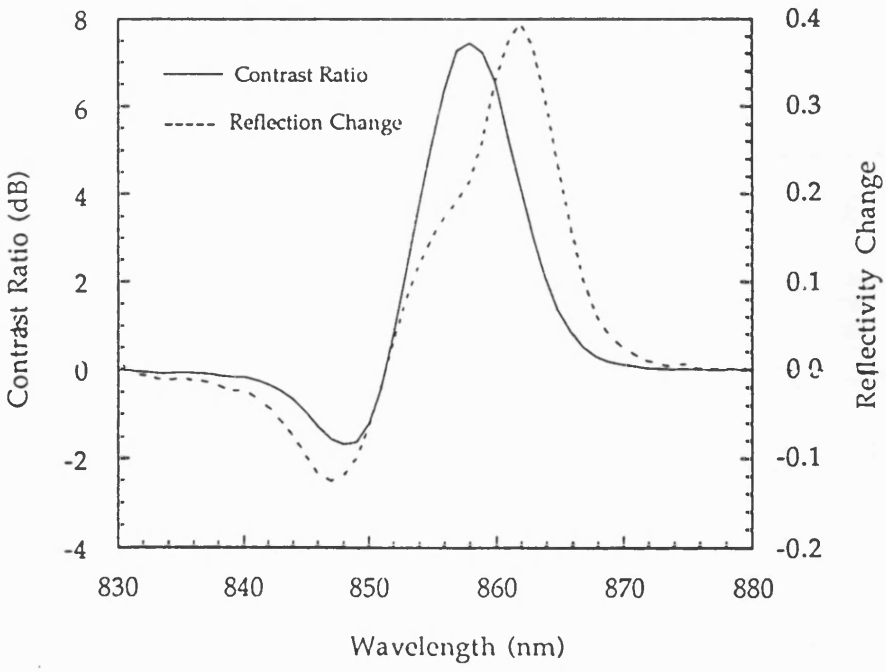


Figure 5.20 *Reflection change versus wavelength and contrast ratio versus wavelength at 5V applied bias for the QT183 reflection modulator. Better than 3dB modulation is maintained over 10nm.*

Because the resonance wavelength, at ≈857nm, was shorter than the design wavelength of 862nm, it was decided to compensate for this by cooling the device slightly, so as to increase the separation between the exciton peak and the resonance. The absorption at the resonance wavelength is thus reduced, increasing the reflectivity in the unbiased state and lowering the insertion loss. The reflectivity at the resonance wavelength increased form 25% to 44% as the temperature was reduced from 22°C to 10°C. The latter reflectivity value is close to that measured on GaAs substrates and is an indication of the high material quality.

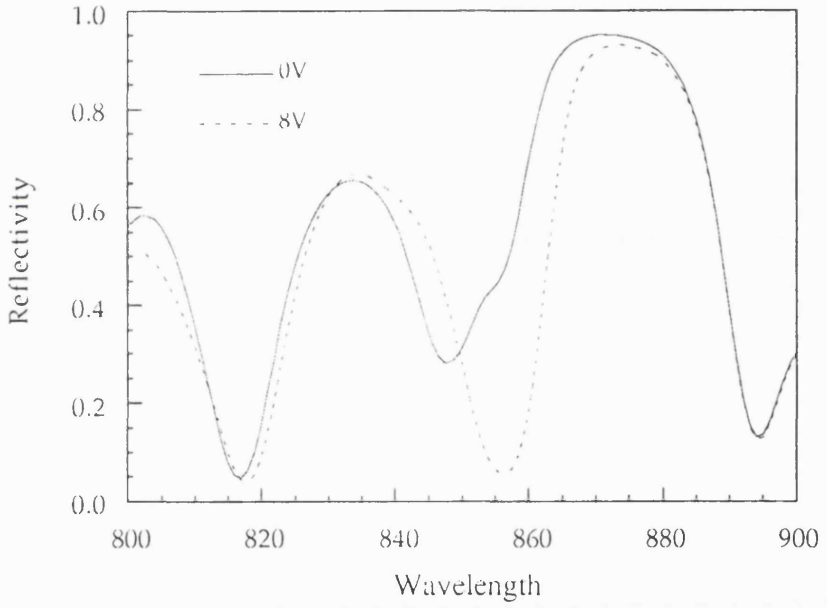


Figure 5.21 *Reflectivity spectra versus wavelength for the QT183 reflection modulator at 0 and 8V applied bias, measured at 10°C. A maximum reflection change of 51% is achieved at 859nm, and a contrast ratio of 9.3dB at 856nm.*

The reflectivity spectra for the cooled device is plotted in Fig 5.21 for 0V and 8V, at which bias maximum modulation occurred. Figure 5.22 shows both the reflectivity change and the contrast ratio plotted against the wavelength for the device operated at 8V bias. The maximum reflection change is 51% which occurs at 859nm and corresponds to an insertion loss of 1.9dB. Greater than 40% reflection change is maintained over a 6nm bandwidth. The contrast ratio reaches a maximum of 9.3dB at 856nm for an insertion loss of 3.2dB; again the relative insensitivity to input wavelength is shown by >6dB contrast being achieved over a 6nm

bandwidth. These reflection changes are comparable to those achieved on GaAs substrates, although the very high levels of contrast (>20dB) have not been equalled. This is due to the reflectivity not falling completely to zero at the Fabry-Perot wavelength when a bias is applied, the minimum being 5.5%.

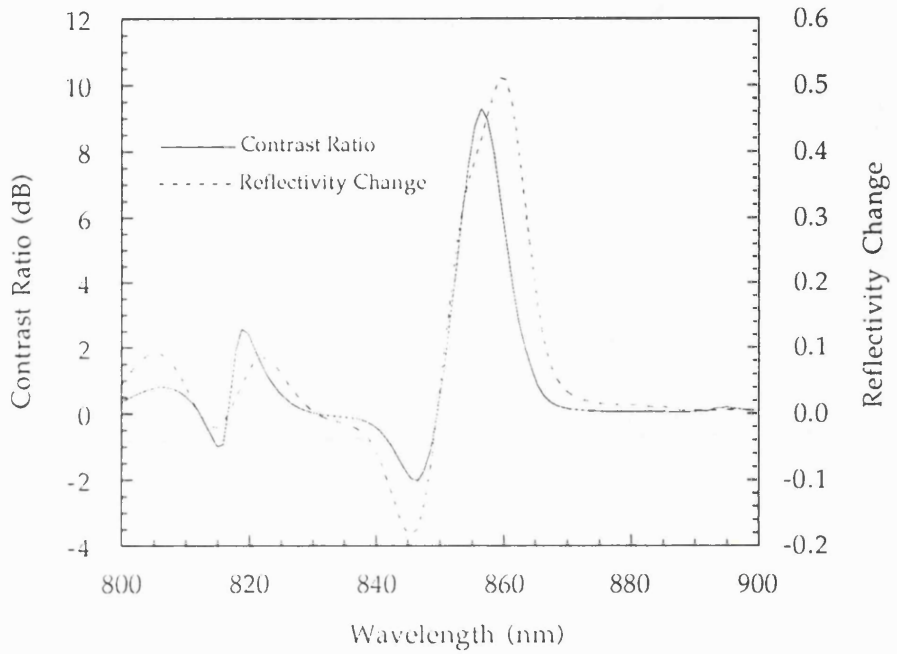


Figure 5.22 *Change in reflectivity and contrast ratio against wavelength for the QT183 reflection modulator at 8V reverse bias, measured at 10°C.*

A regrowth of the QT183 modulator was attempted in order to obtain a structure with the correct Fabry-Perot resonance wavelength. Unfortunately, the regrowth, QT253, was itself miscalibrated, resulting in the Fabry-Perot wavelength being at too long a wavelength (≈878nm) to make useful devices. At this distance from the exciton peak it is not possible to obtain the required change in electroabsorption. It was therefore not possible to improve on the performance of QT183.

5.4.2.3 *Summary*

High performance optical modulators were fabricated on silicon substrates. These show a 51% reflection change, and a maximum contrast ratio of 9.3dB, both at 8V. Alternatively, operation at 5V gives a 40% reflection change and a 7.4dB contrast ratio. To the best of my knowledge these figures represent the best performance reported for a GaAs on Si modulator. They were obtained despite miscalibration in growth resulting in a non-ideal separation between the Fabry-Perot resonance and the exciton peak. Calculations using experimentally derived electroabsorption and reflectivity measurements indicate that a 40% reflection change and a 10dB contrast ratio should be achievable for 5.7V bias. In order to match the performance of modulators grown on GaAs it will be necessary to further improve the reflectivities of the devices. A slight surface texture is lowering the reflectivity of the stacks and causing some scattering. For this reason complete destructive interference does not occur for the off-state of the modulator, thereby leaving a small residual reflection which restricts the available contrast ratio.

Conclusion

CONCLUSION

In Chapter 1 we introduced the motivations for the integration of a GaAs on Si optical modulator. It was shown that optics could be used to enhance electronics, for example by the optical interconnection of high speed electronic circuits. An attractive interface element for this purpose would be a high speed, low voltage optical modulator. Such devices have been demonstrated on GaAs substrates using the Asymmetric Fabry-Perot modulator (AFPM) structure operated in reflection mode, and have shown reflection changes of greater than 40% with contrast ratios of 100:1 at an operating voltage of 8V. A similar structure grown on silicon would allow direct integration with existing high density, reliable and cheap electronics.

Growth quality of GaAs on silicon has been the subject of much recent research but is still limited by the lattice mismatch and difference in linear thermal coefficient of expansion between the two materials. This introduces strain into the epitaxially grown layer. The effects of this on the properties of the MQW were discussed in Chapter 2. The dominant change is a strain splitting of the *hh* and *lh* to conduction band transitions, which is in the opposite direction to that caused by confinement in the well. The result for a 95Å well is an overlap between the two transitions, with only a single excitonic peak being observed on the photocurrent spectra. The change in splitting with well width was experimentally observed. For a 40Å well width the confinement splitting was found to dominate the strain splitting, resulting in both *lh* and *hh* transitions being observed. The strain was also found to shift the transitions to slightly longer wavelength than would occur for devices grown on GaAs substrates.

An extensive investigation into the material quality of GaAs on Si epitaxial layers, grown by both MBE and MOCVD, was presented in Chapter 3. Analysis by TEM showed both the quantum wells and the quarter-wave reflector stacks to have extremely smooth interfaces. Dislocations were found to be concentrated in the first 2μm of the buffer layer. Of those that penetrated further into the epitaxial layer some were

found to be filtered out by the reflector stacks. Analysis of a number of samples showed that the reflector stacks were, indeed, successful in reducing the dislocation density. A further problem that can occur with thick GaAs structures grown on silicon is microcracking of the epitaxial layer. Growth of *pin* MQW structures was carried out on islands, formed by patterning Si substrates, in an attempt to reduce the microcracking. Photoluminescence measurements showed a marked blue shift of the quantum well emission as island size was decreased. This was consistent with a significant reduction in biaxial tensile strain. A corollary of this was that microcrack densities, of up to 60 per mm in the <110> directions on the plain areas, were reduced by an order of magnitude, or even totally eliminated, on patterned areas. Growth on patterned silicon substrates could therefore be beneficial in terms of improved yield and the realization of the optical interconnection of electronic islands. Conversely, it was found that in thinner device structures there was no discernible relationship between microcrack density and device performance. Examination of the devices by optical beam induced current (OBIC) scanning optical microscopy revealed that the microcracks did indeed have little impact on the device performance. This technique reveals which defects or groups of dislocations affect the performance of devices. It was found that dislocations, not microcracks, were of most importance, and that these were evenly distributed across the devices under test, with clustering only occurring at dimensions of 2-3μm. This indicated that modulators could be reduced in size to that required for optical interconnects without resulting in large variability of performance. SEM and optical microscopy revealed that some surface texture was apparent even on the best samples, and that this was responsible for some scattering of the reflected light.

MQW *pin* diode test structures were examined in Chapter 4 and compared to the performance of similar devices grown on GaAs. In addition to the effects of strain described above it was found that the excitonic absorption, although distinctly different from that observed on GaAs substrates, was high enough to permit good device performance. The quantum confined Stark shift did not appear to be strongly influenced by the different substrate. The design and performance of reflector stacks was reported in Chapter 5. A maximum reflectivity of 96% was recorded, slightly lower than that expected on GaAs, due to a slight texture on the

mirror surface. In Chapter 5 we also demonstrated that high performance modulators could be fabricated on Si substrates. These show a 51% reflection change, and a maximum contrast ratio of 9.3dB, both at 8V. Alternatively 40% reflection change and a 7.4dB contrast ratio could be achieved at 5V. To the best of my knowledge these were the best results recorded for a GaAs on Si modulator. The issue of growth on Si VLSI still needs further attention because growth temperatures of up to 700°C are incompatible with silicon processing. However, recent results achieved by, for example, [Nozawa and Horikoshi] on low temperature growth may be used to fabricate modulators and are encouraging for full integration.

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