OPTICALLY CONTROLLED ANALOGUE TO DIGITAL CONVERTERS

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for the degree of Doctor of Philosophy

Richard Mason

Department of Electronic and Electrical Engineering
University College
Gower Street
LONDON

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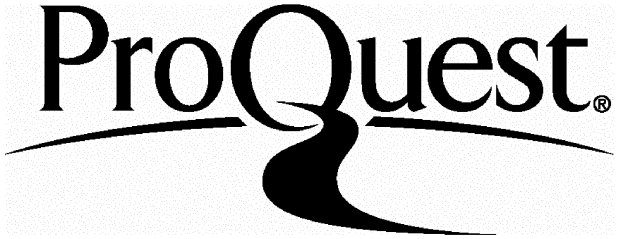

ABSTRACT

This thesis is concerned with the design of analogue to digital converters (ADCs) with high sample rates (in excess of 2Gsample/s) and moderate to high resolution (at least 8-bits). This goal is beyond the capability of current electronic technology, due principally to problems caused by clock timing jitter. To overcome this problem, optoelectronic techniques are examined, which can utilise the inherent low jitter available from modern laser sources and optical clock distribution schemes.

A novel optoelectronic technique is proposed which uses an interleaved ADC architecture and optical clock distribution to obtain the required performance. A key component in this system is an optically triggered sample and hold circuit (OS/H). A range of fully integrated OS/Hs have been fabricated using a standard GaAs MESFET technology. These circuits combine both electronic and optical components on a common substrate and demonstrate the use of a standard electronic technology for optoelectronic applications. Measurements on these circuits have demonstrated their effectiveness for this application.

A discussion of the effects of timing errors (both static and dynamic) in interleaved sampling systems leads to the description of a technique for correcting the effects of clock skew. The implementation of this is very straightforward, involving only the adjustment of DC bias voltages.

The system has been designed so that it can employ current optoelectronic integration technology, and in particular the clock distribution and delay can be realised using integrated optical waveguides.

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ACKNOWLEDGEMENTS

I have heard it said that doing a PhD involves fumbling around in the dark for much of the time, eventually seeing the light just when you think there is no hope. In doing an optics project this has been more true for me than most. The hours spent alone in a darkened laboratory could have made my PhD a very lonely experience. I consider myself very fortunate, then, to have met and worked with so many people who have helped make my PhD so enjoyable.

First, I would like to thank Dr John Taylor for introducing me to this project and for supporting me throughout the difficult times. The transition from a spoon-fed degree to self directed research is very difficult, but John helped me steer this rocky course relatively smoothly. He also taught me the value of communicating ideas — I only hope that a little of his talent has rubbed-off on me. I would also like to thank Professor Gareth Parry for helping me through the occasional moments of self doubt that I had, and for being incredibly supportive throughout my project. In spite of his very busy schedule Gareth remains one of the most approachable and helpful people one could wish to meet.

Reflecting on my time at UCL my overwhelming memories are of the people I have met and worked with. Pask Visocchi was the first person to make the effort to talk to me when I arrived, and he has been talking ever since! With his characteristic unbounded generosity, Pask would leave aside anything if he thought he could be of assistance. It was Pask who I turned to for advice more than anyone else. Hassan Shaffeeu and Dave Grant were also there from the beginning, and together with Pask we developed a camaraderie that helped make the bad times good and the good times unforgettable. The Sun Inn will always have a special place in my heart.

Of course there are many other people I must thank, including Jorge, Mohan, Dave and everyone else in room 621. I feel privileged to have been able to call these people my friends, and look forward to many years of 621 Club reunions.

Life as a PhD student isn't all work and no play and so my friends outside of UCL have been very important in making the last few years so enjoyable. Derk and Martin have managed to live with me for many years without complaining,

and have shown me some of the joys an exuberant lifestyle can bring. I hope that now this thesis is finished I will be able to catch up on all the visits to the pub I have had to miss. Simon and Dave have also been very good friends and I often reflect on the good times we enjoyed in Acton and on our many sojourns to drinking establishments.

On a sunny day in 1985 I arrived in London from the wilds of the North to start my first degree. That was almost nine years ago, and since that time I have been almost totally reliant on my parents for their support. This extends way beyond the financial support I have received (although without this, things would have been practically impossible) to the enormous encouragement they have given me throughout the whole of these many years. This was probably the major factor in enabling me to pursue my studies to completion.

Finally, saving the most important until last, I would like to thank Lola. Her constant nagging has been a major driving force behind the completion of this thesis.

CHAPTER 1

INTRODUCTION

1.1 GENERAL INTRODUCTION

Modern signal processing and instrumentation systems require increasingly high-speed sampling and analogue to digital conversion. For example, we would like to build oscilloscopes which can accurately record transient events generated by high speed electronic circuits. The gate delays of advanced technologies are typically around 100ps [1], so capture of these transients requires sample rates in excess of 20Gs/s. Similarly, the 10Gb/s communication system is fast becoming a reality [2], and so diagnostic equipment of similar or higher speed is in great demand. In the field of optics, sub-picosecond pulses are common (Eg. [3]), ensuring that ever higher-speed instrumentation will readily find applications. Signal processing applications in fields such as wide-band radar also continue to demand higher sample rates, and finally there is a constant demand for higher speed data conversion for military requirements [4].

Accurate, high speed analogue to digital converters (ADCs) are therefore fundamental components of modern, integrated signal processing systems and high-speed measurement and instrumentation systems. In particular, there is a demand for high-resolution (> 8-bits) ADCs with analogue bandwidths and sample rates in the gigahertz region. The achievement of these high sample rates using all-electronic means has proven to be very difficult.

One of the main problems facing designers of high speed sampling systems is that of accurately timing different parts of the system. Achieving appropriate clock phasing without timing jitter is often the single most difficult obstacle to attaining theoretical speed limitations. This problem arises primarily because of the extreme difficulty of impedance matching metallic interconnections at very high speeds as circuit complexity increases. Impedance mismatches at splits, bends and terminations result in high frequency reflections causing loss of pulse definition and therefore reduced timing accuracy. Also, transmission

line dispersion further reduces pulse definition and timing accuracy.

Optics, on the other hand, may offer new solutions to these very serious problems. By replacing the metallic interconnects with optical waveguides or free space optics, the problems of impedance mismatch and dispersion are eliminated [5]. Further advantages include the fact that modern mode-locked laser diodes produce ultra stable, ultra high-power pulses which can serve as an accurate clock source, and that optics has a much greater potential for connecting to the interior of a chip, simplifying pin-out problems. Hence one can see that optics potentially offers jitter-free interconnects with very large fan-out and complex interconnectivity.

This project is a preliminary investigation of the practicalities of using optical clock distribution for high-speed sampled data applications, particularly high speed, high resolution A/D conversion.

1.2 BACKGROUND TO ADCS AND SAMPLE AND HOLD CIRCUITS

The overall field of data conversion has sprung from two distinct sources. Starting in the late 1930s, interest developed in coding and decoding techniques for pulse code modulation (PCM) primarily for telephone communication. This exploits the noise immunity and lack of signal degradation inherent in digital transmission systems. Later, in the 1950s, the advent of digital computers provided a means for storing and manipulating data that was far superior to analogue techniques. By converting the analogue signals produced by natural phenomena into a digital format, signals can be processed using the powerful techniques of computing and digital electronics. This type of data conversion is employed extensively in military and instrumentation applications. Today, practically all communications, signal processing and increasing amounts of instrumentation are performed in the digital domain, with the analogue domain being used primarily as an interface to the outside world. The conversion from analogue to digital, and vice versa, is of crucial importance in a mixed signal system. Once in the digital domain a signal should suffer no further corruption, and therefore the accuracy of the data conversion will limit the overall system [6,7].

Analogue to digital and digital to analogue converters (DACs) translate

between the analogue signals of the real world and the artificial signal required or provided by digital control and computation circuits. They fulfil, therefore, a very important function in analogue control systems. In many analogue control systems using digital circuitry, the ADCs and DACs are the weakest link. Their accuracy and speed of operation limits the overall performance, and their complexity determines the overall size, weight and cost. Consequently, ADCs and DACs are often the bottleneck in applying digital control and computation to analogue control systems.

The performance of ADCs is steadily increasing with improvements in technology. Fig. 1.1 shows the performance of state of the art high-performance monolithic ADCs built in a range of technologies and using a variety of conversion techniques. It is clear from this figure that, for a given technology, there is a simple relationship between resolution and speed. Improvements in

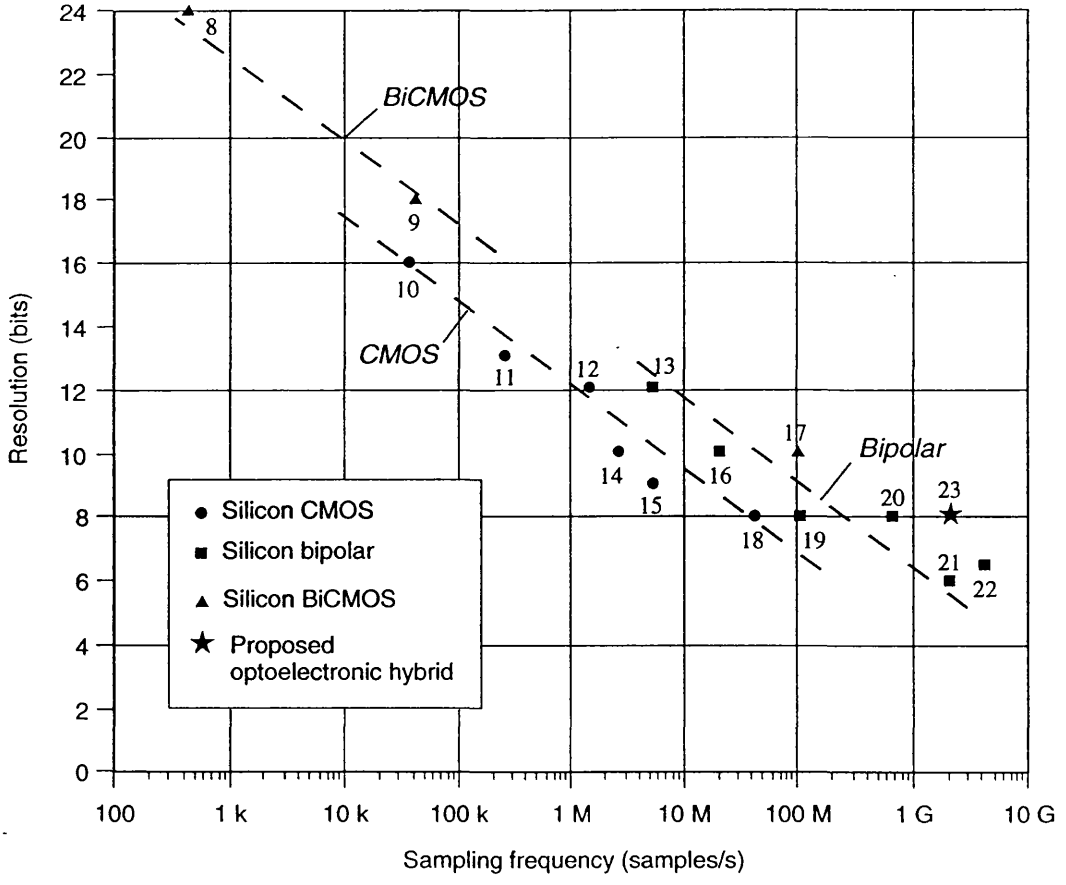


Fig 1.1 Comparison of high-performance ADCs in terms of resolution versus sampling frequency, for various technologies. Ref. [23] shows the performance which should be attainable from the proposed hybrid optoelectronic A/D converter.

technology drive the limit forward, but the trade-off remains. A number of techniques can be used to achieve A/D conversion, each having different aims, such as high speed, high resolution or low cost. For high performance A/D conversion, the most important techniques include oversampled ADCs, flash conversion and time interleaved conversion.

1.2.1 Flash Conversion

Of the numerous digitising architectures, the *parallel* or *flash* converter is the fastest (Eg. [21]). An n-bit flash converter consists of $(2^n - 1)$ parallel comparators, followed by a digital encoding network. Fig. 1.2 shows a 3-bit parallel A/D converter. The reference voltage of each comparator is provided by the resistor chain, which produces seven equally spaced levels, each of which is applied to the positive terminal of a comparator. The application of an input signal V_{in} will cause the comparators with a reference voltage below V_{in} to produce a low output, and the remaining comparators to produce a high output. The resulting 'thermometer' code is encoded into a binary word by the digital encoding network.

This type of converter digitises an analogue signal in one cycle of a two phase clock. During the first phase period, the analogue input voltage is sampled and applied to the comparator inputs. During the second phase period, the digital encoding network determines the correct output digital word and stores it in a register/buffer. The major bottlenecks for the flash ADC sampling rate are in the comparator speed and the encoder circuit which drives the large capacitance of the metallic output lines. The dominant speed-limiting factor for the comparators is the f_T of the IC fabrication process. To improve encoder speed, the power available to drive the metallic line capacitance must be increased. Clearly this power dissipation cannot be increased indefinitely, so a maximum encoder speed is reached. Furthermore, the analogue bandwidth of the converter is determined primarily by the considerable input capacitance associated with the large number of comparators required for high resolution.

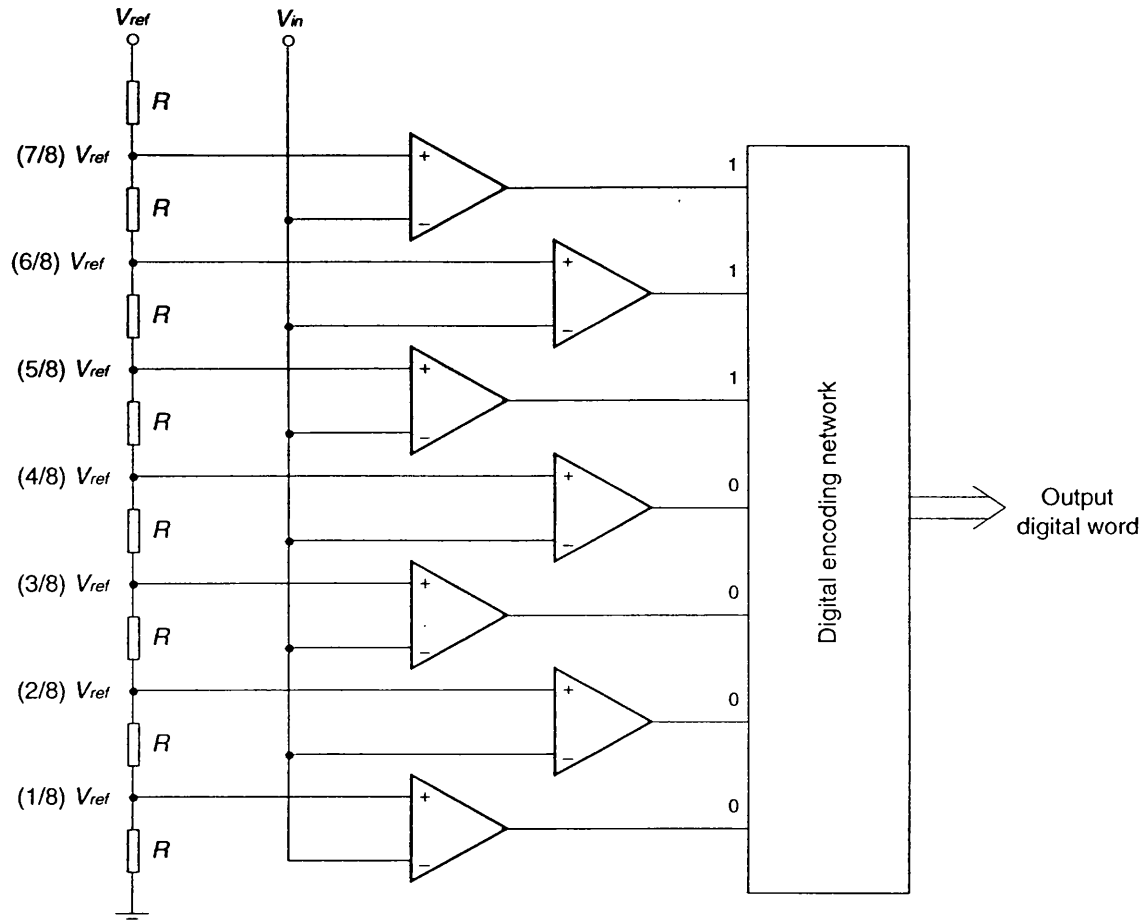


Fig 1.2 A 3-bit parallel A/D converter. This compares the input signal with the chain of reference voltages and produces a digital output in a single clock cycle.

The resolution of a flash converter is determined primarily by the number of comparators. For a resolution above 8-bits, the circuit area and power consumption becomes very large. The effective resolution can be reduced by inaccuracies in the voltage references and comparators, and response time mismatch between the comparators.

The fastest flash converters currently available are built in silicon bipolar ECL technology, and can operate at ~ 650Ms/s with 8-bit resolution [20] or 2Gs/s with 6-bit resolution [21]. The possibility of building flash digitisers in GaAs MESFET technology has been examined [24,25], but this technology was found to be unsuitable due to the frequency dependent drain conductance (see section 2.2) and problems of poor yield.

1.2.2 Interleaved ADCs

Because flash converters digitise in a single clock cycle, these are the fastest type of converters available. To increase the sample rate a number of these converters can be multiplexed in a time-interleaved manner, allowing several conversions to take place within a single clock cycle [22,25,26]. Thus the interleaved architecture offers the potential to increase the sampling rate of an ADC whilst maintaining high resolution. An interleaved ADC is a multi-path system which, in general, consists of N digitisers each clocked at a sample rate of Ss/s. Each ADC is triggered sequentially with a time delay between each path of $1/(N.S)$ s. This gives an overall sample rate of $N.S$ s/s.

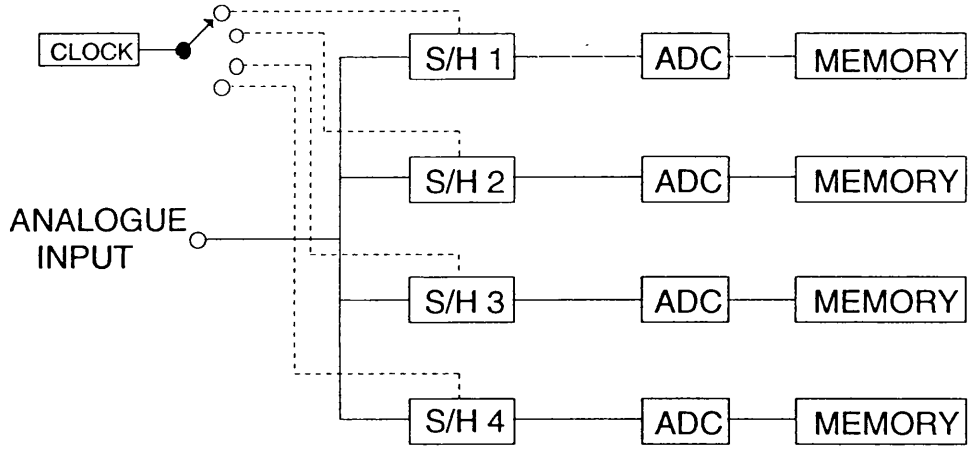


Fig 1.3 Time interleaved analogue to digital converter. The input signal is sampled by each S/H circuit in turn, effectively increasing the sample rate by the number of paths. After the digitised signals are stored, the outputs from the memories can be recombined and manipulated as required.

For example, Fig. 1.3 shows a 4-path system. If each ADC operates at a sample rate of 250Ms/s the overall sample rate will be 1Gs/s. To operate effectively a flash converter needs to be presented with an unchanging signal during the digitising phase. To do this each converter is preceded by a sample and hold (S/H) circuit. In principle the number of paths could be extended indefinitely to produce an ADC of any desired speed. In practice, however, mismatches between the paths, both in time and voltage, will degrade the accuracy and limit performance of this system [25].

(i) Correction for voltage mismatches

With real digitisers, there will be regions in the input voltage range near each code transition where the digitisers will produce different digital codes, even for a dc input voltage. This means that noise of 1 least significant bit (LSB) will be produced when the input is near a transition. This problem can be addressed by offsetting the digitisers in voltage by successive $1/N$-LSB steps [25]. In this way the digitisers are offset in voltage as well as in time. By taking a running average of N adjacent samples, the LSB noise is eliminated.

(ii) High speed clock distribution and the effect of timing errors in the interleaved ADC

The distribution of the master clock in high-speed systems is a long standing problem. Achieving appropriate clock phasing without distortion is often the single most difficult obstacle to attaining theoretical switching speed limits. Design difficulties emerge when typical distances between synchronously clocked circuits become comparable to vt, where v is the speed of signal propagation and t is the clock pulse rise-time. This problem is aggravated by the dispersion caused by metallic interconnects, which increases the clock rise-time [5].

Traditionally, transmission lines are used for the distribution of clock and data signals to separate areas of the system, in which case impedance matching issues become extremely important. Figure 1.4 shows some of the problems encountered in high speed circuit layout topology. Impedance mismatches at bends, splits and terminations give rise to high frequency reflections, and it can be shown that there is an inverse relationship between reflection coefficient and pulse rise-time [27]. Increasing circuit complexity will demand more complex interconnection, proliferating impedance mismatch and high frequency reflections. Further degradation of the signal is caused by transmission line loss, which can typically be around 10dB/m, and by the fact that transmission lines which are fabricated on the dielectric substrates of printed circuit boards or hybrids display a frequency dependent loss above ~100MHz.

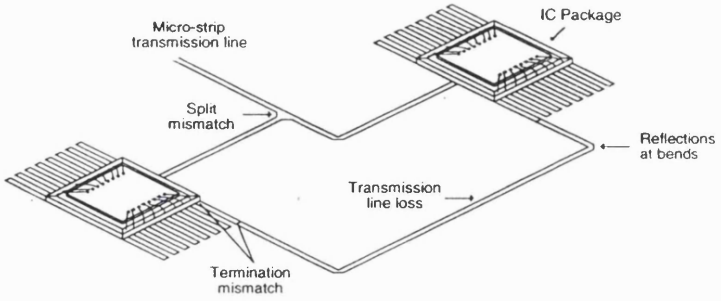


Fig 1.4 Typical issues important in high speed electrical layout topology.

If a source is required to drive multiple terminations, as it is in the case of an interleaved ADC, the limited electronic fan-out capability is a further cause for concern. In this case clock distribution is typically achieved by the driving point-to-point transmission lines with cascaded buffer amplifiers. In a large system this becomes impractical due to physical bulk and excessive power consumption, making it difficult to generate timing edges with an error of less than about 50ps [25].

In the interleaved ADC these problems with clock distribution can severely degrade the accuracy of the conversion. When an alternating input signal is applied to the interleaved converter, the voltage level presented to the flash converters will depend critically on the sampling instant of the S/H circuit. If this is not precise the ADC will digitise an erroneous voltage level causing an effective loss of resolution. In practice it is impossible to generate the S/H clocking instant with arbitrary precision, due to problems associated with described above. The clocking scheme of a typical 4-path system is shown in Fig. 1.5.

The master clock runs at a speed of 4S Hz. This is divided by 4, using counters, to produce the clocks necessary to drive the S/H circuits. When the S/H clocks move from the sample phase to the hold phase, the input signal-level is held, and this is the level that is digitised. As the input signal is continuously changing, the instant of sampling determines the digitised level, so any error in the timing of the sampling instant will cause an error in the digitised level.

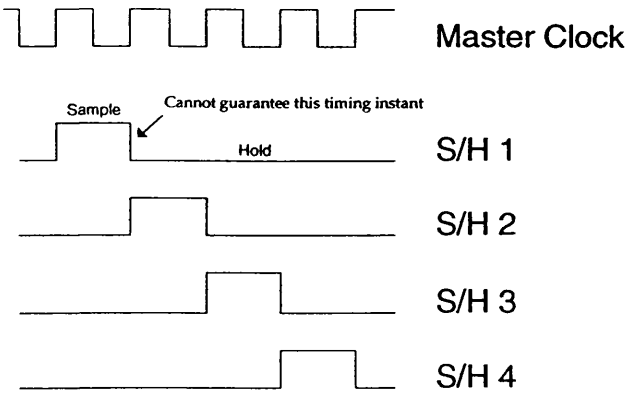


Fig 1.5 Clocking scheme of a 4-path ADC. Electronic counters and delays driven by a single clock provide the timing for each of the paths. This introduces noise which contributes to timing jitter.

To illustrate the difficulties involved, consider the example of a 1Gs/s ADC developed by Hewlett Packard for use in digitising oscilloscopes [25]. In addition to the 1Gs/s sample rate, a resolution of 6-bits and a bandwidth of 1GHz was required. The required accuracy of the sampling instant can easily be calculated. If we take the worst case of a 1GHz sine wave sampled at a zero crossing (Fig. 1.6) we can see how a timing error of 2.5ps can produce an error of 1 LSB.

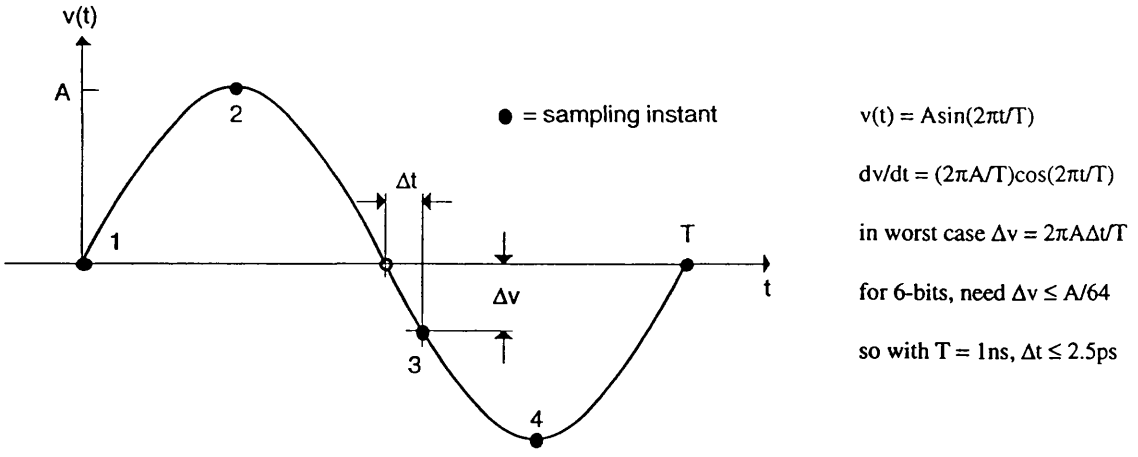


Fig 1.6 Effect of uneven sampling in an interleaved ADC. By sampling at a time Δt away from the correct sampling instant, an error Δv is introduced.

Using all-electronic means it is not possible to generate and distribute the clocks to this degree of accuracy. Hewlett Packard solved the problem by preceding the system with a single S/H implemented in GaAs MESFET

technology, operating at 1Gs/s (Fig 1.7). This relaxes the timing requirement on the second rank S/Hs to about 50ps - an achievable target. The speed of this system is now limited by the first rank S/H circuit: the 1Gs/s sampling rate of this S/H circuit is approaching the limit of current technology.

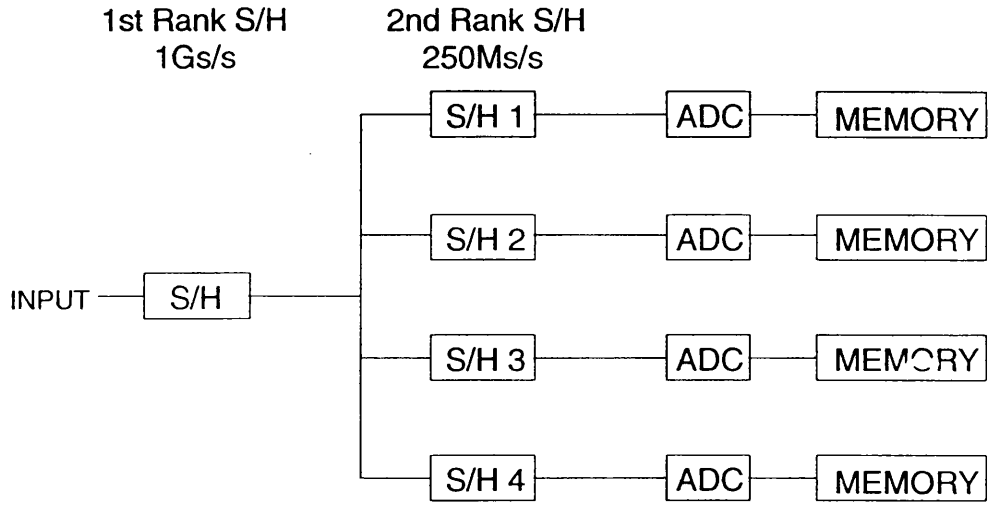


Fig 1.7 Two rank interleaved ADC. The 1st rank S/H circuit relaxes the timing requirements of the 2nd rank S/Hs.

(iii) Sample and filter method

The sample and filter method [22] is a recent development which can be used to relax the *post-sampling* bandwidth requirement of an ADC system. Rather than attempting to charge a hold capacitor to the input voltage and then holding this voltage, the hold capacitor is instead allowed to discharge in a controlled manner through a parallel resistor. The resulting sample pulse has an area or energy which is proportional to the input voltage during the sampling aperture. This pulse is then passed to a high-order Gaussian low-pass filter via a buffer amplifier. Since the area of the pulse at the input to the filter represents the sampled voltage, any point on the output pulse of the filter will be proportional to the sampled voltage. The peak of this pulse, where the slew rate is a minimum, can then be digitized by flash converters. The major advantage of the system is that the ADC input does not have to settle before the next sample is taken, only before the next digitization occurs. This is in contrast to a conventional sample and hold system, which requires the ADC input to settle and be digitized before the next sample is taken. This gives the ADC input

voltage twice as long to settle, and allows the sample rate to be twice the ADC bandwidth. The sample and filter technique does not, however, reduce the timing accuracy with which the sampling instants have to be controlled. It merely allows an ADC with a reduced bandwidth to be used.

In order to increase the sample rate and realise the potential of the interleaved architecture, a clocking scheme which exhibits inherently low timing jitter must be adopted. Optical clock distribution is ideally suited to this problem as such systems can be used to achieve very low timing jitter and clock skew, with high levels of parallelism [28-30]. A proposed design for an optically triggered ADC is described in section 1.5.

1.3 Optical Techniques for A/D Conversion

The need for higher performance ADCs, and the difficulty in achieving this performance using all-electronic means, has been outlined. With the recent dramatic advances in optical techniques, primarily for use in fibre optic telecommunications, it is appropriate to investigate the potential of these to supplement (although not necessarily replace) electronics in A/D (and D/A) converters and other high speed sampling systems. The attractions of optics for this purpose are [76]:

1. High bandwidth (many GHz), leading to picosecond sampling times.
2. Precise timing; mode-locked semiconductor lasers can generate pulse trains with jitter less than 0.1ps [55]. Also, as 1 picosecond corresponds to about 0.2mm in fibre, we can easily manufacture within this tolerance. [31].
3. Little crosstalk between optical signals, and immunity of signals in optical format to electromagnetic interference.
4. Semiconductor lasers are now small and efficient, so power consumption can be low.
5. Optical fibre is increasingly being used to transmit wideband data, so the signal may already be in optical format.

1.3.1 Electro-Optic Diffraction Modulator ADC

The earliest demonstration of electro-optic analogue to digital conversion is that

described Wright *et al* in 1974 [32]. This converter was based on an electro-optic diffraction modulator and incorporated many of the features still evident in more recent work. In this approach the analogue input voltage is applied to an interdigital electrode structure formed on an electro-optic substrate. The voltage applied to the electrode structure produces a spatially periodic variation in refractive index in the crystal, resulting in various diffraction orders in the far-field. The intensities I_m of the various orders are given approximately by

$$I_m = J_m^2(\alpha V) \tag{1.1}$$

where J_m is the mth-order Bessel function of the first kind, V is the applied voltage and α is a constant depending on dimensions and crystal properties. A plot of the 0th and 1st order Bessel functions is shown in Fig. 1.8.

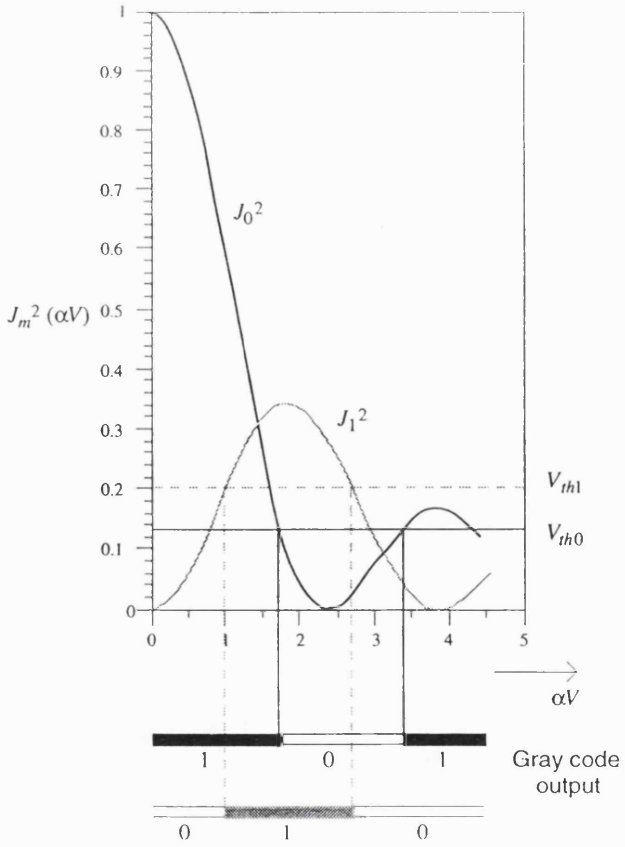


Fig 1.8 Plot of the squared Bessel functions of 0th and 1st order. These are the intensities that are received by the photodetectors at the 0th and 1st order diffraction patterns in the electro-optic diffraction modulator ADC.

The input voltage is applied to the terminals of an electro-optic diffraction modulator and the voltages V_n are derived by detecting particular orders of the diffraction pattern on photodiodes. A digital code can be generated by applying the photodetected voltages to simple threshold detectors. If, for example, voltages derived from the 0th and 1st-order beams are used, and the threshold voltages are set at the levels shown in Fig. 1.8, the digital output will be a 2-bit Gray code representing the input voltage V_{in}. By sensing the sign of V_{in} with a third comparator at the input, a 3-bit code can be generated. The complete system is illustrated in Fig. 1.9.

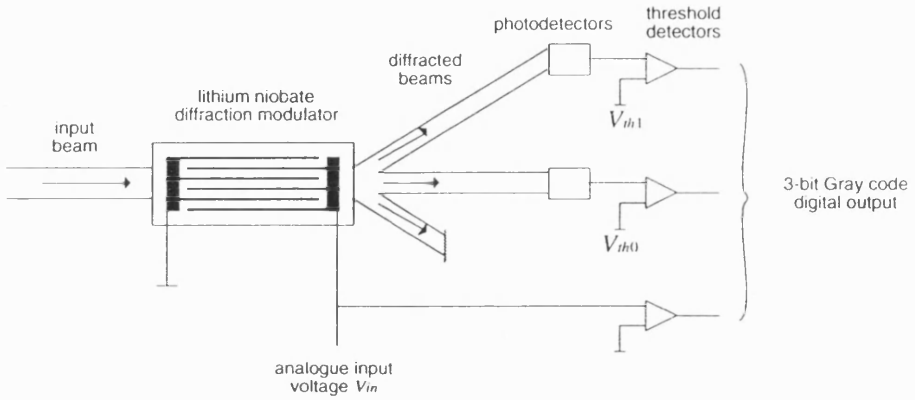


Fig 1.9 Electro-Optic ADC based on a diffraction modulator. By thresholding the output from the photodetectors, a digital representation of the input signal is produced.

This process takes a single clock cycle to convert the input, but unlike a flash converter requires only n comparators for n-bit conversion (rather than $2^n - 1$). A further attraction is the potential for high speed operation. Electro-optic diffraction gratings of this type have been made with analogue bandwidths of ~ 1GHz [33], limited by the electrode capacitance. The main problem with this system is the very limited resolution. A 3-bit digital code can only distinguish eight levels, which is unlikely to be of much practical use. Furthermore, the response is nonlinear, as the Bessel functions do not cross the thresholds at equally spaced input voltage levels.

1.3.2 Mach-Zehnder Interferometric A/D Conversion

The second approach to A/D conversion which uses the electro-optic effect employs an array of integrated optic Mach-Zehnder interferometers [34]. The essence of the design of such a converter is illustrated in Fig. 1.10. The basic element of this converter is the linear Mach-Zehnder interferometer, illustrated in Fig. 1.11, which consists of two back-to-back Y-junctions linked by straight waveguides. The first Y-junction splits the incoming beam into two components which pass along the straight guides and are recombined at the second Y-junction. One of the interferometer arms has electrodes positioned around it, which allows the introduction of a phase shift by means of the electro-optic effect. When the two beams are recombined at the second Y-junction, interference will cause the output intensity to be high if the beams are in phase and low if they are out of phase. In general, the output is periodic with applied voltage, displaying a raised cosine profile. For high-speed applications, both of the arms may have electrodes, which are then driven by complementary signals.

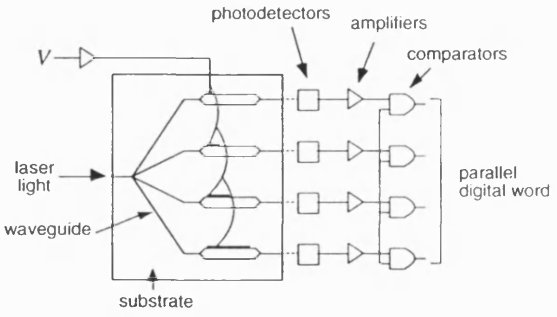


Fig 1.10 Mach-Zehnder optical ADC. This consists of four interferometric modulators with electrodes which increase in length in a binary sequence.

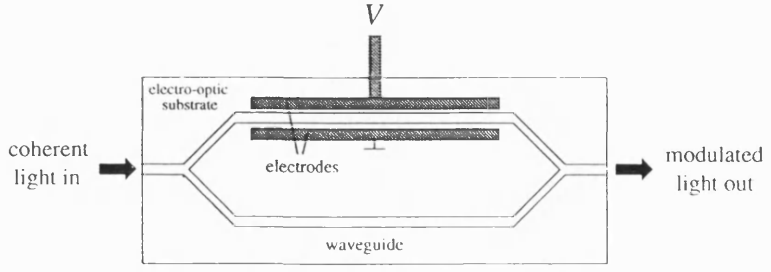


Fig 1.11 Mach-Zehnder interferometric modulator. This is the basic component of the interferometric A/D converter.

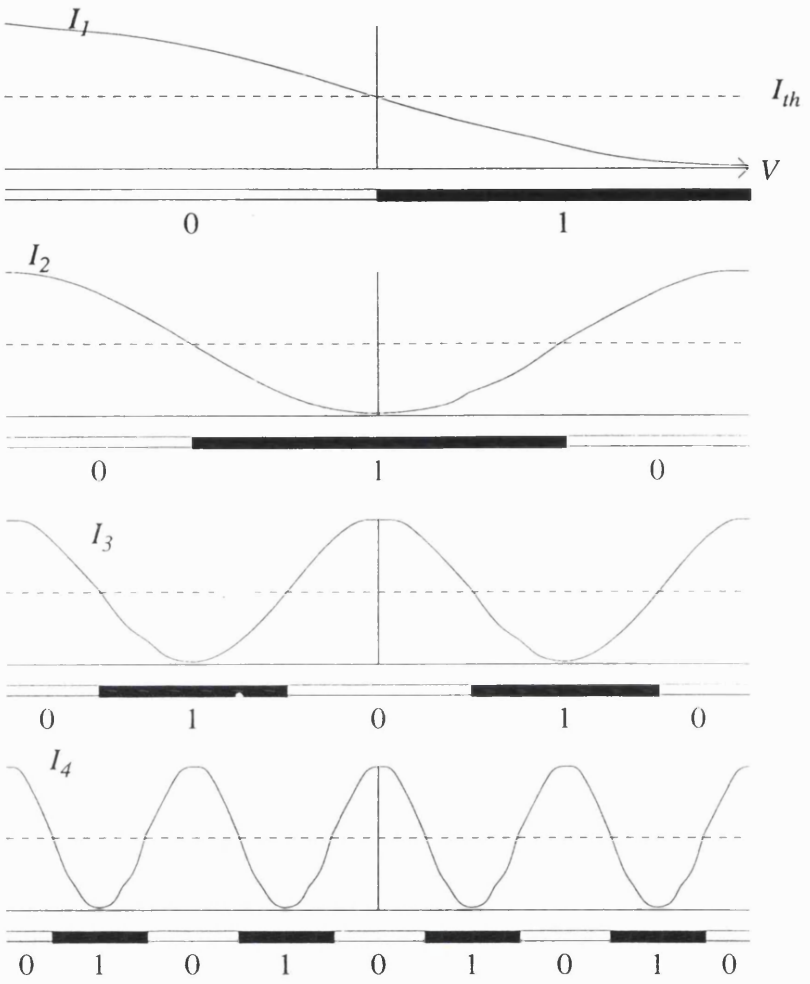


Fig 1.12 Intensity versus voltage plot for a 4-bit Mach-Zehnder ADC with Gray code output.

Because the electro-optic effect is linear, the output of a Mach-Zehnder interferometer depends on both the drive voltage and the electrode length. Thus by doubling the length of an electrode, the voltage change required to produce a complete cycle of the output is halved. To produce an A/D converter, several Mach-Zehnder interferometers are arrayed, and the electrode lengths are varied in a binary sequence, L, $2L$, $4L$, $8L$, and so on. The analogue input voltage, V, is applied simultaneously to the electrodes of each modulator producing outputs which are periodic with input voltage, the period varying in a binary sequence. By placing a photodetector after each interferometer and thresholding at half of the maximum detector output, a binary representation of the analogue input voltage is produced. This can be made to be either a Gray code or offset binary representation by applying an appropriate phase-shifting

bias voltage, the Gray code being preferred as it avoids multiple bit changes for small changes in input voltage. Fig. 1.12 shows the output of the four interferometers configured to produce a Gray code output. If a mode-locked laser is used as the light source, the input will effectively be sampled and held by the ADC.

More recently, a refinement to this device has been introduced by Walker and Bennion [35], who employed channel optical waveguides fabricated in an AlGaAs/GaAs structure. Instead of using an array of Mach-Zehnder modulators they used a single interferometer tapped along its length by a sequence of short directional couplers separated by electrode segments. These couplers are located after 1, 2, and 4 units of accumulated electrode length and the residual light in the interferometer arms is recombined after 8 units. This system performed 4-bit analogue to digital conversion with a bandwidth of 1.2GHz.

This electro-optic ADC can potentially provide several advantages in comparison with conventional fast parallel ADCs such as the flash converter. Perhaps the most important is the very high analogue bandwidth obtainable with this technology. The Mach-Zehnder modulator is a well established device, and has been demonstrated with bandwidths in excess of 25GHz [36]. This is much higher than can readily be achieved using conventional electronics and is the prime motivation for investigating this type of converter. Furthermore, the number of comparators required for n-bit conversion is reduced from $2^n - 1$ to n, substantially reducing the electrical power drain of the unit and simplifying the timing problems which occur in flash converters. The use of a mode-locked laser source could eliminate the need for a S/H circuit and provides a very accurate clock for timing the sampling intervals.

In spite of these attractive features, the Mach-Zehnder ADC has not had a serious impact on the advancement of A/D converters. The major drawback with the system is that it is difficult to increase the resolution beyond about 4-bits. The resolution is limited by the fact that small electrode lengths need high driving voltages. For example, the 1.5mm unit electrode length used in [35] required a driving voltage of 24V. High frequency, high voltage signals are difficult to generate, and so this is approaching the minimum realistic size. Therefore to fabricate an 8-bit ADC, for example, would require the largest

electrodes to be 192mm, very much larger than the maximum substrate size available. A further problem is that the comparators and processing electronics have to operate at the full system sampling rate, limiting ultimate performance.

1.3.3 Electro-Optic Time-Interleaved A/D Conversion

Amongst the more recent proposals for optical A/D conversion is an electro-optic time interleaved ADC [37,38]. This approach is similar to the all-electronic time-interleaved ADC developed by Hewlett-Packard for use in digitizing oscilloscopes [25], but with the time interleaving performed using optical techniques. This converter is based upon the binary tree arrangement of directional couplers commonly used for time division multiplexing (TDM) [39], and is illustrated in Fig. 1.13.

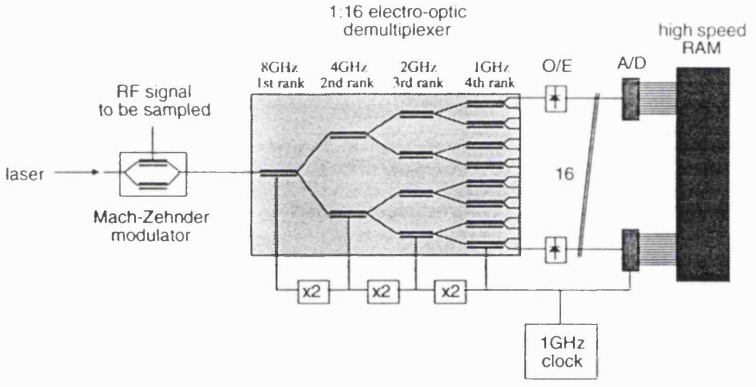


Fig 1.13 Electro-optic ADC based upon an optical time division multiplexer.

The basic building block of an optical multiplexer/demultiplexer is the 1 x 2 directional coupler illustrated in Fig. 1.14, which can couple a single input waveguide into either of two output guides, selected by means of an applied voltage.

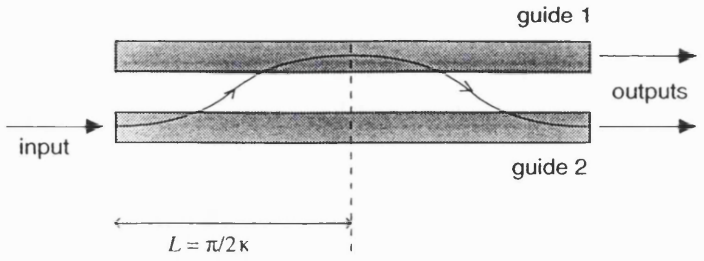


Fig 1.14 Electro-optic directional coupler (electrodes not shown). Light entering guide 2 is progressively transferred to guide 1 as it travels along the guide.

This device consists of two closely spaced parallel waveguides fabricated on a common substrate, with a pair of surface electrodes placed above the guides. When light travels along one waveguide the evanescent field extending outside the waveguide will partially overlap into the second guide, allowing a transfer of optical power. It can be shown [33] that the amount of power interchanged depends upon the length the waveguides and on their relative refractive indices. If the waveguides are identical and the applied field is zero, then 100% cross-over will occur when the length is given by $\pi/2\kappa$, where κ is *coupling coefficient*, a factor which depends on the wavelength of the light, the physical properties of the waveguide and the polarisation. If a voltage is applied the guides become progressively desynchronised, decreasing power transfer, and eventually causing the light to emerge from the original guide without any cross-coupling. The power transfer function of this device is a raised cosine function of the applied voltage. Since the output guide can be selected electronically, the device functions as a two-way switch.

The binary tree demultiplexer use $(n-1)$ switches to provide $1{:}n$ demultiplexing. The first stage is a high speed switch which directs the input to alternate output branches, depending upon the state of the 1st rank clock. Each of these output branches forms the input to a 2nd rank switch which is clocked at half the frequency of the first switch. Subsequent stages of the demultiplexer continue to halve the clock frequency, until the final rank provides n outputs, each one running at a data rate of $1/n$ the original signal. If the 1st rank clock rate is f_s then the demultiplexer effectively samples the input signal at a rate of $2f_s$ samples/sec (the factor of two appears because a sample is made for each

state of the clock) and produces an output at $2f_s/n$ samples/sec. Thus the sample rate is reduced by a factor n, reducing the speed at which the electronic processing is required to operate. The ADC described in [38] uses a 1:16 demultiplexer with the 1st rank driven at 8GHz, providing a sample rate of 16Gs/s, but requiring only 1Gs/s operation from the electronic converters.

This technique is therefore analogous to the electronic time-interleaved ADC [25] in that the final digitising is performed at a much lower rate than the overall sample rate, the difference being that the time interleaving is performed optically rather than electronically. This brings a number of advantages. First, electro-optic modulators and demultiplexers have been demonstrated with bandwidths in excess of 16GHz [39], which means that very high frequency signals can be sampled. The electro-optic ADC described in [38] had a measured analogue bandwidth of 5GHz. The maximum sample rate of this electro-optic ADC is set by the speed of the first rank switch, which can comfortably operate at 16GHz. This compares very favourably to the maximum speed of about 2GHz available from the first rank S/H circuit needed for the electronic interleaved ADC [25].

In spite of the potential performance available from this system, its performance in practice is limited. One significant problem is crosstalk, in which a proportion of the light is delivered to channels other than the desired output. This is influenced by the non-zero extinction ratio of the switches, and by any deviation in the clock from an exact square wave. As the response of the directional coupler switches is a raised cosine, a non-square clock will mean that there is a time when light is delivered to both outputs of the switch. For multi-gigahertz operation it is difficult to generate a square voltage waveform, because of the finite bandwidth of the drive electronics. In practice a sinusoid control voltage must be used, although the non-linear response of the switch tends to make the switch response more square than sinusoidal, resulting in reduced crosstalk.

The most serious drawback, however, is the limited signal to noise ratio. The major sources of noise for the system include shot noise, receiver noise, timing jitter, and laser power fluctuations. These factors limited the signal to noise ratio of [38] to 22dB, which is equivalent to only 3.6-bits resolution. Theoretical considerations in [38,39] calculate the maximum noise limited precision for this

system to be around 5.5-bits, which will limit its suitability for many applications.

1.3.4 Oversampled Optical ADC

A recent development in high-performance electronic analogue to digital conversion is the sigma-delta or oversampling converter [40-44]. Oversampled converters offer a means of exchanging resolution in time for resolution in amplitude in order to avoid the need for complex precision analogue circuits. A typical oversampled converter therefore consists of high speed, low precision components, but produces high resolution conversion at low sampling rates. As many optical components operate at high speed with limited accuracy, this technique appears to be ideally suited to an optical implementation. Although this type of converter has traditionally been used for applications where high precision is required at low sampling rates, the speed advantage of optics should allow high speed conversion at high resolution.

(i) Fundamentals of oversampled A/D conversion

A basic oversampled ADC architecture is shown in Fig. 1.15. This includes an integrator, a course digital estimator with N-bits resolution and a D/A converter, the output of which is subtracted from the input at the summing node. The digital estimate oscillates about the true input with a time average value which is an accurate representation of the input voltage. This output can then be decoded to a higher resolution format at a lower sampling rate by means of a digital filter.

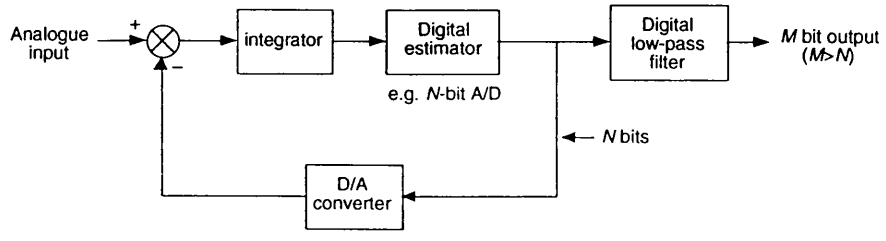


Fig 1.15 A basic oversampled ADC block diagram. This generates a course N bit digital estimate at a very high sampling rate which is then converted to a high resolution representation at a lower sampling rate by the digital low-pass filter.

A case of special interest is that when the $N = 1$. In this case the digital estimator becomes a 1-bit converter – essentially a latched comparator – and the D/A can be removed completely. This 1-bit converter, shown in Fig. 1.16, is known as a *sigma-delta* (Σ–Δ) converter.

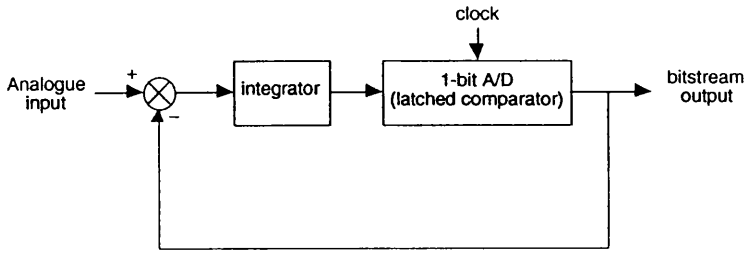


Fig 1.16 1-bit sigma-delta converter. This is a simplified version of the *N*-bit modulator snown in Fig. 1.15.

To understand the operation of this consider the case when the sampling period is T, the slew rate of the integrator is V_{in}/T, and a DC input of 0.75 V_h is applied (where V_h is the voltage of the high logic-level of the comparator). Assuming that the comparator output and integrator output are both initially zero, the input signal will cause the integrator output to rise at a rate 0.75 V_h/T. After a period of T the comparator will sample the integrator output and, as this is above zero, switch to the high state. A voltage V_h will now be subtracted from the input (at the summer), applying a voltage of –0.25 V_h to the integrator. This will cause the integrator output to fall, but now with a reduced slew rate of –0.25 V_h/T. Thus it will take four time intervals for the integrator output to fall below zero and switch the comparator output to the low state.

The cycle now repeats, with a signal of 0.75 V_h again being applied to the integrator. As before, the integrator output will rise at a rate of 0.75 V_h/T, reaching 0.5 V_h after a time T. The comparator then switches, but this time the integrator output will fall below zero after only $3T$, as it started at 0.5 V_h rather than 0.75 V_h. This cycle of $1T$ in the high state and $3T$ in the low state will continue for as long as the input remains at 0.75 V_h. This process is shown in Fig. 1.17.

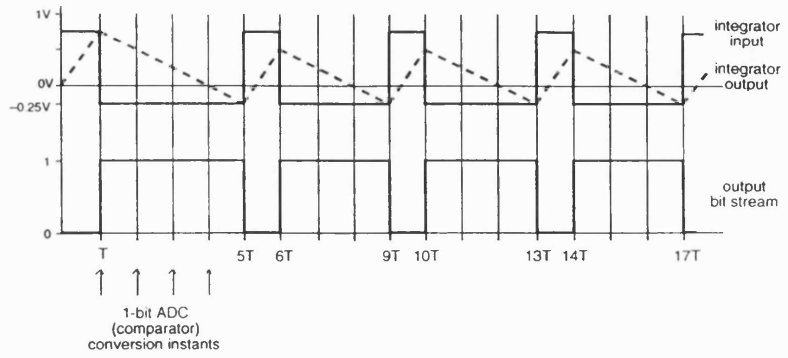


Fig 1.17 Timing diagram of the 1-bit Σ–Δ with a DC input. The 0.75V input produces a bitstream output whose time average value is 0.75V.

Looking at the comparator output over several samples, we see a pulse train whose mean value settles to the level of the input signal. Thus, the analogue input has been converted to a binary bitstream representation. This can now be converted to a standard offset binary representation at a higher resolution, but lower sample rate, by means of a digital low-pass (decimating) filter [45]. To convert an alternating signal, the sampling rate must be much higher than the input signal bandwidth, as several cycles are required before the mean value of the output settles to an accurate representation of the input. The ratio of sample rate to the Nyquist rate of the signal is known as the oversampling rate. The higher the oversampling rate, the more accurately will the mean value represent the input, and therefore the higher the available resolution.

Oversampled A/D converters provide several distinct implementation advantages, which account for their recent popularity. Oversampled converters use low-resolution quantizers that make them more robust against circuit imperfections than other ADC architectures, since circuit errors can be made small compared with the quantizer error. Also, the sampling frequency is large relative to the Nyquist frequency of the sampled signal, which reduces the complexity of the anti-aliasing filter used to bandlimit the input signal. For electronics applications, these converters also lend themselves to small VLSI circuit areas. Because of the need for a large oversampling ratio, the main applications of electronic oversampled A/D converters are in areas such as digital audio, where high resolution is required at relatively low sample rates. Some of the best performance figures of oversampled ADCs include 18-bit resolution at 40kHz [9] and 24-bit conversion at 400Hz [8].

(ii) Optical oversampled A/D conversion

The major drawback of oversampled conversion is that very high oversampling ratios are required for high resolution conversion. This means that the final conversion rate is necessarily much lower than the maximum speed of the individual components. By adopting an optical approach, however, we can capitalise on several advantages of optical technology. First, optical sampling rates exceed electronic sampling rates, making larger oversampling ratios, and therefore higher resolution, possible. Similarly, for a given oversampling ratio the higher optical sampling rate permits the conversion of larger bandwidth input signals. Another advantage associated with optical sampling is the decoupling of the sampled and sampling signals achieved when the sampling is optical and the sampled signal is electronic.

The two essential components in an oversampled converter are a subtraction node and a threshold comparator. The implementation of a subtraction node in optics is relatively simple. By combining two coherent beams with a 180° phase shift between them, destructive interference, and hence subtraction, will take place. An optical threshold comparator is a more complex device, but can successfully be realised by means of a symmetric self electro-optic device (S-SEED) [46]. This device can compare an optical input signal with an optical threshold signal, producing a binary output. Current S-SEEDs have been demonstrated with switching speeds of 33ps, which would allow a sampling rate of about 15Gbit/s [25]. One difficulty of this approach is the requirement for a decimation filter to down-convert the sampling rate. A method of accomplishing this postprocessing function is to convert the optical signal to an electronic signal by means of a photodetector and then to perform the decimation filtering electronically. In this way, we would make use of existing oversampled A/D converter decimation filters. The sampling rate would then be determined by the maximum speed of the decimation filter and would therefore probably not achieve the maximum potential of the optical modulator. As optical digital logic becomes a more mature technology, all-optical decimation filters may be implemented, which would allow the maximum potential of the optical oversampled A/D converter to be realised. A feasibility study of optical oversampled converters has been made [47], which shows that a converters operating at 15Gbit/s sampling rate should be

possible with current optical technology, providing resolutions of 16-bits at 117MHz or 8-bits at 1GHz. These estimations are for the sigma-delta modulator only, and do not take into account the speed limitations introduced by the decimation filter. More recently a practical demonstration of optoelectronic oversampled A/D conversion has been performed, but this achieved a sample rate of only 1kHz [48].

1.4 THE HYBRID APPROACH TO A/D CONVERSION

An alternative approach to the all-optical ADC is to retain an essentially electronic system, but utilise optics in key areas where an improvement can be made upon the electronic performance. Such a hybrid system, which exploits the strengths of both optical and electronic components, has the potential to out-perform any system based upon a single technology. Optics has a number of major advantages over electronics. These include the very stable, high power laser sources which are now available, and the extremely broadband transmission capabilities of guided and free-space optical interconnections.

1.4.1 Modern Laser Sources

The most suitable laser source for hybrid optoelectronic systems is the laser diode. This comprises a semiconductor substrate with a forward-biased *p-n* junction at the surface to provide optical gain through carrier recombination. In the simplest such device the laser cavity is formed by surface and lateral confinement, while the partial end-mirrors are formed by Fresnel reflection at the cleaved end faces. These devices are simple and cheap, but as the cavity length is typically several hundred microns, such lasers are multimoded and relatively unstable. Single mode operation can be achieved by building distributed feedback (DFB) Bragg reflector banks into the cavity [49]. By modulating the drive current, laser diodes can be directly modulated at rates up to 10GHz [50-52], which is a convenient way of imposing analogue or digital data on to the laser output.

One of the key developments that makes optics an attractive technique for sampling applications is the mode locked laser. Mode locked laser diodes are available that can be used as a virtually jitter-free source of high power, short

duration pulses [3,53-54]. Mode locking relies on the fact that the active region of a laser produces radiation with a finite frequency spread or *lineshape*, $\Delta\nu$. From this lineshape, a number of very narrow spectral lines (known as longitudinal modes) are selected by the laser cavity. The frequencies which can resonate in the laser cavity arise because standing wave patterns are set up between the cavity mirrors, which satisfy the condition

$$\upsilon_{mode} = \frac{nc}{2L} \tag{1.2}$$

where υ_{mode} is the modal frequency, c is the speed of light in the cavity, L is the length of the cavity and n is an integer. Therefore the output from a laser will typically be a large number of discrete frequencies separated by

$$\Delta\upsilon_{mode} = \frac{c}{2L} \tag{1.3}$$

The cavity length of a diode laser is typically 200μm to 400μm, so the mode spacing will be ~200GHz to 400GHz. In GaAs lasers the transition linewidth $\Delta\upsilon$ is around $1.5\text{x}10^{13}$Hz, and so there may be around 50 to 100 modes oscillating in the cavity. The relative phases of these modes are unrelated, so the output of the laser is simply the sum of the irradiances of the individual modes. If a number of the modes happen to be in phase at any given time, a peak in the irradiance will occur due to constructive interference. If we now force the various modes to maintain a fixed relative phase to one another, the output will consist of a series of narrow, intense pulses occurring when then peak intensities of the modes coincide. It can be shown [49] that these pulses are separated in time by the cavity round trip time, i.e., $2L/c$, and have a duration $2L/Nc$ ($= 1/\Delta\upsilon$), where N is the number of modes oscillating in the cavity. This is the minimum theoretical duration, and in practice is broadened by effects such as non-ideal mode-locking.

Because of the very small dimensions of diode lasers, the mode spacing is very high and the pulse repetition rate will be in excess of 100GHz. Mode locking a laser at this rate can be complicated, and the resulting pulse train is too fast for many applications. Consequently, most mode locked diode lasers

use external cavities which result in repetition rates of a few hundred MHz to a few GHz [3,54]. Because mode locking concentrates large energies into very narrow pulses, extremely high peak powers are possible. Typical mode locked laser diode performance figures are 70W peak power in 460fs pulses with a repetition rate of 300MHz and absolute rms timing jitter of 400fs [29]. Other systems have achieved absolute rms timing jitter figures as low as 170fs [55]. It is believed that jitter in mode locked lasers is caused by refractive index variations in the cavity due to spontaneous emission, and by phase noise in the driving source generally required to produce mode locking [56].

1.4.2 Optical Clock Distribution

In contrast to the problems encountered in all-electronic schemes, optical clock distribution offers a tremendous advantage (see eg. [5,27,57,58]). The fibre medium is a low loss, low dispersion channel, which has virtually unlimited bandwidth over short distances. The transport of baseband information over a fibre can be thought of as the modulation of a carrier oscillating at approximately 3×10^{14}Hz. With a carrier of this frequency, extremely wide-band signals can be transmitted. By using optical techniques, impedance mismatches are eliminated, and so the most serious reason for failure of electrical interconnects at high frequencies is defeated. Also, the loss of silica fibre is much less than that of metallic interconnects, being around 10^{-3} dB/m at $\lambda = 830$nm falling to 2×10^{-4} dB/m at $\lambda = 1.55\mu$m. Finally, the advent of very high power mode-locked laser diodes has meant that the clock source can be virtually jitter-free, and fan-out can be very high without the difficulties encountered using impedance matched transmission lines [59].

The use of optics as an alternative clock source has been demonstrated with considerable success (eg [30]). One of the most impressive results [29] achieved clock distribution to 1024 ports with a jitter variance of $\sigma < 2$ps, which is an order of magnitude improvement over what can be achieved by conventional electronic means. This system used a combination of 50μm multimode fibres and splitters along with a mode-locked laser diode generating 460fs pulses at a repetition rate of 300MHz. A variety of techniques for making optical interconnects have been proposed, and a brief summary is included here.

(i) Index Guided Interconnections

The use of optical fibres to guide the optical signal is an example of the wider category of index guided interconnections. Using this technique, light is carried from an optical signal source to many sites by means of waveguides such as fibres or integrated optic waveguides [60].

If fibres are chosen as the interconnect technology, then the approach shown in Fig. 1.18 might be used. A single laser source is launched into a fibre and then divided using optical fibre splitters. Each fibre end is carefully located over an optical detector that converts the optical clock into an electrical clock. Alignment of the fibre and detector can be accomplished using micropositioners, and the fibre can be permanently bonded to the detector using UV-hardened epoxy [5]. The difficulties with this approach stem from the alignment requirements of the fibres and from the uniformity requirements of the fibre splitters. The degree of bending of the fibres also needs to be controlled, as this will cause radiation loss which may become severe. The use of fibres, and the requirements regarding allowable degrees of bending, imply that this technology will occupy a three dimensional volume, rather than being purely planar, and this property could be a disadvantage in some applications.

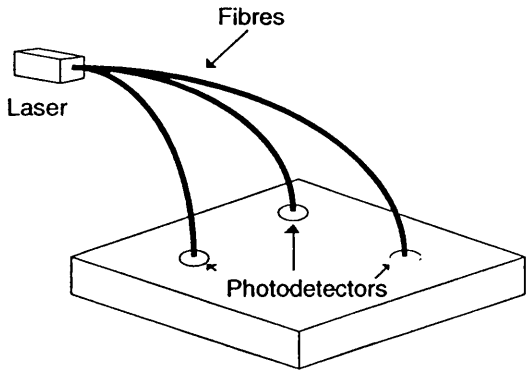


Fig 1.18 Distribution of an optical clock signal by means of fibres.

If integrated optical waveguides are chosen as the interconnect technology, then the geometry might be that shown in Fig. 1.19. The waveguides can be formed using a variety of techniques. For example, waveguides in amorphous materials such as glass, can be formed using r.f. sputtering [5]. Dielectric and polymer waveguides have also been successfully deposited on GaAs substrates [61,62], and epitaxial techniques have been used for the integration of $LiNbO_3$

waveguides with GaAs photodetectors eg [63]. Using this technique one can also fabricate components such as power splitters and delay lines which are necessary for complete optoelectronic integration [33,64,65]. Although the fabrication of this would be more difficult than a fibre based system, there are many advantages including planarity, compactness and stability.

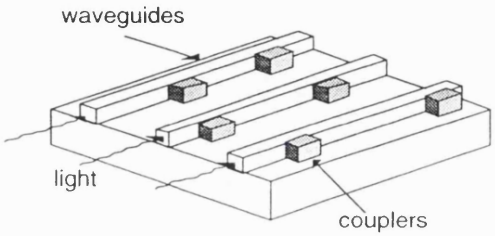


Fig 1.19 Distribution of clock by means of integrated optical waveguides.

(ii) Free Space Interconnections

The free space interconnection technique does not use waveguide structures to guide the light to its destination, but rather free space propagation [66]. Two methods can be used to realise this approach, namely unfocused and focused. Unfocused interconnections would involve distributing the optical clock to all areas of the chip, as illustrated in Fig. 1.20. Detectors integrated in the chip would then receive the clock with identical delays.

The advantage of this technique is that alignment is not critical. So long as the light covers the whole chip, the clock will be distributed correctly. Errors in positioning the lens will have little or no consequence, for example tilting the lens would have no effect upon the plane wave output. Although moving the lens (or the source) in the plane of the chip would tilt the output wave causing different detectors to receive the clock at different times, this would have little effect as the speed of light is very fast, and the tilt angle would be small for any likely displacement. The disadvantages of this technique are that it is inefficient, as only a small fraction of the light falls on the photodetectors, and that the unwanted light may well affect other devices in the chip. This second point could be overcome by adding an opaque mask to the chip.

A more efficient method of free space interconnection involves focusing the light directly onto the detectors using, for example, computer generated

holograms [28,67]. Significant progress has been made in this area; for example, efficient holograms have been generated which distribute light to an 8x8 array of locations with a 125μm pitch [68].

Certain systems, including the interleaved ADC, require accurate delays between clock signals directed to different parts of the circuit. Unlike guided wave interconnects, free space interconnects cannot easily produce these delays.

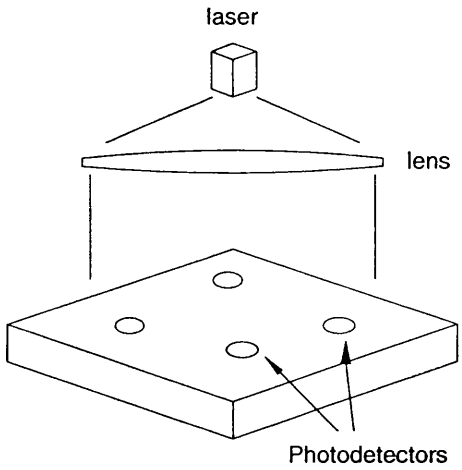


Fig 1.20 Free-space optical clock distribution.

1.5 PROPOSED OPTICALLY TRIGGERED ADC

A block diagram of an optically triggered ADC is shown in Fig. 1.21. In this arrangement the electronic clock is replaced by an optical clock, eg a pulsed laser. This is then distributed by means of waveguides, such as fibres, to the optically triggered S/H circuits. Over the short distances involved, the fibre medium is virtually bandwidth unlimited, and so dispersion and attenuation are insignificant. Thus one of the major sources of jitter found in electronic clock distribution schemes is eliminated.

In addition to the low dispersion, optical clock distribution is advantageous for this application because it avoids the need to use dividing circuits. Rather than dividing a master clock with counters, we simply delay the clock using appropriate fibre lengths. Division of the master clock is another source of timing jitter in the all-electronic system – a consequence of the noise generated by the counters. For a 4-path ADC operating at 1Gs/s, a delay of 1ns is needed

between each path – this can be provided by ≈200mm of fibre.

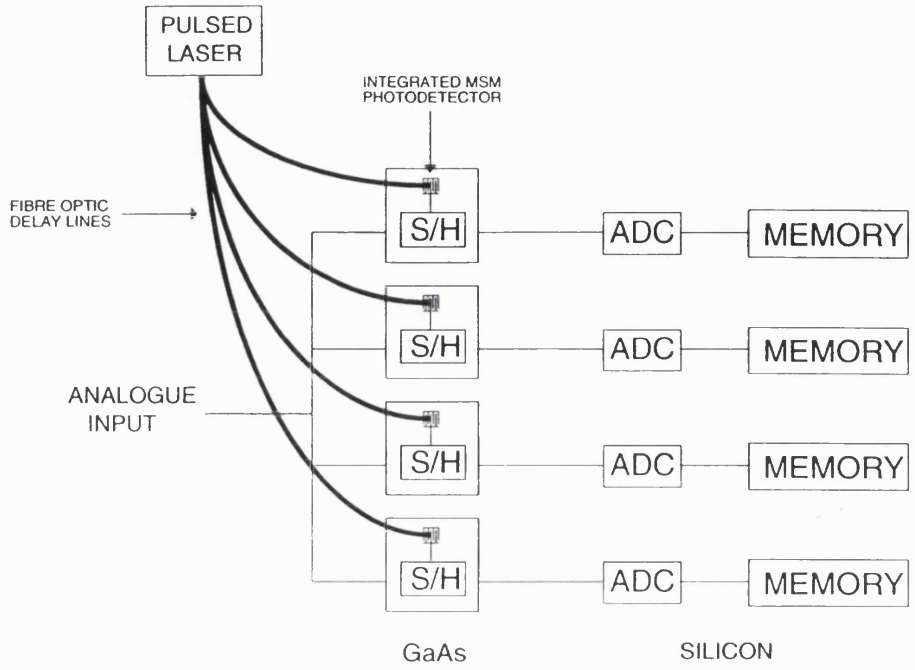


Fig 1.21 Proposed optically triggered ADC. By replacing the electronic clock with an optical clock distribution scheme problems with timing jitter are largely eliminated.

A key component of such a system is an optically triggered sample and hold circuit (OS/H). This component could be realised using a discrete photodetector and conventional electronic circuitry. This, however, would cause problems with stray capacitance and noise. A far more elegant solution is to adopt a fully integrated approach, in which the photodetector and electronic circuitry are fabricated on a common substrate. This approach has been adopted for this project, with a subsidiary aim being to investigate to what extent a standard GaAs MMIC foundry process (the GEC-Marconi F20 process [69]) could be employed in this application. The GaAs OS/H circuits will drive silicon bipolar digitisers, the complete system being mounted on a thin-film hybrid to minimise parasitics.

The optical source is a critical component in such a system. The advantages of the optical distribution will only be effective if the clock itself exhibits very low jitter. Ideally we would use a mode-locked laser as the source, as these can produce trains of pulses with very low relative timing jitter (eg. 170fs reported

in [55]). This technique would, however, complicate the design of the S/H circuits, as the pulses produced are necessarily of ultra-short duration (<500fs). Using such a light source directly would generate an ultra-short OS/H phase (this could either be the sample or the hold phase) that the electronic circuitry would not be able to handle. Techniques for utilising mode locked laser sources are investigated in chapter 8, and demonstrate that the OS/H circuits presented in the following chapters can be used successfully.

Another alternative is to use a CW laser, and modulate this electronically. Electronic pulse generators are available (such as the HP 8131A), which can generate pulses with timing jitter of less than 10ps at 500MHz repetition rates. For this purpose a laser drive circuit which can modulate a 30mW laser diode at >250MHz has been designed (see appendix 1). This circuit will be used for the initial testing of the S/H circuits.

1.6 ORGANISATION OF THESIS

This thesis presents a study of the use optical techniques to enhance the performance of electronic analogue to digital converters and other sampled data applications. This introduction has outlined some of the difficulties involved in realising high performance ADCs and suggests optical techniques which can be used to overcome these difficulties. Chapter 2 describes the relevant physical properties of GaAs which make it particularly suitable for integrated optoelectronic applications. Device models are developed for MESFETs and MSM photodetectors.

A description of general sample and hold architectures is given in chapter 3, and a range of novel optically triggered S/H circuits are described. The difficulties of designing circuits in GaAs are discussed, as well as the problems involved when optical and electronic components are integrated on a common substrate. A complete analysis of these circuits is given, making accurate predictions of their performance.

The implementation of the OS/H circuits is described in chapter 4. This chapter describes the GEC-Marconi F20 foundry process and covers some of the issues involved in high speed analogue IC design. The layout of each chip is described and die photographs are presented. The packaging of the ICs and

PCBs used for testing the circuits is also discussed.

Chapter 5 presents a complete set of simulations and measured results for each circuit. The results from these are discussed and discrepancies between measured results and simulations/analysis are accounted for.

One of the major reasons for developing optically triggered S/H circuits is to take advantage of the very low timing jitter available from mode-locked laser sources. In chapter 6 we investigate the effects of timing jitter in sampled data circuits using numerical simulations and mathematical analysis. A technique for correcting static timing errors in multi-path ADCs is described and used as the basis for simulations of an error corrected ADC using the OS/H circuits.

The demonstration circuits described in earlier chapters use optical fibres to guide light from the laser source to the detectors. Chapter 7 is a review of techniques by which it might be possible to integrate optical waveguides and delays with the optoelectronic substrates, providing much more compact and reliable systems.

Finally, chapter 8 presents overall conclusions to the project, and suggests future directions and further work.

1.7 STATEMENT OF ORIGINALITY

I consider that the following are the most significant results of the research presented in this thesis. These results are, to the best of my knowledge, original. Where appropriate I have also indicated the publications which have arisen as a direct consequence of this work.

In chapter 2

The development of the HSPICE MESFET models from S-Parameter measurements is original. This modelling is described in:

[70] P. Visocchi, J. Taylor, R. Mason, A. Betts and D. Haigh, "Design and evaluation of a high-precision, fully tunable OTA-C bandpass filter implemented in GaAs MESFET technology," accepted for publication in *IEEE J. Solid-State Circuits.*

[71] P. Visocchi, J. Taylor, R. Mason, A. Betts and D. Haigh, "A high-precision, fully tunable OTA-C second order bandpass filter implemented in GaAs

MESFET technology," *IEEE Int. Symposium on Circuits and Systems (ISCAS 94)* London, May 1994.

In chapter 3

The designs of the series photoconductor, series MESFET and diode bridge OS/H circuits are original, as is the analysis of these circuits. These circuits represent the first realisation of integrated optoelectronic sample and hold circuits. The method of adjusting the sampling instant is also novel. These circuit designs are published in:

[72] R. Mason and J. Taylor, "Optically triggered monolithic sample and hold circuit," *Electronics Letters*, vol. 29, no. 9, pp. 796-797, Apr. 1993.

[23] R. Mason and J. Taylor, "High-speed electro-optic analogue to digital converters," *Proc. IEEE Int. Symposium on Circuits and Systems (ISCAS 93)*, vol. 2, pp. 1081-1084, Chicago, USA, May 1993.

In chapter 4

The practical implementation of the OS/H circuits, and the electronic and optical test structures is described. These circuits represent the first use of the GEC-Marconi F20 GaAs MMIC process for optoelectronic applications.

[73] R. Mason and J. Taylor, "Design and evaluation of an optically triggered monolithic sample and hold circuit using GaAs MESFET technology," submitted to *J. Lightwave Technology.*

In chapter 5

All of the simulations and measured results presented in this chapter are original, as is there interpretation. The techniques used to measure the time domain response, sampling time adjustment and aperture jitter are also original. These results are presented in [73] and:

[74] R. Mason and J. Taylor, "An optically triggered monolithic sample and hold circuit using GaAs MESFET technology," *IEEE Int. Symposium on Circuits and Systems (ISCAS 94)* London, May 1994.

[75] R. Mason and J. Taylor, "An electro-optic sample and hold circuit using GaAs MESFET technology," *IEEE 3rd European Gallium Arsenide Applications Symposium (GAAS 94)*, Torino, Italy, Apr. 1994.

In chapter 6

The worked examples of the non-uniform sampling algorithms and their application to the optically triggered interleaved ADC are original.

In chapter 7

The proposal of the fully integrated *N*-path OS/H using polymer waveguides and spiral delay lines is original, and is discussed in [73] above.

In chapter 8

Novel techniques for utilising mode locked laser diodes to control the OS/H circuits are presented.

CHAPTER 2

GaAs DEVICES AND MODELS

2.1 THE PHYSICS OF GaAs

2.1.1 The Attraction of GaAs for High Speed Applications

Until the early 1960's the solid state device industry was dominated by one material – germanium. With the introduction of silicon this situation changed completely. Within just a few years the entire industry was converted because of two important characteristics. First, silicon has a higher energy bandgap (1.12eV cf. 0.66eV for Ge), which permits Si devices to operate over a wider temperature range (a feature especially important to the military), and secondly, Si forms a natural oxide which is one of the best insulators known. This oxide grows from the bulk of the material, whereas insulating layers need to be deposited on the surface of Ge (and GaAs). The silicon oxide provides for improved stability and planar, rather than mesa, type devices. Planar technology quickly led to integrated circuits and the electronics revolution [4].

As a semiconductor, GaAs has one of the characteristics that proved so important to the rapid development of silicon technology. GaAs has an even wider bandgap (1.42eV), allowing operation over a wider temperature range. In a semiconductor the bonds between neighbouring atoms are only moderately strong, and consequently some bonds may be broken at any temperature above absolute zero. When bonds are broken, free electrons are produced and these become available for conduction. The breakage of bonds corresponds to electrons traversing the forbidden energy gap (bandgap). The intrinsic carrier concentration (the number of carriers which will have sufficient thermal energy to occupy the conduction band) therefore depends upon the energy gap and the temperature, and can be summarised by the exponential relationship

$$n_i \propto e^{-E_G/2kT} \tag{2.1}$$

where n_i is the intrinsic carrier concentration, E_G is the energy gap, T is the temperature and k is Boltzman's constant. The intrinsic carrier concentration for GaAs is 1.79×10^6 cm^{-3} compared to 1.45×10^{10} cm^{-3} for Silicon, which means that GaAs has a much lower conductivity that silicon, resulting in the formation of a *semi-insulating*, rather than *semi-conducting*, substrate. This has a major impact on circuit design, since the device to device and device to substrate parasitic capacitance terms are very small. When compared with silicon technologies, this is an enormous advantage, both for digital and analogue circuitry [4,77-79].

The main attraction of GaAs, however, is the very high low-field electron mobility (8500 cm^2/V-s in n-type GaAs compared to 1500 cm^2/V-s in n-type silicon). Electron mobility sets an upper limit on the speed of devices. From these figures it appears that GaAs is about five or six times 'faster' than silicon, but this is actually an over-simplification which will be considered shortly. In a semiconductor there are two principal carrier types: electrons, which are the majority carriers in n-type semiconductors, and holes, which are the majority carriers in p-type semiconductors. The mobility of the carriers depends largely on the effective mass. In a given semiconductor, the holes have a greater effective mass than the electrons, which means that p-type devices will operate more slowly than n-type devices. The peak carrier mobilities of Ge, Si and GaAs are shown in table 2.1. For this reason p-type doping is not generally available with high-speed IC processes, such as the GEC-Marconi F20 process. This can cause serious problems for the circuit designer who is restricted to n-type devices [80].

TABLE 2.1

CARRIER MOBILITIES OF SOME COMMON SEMICONDUCTORS

material	electron mobility (cm^2/V-s)	hole mobility (cm^2/V-s)
Ge	3900	1900
Si	1500	450
GaAs	8500	400

2.1.2 The Energy Band Structure of GaAs

We have seen how the wider energy bandgap of GaAs gives it some useful advantages over silicon. We shall now examine the band structures in slightly more detail, qualifying some of the statements made. Fig 2.1 shows simplified energy band diagrams for silicon and GaAs [81]. In Fig 2.1 we can see that the conduction band of silicon consists of one 'valley' whereas GaAs has two such valleys. Electrons in GaAs exhibit two very different effective masses corresponding to the upper and lower valleys, and transfer from the lower valley to the upper valley as the electric field (and hence momentum) is raised. It can be shown [82] that the mobility is inversely proportional to the radius of curvature of the energy-momentum parabola. From the energy band diagrams (Fig 2.1) we can see that the lower valley of GaAs has a much smaller radius of curvature than the upper valley.

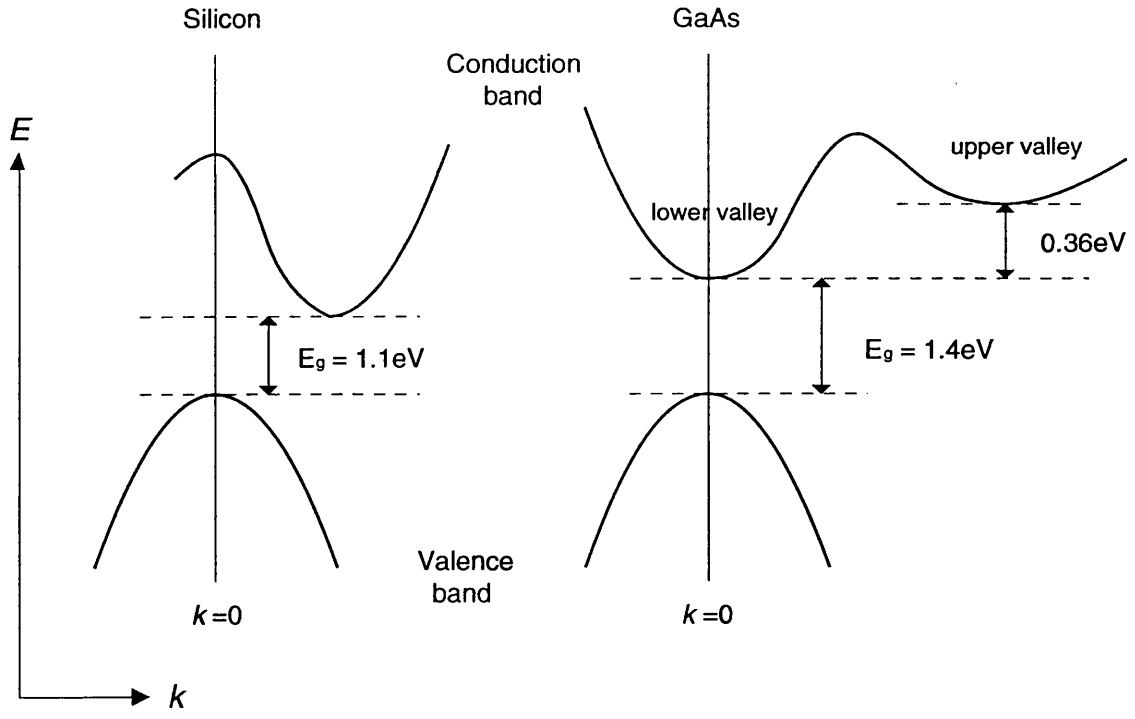


Fig 2.1 Simplified energy band structures of silicon and GaAs, showing larger bandgap and upper and lower valleys of GaAs.

The effective masses in the upper and lower valleys are:

$0.8m_0$ in upper valley

$0.07m_0$ in lower valley

where m_0 is the electron rest mass.

When an electric field is applied to the semiconductor, the carriers will move under its influence. The velocity of the carriers (the drift velocity) is determined by the electric field and by the effective mass. These are related by:

$$\overline{v}_{\text{drift}} = \frac{qE}{2m^*}\tau = \mu E \tag{2.2}$$

Where E = Applied electric field, q = carrier charge, m^* = effective mass, μ = mobility, τ = average time between collisions. We have seen, however, that the effective mass also depends on the electric field, so this is not a simple relationship. The variation of electron drift velocity with electric field is shown in Fig 2.2 [81].

In a sample of GaAs most of the electrons will be low mass (and therefore high mobility) below a critical field of ~ 0.3V/μm. Above this field electrons are excited into the upper valley and therefore become high mass, low mobility. The importance of this is clear when one considers that a typical GaAs MESFET gate width is 1μm. If the voltage across the device is 1 volt, then the field will be ~ 1 V/μm, ie higher than the critical field for high mobility. At high fields the electron drift velocity in GaAs tends to a value about 1.4 times greater than silicon. This is the main reason why GaAs is not 'five times faster' than silicon. Although the electron mobility is a limiting factor, the speed of devices is also effected by parasitic capacitance. The semi-insulating substrate of GaAs has a very low parasitic capacitance which can result in very high speed devices (eg. 80GHz f_T [83]).

Fig 2.2 also shows the drift velocity of electrons in InP. The drift velocity for this material is greater than either GaAs or Si. This property, along with the fact that it has a bandgap such that it can be used for optoelectronic applications in the 1.3μm to 1.55μm wavelength range, is the reason why InP is proving an important material for use in optoelectronic integrated circuits, particularly in the area of optical communications [84-88].

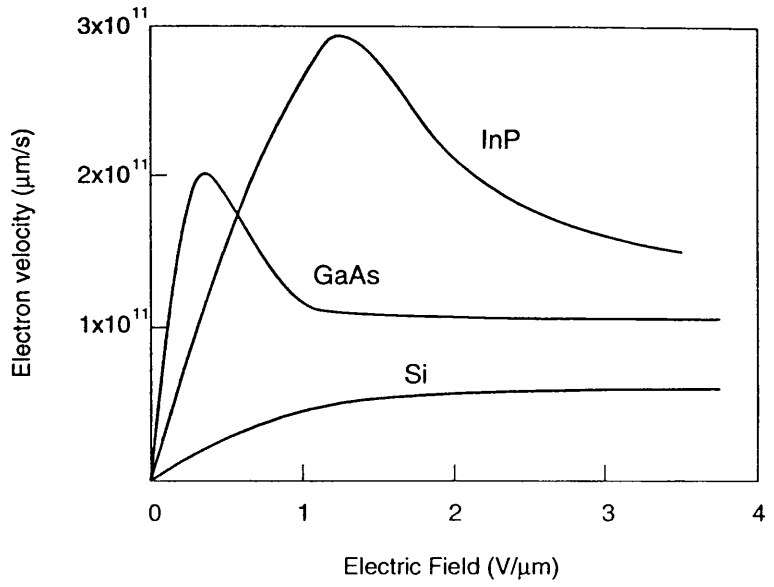


Fig 2.2 Drift velocity as a function of electric field for Si, GaAs and InP. This shows that at E-fields above 1V/μm the electron velocity in GaAs is only about 1.4 times that in silicon.

The other important feature of the energy band diagrams is that silicon has an *indirect* band gap (ie there is a momentum shift as well as an energy shift from the valence band peak to the conduction band valley), whilst GaAs has a *direct* band gap, (the valence band maximum and conduction band minimum appear at the same momentum value). Whether the band gap is direct or indirect has important consequences for the optical properties of materials. This aspect will be considered in the section on GaAs optical devices (Section 2.3).

2.1.3 Metal Semiconductor Contacts

The metal semiconductor contact, [82], is of great importance in semiconductor devices. Under certain conditions it can form contacts of low resistance and is used as an ohmic contact. Under other conditions a barrier is formed, rather like a *p-n* junction, and this can be exploited to make a number of devices. This is known as a Schottky contact. The Schottky contact is especially important when making GaAs devices, as it is difficult to produce an effective *p* dopant in this material.

(i) The Schottky contact

We shall first consider the case of the Schottky contact. The energy band diagrams of a metal and an *n*-type semiconductor in isolation are shown in Fig. 2.3.

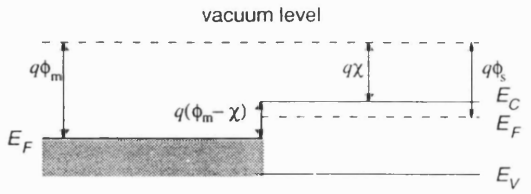


Fig 2.3 Energy band diagrams of a metal and a semiconductor in isolation.

$q\phi_m$ = metal work function, $q\phi_s$ = semiconductor work function and $q\chi$ = electron affinity

In isolation the metal work function does not equal the semiconductor work function. If the two materials are now brought into contact, majority carriers (ie electrons for *n*-type) flow from the semiconductor into the metal, establishing equilibrium and lining up the Fermi levels, Fig. 2.4.

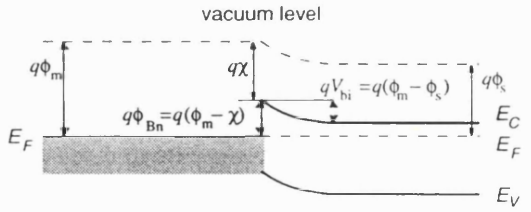


Fig 2.4 Energy band diagram of a metal-semiconductor contact, showing alignment of Fermi levels and development of potential barrier.

For *n*–type GaAs this creates a potential barrier of height:

$$q\phi_{Bn} = q(\phi_m - \chi) \tag{2.3}$$

Under equilibrium conditions electrons flow across the junction in both directions with equal rates, resulting in zero net current flow across the barrier. Applying a forward bias reduces the barrier height creating a larger electron flow from the semiconductor to the metal. The barrier seen by the electrons from the metal is, however, unchanged, leading to a large forward current.

Applying a reverse bias increases the barrier height, reducing the flow of electrons from the semiconductor causing a small net flow of electrons from the metal to the semiconductor. Figure 2.5 shows the processes which lead to current flow across a Schottky barrier.

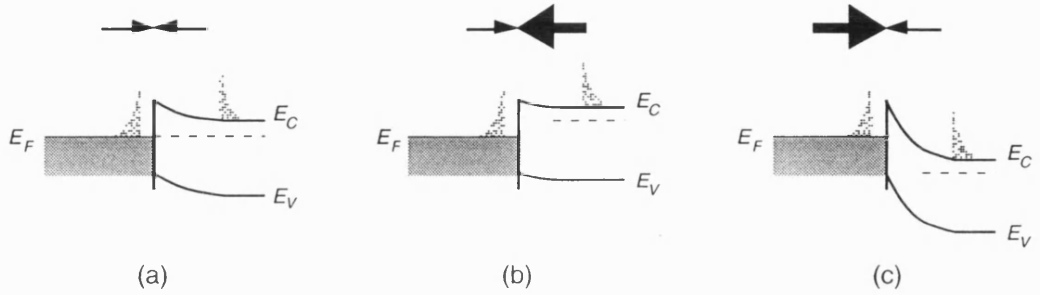


Fig 2.5 Current transport across a metal-semiconductor junction by thermionic emission process. (a) thermal equilibrium, (b) forward bias, (c) reverse bias.

The overall *I-V* characteristics of a Schottky barrier are given by :

$$J = J_o\left(e^{eV/kT} - 1\right) \tag{2.4}$$

where J = current density and J_o = saturation current density. This is the same form as the *I-V* characteristics of a *p–n* junction diode.

(ii) Ohmic contacts

An ohmic contact is a metal-semiconductor contact with a very low resistance and is typically used for the establishment of MESFET source and drain contacts. The resistance of a metal-semiconductor junction can be reduced by lowering the potential barrier height or by promoting quantum mechanical tunnelling through the barrier. From equation (2.2) it can be seen that the barrier height depends on both the electron affinity of the semiconductor and on the metal work function. The electron affinity a property of the semiconductor material and is therefore not within our control. Thus to lower the barrier we must choose a metal with a small work function. Metals such as magnesium and aluminium satisfy this condition. Quantum mechanical tunnelling occurs more readily across very narrow barriers, which can be established by the use of very high doping levels. For this reason it is common

to see ohmic contacts being made to highly doped semiconductors.

2.2 GaAs MESFETs

In the twenty years since the first reported GaAs MMIC [89] a wide range of GaAs devices have emerged, including JFET, MISFET, MESFET, HEMT and HBT types [81,90]. Of these technologies the only one in widespread commercial use at present is the depletion mode MESFET (D-MESFET). Some manufacturers also produce an enhancement mode MESFET (E-MESFET), but these are more difficult to fabricate and tend to find applications in digital, rather than analogue, circuits [78]. A schematic of a typical MESFET is shown in Fig. 2.6.

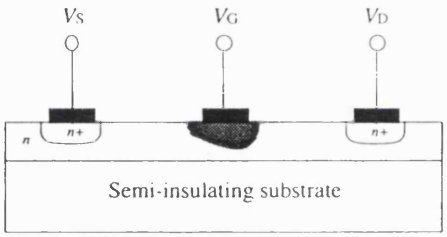


Fig 2.6 Schematic of a MESFET. Application of a negative voltage at the gate forms a depletion region which progressively restricts channel conduction.

The operation of a MESFET is similar to that of a JFET except that the *p-n* junction of the JFET is replaced with a Schottky junction. With the drain contact biased positive and the gate and source grounded, the *n* channel will be conductive with a characteristic *on* resistance. Applying a negative bias to the gate will reverse bias the Schottky junction, depleting the channel and restricting current flow.

2.2.1 Modelling of GaAs MESFETs

Modelling of MESFETs is a complex issue, and detailed accounts can be found in [81,91-96]. Because high performance GaAs MESFETs are typically fabricated with submicron gates, the development of accurate physical models

is very difficult. In practice it is common to use models based on either empirical results, or a combination of empirical and physical principles. Although physical models generally give more accurate results than empirical models, a practical model need not be more accurate than the expected device variations. If it were, processing variations would inevitably mask any performance improvement predicted by the model. Since device uniformity in GaAs technology is still relatively poor compared with silicon technology, the modelling of FET devices for analogue circuit applications should concentrate more on correctly predicting device trends than on precise matching to device characteristics. Furthermore, the circuit designer is often restricted to models which can be used with a circuit simulator with pre-set models. For our simulation purposes we have used the HSPICE circuit simulator, which provides two models suitable for MESFET simulation: the Shichman-Hodges model [97] and the Curtice model [98].

To develop a model for the GEC-Marconi F20 MESFET we were supplied with DC and S-parameter measurements from a range of devices, fabricated over several foundry runs. These results clearly showed that the MESFET characteristics can vary over a wide range between foundry runs and across a single wafer. The wide variations observed in this data led us to adopt the simplest model and to concentrate on making the circuit designs tolerant to device variations.

(i) DC Models

The simplest DC FET model is the Shichman–Hodges model [97], which was developed in 1968 for the simulation of insulated gate FETs. This model separates the FET operation into two regions – the *linear* region and the *saturation* region and assumes quadratic FET behaviour, as shown in Fig. 2.7.

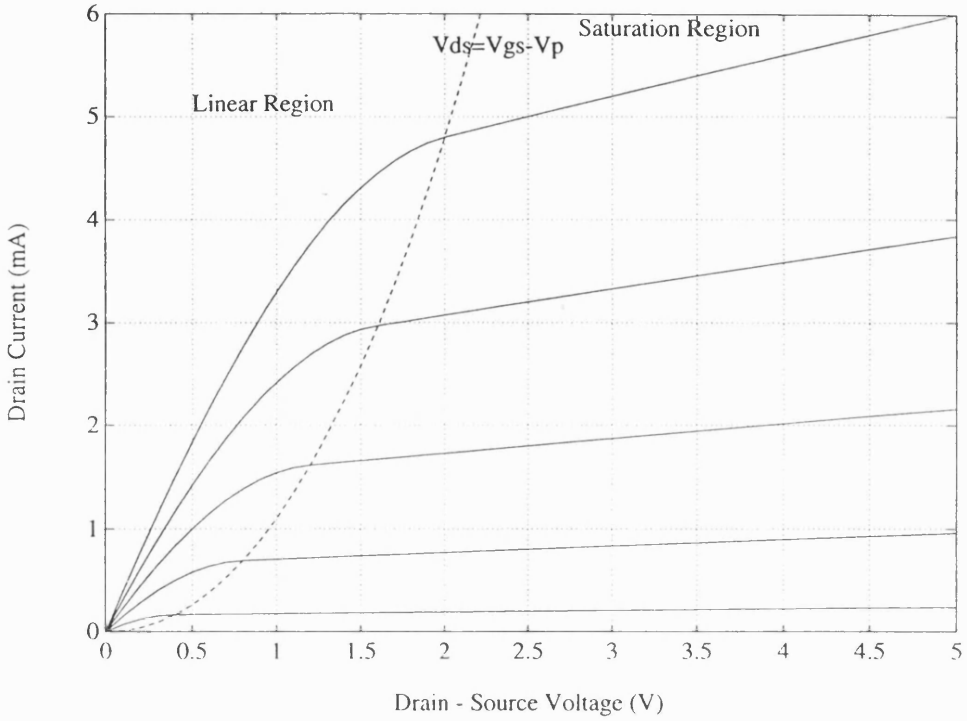


Fig 2.7 Shichman-Hodges model of FET. This is a graphical representation of equations (2.5 – 2.7), showing the linear and saturation regions. (β = 1mA/V^2, λ = 0.1 V^{-1}, V_p = –2V).

This model is described by the following equations:

$$I_D = 0 \qquad \text{cut-off } (V_{GS} \le V_P) \qquad (2.5)$$

$$I_D = \beta\left[2(V_{GS} - V_P)V_{DS} - V_{DS}^2\right](1 + \lambda V_{DS}) \qquad \text{linear region} \qquad (2.6)$$

$$I_D = \beta(V_{GS} - V_P)^2(1 + \lambda V_{DS}) \qquad \text{saturation region } (V_{DS} \ge V_{GS} - V_P) \qquad (2.7)$$

where I_D = drain current, V_{GS} = gate-source voltage, V_P = threshold (pinch-off), α, β, λ = device constants. For this project we have chosen to use a single device geometry throughout all of the circuit designs. This is a 20µm D-MESFET, fabricated in 20-GHz f_T, 0.5µm gate length GEC-Marconi F20 process [69]. The

decision to restrict ourselves to a single device was taken after careful examination of the modelling information with which we have been supplied [99]. It is clear from this data that the MESFET characteristics can show significant variation across a single wafer, and even larger variations between separate foundry runs. Tables 2.2a and 2.2b show both of these effects for 20μm and 40μm devices, complied from data obtained from 4 foundry runs made between 1990 and 1992.

TABLE 2.2A

MAXIMUM VARIATION OF MESFET PARAMETERS ACROSS A SINGLE WAFER

Device Size	β	V_P	λ	α
20μm	26%	11%	19%	16%
40μm	13%	11%	63%	28%

TABLE 2.2B

MAXIMUM VARIATION OF MESFET PARAMETERS ACROSS 4 FOUNDRY RUNS

Device Size	β	V_P	λ	α
20μm	26%	15%	54%	24%
40μm	16%	17%	67%	32%

Data was supplied for devices with gate widths of up to 300μm, and these all show a similar range of variations. Because of these large variations it is impossible to ensure that device characteristics scale in proportion to the device size. By choosing to use a single device we can ensure that the circuits will settle to a DC operating point, as any parameter variation will simply cause a uniform current scaling throughout the circuit. If we were to use a range of device geometries this might not be the case.

A drawback to the Shichman-Hodges model is the assumption that the drain current reaches saturation at $V_{DS} = V_{GS} - V_T$. MESFETs that posses a large negative threshold voltage typically exhibit current saturation at a V_{DS} less than that modelled by (2.7). This effect, known as *early saturation*, is a result of the carrier velocity saturation and reduced mobility at high electric fields. Figure 2.2 shows how the electron velocity reaches a maximum when a field of

about 1V/μm is applied, so increasing the field further will not increase the current flow.

A more sophisticated model, which can also be used with HSPICE, is the Curtice model [98]. This replaces the Shichman–Hodges equations with a single expression, adding a hyperbolic tangent function to adjust the saturation point:

$$I_D = \beta(V_{GS} - V_P)^2(1 + \lambda V_{DS})\tanh(\alpha V_{DS}) \tag{2.8}$$

where α is a device constant. An example of the application of this model to measured data [98] for a 1μm gate length MESFET is shown in Fig. 2.8. This MESFET shows pronounced early saturation. The Curtice model can be tailored to fit the measured data very well, while the Shichman–Hodges model is very inaccurate below the saturation region.

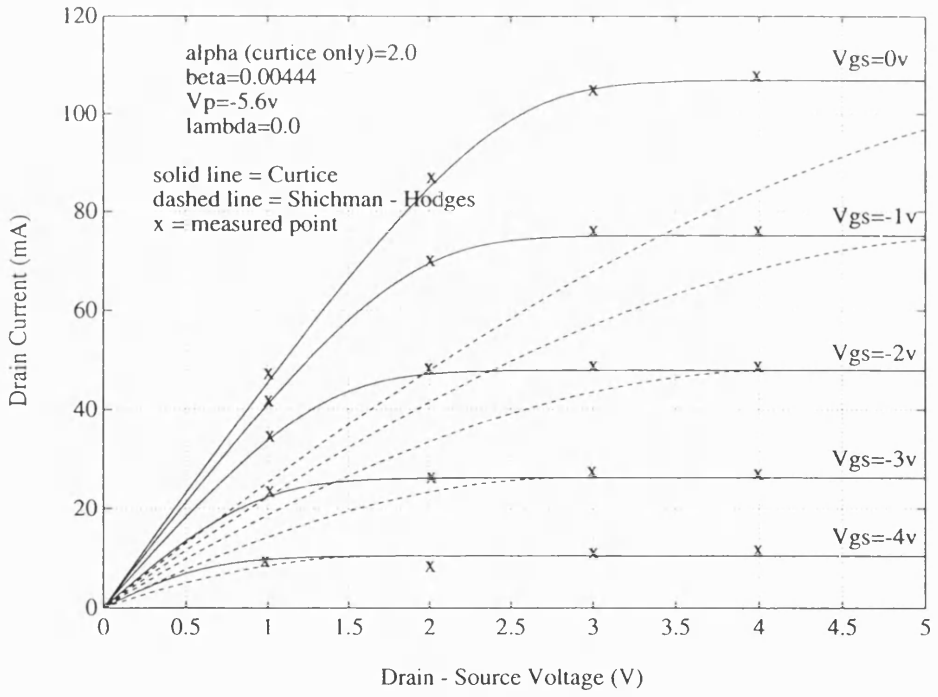


Fig 2.8 Measured characteristics of a 1μm MESFET from [98]. This shows how the Curtice model is a much better fit to the linear region characteristics of certain MESFETs.

Although early saturation is a prominent effect in devices with a large threshold voltage, MESFETs with small threshold voltages exhibit this phenomenon to a much lesser extent. The measured characteristics of the –1V threshold F20 MESFETs show no significant early saturation. This enables us to use the Shichman–Hodges model, which is simpler and uses much less CPU time than the Curtice model. From this data we have developed the worst case SPICE model of the 20µm MESFET shown in figure 2.9. This also shows the Curtice model, demonstrating the similarity between the models.

Many circuit designers choose to exploit the early saturation of GaAs [100,82]. Although this technique has proven successful in some circumstances, the above data show that it cannot be used as a general circuit design method. For this reason we have chosen to operate well into the saturation region (V_{DS} = 2.5v), where the MESFET behaviour is more predictable.

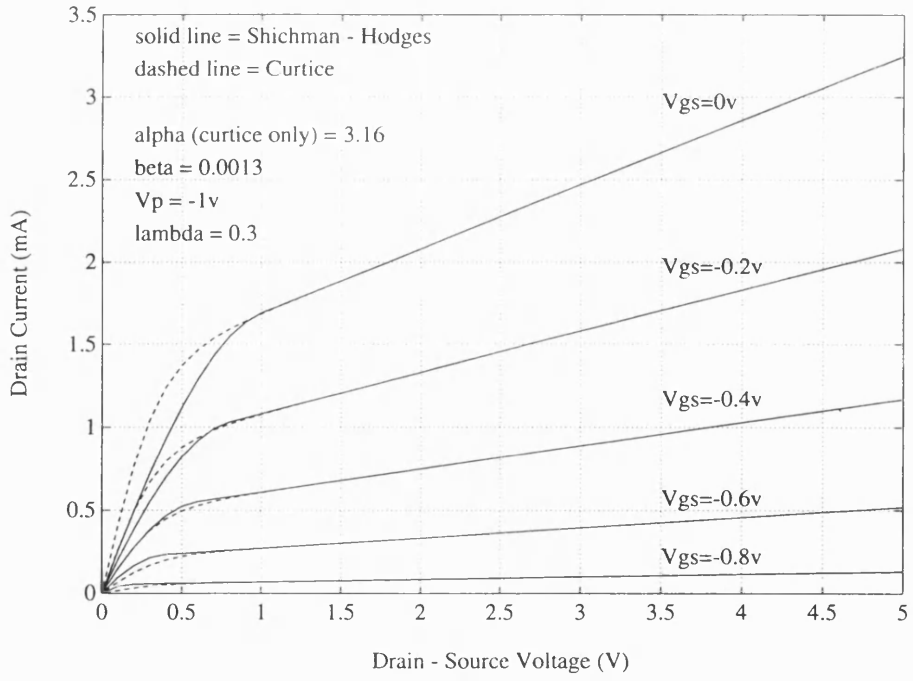


Fig 2.9 Simulated *I-V* curves for a 20µm MESFET fabricated with the GEC-Marconi F20 process. The similarity between the Shichman-Hodges and Curtice models justifies the use of the simpler S-H model for circuit simulation. The model parameters used in this simulation are derived from measured data [99].

(ii) AC Models of GaAs MESFETs

The AC response of a MESFET can be modelled using the small-signal equivalent circuit shown in Fig. 2.10.

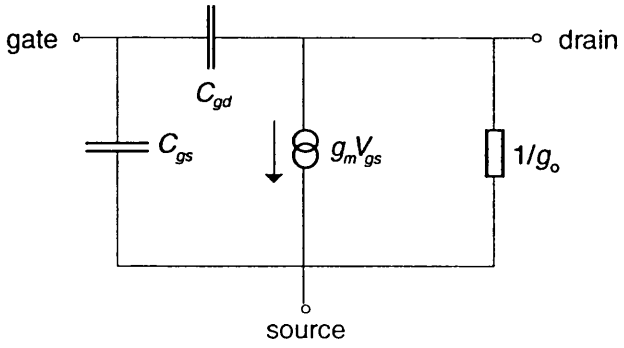


Fig 2.10 MESFET small signal equivalent circuit.

The values of the transconductance, g_m, and the output conductance, g_o, can be found from the saturation region equation of the Shichman-Hodges model (2.7), and are defined as:

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = 2\beta(V_{GS} - V_P)(1 + \lambda V_{DS}) \tag{2.9}$$

$$g_o = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} = \lambda\beta(V_{GS} - V_P)^2 \tag{2.10}$$

Therefore at a given operating point (ie fixed V_{GS} , V_{DS}), g_m and g_o are constant. From these expressions we can therefore derive a small signal description of the FET:

$$i = g_m v_{gs} + g_o v_{ds} \tag{2.11}$$

where i, v_{gs}, v_{ds}, are small signal values.

To determine the component values in the small-signal equivalent circuit we were provided with a set of S-parameter measurements [99]. The S-parameter measurements, which are made in a 50Ω environment, can be de-embedded to give the H and Y-parameters. These are defined using open circuit and short circuit terminations and so we can find the values of each of the equivalent

circuit components. It transpires that the Y-parameters give the simplest expressions for each of the components. The Y-parameters measure the forward and reverse admittance of the network with short-circuit terminations, and are defined as:

$y_{11} = y_i = i_1/v_1$ = short-circuit input admittance ($v_2 = 0$)
$y_{12} = y_r = i_1/v_2$ = short-circuit reverse transfer admittance ($v_1 = 0$)
$y_{21} = y_f = i_2/v_1$ = short-circuit forward transfer admittance ($v_2 = 0$)
$y_{22} = y_o = i_2/v_2$ = short-circuit output admittance ($v_1 = 0$)

where v_1 and i_1 are the input voltage and current, and v_2 and i_2 are the output voltage and current. Applying these to the small-signal equivalent circuit of Fig. 2.10, we find that:

$$y_{11} = j\omega\left(C_{gs} + C_{gd}\right) \tag{2.12}$$

$$y_{12} = j\omega C_{gd} \tag{2.13}$$

$$y_{21} = g_m - j\omega C_{gd} \tag{2.14}$$

$$y_{22} = g_o + j\omega C_{gd} \tag{2.15}$$

therefore we can find the values of g_m, g_o, C_{gs} and C_{gd} from the Y-parameters. Fig. 2.10 shows a complete set of measured Y-parameters for a 20μm gate width MESFET, and from these results we find g_m = 3.7mS, g_o = 300μS, C_{gs} = 47fF and C_{gd} = 5.6fF. By re-arranging equations (2.9) and (2.10) we can find expressions for the SPICE parameters β and λ:

$$\beta = \frac{g_m\left(V_{GS} - V_P\right) - 2g_o V_{DS}}{2\left(V_{GS} - V_P\right)^2} \tag{2.16}$$

$$\lambda = \frac{2g_o}{g_m\left(V_{GS} - V_P\right) - 2g_o V_{DS}} \tag{2.17}$$

giving values of $\beta = 1.1\text{mA/V}^2$ and $\lambda = 0.273\text{V}^{-1}$.

The f_T of a MESFET is the frequency of unity current gain, and is given approximately by:

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{2.18}$$

therefore the f_T of these MESFETs is 12.6GHz. This is somewhat lower than the expected value of 20GHz, but is due to the fact that the –1V threshold process is still in an experimental stage.

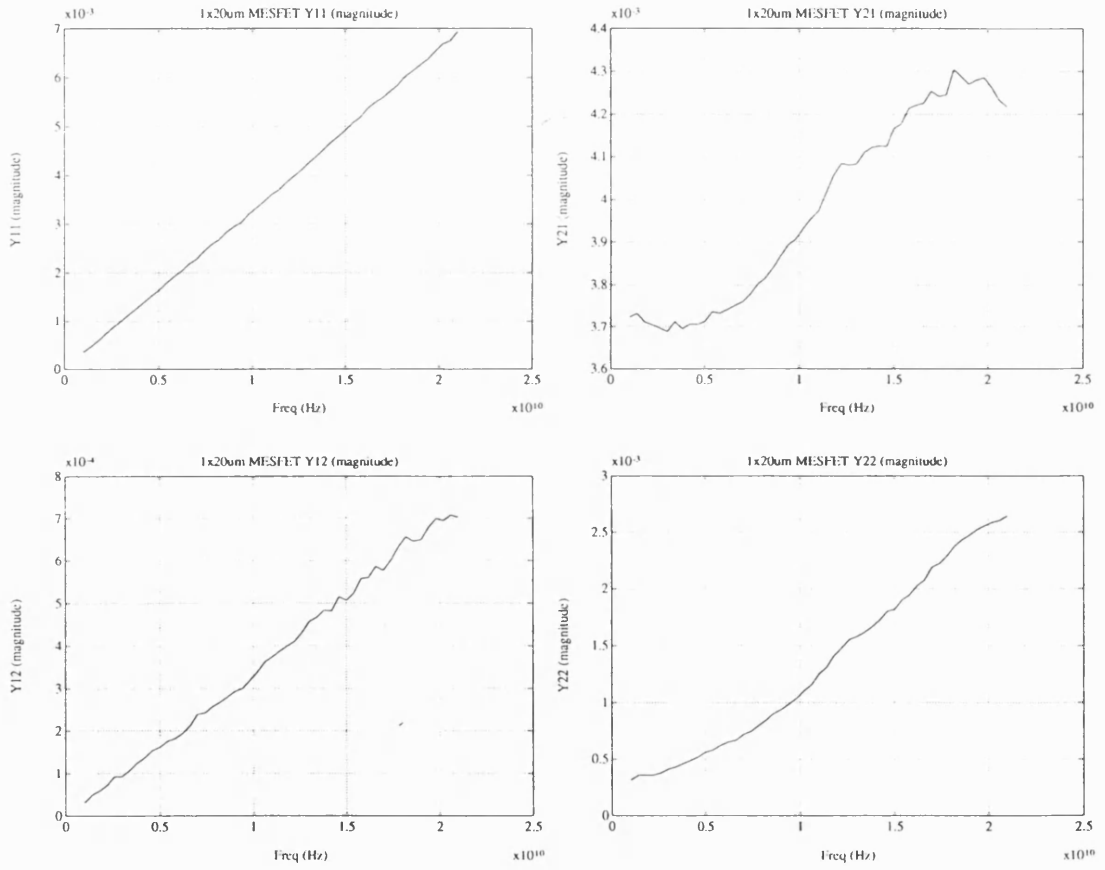


Fig 2.11 Measured Y-parameters of a 20μm MESFET fabricated with the GEC-Marconi F20 process.

An unusual property of GaAs MESFETs, which has serious consequences for circuit design, is that the output conductance, g_o, is dependent on frequency [81]. This frequency dependant drain conductance is caused by the trapping and subsequent thermal re-emission of electrons in the substrate [102]. This thermal process is slow, having a time constant of the order of 1ms to 100ms.

The consequence of this is that the value of λ varies from about $0.06V^{-1}$ below around 1kHz [81], to $0.273V^{-1}$ at high frequency, corresponding to a DC value of $g_o = 96.5\mu S$ and an AC value of $g_o = 300\mu S$. To model this dispersive conductance the small-signal equivalent circuit can be modified, as shown in Fig. 2.12.

The value of C_{oac} is given by

$$C_{oac} = \frac{g_{oac}}{2\pi f_d} \approx 32nF \tag{2.19}$$

where f_d is the dispersion frequency (typically around 1kHz).

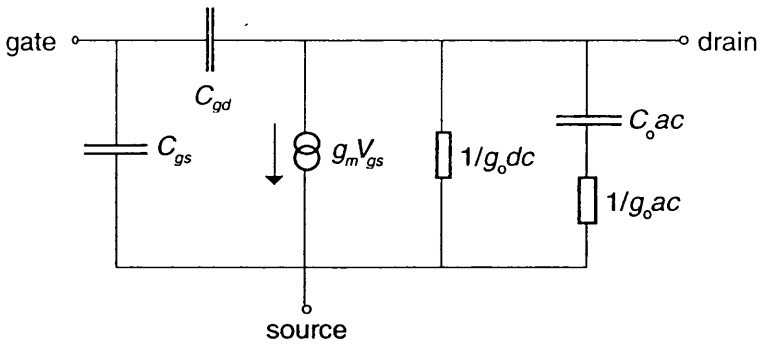


Fig 2.12 Dispersive small-signal equivalent circuit. The components $C_o ac$ and $g_o ac$ simulate the low frequency transient effects observed in GaAs MESFETs.

The S-parameter measurements give the values of g_m, g_o, C_{gs} and C_{gd} for a given operating point (i.e. V_{GS} = 0V, V_{DS} = 2.5V). To enable accurate predictions of behaviour, this operating point has been maintained throughout the circuit designs as far as possible. However, there are examples of where this cannot be done, such as when a MESFET is used as a diode or a series analogue switch. To estimate circuit performance under these circumstances we need to determine approximate values for the parasitic capacitance.

The parasitic capacitances in a MESFET are depletion capacitances, i.e. they depend on the charge in the depletion layer, and hence the applied voltage. The capacitance C_v at a given voltage V is given by:

$$C_v = \frac{C_0}{\sqrt{1 - V/V_{bi}}} \tag{2.20}$$

where C_0 = zero applied voltage capacitance, V_{bi} = built-in voltage (~1.1V for GaAs [82]).

This equation is useful in many circumstances, but does not correctly describe the value of capacitance beyond the pinch-off voltage, and gives infinite or complex values for voltages equal to, or larger than V_{bi}. For junction voltages equal to or beyond pinch-off, the depletion layer extends to the substrate and the associated capacitance falls to zero. Only small fringing capacitances remain. For the purpose of later calculations, I have assumed that C_{gs} below pinch-off is approximately equal to the measured value of C_{gd} at V_{DS} = 2.5V, i.e. 5.6fF.

2.3 GaAs OPTICAL DEVICES

An important difference between the band structures of silicon and GaAs (Fig 2.1) is that silicon has a *indirect* bandgap, whilst GaAs has an *direct* bandgap. In light-emitting devices, photons are emitted when recombination of electrons and holes occurs [49,82]. Recombination in indirect bandgap semiconductors, eg silicon, involves a change in momentum as well as a change in potential energy. This recombination process, which results in excess energy being transferred to the lattice where it appears as heat, is less likely to occur than the transition which occurs in direct bandgap semiconductors, such as GaAs. In direct bandgap materials recombination can occur without a change in momentum, therefore most of the energy appears as a photon with a wavelength given by Planck's law:

$$\lambda = \frac{hc}{E_G} \tag{2.21}$$

where h = Planck's constant and E_G = energy band-gap. As the band-gap of GaAs is 1.42eV, the cut-off will occur at 874nm.

The reverse of this process occurs in a photodetector: absorbing a photon of sufficient energy will promote a valance electron into the conduction band, causing the formation of an electron-hole pair. If the band gap is indirect a momentum change will occur and therefore some of the energy will be lost. The energy of the absorbed electron must be at least equal to the energy

bandgap, E_G, so the photodetector will have a long wavelength cut-off given by Planck's law (2.21). Below this wavelength photons will have sufficient energy to promote electrons to the conduction band. The excess photon energy will be given up to the lattice in the form of heat. Therefore we would expect the wavelength response to rise linearly from short wavelengths until the long wavelength cut-off, and then decrease to zero. Fig 2.13 shows an experimental plot of sensitivity versus wavelength for a GaAs MSM PD [103].

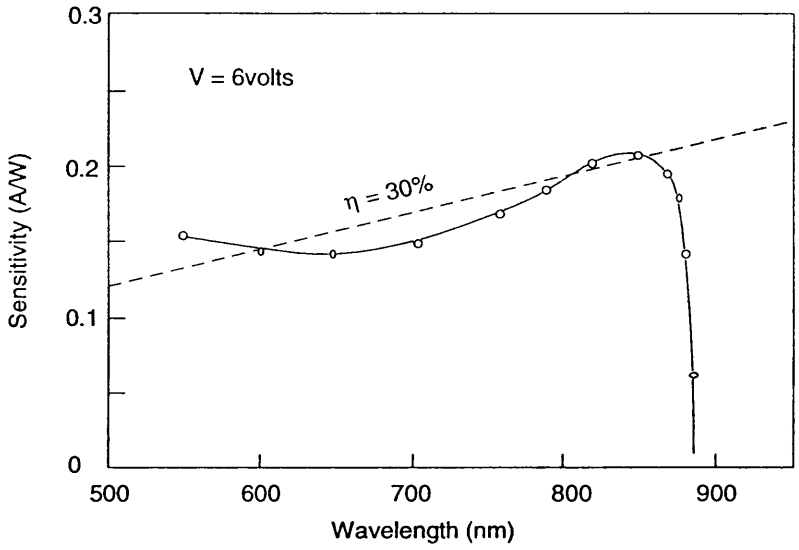


Fig 2.13 Spectral response of a GaAs MSM-PD showing long wavelength cut-off at ~ 870nm.

2.3.1 Identification of Suitable Photodetectors

We saw in section 1.5 that a key component in an optically triggered ADC is an integrated photodetector. A suitable photodetector must have a very high bandwidth (in excess of 1GHz for this application) and a responsivity such that it can generate adequate photocurrent when illuminated by a laser diode. In addition we must be able to fabricate the device using the GEC-Marconi F20 process without modification. Two suitable detectors have been identified: a metal-semiconductor-metal photodetector (MSM-PD) [104] (this device is identical to an MMIC interdigital capacitor), and a diode connected MESFET [105]. The bandwidth of these devices is typically in excess of 5GHz [106], and has been reported as high as 105GHz for the MSM-PD [107].

2.4 METAL-SEMICONDUCTOR-METAL PHOTODETECTORS

The metal-semiconductor-metal (MSM) photodetector was first introduced in 1980 [104] and has proved to be one of the most important photodetector structures available, as demonstrated by the vast amount of literature concerning this device [eg. 108-115]. The detector owes its popularity mainly to the ease of integration in standard planar IC fabrication processes. This has simplified the realisation of optoelectronic integrated circuits (OEICs), with the advantages these bring, namely larger bandwidth due to reduction of parasitic capacitance and bond induction, improved sensitivity (also due to reduced capacitance), economies of scale, etc. Many examples of the application of MSM photodetectors in OEICs can be found, eg [103,116-126].

2.4.1 Energy Band Description

The simplest form of MSM structure is a two terminal device having a uniformly doped semiconductor slice with metal contacts on the opposite sides of the slice, as shown in Fig. 2.14. As each metal-semiconductor junction forms a Schottky contact, the energy band diagram for the MSM at thermal equilibrium is as shown in Fig. 2.15, where Φ_{n1} and Φ_{n2} are the barrier heights for the two contacts, V_{D1} and V_{D2} are the built-in potentials, and L is the thickness of the slab. Corresponding charge and field distributions are shown in Figs 2.16 and 2.17. Applying a negative voltage to contact No. 1 causes it to become reverse biased and contact No. 2 to become forward biased. This will increase the depletion region around contact No. 1, and decrease the depletion region around contact No. 2. As the applied voltage increases, the *sum* of the two depletion widths also increases, until they eventually meet, at the *reach-through* voltage V_{RT}, and complete depletion occurs. This situation is illustrated in Fig. 2.18. Further increases in applied voltage bend the energy bands further downward, until avalanche breakdown occurs near contact No. 1. A more complete discussion of the current transport mechanisms in the MSM can be found in [127].

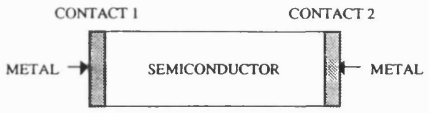


Fig 2.14 Structure of a metal-semiconductor-metal diode.

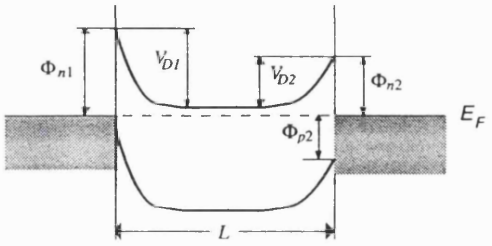


Fig 2.15 Energy band diagram of an MSM diode showing the formation of potential barriers at the metal-semiconductor junctions.

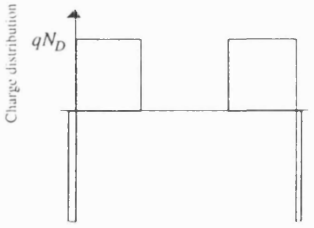


Fig 2.16 Charge distribution of an MSM diode

Fig 2.17 Field distribution in an MSM diode

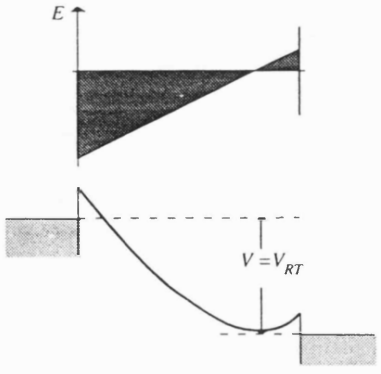


Fig 2.18 MSM diode at the reach through voltage V_{RT} where the two depletion regions touch each other.

In order that the MSM can be incorporated into a planar IC fabrication process, a modified structure is used. This consists of a series of interdigitated Schottky metal fingers placed directly on the lightly doped substrate, as shown in Fig. 2.19. This type of structure is commonly used to form accurate, small-value capacitors for GaAs MMICs, and is therefore a standard component in most MMIC fabrication processes.

As we will be using fibres to illuminate this device, we have chosen the dimensions of the device to be similar to the core diameter of a multimode fibre (50μm). The MSM fingers are drawn in 4μm level 2 metal (the finest width for this level), with 4μm gaps. We have arranged for the side-by-side combination used in the bridge circuit to cover 60μm x 60μm, so each device has 4 fingers, 56μm long. The capacitance of each MSM is about 20fF.

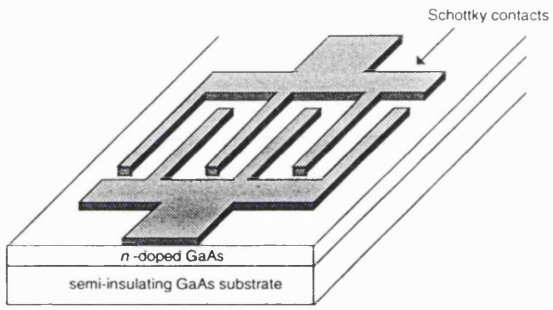


Fig 2.19 Planar MSM photodetector, consisting of Schottky metal fingers placed directly on the lightly doped substrate.

2.4.2 Optical Properties

From the energy band diagrams of the MSM it is easy to see how this device might be used as a photodetector. When a bias voltage is applied a potential gradient is established. If a photon of sufficient energy is absorbed in this depletion region it will generate an electron-hole pair by promoting an electron from the valance band to the conduction band. This electron will consequently be swept down the potential gradient, causing current flow.

As a minimum photon energy is required to promote an electron into the conduction band, we would expect the MSM detector to exhibit a long-wavelength cut-off given by Planck's Law (2.21).

The quantum efficiency of a photodetector is defined as the ratio of electrons

generated to incident photons. If the incident optical power is P watts, the number of incident photons per second, N_p, is given by:

$$N_P = \frac{P}{h\upsilon} = \frac{P\lambda}{hc} \tag{2.22}$$

If a photocurrent I is generated, the number of photons per second is I/q, where q is the electron charge. Therefore the quantum efficiency, η, is given by:

$$\eta = \frac{Ihc}{qP\lambda} \tag{2.23}$$

As the MSM detectors used for all of these experiments are fabricated with a finger width and gap width of 4μm, only half of the total device area is available for light absorption. Therefore the absolute maximum quantum efficiency is 50%.

2.4.3 Pulse response

The pulse response of an MSM detector is determined by two effects, namely the carrier transit time and parasitic effects [128-131]. The transit time can be estimated by considering the electron velocity in GaAs. From Fig. 2.2 we can see that above an electric field of 1V/μm the electron velocity is ~10^{11}μm/s. So if the bias voltage is above 4V the maximum transit time across a 4μm gap will be around 40ps. If we take this as an indication of the rise-time of the device, then the bandwidth (given by $0.35/t_r$) will be ~9GHz. By reducing the finger and gap width the bandwidth of the device has been increased to 105GHz [107]. The capacitance of the MSM will cause an RC limited response. For example, for a typical capacitance of 20fF and a 50Ω environment the RC response will set an upper limit on the –3dB bandwidth of 160GHz, indicating that the bandwidth is limited primarily by the transit time effects. These arguments are somewhat oversimplified, because in a planar device both of the electrodes are on the surface. Light of 830nm will penetrate a few microns into the device and so the carriers actually travel in curved paths through the E-field [132]. Also, the magnitude of the E-field is decreased as it penetrates into the device. However, since we only require the detectors to operate at speeds of <1GHz in

this application, we can confidently assume that they will be fast enough.

A variety of sophisticated MSM models have appeared in the literature [133,134], but as with the MESFET models, these cannot be used with a fixed model simulator. Instead we have modelled the MSM simply as an ideal current source in parallel with a capacitor, and the optically controlled MESFET as a current source in parallel with the standard HSPICE MESFET model (section 2.2.1).

CHAPTER 3

CIRCUIT DESIGN

In the introduction the OS/H was identified as a key component in an interleaved ADC. By employing the OS/H, we are able to exploit some of the inherent advantages of optical technology. For example, in the area of high-speed pulse technology, optical techniques are clearly superior to conventional electronic capabilities. Intense ultrashort pulses having durations of less than 0.5ps and peak powers of >50W can be generated from mode-locked semiconductor diode lasers [135]. These pulses can be distributed to large numbers of separate locations with effectively zero dispersion and timing jitter by means of optical clock distribution [29]. These properties naturally lead one to investigate the use of optics for high speed sampling.

Perhaps the earliest work on optoelectronic sampling was that by Auston in 1975 [136], which addressed problems in wideband radar signal processing. This technique involves fabricating a photoconductive transmission switch on a microstrip transmission line. In Auston's work the microstrip line consists of a silicon substrate with a uniform aluminium ground plane on the bottom and a narrow aluminium strip for a upper conductor. The upper conductor has a gap of high resistance, preventing transmission of the signal across the device.

Two optical pulses are needed to operate the device. To turn the switch on a pulse with a wavelength of 0.53μm is used. This pulse is absorbed near the surface of the crystal, producing an area of high conductivity. If this pulse is then removed, the switch will continue to conduct for some time, due to the slow recombination of the carriers (typically 10ns [82]). To overcome this problem the switch is turned off by means of a second pulse with a wavelength of 1.06μm. This pulse is absorbed to a much lesser extent than the short wavelength pulse, and so the region of high conductivity extends down to the ground plane, short-circuiting the transmission line and preventing further conduction. This type of transmission gate can achieve rise times of around 10ps and has been used with some success for radar signal processing and

analogue sampling oscilloscopes [137-142]. The very short sampling period produced by this technique is not, however, suitable for use in analogue to digital conversion. This is because ADC circuitry needs to be presented with an unchanging voltage during the conversion period, and so a sample and hold function is required.

A more recent approach to optoelectronic sampling involves growing GaAs at low temperatures using molecular beam epitaxy (MBE). This has the effect of reducing the carrier lifetimes from around 10ns to <0.5ps, and overcomes one of the major problems of the photoconductive optoelectronic switch. Using this approach optoelectronic sampling gates have been fabricated using GaAs grown at ~200°C (as opposed to the more usual growth temperature of ~600°C) which reveal a FWHM response time of ~1ps [143-146]. These include an MSM type device with 0.2μm finger width and gap width and an active area of 7μm x 7μm which displayed a responsivity of 0.1A/W, a –3dB bandwidth of 375GHz and a FWHM response time of 1.2ps [415]. Similar devices have recently been fabricated in InGaAs/GaAs for use at 1.3μm - 1.55μm , although these currently have a very low responsivity and need further development [147].

3.1 FUNDAMENTALS OF SAMPLE AND HOLD CIRCUITS

We saw in chapter 1 that an essential component in an optoelectronic ADC is an optically triggered sample and hold circuit (OS/H). The operation of a sample and hold circuit consists of two phases. The *sample* (or *track*) mode is the digitally controlled state of the S/H circuit during which the output is coupled to the input. The circuit switches to the *hold* mode upon receipt of a hold command. In this state the output takes on the value of the input at the instant the command is received and holds that value until another sample command is received. An example of *ideal* sampling is shown in Fig. 3.1.

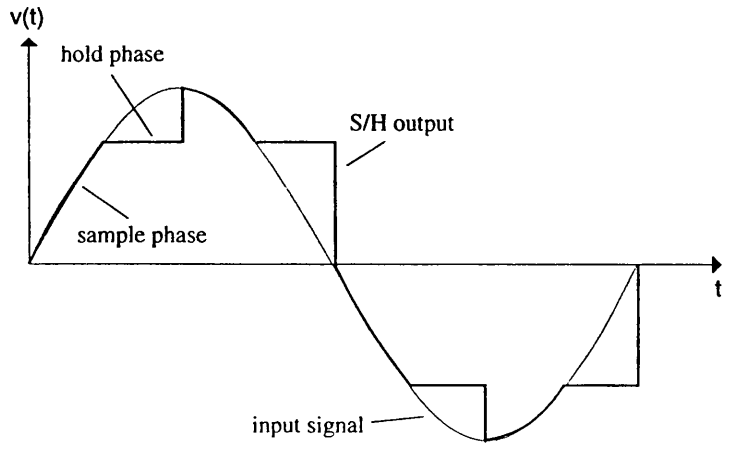


Fig 3.1 The operation of an ideal sample and hold circuit.

The simplest realisation of the S/H function consists of a switch and a holding capacitor as shown in Fig. 3.2.

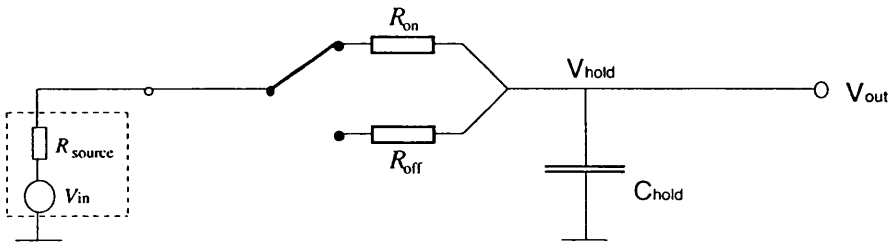


Fig 3.2 Simplest sample and hold realisation.

With the switch closed, the circuit is in the sample mode and the output voltage is equal to the input voltage. When the switch is opened, the circuit changes to the hold mode, with the capacitor holding the value of the input voltage which was present at the instant the switch was opened. A serious drawback of this circuit is that any load on the output will discharge the holding capacitor resulting in an error in the stored value. Furthermore, if R_{on} is comparable to, or smaller than the source impedance R_{source} then the voltage appearing at the input terminals will be reduced, causing a gain error and a reduction in the current available to charge C_{hold}. These shortcomings can be overcome by using input and output unity gain buffers as shown in Fig. 3.3. However, the input offset voltages associated with each buffer amplifier add to give an overall offset which is the algebraic sum of the two offset voltages, and

the finite bandwidth of the buffers will reduce the bandwidth of the sample and hold circuit. If we need to operate this circuit at high sampling rates then further difficulties will be encountered, such as clock feedthrough which causes an effect known as the *pedestal* — a jump in the voltage on the hold capacitor that occurs when the circuit switches from sample to hold. This can be eliminated if we move to a fully balanced architecture, such as a diode bridge circuit. Further discussion of this can be found in section 3.4.

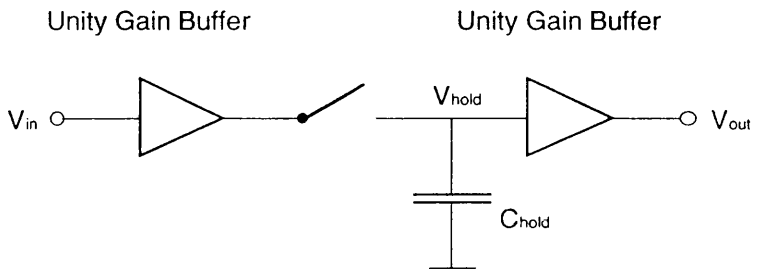


Fig 3.3 Buffered sample and hold circuit. This prevents discharging of C_{hold} through the output load, and provides a low impedance source to drive the sampling gate.

Some of the terminology used to describe the performance of sample and hold circuits is illustrated in Fig. 3.4, and a more complete definition can be found in appendix 2 and in [148].

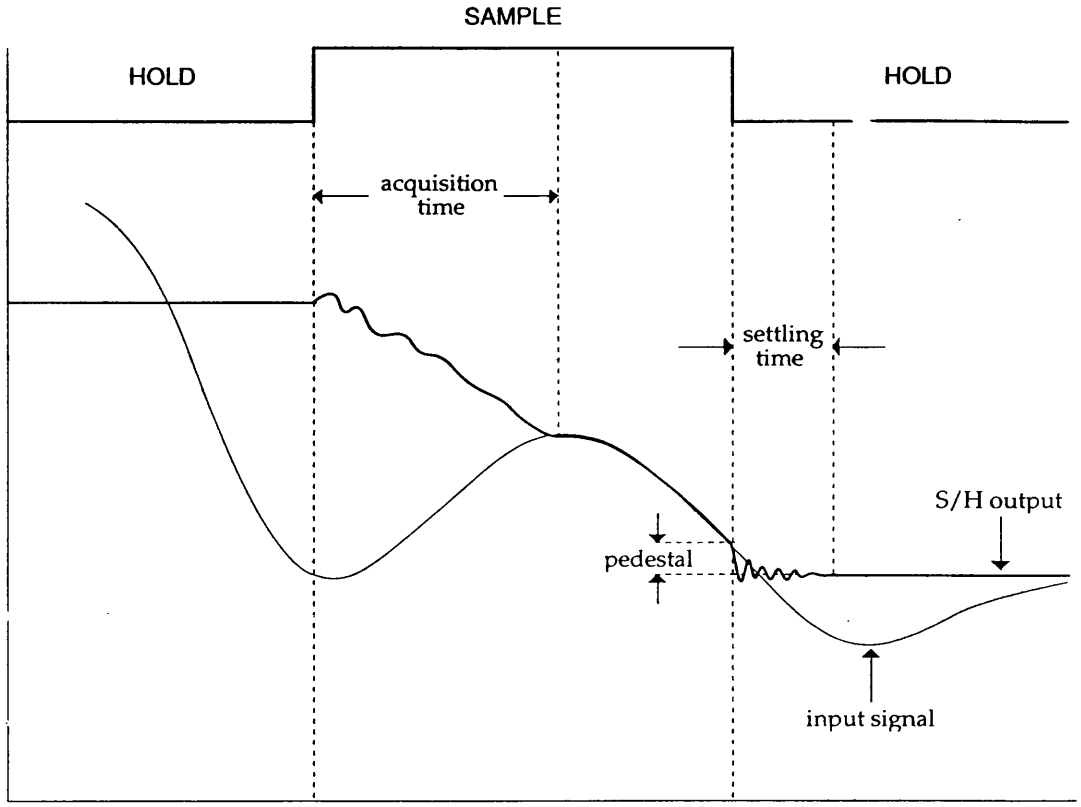


Fig 3.4 Common terminology used to describe the performance of S/H circuits. A more detailed account can be found in appendix 2 and in [148].

3.2 SERIES PHOTOCONDUCTIVE OS/H

Perhaps the simplest realisation of an OS/H consists of a photoconductive switch in series with a hold capacitor as shown in Fig. 3.5. As the MSM has photoconductive properties it can readily be used for this purpose. With zero illumination the resistance of the MSM will be high, corresponding to the switch being turned off, but under illumination by light of an appropriate wavelength electron-hole pairs will be generated, causing current flow, corresponding to a low resistance and the switch being turned on. This type of circuit was first proposed for wideband radar signal processing [142] and employs an optoelectronic sampling gate similar to those developed by D H Auston [36]. For simplicity we have assumed that the input signal derives from a low impedance (50Ω) source, so we can dispense with the input buffer shown in Fig. 3.5.

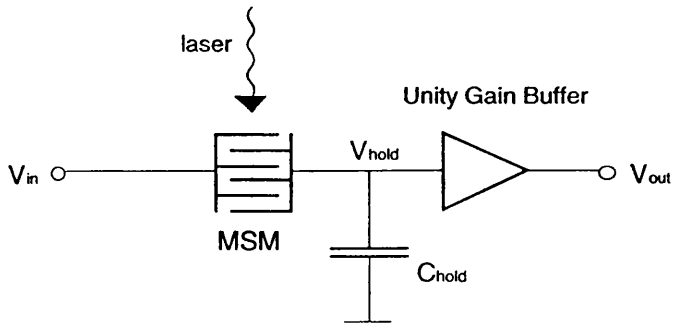


Fig 3.5 Series photoconductive optoelectronic sample and hold circuit.

The speed of such a circuit is limited by the turn-on time and the turn-off time. The turn-on time is determined by the $R_{on}C_{hold}$ time constant. A typical value of R_{on} is around 10kΩ, with an optical power of 5mW [31]. To prevent loss of charge, the capacitance of C_{hold} needs to be higher than the input capacitance of the buffer. A value of C_{hold} = 0.75pF is found to be appropriate for the buffer we will be using (section 3.6), giving an $R_{on}C_{hold}$ time constant of ~7.5ns - limiting the analogue bandwidth to a maximum of about 21MHz.

The maximum sample rate of the circuit is determined by both the acquisition time and the turn-off time. The acquisition time of a S/H circuit is defined as the minimum time required for the hold capacitor to charge to within a specified error band of the input signal. If we consider the worst theoretical case of an input square wave at full amplitude, we can put an upper limit on the acquisition time. During the sample phase we effectively have a low pass filter consisting of R_{on} and C_{hold}. If this is driven by a step input of amplitude V_{in}, the output voltage, V_{out}, after a time t is given by:

$$V_{out} = V_{in}\left[1 - e^{-t/R_{on}C_{hold}}\right] \tag{3.1}$$

Therefore, if we require n bits accuracy, the acquisition time, t_a, is given by:

$$t_a = -R_{on}C_{hold}\ln\left(\frac{1}{2^n}\right) \tag{3.2}$$

If we require a resolution of 8-bits, then the acquisition time t_a will be 42ns, which with a 50% duty cycle clock, would limit the sample rate to 12Ms/s.

The maximum sample rate of this circuit is further limited by the slowness of the turn-off transition. This problem arises from the fact that in the absence of a static electric field across the MSM, the transition is brought about by the recombination of the electron-hole pairs. This is a thermal process, having a time constant of a few milliseconds, and will decrease the sampling rate much further [82]. In spite of the limited performance, a circuit of this type has been fabricated because of its simplicity and as a comparison with the more complex circuits which follow.

3.3 SERIES MESFET SAMPLE AND HOLD CIRCUIT

The simplest all-electronic S/H circuit consists of a single FET operated in the triode (ie. linear) region as a series analogue switch of the type employed in switched capacitor networks [149]. Fig. 3.6 shows such a circuit.

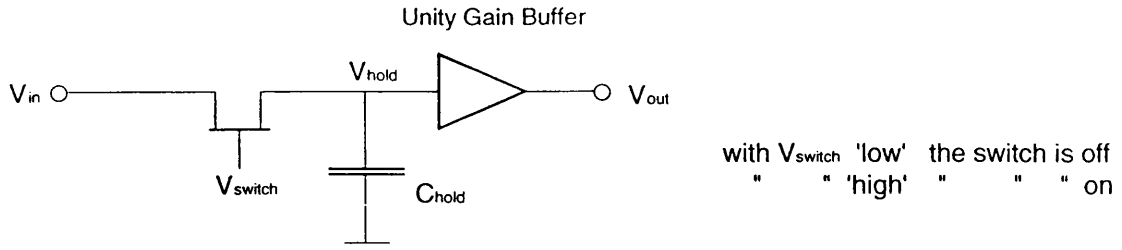


Fig 3.6 Simplest all-electronic sample and hold circuit.

The speed of this circuit is limited by the ON resistance of the switching FET, which is ~450Ω for a 20μm MESFET (eq. 3.5). With C_{hold} = 0.75pF the $R_{on}C_{hold}$ time constant will be ~340ps, which sets a limit on both the acquisition time and analogue bandwidth of the circuit.

To control this type of circuit optically the approach shown in Fig. 3.7 can be used. The pass transistor, *M1*, is turned on by switching its gate-source potential form a large negative value (i.e. more negative than the threshold voltage) to zero. This voltage transition is produced by passing the photocurrent, I_P, through the combination of a current source, I_{source}, and a shunt resistance, R_{source}. When I_p is less than I_{source}, the gate voltage of *M1* is close to V_{ss} and the device is turned off. When I_p exceeds Isource, the gate voltage rises rapidly until *M1* switches on.

Using this technique allows the separation of the functions of photodetection and switching, enabling the components representing both functional blocks to operate under more ideal conditions than is possible in the case of the Auston switch. In particular, the MSM is operated under an almost constant bias voltage, ensuring that it is fully depleted at all times. The advantages of this are that the device will be operating near the maximum quantum efficiency, and at the instant of turn-off the carriers will be swept away by the electric field rather than relying on the slow diffusion process observed in the Auston switch. We have seen (Fig. 2.2) that the electron drift-velocity in GaAs tends to a high-field value of ~$1x10^{11}$ μm/s, therefore, as the minimum finger gap of a F20 MSM is 4μm, we would expect a response time of around 40ps, compared with the millisecond response time of the thermal recombination process. Further benefits of this circuit are that the impedance of the current source can be made very high, ensuring that *M1* will be switched on and off by a relatively small change in photocurrent, and that the MSM does not need to turn fully on or off to activate the switch. The implication of this is that the circuit has some degree of immunity to the laser extinction ratio (a property of particular importance at high laser repetition rates) and also that the exact sampling instant can be controlled by adjusting the threshold at which the switching occurs.

There are, however, some problems with this circuit as it stands. Since the gate-source and gate-drain junctions of a MESFET are Schottky junctions, care must be taken to prevent these becoming forward biased. Failure to do this would cause the hold capacitor to be charged directly from the photocurrent, resulting in clock feedthrough and corruption of the output signal. A further problem, which is characteristic of unbalanced circuits, is that of parasitic clock feedthrough. In this circuit this is generated by the charging of the gate-source capacitance of *M1* from the hold capacitor, resulting in pedestal appearing on the output.

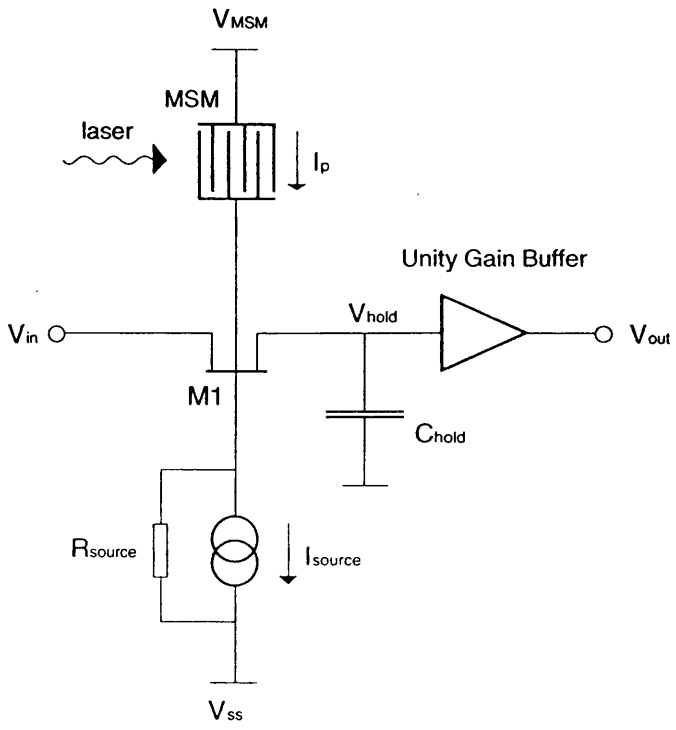


Fig 3.7 Optically controlled series MESFET S/H circuit.

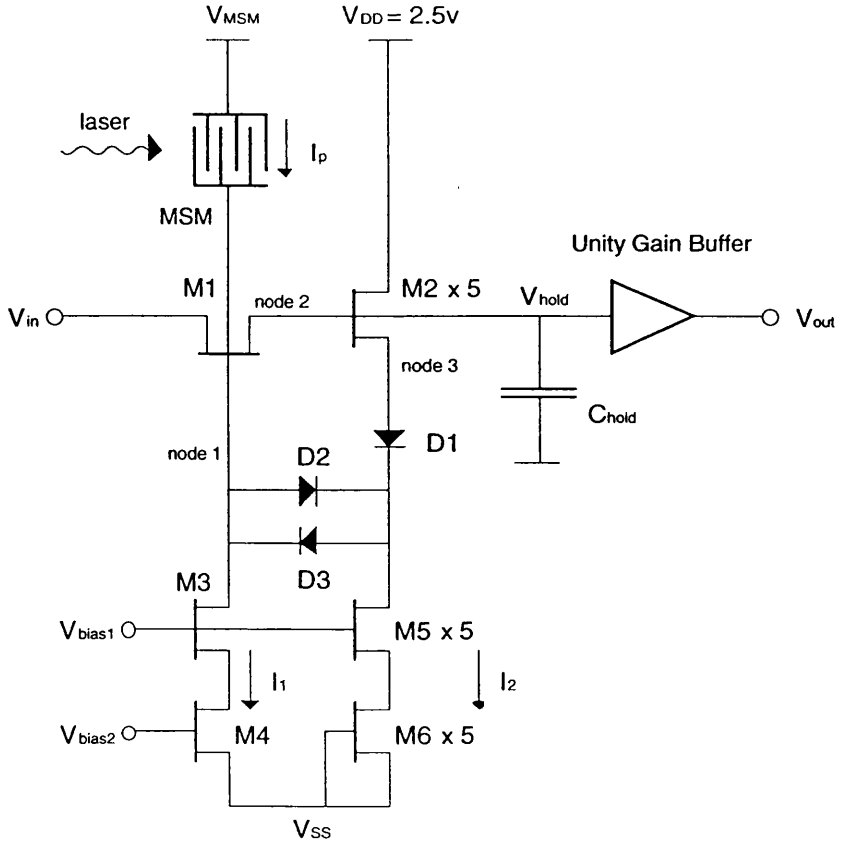


Fig 3.8 Series MESFET OS/H with diode clamping. The extra circuitry prevents gate conduction of *M1* and reduces pedestal.

To alleviate these difficulties the circuit shown in Fig. 3.8 was designed. The current-source/impedance combination is realised by the variable cascode current source of *M3* and *M4*. The impedance of such a source is about 41kΩ, (§ 3.5.2) which means that a photocurrent swing of only 25μA will be sufficient to turn *M1* on and off. The gate-source junction of *M1* is prevented from becoming forward biased by the source follower *M2* and the diodes *D1* and *D2*. The action of the source follower ensures that $V_{node2} \approx V_{node3}$. The back-to-back combination of diodes *D1* and *D2* ensures that the gate of *M1* cannot rise above V_{node3} (and hence V_{node2}) preventing gate conduction.

When the photocurrent I_p is turned off, the series combination of diodes *D1* and *D3* sets a lower limit on the gate voltage of *M1* of two diode drops (approximately –1.4V) below V_{node3}. By defining the turn-off voltage swing across C_{gs} with this diode clamp, it is made almost independent of the input signal level and consequently the pedestal appearing at the output is also independent of signal level. As a result, the pedestal has a minimal effect on the accuracy of the sample and hold process, resulting mainly in a small DC offset on the output voltage.

The source follower, *M2*, and its cascoded current source, *M5* and *M6*, each consist of 5 MESFETs connected in parallel. This has the effect of reducing the source impedance of *M2*, ensuring that the current through *D2* and *D3* is much smaller than that through *D1*, and hence providing a high quality voltage reference for the diode clamp circuit. The extra capacitance at the gate of *M2* is effectively absorbed into C_{hold}.

3.3.1 Detailed Analysis of Series MESFET Circuit

(i) Analogue bandwidth and acquisition time

When operating in the sample mode, the pass transistor circuit is effectively a first order low pass filter, with a time constant given by $R_{on}C_{hold}$. The *on* resistance of the FET in the linear region can be estimated from the Shichman-Hodges model [97]. The drain current in the linear region is given by:

$$I_D = \beta\left[2(V_{GS} - V_P)V_{DS} - V_{DS}^2\right](1 + \lambda V_{DS}) \qquad (3.3)$$

When the MESFET is switched on, $V_{GS} = 0$V, so

$$I_D = -\beta\left(2V_P V_{DS} + V_{DS}^2\right)\left(1+\lambda V_{DS}\right) \tag{3.4}$$

The conductance can be found by differentiating with respect to V_{DS}

$$\frac{\partial I_D}{\partial V_{DS}} = -\beta\left[3\lambda V_{DS}^2 + 2V_{DS}\left(1+2\lambda V_P\right) + 2V_P\right] \tag{3.5}$$

Assuming small signal operation around V_{DS} = 0V, the conductance = $-2\beta V_p$, so with β = 1.1mA/V^2, V_p = – 1V, we find R_{on} = 455Ω. With a fabricated hold capacitor of 0.75pF, this value of R_{on} gives a – 3dB bandwidth of 466MHz. The measured results presented in chapter 5 clearly support this estimate of MESFET *on* resistance.

The acquisition time t_a of this circuit can be found in a similar way to that of the Auston switch. From (3.2), we can see that for 8-bits accuracy, t_a = 1.89ns, which with a 50% duty cycle clock would allow a maximum sample rate of 265Ms/s

(ii) Pedestal

In section 3.3 we described how the series MESFET S/H was designed to minimise the pedestal by restricting the voltage swing of the gate of the switching MESFET. The remaining pedestal will consist of an invariant component and a small signal-dependant component. The magnitude of the invariant component of the pedestal can be estimated by considering the simplified circuit shown in Fig. 3.9, in which the cascoded current sources are replaced with ideal current sources, and the diode clamp by an ideal voltage level shift.

When the circuit switches from sample to hold the voltage level shift changes from 0V to about – 1.4V. A charge Q will therefore be moved from C_{hold} to C_{gs}, where

$$Q = C_{gs}V_{shift} = -C_{hold}V_{ped} \tag{3.6}$$

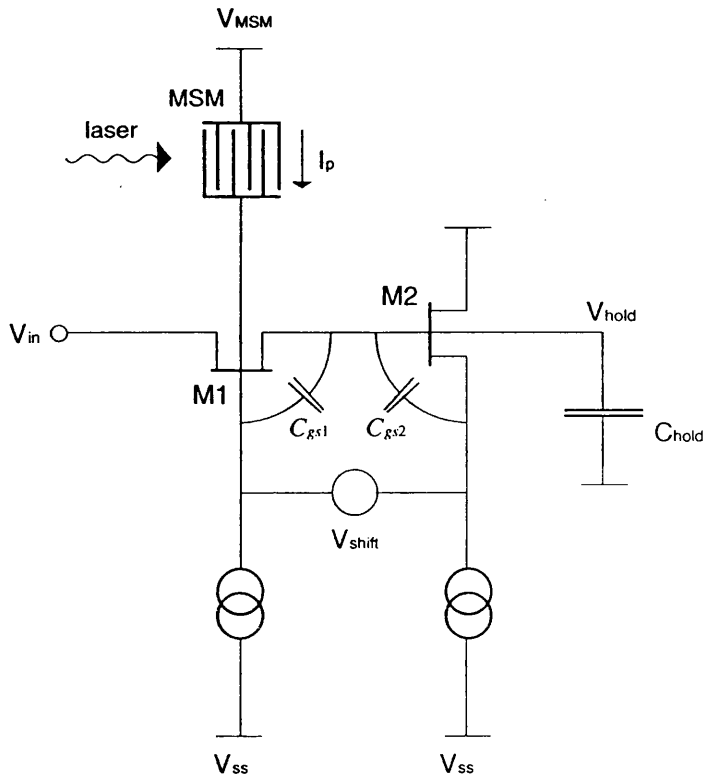


Fig 3.9 Simplified circuit for calculation of pedestal.

Therefore the invariant component of the pedestal, V_{ped}, is given by:

$$V_{ped} = \frac{-C_{gs1}V_{shift}}{C_{hold} + C_{gs2}} \tag{3.7}$$

which evaluates to ~10mV, assuming C_{gs1} is fully depleted (section 2.2.1(ii)).

The fact that the parasitic capacitances are depletion capacitances will tend to increase this value (as C_{gs1} will not be depleted initially), and the non-linear behaviour will lead to harmonic distortion. The magnitude of these effects are, however, difficult to estimate and are instead addressed by means of HSPICE simulations in chapter 5.

The input dependent component of the pedestal arises because the operating point of the circuit varies with input level. This means that the gain of the follower formed by *M2* and the voltage drop across the diodes will depend on the input signal to a certain extent. The magnitude of this effect is difficult to calculate, but from HSPICE simulations we can see that the *on* to *off* voltage swing across C_{gs} varies from 1.278V to 1.281V as the input varies from – 0.5V to

+ 0.5V. This will cause a difference in pedestal of around 1mV.

(iii) Sampling Time Adjustment

The gate of the switching transistor *M1* is controlled by the combination of the MSM and the cascoded current source *M3* and *M4*. As the impedance of this source is about 41kΩ, a photocurrent swing of only 25μA is needed to switch *M1* from fully *off* (V_{gs} = –1V) to fully *on* (V_{gs} = 0V). This switching occurs when the photocurrent is equal to the saturation current of the source. As the photocurrent pulse has a finite rise-time, the switching instant can be controlled by adjusting the saturation current of the cascoded source by means of the external bias voltage. The amount of adjustment available depends, therefore, on the rise-time of the photocurrent pulse. If the MSM is driven from a laser source with a very fast rise-time, the intrinsic rise-time of the MSM will determine the photocurrent rise-time, which typically has a value of 50ps [106]. In this demonstration circuit the laser was driven by a pulse generator with a rise-time of 200ps, allowing even more adjustment. This full range of adjustment cannot be used as the minimum source-current has to be sufficient to ensure that the switching transistor is fully turned-off during the hold phase.

3.4 DIODE BRIDGE SAMPLE AND HOLD CIRCUIT

3.4.1 Principle of the Current-Steering Diode-Bridge S/H Circuit

The series MESFET OS/H circuit proves to be an elegant solution to the problem of constructing an optically triggered sample and hold circuit. However, the ultimate performance of this circuit is limited by the restricted analogue bandwidth and by the pedestal. A circuit which eases these difficulties is the current steering diode bridge, the essential components of which are shown in Fig. 3.10. This circuit is frequently used in all-electronic sample and hold circuits and ADCs [25, 150,151].

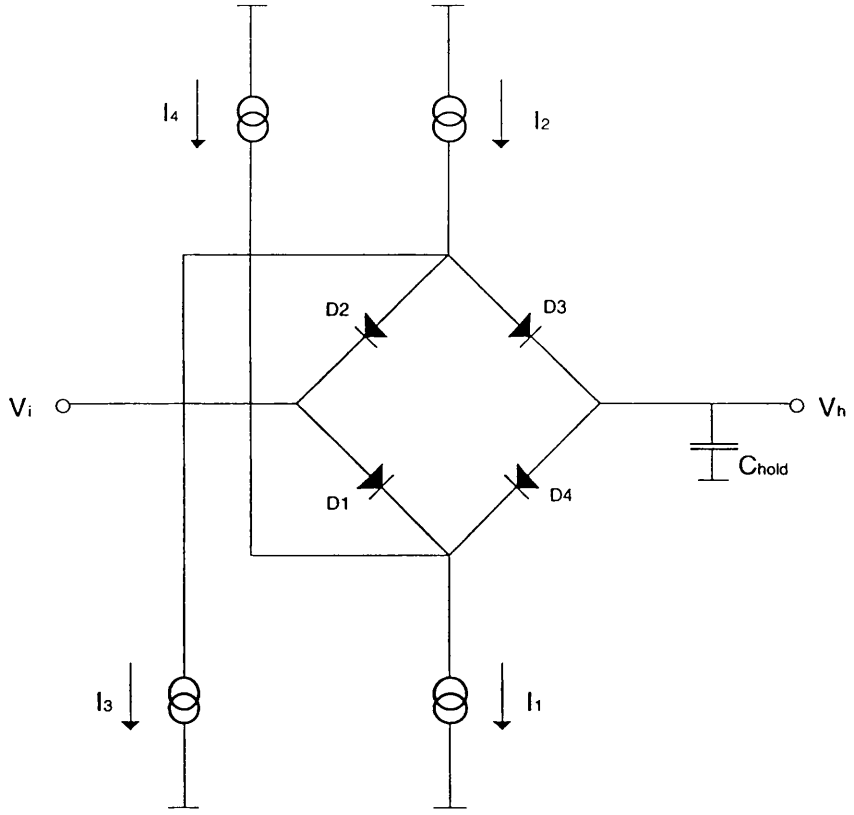


Fig 3.10 Simple diode bridge S/H circuit.

The simplest realisation of the circuit consists of four Schottky diodes arranged in the manner of a rectifying bridge, driven by two pairs of complementary current sources. During the sample period the current sources I_1 and I_2 are turned *on*, with I_3 and I_4 turned *off*. This drives current down through the bridge, turning on the diodes *D1-D4*. If the voltage on the hold capacitor V_h is larger than the signal voltage V_i, the diodes *D2* and *D4* will be

more conductive than diodes *D1* and *D3*. Therefore a larger current will flow through diode *D4* than through diode *D3*, discharging C_h and reducing V_h. If V_h is smaller than V_i this process will be reversed, with excess current flowing through *D3*, increasing V_h. This charging and discharging process continues in the sample period until $V_h = V_i$. During the hold period of the cycle the current sources I_1 and I_2 are turned *off*, with I_3 and I_4 turned *on*. This reverse biases the diodes and effectively disconnects the input source from the hold capacitor. The voltage on the hold capacitor is therefore maintained at a constant value during this phase.

As the hold capacitor is now charged by a constant current source the restrictive *RC* nature of the series MESFET and Auston switch sample and hold circuits is avoided. Instead the circuit is slew-rate limited with a slew rate *S* given by:

$$S = \frac{\partial V}{\partial t} = \frac{I}{C_h} \tag{3.8}$$

where *I* is the current available to charge the hold capacitor. If we assume a current of 1mA and a hold capacitor of 0.75pF the slew rate will be 1.3V/ns. Therefore with the worst case of a 1V input square wave, the circuit will acquire the signal in ~0.75ns — compared to 1.89ns for the series MESFET circuit to acquire the signal to within one LSB (§ 3.3.1(i)). This very fast slew rate will also be reflected in a much increased analogue bandwidth for this circuit.

In common with the series MESFET circuit, this circuit suffers from pedestal. A major cause of the pedestal in this circuit is the capacitance of the two bridge diodes connected to the hold capacitor. As the bridge is switched off, the voltage across these two diodes changes from an *on* bias of about 0.7V to an indeterminate *off* bias. An amount of charge will therefore flow onto the hold capacitor from one of the diodes to which it is connected, and a corresponding (but not necessarily identical) charge will flow from the hold capacitor onto the other diode. The magnitude of the reverse bias voltages will depend on the reverse bias characteristics of the diodes, the impedance of the current sources and the voltage on the hold capacitor. If the voltage on the hold capacitor is non-zero, these reverse bias voltages will be asymmetrical and the

charging/discharging of the diodes will be unequal, resulting in pedestal. Furthermore, since the diode capacitances are highly non-linear, significant harmonic distortion of the signal will also occur. To avoid this problem a 'bootstrapping' technique is employed [25], in which a further four diodes are added to define the total reverse bias voltage across the bridge. To ensure that this is symmetrical at the instant of turn-off, the centre of this chain is forced to be equal to the voltage on the hold capacitor by means of two unity gain buffers. This improved circuit is shown in Fig. 3.11.

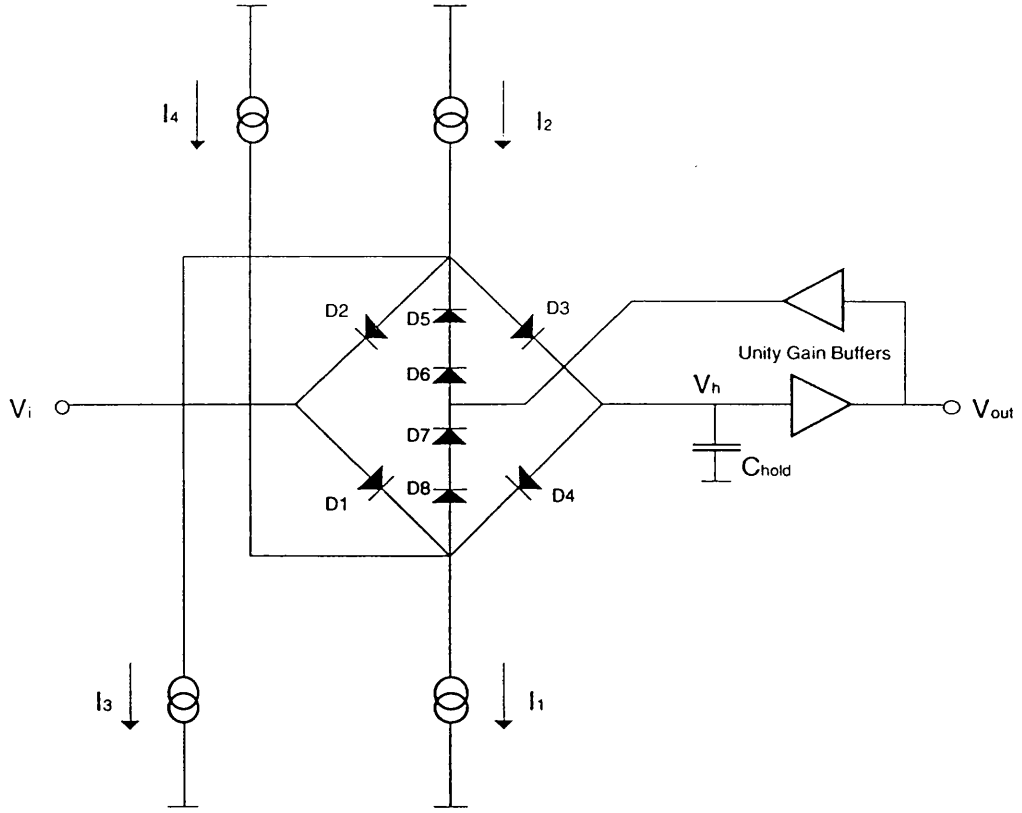


Fig 3.11 Bootstrapped diode bridge S/H circuit. The bootstrapping reduces pedestal.

3.4.2 Optically Controlled Diode Bridge S/H

The simplest way to control a circuit of this type optically is to replace the four current sources with optoelectronic switches, using the photocurrent to control the switching of the bridge . This approach, with some modification , is described in [31]. This circuit, which is shown in Fig. 3.12, is a discrete component model which uses four MSM photodetectors fabricated on an InP

substrate connected to a bridge consisting of eight Schottky diodes. Bootstrapping is provided by two 350MHz unity gain amplifiers. The four MSM switches are configured as two complimentary pairs biased at +10V (*S2* and *S4*) and -10V (*S1* and *S3*), thus maintaining a large bias voltage and eliminating slow recombination effects.

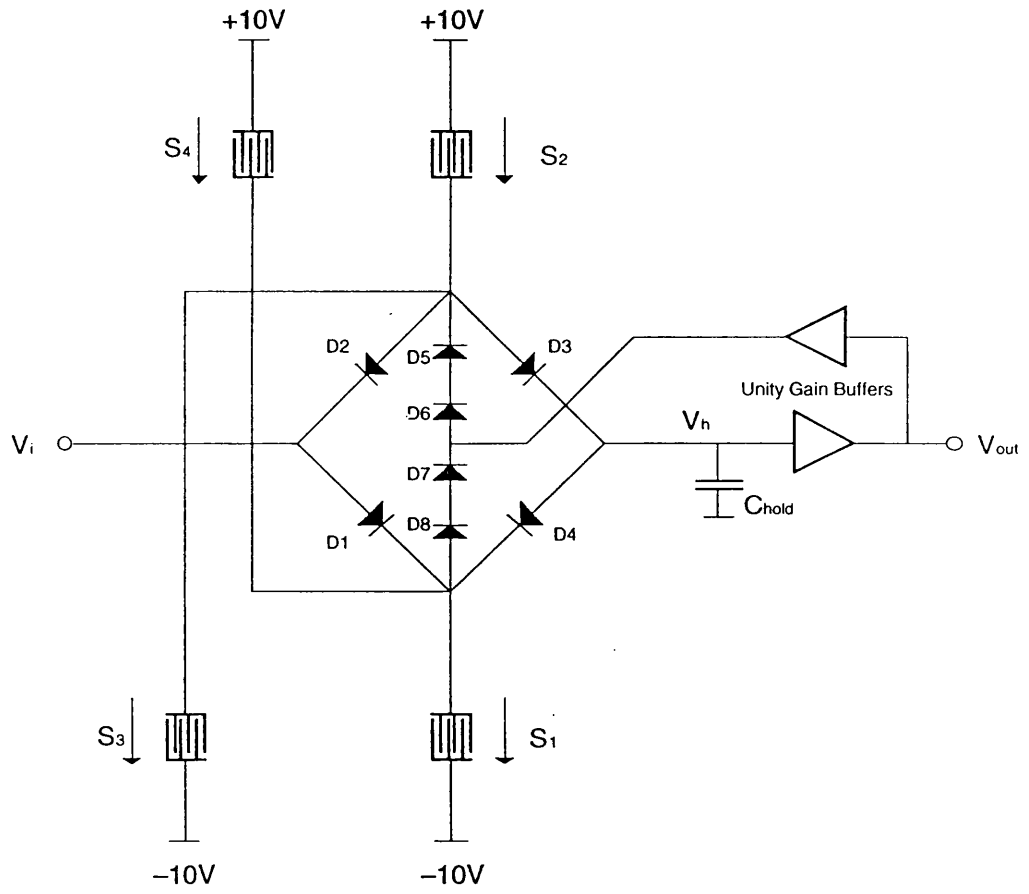


Fig 3.12 Optically controlled diode bridge sample and hold (OS/H).

Sampling of the input is accomplished by simultaneously illuminating switches *S1* and *S2*, which drives current through the diodes *D1-D4* and therefore switches on the bridge. In order to hold the voltage on C_{hold}, *S3* and *S4* are illuminated with a delayed laser pulse while the illumination on *S1* and *S2* is removed. This reverse biases diodes *D1-D4* and effectively disconnects the input from C_{hold}. The four laser pulses required for this circuit are generated from a single laser pulse which is power divided and coupled into four fibre optic delay lines. As this system was a discrete model with

associated parasitic capacitance, impedance mismatch and electrical delays, the maximum sample rate was 20Ms/s. Although these effects can be substantially reduced by means of integration, the circuit still requires four independent optical drives. In a practical situation this would be very difficult to implement as the fibre splicing, alignment, length adjustment, maintenance and so-on would be very difficult and labour intensive. One must also remember that in an interleaved n-path system these difficulties would be multiplied many times.

3.4.3 Fully Integrated Diode Bridge OS/H

For this project a new current-steering diode-bridge circuit was developed which is fully integrated and requires only a single optical address. In common with the series MESFET OS/H, the diode bridge circuit is fabricated using GaAs MESFET technology, with MSM interdigital capacitors operating as the photodetector element.

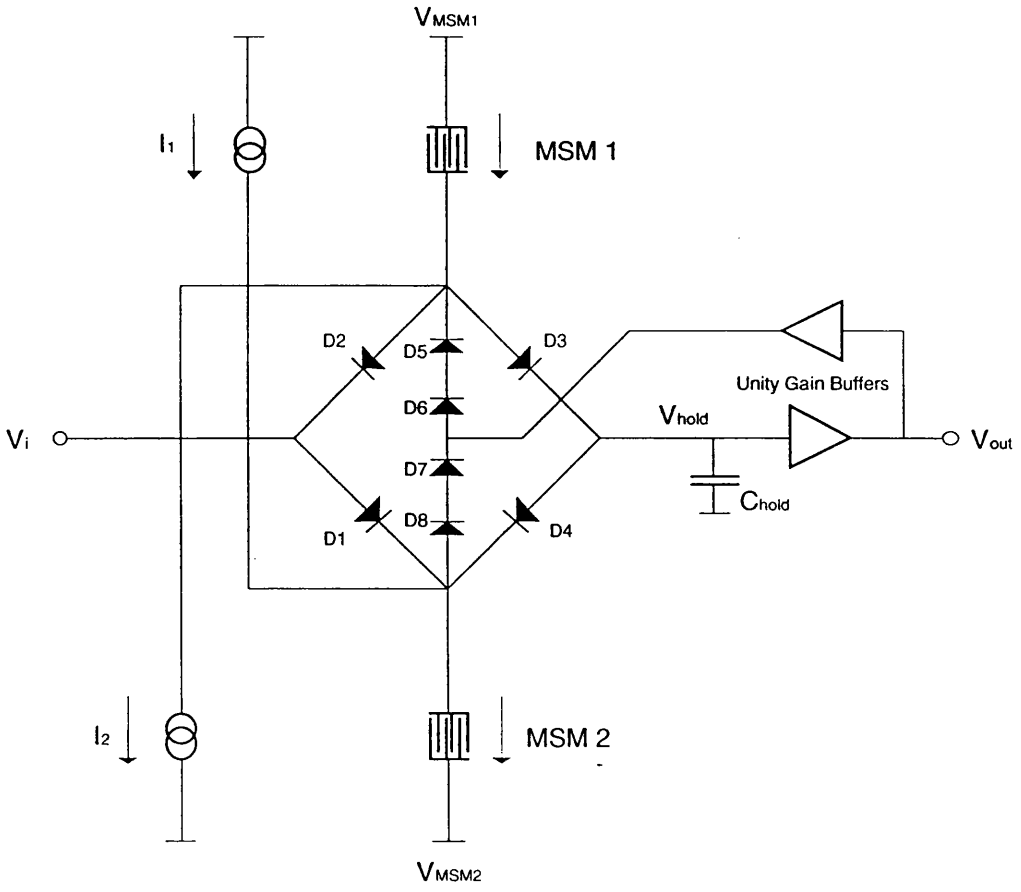


Fig 3.13 Diode bridge OS/H requiring a single optical address.

To reduce the number of photodetectors, we have replaced those which facilitate the hold function with fixed current sources. The two remaining MSMs are required to be illuminated simultaneously and can therefore be addressed with a single laser spot, providing the geometry is appropriate. This modified circuit is shown in Fig. 3.13.

With the MSMs turned off, the fixed sources I_1 and I_2 provide sufficient current to reverse bias the diodes *D1-D4*, causing the output voltage to be held. When the MSMs are illuminated, the fixed current sources draw a proportion of the photocurrent, any extra photocurrent being driven through diodes *D1-D4* causing the bridge to be turned on. Therefore the photocurrent has to be larger than the current generated by the sources I_1 and I_2. Although this system reduces the efficiency somewhat, with only a part of the photocurrent being available to charge the hold capacitor, the removal of the requirement for the holding MSMs significantly increases its practicality.

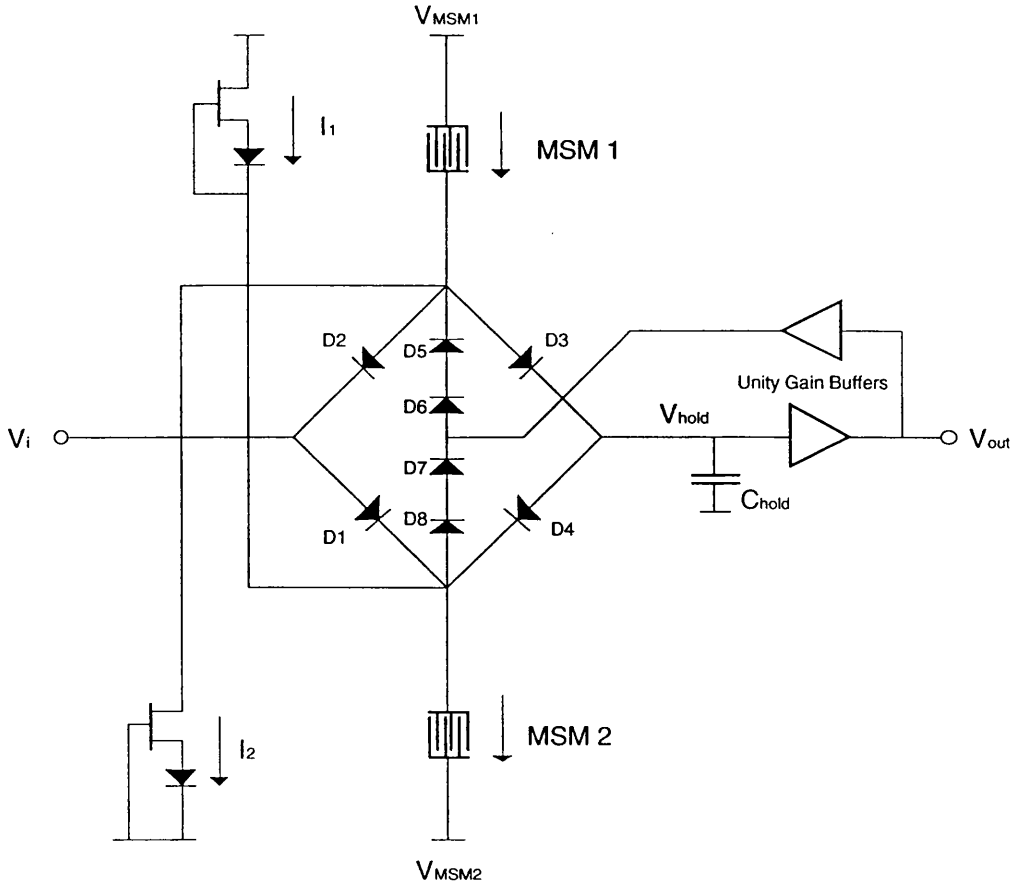


Fig 3.14 Diode bridge OS/H with fixed current sources.

One of the problems of the diode bridge circuit is the need for a negative current source. This current source needs to supply a current which is substantially less than the photocurrent, otherwise the bridge will not switch on, but still large enough to reverse-bias the bridge in the hold phase. Two methods have been used for this, one with adjustable current sources and one with fixed current sources. A detailed description of these sources can be found in section 3.5. The two complete diode bridge circuits are shown in Figs. 3.14 and 3.15.

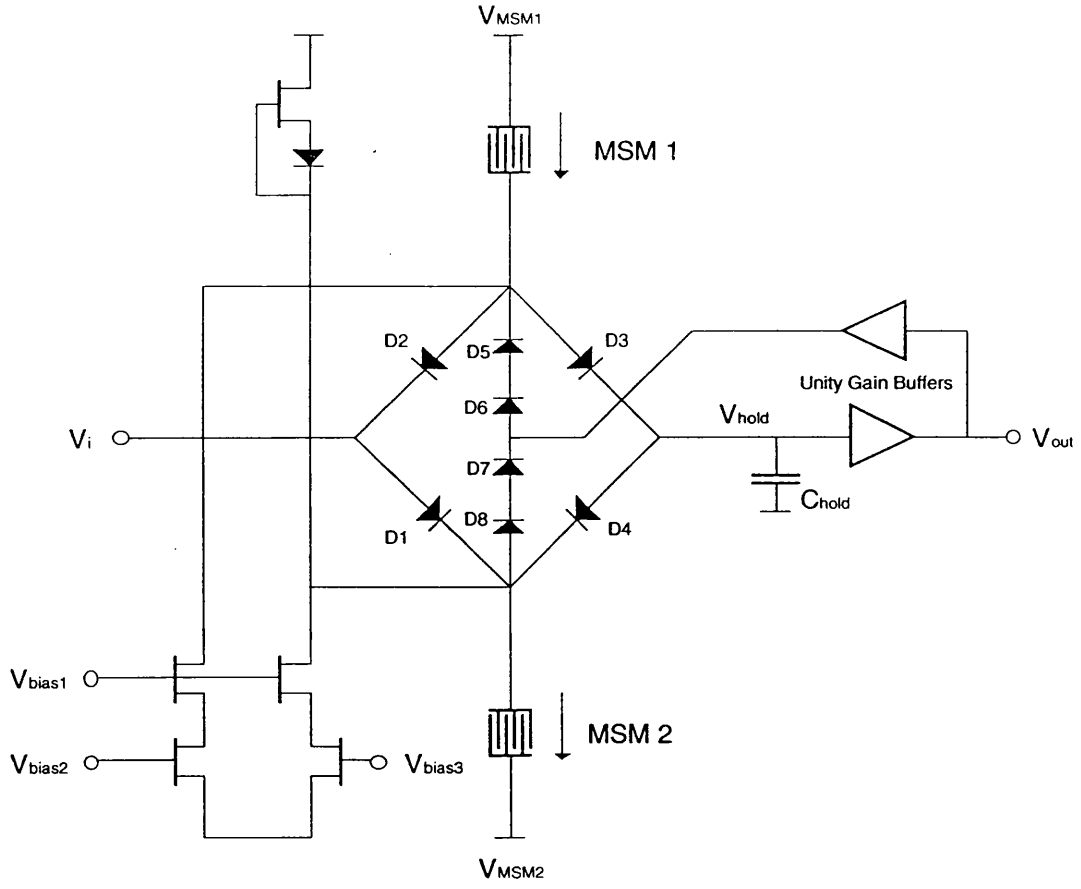


Fig 3.15 Diode bridge OS/H with tuneable current sources. This allows optimisation of the circuit for a range of photocurrents.

3.4.4 Detailed Description of the Diode Bridge Circuit

(i) Analogue Bandwidth

Unlike the Auston switch and series MESFET circuits, the hold capacitor of the diode bridge circuit is charged by a constant current source, rather than by the

input voltage source via a series on resistance. This means the speed of the circuit is slew rate limited, rather than being determined by an RC time constant. If the fixed current sources of Fig. 3.14 generate a current of I_s, and the photocurrent is I_p, then the excess current available to charge C_{hold}, I_c, is equal to $I_p - I_s$. The maximum slew rate, S, therefore becomes:

$$\frac{\partial V}{\partial t} = \frac{I_c}{C_{hold}} = \frac{I_p - I_s}{C_{hold}} \tag{3.9}$$

So, for typical values of I_s = 0.3mA and I_p = 1mA, the slew rate will be 0.933V/ns. To estimate the analogue bandwidth we can calculate the time it takes for the circuit to slew $1/\sqrt{2}$ the value of a given input amplitude. For example, if the designed input amplitude is A volts, then the time T to slew a total of $2A/\sqrt{2}$ is given by:

$$T = \frac{2A}{S\sqrt{2}} \tag{3.10}$$

where S is the circuit slew rate. This will be the duration of one half cycle of the -3dB frequency, so with the previously used values we find that $f_{\text{-3dB}}$ = 660MHz. This is compared to the -3dB bandwidth of 470MHz available with the series MESFET circuit. Also, the slew rate of this circuit is proportional the magnitude of the excess current I_c, so by increasing the incident laser power the analogue bandwidth can be substantially increased.

We have until now assumed that the current available to charge C_{hold} is constant. However, when V_{in} is close to V_{out} this will not be the case. If we consider the bridge in the sample mode and remove the bootstrap feedback for simplification, the circuit reduces to Fig. 3.16. Assuming the current-voltage relationships of the diodes follow an exponential law, the current through diode *D1* will be given by:

$$I_1 = I_s \text{Exp}\left(\frac{V_1 - V_2}{V_r}\right) \tag{3.11}$$

where $V_r = kT/q$. Similar expressions can be written for each of the other diodes.

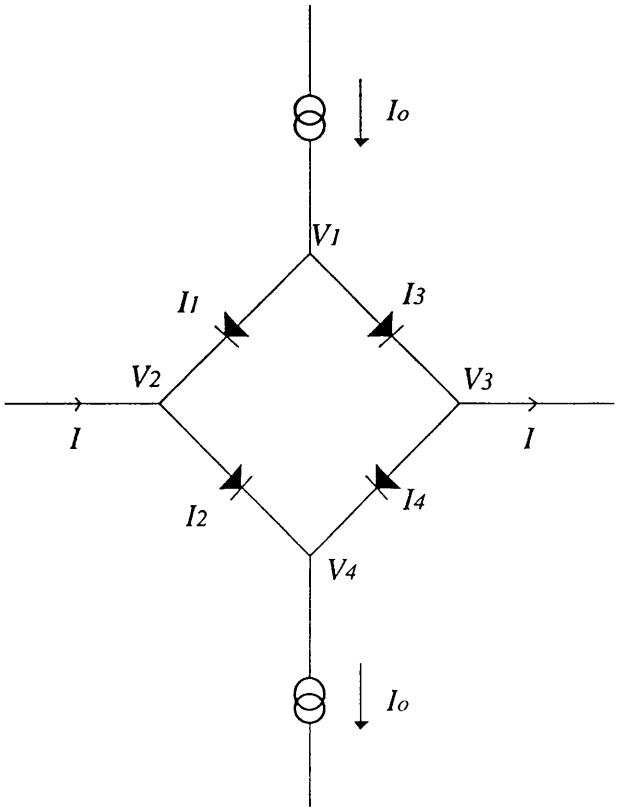


Fig 3.16 Simplified diode bridge S/H for circuit analysis.

Now we can see that:

$$I_o = I_1 + I_3 = I_2 + I_4 \tag{3.12}$$

$$I = I_2 - I_1 = I_3 - I_4 \tag{3.13}$$

So, combining equations 3.11, 3.12 and 3.13 and eliminating the currents I_1 to I_4 we find:

$$I = \frac{I_o\left(e^{V_2/V_r} - e^{V_3/V_r}\right)}{\left(e^{V_2/V_r} + e^{V_3/V_r}\right)} \tag{3.14}$$

Now, as the hyperbolic tangent function is defined as:

$$\tanh(x) = \frac{e^x - e^{-x}}{e^x + e^{-x}} \tag{3.15}$$

we can re-write this as:

$$I = I_o \tanh\left(\frac{V_2 - V_3}{2V_r}\right) = I_o \tanh\left(\frac{V_{in} - V_{out}}{2V_r}\right) \tag{3.16}$$

This equation is plotted in Fig. 3.17. From this we can see that for $V_2 - V_3 \leq 2V_r$ (= 51.8mV) the current varies in an approximately linear manner with voltage, so the circuit is effectively resistive in this region, with a resistance R_l given by $R_l = 2V_r/I_o = 74\Omega$ for $I_o = 0.7$mA. When $V_2 - V_3 > 2V_r$ the current is constant at I_o. The consequence of this hyperbolic tangential charging is to reduce the slew rate when $V2 \approx V3$. This will cause a slight reduction in analogue bandwidth and an increase in acquisition time.

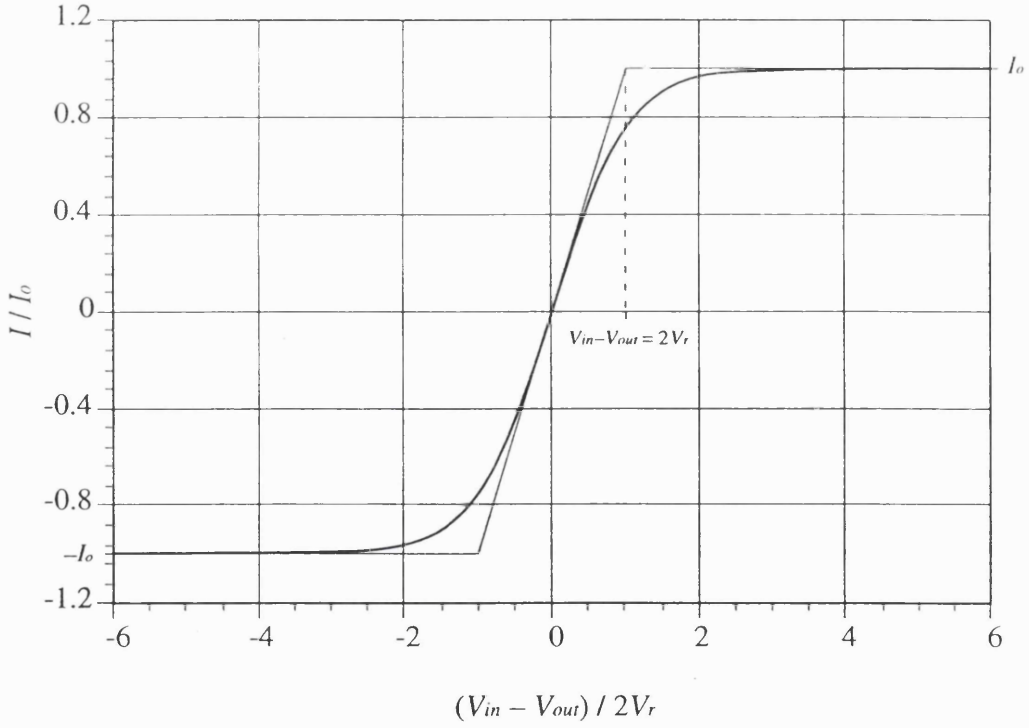


Fig 3.17 I–V characteristic of the diode bridge. This is a plot of equation (3.16).

(ii) Acquisition Time

We have seen that the charging current is a hyperbolic tangential function of the voltage across the bridge. The rate of change in voltage on the hold capacitor is therefore given by:

$$C_h \frac{\partial V_{out}}{\partial t} = I = I_o \tanh\left(\frac{V_{in} - V_{out}}{2V_r}\right) \tag{3.17}$$

To find V_{out}(t) requires a solution to this differential equation. However, as the expression involves transcendental functions an analytical solution cannot be found. A simpler technique is to split the function into regions of constant current ($V_{in} - V_{out} > 2V_r$) and linear RC charging ($V_{in} - V_{out} \leq 2V_r$).

During constant current charging we have:

$$\frac{\partial V_{out}}{\partial t} = \frac{I_o}{C_h} \tag{3.18}$$

This continues until the RC region is reached and exponential charging takes over. If we refer to this output voltage as V_c, the output voltage at a time t after this point will be given by:

$$V_{out} = V_c + (V_{in} - V_c)\left[1 - e^{-t/R_l C_h}\right] \tag{3.19}$$

where R_l is the effective resistance in the linear RC region. This charging characteristic is shown in Fig. 3.18.

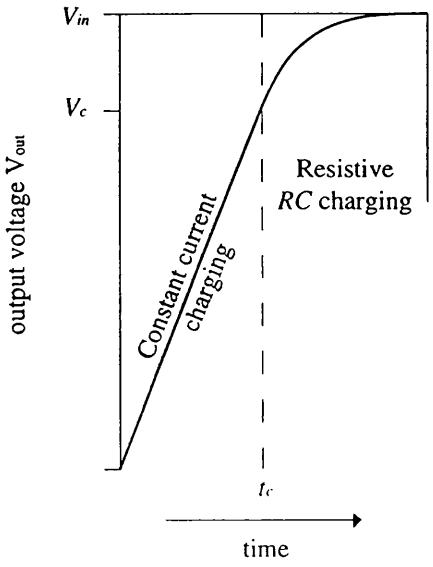


Fig 3.18 Response of the diode bridge S/H to a step input. The initial linear charging becomes exponential after a time t_c.

To find the acquisition time we can consider applying a step input voltage to the circuit from 0V to Vin. The time t_c for the output to reach V_c is given by:

$$t_c = \frac{V_c C_h}{I_o} \tag{3.20}$$

The remaining portion of the acquisition is an exponential rise, so we can only specify the time it takes for the circuit to settle within a specified band of the input voltage. For n-bits accuracy V_{out} is given by:

$$V_{out} = \frac{\left(2^n - 1\right)}{2^n} V_{in} \tag{3.21}$$

So the time, t_l taken during the linear RC phase for the output voltage to reach this level can be found by combining equations 3.20 and 3.21

$$t_l = -R_l C_h \ln\left[\frac{V_{in}}{2^n (V_{in} - V_c)}\right] \tag{3.22}$$

The total acquisition time, $t_a = t_c + t_l$

$$t_a = \frac{V_c C_h}{I_o} - R_l C_h \ln\left[\frac{V_{in}}{2^n (V_{in} - V_c)}\right] \tag{3.23}$$

If V_{in} = 1V and I_o = 0.7mA we find the total acquisition time, t_a = 1.16ns.

(iii) Pedestal

The pedestal is caused by the unequal charging/discharging of the capacitors connected to the hold capacitor, but can be eliminated by using bootstrap feedback. To estimate the magnitude of the pedestal when the bootstrap feedback circuitry is operating we can consider the following half circuit (Fig. 3.19).

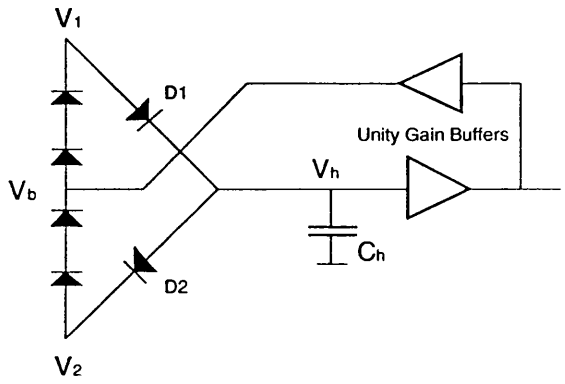


Fig 3.19 Diode bridge half-circuit for calculation of pedestal.

The voltage V_b at the centre of the bootstrap diode chain is given by:

$$V_b = G^2 V_h \tag{3.24}$$

where V_h is the voltage on the hold capacitor and G is the gain of the feedback buffers. If we assume that the diode voltage drop is fixed at 0.7V we can see that in the sample phase, the voltage at V_1 is $V_h + 0.7\text{V}$ and at V_2 is $V_h - 0.7\text{V}$. In the hold phase the voltages at V_1 and V_2 respectively are $V_b - 1.4\text{V}$ and $V_b + 1.4\text{V}$. As the circuit switches from sample to hold, the voltage swing across diode *D1* is therefore :

$$V_{S1} = V_{1(off)} - V_{1(on)} = V_h\left(G^2 - 1\right) - 2.1 \tag{3.25}$$

and similarly, the voltage swing across *D2* is:

$$V_{S2} = V_{2(off)} - V_{2(on)} = V_h\left(G^2 - 1\right) + 2.1 \tag{3.26}$$

If the capacitance of each diode when switched off is C_{off}, then the charge flowing onto C_h due to diode *D1* will be $Q_1 = V_{S1}C_{off}$, and similarly the charge due to diode *D2* will be $Q_2 = V_{S2}C_{off}$. The total change in charge Q_h on C_h will therefore be:

$$Q_h = Q_1 + Q_2 = C_{off}\left(V_{S1} + V_{S2}\right) = 2C_{off}V_h\left(G^2 - 1\right) \tag{3.27}$$

This will generate a pedestal V_{ped} of:

$$V_{ped} = \frac{2C_{off}V_h}{C_h}\left(G^2 - 1\right) \tag{3.28}$$

If we assume a typical buffer gain of 0.994 (derived from measured results, § 5.1.1(i)) and fully depleted parasitic capacitances (§ 2.2.1(ii)) then the pedestal will vary from +0.1mV to –0.1mV as the input varies from –0.5V to +0.5V.

(iv) Sampling Time Adjustment

As with the series MESFET OS/H, the instant at which the diode bridge OS/H switches from sample to hold depends on the ratio of photocurrent to holding current. Thus if this ratio can be adjusted, the sample time can be varied, and correction for timing interval errors can be performed. The two diode bridge circuits differ in the manner in which this can be performed. The circuit shown in Fig. 3.15 has fully adjustable current sources, and therefore this ratio can be adjusted directly, although this variation will be necessarily small as the available current range is only about 200µA. In contrast, the circuit shown in Fig. 3.14 uses the diode biased current source which cannot be adjusted, so to vary the sampling instant the current ratio requires some other means of control. One possible way of achieving this is to vary the MSM bias voltage, thus varying the photocurrent. Although this will have some effect, any variation in current ratio will be quite small as the MSM acts as a high impedance source. Nonetheless, a useful variation in sampling instant can be obtained, as is demonstrated by the simulations in section 5.2.3(vi).

3.5 CURRENT SOURCES

In chapter 2 we saw that the carrier mobility of n-type GaAs can be as high as 8500 cm^2/V-s, while that of p-type GaAs is only 400 cm^2/V-s. For this reason p-type doping is not generally offered with GaAs foundry processes, and we are therefore restricted to n channel FETs. This causes serious problems in the design of high quality negative current sources [81]. The definition of positive and negative current sources is illustrated in Fig. 3.20.

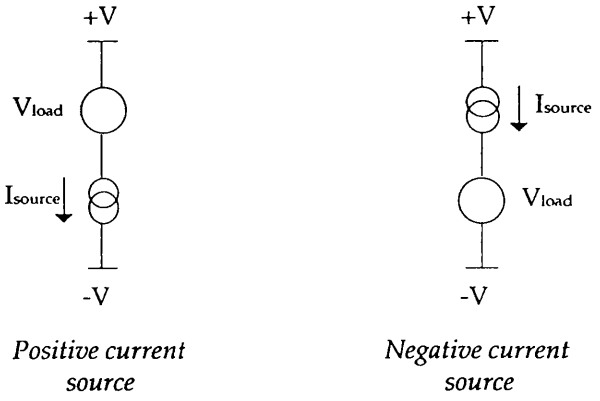


Fig 3.20 Definition of positive and negative current sources.

3.5.1 Simple Current Source

The simplest current source possible is just a FET with the gate and source connected together (Fig. 3.21). The operation of a simple current source such as this is described by the $V_{gs} = 0$ curve of the MESFET I-V characteristics, Fig. 2.9.

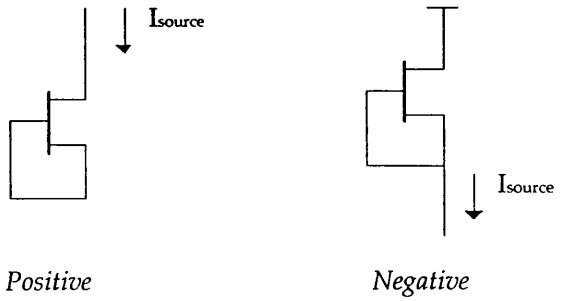


Fig 3.21 Simple MESFET current sources.

We can see that the current changes quite significantly with V_{DS}, corresponding to a high output conductance. The output conductance can be calculated quite simply:

We have from chapter 2:

$$i_d = g_m v_{gs} + g_o v_{ds} \tag{3.29}$$

but as $v_{gs} = 0$, $i_d = g_o v_{ds}$ and so the output conductance is g_o.

For the 20μm FET g_o = 300μS, which corresponds to an output impedance of 3.3kΩ. This method can be used for making both negative and positive current sources.

3.5.2 Cascoded Current Source

In order to reduce the output conductance we need to reduce the change in V_{DS} with I_D. This can be done by cascoding:

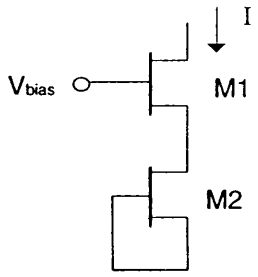


Fig 3.22 Cascoded current source.

The drain of *M2* is held at an almost constant voltage by V_{bias}. This increases the output resistance to

$$g_{out} = \frac{g_o^2}{g_m + 2g_o} \approx \frac{g_o^2}{g_m} = 24\mu S \text{ for the } 20\mu m \text{ MESFET.} \tag{3.30}$$

Unfortunately this technique cannot be used for negative sources (Fig 3.23):

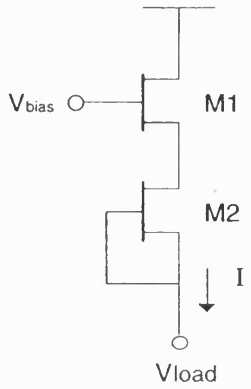


Fig 3.23 Cascoded current source used as negative source. In this case V_{DS} of *M2* is not constant, so the output conductance is simply g_o.

In section 3.4 a diode bridge OS/H was described. This circuit requires both positive and negative sources which supply a current smaller than the photocurrent generated by the photodetectors. From measurements made on MSMs it was found that a photocurrent of ~1mA could be generated. The current from the fixed sources needs to be less that this, but still sufficient to switch the bridge off. With a 20µm F20 MESFET, I_{DSS} = 1.1mA, so at a typical operating point of V_{DS} = 2.5v a simple current source will supply ~1.85mA. The current generated by a positive cascoded current source (Fig. 3.22) can be reduced by simply pinning out the gate of the lower FET, but unfortunately this is not possible with a negative source.

3.5.3 Diode Biased Current Source

A technique which can be used to reduce the current produced by the simple current source is to place a diode in series with the FET source, as shown in Fig. 3.24.

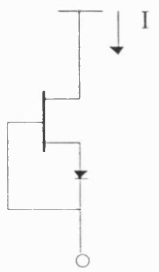


Fig 3.24 Diode biased current source.

This source will supply around 300μA. Assuming that the voltage drop across the diode is constant, the output conductance of this source is given by g_o. However, because the operating point has changed ($V_{gs} \approx -0.7$v), g_o will now be much lower (2.10), giving an output conductance of ~30μS to 50μS (corresponding to an impedance of ~20kΩ to 30kΩ), depending on the exact voltage drop across the diode. This type of current source has been used with some success for gain enhancement in GaAs amplifiers [152].

There are, however, problems associated with this source. Firstly, the current relies critically on the diode voltage drop. This has not as yet been modelled accurately. Secondly, the FET is operating away from I_{DSS} – ie away from the area of the most accurate modelling, and finally, the threshold voltage (V_P) of a FET is subject to fabrication errors. This will cause large changes in the current.

3.5.4 Tuneable Negative Current Sources

The diode biased current source is useful for supplying currents lower than I_{DSS} but this current cannot be controlled, and is not easily predicted. Ideally we would like to use fully tuneable current sources for the diode bridge circuit. One method of tuning is to sink a fraction of the current with a positive source (Fig. 3.25).

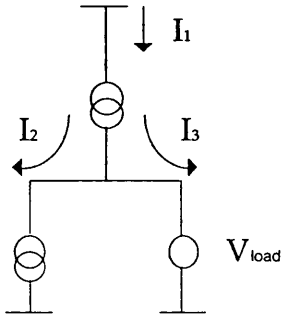


Fig 3.25 Tuneable negative current source. The lower source sinks I_2, so the current through V_{load}, $I_3 = I_1 - I_2$.

Using this technique we have designed a tuneable, negative current source, employing a diode biased source for the upper source, and a single cascode for the lower source (Fig. 3.26). The output conductance of this source is given by:

$$g_{out} = \frac{g_{diode} + g_{cascode}}{g_{diode} g_{cascode}} \tag{3.31}$$

Where g_{diode} is the conductance of the diode biased current source and g_{source} is the conductance of the cascoded current source. This source will therefore have a conductance of ~60μS to 80μS (corresponding to an impedance of ~13kΩ to 17kΩ) depending on the exact value of the diode voltage drop.

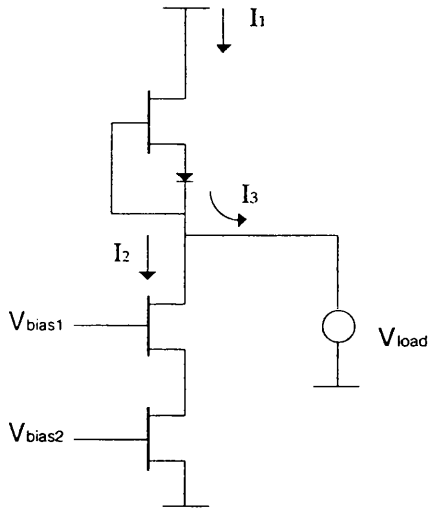


Fig 3.26 Complete tuneable negative current source.

3.5.5 High Impedance Negative Current Sources

One technique available to us for decreasing the conductance of negative sources is 'bootstrapping'. A cascoded negative source can be built by tying the gates of two FETs to the load, via a voltage level shift (Fig. 3.27).

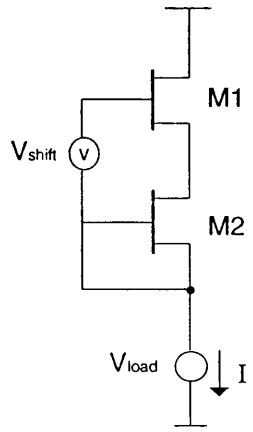


Fig 3.27 Bootstrapped current source. The bootstrap feedback maintains a constant voltage drop across *M2*, generating a low output conductance.

With an ideal level shift this would have an output conductance identical to the cascoded positive source, ie. 24μS. In reality an ideal level shift is difficult to realise. For example, adding a diode string directly to the lower FET will cause loading problems (Fig. 3.28). This can be improved by buffering the diode string. The buffering FET can also be bootstrapped in the process (Fig. 3.29).

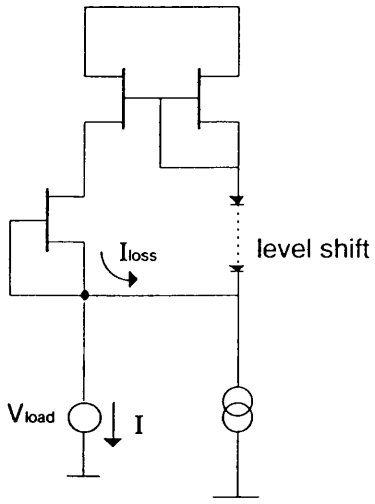


Fig 3.28 Current source bootstrapped using a diode level shift. Some of the required current will be lost through the level shift circuitry

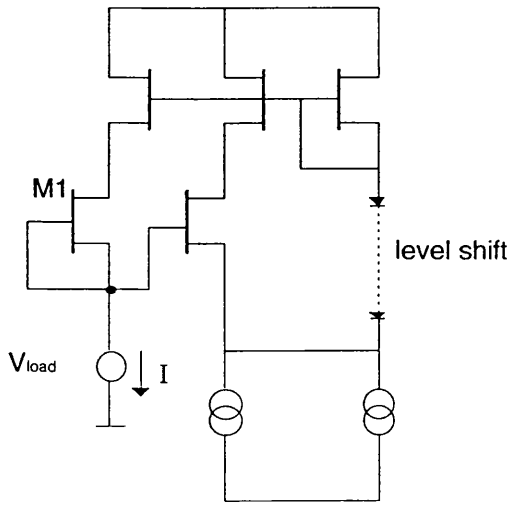


Fig 3.29 Complete bootstrapped negative current source.

The output conductance of the complete source (Fig. 3.29) is given by:

$$g_{out} = -\left(\frac{g_o^2 + g_m g_o (1-G)}{2g_o + g_m} \right) \tag{3.32}$$

where G, the gain of the follower is:

$$G = \frac{g_m^2 + g_m g_o}{g_m^2 + g_m g_o + g_o^2} \tag{3.33}$$

Using the 20µm FET, this gives g_{out} = 22.5µS. As the V_{gs} of $M1$ = 0v, this circuit will source ~1.85mA. To reduce this we can add current steering circuitry, as in section 3.5.4. Although the impedance of this circuit is slightly higher than the diode biased source it is doubtful whether the additional complexity is warranted. A double bootstrapped source was also investigated, but again this ultimately affords little improvement in the final system.

3.6 UNITY GAIN BUFFER

All of the sample and hold circuits presented require the use of unity gain buffers. It is therefore important that a high quality buffer can be built. In chapter 2 we saw that one property of GaAs FETs is a frequency dependent drain conductance, g_o. This can have a serious effect on the performance of follower circuits. A simple follower consists of a FET and a current source (Fig. 3.30).

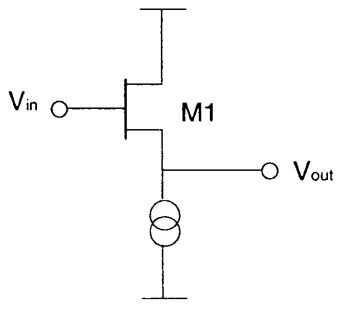


Fig 3.30 The simplest possible follower arrangement.

The gain of this follower is given by:

$$gain = \frac{g_m}{g_m + g_o} \tag{3.34}$$

Given that g_o can vary from ~96.5uS (low freq.) to 300μS (high freq.) and g_m = 3.7mS, we can see that the gain will vary from 0.925 to 0.975 depending on the frequency of the input signal. This will be most noticeable with a step input (Fig. 3.31). This slow transient gain error of around 5% would allow a resolution of around only 4-bits.

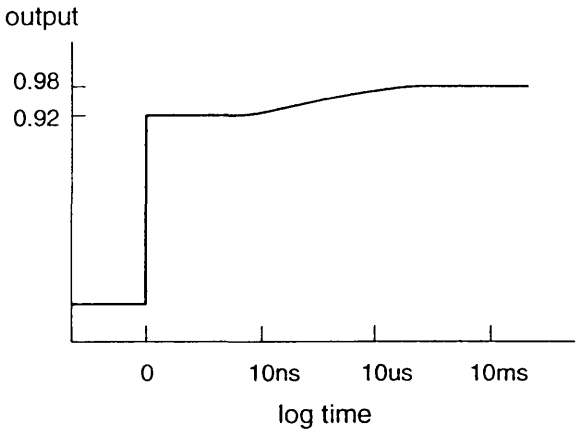


Fig 3.31 Time Domain step response of the simple follower circuit of Fig. 3.30.

To overcome this problem we must ensure that the V_{DS} of the follower is held constant. This can be done using bootstrapping, in a similar way to which it was used in the design of high impedance negative current sources (Fig. 3.32).

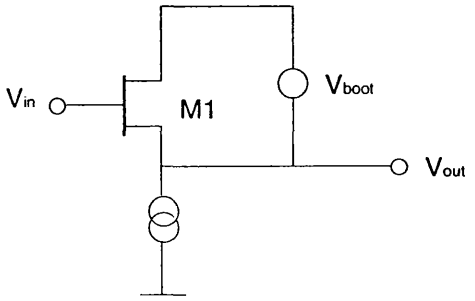


Fig 3.32 Bootstrapped Follower. This prevents the slow transient gain error of the simple follower circuit.

The bootstrapping is realised using a source follower and diode level shift (Fig. 3.33). The gain of this follower can be shown to be given by:

$$gain = \frac{g_m(g_m + g_o)}{(g_m + g_o)^2 - g_m g_o G} \tag{3.35}$$

where $G = \frac{g_m^2 + g_m g_o}{g_m^2 + g_m g_o + g_o^2}$ as before (3.33).

Using the values of g_m = 3.7mS, g_o (low frequency) = 96.5µS and g_o (high frequency) = 300µS given in section 2.2, this evaluates to 0.999 at low frequency and 0.994 at high frequency, an error of only 0.5% allowing a resolution of 7.65 bits.

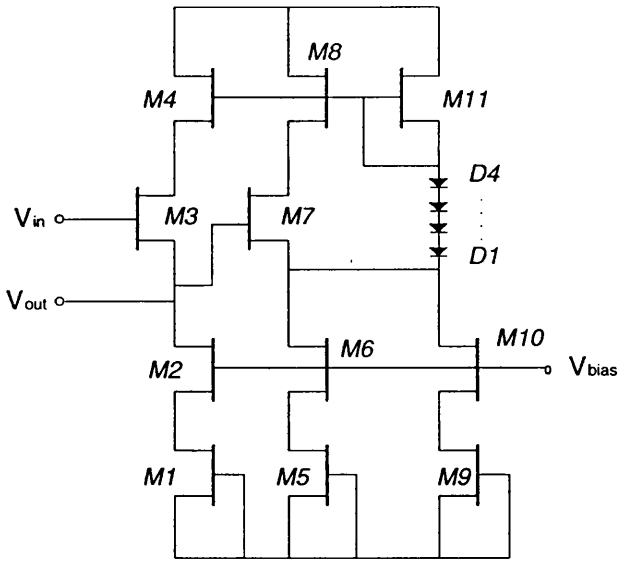


Fig 3.33 Final realisation of a bootstrapped follower circuit.

CHAPTER 4

IC FABRICATION

4.1 THE GEC-MARCONI F20 GaAs FOUNDRY PROCESS

The GEC-Marconi F20 process, [69,81,153], is a commercial foundry process for the manufacture of monolithic microwave integrated circuits (MMICs). It is an ion-implanted process with two layers of interconnection metal and a minimum feature size of 0.5μm providing performance to frequencies in excess of 20GHz. The process offers a catalogue of components including MESFETs, inductors, capacitors, resistors, diodes, and transmission lines. A complete description of the F20 process can be found in appendix 3.

4.1.1 GaAs MMIC Devices

(i) The GaAs MESFET

The MESFET is the most important active component for microwave integrated circuits and has been in use since 1974 [89]. The basic MESFET structure is known as a π-gate structure and is configured physically as shown in Fig. 4.1. The number of gate stripes or fingers (N) can be 1, 2, 4, or 6 and the width of each individual finger (W) can range from 20μm to 175μm. The MESFET active area is defined by the mesa layer (layer 1) with ohmic contacts (source and drain) in *M1* metallisation. The gate is defined in the first level interconnect metal (*M2*) and the FET is passivated with silicon nitride. Interconnections from the ohmic source and drain contacts are made using the second layer interconnect metallisation (*M3*). To minimise power consumption the smallest geometry device (single stripe, 20μm gate width) was used throughout all of the designs. Any device scaling needed was obtained by using multiple devices in parallel.

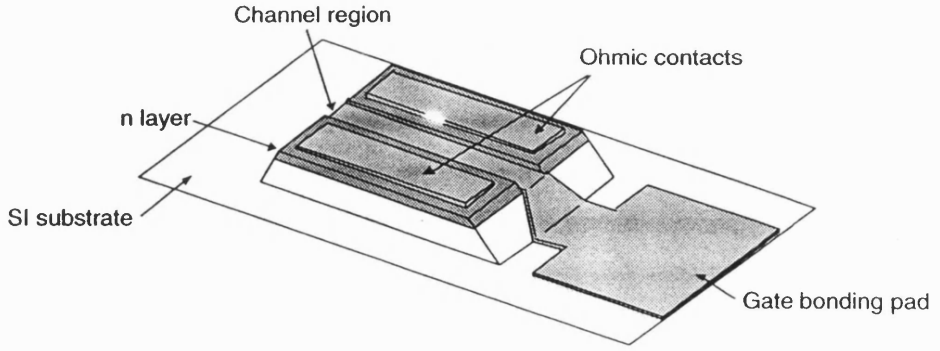


Fig 4.1 Schematic of a typical MESFET structure suitable for fabrication in a planar GaAs MMIC process.

(ii) Inductors

Inductors are used particularly in lower-frequency circuits as tuning elements between transistors. The most common implementation of MMIC inductors is the planar spiral inductor, shown in Fig. 4.2. This is formed by winding a number of turns of track in the top layer metallisation (*M3*) and making connection to the centre by means of an underpass in lower level metallisation (*M2*). Inductances in the range of 0.35nH to 13nH can be made with very high accuracy in this form. Other values of inductances can be made using either short lengths of transmission line (low values), or stacked spirals (high values).

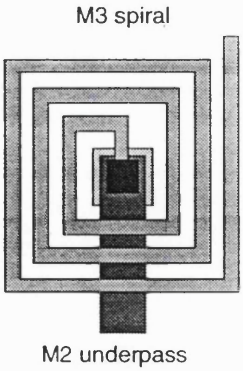


Fig 4.2 Spiral inductor suitable for fabrication in a planar GaAs MMIC process.

(iii) Capacitors.

The GEC-Marconi F20 process supports two basic types of capacitor structure: overlay and interdigital. Overlay, or metal-insulator-metal (MIM) capacitors are parallel plate capacitors with either silicon nitride or a combination of

silicon nitride and polyimide as the insulating material. The silicon nitride (MIM) capacitor consists of a bottom plate formed in first level metal *M2* separated from the *M3* top plate by a dielectric layer of silicon nitride, giving capacitances in the range 1.3pF to 59pF. A polyimide dielectric via is used to remove the polyimide from the capacitor. An example of a silicon nitride capacitor is shown in Fig. 4.3.

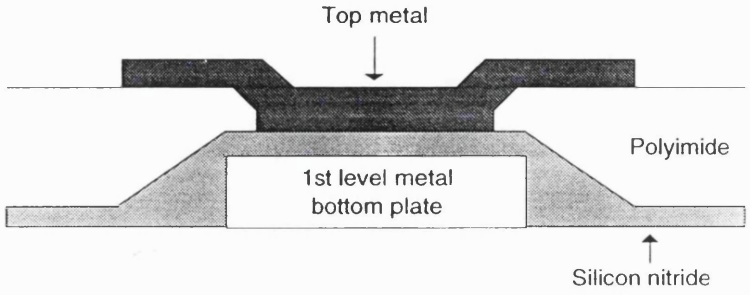


Fig 4.3 Section through a silicon nitride MIM capacitor.

The structure of the polyimide capacitor is identical to that of the silicon nitride capacitor except that the polyimide layer is not removed. This structure therefore has a lower capacitance per unit area than the silicon nitride capacitor and is suitable for capacitances in the range of 0.06pF to 2.5pF. One major difference in these capacitors is the level of resistive loss. The dominant contribution to this is from the dielectric material and because the dielectric loss of silicon nitride is much lower than polyimide, the silicon nitride is much lower loss than the polyimide capacitor. For this reason the silicon nitride capacitor is used wherever possible. The tolerance of both these type of capacitor is ±12%.

The final structure is the interdigital capacitor. These are formed by interleaving fingers deposited in the *M2* metallisation, and are are used for values of capacitance less than 0.5pF. Interdigital capacitors have negligable tolerance because the definition of the M2 metal is very accurate. The structure of an interdigital capacitor is identical to the MSM devices shown in Fig. 2.19, which allows us to use the GEC-Marconi F20 process for the fabrication of integrated MSM photodetectors.

(iv) Resistors

Resistors in the F20 process are fabricated in the ion implanted GaAs mesa layer, and can provide a resistance range from about 10Ω to 10kΩ, with a wafer to wafer tolerance of ±10%. The active area of the mesa resistor is defined by layer 1 (mesa). Ohmic contacts are then formed at each end in layer 2 (M1). The resistivity of the resistor material is set using layer 3 (mesa trim) to 300 W/sq.

4.2 IC LAYOUT

In order to produce a mask layout for the OS/H circuits described in chapter 3, a full custom physical layout editor – Silvar Lisco Princess – was used. Correct layout of high speed circuits is always critical, but it is particularly important when both analogue and digital signals are involved. These circuits combine analogue, digital and optical signals on a single substrate of GaAs, and so this problem is further exacerbated. To minimise signal degradation, analogue signal paths are kept as short as practical, avoiding bends and vias, and the digital paths are separated from these to reduce the possibility of capacitively coupling switching-noise into the analogue circuitry. As the ground connections form the return path for the analogue signal, these are treated in the same manner as analogue signal paths. The routing of DC supplies is much less critical, so these paths can afford to be much longer than the analogue signal paths and can accommodate bends and vias with fewer derogatory effects. To reduce noise on critical DC supplies these are decoupled to ground on the chip using 1pF silicon nitride capacitors. To avoid any possibility of the laser clock interfering with the light sensitive electronic components, the photodetectors are placed a minimum of 500μm from the electronic circuitry.

4.2.1 Unity Gain Buffer

The unity gain buffer was laid out following this design philosophy as closely as the design rules allow. Fig. 4.4 shows a photomicrograph of this circuit, in which the components are labelled the same as in the schematic of Fig 3.33. The input signal is applied to the gate of MESFET *M3* and the output is from the

source of this MESFET. The level shift diodes are shown as *D1 – D4*. MESFETs *M1 – M4* each consist of five devices in parallel to reduce the output impedance of the buffer to around 50Ω.

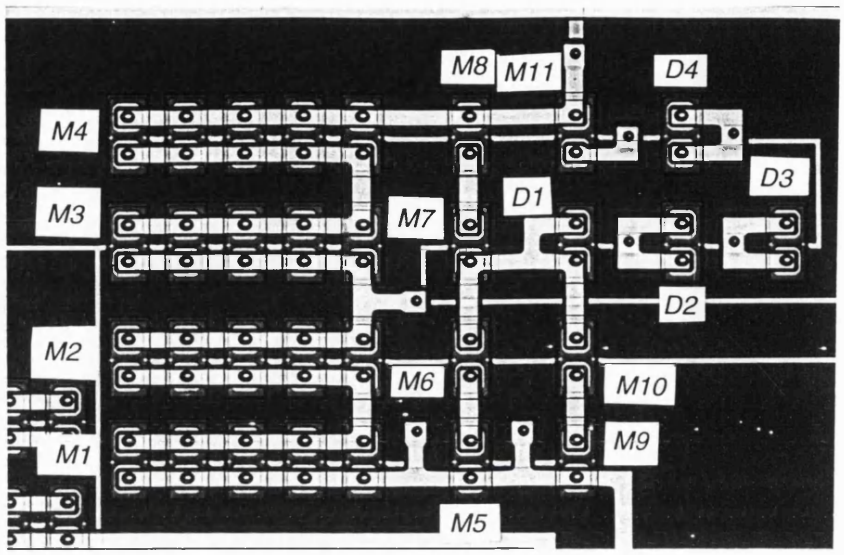


Fig 4.4 Photomicrograph of unity gain buffer.

4.2.2 Series Photoconductor OS/H

The series photoconductor OS/H is the simplest of the circuits to layout as it consists of only an MSM, a hold capacitor and a unity gain buffer. As these components occupy a small amount of die area (about 0.8mm x 1.2mm), two complete OS/H circuits with different sized MSMs are placed on a single chip, shown in Fig. 4.5. The MSMs are placed about 500μm away from the electronic components and the 0.75pF hold capacitor is made from two 1.5pF silicon nitride capacitors in parallel. Although this component could have been fabricated using a single polyimide capacitor, silicon nitride was used because of its lower resistive loss. The series photoconductor OS/H IC measures 1.6mm x 1.2mm in total, contains 62 MESFETs, and consumes an average power of 0.3W.

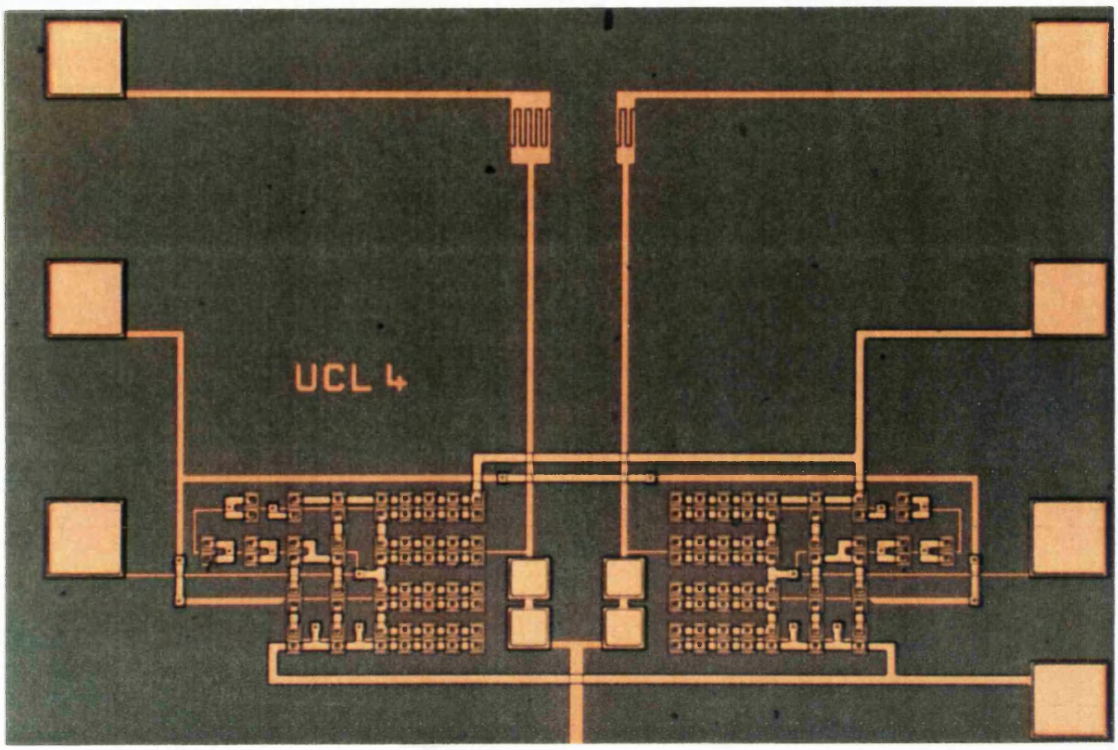


Fig 4.5 Photomicrograph of series photoconductor OS/H IC.

4.2.3 Series MESFET OS/H

The series MESFET IC also contains two complete circuits, but this time a diode connected MESFET is used as a photodetector in one of the circuits. The input and output terminals are labelled on the chip photograph (Fig. 4.6), showing that the signal path is completely straight, although it does go through two unavoidable vias. The DC MSM bias voltages are decoupled to ground using a 1pF on-chip capacitor. The purpose of this is to eliminate switching noise on the DC supply. This IC contains 104 MESFETs, measures 2.1mm x 1.4mm and consumes an average power of 0.4W.

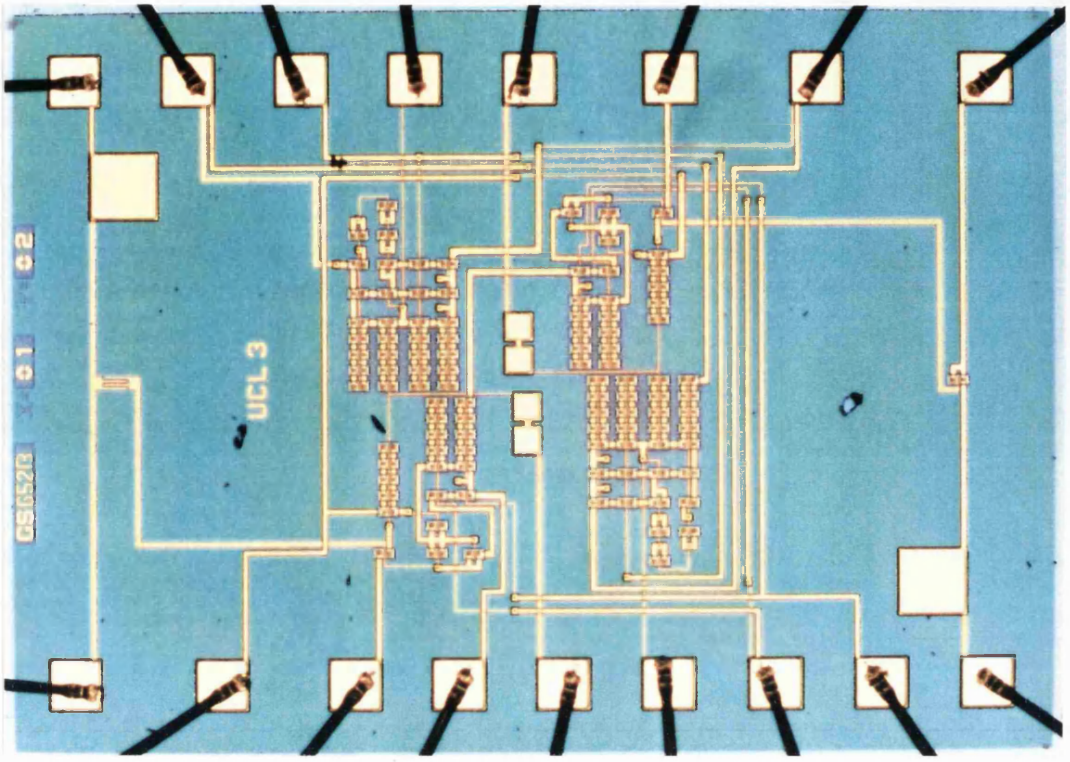


Fig 4.6 Photomicrograph of series MESFET OS/H IC.

4.2.4 Diode bridge OS/H

The diode bridge OS/H requires two photodetectors to be illuminated simultaneously. To ease this difficulty, the two detectors are placed alongside one another, so that they can be illuminated with a single spot of light. To minimise coupling of the clock signal between these detectors, they are arranged so that the adjacent fingers are connected to the DC bias voltages. Two individual diode bridge ICs have been fabricated, corresponding to the use of fixed and variable current sources as shown in Figs. 3.14 and 3.15. Each IC contains two complete OS/H circuits – one with MSM photodetectors, and the other with diode connected MESFET photodetectors. The IC shown in Fig. 4.7 consists of two OS/H circuits with fully tuneable current sources and contains 154 MESFETs, measures 2.3mm x 1.6mm, and consumes an average power of 0.6W. The second IC, shown in Fig. 4.8, comprises two OS/H circuits with fixed current sources. This IC contains 152 MESFETs, and has the same power consumption and size as the first diode bridge OS/H.

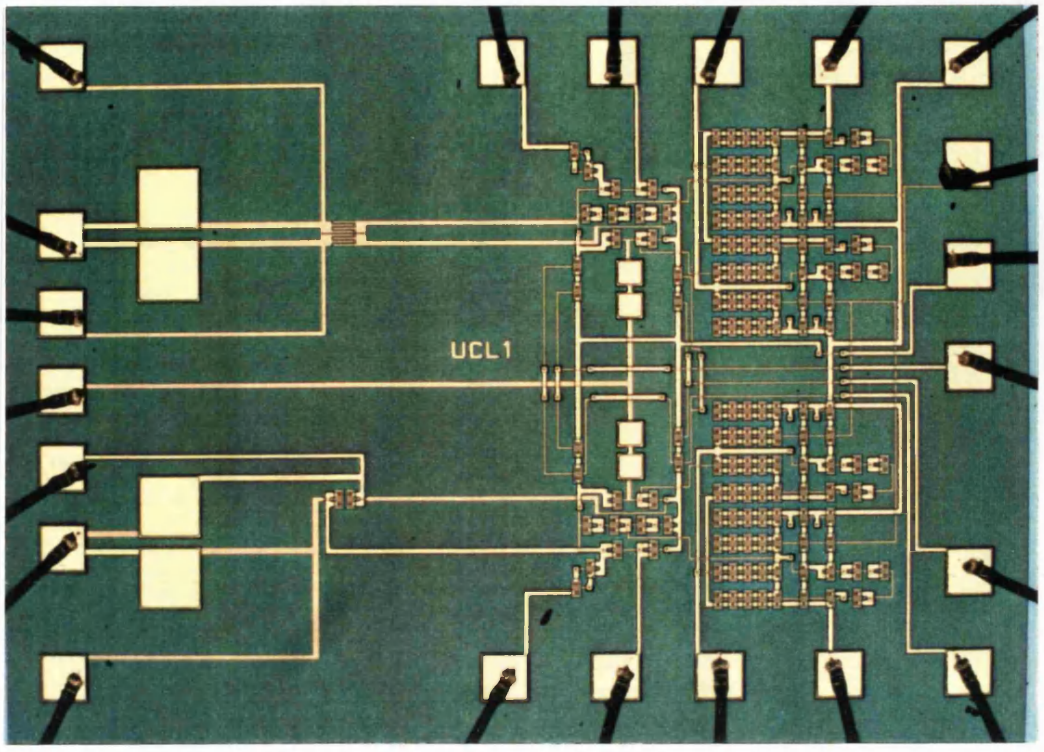


Fig 4.7 Photomicrograph of diode bridge OS/H IC (tuneable current sources).

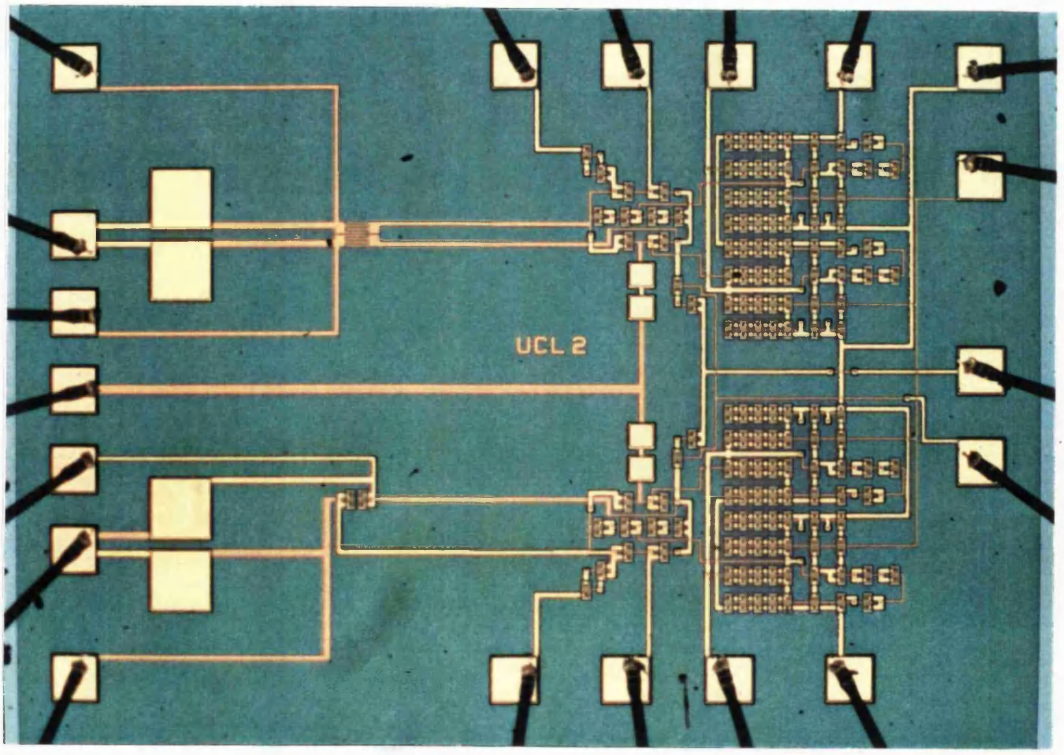


Fig 4.8 Photomicrograph of diode bridge OS/H IC (fixed current sources).

4.2.5 Electronic test structures

A chip containing key electronic components was built to allow these to be tested individually. The chip includes two unity gain buffers (one with single output FETs and the other scaled to 50Ω), a diode biased current source and a cascoded current source. A photograph of this chip is shown in Fig. 4.9.

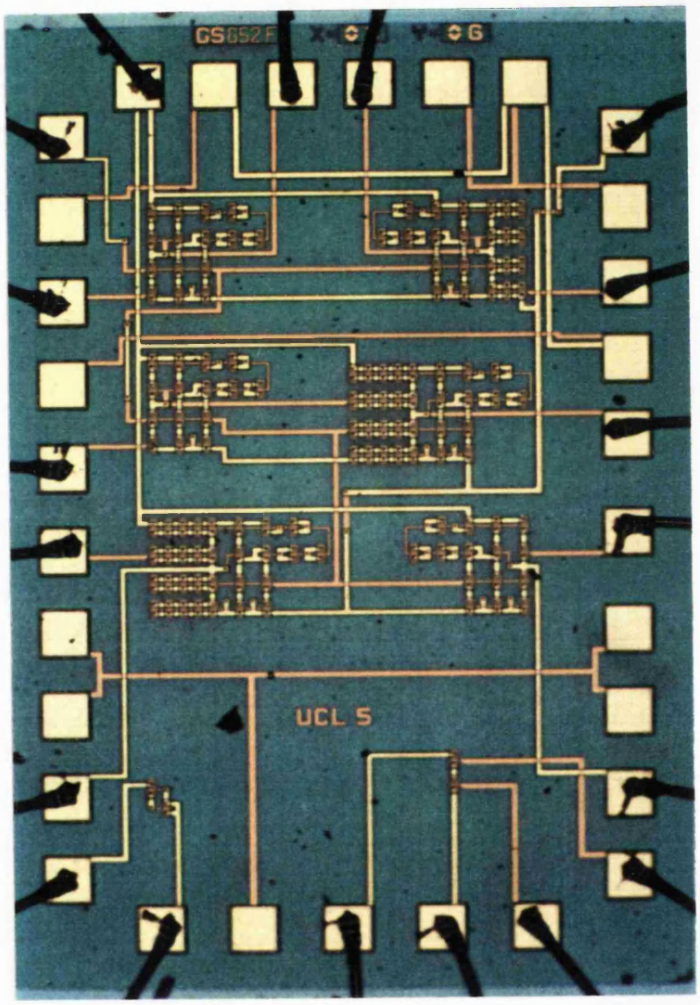


Fig 4.9 Photomicrograph of electronic test IC.

4.2.6 Optical test structures

The optical test structure IC, shown in Fig 4.10, is designed to allow the independent testing of a range of photodetectors. The chip comprises a total of six photodetector structures, including all of the photodetectors used in the OS/H circuits, along with some different geometry MSMs and an MSM pair with a larger spacing than used in the bridge circuits. This chip was used for

measuring the AC and DC characteristics of the photodetectors, enabling the determination of the optical powers and bias voltages needed in the circuits.

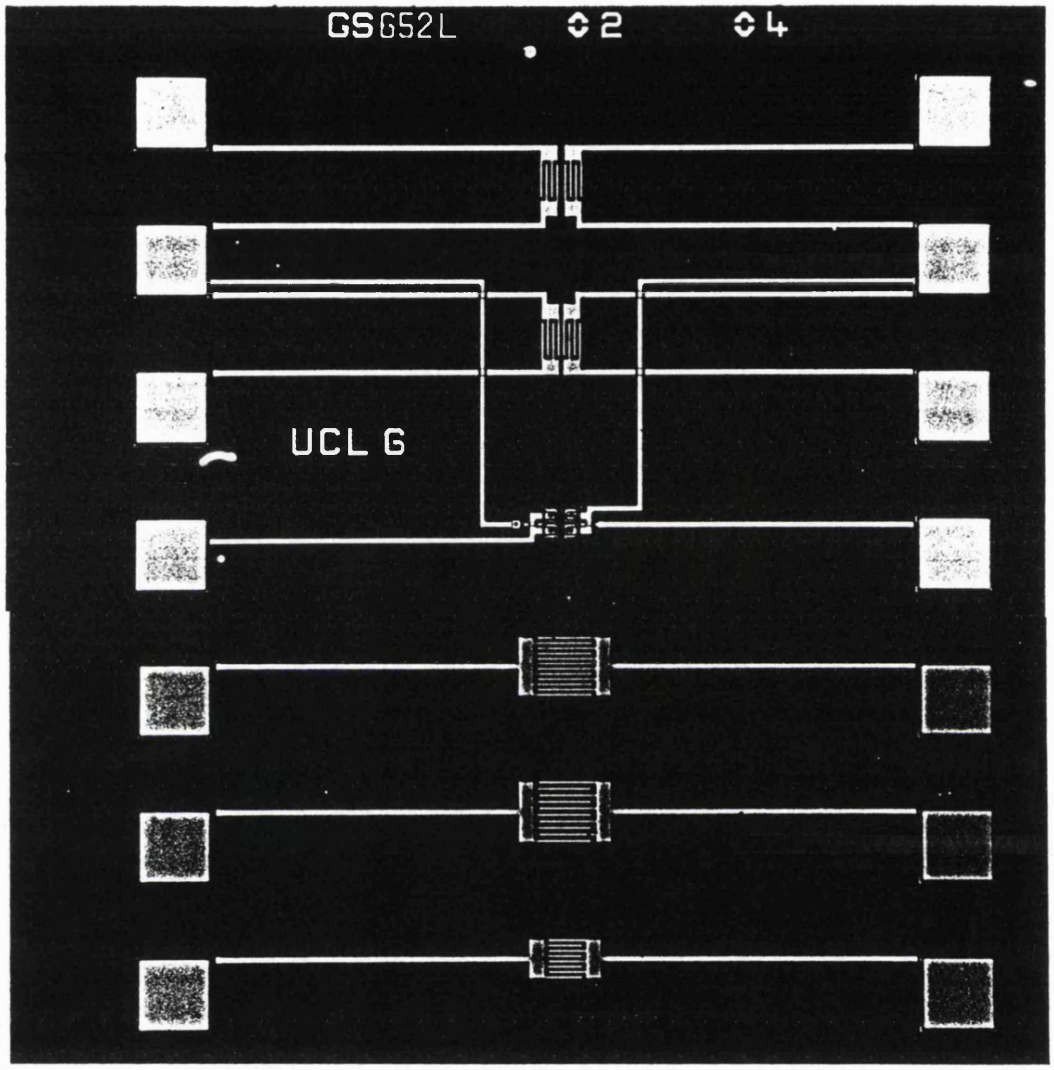


Fig 4.10 Photomicrograph of optical test IC.

4.3 PACKAGING AND PCBS

Each IC is gold wire bonded to a 400MHz ceramic dil package. For testing the circuits, custom built PCBs were used. As these circuits are used for signals in excess of 250MHz, the layout of the PCBs needs to be done with great care. In the layout of PCBs for high speed circuits, the layout of ground connections is an important factor. To reduce noise and interference on the circuit ground, a

double-sided copper-clad printed circuit board was used. Every part of the board not used for components or connections forms part of a continuous ground plane. This ground plane covers both sides of the board and is joined around the edge by a continuous soldered seal of tinned copper foil. Each of the signal connections are made via gold-plated SMA sockets, mounted as close to the relevant IC pins as possible. To eliminate noise on DC power supplies, these are capacitively decoupled to the ground plane using 0.1μF surface mount capacitors connected directly to the power supply pins. Low frequency ripple is minimised by further decoupling using 22μF tantalum capacitors. Both of these types of capacitor have high resonant frequencies, ensuring that they maintain their characteristics over the high frequency ranges involved. In addition, incoming noise on each DC supply is minimised by connecting these through a series 0.1μH inductor. A typical PCB board is shown in Figs. 4.11a and 4.11b.

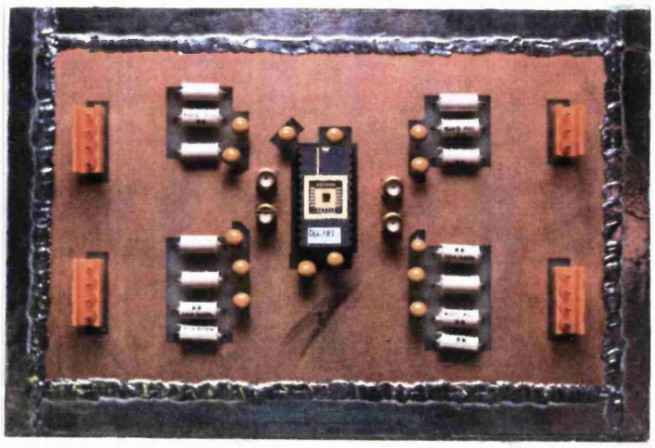


Fig 4.11a Top side of a typical PCB used for testing the OS/H circuits.

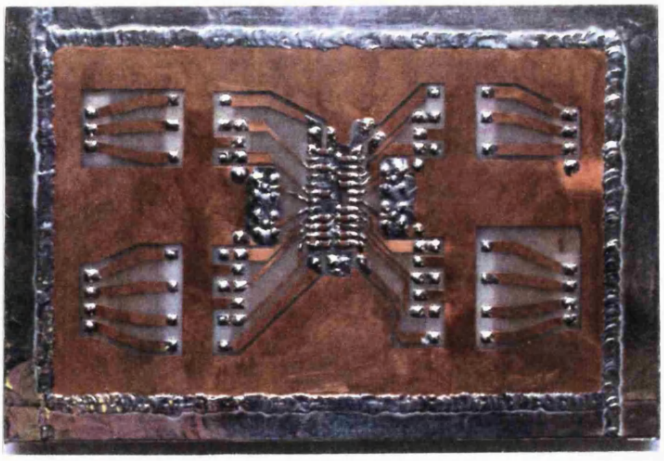


Fig 4.11b Bottom side of a typical PCB used for testing the OS/H circuits.

CHAPTER 5

MEASURED RESULTS

This chapter contains measured results and HSPICE simulations for all of the circuits described in chapter 3. It begins by describing the measurements made upon the electronic and optical test structures, and continues with a wide range of tests on the OS/H circuits. These tests are designed to give an insight into the action of the circuits and highlight their qualities and deficiencies. Where possible the measured results are compared directly to simulations and the calculations made in chapter 3.

5.1 CIRCUIT BUILDING BLOCKS

Before testing the S/H circuits a series of measurements were made on the electronic and optical test structures included on the test chips. In particular, the characteristics of the current sources and photodiodes were measured so that the correct bias voltages for the S/H circuits could be determined. A number of preliminary tests have been made on these circuits and the results are presented here.

5.1.1 Unity Gain Buffer

As the unity gain buffer is a key component in all of the OS/H circuits, its performance will affect each of these circuits. A series of measurements have shown that in key areas of performance the buffer functions correctly, and is appropriate for use in the OS/Hs. Comparisons with the SPICE simulations are made which highlight the similarities (and differences) between the measured and simulated results. A test jig was built consisting of a dil socket mounted on plain matrix board. In order to damp unwanted oscillations tinned copper shielding is used as a ground plane, DC connections are made via 10μH inductors, and all DC points are decoupled directly to ground with 0.1μF surface mount capacitors. Additionally, all unused pins are connected to either 0v or – 5v as appropriate.

(i) Frequency Response

The frequency response of the buffer was simulated using HSPICE with a 1V peak to peak input signal swept from 1Hz to 10GHz, as shown in Fig. 5.1. This simulation uses the dispersive MESFET model shown in Fig. 2.12. At low frequencies (< ~100Hz) the output conductance takes the DC value of 96.5μS giving a gain of 0.999 (–8.69mdB). At frequencies above 1kHz the output conductance increases to 300μS, reducing the gain to 0.994 (–0.052dB) and indicating a gain error of about 0.5%. This is equivalent to the gain error calculated in section 3.6. The – 3dB frequency is in excess of 10GHz.

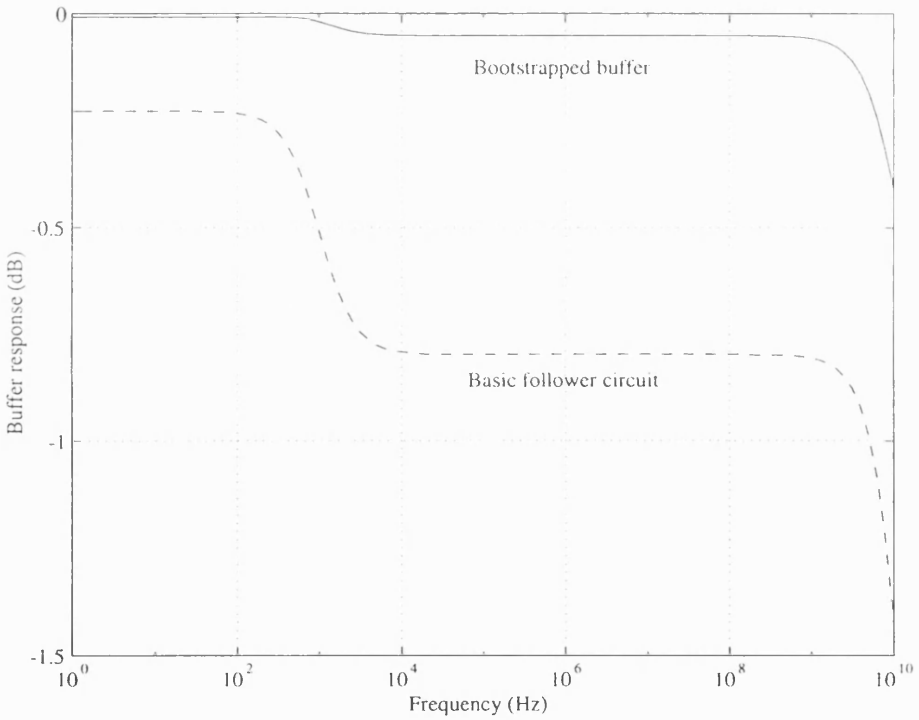
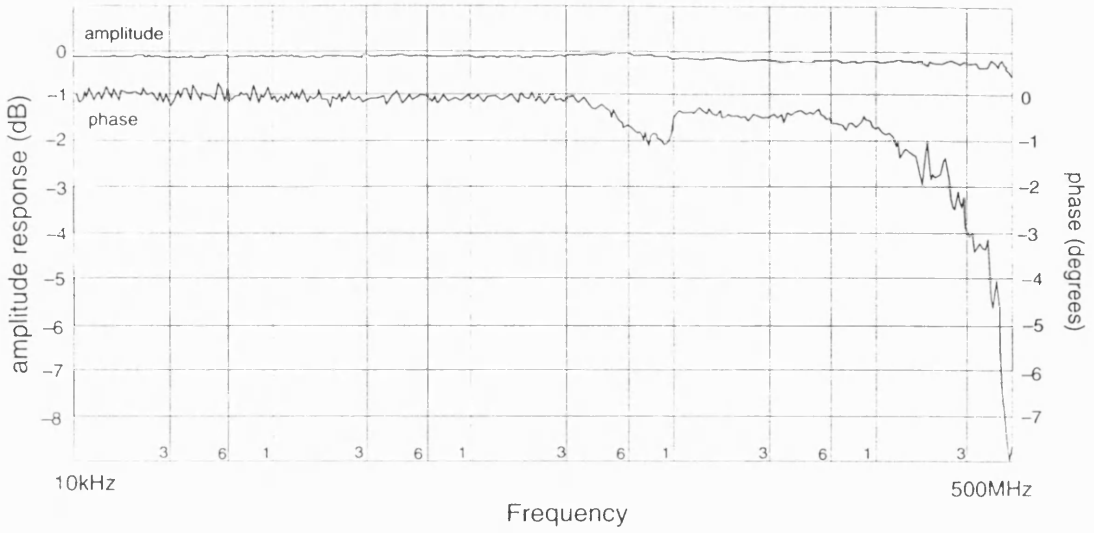
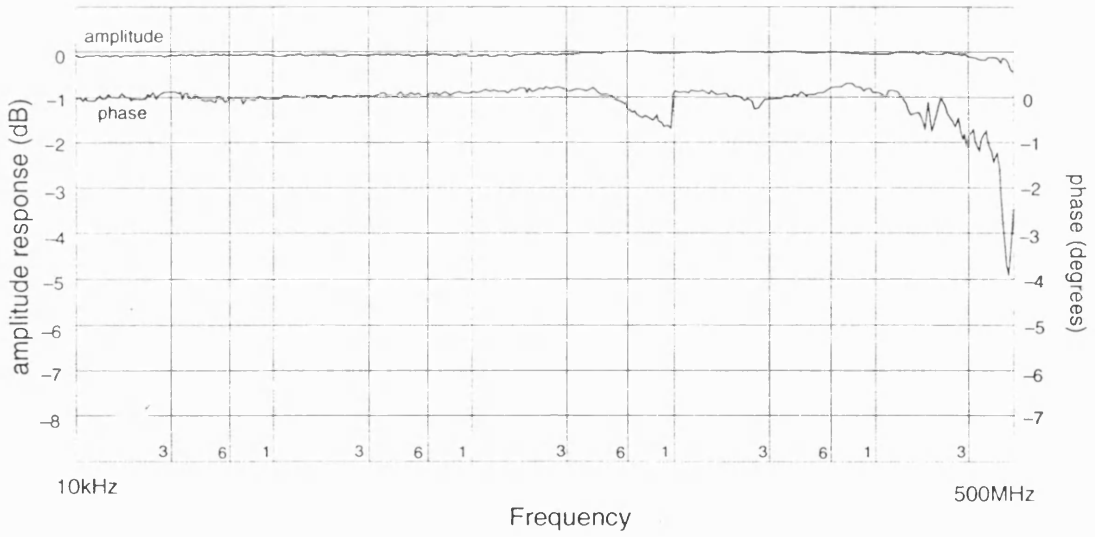


Fig 5.1 Simulated frequency response of the unity gain buffer. This shows the effect of frequency dependent drain conductance.

The frequency response was measured in a 50Ω environment using a Hewlett-Packard 500MHz network analyser delivering a 0dBm (224mV rms.) output. To correct for the effects of the PCB board, cables etc, a calibration was performed by replacing the buffer chip with a straight-through connection. Fig. 5.2 shows the results of these measurements, revealing a frequency response which is flat to within 0.5dB and 4° up to 500MHz, supporting the simulated measurements.



(a) Uncalibrated measurement.



(b) Calibration of test jig.

Fig 5.2 Measured Frequency response of buffer. The intrinsic buffer response can be found by subtracting the calibration curve from the uncalibrated curve.

From these result the gain of the buffer was measured at –0.05±0.01dB (i.e. a gain of 0.994), which corresponds to the value predicted from the calculations and simulations.

(ii) Step Response

We have seen that a characteristic of GaAs MESFET technology is a frequency dependent output conductance, and have described how the unity gain buffer was designed to minimise this effect. From simulations made in section 5.1.1(i) we expect to find that the step response will vary by around 0.5% over a period of a few milliseconds. To measure this effect the buffer was driven with a 50Hz, 0.5V peak to peak square wave while the input and output were monitored with high impedance FET probes. These signals were recorded using a digital oscilloscope set on the most sensitive voltage setting of 1mV/division (which gives a sensitivity of 10mV/division when used in combination with the x10 FET probes). The results of this measurement are shown in Fig. 5.3, and reveal that the input rises by 5.0±0.5mV over a period of 10ms, while the output rises by 8.75±0.5mV over the same period. The difference between these two figures gives the rise due to the buffer. As the input signal level was 0.5V peak to peak, the gain error G_E is 3.75/500 = 0.75±0.14%, or 7.1±0.3 bits. This error is a slightly higher then predicted, but it must be noted that this figure is an *upper limit* on the intrinsic slow transient gain error, and also includes the *RC* time constants due to the PCB, packaging etc. This measurement does show that the slow transient effects of GaAs have been largely eliminated in the buffer design.

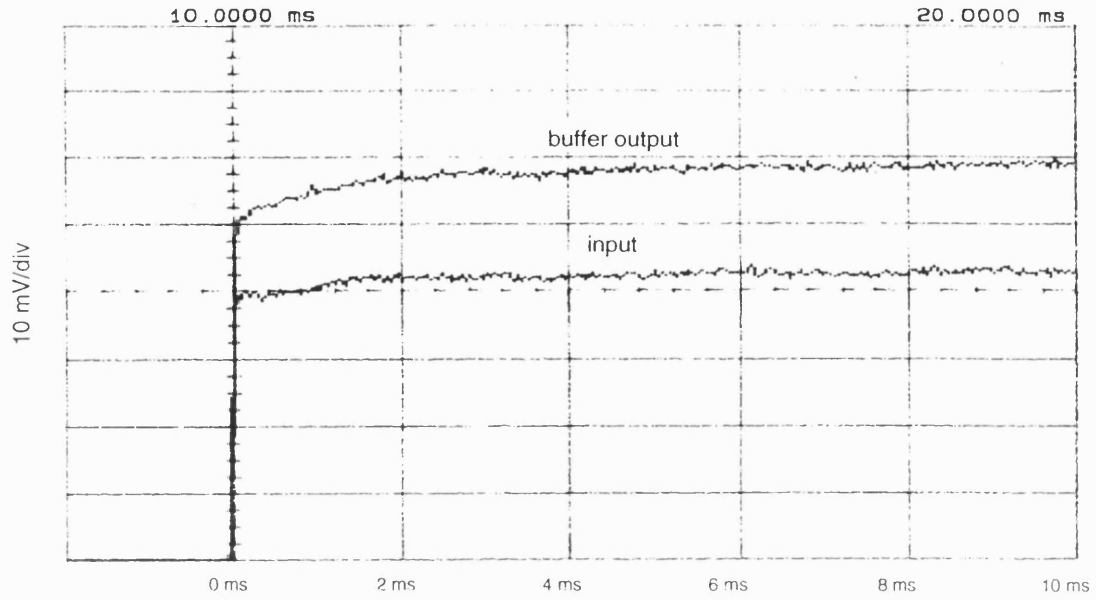


Fig 5.3 Step response of buffer. The output rises by < 0.75% over 10ms, demonstrating the effectiveness of the bootstrap feedback circuitry.

(iii) Output Impedance

In order that the unity gain buffer can be used in a 50Ω environment it is scaled so that the output impedance is as close to 50Ω as possible. With a single 20μm output MESFET, the output impedance is approximately 270Ω (given by the value of $1/g_m$ of the output MESFET). By using five MESFETs in parallel for the output stage, the impedance is reduced to 54Ω. The output impedance was measured by loading the output with a range of resistors, and measuring the drop in output. The input was driven by a sinusoid of varying amplitude and frequency. Using this method an output impedance of $68 \pm 2\Omega$ was measured. This corresponds to a value of g_m of 2.94mS, a drop of around 20% below he estimated figure.

(iv) Harmonic Distortion

Harmonic distortion is an important effect in any linear system: in an ADC the effect is to lower the resolution. The total harmonic distortion (THD) was measured with a range of input frequencies, at varying input signal levels. With input levels of 100mV and 500mV the THD is below the noise floor (-80dB).

5.1.2 Current Sources

In all of the circuits it is necessary to adjust the current sources to generate currents appropriate to the available photocurrent. The *I-V* response of the cascoded current source (Fig. 3.22) is shown in Fig. 5.4, along with corresponding HSPICE simulations. This measurement was made using a 100kHz sine wave as the voltage source thus avoiding the effect of output conductance dispersion. We can see in this figure that the measured current is slightly lower than the simulated result, indicating a value of transistor beta around 20% lower than expected.

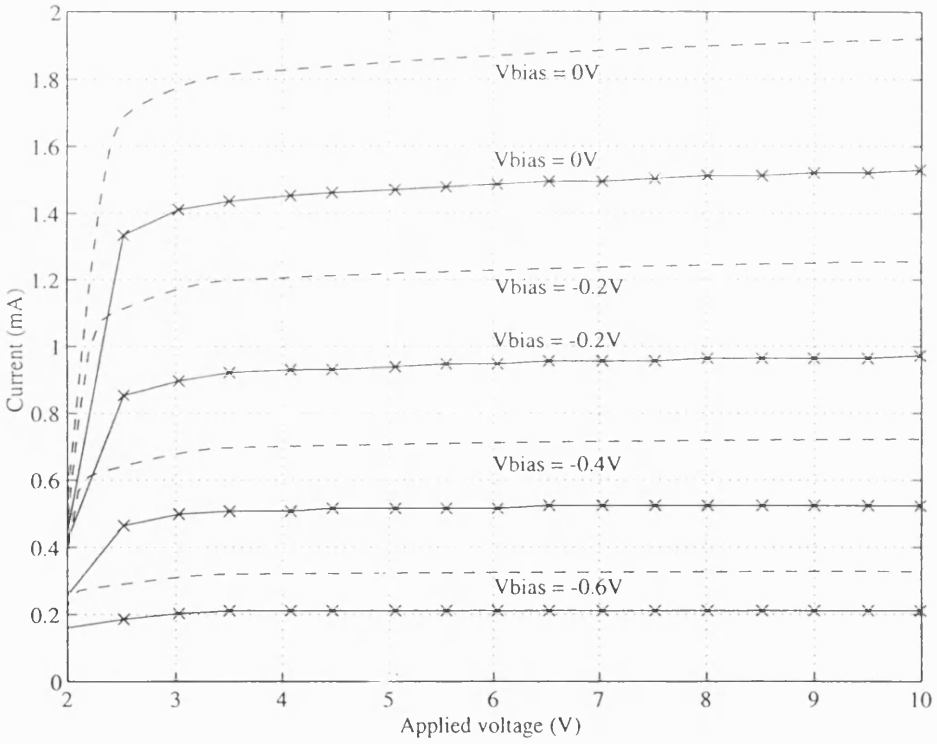


Fig 5.4 DC response of cascoded current source, solid line = measured response, dashed line = simulated response. The slight difference between these suggests that the actual value of MESFET beta is ~20% lower than expected.

5.1.3 MSM Photodetectors

(i) DC response

Before any accurate circuit design could be performed the action of the MSMs had to be established. The response of a 60μm by 60μm MSM was measured using the experimental arrangement illustrated in Fig. 5.7. Light from a 50μm core multimode fibre was directed onto the MSM surface, and the position of the fibre was adjusted by means of micro-positioners with 50μm piezoelectric stacks. The maximum power incident on the MSM was 10mW, and this was varied by means of neutral density filters, allowing the optical power to be adjusted without changing the experimental set-up.

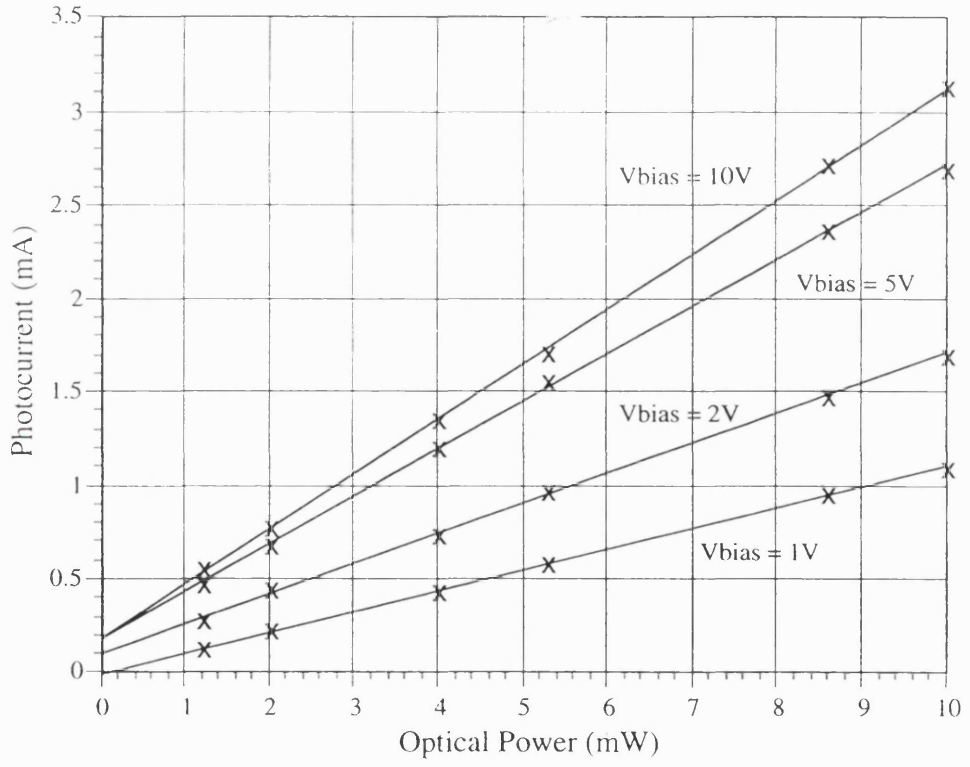


Fig 5.5 DC Response of a 60μm x 60μm MSM Photodetector.

With a 10V bias, the responsivity is ~0.3A/W.

A plot of photocurrent versus optical power at constant bias voltage is shown in Fig. 5.5, revealing a responsivity of 0.313A/W at a bias of 10V. From equation (2.23) this gives a quantum efficiency of 47%, which considering that half of the MSM area is covered by the metal fingers, is about the maximum one might expect. The high measured quantum efficiency, suggests that a certain

amount of gain is occurring in the device (i.e. more than one electron being generated for each absorbed photon). This is a common effect in MSM photodetectors and is usually attributed to electron accumulation at the anode-semiconductor interface [103].

(ii) Pulse response

To test the AC response of the MSMs a laser drive circuit has been built which can modulate a 40mW laser diode at 250MHz (appendix 1). This source, driven by a high quality pulse generator, will also be used to drive the S/H circuits. The response of a 60µm x 60µm MSM to a 100MHz optical pulse is shown in Fig. 5.6. This trace shows the voltage developed across a 47Ω resistor and measured into the 50Ω input of a digitizing oscilloscope. The 10±1mV peak is equivalent to 413±42µA. As the peak output power of the laser was 1.6mW and the MSM responsivity 0.3A/W, we would expect a photocurrent of 480µA. The reduced value is due to slight misalignment of fibre and the reduction in extinction ratio of the laser.

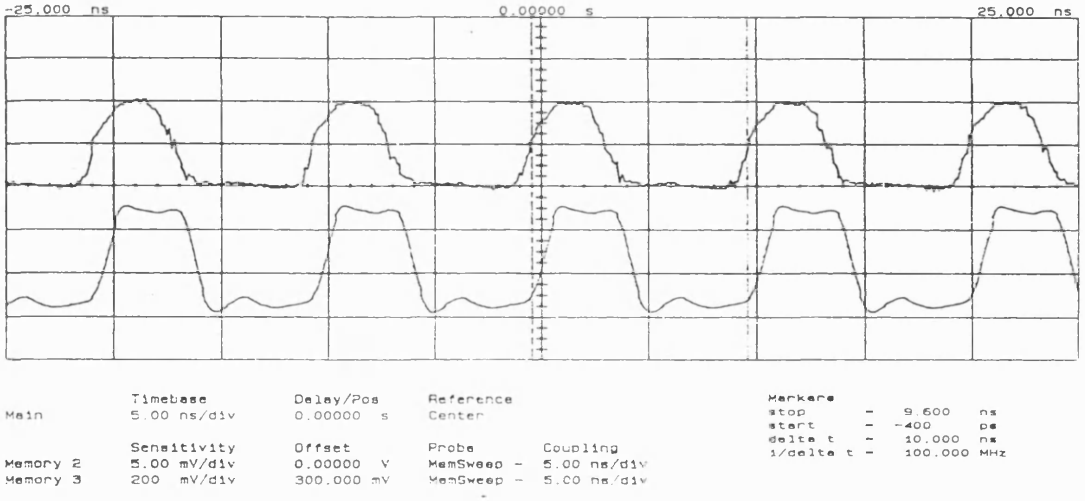


Fig 5.6 Response of a 60µm x 60µm MSM to a 100MHz laser source.

Upper trace = MSM photocurrent, lower trace = driving signal.

5.2 OPTICALLY TRIGGERED SAMPLE AND HOLD CIRCUITS.

This section describes the measured results obtained from the OS/Hs, and a comparison is made between the measured results and the simulations. To make an accurate comparative test between each of the different circuits, a standard test set-up was used. To eliminate problems of impedance mismatch a 50Ω environment was maintained throughout all the measurements, and common signal amplitudes and optical powers were used. The MSM photodetectors on the OS/H chips were designed to be illuminated by a 50μm core multimode fibre. We therefore required an experimental arrangement which allowed accurate alignment of the fibre with the MSM to a resolution within a few microns. This was achieved using a 3-way micropositioner with piezoelectric adjustment, the position of the fibre tip being monitored using a long working-distance microscope. Fig. 5.7 shows the experimental arrangement used for all the measurements, and Fig. 5.8 is a photograph of the fibre alignment apparatus.

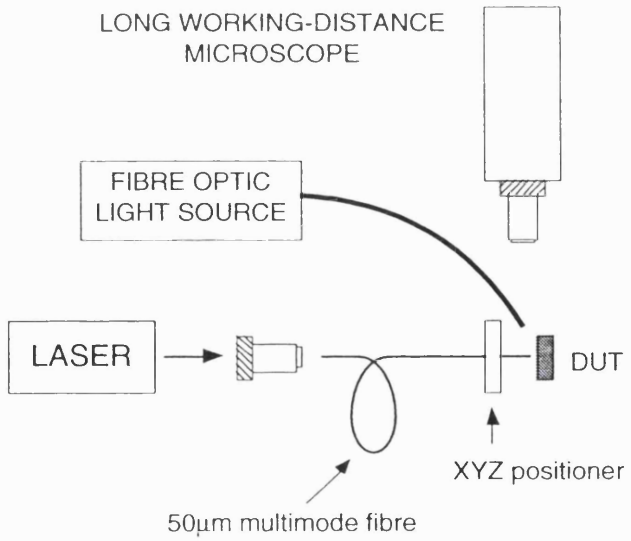


Fig 5.7 Experimental arrangement for OS/H measurements.

The laser is an 830nm laser diode with collimating optics.

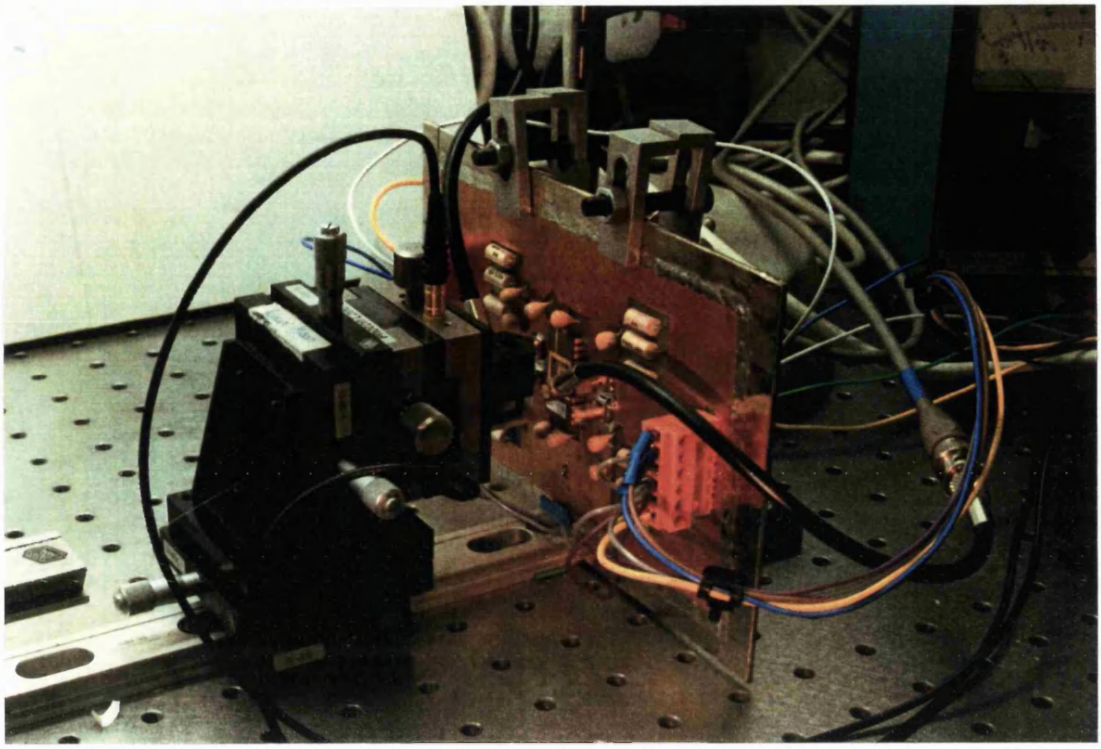


Fig 5.8 Alignment of optical fibre with a test chip using piezo-electric positioners. The long working-distance microscope is removed for clarity.

Recording the output of a S/H circuit presents problems, as the input signal is, in general, uncorrelated to the sampling clock. Ideally one would use either a fast single-shot analogue oscilloscope or a high sample-rate digitizing oscilloscope to capture the signal. For a signal sampled at 250Ms/s the analogue scope needs a very high photographic write speed, which is only found on instruments with image intensified displays. Similarly a digitizing oscilloscope would require a sample rate of at least 1Gs/s, and ideally much higher, to capture the signal adequately. As these high performance instruments were not available, alternative methods for capturing the signal were devised.

Recording the signal with the analogue scope is somewhat easier than with the digital scope, as it can trigger on signals which are only partially repetitive. It was found that by adjusting the input signal frequency until there was (as near as possible) an integer number of sampling pulses per period allowed AC coupled triggering on the signal. Careful adjustment of the trigger level and hold-off is necessary to produce a steady trace. This method of triggering

captures and overlays traces where the sampling occurs at an approximately common point on the input signal. The variation in sampling instant results in a slight blurring of the signal during the HOLD phase, but this can be reduced to tolerable levels. All of the analogue scope photographs are taken in this manner.

The digitizing oscilloscope used has an analogue bandwidth of 500MHz, but the sample rate is only 20Ms/s. This means that high speed signals have to be highly repetitive before they will be recorded. There are, however, many advantages to using a digitizing oscilloscope, such as the ability to process results by computer, allowing accurate measurements of effects such as harmonic distortion, pedestal and droop to be made. To produce a repetitive signal requires the synchronisation of the input signal with the sampling clock. This was done by triggering the onset of a burst of clock pulses with the input sinusoid. When triggered from an external source, the maximum pulse generator repetition rate is 200MHz. To test the high-speed OS/Hs an input signal frequency of 16.67MHz (60ns period) was used, triggering a burst of twelve 5ns period (50% duty cycle) pulses. This produces a waveform with exactly twelve sample pulses for each input period, the pulse generator being re-synchronised with each input cycle. Accurate triggering can be obtained using the edge hold-off facility of the digitizing scope.

5.2.1 Series Photoconductor OS/H

The series photoconductor OS/H circuit consists of a 60μm x 60μm MSM used as a photoconductive switch, and a 0.75pF hold capacitor, buffered by a 50Ω unity gain buffer. The performance of this circuit is predicted in section 3.2.

(i) Analogue Bandwidth

The first test made on the series photoconductor circuit was to measure the analogue bandwidth. From this measurement we can determine the value of R_{on} for the MSM photodetector. The MSM was illuminated with a CW laser power of 5mW, using the 50μm multimode fibre. With an input voltage of 1V p-p the −3dB bandwidth was found to be 23±0.2MHz, corresponding to $R_{on} = 9.2 \pm 0.2 k\Omega$.

(ii) Pulsed Measurements.

Fig. 5.9 shows an analogue oscilloscope photograph of the series photoconductor OS/H sampling a 1MHz 0.4V rms sinusoid at 5Ms/s. This is approaching the maximum sample rate for this circuit. The sample rate of this circuit is dominated by the acquisition time. As the hold capacitor is effectively charged by a fixed resistance R_{on}, we can calculate the time to charge to with a specified error band assuming a first order system. For example, if we require 8-bit resolution, the time to acquire the input to within 1 lsb t_a can be found from:

$$1 - e^{-2\pi t_a f_{-3dB}} = {}^{255}\!/_{256} \tag{5.2}$$

$$t_a = \frac{-\ln\left(1 - {}^{255}\!/_{256}\right)}{2\pi f_{-3dB}} = 38.4 \pm 0.3\text{ns} \tag{5.3}$$

This would limit the sample rate to about 13Ms/s with a duty cycle of 50%.

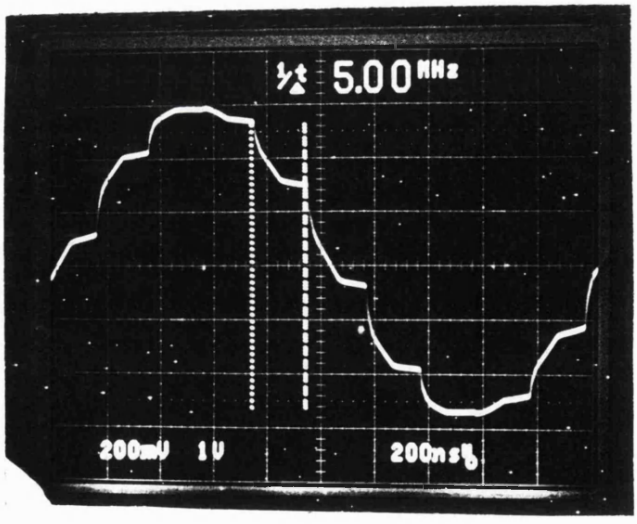


Fig 5.9 Series photoconductor OS/H shown sampling a 500kHz sinusoid at 5Ms/s. This is the maximum rate at which the circuit can operate effectively.

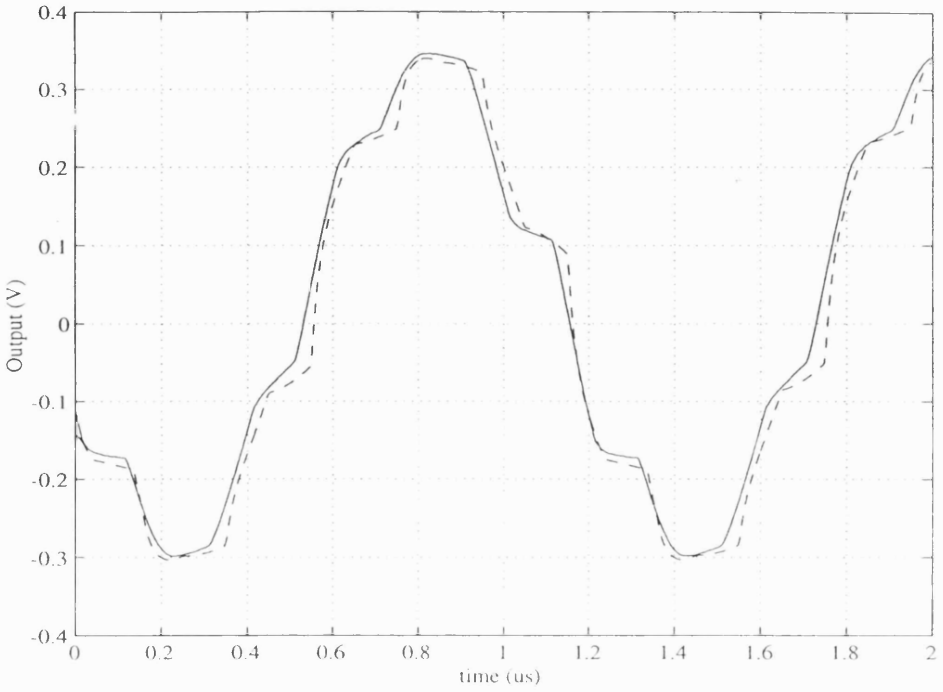


Fig 5.10 This shows the series photoconductor OS/H sampling a 833kHz signal at 5Ms/s, as recorded by a digitizing oscilloscope. The solid trace is the measured response and the dashed trace is a simulation.

In order to compare the measured circuit response with simulations, the signal was also recorded with a digitizing oscilloscope. In Fig. 5.10 we show a 833kHz 0.4V rms input sampled at 5Ms/s (i.e. 6 samples/period) and the corresponding SPICE simulation. To simulate the series photoconductor OS/H the MSM was modelled as a voltage controlled resistor switch with a small (20fF) capacitor in parallel. A close fit to the measured result was achieved using an *on* resistance of 9kΩ and an *off* resistance of 200kΩ. The value of R_{on} is close to the value suggested by measurements of the analogue bandwidth and CW photodiode response. The *off* resistance is somewhat lower than we would expect under zero illumination, but this is be due to the laser extinction ratio being less than 100%.

5.2.2 Series MESFET OS/H

From the calculations in the section 3.3 we have shown that the series MESFET circuit is capable of sample rates in excess of 250Ms/s, and have estimated some of the other aspects of its behaviour. We now present a wide range of

simulations and measurements which demonstrate the viability of the circuit design for the intended purpose.

(i) Simulation of Operation at 250Ms/s

Figure 5.11 shows an HSPICE simulation of the pass transistor circuit. This simulation was performed with a 1V peak to peak, 50MHz input sinusoid, and a sample rate of 250Ms/s. The photocurrent was a 1mA square wave with 200ps rise and fall times and a 50% duty cycle. Thus the photocurrent pulse is approximately the same as we would expect in the real circuit. From this simulation we can see that the circuit is capable of sampling the input signal comfortably at 250Ms/s. There is a slight phase shift between the input and output of ~ 6°, which arises because of the RC nature of the circuit. By assuming a first-order response, the phase shift, φ, is given by:

$$\varphi = \tan^{-1}\left(-\omega R_{on} C_{hold}\right) \tag{5.4}$$

so, with an input of 50MHz we would expect a phase shift around 6°.

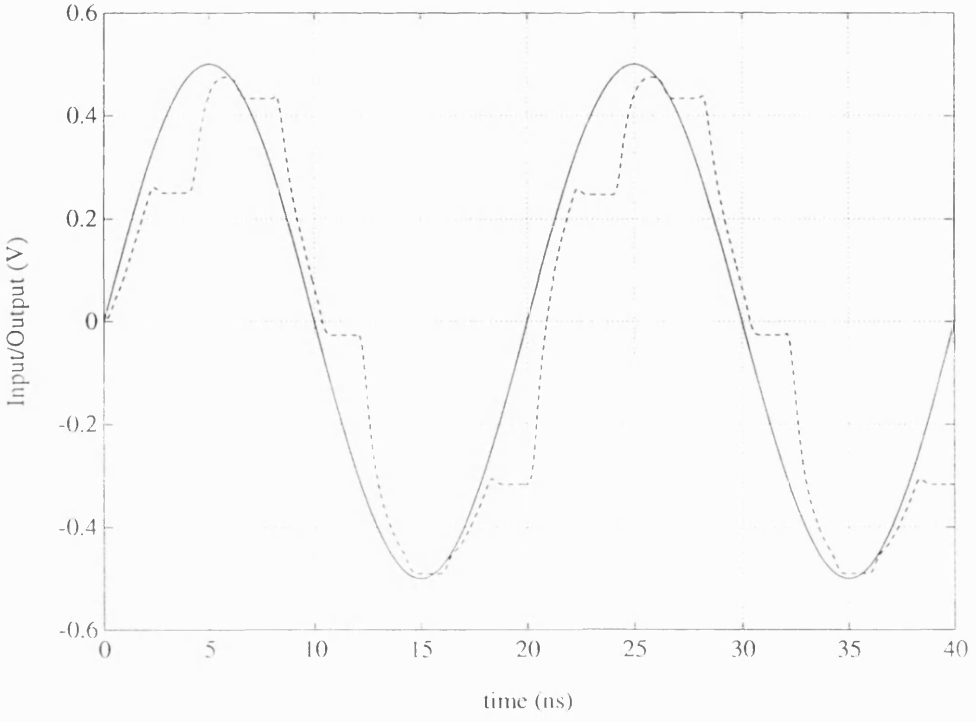


Fig 5.11 HSPICE simulation showing the series MESFET OS/H sampling a 50MHz sinusoid at 250Ms/s.

(ii) Measured Operation at 250Ms/s

Simulations suggest that the maximum sample rate of the series MESFET OS/H is in excess of 250Ms/s. To measure this performance the OS/H input was driven by a 62.5MHz 0.4V rms sinusoid and the laser was pulsed at 250MHz, providing 4 samples/period. The output from the OS/H was recorded using a 400MHz analogue oscilloscope and is shown in Fig. 5.12. This photograph shows the circuit operating very satisfactorily. The acquisition time is ≈ 1.5ns, suggesting an upper limit to the sample rate in excess of 300Ms/s. A simulation of this circuit under identical conditions is shown in Fig. 5.13 and corresponds exactly to the measured result. The circuit was also recorded using the digitizing oscilloscope with a 16.67MHz input and 200Ms/s (12 samples per input cycle). This is shown in Fig. 5.14, with a simulation overlaid.

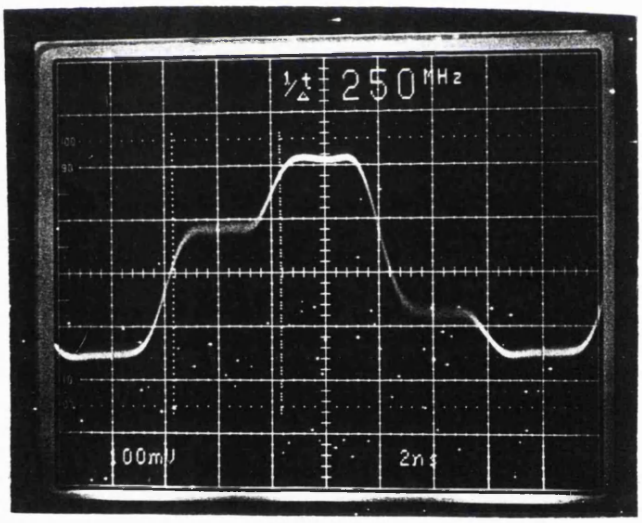


Fig 5.12 Scope photo of series MESFET OS/H sampling a 62.5MHz 0.4V input sinusoid at 250Ms/s.

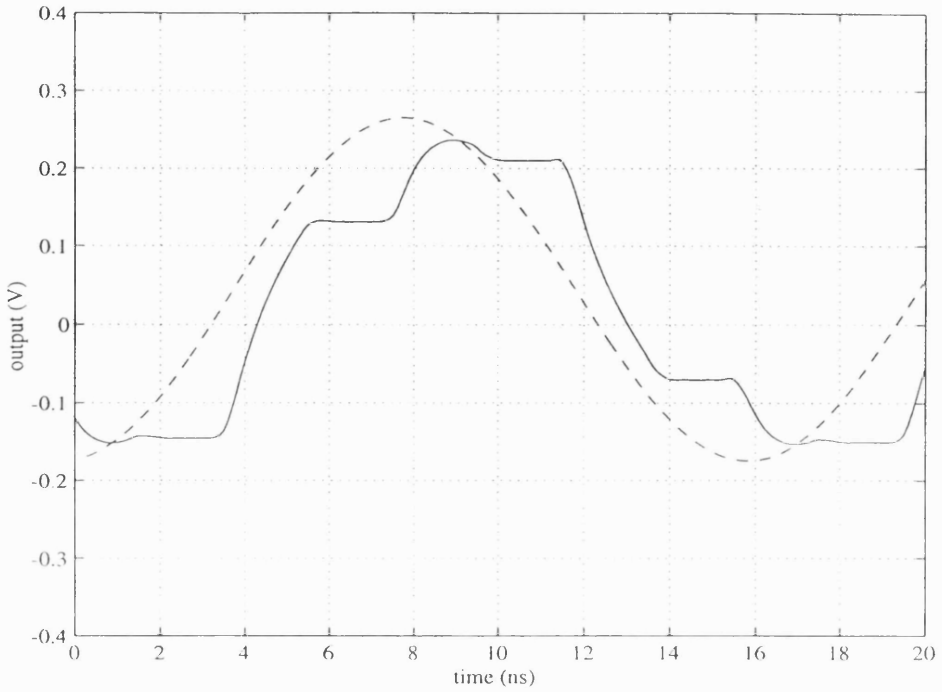


Fig 5.13 Simulation of series MESFET OS/H sampling a 62.5MHz input at 250Ms/s. This shows very close agreement to the measured result in Fig. 5.12.

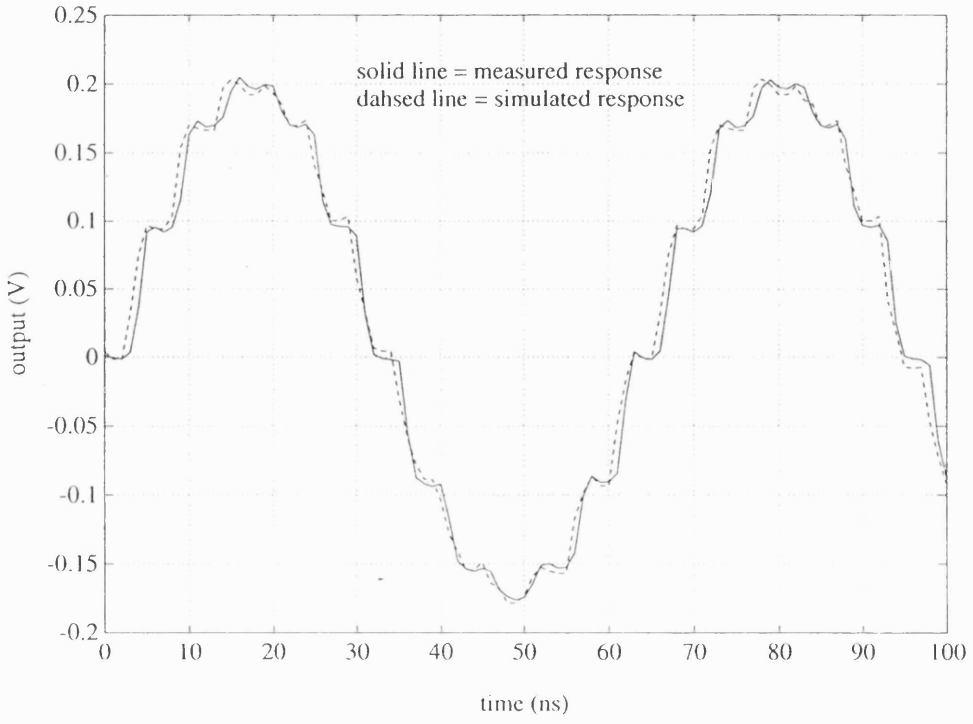


Fig 5.14 Digital scope record of the series MESFET OS/H sampling a 16.67MHz signal at 200Ms.s.

(iii) Simulation of Harmonic Distortion

To measure harmonic distortion the circuit was simulated as before, with a 16.67MHz 1V p-p sinewave input and a 200Ms/s sampling rate, but for a duration of 500ns, corresponding to about eight complete cycles of the input waveform. The frequency spectrum was then found by performing a fast Fourier transform (FFT) using MATLAB. This FFT (normalised to unity) is shown in Fig. 5.15, and reveals several aspects of the performance of the circuit. The 2nd harmonic (at 33.34MHz) of 0.22% and the 3rd harmonic (at 50MHz) of 0.02% show that significant harmonic distortion is present. There are two major causes of this harmonic distortion. Firstly, the *on* resistance of *M1* is a nonlinear function given by equation (3.5) and secondly, there will be a slight variation in V_{gs} as the input changes - due in turn to the variation in follower gain and diode drop. The components at 183MHz and 217MHz are the side-bands generated by the 200MHz sample rate and clock feedthrough of 2.8% (28mV) is visible at the clock frequency. In section 3.3.1(ii) the invariant component of pedestal was estimated at 10mV. The larger value found by simulation is due to the fact that the C_{gs} of the series MESFET is not depleted when the turn-off phase begins, so a larger charge is transferred.

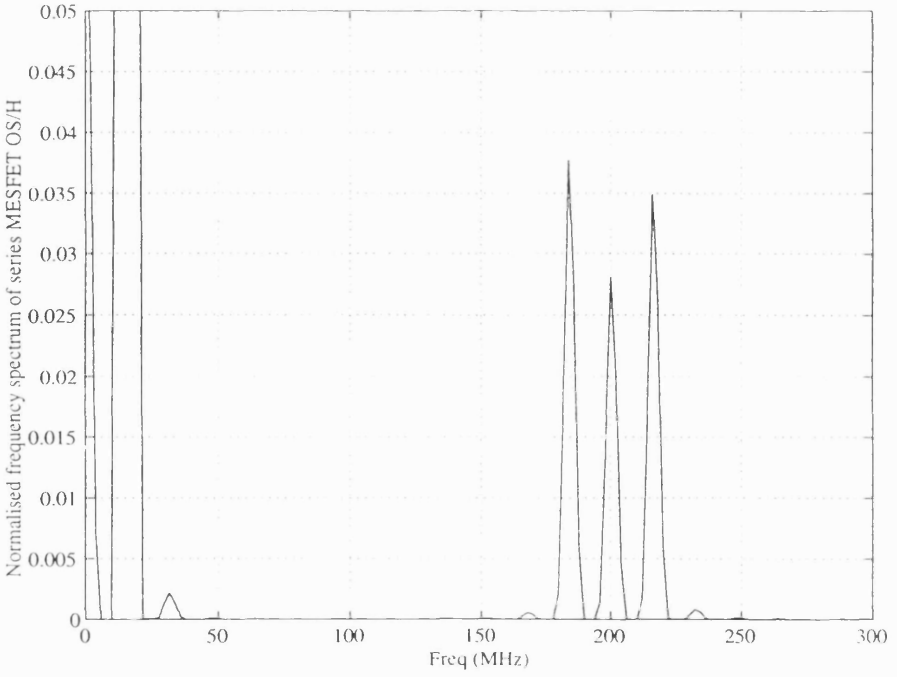


Fig 5.15 Frequency spectrum of the output of the series MESFET OS/H when sampling a 16.67MHz signal at 200Ms/s. This clearly shows 2nd harmonic distortion at 33MHz and clock feedthrough 200MHz.

(iv) Measured Harmonic distortion

To enable a comparison between the simulated and measured results, the harmonic distortion was measured by recording the output of the OS/H while sampling a 16.67MHz sinewave at a nominal sampling rate of 200Ms/s over a period of 500ns using the digitizing oscilloscope. The frequency spectrum, shown in Fig. 5.16 is found by taking the Fourier transform of the result using MATLAB. This figure also shows the output of the circuit when forced to remain in the sample mode by applying CW laser illumination of 5mW to the MSM photodetector.

The 2nd harmonic distortion recorded by this measurement is 0.5±0.05%, while the 3rd and subsequent harmonics are below the noise threshold. Although simulations of the circuit at this frequency suggest a 2nd harmonic distortion of 0.22%, the accuracy of these is likely to be poor as the distortion is dependent on the nature of the characteristics of the series MESFET in the linear region. The SPICE model we have used for these simulations is optimised for accuracy in the saturation region and therefore is unlikely to give accurate results in the linear region. The spectrum of the sampled output shows sidebands at 190MHz ± 16.67Mhz with clock feedthrough at 190MHz of 2.9%, approximately the same as the value given by the simulation. The sampling rate is slightly lower than the intended 200Ms/s, as the pulse generator requires a small time window after each burst of pulses before the next trigger event.

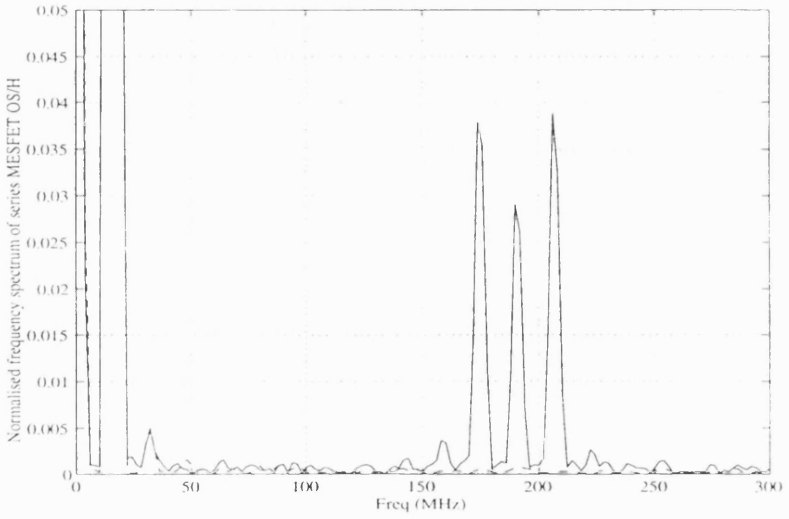


Fig 5.16 Measured frequency spectrum of the series MESFET OS/H with a 16.67MHz input sampled at 190Ms/s (the dashed line shows the circuit held in sample mode).

(v) Simulated Pedestal

In the previous section the magnitude of pedestal expected was estimated by measuring clock feedthrough in the frequency domain. In this section the pedestal is measured directly by simulating the circuit at a much lower sampling rate. Fig. 5.17 shows the circuit sampling a 1MHz sinusoid at 5Ms/s. By slowing down the circuit we can make the effect of pedestal much clearer and easier to measure. The areas around the sample to hold transitions at input voltages of around 0V and ±0.5V were expanded, allowing accurate measurement of the pedestal. From these figures we find that the pedestal varies from 28mV with a –0.5V input to 27mV with a +0.5V input, so the amplitude dependent component of the pedestal is around 1mV.

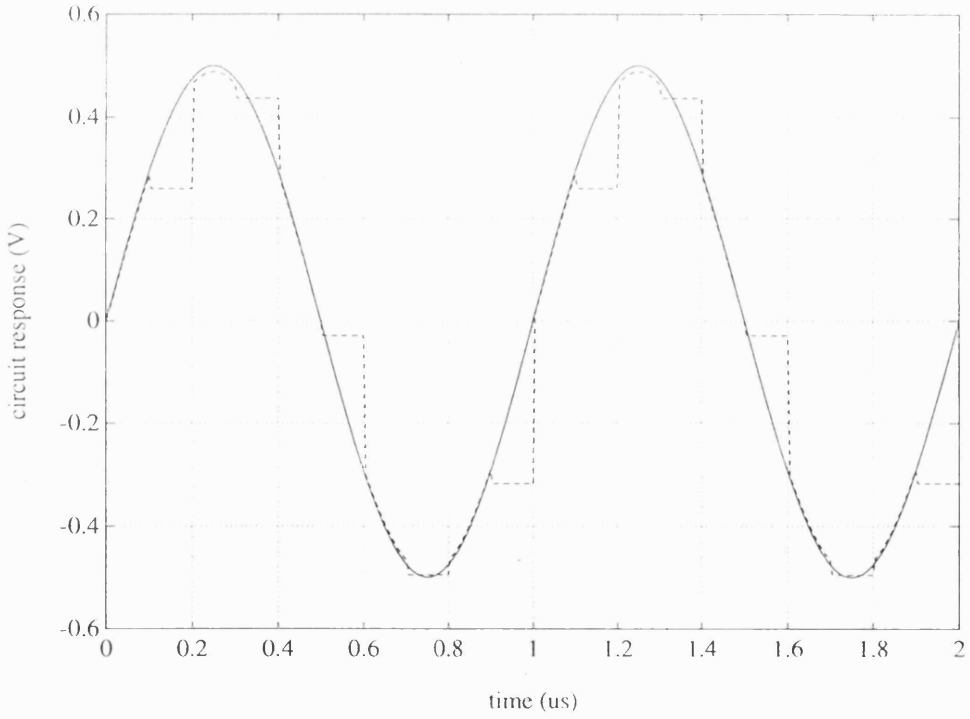


Fig 5.17 Simulation of series MESFET OS/H sampling a 1MHz sinusoid at 5Ms/s. This simulation demonstrates the effect of pedestal more clearly than the higher speed simulations.

(vi) Measured Pedestal and droop

In order to measure the pedestal directly, the input signal frequency (0.4V rms sinewave) was reduced to 1MHz, and the sample rate was reduced to 5Ms/s. This measurement, shown in Fig. 5.18, therefore matches the simulations made in section 5.2.2(v). A number of measurements of the pedestal were made, which revealed a constant value (ie. DC offset) of 15mV and a signal dependent component of 3±1mV which corresponds to an effective resolution of 7.6±0.5 bits. This arrangement was also used to measure the droop of the output during the hold phase, the value of which was found to be about 200μV/ns. This is quite large compared to that reported in [25], but will still cause and error of only 400μV in a period of 2ns, which is small compared to the effect of the pedestal.

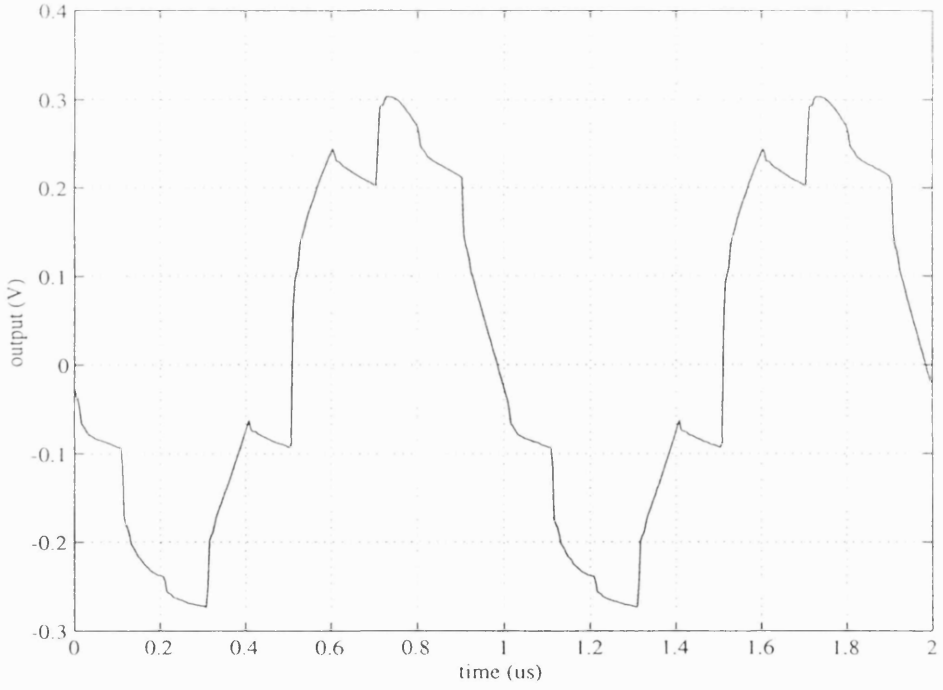


Fig 5.18 Measured pedestal and droop of series MESFET OS/H with the sample rate reduced to 5Ms/s to highlight effect. The signal dependent component of pedestal corresponds to an accuracy of 7.6±0.5-bits.

(vi) Simulated Bandwidth

The frequency response was measured by applying a constant photocurrent of 1m^ and performing an HSPICE AC analysis. Figure 5.19 clearly shows a –3dB bandwidth of 470MHz. The limited bandwidth of this circuit is one of its major drawbacks, meaning that it cannot be used for sampling high bandwidth signals. To increase the analogue bandwidth of the circuit we must either reduce the *on* resistance of the series MESFET (by increasing the gate width), or reduce the value of the hold capacitor. However, these measures will cause an increase in pedestal and an associated loss of resolution, as the pedestal depends on the ratio of C_{hold} to the parasitic C_{gs} of the series MESFET (Eq. 3.7). Therefore to increase the bandwidth without any loss of resolution requires a IC fabrication process with reduced parasitic capacitances.

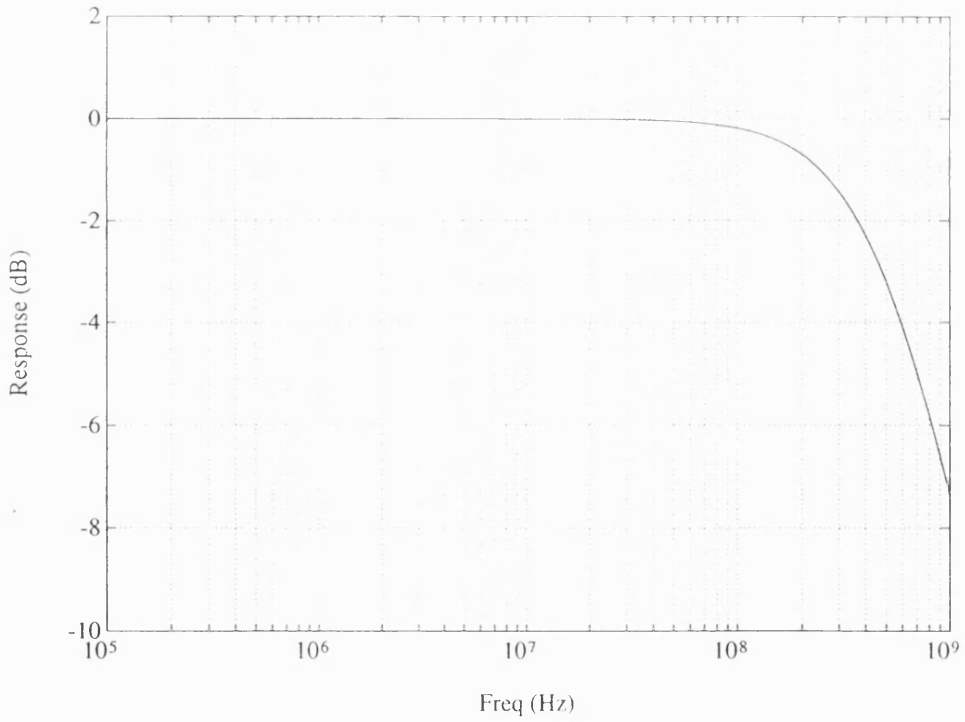


Fig 5.19 Simulation of the frequency response of the series MESFET OS/H in the sample mode.

(vii) Measured Bandwidth

Like the series photoconductor, the pass transistor circuit behaves as a first order low pass filter during the sample phase, but the hold capacitor is now charged via the ON resistance of the MESFET operating in the linear region

(approx. 450Ω). Therefore, with a hold capacitor of 0.75pF, we would expect a –3dB frequency of ≈ 470MHz. The analogue bandwidth of the pass transistor circuit was measured in a 50Ω environment using a HP 500MHz network analyser and Tektronix 400MHz FET probes. Fig. 5.20 shows the result of a frequency sweep from 10kHz to 500MHz with a 5dBm (0.4V rms into 50Ω) input signal. The upper trace shows the direct measured response and the lower trace shows the response after correction for the effects of the PCB and cabling. The calibration was done by replacing the IC with a straight-through connection and measuring the response. From these measurements we can see that the gain flatness is < 0.5dB up to 400MHz. Above this frequency the output is somewhat erratic, but this is probably due to instrumentation effects.

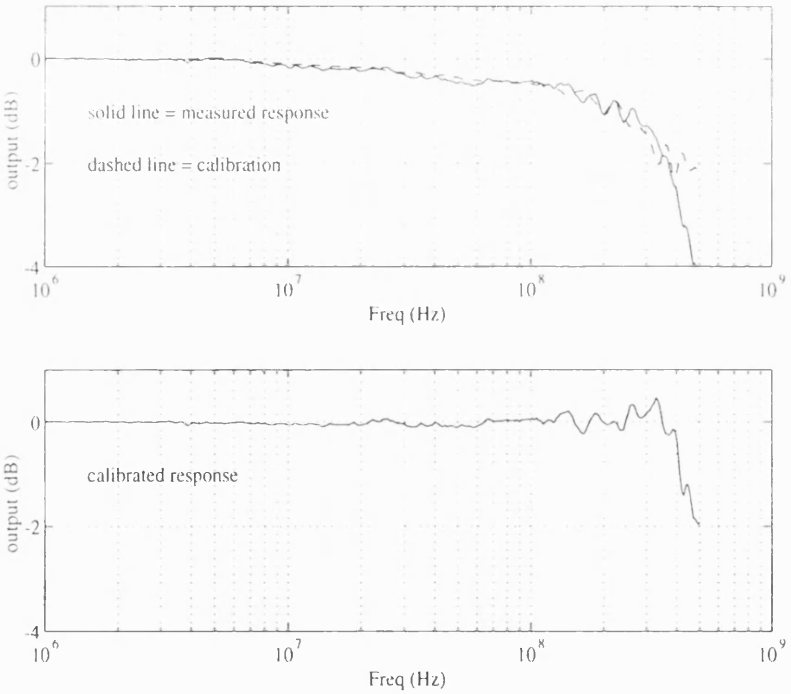


Fig 5.20 Measured frequency response of the series MESFET OS/H.

(ix) Simulated Acquisition Time

In common with the analogue bandwidth, the acquisition time is limited by the *RC* time constant of the circuit. This was measured applying a 1V peak to peak input square wave of the same frequency as the clock. By delaying the clock by one quarter of a cycle we can measure the time it takes for the circuit acquire a +0.5V input when starting from a held value of –0.5V. This is shown in

Fig. 5.21. Using this technique we can measure the time to acquire the signal to with 1 LSB, with 8-bits resolution to be 1.93ns. This is slightly higher than the 1.89ns estimated in section 3.3.1(i), but this calculation only accounted for the C_{gs} parasitic of the sampling MESFET. The complete simulation uses all of the parasitics in the circuit. In a practical situation it will be difficult to measure this rise-time directly – instead we measure the 10% to 90% rise-time. Using the simulation in Fig. 5.21 we see that this is 0.78ns

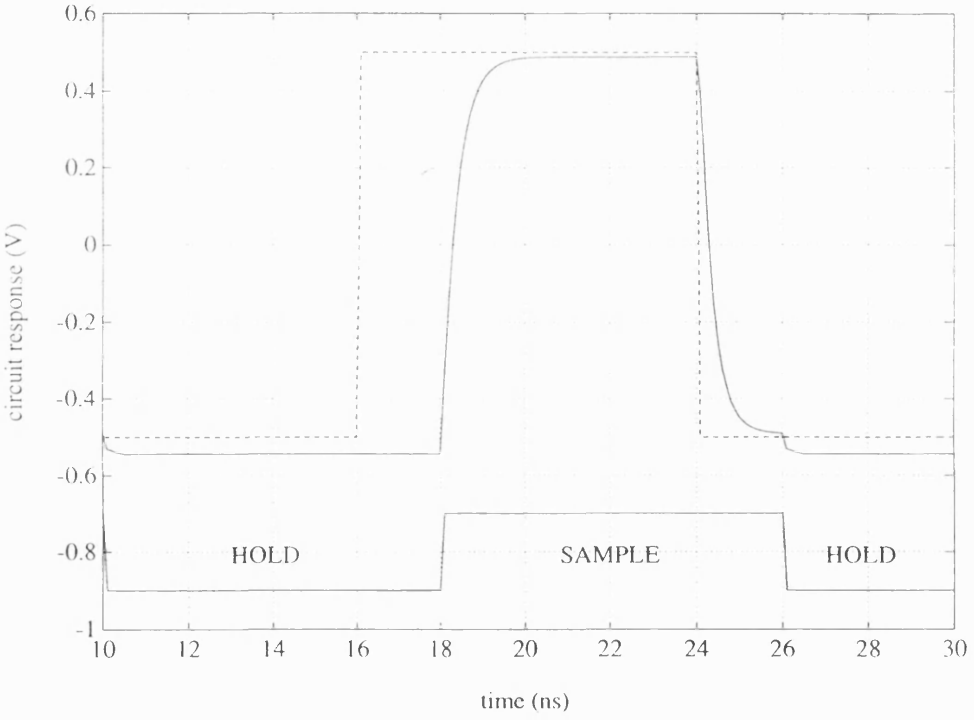


Fig 5.21 Simulation showing the acquisition of a 1V peak to peak square wave.

(x) Measured Acquisition Time

The acquisition time (section 3.1.2) is the time the OS/H takes to acquire the input signal to within a given error band after a sample to hold transition. This will depend on the amplitude and frequency of the input signal, the most demanding case being with a full speed, maximum amplitude signal. A worst case measurement of this was performed by sampling a 0.5V amplitude square wave input signal. The input signal and laser drive pulse were generated using two channels of a pulse generator with the delay between the pulses being adjusted until the transition from hold to sample occurred during a minimum

in the input signal.

Using this method both the rise-time and fall-time were measured at 1.29±0.02ns (10% to 90%). This result, however, needs to be de-embedded from the effect of the oscilloscope rise-time of 875ps. To do this we can represent each time constant by a first order filter separated by a unity gain buffer, as shown in Fig. 5.22.

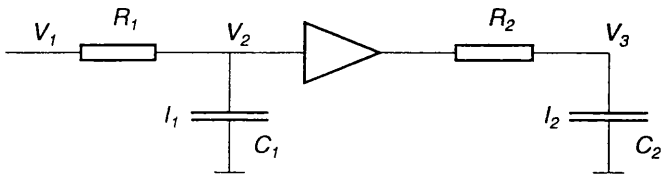


Fig 5.22 Equivalent circuit used to de-embed the OS/H time constant from the measuring system.

The 10% to 90% rise time, t_r, is related to the RC time constant by $t_r = 0.35\ (2\pi\ RC)$. The current flowing on to each capacitor is therefore:

$$I_1 = C_1 \frac{\partial V_2}{\partial t} = \frac{V_1 - V_2}{R_1} \tag{5.5}$$

$$I_2 = C_2 \frac{\partial V_3}{\partial t} = \frac{V_2 - V_3}{R_2} \tag{5.6}$$

If the input signal (V_1) is a step waveform we can eliminate V_2, I_1 and I_2 and writing R_nC_n as τ_n we find:

$$V_3(t) = 1 + \frac{\tau_2 e^{-t/\tau_2}}{(\tau_1 - \tau_{2)}} + \frac{\tau_1 e^{-t/\tau_1}}{(\tau_2 - \tau_1)} \tag{5.7}$$

where $V_3(t) = V_1(1 - e^{-t/\tau_T})$ and τ_T is the total (measured) time constant. Therefore, from the measured time constant and the known oscilloscope time constant, we can calculate the intrinsic OS/H time constant to be 369 ± 13ps (equivalent to a 10% to 90% rise-time of 812 ± 29ps). Assuming the hold capacitor is 0.76 ± 0.09pF (12% tolerance), this measurement gives a value of the

ON resistance of the pass transistor MESFET of 486 ± 61Ω.

Knowing the *RC* time constant allows an estimation of the true acquisition time, i.e. the time to settle to within a given error band. For example, for 8 bit resolution the time to settle within 1 lsb is given by:

$$t = R_{on}C_{hold} \ln(256) = 2.05 \pm 0.07\text{ns} \quad (5.8)$$

Therefore the acquisition time is fast enough to allow 8-bit resolution at 250Ms/s. This result is also somewhat pessimistic, as is does not take into account the finite rise-time of the ancillary equipment such as cables, PCBs, dil sockets etc.

(xi) Simulated Sampling Time Adjustment

We saw in section 3.3.1(iii) that the exact turn-off time of the pass transistor depends on the ratio of the photocurrent pulse to the saturation current of the cascoded current source formed by *M3* and *M4*. This means that by varying I_{source} we can adjust the sampling instant of the OS/H. In a system driven by a fast laser this would depend on the response time of the MSM. In the demonstration circuit the rise-time of the photocurrent pulse is determined by the pulse generator rise-time of about 200ps. We would therefore expect to be able to adjust the sampling instant by at least 100ps, which is equivalent to about 20mm travel in a glass fibre. The simulation in Fig. 5.23 shows the effect of varying the bias voltage applied to *M3* from –5.60V to –5.43V, which causes the holding current to vary from 323μA to 639μA. This results in a shift in effective sampling instant of ~150ps.

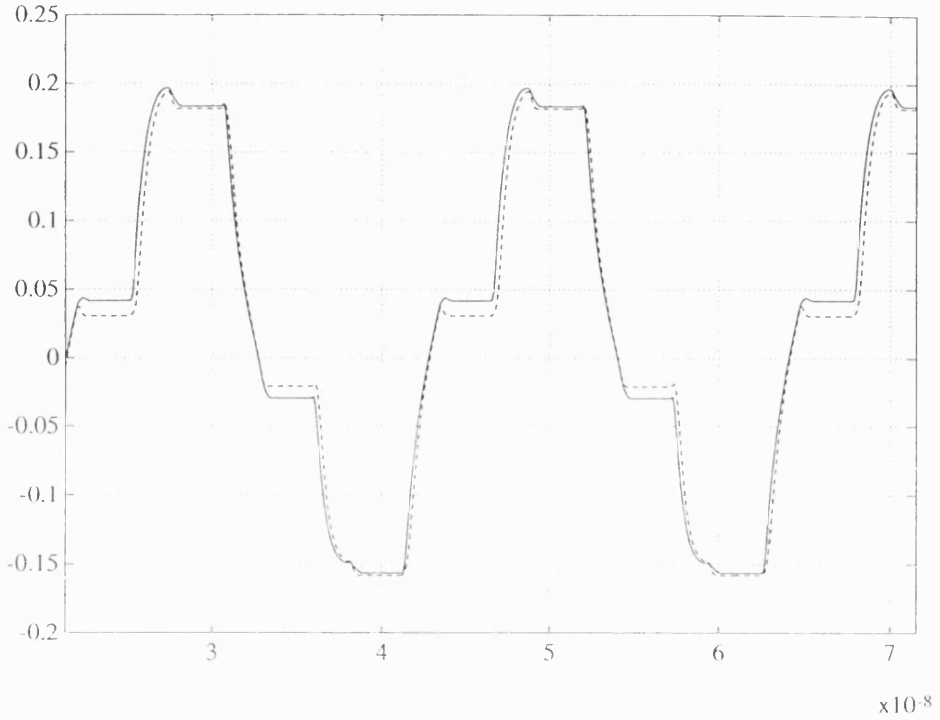


Fig 5.23 Simulation of sampling time adjustment of series MESFET OS/H.

(xii) Measured Sampling time adjustment

To measure sampling time adjustment attainable from the OS/H it was driven by a 47MHz 0.4V rms sinusoid and the bias voltage adjusted from -5.43V to -5.60V. The effect of this is shown on Fig.5.24. At the zero crossing the held voltage varies by ≈ 8mV corresponding to a variation in the sampling instant of 134ps.

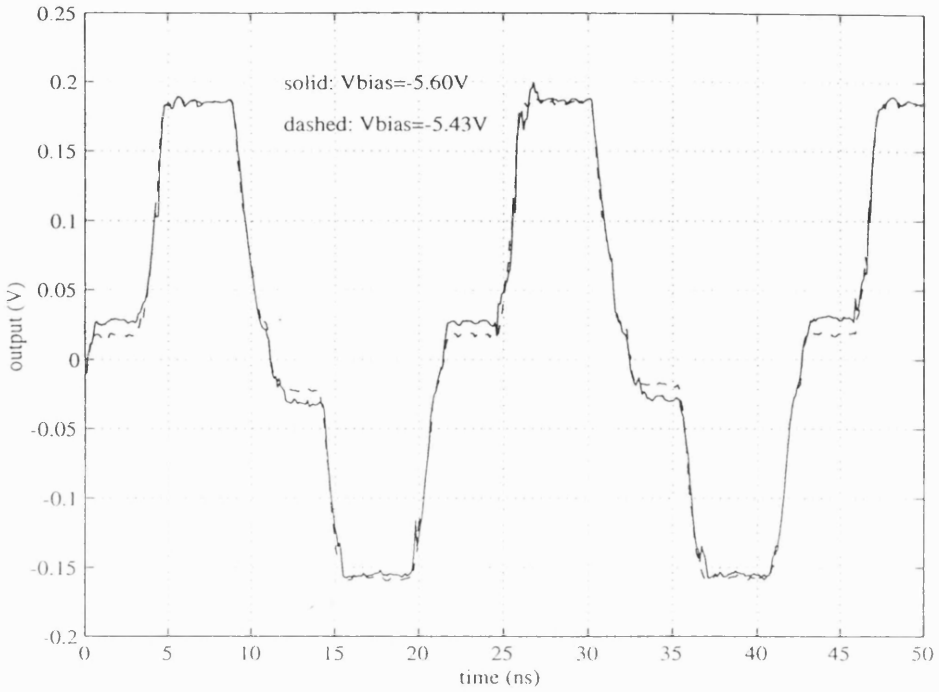


Fig 5.24 Measured sampling time adjustment of series MESFET OS/H.

(xiii) Aperture jitter

Since the minimisation of the timing jitter is such a fundamental issue, it is important to estimate the contribution from the OS/H itself. The aperture jitter can be measured by comparing the noise recorded by the OS/H with the input grounded (through a 50Ω termination), to the noise recorded when a sinusoidal input signal is sampled at the zero crossing. In the absence of timing jitter, these two measurements will be identical, but if the sampling instants are affected by timing jitter the OS/H will record an additional component, equal to the aperture jitter multiplied by the input slew rate.

To perform this experiment a 50MHz 0.2V r.m.s. sinusoid was sampled at 100Ms/s using a clock which was locked to the input signal in the manner described at the beginning of section 5.2. The phase angle between the two signals was adjusted so that the transition from sample to hold occurred precisely at the zero-crossing points of the sinewave. The output from this was displayed on an analogue oscilloscope set at 2mV/division. Fig. 5.25 shows the output we would expect to see. As the analogue oscilloscope display is a composite of several overlaid cycles of the signal, timing jitter will cause broadening of the part of the trace which represents the output in the hold

phase (shown as Δv in Fig. 5.25).

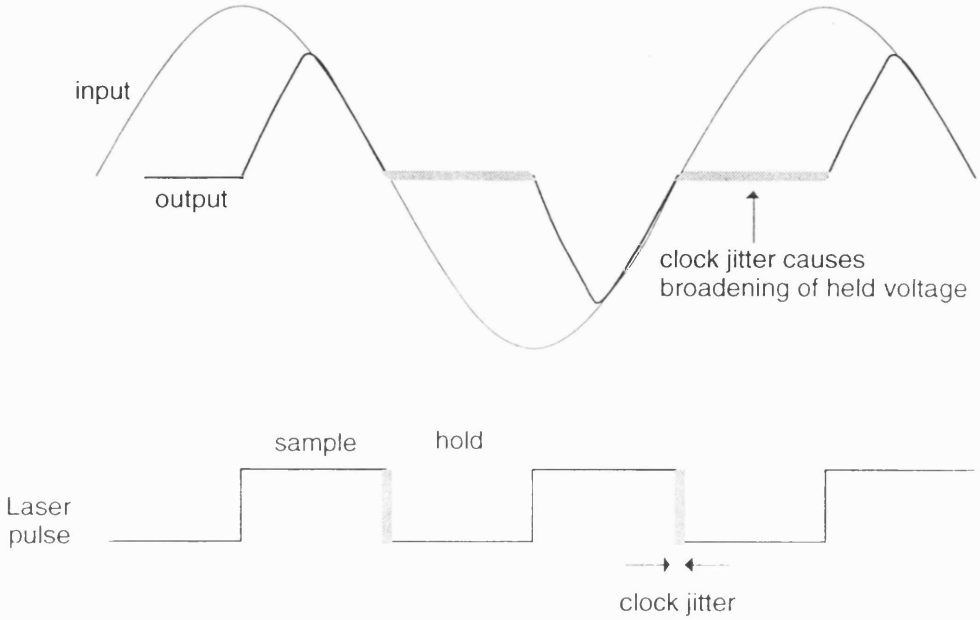


Fig 5.25 Measurement of timing jitter.

With the input grounded no broadening of the line was observed, but with the sinusoidal input a broadening of 5±1mV was measured. This corresponds to a timing error Δt of

$$\Delta t = \Delta v \,/\, (2\pi A f) \;=\; 56 \pm 11\text{ps peak to peak jitter} \qquad (5.9)$$

where A = signal amplitude, f = signal frequency. This is equivalent to 20 ± 4ps rms jitter. The pulse generator jitter is specified as < 20ps rms at this frequency, so we can attribute the measured jitter to this source.

5.2.3 Diode Bridge OS/H

The basic operation of the diode bridge circuit has been described in the preceding sections. To confirm these calculations and to examine the circuit in more detail, a range of simulations have been performed which match exactly those employed with the series MESFET OS/H. As with the simpler circuit, the simulations of the diode bridge circuit demonstrate its suitability for sampling

at rates in excess of 250Ms/s.

(i) Simulation of Operation at 250Ms/s

The simulation of Fig. 5.26 shows the diode bridge circuit under identical conditions to those used for the simulation of the series MESFET circuit in Fig. 5.11, namely a 1V peak to peak, 50MHz input sinusoid and a sample rate of 250Ms/s. In contrast with the series MESFET OS/H, this circuit exhibits zero phase shift and effectively zero pedestal. The slew rate during the sample phase depends on the current available for charging the hold capacitor. As this simulation was carried out using a photocurrent of 1mA, and the fixed current sources draw approximately 0.35mA, then we can see from equation (3.9) that the maximum slew rate should be about 870mV/ns. This is approximately the value observed. A small, residual pedestal of ~2mV can also be observed from this simulation, which is approximately equivalent to the value calculated in section 3.4.4(iii).

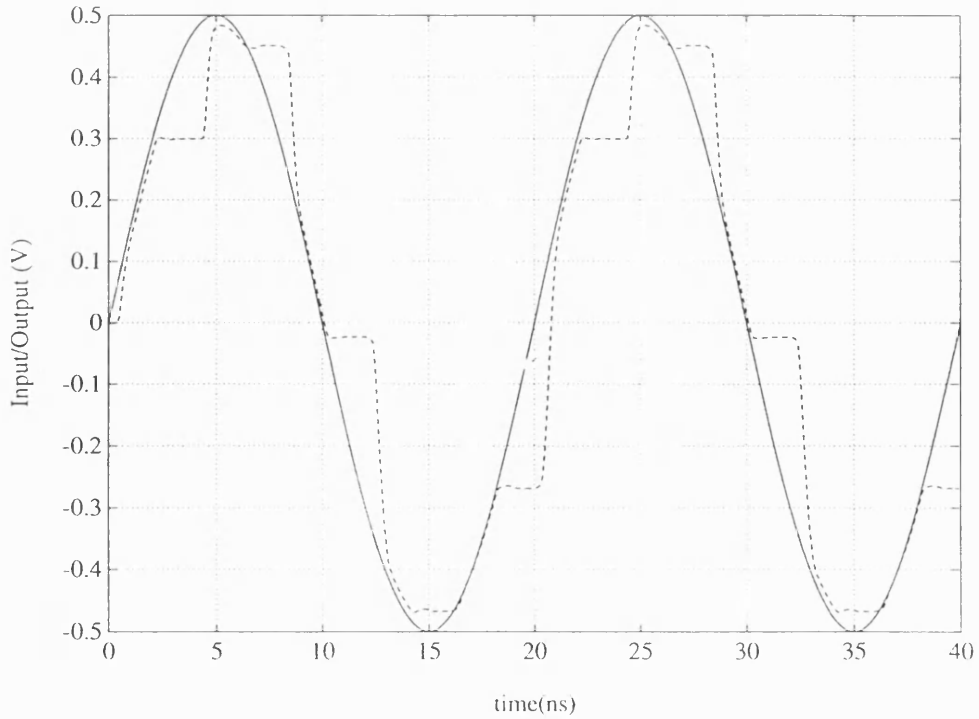


Fig 5.26 HSPICE simulation of diode bridge OS/H sampling a 50MHz sinusoid at 250Ms/s.

(ii) Simulation of Harmonic Distortion

Figure 5.27 shows the FFT of the output of the diode bridge circuit when sampling a 16.67 MHz input sinusoid at 200Ms/s. This frequency spectrum shows classic sample and hold characteristics. The input signal at is normalised to unity and aliases of this signal can be seen at $f_s \pm f_o$. The magnitude of the component at the sample frequency is virtually zero, demonstrating the effectiveness of the bootstrap feedback circuitry in cancelling the clock feedthrough (pedestal). Levels of harmonic distortion are also much lower than those recorded from the pass transistor OS/H, being below the noise level of around 0.1%.

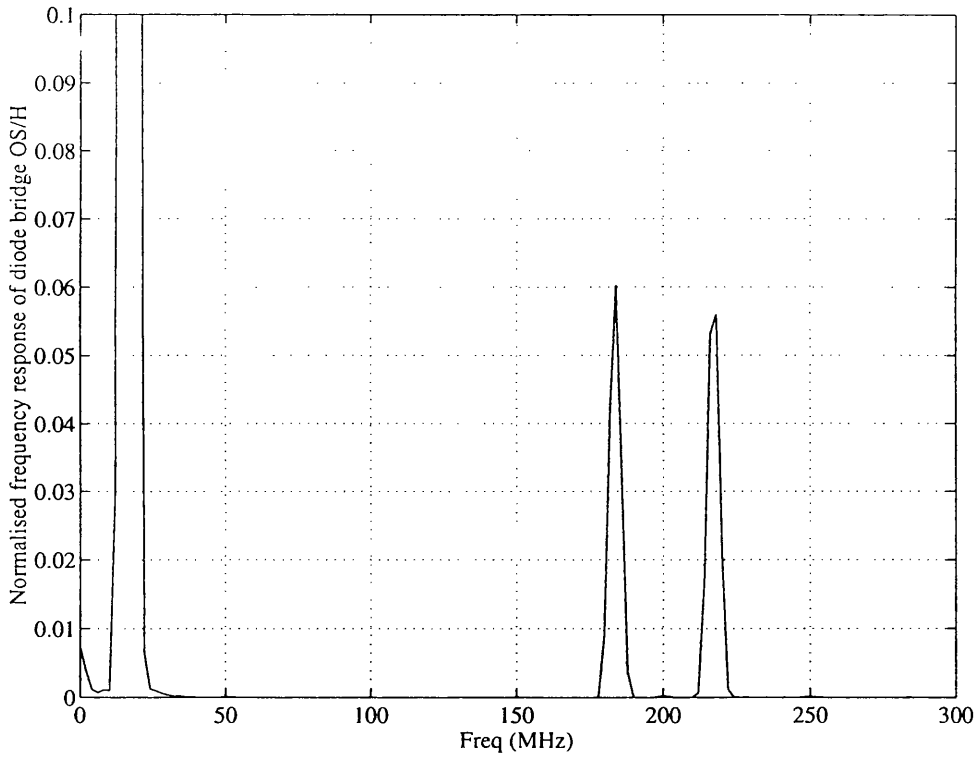


Fig 5.27 Simulated frequency spectrum of the output of the diode bridge OS/H when sampling a 16.67MHz sinusoid at 200Ms/s

(iii) Pedestal

As with the series MESFET circuit the pedestal was measured by slowing down the input and sampling rates to 1MHz and 5MHz respectively (Fig. 5.28). With the diode bridge circuit the pedestal is almost completely eliminated by means

of the bootstrap feedback. This leaves a residual value of pedestal (including both variant and invariant components) of under 1mV, which corresponds to an accuracy of >10-bits. The effectiveness of the bootstrap feedback is also demonstrated here by including a simulation of the circuit with the feedback removed. This is shown as the dashed line on Fig. 5.28, and displays a pedestal of ~30mV when V_{in} = 0.5V.

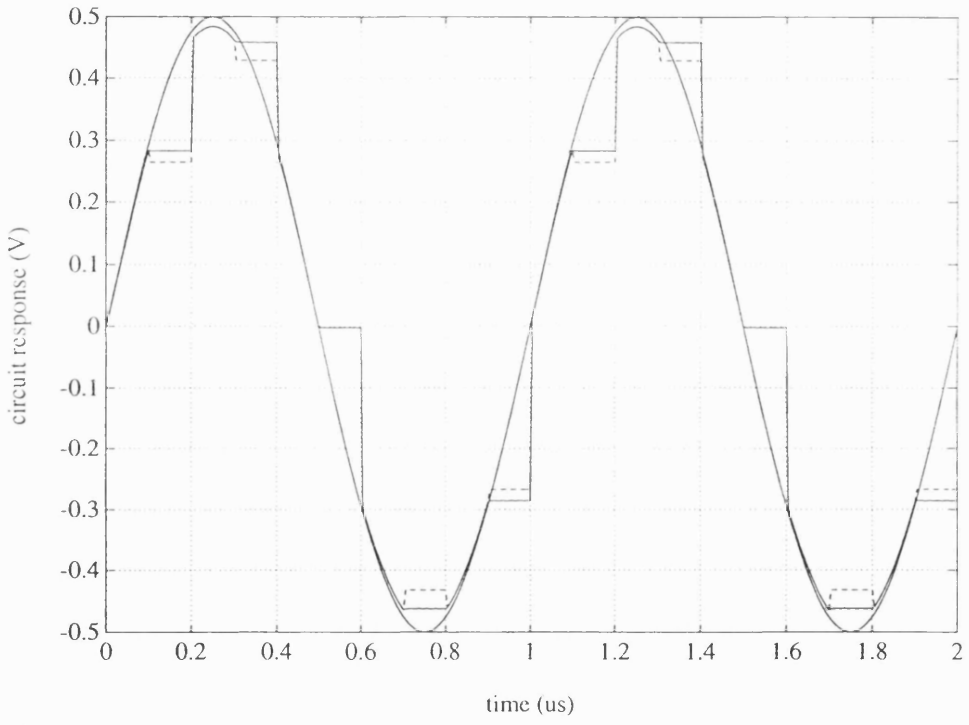


Fig 5.28 HSPICE simulation of the diode bridge OS/H sampling a 1MHz sinusoid at 5Ms/s (solid line = bootstrapped circuit, dashed line = bootstrapping removed). This simulation is used to highlight the effect of pedestal.

(iv) Frequency Response

The result of an AC analysis with a constant photocurrent of 1mA is shown in Fig. 5.29, revealing a –3dB bandwidth of 1.3GHz. This very high bandwidth is one of the main attractions of the diode bridge circuit as it means the circuit can be used to process signals well beyond the Nyquist limit. As expected, the –3dB bandwidth for this circuit is much higher than for the series MESFET circuit.

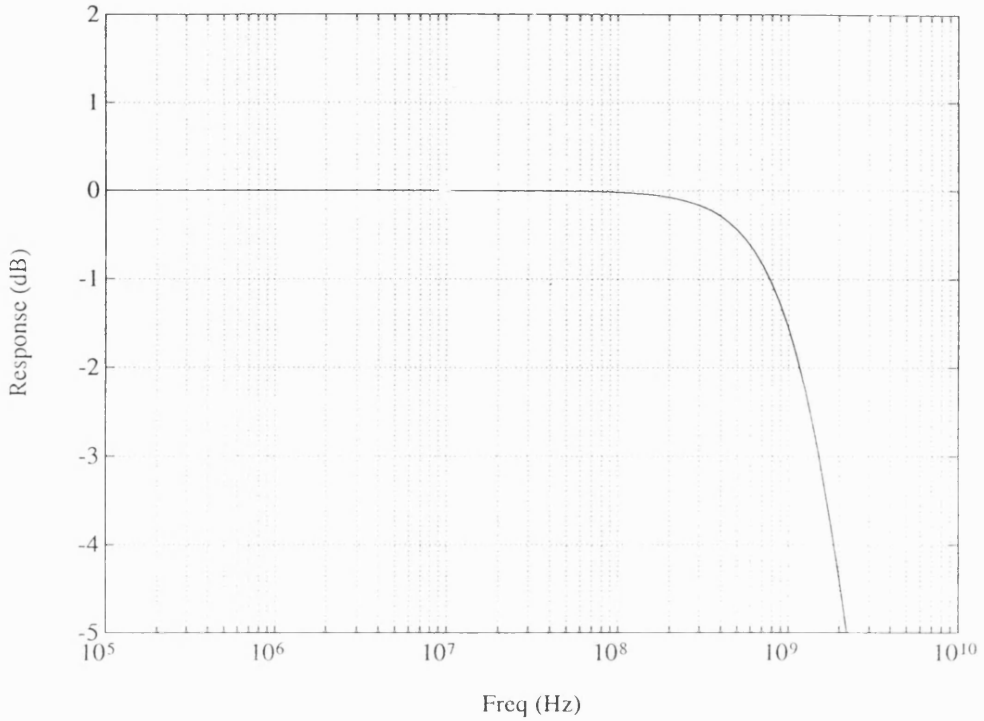


Fig 5.29 HSPICE simulation of frequency response of diode bridge OS/H.

(v) Acquisition Time

The acquisition time of the diode bridge circuit was measured in the same way as for the series MESFET circuit, and is shown in Fig. 5.30. This measurement clearly shows the slew rate limiting of the diode bridge circuit, as opposed to the *RC* charging of the series MESFET OS/H. As predicted in section 3.4.4, the hold capacitor charging rate is constant while $V_{in} \leq V_h$. Beyond this point the charging rate becomes exponential. The slew-rate in the linear region is 0.9V/ns, the 10%–90% rise time is 0.8ns and the time to acquire the input signal to within 8-bits is 1.6ns.

(vi) Sampling time adjustment

The sampling time of the diode bridge can be adjusted by varying the ratio of photocurrent to holding current. The most practical method of changing this ratio is by adjusting the MSM bias voltage, which with 5mW optical power, allows a variation of photocurrent from 1.4mA to 1.9mA as the bias voltage is varied from 5V to 10V. This small variation in photocurrent causes a variation

in sampling time of around 25ps, sufficient to correct for errors in fibre length of up to 5mm.

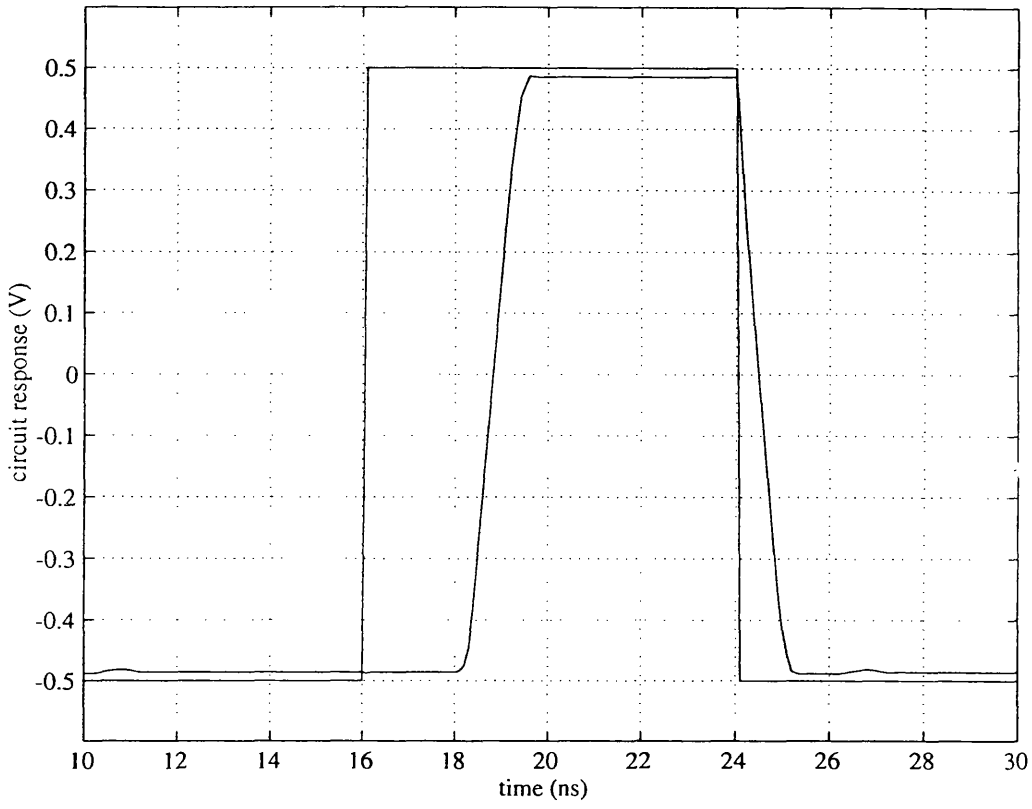


Fig 5.30 HSPICE simulation of diode bridge OS/H showing acquisition of a 1V peak to peak square wave input signal.

5.2.4 Measured Performance of Diode Bridge OS/H

The operation of the diode bridge circuits has proved to be much less satisfactory than the series MESFET OS/H. Although a sample and hold action has been observed, shown in Fig. 5.31, the circuit suffers from very severe clock feedthrough, which is most acute around the maximum and minimum of the input signal. The reason for this is unclear, but could be due to the extreme difficulty in balancing the photocurrents and fixed current sources. A large mismatch in these will cause unequal voltage swings across the diodes connected to the hold capacitor (shown as *D3* and *D4* in Fig. 3.14), which may result in some current flow through one of the diodes during the hold phase.

In spite of these difficulties some aspects of the performance can be observed. For example, we can see from Fig. 5.31 that the sample rate of 200Ms/s presents no difficulties to the circuit, and that the acquisition time is well within the sample period. Measurements of the analogue bandwidth and harmonic distortion have also been made by illuminating the MSMs with CW laser light and so forcing the circuit to remain in the sample mode. From these measurements we observe a gain flatness within ± 0.5dB up to 500MHz, and levels of 2nd and 3rd harmonic distortion of around 0.8%.

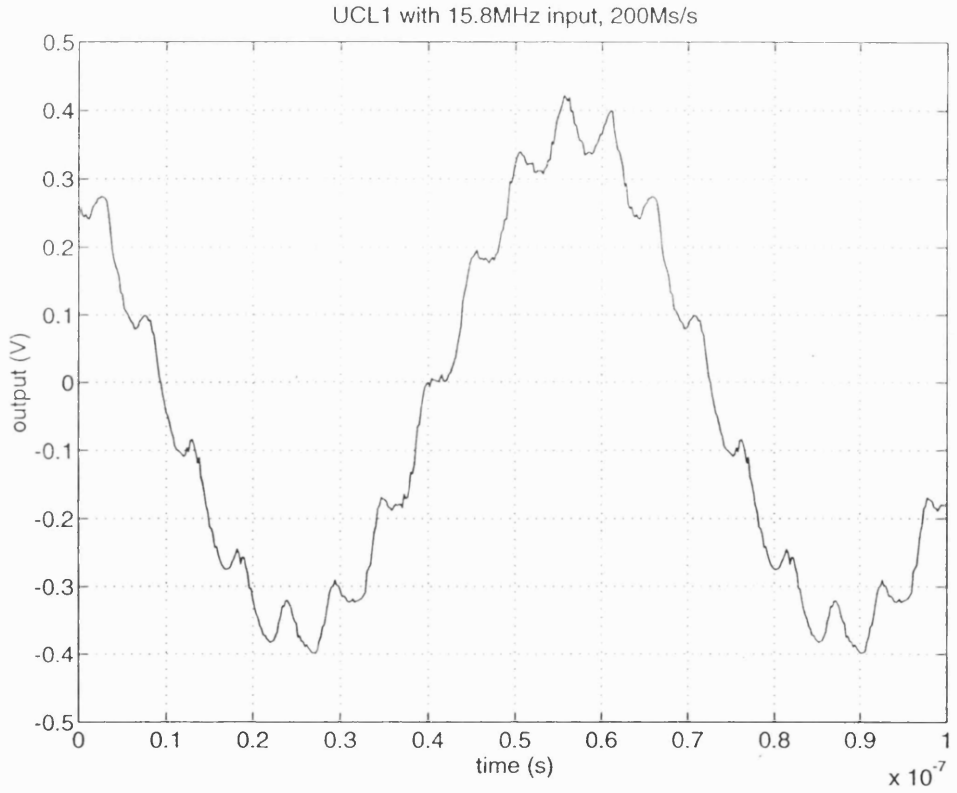


Fig 5.31 Measured response of the diode bridge OS/H sampling a 16MHz input at 200Ms/s. Although a sample and hold action is clearly taking place, this is distorted by severe clock feedthrough.

5.3 SUMMARY AND CONCLUSIONS

A range of optically triggered sample and hold circuits have been fabricated using GaAs MESFET technology. The purpose of these circuits is to allow us to exploit the inherent jitter-free performance of optical clock distribution in high speed sampled data systems. To meet this demand the OS/H circuits must be capable of sampling an input signal at a sample rate of 250Ms/s with a resolution of around 8-bits. In addition to this the jitter introduced by the circuits must be very low (< 1ps) and the optical clock required must be of sufficiently low power to allow the use of a laser diode for the optical address.

The series photoconductor OS/H is the simplest of the circuits and was designed as a control circuit to demonstrate the principle of optically triggered sampling. The performance of this circuit is, as expected, very limited, but it does show that we can use the GaAs foundry process for optoelectronic applications with some success.

The series MESFET OS/H proved to be the most successful of the circuits, and the measured performance matches the simulations very closely. The circuit has an analogue bandwidth of around 500MHz and can sample a 62MHz input signal comfortably at 250Ms/s. The resolution of this circuit is close to 8-bits and the acquisition time for this resolution is 2ns. This means that the circuit could successfully be used in, for example, an 8-path interleaved ADC, giving a sample rate of 2Gs/s. Measurements on aperture jitter suggest that this is set by the jitter of the optical drive – the OS/H itself making no measurable contribution.

The performance of the diode bridge is less satisfactory than the series MESFET OS/H, due to excessive clock feedthrough. In spite of this some useful measurements have been made which show that the circuit is capable of sample rates in excess of 250Ms/s and has a high analogue bandwidth.

CHAPTER 6

NONUNIFORMLY SAMPLED SIGNALS: THEORY AND APPLICATIONS

The overwhelming majority of signal processing theories assume that a digital signal is obtained through sampling an analogue waveform at uniform time intervals. However, in practice, nonuniform sampling occurs in many data acquisition systems, and the errors it produces can be dominating in high-speed, high-precision instrumentation. This chapter includes a review the published work on the subject of nonuniform sampling [154-158], and applies some of these theories to the problem of interleaved sampling and the optically triggered ADC.

In an interleaved ADC there are two causes of nonuniform sampling. The first is random timing jitter caused by, for example, shot noise or thermal noise in the clock and electronic components, or by dispersion along the clock distribution lines. When this type of nonuniformity is present in an ADC it cannot be corrected by any post processing techniques. Instead we must try to eliminate the sources of jitter, and to characterise its effect. The second cause of nonuniform sampling in a time interleaved ADC is due to static errors in the delay between each path. In an optically triggered ADC it is expected that these will be caused by inaccuracies in the length of the delay lines, and possibly by thermal expansion. These static and slowly varying nonuniformities can be corrected by post processing, and the aim of this chapter is to examine these techniques and to investigate their application to the optically triggered ADC.

6.1 SPECTRA OF SAMPLED SIGNALS

Before tackling the problem of nonuniform sampling, it is worth looking at the effects of uniform sampling in single path and N-path systems. The sampling of a continuous signal can be thought of as multiplying the signal with a series of delta functions separated by a constant time interval. A series of delta

functions (Dirac comb) of period T is given by

$$u(t)=\sum_{n=-\infty}^{\infty}\delta(t-nT)=\frac{1}{T}\sum_{n=-\infty}^{\infty}e^{j2\pi nt/T} \tag{6.1}$$

The Fourier transform of this is

$$U(f)=\sum_{n=-\infty}^{\infty}e^{-j2\pi fnT}=\frac{1}{T}\sum_{n=-\infty}^{\infty}\delta\left(f-\frac{n}{T}\right) \tag{6.2}$$

ie Dirac comb of period $1/T$ and mass $1/T$. To find the spectrum $G(f)$ of signal $g(t)$ sampled with $u(t)$ we can use the convolution theorem, ie

$$G(f)=G^a(f)\otimes U(f) \tag{6.3}$$

where $G^a(f)$ is the analogue (unsampled) transform of $g(t)$. The discrete convolution $y(s)$ of two functions $h(s)$ and $x(s)$ is

$$y(s)=\sum_{\tau=-\infty}^{\infty}h(\tau)x(s-\tau) \tag{6.4}$$

where τ is a dummy variable. So we have

$$G(f)=\sum_{\tau=-\infty}^{\infty}\left[G^a(\tau)\frac{1}{T}\sum_{n=-\infty}^{\infty}\delta\left(f-\frac{n}{T}-\tau\right)\right] \tag{6.5}$$

now, $\delta\left(f-\frac{n}{T}-\tau\right)$ =1 for $\tau=f-\frac{n}{T}$

=0 elsewhere.

So we can re-write (6.5) as

$$G(f)=\frac{1}{T}\sum_{n=-\infty}^{\infty}G^a\left(f-\frac{n}{T}\right) \tag{6.6}$$

The resulting spectrum is periodic on the frequency axis with the period $1/T$, and each frequency f_0 in the baseband generates components at $(n/T\pm f_0)$. This

is illustrated in Fig 6.1.

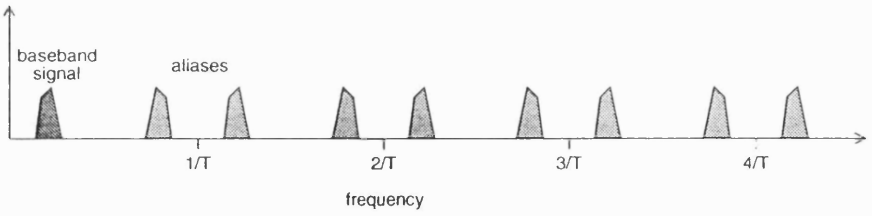


Fig 6.1 Frequency spectrum resulting from sampling with a frequency of $1/T$.

6.1.1 Spectrum of *N*-path Interleaved Sampler

An interleaved sampler consists of N individual paths clocked at a rate of $1/T$ but offset in time by an interval of T/N, as illustrated in Fig. 6.2.

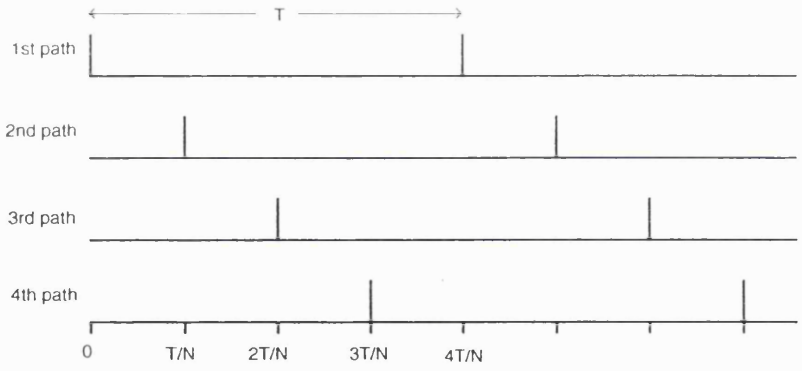


Fig 6.2 Timing intervals of *N*-path interleaved sampler.

The sampling function due to the mth path will therefore consist of a Dirac comb of period $1/T$ offset by mT/N, ie

$$u_m(t) = \sum_{n=-\infty}^{\infty} \delta\left(t - nT - \frac{mT}{N}\right) \tag{6.7}$$

To find the Fourier transform of this we can use the shift theorem

$$h(t - t_o) \Leftrightarrow H(f)e^{-j2\pi ft_o} \tag{6.8}$$

We have a Dirac comb shifted by mT/N, so from (6.2) and (6.8) we can see that the Fourier transform $U_m(f)$ of the Dirac comb produced my the mth path is

$$U_m(f) = \frac{1}{T}\sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T}\right) e^{-j2\pi fmT/N} \tag{6.9}$$

By employing the convolution theorem, the spectrum produced by the mth path, $G_m(f)$, is given by

$$G_m(f) = \sum_{\tau=-\infty}^{\infty} G^a(\tau) \frac{1}{T}\sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T} - \tau\right) e^{-j2\pi(f-\tau)mT/N} \tag{6.10}$$

this simplifies, as in (6.5), to

$$G_m(f) = \frac{1}{T}\sum_{n=-\infty}^{\infty} G^a\left(f - \frac{n}{T}\right) e^{-j2\pi nm/N} \tag{6.11}$$

The spectrum for the complete N-path sampler, $G(f)$, can be found by summing the contributions due to all N paths

$$G(f) = \frac{1}{T}\sum_{m=0}^{N-1}\sum_{n=-\infty}^{\infty} G^a\left(f - \frac{n}{T}\right) e^{-j2\pi nm/N} \tag{6.12}$$

now, $\sum_{m=0}^{N-1} e^{-j2\pi nm/N} = 1$ if n/N = integer

$= 0$ elsewhere.

So we can re-write $G(f)$ with n in multiples of N (e.g. if $N = 4$, $n = 0, 4, 8, \ldots$). Therefore, the complete spectrum of an N-path sampler is given by

$$G(f) = \frac{1}{T}\sum_{n=-\infty}^{\infty} G^a\left(f - \frac{nN}{T}\right) \tag{6.13}$$

Comparing this to the (6.6), we can see that a sampler with N interleaved paths increases the effective sample rate by a factor N. The spectrum resulting from an N-path interleaved sampler is illustrated in Fig. 6.3.

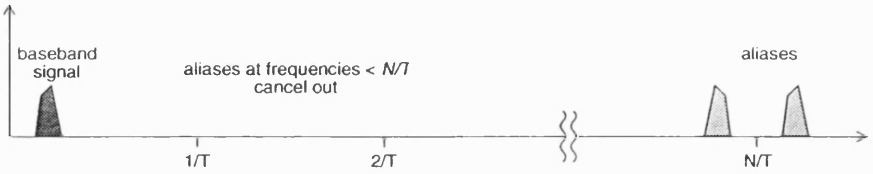


Fig 6.3 Frequency spectrum of N path interleaved sampler.

6.1.2 Sampling with non-uniform intervals

In the previous section we developed the spectrum of an N-path sampler with equally spaced sampling intervals. In a real sampler, however, we would not except the intervals between each path to be exactly equal. For example, in an optically triggered ADC, errors in the lengths of the delay lines would cause the sampling instants to be irregular within each cycle, but periodic over a time T, as shown in Fig. 6.4.

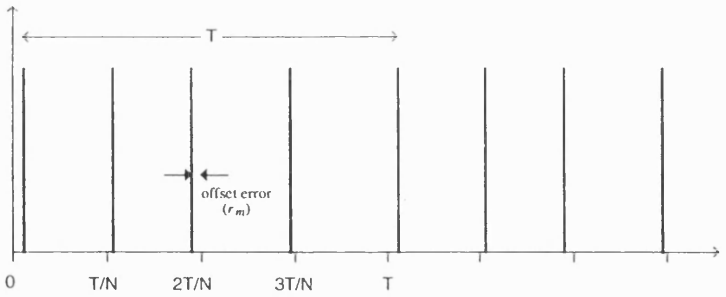


Fig 6.4 Sampling intervals of an N-path sampler with offset errors given by $r_m T/N$ and N=4.

If the delay of the mth path is given by $(m + r_m)T/N$, where r_m is a randomly distributed error, then it can be shown [154] that the complete spectrum is given by

$$G(f) = \frac{1}{T}\sum_{n=-\infty}^{\infty}\left(\frac{1}{N}\sum_{m=0}^{N-1} e^{-j2\pi(f-(n/T))r_m T/N} e^{-j2\pi nm/N}\right) G^a\left(f-\frac{n}{T}\right) \qquad (6.14)$$

Clearly, if the timing error $r_m = 0$, then this equation reduces to that for equal sampling intervals (6.13).

To gain some insight into the meaning of this consider the case of a nonuniformly sampled sinusoid, $e^{j2\pi f_o t}$. The digital spectrum of a sinusoid digitized by this waveform digitizer is given by

$$G(f) = \frac{1}{T} \sum_{n=-\infty}^{\infty} A(n)\delta\left[f - f_o - \frac{n}{T}\right] \tag{6.15}$$

where the coefficient $A(n)$ is defined as

$$A(n) = \sum_{m=0}^{N-1}\left[\frac{1}{N} e^{-j2\pi r_m f_0/Nf_s}\right] e^{-j2\pi nm/N} \tag{6.16}$$

where $f_S = 1/T$ and $k = 0, 1, 2, \ldots, N-1, N$.

For the sinusoidal input signal the spectrum comprises N line spectra uniformly spaced on the frequency axis with intervals of f_S. If we have a sine wave input, $\sin(2\pi f_0 t)$, instead, then the spectrum comprises N pairs of line spectra with uniformly spaced centres separated by the amount f_S on the frequency axis. The harmonic components appear at frequencies of $(nf_S \pm f_0)$ where n is an integer, and the coefficients in each pair are given by $A(n)/2j$ and $-A^*(N-n)/2j$ respectively. As an example, an interleaved sampler consisting of 8 parallel 250Ms/s paths (giving an overall sample rate of 2Gs/s) has been simulated. A 50MHz sine wave is digitized over 100 complete cycles with randomly generated sampling time offsets uniformly distributed in the range $\pm 0.2T/N$, and its spectrum is then computed and plotted in Fig. 6.5. The coefficients $A(n)$ have also been calculated and are given in Table 6.1. By comparing these values to the magnitude of the computed spectral components shown in Fig. 6.5, we can confirm the accuracy of equation (6.16).

TABLE 6.1

COEFFICIENTS $A(n)$ OF SPECTRAL COMPONENTS DUE TO NONUNIFORM SAMPLING

n	0	1	2	3	4	5	6	7
$A(n)$	1.00	$4.12e^{-3}$	$7.27e^{-3}$	$6.14e^{-3}$	$4.14e^{-3}$	$6.09e^{-3}$	$7.19e^{-3}$	$4.16e^{-3}$

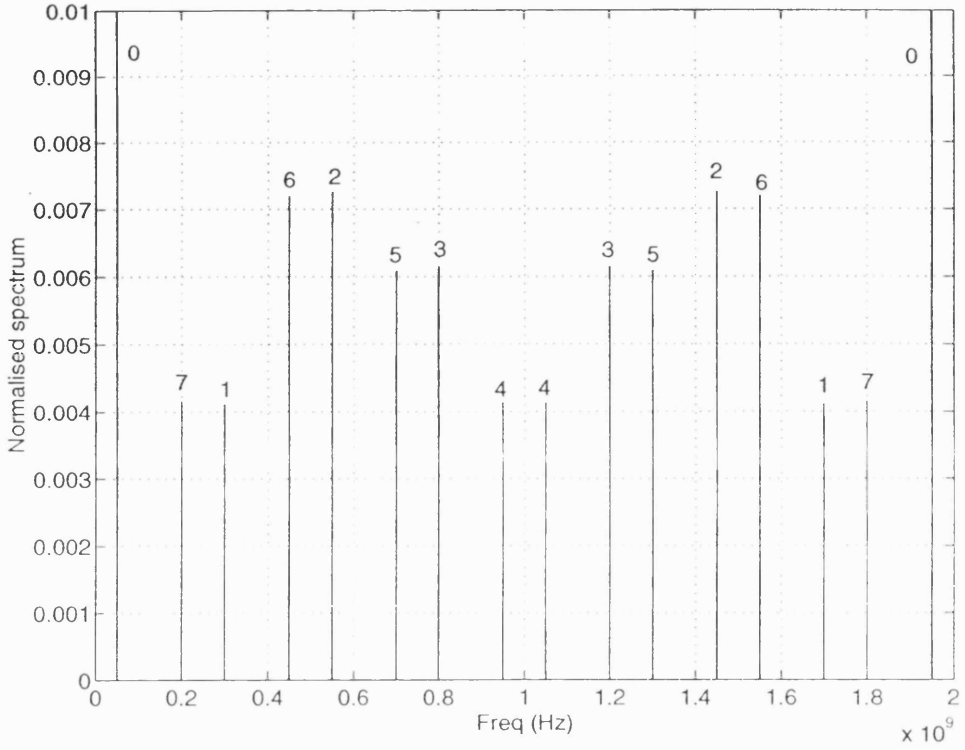


Fig 6.5 Spectrum of a nonuniformly sampled sinewave.

6.2 SAMPLING TIME OFFSET ESTIMATION ALGORITHM

By using the expressions for the non-uniformly sampled spectra, we can derive the sampling time offsets by examining the output of the converter with a known test signal input. The key to this is to recognise that equation (6.16) is DFT of the sequence :

$$\frac{1}{N} e^{-jr_m 2\pi f_o / N f_s} \tag{6.17}$$

for $m = 0, 1, 2, \ldots, N-1$. Therefore equation (6.17) is the inverse DFT of $A(n)$, and we can write:

$$e^{-jr_m 2\pi f_o / N f_s} = \sum_{n=0}^{N-1} A(n) e^{-j2\pi nm/N} \tag{6.18}$$

for $m = 0, 1, 2, \ldots, N-1$. Therefore, if we can measure the coefficients $A(n)$ resulting from the application of a known test frequency, f_o, then the offsets r_m

can be calculated.

The first stage in calculating the offsets involves recording a set of $M.N$ data points from the output of the digitizer and finding the DFT. As this data record will necessarily be of finite length, taking the DFT directly will not give accurate results. A finite data record can be thought of as an infinite data record multiplied by a rectangular pulse. Therefore, the Fourier transform of the finite data record is the transform of the infinite data, convolved with the transform of the rectangular pulse, which is a *sinc* function. Each frequency component in the signal will therefore generate a sinc function in the frequency domain, consisting of a central lobe and a set of side lobes of diminishing amplitude extending to infinity. This characteristic ringing will contribute to the noise in the frequency domain, and reduce the accuracy of the algorithm. The effect can be reduced if we multiply the data with a *windowing function* with smoother transitions than the rectangular pulse. The windowing function can be chosen so that its Fourier transform has very low amplitude sidelobes, and therefore generates minimal frequency domain noise.

Following windowing, the N points corresponding to the coefficients $A(n)$ are collected and an N point inverse DFT is performed, resulting in the complex numbers given by the left hand side of equation (6.18). By extracting the angles from these complex numbers and dividing by $2\pi f_0$ the sampling time offsets can be calculated. In a practical system it would be advantageous if the number $N.M$ was a power a two, allowing the use of a Fast Fourier transform (FFT) to compute the spectra.

This algorithm has been tested by simulating an 8-path interleaved sampler with an overall sample rate of 2Gs/s (i.e. each path is 250Ms/s) and input frequencies of 100MHz and 200MHz. Random timing offset errors were generated with a uniform distribution in the range ±0.1ns (ie $r_m = \pm 0.2$). Also, the total data length, $M.N$, was varied from $M = 16$ to $M = 256$ (128 points to 2048 points) to determine the effect on the accuracy. The results of this simulation are shown in Fig. 6.6, which shows that even with moderate record lengths and input frequencies the rms offset errors can be reduced to much below 1ps.

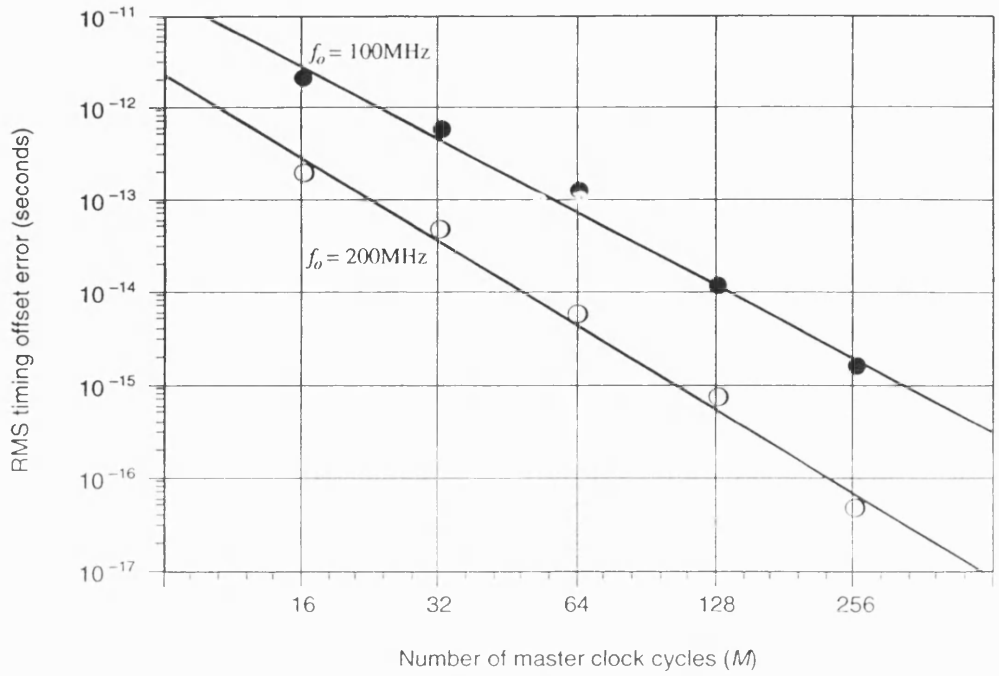


Fig 6.6 Timing offset error remaining after correction with algorithm.

The system was also simulated for a range of offset errors with $f_o = 200\text{MHz}$ and $M = 64$. The results of this are given in Table 6.2, showing that errors as large as a half of one period can be corrected, and that the corrected error is virtually independent of the original error.

TABLE 6.2

RMS VALUES OF RESIDUAL TIMING OFFSET FOR A RANGE OF TIMING ERRORS

Timing offset error	RMS value before adjustment (seconds)	RMS value after adjustment (seconds)
0.05	$1.38\text{x}10^{-11}$	$5.57\text{x}10^{-15}$
0.1	$2.77\text{x}10^{-11}$	$5.73\text{x}10^{-15}$
0.3	$8.74\text{x}10^{-11}$	$5.66\text{x}10^{-15}$
0.5	$1.47\text{x}10^{-10}$	$5.69\text{x}10^{-15}$

These results show that the algorithm can be used successfully to correct for static timing errors in a time interleaved ADC. The accuracy of the correction depends upon the sample size and the input frequency. For 8-bit conversion at

2Gs/s we require a timing accuracy of ~0.3ps, which from Fig. 6.6 we can see can be achieved by recording $64N$ points with an input test signal of 100MHz. The hardware required to compute the FFTs and determine the offset corrections would thus be very straightforward.

In section 3.3.1(iii) a method for adjusting the exact sampling instant of the OS/H circuits was described. We can therefore build a calibration system into the optically triggered ADC which records the output with a known test signal frequency, computes the offset errors, and corrects them by adjusting the necessary bias voltages on the OS/H circuits.

CHAPTER 7

OPTOELECTRONIC INTEGRATION

The demonstration circuits fabricated for this project have all used optical fibres for the distribution of the clock signal. This is an apparently simple solution to the interconnect problem which utilises the mature technology which has been developed for the telecommunications industry. All of the components required for this application are available commercially.

Unfortunately, an optical fibre system has many drawbacks. For example, optical fibres are not compatible with the abrupt directional changes required for high density mappings. Bend radii of a few centimetres are typically the smallest permissible without high loss and long term degradation of mechanical integrity. Connectors and other ancillary components have been developed for applications where lateral dimensions are not restricted, thus new components would have to be developed for use in a compact system. In comparison with integrated circuits, the fibres themselves have unsuitably large dimensions, typically 125μm diameter. A further, very important, consideration is the difficulty involved in accurately aligning large numbers of fibres and detectors. This will naturally decrease reliability and increase manufacturing costs. These considerations of size, cost and reliability clearly advocate that a move to integrated technology, analogous to that which has taken place in electronics, is necessary if optical waveguide techniques are to be employed in practical implementations.

The goal of optoelectronics, then, is the integration of optical and electronic devices on a single chip to obtain the cost and performance benefits over discrete and hybrid circuits similar to those achieved in electronic integrated circuits. In integrating electronic components, devices with similar structures are electronically interconnected with wires. In contrast, the integration of optoelectronic components into optoelectronic integrated circuits requires interconnecting optically and electronically several different types of devices

with dissimilar structures. These differences have hindered the progress in this field.

Unfortunately, traditional optical waveguide materials such as $LiNbO_3$ cannot be grown directly on GaAs substrates due to lattice mismatches. Other waveguide materials which can be grown easily on GaAs absorb very highly at the wavelengths needed to activate the photodetectors. However, a number of techniques have been suggested which exhibit low loss at the required wavelength and are compatible with GaAs substrates, and these are presented here.

7.1 WAVEGUIDES ON GaAs

7.1.1 Lattice Matched Waveguides

The first class of waveguides we discuss are made form crystalline substances which can be grown directly on GaAs substrates with a very small degree of lattice mismatch (the lattice constant is a measure of the size of the unit crystalline cell).

An obvious route is to use the semiconductor material itself as the waveguide. Significant advances have been made in recent years in the development of GaAs low-loss optical waveguides designed for operation at 1.15–1.52μm [159-162]. However, compatibility of optical waveguides with GaAs based transmitters and detectors requires low-loss transmission at 820–870nm. Single crystals of GaAs have an energy gap of 1.42 eV, which means that they are highly absorbent at wavelengths below around 900nm, and cannot therefore be used for waveguiding at shorter wavelengths. However, the energy gap, and hence the optical cut-off frequency, can be shifted towards the visible when alloys of AlGaAs and PGaAs are formed. AlGaAs structures can be epitaxially deposited on GaAs with a very small degree of lattice mismatch, which is important for long term reliability. Epitaxial techniques for growing $Al_xGa_{1-x}As$ are well developed and have received a strong impetus because of their importance in the fields of solid state microwave oscillators and heterojunction lasers. The presence of a fraction x of aluminium causes the index to change by approximately:

$$\Delta n \sim -0.4x \tag{7.1}$$

so that a simple dielectric waveguide can be fabricated by growing epitaxially a $Al_xGa_{1-x}As$ layer on a substrate containing a larger aluminium concentration. AlGaAs waveguide heterostructures of this form have been reported with a propagation loss of less than 0.1dB/cm at 830nm [163]. These guides consist of three layers of AlGaAs deposited on a GaAs substrate using organometallic vapour phase epitaxy (OMVPE), as shown in Fig. 7.1, forming waveguides with dimensions as small as 0.5μm x 2μm.

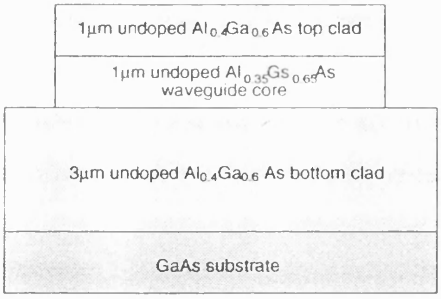


Fig 7.1 AlGaAs waveguide structure

This process can be extended to allow the coupling of electronic devices with the waveguide. To do this one must grow a further layer of GaAs on the top AlGaAs layer, which can then be used as the active layer for optoelectronic components. Monolithic integration of AlGaAs optical waveguides at 830nm with GaAs MSM photodetectors and MESFETs has been demonstrated using this technique [164] as shown in Fig 7.2.

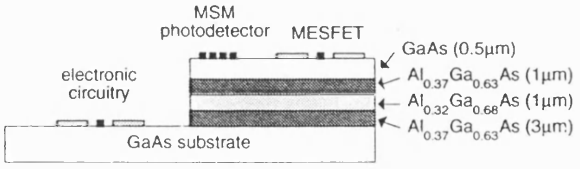


Fig 7.2 Monolithic integration of AlGaAs optical waveguide with GaAs optoelectronic devices

The main problem with this approach is that the processing is far more complex than the basic GaAs fabrication.

7.1.2 Polymer Waveguides

The waveguide structures described so far have required complex epitaxial processing steps which increase cost and complexity, and compromise the functionality of the chip. A guided wave implementation that is perhaps more compatible with our goals is a polymer waveguide technology. The use of polymer optical waveguides instead of semiconductor waveguides has the advantage of separating optoelectronic and electronic functions (detection, amplification, etc) from optical functions (waveguiding, etc). It is thus possible to fabricate the optoelectronic chip without taking into account optical waveguiding requirements, and to deposit optical interconnections afterwards. Using standard microfabrication procedures, singlemode or multimode optical rib waveguides can be fabricated from a range of polymers on almost any substrate [59,62,165-166]. Examples of waveguides of this type include 8μm x 8μm rib waveguides fabricated in etched polyimide, which exhibited propagation losses of 0.3dB/cm at 830nm [166]. Mirror-like bends can be made by utilising total internal reflection at the air-waveguide interface. Bends with angles of 90° or shallower can easily be fabricated, and typical losses are 0.4dB for a 90° bend and 0.15dB for a 45° bend. Similarly, 90° waveguide interconnects can be fabricated with losses of 0.006dB. The dimensions of the waveguides can be further reduced, allowing a pitch of 10μm to be easily fabricated [59].

To couple light into the waveguides one could use a laser with a fibre pigtail. The optical fibres can then be coupled to the polymer waveguides with relative ease. A simple technique is to use butt-coupling, in which cleaved fibre ends are positioned against the end of the waveguide and permanently bonded using a liquid polymer formulation. A technique which offers easier alignment and improved mechanical rigidity employs an excimer laser to ablate grooves into which the fibres can be placed for alignment to the guide [165]. Again, the fibres are bonded with liquefied polymer, providing an index matched bond with a coupling loss of around 0.5dB.

Similar work has involved the fabrication of a dielectric SiO_2/Si_3N_4 waveguide on a GaAs substrate [61], and the coupling of this to an integrated MSM detector. This material has similar properties to the polymer waveguides

and can also be fabricated on any substrate although coupling is more difficult as butt-coupling cannot be used. Instead prism or grating coupling are commonly used.

7.1.3 Coupling of Integrated Waveguides to Photodetectors

Monolithic coupling of waveguides and photodetectors has been achieved in each of the materials systems described. The most common technique for this relies on the evanescent field coupling technique, and is therefore similar in principle to the operation of an electro-optic coupler as discussed in chapter 1. In the case of the SiO_2/Si_3N_4 dielectric waveguide on GaAs an MSM photodetector was used [61]. The MSM consisted of two Schottky electrodes separated by a distance equal to the waveguide width. It was found that an electrode length of 25μm was sufficient to detect all of the 830nm guided light. In the InGaAsP system used for long wavelength applications, 90% absorption at 1.52μm has been achieved with a waveguide length of 42μm [167].

7.2 INTEGRATED OPTIC SPIRAL DELAY LINES

Optical clock distribution is usually viewed as a means of distributing a clock to several areas in a digital system without introducing clock skew. The interleaved ADC, however, requires an accurate, constant, delay between each of the paths. The delay required depends upon the number of paths, and the overall clock speed. If the sample period of each path is T and there are N paths, then the maximum delay required will be $T(1-1/N)$. For example, an 8-path ADC with a sample period of 4ns for each path, will require a maximum delay (between the first and last paths) of 3.5ns. The speed of light in glass is ~ $2x10^8$ms, so a 3.5ns delay would require a waveguide length of 70cm.

It might appear that delay lines of this length would be too long for an integrated circuit format. However, by winding the waveguide into a spiral, these delays can be provided in a relatively compact area. An apparent difficulty with the spiral geometry is that a means must be provided to allow the guide to exit from the centre of the spiral. The simplest solution is to allow the exiting guide to simply cross through the bounding guides with a series of 90° intersections, as shown in Fig. 7.3. We have seen in section 7.1.2 that a 90°

intersect can be fabricated with a loss of only 0.006dB, so several of these crossings can be made, with little detrimental effect. The size of the spiral is determined by the number of turns n, the inner diameter d, and the spacing between the waveguides p . If the product np is much smaller than d then the outer diameter will be dominated by d. If, however, np is much greater than d (as in the case of a spiral with a large number of turns) then minimum bend radius will have little effect on the overall size of the spiral.

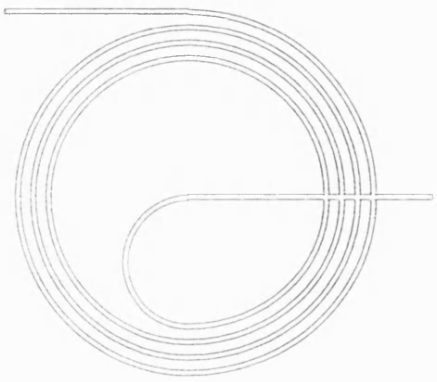


Fig 7.3 Spiral optical waveguide delay. The relative width and spacing of the waveguides in this figure have been enlarged for purposes of clarity.

Several recent publications have reported the successful implementation of spiral optical waveguides using various material combinations, in principle providing delays of the order of tens of nanoseconds. For example, GaAs spiral delay lines have been fabricated which provide a delay of ~ 1.5ns with a four-turn spiral [64]. The spiral diameter was chosen somewhat arbitrarily to be 1cm, the waveguide width was 5μm and the separation between the guides was 100μm. The radius of the small semicircle connecting the exiting waveguide to the innermost turn of the spiral was 0.25cm. It was found that the bend loss of even the smallest radius turn was only 0.01dB/cm, suggesting that the spiral could be made much more compact. Also the pitch radius could be reduced from 100μm to 10μm, reducing the radius even further.

Waveguides with bend radii as small as 75μm have been fabricated in GaAs/AlGaAs [168], but these suffered a relatively high loss of 0.6dB/radian. However, it was shown that this was dominated by scattering loss due to

sidewall roughness. These guides were fabricated using ion-beam milling and a mask defined by electron-beam lithography. The lithography produced quantization steps of 1/16μm, causing the sidewall roughness.

The size of spiral needed for a given delay can be estimated if we assume that the turns of the spiral are concentric circles. If the diameter of the innermost turn is d and the pitch p, then the length of the nth turn l_n is:

$$l_n = \pi(d + 2(n-1)p) \tag{7.2}$$

So, the total length of an n turn spiral is:

$$L = \sum_{n=1}^{n} \pi(d + 2(n-1)p) = \pi n(d + (n-1)p) \tag{7.3}$$

If the number of turns required is very large, then the total path length is approximately given by:

$$L \approx \pi n d + \pi n^2 p \tag{7.4}$$

So the number of turns of a given total length L is

$$n = \frac{\sqrt{\pi d^2 + 4pL}}{2p\sqrt{\pi}} - \frac{d}{2p} \tag{7.5}$$

and the outside diameter D is given by

$$D = d + 2p(n-1) = \frac{\sqrt{\pi d^2 + 4pL}}{\sqrt{\pi}} - 2p \tag{7.6}$$

From this we can see that a spiral with a length of 70cm, a minimum bend radius of 250μm (giving an inner diameter of 1mm), and a pitch of 5μm would require about 134 turns and a diameter of ~ 2.33mm. An area of 1mm x 1mm has been allowed around each photodetector on the OS/H circuits, so incorporation of the spirals would not seriously increase the total chip area beyond that used for the demonstration circuits.

Several of these spiral delays could be combined with waveguide splitters to provide the complete optical clock system for a single laser source. An example of a 4-path ADC is shown in Fig. 7.4, which uses three spiral delays, three power splitters and four OS/H circuits. Such a system would require a chip area of about 16mm^2, well within the maximum recommended area for the F20 process of 25mm^2.

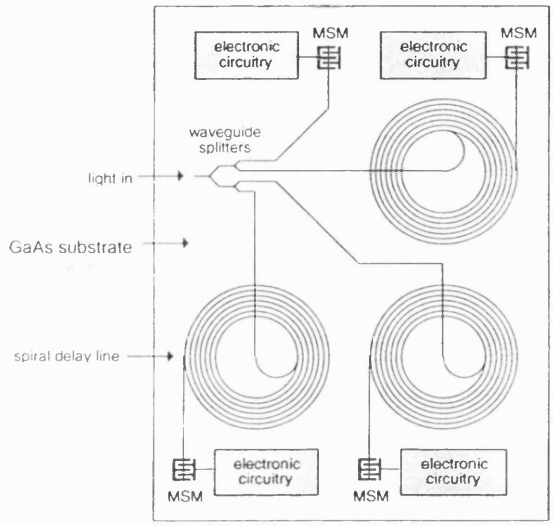


Fig 7.4 Proposed layout of a 4-path monolithic ADC OEIC.

7.3 CONCLUSIONS

This chapter has described a selection of techniques for fabricating integrated waveguides on GaAs for use at 830nm. These waveguides range in complexity from OMVPE epitaxially grown heterostructures to much simpler polymer waveguides. The current performance of these waveguides is high enough to allow them to be used for the guiding, division and timing of the optical clock. Future improvements will allow more compact and higher quality components, leading to higher levels of integration.

CHAPTER 8

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

8.1 SUMMARY AND CONCLUSIONS OF THESIS

Since the development of semiconductor diode lasers and low loss fibres in the 1970s, optical technology has challenged the dominance of electronics in an ever expanding field. This project is an investigation of the use of optical techniques to improve the performance of one very important IC application – the analogue to digital converter. The main objectives of this research were to explore the use of a commercial GaAs IC technology for optoelectronic applications and to investigate the use of optics and optoelectronics in high performance A/D conversion. The broad scope of the project brings together a variety of fields, including device modelling, GaAs analogue circuit design, and optical system design.

Traditionally, the distinction between optics and electronics has been clear. Optics is used for long haul communications, where the enormous bandwidth of optical fibres makes it vastly superior to electronic transmission systems. Electronics is the dominant technology for almost every other application, including signal processing, data storage, coding etc, with optoelectronics aimed primarily at converting between the two mediums. However, with improved optical technology, many traditionally electronic applications will be improved by the use of optics, and future systems designers will have to examine the whole range of electronic and optical techniques if they are to produce optimal solutions. A major aim of the project has been to adopt this hybrid approach and not to be restricted to a single medium.

With improvements in optical technology, some of the all-optical techniques for A/D conversion may become more important. For example, the optical oversampled converter [47] will be improved if the theoretical switching speeds of S-SEEDs can be attained, and if techniques for optical decimation can be developed. Similarly, improvements in IC processes (for example the

introduction of GaAs HEMTs and HBTs) will improve the performance of electronic converters such as flash converters. In spite of this the hybrid approach will continue to offer advantages, as it makes optimal use of all available technologies.

A major aspect of this work has been the practical implementation of the OS/H circuits. This represents, to my knowledge, the first time that the GEC-Marconi F20 MMIC process has been used for optoelectronic applications. Similarly the OS/H, identified as the key component in optically controlled signal processing applications, has only been investigated in discrete form in previous work. The move to integrated technology has improved the performance of this component by an order of magnitude.

In the introduction the design issues of ADCs are discussed and the time interleaved ADC is identified as the most appropriate architecture for the realisation of high speed converters at moderate resolution. The recognition of timing errors as a major deficiency in this architecture leads to the suggestion that optical clock distribution might be used to dramatically improve the performance. A discussion of optical clock distribution techniques then follows and the OS/H is identified as the key component of a time interleaved ADC.

An understanding of the physical properties of GaAs forms an essential background to this work, and this is discussed in chapter 2. Following this discussion we investigate models for MESFETs and MSM photodetectors with the requirement that they can be used in the HSPICE circuit simulator. These models were developed from measured S-parameter data.

Three S/H architectures have been identified as suitable for use in an optically controlled system, and these are discussed in chapter 3. A number of circuit designs are presented which include a simple photoconductive OS/H with a very limited performance, a more complex series MESFET circuit, and a diode bridge OS/H both with potentially a much higher performance. A complete analysis of all the circuit designs is given, which allows accurate predictions of performance and a clear understanding of the circuit operation. Designing circuits in GaAs is hampered by the fact that GaAs IC processes generally do not provide p-type devices. This complicates the design of active loads to such an extent that it can become the most problematic aspect of a circuit design. This problem is also discussed in chapter 3 and some solutions

are presented.

The realisation of a working IC from is far from trivial. IC layout is time consuming and error prone, and can lead to unexpected effects, particularly where high speed analogue circuitry is concerned. For this project a total of six different ICs were designed and manufactured in a single fabrication run. Similarly, testing the fabricated ICs is complicated by the high frequencies involved and the need to deal with optical and electronic signals. An account of the layout of the ICs and PCBs is given in chapter 4, and the steps taken to ensure accurate measurement are highlighted. Photographs of the completed ICs and PCBs are also included in this chapter.

In chapter 5 we discuss the measured results and the steps taken to make these measurements. The nature of these circuits means that the problems normally associated with high speed analogue circuit testing are exasperated by the difficulties of the optical requirements. In spite of these difficulties, many very satisfactory measured results were obtained. The photoconductive OS/H operates at a speed of about 10Ms/s, which is approximately as we would expect from results available in the literature [31]. The speed of this circuit is determined principally by the high *on* resistance of the MSM photoconductor. The series MESFET OS/H is the most successful of the OS/H circuits, with a sample rate in excess of 250Ms/s at over 7-bits resolution. This circuit therefore meets the requirements of the optically triggered ADC and demonstrates the feasibility of this approach. A wide range of test results are presented which completely characterise this circuit, the main features of which are as follows

- *Maximum sample rate:* 300MHz
- *Acquisition time:* 2ns
- *Total harmonic distortion:* 0.5±0.05%
- *Resolution:* 7.6±0.5-bits
- *Gain flatness:* < 0.5dB up to 400MHz

The diode bridge circuit offers a potential improvement in the analogue bandwidth and sample rate over the series MESFET OS/H, but difficulties in the realisation of the circuit prevented satisfactory operation. Alternative circuits are given in section 8.2.1 which should overcome these problems, albeit

at the expense of a slight reduction in performance and increased die area.

It has been asserted many times in the literature that timing jitter and clock skew can have a major detrimental effect upon high speed circuitry. What is less well publicised is a quantitative analysis of this effect. Chapter 6 is an investigation into this problem, which collects together much of the research in this area. This leads to an algorithm for determining static sampling time offsets which can be applied to the N-path optically triggered ADC. Simulations of this system show that sampling time offsets can be reduced to under 0.1ps. This is important as temperature effects and errors in fabricating waveguide delays will mean that static and slowly varying timing offset errors will be unavoidable in an interleaved ADC.

Finally, chapter 7 discusses means by which optical waveguides and delay lines can be integrated on GaAs substrates. A variety of techniques are described and contrasted, and recommendations for the most appropriate are made. Means by which these waveguides can be coupled to integrated photodetectors are then described and the possibility of fabricating integrated spiral delay lines in these technologies is considered.

8.2 SUGGESTIONS FOR FURTHER WORK

8.2.1 Optically Triggered S/H Circuits

Successful operation of the series MESFET OS/H demonstrates both the feasibility of the OS/H approach and the use of a standard GaAs MMIC foundry process for optoelectronic applications. The problems with the diode bridge have been identified as being due to the negative current sources. A simple approach to this problem is to replace the current sources with resistors, although this would mean a very large increase in die size. A more satisfactory solution would be to use bootstrapped active loads such as those described in [169]. Although this would add complexity, it would be worthwhile in applications where the high analogue bandwidth of the diode bridge circuit is required.

The laser clock used for the demonstration circuits was generated by driving a CW laser diode with an electronic pulse generator. To realise the full benefit of the optical clock we would like to use a mode locked laser diode as the light

source. These devices can generate very short duration pulses with high power and extremely low timing jitter. One problem with this approach is that the OS/H circuits have been designed to use a light source with an approximately 50% duty cycle. To solve this problem we could use divide-by-two counters immediately after the photodetectors, thus providing a 50% duty cycle clock from the narrow laser pulse. This technique has been used successfully in an optical clock distribution demonstration [29] but would add considerably to the complexity of the OS/H circuits (particularly as the depletion-only GaAs process used is not well suited to digital logic functions). Also, the added circuit complexity between the photodetector and the sampling element is likely to introduce noise, ultimately reducing timing accuracy.

A second approach is to adapt the circuits to use the narrow laser pulse directly. The response time of an MSM photodiode is approximately 50ps [106], and so one of these devices would produce a large current pulse of this duration in response to a mode locked laser pulse. Now, the acquisition time of the diode bridge circuit is proportional to the photocurrent, so if we can generate sufficient photocurrent to acquire the input signal in ~ 50ps, then we could use a mode locked laser directly. From equation (3.9) we can see that the slew rate of the diode bridge is given approximately by I/C_h, where I is the photocurrent and C_h is the hold capacitor. So if we require a slew rate of 1V in 50ps with a hold capacitor of 0.75pF, then we need to generate ~15mA of photocurrent. As mode locked laser diodes can generate peak powers of tens of watts, this level of current could easily be generated. The maximum power dissipation of an F20 MESFET is 1mW per μm gate width, so when used as a diode the power consumption would be 15mA x 0.8V = 12mW, which is well within the maximum power dissipation of 20mW allowed with a 20μm MESFET. Similarly, this current is within the capacity of the metallic interconnects (20mA for the minimum width of 4μm).

Driving the series MESFET OS/H with a mode-locked laser presents further difficulties as the power of the laser pulse does not affect the acquisition time of the circuit. Therefore we cannot exploit a reduced acquisition time effect such as that occurring in the diode bridge OS/H. A possible solution that has been investigated involves generating a burst of narrow pulses that lasts for the duration of the sample phase. If the separation of the pulses is not too great,

the combination of the finite response time of the MSM photodetector and the integrating action of the series MESFET OS/H will be sufficient to maintain the circuit in the sample phase throughout the pulse burst.

Generation of the bursts of pulses can be achieved by using a system of optical power splitters/couplers and fibre optic delay lines, as shown in Fig. 8.1.

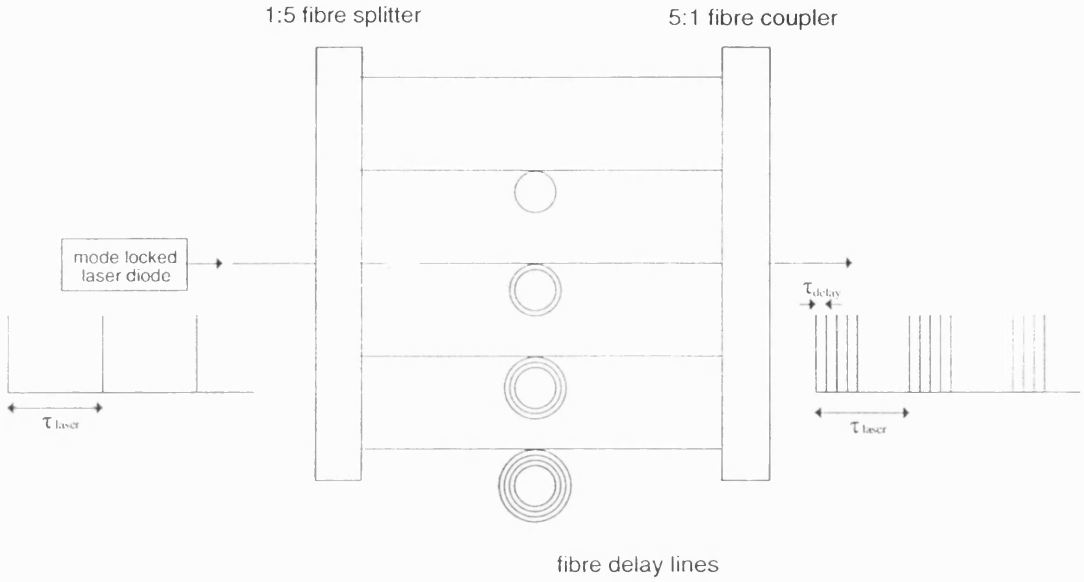


Fig 8.1 Generation of a train of pulse bursts from a mode locked laser source. The laser has a repetition period of τ_{laser} and the fibre optic delay lines produce pulses with a separation of τ_{delay}.

Fibre splitter/couplers such as this are commercially available and typically exhibit an excess loss of around 1.5dB. Therefore this system would cause a total power loss of about 3dB .

Simulations have been made to determine the maximum pulse separation that can be tolerated if the circuit is to track the input signal accurately. Assuming an MSM response time of 50ps FWHM a pulse separation of ~250ps was found to be the maximum allowable. Therefore a 500MHz sample rate can be provided by generating an optical signal consisting of a burst of five pulses separated by 250ps and repeated every 2ns. Figure 8.2 shows a simulation of the series MESFET OS/H that compares the output when driven by such a train of pulses, to the output when driven by a 50% duty cycle, 500MHz square

wave. These results clearly show the equivalence in the hold phase of the two approaches. The advantage of this technique is that the timing accuracy depends only on the timing of the final pulse in the burst, and therefore the fabrication of the delay lines and power splitter will not be critical.

The optical power needed to drive this system can be estimated quite easily. If the responsivity of the MSM is R, then for a photocurrent I_{ph}, we need an optical power of I_{ph}/R Watts. With an MSM pulse duration of τ_{MSM}, then the energy per pulse, E, is

$$E = \frac{I_{ph}\tau_{MSM}}{R} \tag{8.1}$$

If this energy is supplied from a narrow laser pulse with a duration of τ_o, then the peak power of the laser pulse, P, will be

$$P = \frac{I_{ph}\tau_{MSM}}{R\tau_o} \tag{8.2}$$

Therefore, for I_{ph} = 5mA, τ_{MSM} = 50ps, R = 0.3A/W and τ_o = 0.5ps a peak power of 1.7W per pulse is required. In this system we need to derive 5 pulses from a single laser source so assuming the loss of the fibre splitter/coupler combination is 3dB, a pulse with a peak power of at least 17W is required. Mode-locked laser diodes have been demonstrated with peak powers of 70W and durations of ~0.5ps [29], which would allow us to drive four complete interleaved paths using this system.

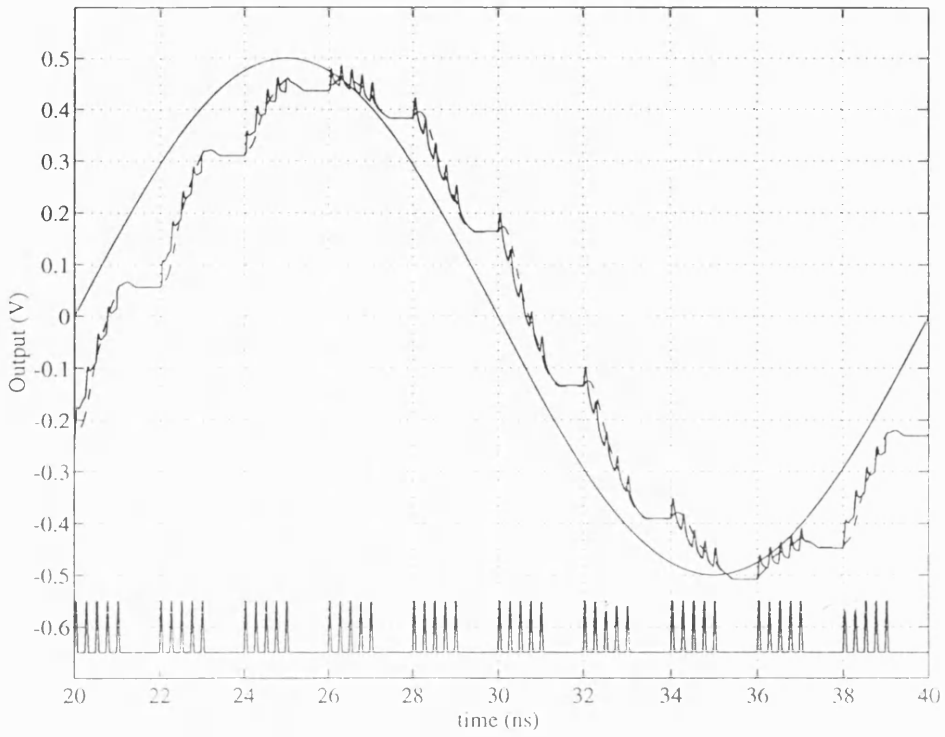


Fig 8.2 Series MESFET OS/H driven by a clock consisting of bursts of narrow current pulses with a separation of 250ps (solid line). The dashed line shows the circuit when driven by a 50% duty cycle clock, and demonstrates that the output during the hold phase is identical for both clock sources.

In section 1.2.2(iii) the sample and filter method of A/D conversion was mentioned briefly. This technique can be used to reduce the post sampling bandwidth requirements of ADC systems by allowing the hold capacitor to discharge through a resistor and then passing the resulting pulse through a low-pass filter [22]. An important aspect of the technique is that it is not necessary to fully charge the hold capacitor and so it may be possible to employ a short duration sample strobe such as that generated by a mode-locked laser. The present OS/H circuits can not be used for this purpose, but modification of the circuit design would be quite straightforward, probably involving only changing the hold capacitor and adding a parallel resistance to ground as a discharge path. Simulations and calculations would be necessary to verify the applicability of this technique.

8.2.2 *N*-path Optically Triggered ADC

The most logical step in extending this project would be the realisation of a multipath ADC using the series MESFET OS/Hs and commercial flash converters. Many of the important properties of this could be observed in a simple 2-path system. For example, the effect of mismatched light intensity on the two photodetectors could be measured and correction for static timing errors could be made. By digitising the output with flash converters, more appropriate measurements of the effective resolution could also be made. Ideally the OS/H circuits and flash converters would be mounted on a thin-film hybrid substrate avoiding the need to package the chips separately. However, for the purpose of a first demonstration, a carefully made PCB could be used, simplifying fabrication.

8.2.3 Optoelectronic integration

In chapter 7 a wide range of techniques for integrating the optical waveguides with the GaAs circuits were discussed. A large amount of practical work could now be done in this area. The first step would be to grow simple waveguides on the GaAs substrates. I would suggest that a polymer type of waveguide would be most suitable, as this involves the least complex processing and is available commercially (DuPont [165]). The next stage would be to couple the waveguide to a photodetector, perhaps using evanescent coupling, and to fabricate the spiral delay lines and splitters.

APPENDIX 1

LASER DRIVE CIRCUIT

Fig. A1.1 shows the laser drive circuit used for testing all of the OS/H ICs. This circuit is built using 4GHz f_T silicon bipolar transistors and can drive a Sharp 40mW 830nm laser diode with a square wave in excess of 250MHz.

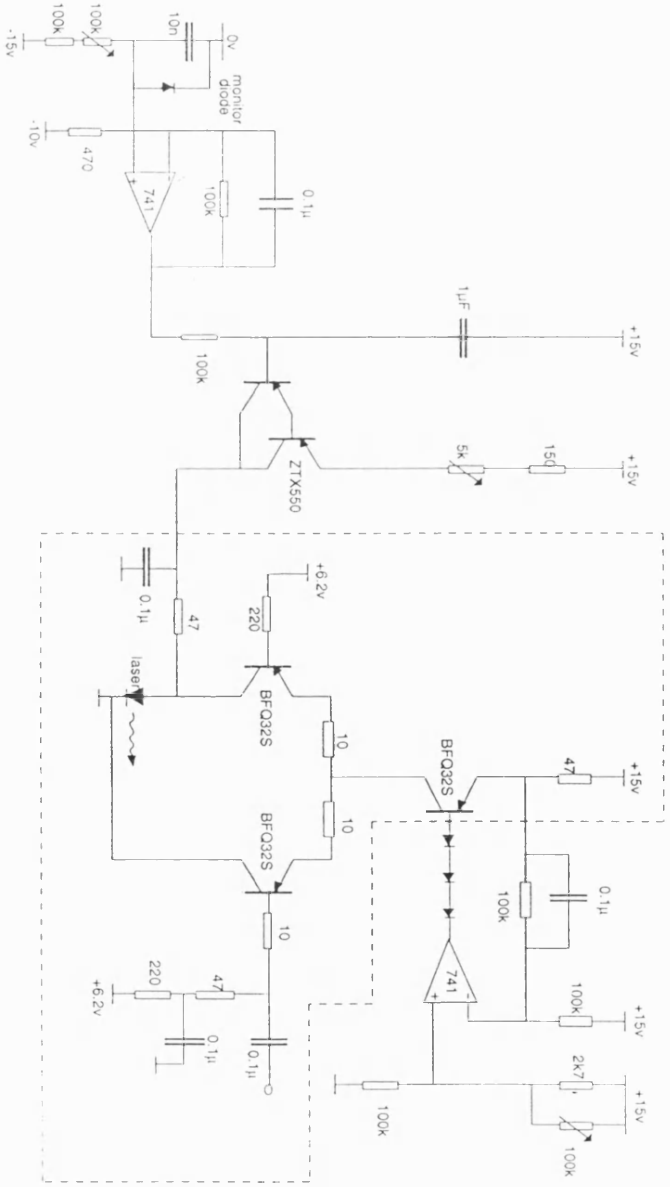


Fig A1.1 250MHz Laser Drive Circuit.

APPENDIX 2

TERMINOLOGY RELATED TO THE PERFORMANCE OF S/H CIRCUITS

The terminology used to described the performance and S/H circuits, and ADCs in general, is often misused or misunderstood. A review of this terminology, with the aim of establishing at set of standard definitions, has been made by the IEEE Network Applications and Standards Committee [148]. A brief outline of the relevant sections of this is presented here, and illustrated in Fig. 3.4.

A2.1 Sample Period

The sample period is the time interval between successive S/H mode transitions. The sample rate is the maximum rate at which such transitions can occur.

A2.2 Acquisition Time

The acquisition time is the time during which the S/H must remain in the sample mode to ensure that the subsequent hold mode output will be within a specified error band; ie. the worst case of the time it takes the S/H to 'catch up' with the input after the onset of the sample mode.

A2.3 Settling Time

The settling time is the time interval between the S/H transition and the time when the output transients and subsequent ringing have settled to within a specified error band.

A2.4 Aperture Time and Aperture Uncertainty

The aperture time is the elapsed time between initiation and completion of the S/H mode transition. The aperture uncertainty is the variance of the aperture time (ie.. the uncertainty in the duration of the time interval).

A2.5 Effective Sampling Instant and Aperture Jitter

The response of the S/H circuit during the aperture time may be different to that during the sample mode. The effective instant at which the sample is taken will therefore depend on this response, as well as the variation of the aperture time. The aperture jitter is the variation in the effective sampling instant due to these effects.

APPENDIX 3

GEC-MARCONI F20 FOUNDRY PROCESS

A3.1 Process Description

The process starts with a cut and polished semi-insulating *100* GaAs substrate. The first step is to coat the substrates on both sides with silicon nitride, deposited by plasma enhanced chemical vapour deposition. The purpose of this is to prevent dissociation of the arsenic from the substrate during the high temperature annealing stage.

Next the complete surface of the wafer is implanted with Si + 29 to form the *n*– type active layer for the FET channels and mesa resistors. Following this an *n*+ layer is formed by further implantation with Si + 29, which reduces contact and parasitic resistances. This region is formed by selective implantation, using photoresist to mask the areas where the *n*+ layer is not required, and is used as the semiconductor region for ohmic contacts. The photoresist mask is then removed and the implants activated by high temperature annealing. Following the anneal stage the silicon nitride coating is removed either by plasma etching or wet etching. In order to isolate the MESFETs, diodes and mesa resistors, the *n* implantation layer is removed in the required places. This is achieved by masking the required device areas with photoresist (layer 1) and etching the exposed GaAs in ammonia peroxide.

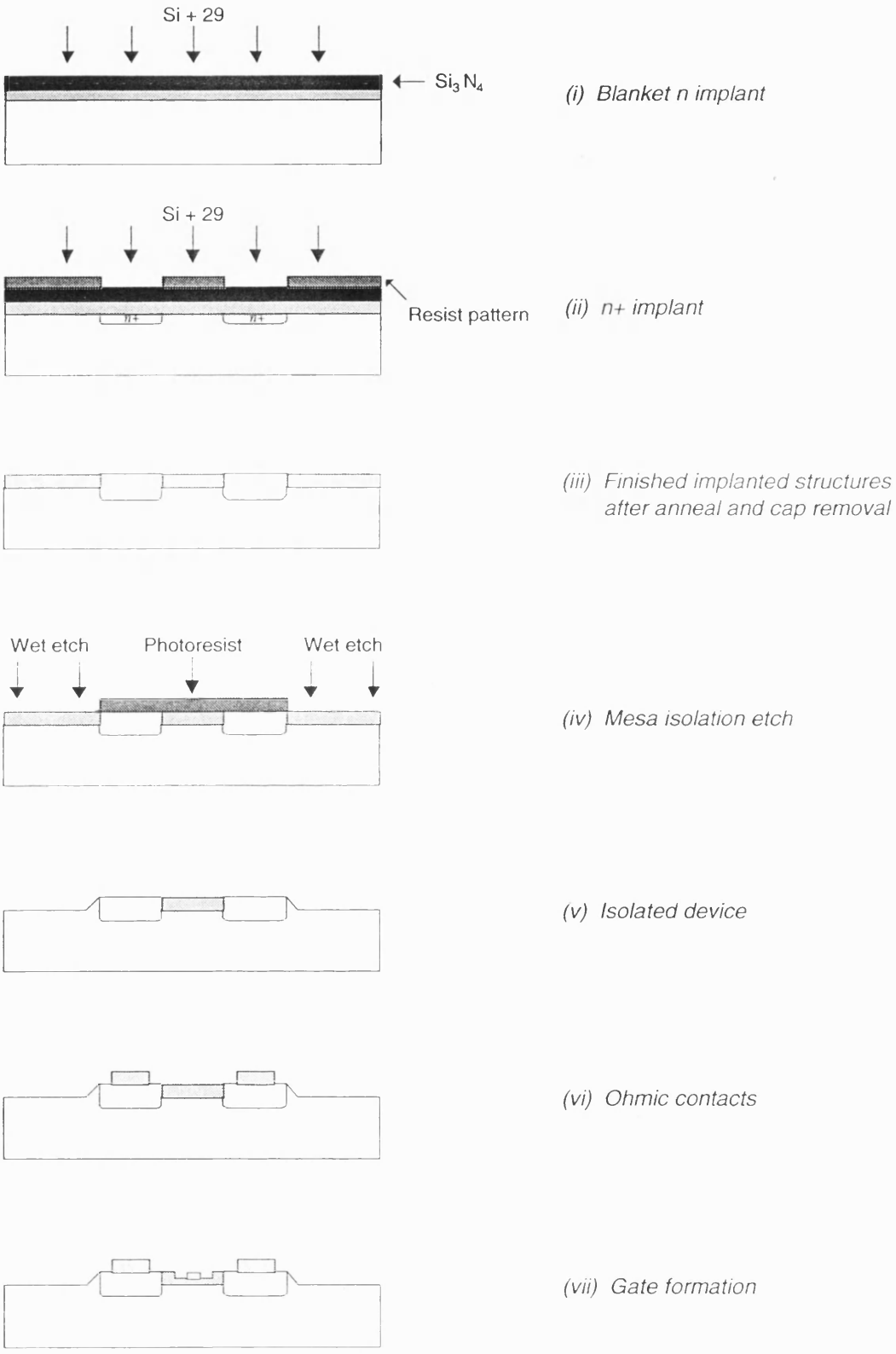


Fig A3.1 Fabrication of a MESFET using the GEC-Marconi F20 foundry process.

The next stage of the process (layer 2) involves forming the ohmic contacts for the MESFET source and drain contacts, and for the mesa resistors. The wafer is coated with photoresist and patterned to expose the surface in areas where ohmic contacts are required. The metallisation is then evaporated onto the wafer, covering both the exposed GaAs and the photoresist. The unwanted metal and photoresist are then floated-off using a suitable solvent. The ohmic contacts must then be alloyed either in a furnace or by flash annealing. This metallisation layer (*M1*) cannot be used for current carrying applications. To allow more precise resistance values, an optional etch (layer 3) can be used to trim the mesa resistors.

The most critical stage of the process is the gate formation, layer 4. The first step is to coat the wafer with photoresist and then expose and develop the required gate pattern to leave exposed GaAs where the metallisation is required. The gate metal is then deposited by evaporation and floated-off in the unwanted areas. This metal layer (*M2*) is also used as the first level of interconnect, the bottom plate of metal-insulator-metal (MIM) capacitors, interdigital capacitors and bond pad base metallisation, resulting in these components being manufactured with the same sub-micron accuracy as the gate process.

Following the gate formation, the wafer surface is passivated by depositing a layer of silicon nitride (layer 5). Windows are etched through this layer where interconnects to the top layer metallisation are required. This layer also acts as the dielectric layer of MIM capacitors. The surface is now insulated to allow metal crossovers by applying a polyimide layer (layer 6), and windows are etched into this to allow interconnection with the top layer metal. The polyimide layer also acts as the dielectric for polyimide capacitors, which have a lower capacitance per unit area than silicon nitride capacitors.

The top layer metallisation (*M3* – layer 7) of titanium-platinum-gold is r.f. sputtered onto the wafer surface. This technique is used for its excellent step coverage characteristics which are needed to provide reliable, low resistance interconnections to the lower metallisation levels. This layer forms the second layer interconnect, the upper electrode of MIM capacitors, spiral inductors, transmission lines and bonding pads. The loss of this metal is lower than that of the first level metal *M2*.

Finally the whole wafer surface is passivated by a further layer of silicon nitride (layer 8). Windows are etched through this to expose the bonding pads. The complete process is shown in Fig A3.1, using the fabrication of a MESFET as an example, and a summary showing the most important layers of the process is given in table A3.1.

TABLE A3.1

LAYER DESCRIPTION OF THE F20 PROCESS

Layer 1 (Mesa)	Electrical isolation of active areas (FETs and resistors).
Layer 2 (M1)	Alloyed ohmic contact metallisation.
Layer 3 (Mesa Trim)	Etching of mesa resistors to achieve the designed component value.
Layer 4 (M2)	Schottky contact metallisation to form FET gates, low level electrodes of MIM capacitors, first level interconnections, interdigital capacitors, bond pad base metallisation.
Layer 5 (Nitride 1)	Passivation of active areas of FETs, dielectric in MIM capacitors.
Layer 6 (Polyimide)	Interlayer dielectric in metal crossovers, dielectric MIM capacitors.
Layer 7 (M3)	Second level interconnect, multi-turn spiral inductors, top electrode in MIM capacitors, transmission lines, bond pads.
Layer 8 (Nitride2)	Encapsulation of entire circuit with bonding areas left open.

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