Thin Film Transistor Circuits

for Active Matrix Liquid Crystal Displays

by

Martin John Edwards

Department of Electronic and Electrical Engineering

University College London

A thesis submitted for the degree of

Doctor of Philosophy of the University of London

March 1998
Abstract

The demand for a high quality flat panel video display device for use in consumer and professional products has led to the rapid development of Active Matrix Liquid Crystal Displays (AMLCD). The majority of these displays use Thin Film Transistors (TFTs) as the active devices and improvements in the performance of these transistors is creating the opportunity to integrate increasingly sophisticated circuits onto the glass substrates of the displays. This thesis describes a number of aspects of the use of thin film transistor circuits for active matrix liquid crystal displays.

The electrical characteristics of TFTs differ in a number of respects from those of conventional MOS devices. This is illustrated with measurements of transistors and simple circuits fabricated using two different low temperature poly-Si TFT technologies.

At present the key application for TFT circuits is integration of the row and column drive circuits for active matrix liquid crystal displays. The issues which arise in the design of TFT drive circuits are discussed and the design and operation of a prototype display with integrated drive circuits is described.

The availability of high mobility TFTs makes it possible to integrate signal processing functions within the pixels of a display. A novel technique employing digital to analogue conversion of the video data within the pixels of a display is presented. This technique allows the display to be addressed with digital column drive waveforms simplifying the column drive circuit. Operation of the pixel data converters has been demonstrated by the design and measurement of small arrays of test pixels.
### Contents

Abstract 2

Contents 3

List of Figures 7

List of Tables 13

Acknowledgements 14

1 Introduction 15

1.1 The Video Display Market 15

1.2 Large Area Electronics 16

1.3 Outline of Thesis 17

1.4 Statement of Originality 18

1.5 Publications and Patents 18

2 Active Matrix Liquid Crystal Displays and Thin Film Transistors 19

2.1 Introduction 19

2.2 The Twisted Nematic LC Cell 19

2.3 Active Matrix Addressing 22

2.4 Drive Circuits for Active Matrix LC Displays 25

2.5 Integrated Drive Circuits 27

2.6 TFT Technologies 28

2.7 Summary 30

3 Electrical Characteristics of Low Temperature Poly-Si TFTs 32

3.1 Introduction 32

3.2 Review of Poly-Si TFT Performance 32

3.3 PRL Low Temperature Poly-Si Technologies 35

3.4 DC Characteristics 36

3.5 Transient Behaviour 41

3.6 Small Signal Characteristics 45

3.7 TFT Stability 50

3.8 Summary 52
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Introduction</td>
<td>54</td>
</tr>
<tr>
<td>4.2</td>
<td>Review of Poly-Si TFT Circuit Performance</td>
<td>54</td>
</tr>
<tr>
<td>4.3</td>
<td>Measurement of Simple Digital TFT Circuits</td>
<td>54</td>
</tr>
<tr>
<td>4.3.1</td>
<td>NMOS and CMOS Inverters</td>
<td>55</td>
</tr>
<tr>
<td>4.3.2</td>
<td>NMOS and CMOS Shift Registers</td>
<td>62</td>
</tr>
<tr>
<td>4.4</td>
<td>Measurement of Simple Analogue TFT Circuits</td>
<td>68</td>
</tr>
<tr>
<td>4.4.1</td>
<td>Two Stage CMOS Differential Amplifier</td>
<td>69</td>
</tr>
<tr>
<td>4.4.2</td>
<td>Single Stage CMOS Differential Amplifier</td>
<td>71</td>
</tr>
<tr>
<td>4.5</td>
<td>Summary</td>
<td>73</td>
</tr>
<tr>
<td>5</td>
<td>TFT Drive Circuits for AMLCDs</td>
<td>75</td>
</tr>
<tr>
<td>5.1</td>
<td>Introduction</td>
<td>75</td>
</tr>
<tr>
<td>5.2</td>
<td>Drive Requirements of TFT Active Matrix LC Displays</td>
<td>76</td>
</tr>
<tr>
<td>5.3</td>
<td>Design of Poly-Si TFT Row Drive Circuits</td>
<td>85</td>
</tr>
<tr>
<td>5.4</td>
<td>Design of Poly-Si TFT Column Drive Circuits Based on Analogue Multiplexers</td>
<td>90</td>
</tr>
<tr>
<td>5.4.1</td>
<td>Principles of Multiplexer Operation</td>
<td>90</td>
</tr>
<tr>
<td>5.4.2</td>
<td>Factors Determining Multiplexer Operating Speed</td>
<td>94</td>
</tr>
<tr>
<td>5.4.3</td>
<td>Column Electrode Time Constant</td>
<td>95</td>
</tr>
<tr>
<td>5.4.4</td>
<td>Multiplexer Switch Design</td>
<td>100</td>
</tr>
<tr>
<td>5.4.5</td>
<td>Multiplexer Video Bus Design</td>
<td>111</td>
</tr>
<tr>
<td>5.4.6</td>
<td>Multiplexer Control Circuit Design</td>
<td>115</td>
</tr>
<tr>
<td>5.4.7</td>
<td>Summary of Column Drive Circuit Design</td>
<td>122</td>
</tr>
<tr>
<td>5.5</td>
<td>Prototype Datagraphic AMLCD</td>
<td>123</td>
</tr>
<tr>
<td>5.5.1</td>
<td>Row Drive Circuit</td>
<td>123</td>
</tr>
<tr>
<td>5.5.2</td>
<td>Column Drive Circuit</td>
<td>127</td>
</tr>
<tr>
<td>5.5.3</td>
<td>Test Multiplexers</td>
<td>132</td>
</tr>
<tr>
<td>5.5.4</td>
<td>Display Operation</td>
<td>135</td>
</tr>
<tr>
<td>5.6</td>
<td>Summary</td>
<td>142</td>
</tr>
</tbody>
</table>
6 Pixel Level Digital to Analogue Conversion

6.1 Introduction

6.2 Pixel D/A Conversion Techniques
   6.2.1 Converter Using Binary Weighted Capacitors
   6.2.2 Serial Charge Redistribution Converter
   6.2.3 Sampled Ramp Converter
   6.2.4 Time Weighted Digital Signal
   6.2.5 Subdivided Pixel
   6.2.6 Resistor Ladder Network
   6.2.7 Review of Conversion Techniques

6.3 Matrix Addressing of NMOS Serial D/A Converter Pixels

6.4 CMOS Serial D/A Converter Pixels

6.5 Pixel Charging Time
   6.5.1 Multiplexed Column Data
   6.5.2 Multi-Level Column Data

6.6 Pixel Capacitor Accuracy

6.7 Input Data Weighting

6.8 Converter Circuit Using Discrete Capacitors and TFTs

6.9 Layout of Converter Pixels

6.10 Measurement of Pixel Circuit Performance
   6.10.1 Measurement of First Generation Pixels
   6.10.2 Measurement of Second Generation Pixels
   6.10.3 The Effect of Parasitic Capacitance Between Half Pixels

6.11 External Drive Circuit Requirements

6.12 Summary
7 Circuit Yield and Fault Tolerance

7.1 Introduction

7.2 A Perspective on the Issue of Yield

7.3 Repair with Redundant Circuit Elements

7.4 Fault Tolerant Circuits

7.5 Self Testing Circuits

7.6 Simple Yield Analysis for Self Testing Shift Register

7.7 Summary

8 The Future for Display System Integration

9 Conclusions

Appendices

A Estimation of TFT Charging Times

B AMLCD Design Equations

C CMOS Switch Resistance

References
### List of Figures

<table>
<thead>
<tr>
<th>Figure 2-1</th>
<th>Twisted Nematic LC Cell</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 2-2</td>
<td>Operation of TN-LC Cell</td>
<td>20</td>
</tr>
<tr>
<td>Figure 2-3</td>
<td>TN-LC Electro-optical</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td>characteristics</td>
<td></td>
</tr>
<tr>
<td>Figure 2-4</td>
<td>Electrical equivalent circuit</td>
<td>22</td>
</tr>
<tr>
<td></td>
<td>of passive matrix LCD</td>
<td></td>
</tr>
<tr>
<td>Figure 2-5</td>
<td>Electrical equivalent circuit</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>of active matrix LCD</td>
<td></td>
</tr>
<tr>
<td>Figure 2-6</td>
<td>Cross section of active</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td>matrix LCD</td>
<td></td>
</tr>
<tr>
<td>Figure 2-7</td>
<td>Equivalent circuit for a</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>single pixel in a TFT AMLCD</td>
<td></td>
</tr>
<tr>
<td>Figure 2-8</td>
<td>Simple column drive circuit</td>
<td>26</td>
</tr>
<tr>
<td>Figure 2-9</td>
<td>Simple row drive circuit</td>
<td>26</td>
</tr>
<tr>
<td>Figure 2-10</td>
<td>TFT technologies</td>
<td>28</td>
</tr>
<tr>
<td>Figure 3-1</td>
<td>Cross section of SPC poly-Si</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>TFT</td>
<td></td>
</tr>
<tr>
<td>Figure 3-2</td>
<td>Cross section of laser</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>crystallised poly-Si TFT</td>
<td></td>
</tr>
<tr>
<td>Figure 3-3</td>
<td>Cross section of laser</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>crystallised poly-Si TFT with</td>
<td></td>
</tr>
<tr>
<td></td>
<td>gate overlapped LDD</td>
<td></td>
</tr>
<tr>
<td>Figure 3-4</td>
<td>SPC TFT transfer characteristics</td>
<td>37</td>
</tr>
<tr>
<td>Figure 3-5</td>
<td>SPC TFT transfer characteristics with threshold control implants</td>
<td>37</td>
</tr>
<tr>
<td>Figure 3-6</td>
<td>SPC p-type TFT in linear region with threshold control</td>
<td>38</td>
</tr>
<tr>
<td>Figure 3-7</td>
<td>SPC n-type TFT in linear region with threshold control</td>
<td>38</td>
</tr>
<tr>
<td>Figure 3-8</td>
<td>SPC TFT, field effect mobility calculated from transconductance</td>
<td>38</td>
</tr>
<tr>
<td>Figure 3-9</td>
<td>Laser crystallised poly-Si TFT characteristics</td>
<td>39</td>
</tr>
<tr>
<td>Figure 3-10</td>
<td>Laser crystallised poly-Si TFT characteristic without LDD</td>
<td>39</td>
</tr>
<tr>
<td>Figure 3-11</td>
<td>Laser crystallised poly-Si TFT p-channel</td>
<td>39</td>
</tr>
<tr>
<td>Figure 3-12</td>
<td>Laser crystallised poly-Si TFT n-channel with LDD</td>
<td>39</td>
</tr>
<tr>
<td>Figure 3-13</td>
<td>Laser TFT, field effect mobility calculated from transconductance</td>
<td>40</td>
</tr>
<tr>
<td>Figure 3-14</td>
<td>Transient behaviour of SPC TFTs</td>
<td>41</td>
</tr>
<tr>
<td>Figure 3-15</td>
<td>Pulsed measurement of SPC poly-Si p-type device</td>
<td>42</td>
</tr>
<tr>
<td>Figure 3-16</td>
<td>Pulsed measurement of SPC poly-Si n-type device</td>
<td>42</td>
</tr>
<tr>
<td>Figure 3-17</td>
<td>Change in transient current in p-type SPC TFT with switching frequency</td>
<td>43</td>
</tr>
<tr>
<td>Figure 3-18</td>
<td>Pulsed measurement of laser poly-Si p-type device</td>
<td>44</td>
</tr>
<tr>
<td>Figure 3-19</td>
<td>Pulsed measurement of laser poly-Si n-type device</td>
<td>44</td>
</tr>
<tr>
<td>Figure 3-20</td>
<td>Output characteristics of n-type TFTs L=6um</td>
<td>45</td>
</tr>
<tr>
<td>Figure 3-21</td>
<td>Output characteristics of p-type TFT L=6um</td>
<td>45</td>
</tr>
<tr>
<td>Figure 3-22</td>
<td>Output Characteristics of n-type TFTs L=15um</td>
<td>46</td>
</tr>
<tr>
<td>Figure 3-23</td>
<td>Output Characteristics p-type TFT L=15um Vgs=-5 to -12V</td>
<td>46</td>
</tr>
<tr>
<td>Figure 3-24</td>
<td>Variation of λ with gate length for laser crystallised poly-Si TFTs</td>
<td>46</td>
</tr>
<tr>
<td>Figure 3-25</td>
<td>Ratio of output conductance to drain current for n-channel TFT</td>
<td>47</td>
</tr>
</tbody>
</table>
Figure 3-26 Ratio of output conductance to drain current for p-channel TFT
Figure 3-27 Variation of transconductance with Vgs n-channel
Figure 3-28 Variation of transconductance with Vgs p-channel
Figure 3-29 Gain of n-channel LDD TFT as a function of bias voltages L=15μm
Figure 3-30 Gain of p-channel TFT as a function of bias voltages L=15μm
Figure 3-31 Circuit for measuring inverter drive capability
Figure 3-32 Output current of laser crystallised poly-Si inverter without LDD
Figure 3-33 Change in output drive current of n-type TFTs in CMOS inverters
Figure 4-1 SPC poly-Si inverter circuits
Figure 4-2 NMOS inverter DC characteristics
Figure 4-3 NMOS inverter DC characteristics, TFTs with threshold shifting implants
Figure 4-4 CMOS inverter DC characteristics
Figure 4-5 CMOS inverter DC characteristics, TFTs with threshold shifting implants
Figure 4-6 High logic level for CMOS inverters
Figure 4-7 Laser crystallised poly-Si CMOS inverter characteristics
Figure 4-8 Laser crystallised poly-Si CMOS inverter noise margins
Figure 4-9 Laser crystallised poly-Si CMOS inverter threshold voltage
Figure 4-10 Static ratioed NMOS shift register
Figure 4-11 Ratioed NMOS shift register waveforms
Figure 4-12 Ratioless NMOS shift register
Figure 4-13 Ratioless NMOS shift register waveforms
Figure 4-14 Dynamic CMOS shift register
Figure 4-15 CMOS shift register waveforms
Figure 4-16 Maximum shift register operating frequency
Figure 4-17 Power consumption of shift register circuits
Figure 4-18 CMOS static shift register
Figure 4-19 Laser crystallised poly-Si CMOS shift register
Figure 4-20 CMOS shift register power-delay performance
Figure 4-21 Two stage CMOS differential amplifier
Figure 4-22 Frequency response of CMOS differential amplifier L=15μm
Figure 4-23 Gain of two stage CMOS differential amplifiers
Figure 4-24 Single stage CMOS amplifier
Figure 4-25 Open loop frequency response with 20pF load
Figure 4-26 Closed loop transient response with gain of +1
Figure 5-1 Pixels storage capacitors in AMLCDs
Figure 5-2 TN-LC Electro-optical characteristics
Figure 5-3 Typical pixel drive voltage waveforms for a TFT AMLCD
Figure 5-4 Reduced column drive voltage schemes for TFT AMLCD pixels
Figure 5-5  TFT AMLCD drive polarity inversion schemes 81
Figure 5-6  Schematic representation of colour filter layout 83
Figure 5-7  Row drive circuit using a shift register 85
Figure 5-8  Row drive circuit using a decoder 86
Figure 5-9  Row capacitance of displays with different resolutions and diagonals 88
Figure 5-10  Row capacitance with and without separate capacitor electrode 89
Figure 5-11  TFT column drive circuit based on multiplexing 91
Figure 5-12  Timing of column drive circuit 92
Figure 5-13  External circuits required to generate parallel video signals 92
Figure 5-14  External circuits required for use with interlaced video signal source 93
Figure 5-15  Equivalent circuit for multiplexer operation 94
Figure 5-16  Multiplexer design considerations 96
Figure 5-17  Simulation of variation of column voltage with position during charging 97
Figure 5-18  Variation of column voltage error with normalised charging time 98
Figure 5-19  Minimum number of video lines based on column electrode time constant 99
Figure 5-20  NMOS multiplexing switch 100
Figure 5-21  Equivalent circuit of TFT 102
Figure 5-22  Measured and calculated offset voltage of NMOS multiplexing switch 104
Figure 5-23  Operating regions of a CMOS transmission gate 105
Figure 5-24  CMOS transmission gate offset voltage 108
Figure 5-25  Variation of column capacitance with display diagonal 110
Figure 5-26  Minimum number of video lines required based on multiplexer TFT size 110
Figure 5-27  Grouping of multiplexer switches 112
Figure 5-28  Minimum number of video bus lines 5-inch colour VGA 114
Figure 5-29  Effect of bus width on minimum number of video lines 114
Figure 5-30  Combinations of shift registers and video lines 115
Figure 5-31  Shift registers for single scan direction 116
Figure 5-32  Shift registers for bi-directional scanning 116
Figure 5-33  Shift register with reduced clock line loading 117
Figure 5-34  Shift register with locally generated complementary clocks 118
Figure 5-35  Multiplexer switch timing 119
Figure 5-36  The effect of overlapping multiplexer control signals 120
Figure 5-37  Divided video bus 120
Figure 5-38  Use of NOR gates to prevent overlapping pulses 121
Figure 5-39  Generation of CMOS transmission gate control signals 121
Figure 5-40  Schematic diagram of row drive circuit 124
Figure 5-41  One section of row drive circuit 125
Figure 5-42  Layout of row drive circuit 126
Figure 5-43  Schematic diagram of column drive circuit
Figure 5-44  Column drive circuit video data transfer timing
Figure 5-45  Schematic diagram of column drive circuit shift register
Figure 5-46  Layout of shift registers of column drive circuit
Figure 5-47  Layout of column multiplexer transmission gates
Figure 5-48  Location of test multiplexers
Figure 5-49  One section of test multiplexer circuit
Figure 5-50  Row and column resistance measurements
Figure 5-51  Processed substrate with active matrix and drive circuits
Figure 5-52  Image on the 640x160 pixel display
Figure 5-53  Image on the 640x160 pixel display
Figure 5-54  Row drive waveform
Figure 5-55  Column driver waveforms
Figure 5-56  Column waveforms measured in field inversion
Figure 5-57  Column driver transmission gate resistance
Figure 5-58  Column driver transmission gate offset voltage (12pF load)
Figure 5-59  Leakage current of column driver transmission gate
Figure 6-1   Pixel performing a conversion using weighted capacitors
Figure 6-2   Pixel using serial charge redistribution conversion
Figure 6-3   Pixel using sampled ramp conversion
Figure 6-4   Conversion using time averaging of a digital signal
Figure 6-5   Pixel with electrode divided into four binary weighted areas
Figure 6-6   Pixel converter using resistor network
Figure 6-7   Components of a conventional AMLCD pixel
Figure 6-8   Circuit for serial charge redistribution digital to analogue converter
Figure 6-9   Equivalent circuit for D/A converter pixel
Figure 6-10  Matrix of NMOS D/A converter pixels
Figure 6-11  Row addressing waveforms for 8-bit pixel conversion
Figure 6-12  CMOS D/A pixel array
Figure 6-13  Addressing waveforms for CMOS pixel circuit
Figure 6-14  TN LC pixel drive voltage requirements
Figure 6-15  Normalised pixel charging time for n-type TFT
Figure 6-16  Normalised pixel charge redistribution time for n-type TFT
Figure 6-17  Multiplexing of column data for two pixel conversions
Figure 6-18  Selection of multilevel column data for simultaneous bit conversion
Figure 6-19  Circuits for simultaneous bit conversion and divided range conversion
Figure 6-20  Effect of parameter K1 on DNL
Figure 6-21  Converter circuit waveforms with data equal to 255
Figure 6-22  8-bit conversion with \( W = 1 \)

Figure 6-23  Effect of \( W \) value on differential non-linearity

Figure 6-24  8-bit conversion with \( W = 1.062 \)

Figure 6-25  2x4-bit conversion with \( W = 1.062 \)

Figure 6-26  SPC poly-Si digital to analogue converter pixels

Figure 6-27  Layout of a converter pixel using NMOS TFTs

Figure 6-28  CMOS converter pixel layout

Figure 6-29  Light masking between pixel electrodes

Figure 6-30  Dark state of CMOS pixels with and without light masking

Figure 6-31  Common centroid CMOS pixel

Figure 6-32  Common centroid CMOS pixel with light masking

Figure 6-33  Pixel measurement system

Figure 6-34  SPC pixel design 8-bit pixel conversion

Figure 6-35  Effect of pixel charging time on pixel transmission

Figure 6-36  8-bit pixel conversion with an input data weighting factor of 0.9678

Figure 6-37  NMOS pixel, 6-bit conversion, 4\( \mu \)s charging time

Figure 6-38  CMOS pixel, 6-bit conversion, 4\( \mu \)s charging time

Figure 6-39  CMOS pixel with common centroid layout of ITO electrodes

Figure 6-40  Effect of pixel charging time on transmission for NMOS and CMOS pixels

Figure 6-41  NMOS D/A pixel with input data weighting, \( W = 1.023 \)

Figure 6-42  CMOS D/A pixel with input data weighting, \( W = 1.021 \)

Figure 6-43  CMOS D/A pixel with common centroid layout of ITO

Figure 6-44  Pixel equivalent circuit including capacitance between two half pixels

Figure 6-45  Variation of differential non-linearity with pixel coupling capacitance

Figure 6-46  Cross section and plan views of pixel used for capacitance calculation

Figure 6-47  Variation of pixel coupling with electrode separation

Figure 6-48  Difference in \( C_1 \) and \( C_2 \) values required to compensate for \( C_c \)

Figure 6-49  Row driver for use with pixel conversion

Figure 6-50  Row driver waveforms

Figure 6-51  Column drive circuit for serial pixel conversion

Figure 6-52  Simple column drive circuit for serial pixel conversion

Figure 7-1  Redundancy using double ended addressing

Figure 7-2  Redundancy using laser repair

Figure 7-3  Circuit with limited fault tolerance

Figure 7-4  More complex fault tolerant circuit

Figure 7-5  General self testing circuit

Figure 7-6  Self testing shift register circuit

Figure 7-7  Shift register testing circuit

11
Figure 7-8 Display after test operation 213
Figure 7-9 Display before test operation 213
Figure 7-10 One block in a self testing row drive circuit 213
Figure 7-11 Effect of number of shift register sections in a block on circuit yield 216
Figure 7-12 Effect of number of TFTs in the testing circuit on yield 217
Figure 8-1 Analogue AMLCD drive system 218
Figure 8-2 Digital AMLCD system for hand held computing 219
Figure A-1 Pixel charging circuit 225
Figure A-2 Pixel charge redistribution 227
Figure A-3 Discharge of a load capacitor 228
Figure B-1 Simple pixel layout 230
Figure B-2 Calculated column capacitances including edge effect 233
Figure B-3 Variation of column, row and TFT width with VGA display diagonal 236
Figure B-4 Variation of row and column resistance with VGA display diagonal 236
Figure B-5 Variation of column and row capacitance with VGA display diagonal 237
Figure C-1 Operating regions of a CMOS transmission gate 238
List of Tables

Table 3-1  Reported performance of high temperature poly-Si TFTs 32
Table 3-2  Reported performance of SPC poly-Si TFTs 33
Table 3-3  Reported performance of laser crystallised poly-Si TFTs 33
Table 4-1  SPC poly-Si ratioed NMOS inverter logic levels and noise margins 57
Table 4-2  SPC poly-Si CMOS inverter logic levels and noise margins 59
Table 4-3  Laser crystallised poly-Si CMOS inverter logic levels and noise margins 60
Table 4-4  Power delay product figures for SPC poly-Si shift register 66
Table 4-5  Gain and offset voltage variation 72
Table 5-1  Maximum display size based on width of row driver output transistors 89
Table 5-2  Summary of considerations for minimum number of video lines per colour 122
Table 5-3  Prototype VGA direct view display 123
Table 6-1  Estimated area required for components used within pixels 153
Table 6-2  Estimated apertures for D/A converter pixels 153
Table 6-3  Summary of conversion methods 154
Table 6-4  Estimated relative charging times for conventional and converter pixels 165
Table 6-5  Combinations of column levels and charging cycles for an 8-bit conversion 168
Table 6-6  Values of multilevel digital data for an N-bit simultaneous bit conversion 168
Table 6-7  Values of capacitor tolerance giving a differential non-linearity of ±1/2 LSB 174
Table 6-8  Addressing voltages for SPC poly-Si pixel array 186
Table 6-9  Addressing voltages for laser crystallised poly-Si pixels 191
Table 6-10 DNL values and required weighting for different pixel layouts 193
Table B-1 Parameters used in calculating display resistances and capacitances 235
I would like to express my thank to Dr S.D.Brotherton, Dr N.D.Young and Dr J.R.Ayres for many useful discussions on the physics and behaviour of poly-Si TFTs and also to Dr M.J.Trainor, Mrs R.M.Bunn and Mrs A.Gill for processing the test devices, circuits and arrays and to Mr A.D.Pearson for fabricating the liquid crystal cells. Thanks also go to Dr D.G.Haigh and Dr S.E.Day of University College London, Dr J.B.Hughes and Dr A.G.Knapp of Philips Research Laboratories for their help and advice during the course of this work. I would also like to thank Philips Research Laboratories who have funded this work and supported my contact with University College London.
1 Introduction

Video displays, that is displays which are capable of producing high resolution, grey scale images with frame rates of at least 25 frames/second, are widely used in domestic and professional electronic systems. The application which over the last 80 years has driven many of the developments in display technology and which today remains the main application for video displays is television. At a time when the most widely used video display device, the Cathode Ray Tube (CRT), is celebrating its 100th anniversary, a much more recent technology, that of Active Matrix Liquid Crystal Displays (AMLCD), is taking an increasingly important position within the video display market.

1.1 The Video Display Market

The market for video displays is large and is dominated by the CRT. No other display device offers the same combinations of high image quality and low manufacturing cost. The world wide market for CRTs rose to 220 million units in 1996 with a value of nearly 20,000 million US$.\textsuperscript{[1 Castellano 1997]} Television represents the largest segment of the market accounting for 70% of CRTs manufactured.\textsuperscript{[1 Smith 1996]} The consumer TV market is cost sensitive and the low cost and high picture quality offered by the CRT make it an ideal display device for this application. Computer monitors form the second major application of the CRT accounting for a further 26% of displays manufactured. Despite the dominance of the CRT active matrix liquid crystal displays have become established as the preferred display technology for certain key application areas, those in which the CRT is far from ideal. The main limitation of the CRT is its bulk. The high mass and large volume of the evacuated glass envelope mean that the CRT is unsuitable for portable and hand held equipment such as computers, small televisions and electronic cameras. In these applications where low mass, compactness and low power are critical parameters active matrix liquid crystal displays have become the preferred display technology.

The field of active matrix liquid crystal displays has seen rapid development over the last fifteen years with a number of the major electronics companies, particularly in Japan, making large investments in order to industrialise this technology. The first AMLCDs were small, 1-3 inches diagonal, and began to appear in products, such as hand held televisions, in the mid 1980’s. By the end of the 80’s the size of displays had increased to
around 5 inches diagonal as the equipment and processes for fabricating the displays improved. In the early 90’s a number of companies decided to invest in large scale production facilities capable of producing displays of around 10 inches diagonal for use in the growing market for notebook computers. Between 1990 and 1995 the value of the market for liquid crystal displays grew on average by 25% each year, reaching a value of around 8,000 Million US$ by the end of this period. [Nikkei Microdevices 1996] 1995 proved to be a difficult year for LCD manufacturers as an increase in production capacity coincided with a reduction in the growth of the notebook PC market. The price of a 10.4 inch VGA TFT display dropped by 50% in one year, prompting manufacturers to seek new markets for their displays. One of these markets is desktop monitors where the AMLCD is competing directly with the CRT. The size of active matrix displays is continuing to increase with displays for desktop applications currently based around 15 inches and with announcements of displays over 22 inches diagonal becoming available during 1998. The cost of these displays is high compared to CRT monitors, and their use is restricted to applications where the small footprint of the LCD monitor is a significant advantage, such as in financial dealing rooms and other business computing applications. The resolution of the displays has also been increased for the desktop monitor application with UXGA (1600x1200) resolution displays being developed for use in computer aided design. While large high resolution displays are being developed for use as desktop monitors, smaller, lower cost and low power displays are being developed for use in hand held computers, electronic cameras and car navigation systems. One of the routes to achieving lower cost, more compact and more robust displays is to integrate the drive circuits for the display onto the displays substrate. The drive circuits are then fabricated at the same time as the active matrix of the display using the same thin film transistors. This follows the trend of increasing circuit integration which can be seen in electronic products more generally.

1.2 Large Area Electronics

The technology for manufacturing active matrix LC displays is very different from the vacuum device technology of the CRT. Each active matrix display contains a million or more electronic switching devices which control the addressing of the display’s pixels. The displays are fabricated under clean room conditions similar to those used for integrated circuit manufacture. Many of the processes used to make the displays are also similar to those used in the production of integrated circuits including deposition of metal,
insulating and semiconducting layers and patterning of the layers using photolithography. In fact an active matrix display can be thought of as a very large integrated circuit and this has led to the use of the term large area electronics to describe this field.

Active matrix liquid crystal displays are the most obvious application for large area electronics technology but there are also others. In particular, large area imaging devices for use in fax machines, scanners, copiers and medical imaging have been developed using technologies similar to those used for active matrix displays. In the future there are likely to be other new applications where the manufacturing techniques and circuit design experience developed for active matrix displays can be applied.

1.3 Outline of Thesis

The aim of the work described in this thesis is to investigate some of the issues of circuit design using Thin Film Transistors (TFT). The particular application which is considered is the integration of the drive circuits for active matrix liquid crystal displays onto the display substrate. In the following chapter, chapter 2, the basic operation of an active matrix liquid crystal display is described and the range of different technologies which can be used for fabricating the electronic devices within the display is indicated.

Low temperature polysilicon (poly-Si) is the most promising technology for drive circuit integration and it is this technology which has been used for fabrication of the circuits described in this work. Chapter 3 describes the electrical characteristics of two types of low temperature poly-Si TFTs which have been developed at Philips Research Laboratories (PRL). The performance of simple circuits fabricated using these poly-Si TFTs is described in chapter 4. These circuits form the basic building blocks from which more complex circuits, described in chapter 5, are constructed.

The main interest in circuits fabricated using TFTs is the integration of the row and column addressing circuits for active matrix liquid crystal displays. The issues involved in the design of such circuits are discussed in some detail in chapter 5. The extension of current drive circuit design techniques to the larger sized displays which become possible with low temperature poly-Si technology is considered. The chapter concludes with the presentation of a prototype display which has integrated row and column drive circuits.
A novel approach for addressing active matrix liquid crystal displays using digital video information is described in chapter 6. The technique uses a serial digital to analogue converter circuit fabricated within each pixel of the display to convert serial digital information applied to the column electrodes into the analogue voltages required to drive the liquid crystal. The results of measurements made on test pixels are presented and comments are made on the potential use of this technique.

Yield is an important issue for active matrix displays since it can have a dramatic impact upon the cost of producing the displays. Integrating the row and column drive circuits may lead to a reduction in display yield. In chapter 7, a number of existing techniques for improving the yield of integrated drive circuits are presented and a novel approach to self testing circuits is described.

The ability to integrate circuits onto the substrate of active matrix displays will in the future allow integration of more than just the display drive circuits. Chapter 8 considers what other circuits might also be integrated onto displays in the future. The work described in this thesis is summarised in chapter 9 and suggestions of areas where the work could be extended in the future are given.

1.4 Statement of Originality

The design, layout, measurement and analysis of the circuits reported in this thesis was carried out by the author, unless indicated otherwise within the text. Fabrication of the devices, circuits and displays was carried out by staff of the Philips Research Laboratories.\textsuperscript{[PRL]}

1.5 Publications and Patents

Three patent applications have been made\textsuperscript{[M Edwards P1][M Edwards P2][M Edwards P3]} and two papers have been published in connection with this research.\textsuperscript{[M Edwards 1994][M Edwards 1995]}
2 Active Matrix Liquid Crystal Displays And Thin Film Transistors

2.1 Introduction
The search for an alternative high information content display to the Cathode Ray Tube (CRT) has for many years driven research into flat panel displays. Of the various display technologies investigated Liquid Crystal Displays (LCDs) have proved to be particularly successful. Since the first liquid crystal displays were reported in 1968[^1] a number of different Liquid Crystal effects have been developed. One of these, the Twisted Nematic (TN) effect[^2] when combined with the technique of Active Matrix addressing allows displays to be produced which can rival the performance of the CRT. This section introduces the TN-LC effect, the technique of active matrix addressing and the opportunity this offers for integration of circuits onto the display substrate using Thin Film Transistors.

2.2 The Twisted Nematic LC Cell
The basic structure of a TN-LC cell is shown in Figure 2-1. The cell acts as a light modulator and is often operated in a transmissive mode where the cell is illuminated from below and viewed from above. It consists of two glass plates which are separated and have a layer of LC material between them. The inside surfaces of the plates are coated with a transparent conducting electrode, typically Indium Tin Oxide (ITO). The cell is placed between linearly polarising layers and operates by altering the polarisation of the light passing through it. By treating the inner surfaces of the glass plates the long rod-shaped molecules of the LC are made to form into a helix structure within the body of the liquid, as illustrated in the diagram on the left of Figure 2-2.

The direction of orientation of the molecules rotates through an angle of 90° moving from one side of the cell to the other. The polarising layers placed on either side of the cell are arranged with their plane of polarisation parallel to the direction of orientation of the LC molecules at the surface.
Figure 2-1 Twisted Nematic LC Cell

Figure 2-2 Operation of TN-LC Cell

Plane polarised light entering the bottom of the cell is guided by the optical properties of the LC molecules and its plane of polarisation is rotated through 90° as it passes through the LC layer. As the polarisation of the top polariser is arranged at right angles to that at the bottom, the light is able to pass through this second polariser and the cell has a high transmission and appears to be bright.
The optical behaviour of the cell can be altered by creating a potential difference between the two transparent electrodes. When a voltage is applied between the two electrodes an electric field is generated within the LC layer. This causes the LC molecules to experience a force which tends to cause them to reorientate with the direction of their long axis parallel to the direction of the electric field, as illustrated on the right of Figure 2-2. The reorientation of the molecules disrupts the helical structure within the cell and alters the degree of rotation of the polarised light. Light leaving the top of the cell no longer has the same plane of polarisation as the top polarising layer and much of the light is absorbed causing the cell to appear dark.

By varying the potential applied between the two electrodes of the cell a continuous variation of transmission from a high level to a low level can be produced. This is illustrated in Figure 2-3 which shows how the relative transmission of a TN-LC cell varies with the applied voltage. It is necessary to periodically invert the polarity of the voltage applied to the cell in order to avoid degradation of the LC material. The transmission of the cell is determined by the root mean square (rms) value of the alternating voltage waveform applied to it. When the voltage is low the transmission of the cell is high but as the voltage increases above a threshold value $V_{th}$, typically $2V_{rms}$, the transmission starts to fall. When the voltage reaches the saturation value $V_{sat}$, typically $4V_{rms}$, the transmission tends towards a minimum value. An important feature of TN-LC cells is their inherent grey scale capability. Grey levels are produced simply by driving the LC cell with an appropriate voltage between the threshold and saturation values.

The LC cell described so far represents only a single display element, the brightness of which can be controlled by varying the applied signal voltage. For a high resolution display a
million or more of these elements must be combined in a matrix of rows and columns in such a way that each can be individually addressed with video information. This is achieved using the technique of active matrix addressing.

2.3 Active Matrix Addressing

Active matrix addressing of LC displays was first proposed in a paper by Lechner et al. in 1971. The advantages of active matrix addressing can be illustrated by comparing it to the conventional passive matrix approach. In a matrix display device the individual display elements, pixels, are addressed by means of row and column addressing electrodes, as indicated in Figure 2-4. This diagram shows an electrical equivalent circuit for part of a passive matrix LC display in which individual display elements or pixels are represented by capacitors. Video information to control the brightness of the display elements is applied to the column electrodes of the display and selection signals are applied to the row electrodes. The display is normally addressed one line at a time, signals representing the brightness level for a complete row of pixels are applied to the columns and a selection signal is applied to the appropriate row.

![Figure 2-4 Electrical equivalent circuit of passive matrix LCD](image)

During each field of the video signal, every row in the display is addressed in turn to build up a complete picture. One of the characteristics of passive matrix addressing is that the signal representing the video information for a particular display element appears across that element for only a small fraction of the field time. The reason for this is that once a particular row of picture elements has been addressed the column signals must be changed to
those for the next row of pixels. The ratio of the maximum rms voltage to the minimum rms voltage that can be produced across a display element decreases as the number of rows of elements increases. This means that as the resolution of a passive matrix LC display is increased the contrast ratio, the ratio of the maximum to the minimum brightness levels, decreases. In practice, because of this relationship between contrast and resolution and the additional effects of crosstalk and poor angular viewing characteristics, it is not possible to produce a high performance TN-LC video display using passive matrix addressing.

In an active matrix display the limitations of passive matrix addressing are overcome by connecting an active element, a switching device, in series with each pixel as indicated in Figure 2-5. The active element may be a two terminal device, such as a Thin Film Diode (TFD) or a Metal Insulator Metal device (MIM), or it may be a three terminal device, a Thin Film Transistor (TFT). Figure 2-5 illustrates the equivalent circuit for a display using TFTs. A common feature of these active elements is that they can be switched between a low impedance conducting state and a high impedance non-conducting state under the control of addressing signals, called row selection signals, which are applied to the row electrodes of the display.

![Figure 2-5 Electrical equivalent circuit of active matrix LCD](image)

Figure 2-6 shows a cross section through a small part of an active matrix LC display which uses TFTs as the active elements. The basic structure is the same as the TN-LC cell however the transparent ITO electrode on the lower glass substrate is now patterned to form individual pixel electrodes. A thin film transistor is associated with each pixel electrode and is connected between the adjacent row and column electrodes and the pixel electrode.
Figure 2-7 shows a simple electrical equivalent circuit for a single pixel in the display and the associated row and column voltage waveforms. The LC pixel can be represented by a capacitor and the thin film transistor can be considered to behave like an enhancement mode n-channel insulated gate field effect transistor. The TFT has gate, source and drain connections and by applying a positive voltage to the gate, a low resistance is obtained between the drain and source. The gate of the transistor is connected to the row electrode, the source to the column electrode and the drain to the pixel.

When the pixel is addressed a voltage which represents the video level required on the pixel is first applied to the column electrode. The TFT is then switched on by taking the row electrode to a high voltage level. Current flows between the drain and source of the transistor until the voltage on the pixel capacitor is the same as that on the column. At the end of the addressing period the row voltage is returned to a low level and the TFT turns off. While the TFT is turned off, the voltage across the LC pixel is maintained by the pixel capacitance. In the ideal case, once the pixel has been addressed the pixel voltage will not change until the pixel is addressed again with new information.

It is this ability to maintain the voltage across the LC display elements when they are not being addressed which allows active matrix displays to achieve a high level of performance. There is in principle no degradation of the drive voltages on the display elements as the resolution of the displays is increased and TN-LC displays having more than 1000 rows can be made without compromising the display performance.

24
2.4 Drive Circuits for Active Matrix LC Displays

As the gates of all the TFTs in one row of an active matrix display are connected to the same row electrode, a complete row of pixels must be addressed at the same time using "line at a time" addressing. Voltages must be established on the columns of the display which represent the variation of the video information through one complete line of the video signal. These voltages are produced by the column drive circuits which effectively perform a serial to parallel conversion of the information in each line of the video signal. A schematic diagram of a simple column drive circuit is shown in Figure 2-8. It consists of a large number of sample switches, one for each column in the display, which take samples from the signal at the video input and transfer them to the columns where they are held on the column capacitance. A shift register is used to control the switching of the sampling circuits.

The circuit is operated by applying a pulse to the input of the shift register at the start of each line of the video signal. The register is clocked at the sampling frequency, typically 1-20MHz, and as the pulse appears at each output of the register in turn the corresponding sampling circuit takes a sample from the video signal. At the end of the video line period, when all the circuits have taken a sample, the video information from one line of the signal is available in parallel on the columns of the display and the appropriate row can be addressed.
To build up a complete picture on the display, each row is addressed in turn by taking the row voltage to a high level for a short period of time and then returning it to the low level. This function is performed by the row drive circuits. In its simplest form the row drive circuit simply consist of a shift register having each successive output connected to one of the rows in the display, as shown in Figure 2-9.

Figure 2-9 Simple row drive circuit
The addressing of the display is initiated by feeding a single pulse to the input of the register. As the register is clocked, the pulse appears at each output in turn selecting one of the rows. The row drive circuits operate at a relatively low frequency compared to the column drive circuits, 10-30kHz, determined by the line frequency of the video signal.

2.5 Integrated Drive Circuits

It was realised at an early stage that when transistors are used as the switching devices in active matrix displays, these same transistors could in principle be used to fabricate other circuits on the display substrate. Integration of the row and column drive circuits offers a number of advantages over conventional techniques such as Chip On Glass (COG) in which crystalline silicon integrated circuits are bonded to contacts on the display substrate using an anisotropic conducting adhesive. The principle advantages are a substantial reduction in the interconnect complexity, that is the number and density of signal connections, and a reduction in the size and cost of the displays. When the drive signals for the display are generated by conventional circuits, for example COG drivers, a separate electrical connection to the display substrate is required for each row and column addressing electrode. A typical television display would have more than 1200 connections raising issues in terms of both the yield and reliability of the connections to the display. When the drive circuits are integrated onto the display substrate using TFTs, the number of external connections is reduced to only those power supply, clock and video signal connections required to operate the circuits. In practice there may be no more than 20-40 of these connections. Drive circuit integration also has the potential for lower display costs since conventional silicon drive circuits account for a significant fraction of the total cost of a display. If little or no increase in processing complexity is required in order to integrate the drive circuits then these circuits will add little to the cost of fabricating the active matrix of the display.

Important issues for drive circuit integration include the performance of the thin film transistors, the stability of the circuits over long periods of time and the effect of circuit integration on display yield. As the following section will show there are a wide range of technologies for producing the transistors in active matrix displays and these result in transistors with an equally wide range of electrical characteristics. The favoured technologies for the future make use of inexpensive glass substrates and these require the use of low
temperature processing. It is important that drive circuit integration should not result in a significant reduction in the yield of working displays. Redundancy and repair techniques can be used to enhance the yield of the active matrix of the display and the adoption of fault tolerant design techniques may initially be an important factor in achieving the required yield of working circuits.

2.6 TFT Technologies

The transistors used in active matrix LC displays can be fabricated using a number of different technologies, each having certain advantages and disadvantages. The main technologies are summarised in Figure 2-10 which illustrates one aspect of their performance, the field effect mobility.

![Figure 2-10 TFT technologies](image)

This is an important parameter since the speed at which circuits made using a particular technology can operate is proportional to the mobility. The use of crystalline silicon wafers and conventional silicon processing techniques for producing active matrix displays is attractive from the point of view of drive circuit integration. The high performance of the crystalline silicon transistors makes them ideally suited for integration of circuits around the display and prototype displays have been demonstrated. However, the use of a silicon wafer as the display substrate has a number of limitations. For directly viewed displays the cost and limited size of the silicon substrates makes this approach unattractive.
Projection systems make use of displays which are small in size and therefore the limited area of silicon substrates is not a problem. As the substrate is opaque, the display has to be operated in a reflective rather than a transmissive mode and high resolution projection display systems using this approach are under investigation. A technique has also been developed for making transmissive displays with crystalline silicon. This involves transferring the complete active matrix, including the addressing circuits, from a silicon wafer onto a transparent glass or quartz substrate which can then be used to make a TN-LC display. [Salerno 1992]

Other technologies used for active matrix displays are based on thin film techniques where a thin layer of semiconductor material is used to form the transistors. The compound semiconductor cadmium-selenide (CdSe) was used to produce the first active matrix LC displays [Brody 1973] and this material has some attractive features including relatively high mobility and low processing temperatures [De Rycke 1990]. Despite its early start, CdSe does not yet have a significant presence in the AMLCD market.

The first silicon thin film technology to be developed for use in active matrix displays and circuits was based on amorphous silicon (a-Si). [LeComber 1979] The ability to deposit a-Si layers over large area glass substrates makes it ideal for direct view active matrix displays. Displays have been demonstrated with sizes ranging from less than 3 inches to more than 20 inches diagonal and amorphous silicon is currently the leading technology for active matrix displays. The mobility of a-Si devices is limited, typically 0.3-1 cm²/Vs, making the integration of drive circuits onto a-Si displays very difficult. While circuits can be made using a-Si TFTs, the low mobility is reflected in low operating speeds and until recently published results were limited to a number of research prototype row addressing circuits where high speed operation is not required. [Chenevas-Paule 1984][Akiyama 1986][Khazak 1989] A prototype display having both row and column drive circuits integrated using a-Si TFTs has more recently been demonstrated, made possible by a novel design for the column drive circuits. [Stewart 1995] TFT circuits using a-Si devices require relatively high power supply voltages to achieve acceptable performance and as a result the long term stability of the TFTs is an issue. Careful circuit design is needed to avoid excessive stressing of the transistors, prolonged gate bias being the main source of instability in these devices.
The use of polycrystalline silicon (poly-Si) to produce transistors allows much higher mobilities to be achieved than is possible with a-Si. A number of different processes exist for making poly-Si and these result in devices with a range of mobility values. The most highly developed techniques use high temperature processing, ≈1000°C, using quartz rather than glass substrates. The fabrication techniques for these devices are very similar to those used in the production of conventional silicon MOS integrated circuits and are therefore relatively well understood. There are many examples of high temperature poly-Si displays with integrated row and column drive circuits.\cite{Matsuo1994, Nakamura1994} However, the high cost of quartz substrates compared to glass means that display sizes are limited. The main applications for these displays are projection systems and viewfinders for which display diagonals are typically less than two inches.

A number of low temperature processes for fabricating poly-Si material have been developed. One of these is Solid Phase Crystallisation (SPC) in which an amorphous silicon film is crystallised to form polycrystalline silicon by heating in a furnace at a moderate temperature, 600-650°C. The mobility values achieved using this process are somewhat lower than those of a high temperature process but considerably higher than can be achieved from amorphous silicon. A second technology for converting amorphous silicon to polycrystalline silicon is the use of a laser to heat the a-Si film.\cite{Ohshima1993} In this process the laser is scanned across the substrate resulting in localised melting of the silicon and formation of a thin layer of high quality poly-Si material. The poly-Si TFTs having the highest mobility values have been fabricated using laser crystallisation. This technology is now receiving much attention with a number of pilot production facilities being established and the first products becoming available.

### 2.7 Summary

Active matrix addressing techniques have allowed liquid crystal displays to be developed which in most respects match the performance of the CRT as a video display device. By introducing an electronic switching device in series with each pixel, the dependence of the display performance on resolution which is observed for passive matrix addressing is largely absent in active matrix addressed liquid crystal displays. Displays which use amorphous silicon (a-Si) thin film transistors as the electronic switching devices currently dominate the market for direct view AMLCDs with display sizes which range from less than 3-inches to
more than 20-inches diagonal. This position has been established as a result of 18 years of steady development of a-Si technology and the techniques for manufacturing active matrix LC displays. In common with other types of matrix display device, the large number of row and column addressing signals which are required by an active matrix liquid crystal display make provision of the row and column drive circuits an important aspect of the overall display design. The conventional crystalline silicon integrated circuits used for addressing a-Si active matrix displays contribute a significant fraction to the total cost of the display and represent a source of defective displays both at the time of manufacture and while in service. Integration of the drive circuits onto the display substrate using TFTs therefore has the potential to reduce the cost of displays and to increase their robustness, reliability and compactness. However, the low field effect mobility of a-Si TFTs makes them unattractive for drive circuit integration.

High temperature polycrystalline silicon technology is applied to small displays, less than 2-inches diagonal, for projection systems and direct view applications such as camera viewfinders. The relatively high performance of high temperature poly-Si TFTs allows integration of the display’s drive circuits but this technology cannot easily be extended to larger direct view displays because of the high cost of the quartz substrates needed to withstand the high temperature processing. Low temperature poly-Si processing allows the advantages of drive circuit integration to be extended to larger sized displays and is the most rapidly developing technology at the present time. The processing temperatures are compatible with glass substrates allowing, in principle, the same range of display sizes to be developed as are currently available using a-Si technology. Low temperature poly-Si processing has been used to fabricate the circuits described in this thesis and in the following chapter the performance of low temperature poly-Si TFTs is examined in some detail.
3 Electrical Characteristics of Low Temperature Poly-Si TFTs

3.1 Introduction

The electrical characteristics of low temperature poly-Si transistors differ in a number of respects from conventional MOS devices. This chapter begins by briefly reviewing published results illustrating the performance of thin film transistors fabricated using three different poly-Si technologies. Two of these technologies are low temperature, glass compatible processes comparable to those investigated at PRL while the third is a high temperature technology based on quartz substrates. This high temperature technology is now in production within a number of companies and provides a useful bench mark for the low temperature devices. In the sections of this chapter which follow the review, various aspects of the performance of the low temperature poly-Si devices fabricated at PRL are described and illustrated with measurements.

3.2 Review of Poly-Si TFT Performance

A number of different techniques for forming low temperature poly-Si thin film transistors have been considered over the last 10 years. Two of these, Solid Phase Crystallisation (SPC) and laser crystallisation, have been investigated at PRL. A brief description of the structure of these devices is given in section 3.3. The published performance of TFTs fabricated using these two low temperature technologies and the high temperature process are summarised in the following tables. It can be seen that there is a considerable spread in the electrical characteristics of devices fabricated using each technology reflecting variations in the details of the processes used in each case.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Mobility (cm²/Vs)</th>
<th>Threshold (V)</th>
<th>Mobility (cm²/Vs)</th>
<th>Threshold (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A Lewis 1992</td>
<td>100</td>
<td>2</td>
<td>50</td>
<td>-3</td>
</tr>
<tr>
<td>M Matsuo 1994</td>
<td>101</td>
<td>?</td>
<td>70</td>
<td>?</td>
</tr>
<tr>
<td>N Harada 1994</td>
<td>160</td>
<td>?</td>
<td>110</td>
<td>?</td>
</tr>
<tr>
<td>T Hashizume 1994</td>
<td>118</td>
<td>?</td>
<td>88</td>
<td>?</td>
</tr>
</tbody>
</table>

Table 3-1 Reported performance of high temperature poly-Si TFTs
<table>
<thead>
<tr>
<th>Reference</th>
<th>Mobility (cm$^2$/Vs)</th>
<th>Threshold (V)</th>
<th>Mobility (cm$^2$/Vs)</th>
<th>Threshold (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M Takabatake 1991</td>
<td>35</td>
<td>8.5</td>
<td>30</td>
<td>-16</td>
</tr>
<tr>
<td>A Lewis 1992</td>
<td>40</td>
<td>2</td>
<td>20</td>
<td>-8</td>
</tr>
<tr>
<td>S Fluxman 1992</td>
<td>35</td>
<td>11</td>
<td>33</td>
<td>-16</td>
</tr>
</tbody>
</table>

Table 3-2 Reported performance of SPC poly-Si TFTs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Mobility (cm$^2$/Vs)</th>
<th>Threshold (V)</th>
<th>Mobility (cm$^2$/Vs)</th>
<th>Threshold (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y Nishihara 1992</td>
<td>62</td>
<td>1.7</td>
<td>51</td>
<td>-2.7</td>
</tr>
<tr>
<td>S Yamamoto 1992</td>
<td>69</td>
<td>1</td>
<td>54</td>
<td>-2.9</td>
</tr>
<tr>
<td>H Ohshima 1993</td>
<td>38</td>
<td>?</td>
<td>30</td>
<td>?</td>
</tr>
<tr>
<td>S Chen 1993</td>
<td>208</td>
<td>1.5</td>
<td>92</td>
<td>-0.7</td>
</tr>
<tr>
<td>K Sera 1994</td>
<td>45</td>
<td>3</td>
<td>33</td>
<td>-4</td>
</tr>
<tr>
<td>T Morita 1995</td>
<td>100</td>
<td>0.3</td>
<td>53</td>
<td>-2.5</td>
</tr>
<tr>
<td>Y Morimoto 1995</td>
<td>45</td>
<td>2.5</td>
<td>20</td>
<td>-5.5</td>
</tr>
<tr>
<td>H Hayashi 1995</td>
<td>73</td>
<td>?</td>
<td>30</td>
<td>?</td>
</tr>
<tr>
<td>S Inoue 1995</td>
<td>181.8</td>
<td>?</td>
<td>86.5</td>
<td>?</td>
</tr>
<tr>
<td>T Ohori 1996</td>
<td>59</td>
<td>1.5</td>
<td>49</td>
<td>-1.16</td>
</tr>
<tr>
<td>N Kato 1996</td>
<td>62</td>
<td>?</td>
<td>35</td>
<td>?</td>
</tr>
<tr>
<td>M Furuta 1996</td>
<td>48.5</td>
<td>3.9</td>
<td>23.6</td>
<td>-6.6</td>
</tr>
</tbody>
</table>

Table 3-3 Reported performance of laser crystallised poly-Si TFTs

The field effect mobility of high temperature poly-Si devices is typically around 100 cm$^2$/Vs for n-channel transistors and somewhat more than half this value for p-type devices. The threshold voltage of the devices is relatively low and well matched for n-channel and p-channel transistors. The transistor mobility and threshold voltage values reported for devices fabricated using the low temperature SPC poly-Si process are poorer than those of the high temperature devices. The field effect mobility of the TFTs is approximately one third of that achieved using high temperature processing and the threshold voltages are higher, particularly in the case of the p-channel transistors. The performance of the laser crystallised poly-Si devices is much better than the SPC devices and in some cases exceeds that of high temperature poly-Si. This improvement in performance has been attributed to the increased quality of the polysilicon film resulting from laser crystallisation.\[S Brotherton 1995\] The devices exhibit high values of field effect mobility and the threshold voltages for both n-type and p-type transistors are relatively low and can be well matched.
Defining the values of mobility and threshold voltage for poly-Si devices is not straightforward due to the relatively high density of carrier trapping states. These traps may be associated with defects which are within the grains of the polysilicon, at the grain boundaries or at the surface of the polysilicon film. Their effect is to cause the electrical behaviour of poly-Si TFTs to depart, to some extent, from that described by the conventional MOS device equations. One effect of the high density of trapping states is to introduce a pronounced gate voltage dependence to the field effect mobility, as determined from the transconductance of the transistor at low drain bias [S. Sze 1981]. In high temperature poly-Si devices [A. Lewis 1992] the effective mobility has been observed to increase steadily as the gate voltage rises above threshold and then to saturate at higher values of gate voltage. In contrast to this the field effect mobility of crystalline silicon devices is high even when the gate voltage is only just above the threshold voltage. Other parameters of poly-Si TFTs which are influenced by the high density of trapping states are the threshold voltage, which is generally higher than in crystalline silicon devices, and the slope of the transfer characteristics of the devices below the threshold voltage, the sub-threshold slope, which is less steep than in crystalline silicon transistors.

The use of poly-Si thin film transistors for analogue circuit designs is of interest for application in displays and sensors. A limited amount of work has been published on the characteristics of high temperature poly-Si TFTs [A. Lewis 1988] and SPC poly-Si TFTs [H-G Yang 1994] from the point of view of analogue circuit design. The gate voltage dependence of the transconductance of poly-Si TFTs means that the transconductance of a device in saturation and at low gate bias may not scale with the width and length of the transistor as would be expected from the simple MOS device equations [A. Lewis 1988]. Another feature of poly-Si TFTs which is of importance in analogue circuit design is the presence of a kink in the output characteristics of the transistors which results in an increased output conductance at higher drain biases. This has been attributed to impact ionisation due to the high electric field at the drain of the device [A. Lewis 1988] and it has been compared to the kink effect which is observed in crystalline silicon SOI devices. It has also been observed that poly-Si TFTs exhibit significantly higher levels of 1/f noise than would be expected from crystalline silicon devices [A. Lewis 1988][C. Reita 1994]
3.3 PRL Low Temperature Poly-Si Technologies

The circuits described in this thesis have been fabricated using one of two low temperature poly-Si thin film transistor processes, either Solid Phase Crystallisation or Laser Crystallisation. In both cases the development of the processes and fabrication of the devices was carried out by staff of the Philips Research Laboratories [PRL].

The first process is a low temperature (600-625°C) Solid Phase Crystallisation (SPC) process [S Brotherton 1991] in which an amorphous silicon film on a glass substrate is crystallised by heating in a furnace to produce poly-Si. A cross section illustrating the structure of an n-channel device fabricated using this process is shown in Figure 3-1. The p-channel devices have the same structure as the n-type but use p+ rather than n+ doped regions. The device is a top gated structure in which ion implantation is used to form the source and drain regions. The poly-Si gate acts as a mask during the implantation to produce a self aligned structure with low gate/source gate/drain capacitance. As in conventional MOS devices, channel region implants can be used to improve the electrical characteristics of the devices, in particular to control the threshold voltage and to match the threshold of the n-channel and p-channel transistors for CMOS circuits.

In the second process amorphous silicon starting material is crystallised by irradiation of the film using an Excimer laser [S Brotherton 1994-1] to produce a high quality poly-Si film. The cross section of a laser crystallised poly-Si transistor is shown in Figure 3-2. These devices have a metal gate electrode which is formed after ion implantation of the source and drain regions and as a consequence the devices are not self aligned and have significant gate/source gate/drain overlap capacitance. As in the SPC process, p-channel devices are produced by using a p+ implant to form the source and drain regions. In order to improve the long term stability of devices a Lightly Doped Drain (LDD) structure is used in n-channel transistors. Figure 3-3 illustrates the gate overlapped LDD approach [M Edwards 1995] which has been adopted in the circuits described in later sections of the thesis.
3.4 DC Characteristics

There are considerable differences in the electrical behaviour of TFTs fabricated using the SPC and laser crystallisation processes. Transfer characteristics of typical n-type and p-type transistors fabricated using the SPC process are shown in Figure 3-4 and Figure 3-5. The difference between these two pairs of devices is that those in Figure 3-5 have been fabricated with additional threshold shifting channel region implants.
For the n-channel transistors it is possible to obtain approximate values for the threshold voltage and field effect mobility from a plot of drain current versus gate voltage in the linear operating region (Vds=2V), as shown in Figure 3-7. The mobility value for these n-channel devices is typically 15 cm^2/Vs while the threshold voltage is 5.5V for standard devices and 7.9V for devices which have received a threshold shifting channel implant. The characteristics of the p-channel devices are much poorer than the n-type. It can be seen in the plots of the transfer characteristics of the devices that the slope of the characteristic in the sub-threshold region is lower, with the effect that the device turns on more gradually as the gate voltage is increased. This can also be seen in the plot of the device characteristics in the linear operating region, Figure 3-6, where the slope of the plot continues to increase even as the gate voltage approaches -20V. The values of threshold voltage and mobility approximated from such a plot are 0.7 cm^2/Vs and -14.4V respectively. The low value of mobility reflects the fact that even at this relatively high gate bias the device is effectively operating in the subthreshold region. Measurements made at higher gate biases, above 30V, indicate a typical p-channel device mobility of up to 8cm^2/Vs. The gate voltage dependence of the field effect mobility, determined from the transconductance of the device, is illustrated in Figure 3-8.
For the n-channel device, as the gate voltage increases above the threshold voltage there is a steady increase in the effective mobility until it saturates at gate-source voltages above 15V. This is similar to the behaviour reported for other poly-Si devices. The effective mobility of the p-channel device only starts to rise as the gate voltages approaches the maximum value for these measurements, 20V. The values of mobility measured for the n-channel TFTs are somewhat lower than those reported for comparable technologies in section 3.2. This difference is believed to be related to the thickness of the poly-Si layer used to form the transistors.\cite{Brotherton1994} In PRL SPC devices the thickness of this layer is reduced in order to minimise the device leakage currents, an important requirement for the pixel transistors of an active matrix LC display. However, a consequence of using a thinner poly-Si film is a lower value of mobility. The poor performance of the p-channel devices, in particular the high threshold voltage, follows the trend observed in published reports of devices fabricated with similar technologies.
The higher quality of poly-Si films formed by laser crystallisation results in TFTs with greatly improved electrical characteristics. The transfer characteristics of a p-channel device and an n-channel device with LDD are shown in Figure 3-9, while the characteristic of an n-channel device which does not include LDD is shown in Figure 3-10.

**Figure 3-9** Laser crystallised poly-Si TFT characteristics

**Figure 3-10** Laser crystallised poly-Si TFT characteristic without LDD

**Figure 3-11** Laser crystallised poly-Si TFT p-channel

**Figure 3-12** Laser crystallised poly-Si TFT n-channel with LDD
Much higher values of field effect mobility can be achieved with laser crystallisation compared to the SPC process. From the characteristics illustrated in Figure 3-11 and Figure 3-12 where the devices are operating in the linear region, mobility values of approximately $105\text{cm}^2/\text{Vs}$ and $88\text{cm}^2/\text{Vs}$ are calculated for n-type and p-type devices respectively. The threshold voltage values are $+6.0\text{V}$ and $-5.6\text{V}$. There is good matching between the characteristics of the complementary devices and the particularly poor sub-threshold behaviour seen in the SPC p-channel devices is absent in the laser processed TFTs. Values of mobility and threshold voltage obtained from the characteristics of the devices in the saturation region are slightly different. Mobility values of $120\text{cm}^2/\text{Vs}$ and $98\text{cm}^2/\text{Vs}$ are obtained for n-type and p-type devices respectively while the threshold voltage values are $+4.9\text{V}$ and $-4.1\text{V}$.

In calculating the mobility of the n-channel devices, it has been assumed that the gate length is $6\mu\text{m}$. In fact in the case of transistors with LDD the channel consists of $6\mu\text{m}$ of undoped poly-Si and $3\mu\text{m}$ of lightly doped material. It can be argued that the effective channel length of the device is $9\mu\text{m}$. If a value for the channel length of $9\mu\text{m}$ is taken then a higher value of mobility is obtained, $158\text{cm}^2/\text{Vs}$ in the case of a device operating in the linear region. Care must therefore be exercised in the use of mobility values for devices with gate overlapped LDD to ensure that in calculations of circuit performance consistent values of gate length and mobility are used.

The gate voltage dependence of the field effect mobility, calculated from the device transconductance, is illustrated in Figure 3-13. The effective mobility rises steadily for gate voltages above the threshold voltage and tends towards a maximum value at approximately $10\text{V}$. The values of mobility and threshold voltage measured for the laser crystallised poly-Si devices compare well with devices reported for other laser crystallisation processes and summarised in Table 3-3.

![Figure 3-13 Laser TFT, field effect mobility calculated from transconductance with Vds=1V](image-url)
3.5 Transient Behaviour

From the poor transfer characteristics of the p-channel TFTs fabricated using the SPC process it would be expected that CMOS circuits fabricated using this process would have a correspondingly poor performance. However, the measured dynamic performance of circuits fabricated using these devices is significantly better than these DC characteristics would suggest. This can be explained by considering the transient behaviour of the SPC devices.

The trapping of carriers within the transistors affects their electrical characteristics and because of the relatively high density of trap states in SPC poly-Si the effect of carrier trapping in these devices cannot be neglected. The filling and emptying of the traps takes place at rates which are comparable to the operating speed of the circuits and as a result the transient behaviour of the transistors becomes a significant factor in predicting the performance of circuits.

The variation in the drain current with time for p-channel and n-channel TFTs is illustrated in Figure 3-14. Considering first the p-channel device, when the gate bias is switched to a negative value the drain current initially rises to a high level as the device turns on. However, the current then falls rapidly towards a steady state value which is very much lower than the peak. In the case of the n-channel device the fall in current after the initial peak is very much smaller.

![Figure 3-14 Transient behaviour of SPC TFTs](image-url)
The most likely explanation for the transient behaviour is that when the transistor is first switched on a high concentration of free carriers, holes in the p-type devices and electrons in the n-type, is formed in the channel region below the gate of the device. The movement of these carriers under the influence of the drain-source bias produces the high value of drain current. Over time an increasing number of the carriers are captured by traps within the poly-Si. These trapped carriers are no longer able to contribute to the conduction in the channel of the device, although they still act to balance the charge applied to the gate of the transistor, and as a result the drain current falls.

The gate bias dependence of the transient current peak is illustrated in Figure 3-15 and Figure 3-16. This was measured by applying a square voltage waveform to the gate of the transistor and measuring the change in the drain current of the device as a function of time. The frequency of the gate drive signal was 6Hz and one of the two gate voltage levels was fixed at 0V. The current was recorded at a number of values of time following the switching of the gate from 0V to the second voltage level. The current at times of 5μs, 50μs, 500μs and 5ms after switching are indicated in the figures. The drain source bias was set at 5V. The results clearly show the transient nature of the drain current.

As time increases following the switching of the gate voltage the drain current of the devices decreases and tends towards the value which is measured under DC conditions. It is also clear that the magnitude of the transient effect is greatest at low gate voltage levels when the
transistor is still operating in the subthreshold region. For example in the case of the p-channel device, at a gate voltage of -10V the drain current falls by more than a factor of forty between 5\mu s and 5ms after the application of the gate voltage. At higher gate voltages the reduction in drain current is smaller, at 20V the current falls by a factor of four during the same time period. In the n-type device the time dependence of the drain current is very much lower, less than a factor of 1.6 between 5\mu s and 5ms at V_{GS}= 10V, and when the device is biased well above the threshold voltage the changes become negligible.

The significant transient behaviour of the p-channel devices makes accurate prediction of the performance of CMOS circuits very difficult. The drain current at any moment in time depends not only on the bias conditions at that moment but also on the voltages applied to the device in the past. In circuits where devices are being switched repeatedly between the on and off conditions the switching frequency becomes an important factor. Figure 3-17 shows that for the p-type device, as the switching frequency is increased the magnitude of the transient effect and the peak value of current both decrease.

![Figure 3-17 Change in transient current in p-type SPC TFT with gate switching frequency](image)

The shape of these curves and the frequency range over which the peak current reduces depend on the rate at which traps within the device fill and empty as the transistor is switched. At low frequencies, much of the charge trapped when the device is turned on will be released during the time when the device is turned off and as a result the device will show
a strong transient behaviour with an initially high value of current each time that it is turned on. At higher frequencies, the period during which the device is turned off is insufficient for all the trapped charge to be released and therefore the device will settle into a state where a certain amount of charge remains trapped within the device. This will reduce the magnitude of the transient current when the device is first switched on.

It is beyond the scope of this work to investigate this transient behaviour further. However a knowledge of the presence of this effect is important in understanding why the performance of CMOS circuits fabricated using the SPC process is significantly better than would be expected given the poor DC performance of the p-channel TFTs.

Pulsed measurements illustrating the transient performance of laser crystallised poly-Si TFTs are shown in Figure 3-18 and Figure 3-19. The drain bias applied to the devices is 5V and the gate signal is a square waveform of 6Hz with one level fixed at 0V. The magnitude of the transient effects in these devices is very much lower than in the SPC devices and is restricted to the subthreshold region of the device characteristics. At a gate voltage of 5V the reduction in drain current for both n-channel and p-channel devices is a factor of two during the time period from 5µs to 5ms. For digital circuits which are designed using the DC characteristics of the TFTs and which are operated with supply voltages well above the threshold voltage, this residual transient behaviour can be neglected. However it may be of more significance in analogue circuits where the TFTs may be operated close to threshold.
3.6 Small Signal Characteristics

The high quality of laser crystallised poly-Si TFTs means that they will be used in a wider range of applications than SPC poly-Si devices. One area which is likely to receive more attention in the future is the design of analogue circuits using poly-Si TFTs. The output conductance, \( g_d \), and the transconductance, \( g_m \), of the transistors are important parameters for determining the suitability of laser crystallised poly-Si devices for analogue circuits. The output characteristics of devices having gate lengths of 6\( \mu \)m are shown in Figure 3-20 and Figure 3-21. In n-channel devices which do not include LDD, the output resistance rapidly decreases when the drain bias exceeds approximately 6V, this effect is referred to as the ‘kink effect’ due to the similarity of its appearance to the effect of that name seen in silicon on insulator devices. Introduction of an LDD structure greatly improves the output characteristics of the n-channel devices resulting in a behaviour which is similar to that of the p-channel transistors. The output characteristics of transistors having gate lengths of 15\( \mu \)m are shown in Figure 3-22 and Figure 3-23.

![Figure 3-20 Output characteristics of n-type TFTs L=6\( \mu \)m Vgs=5 to 12V solid=LDD dashed=no LDD](image1)

![Figure 3-21 Output characteristics of p-type TFT L=6\( \mu \)m Vgs=-5 to -12V](image2)

The increased gate length results in a higher output resistance and in the case of the n-channel device without LDD an increase in the drain bias at which the ‘kink’ in the output characteristics becomes apparent. In simple models for conventional MOS transistors the finite output resistance of devices in the saturated region is represented by the channel length
modulation parameter $\lambda$. The output conductance of the device is approximated by the expression $g_d \approx \lambda I_d$. A similar approximation can be made for laser crystallised poly-Si TFTs and the inverse relationship between the channel length modulation parameter and gate length for p-channel and n-channel TFTs is illustrated in Figure 3-24. The values of $\lambda$ were determined by taking the minimum value of the ratio of the output conductance to the drain current, $\lambda \approx g_d / I_d$, for transistors of different gate lengths.

![Figure 3-22 Output Characteristics of n-type TFTs L=15um Vgs=5 to 12V solid=LDD dashed=no LDD](image1)

![Figure 3-23 Output Characteristics p-type TFT L=15um Vgs=-5 to -12V](image2)

![Figure 3-24 Variation of $\lambda$ with gate length for laser crystallised poly-Si TFTs](image3)
The values of $\lambda$, obtained for p-channel devices and for n-channel devices with LDD are similar for channel lengths of less than 10$\mu$m. For longer channel length devices the n-type transistors have higher values of $\lambda$. For TFTs with gate lengths in the range 10-20$\mu$m the minimum values of $\lambda$ for the p-type devices are similar to those typical of a silicon-gate bulk CMOS p-well process\(^{[P \text{ Allen 1987}]}\) while the values for the n-type TFTs with LDD are 2-3 times higher than crystalline silicon devices.

The output conductance of the n-channel TFTs operating in the saturation region depends on the value of the drain source voltage of the TFT. This is illustrated in Figure 3-25 which shows how the ratio of the output conductance to the drain current varies with the difference between the drain-source voltage and the gate-source voltage for an n-channel device with a gate length of 15$\mu$m.

![Figure 3-25 Ratio of output conductance to drain current for n-channel TFT with LDD, L=15$\mu$m W=50$\mu$m, Vgs=5V to 12V](image)

The rapid increase in the ratio of output conductance to drain current for values of $V_{ds}-V_{gs}$ which are less than 0V represents the region where the device moves out of saturation into the linear region and consequently there is a rapid decrease in the output resistance. However, the ratio of output conductance to drain current also increases as the voltage increases above zero and the device moves further into the saturation region. The region in which the value of $\lambda$ is at a minimum is quite narrow so that for maximum gain the n-type transistors should be operated close to the point at which they become saturated. The effect that the drain bias has on the ratio of output conductance to drain current for p-type transistors is significantly lower than for n-type as indicated by Figure 3-26.
The dependence of the transconductance of the TFTs on gate bias for p-type and n-type transistors is illustrated in Figure 3-27 and Figure 3-28. When the gate voltages is well above the threshold voltage and the device is saturated the transconductance is approximately proportional to the gate voltage, as in crystalline silicon MOS devices. The slope of the characteristics is approximately $4 \mu A/V^2$ for the n-channel device and $2 \mu A/V^2$ for the p-channel transistor. These values are approximately four times lower than those of crystalline silicon devices.\[^{[P \text{ Allen 1987}]}\]

![Figure 3-27 Variation of transconductance with $V_{gs}$ n-channel $L=15 \mu m$ with LDD $V_{ds}=1V$ to $14V$](image1)

![Figure 3-28 Variation of transconductance with $V_{gs}$ p-channel $L=15 \mu m$ $V_{ds}=1V$ to $14V$](image2)

The open circuit voltage gain of transistors with gate lengths of 15\(\mu m\) is shown in Figure 3-29 and Figure 3-30. The gain was calculated from the ratio of the transconductance and output conductance values obtained from the DC device characteristics. In both p-channel and n-channel devices the peak gain is approximately 45-50 and the highest gain is achieved when the device is operated with a gate-source voltage close to the threshold voltage. The values of gain are considerably lower than is typical for crystalline silicon MOS devices, 500-2000,\[^{[P\text{ Gray 1982}]}\] the difference being broadly consistent with the fact that the field effect mobility and transconductance of the TFTs are approximately 4 times lower and the output conductance approximately 2-3 times higher than for the crystalline silicon transistors.

48
The increase in the output conductance of the n-channel TFT with increasing drain-source voltage has a clear effect on the gain of the transistor which falls steadily as Vds increases in the saturated operating region. The effect of drain bias on gain in the p-channel device is significantly lower than in the n-channel TFT.

Figure 3-29 Gain of n-channel LDD TFT as a function of bias voltages L=15\mu m

Figure 3-30 Gain of p-channel TFT as a function of bias voltages L=15\mu m
3.7 TFT Stability

The values of threshold voltage for Poly-Si TFTs, in particular for p-channel SPC devices, are large compared to conventional silicon MOS transistors and it would therefore be expected that poly-Si circuits should be operated with relatively high power supply voltages. The voltages applied to the TFTs, and therefore the operating voltage of the circuits, must be limited in order to ensure that the devices are stable over long periods of time. The main cause of instability is hot carrier degradation\textsuperscript{[J Ayres 1994]} and the drain-source voltage seen by the transistor has a strong influence on the rate of degradation. Measurements made by N.D. Young\textsuperscript{[PRL]} on n-channel devices fabricated using the SPC process have indicated that it is necessary to limit the drain source voltage of the transistors to approximately 16V for stable operation over several thousands of hours. This means that for circuits fabricated using this process the supply voltage of the circuits is only two to three times the value of the n-type threshold voltage and is less than the threshold voltage of the p-type devices measured under DC conditions.

The DC characteristics of the laser crystallised Poly-Si devices are significantly better than the SPC transistors. However, the values of threshold voltage are still relatively high and the circuits are typically operated with supply voltages of 2-3 times the n-channel and p-channel threshold voltages. The improvement in the electrical characteristics of the devices, in particular the increased mobility, has been found to be accompanied by a greater susceptibility to hot carrier degradation in n-channel devices. Engineering of the structure of the n-channel devices is necessary to achieve stable operation over long periods of time. The p-channel transistors have not shown any significant hot carrier effects at normal biases and no special techniques are required in these devices.

The effect of hot carrier degradation can be substantially reduced by introducing a drain field relief structure such as gate overlapped LDD.\textsuperscript{[M Edwards 1995]} The importance of such a structure in n-channel devices fabricated by laser crystallisation has been demonstrated in life test measurements made on CMOS inverters. Inverters constructed using devices with a range of gate lengths and both with and without LDD in the NMOS devices have been tested. The inverters are operated at a fixed supply voltage with a square waveform of 100kHz applied to their inputs. While the inverters are being stressed there is no load applied to their outputs.

50
During the life test, the output drive capability of the inverters is measured periodically. This is done by applying a 330pF capacitor to the output of the inverter and recording the transient response of the circuit using a digital storage oscilloscope as illustrated in Figure 3-31. By differentiating the output voltage waveform, the drive current of the inverters can be determined as a function of the output voltage. This drive current represents the output characteristic of either the p-channel or n-channel device with the condition that the gate source voltage is equal to the supply voltage of the inverter. Examples of the drive current of an inverter which did not have LDD in the n-channel device, measured before and after stressing, are shown in Figure 3-32. The curves in which the output current increases with output voltage represent the current through the n-channel device while those which show a decrease of output current with voltage represent the current through the p-channel transistor.

![Figure 3-31 Circuit for measuring inverter drive capability](image)

![Figure 3-32 Output current of laser crystallised poly-Si inverter without LDD](image)
The change in the shape of the output characteristic of the n-channel transistor after 60500 minutes is characteristic of hot carrier degradation. Changes in the value of the output drive current at an output voltage equal to half of the supply voltage have been taken as a measure of the degradation of the device performance with time. Figure 3-33 shows the degradation of inverters with and without LDD and for a number of gate lengths. If LDD is not used then the inverters show severe degradation after only a few hours operation, even if relatively long channel lengths of 16μm are used. Inverters with LDD show negligible degradation after 3000 hours even when the device gate length is as short as 3μm.

![Graph showing degradation of inverters with and without LDD](image)

**Figure 3-33 Change in output drive current of n-type TFTs in CMOS inverters for an output voltage of 8V and a supply voltage of 16V**

### 3.8 Summary

A number of different techniques exist for fabricating low temperature poly-Si devices. The work reported in this thesis makes use of devices fabricated using two different processes, Solid Phase Crystallisation and laser crystallisation. The SPC devices are formed by converting an amorphous silicon film to polycrystalline silicon by heating in a furnace. The n-channel SPC devices exhibit acceptable electrical characteristics with
moderate values of mobility and threshold voltage, while the p-channel devices have relatively poor electrical characteristics, in particular a poor subthreshold slope which leads to very high values of threshold voltage. The p-type transistors also show a strong transient behaviour which is related to carrier trapping within the devices and represents a further complication in designing circuits using these transistors. While this transient behaviour has not been discussed in published work on TFT circuit design, it seems likely that the SPC poly-Si devices reported by others also exhibit such effects given the generally high values of threshold voltage reported for p-channel SPC poly-Si transistors.

The second process used for fabrication of low temperature poly-Si TFTs is laser crystallisation, in which a laser is used to melt an amorphous silicon film converting it to polycrystalline silicon. This results in much higher quality devices than the SPC process with high values of mobility, well matched n-channel and p-channel device characteristics and a substantial reduction of the transient behaviour observed for the SPC devices. The behaviour of laser crystallised poly-Si TFTs from the point of view of analogue circuit operation has not been reported previously. The measurements made on PRL devices indicate that useful levels of gain can be achieved using these transistors. More work is needed to investigate in more detail aspects such as device uniformity and noise performance, which are also of importance for analogue circuit design.

A consequence of the significant difference in transistor performance between these two low temperature processing methods is that work towards the industrialisation of low temperature poly-Si technology is now concentrated on laser crystallisation techniques. This is reflected in the large number of recent publications describing various aspects of laser crystallised poly-Si technology.
4 Digital and Analogue TFT Circuit Building Blocks

4.1 Introduction

Simple digital circuits form the major part of the addressing circuits for active matrix displays and have therefore been used to demonstrate the potential performance of circuits fabricated using PRL poly-Si transistors. Shift registers are used in both the row and column drive circuits of a display and inverters are used to supply the charging currents needed to address the rows of the display. The performance of these circuits is therefore an important measure of the quality of a TFT technology. Analogue TFT circuits, with the exception of simple analogue switches, have not yet been employed outside research activities. However, the ability to produce TFT amplifiers with reasonable levels of performance may in the future extend the range of circuits which can be integrated onto active matrix displays.

In this chapter published results on the performance of simple poly-Si TFT circuits are reviewed and then the performance of circuits fabricated using PRL devices is presented. Simple digital circuits have been fabricated using both the SPC and laser poly-Si technologies while simple analogue circuits have been fabricated using laser crystallised poly-Si TFTs.

4.2 Review of Poly-Si TFT Circuit Performance

Poly-Si TFT circuits, while not providing the levels of performance normally associated with modern crystalline silicon circuits, are quite adequate for the scanning functions required in active matrix displays. I-W Wu compared the performance of simple digital circuits fabricated using a number of processing techniques. Ring oscillator circuits fabricated with high temperature processing and using CMOS inverters with a TFT gate length of 10µm operated with propagation delays of 7ns per section at a supply voltage of 15V. Similar CMOS circuits fabricated with an SPC process resulted in delays of 49ns while for an NMOS circuit using ratioed logic the propagation delays were 110ns. Power delay product values for these three circuits were 24pJ, 22pJ and 182pJ respectively. CMOS dynamic shift registers fabricated using the high temperature and SPC processes had maximum clock frequencies of 22MHz and 4.7MHz respectively with a supply voltage of
15V. Circuits fabricated using a low temperature SPC poly-Si technology have also been reported by M Takabatake. In this case the maximum operating frequency of a CMOS dynamic shift register with a power supply voltage of 20V was 1.25MHz. The transistor gate length used in this circuit was 10μm.

There have been a number of research publications describing poly-Si TFT amplifiers fabricated using high temperature and low temperature SPC processes. Using high temperature poly-Si TFTs, a conventional design of two stage differential CMOS amplifier has been fabricated and a low frequency gain of 47dB has been obtained. More complex circuits have also been described including an amplifier having two gain stages and a complementary source follower output. This achieved a maximum gain of 80dB and was used to demonstrate a 4-bit TFT charge-redistribution digital to analogue converter. A simple two stage CMOS differential amplifier has also been fabricated using SPC poly-Si devices. This circuit achieved a low frequency gain in the range of 37-42dB depending on the bias conditions. The gate length of the devices was 15μm. A three stage amplifier consisting of a differential input followed by two further gain stages, one using a cascode load, achieved a maximum gain of 55dB.

4.3 Measurement of Simple Digital TFT Circuits

4.3.1 NMOS and CMOS Inverters

The basic element of digital circuits is the inverter. It not only provides inversion of a digital signal but also acts to restore the level of a signal which has been degraded by noise. This noise can arise from a number of sources such as coupling of clock signals, the effect of leakage currents degrading the voltage levels in a dynamic circuit or variations in the TFT characteristics changing the logic levels coming from previous circuit elements. Measurements of the DC transfer characteristics of an inverter indicate how well it can cope with noise present at its input as well as showing the logic levels it will generate at its output. The characteristics of two types of inverter, ratioed NMOS and CMOS, fabricated using SPC poly-Si TFTs have been measured. The inverter circuits are shown in Figure 4-1.
The ratioed NMOS inverter consists of a low resistance driver transistor, the gate of which is the input to the inverter, and a high resistance load transistor. The ratio of the W/L of the driver to that of the load, the beta ratio, determines both the low level output voltage of the inverter and the slope of the transition from high to low level, the gain. The inverters measured have a beta ratio of 15 and a gate length of 6μm. The DC characteristics of the inverters obtained at various supply voltages, with VGG=VDD, using devices both with and without threshold shifting channel implants are shown in Figure 4-2 and Figure 4-3.
Superimposed on each plot of the characteristic is a second plot, shown dashed, in which the input and output voltage axes are reversed. For a functional inverter the two curves will cross at three points. The two outer points represent the nominal voltage levels corresponding to high and low logic signals within a circuit made up of similar inverters. When there is only one crossing point on the characteristic the inverter no longer restores the level of the signal passing through it. The effect of this is that a signal passed through a chain of such inverters would fall in amplitude as it passed through each one and would eventually become lost in noise. The noise margins of the inverters have been evaluated using the method of maximum squares\[^\text{C Hill 1968}\] in which the noise margin is equal to the length of the side of the largest square that can be fitted within the loops of the inverter DC characteristics. The logic levels and noise margins for the NMOS inverters are summarised in Table 4-1.

<table>
<thead>
<tr>
<th>VDD / V</th>
<th>High Level / V</th>
<th>Low Level / V</th>
<th>Noise Margin / V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Transistors</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>3.6</td>
<td>0.5</td>
<td>0.1</td>
</tr>
<tr>
<td>16</td>
<td>9.3</td>
<td>1.0</td>
<td>0.5</td>
</tr>
<tr>
<td>Transistors with Threshold Shifting Implant</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>7.0</td>
<td>0.2</td>
<td>1.0</td>
</tr>
<tr>
<td>16</td>
<td>14.3</td>
<td>0.4</td>
<td>1.6</td>
</tr>
</tbody>
</table>

Table 4-1 SPC poly-Si ratioed NMOS inverter logic levels and noise margins

The characteristics of the inverter using normal transistors are poor compared to the circuit using transistors with the threshold shifting implants. The noise margin values are low indicating that the inverter is more susceptible to the effects of noise. The differences can be explained by the characteristics of the TFTs in the subthreshold region, Figure 3-4 and Figure 3-5 of chapter 3. In the inverter formed using normal devices, the high output voltage level is limited because when the gate source voltage of the driver transistor is zero a significant drain current still flows. This current flows through the load device resulting in an output voltage which is well below the level of the supply voltage. For the TFTs with the threshold shifting implants, the value of drain current for a gate source voltage of zero is at least two orders of magnitude lower. This results in a much smaller voltage drop across the load device of the inverter and therefore a higher output voltage level. There is relatively little difference in the values of the low logic levels of the circuits using normal and threshold shifted TFTs because when the output voltage is low both the load and driver transistors are turned on and neither device is operating in the subthreshold region.
The DC characteristics of the inverters indicate that the minimum operating voltage of the inverters lies between 4 and 6V for both circuits. Operating at 4V neither of the inverters provides restoration of the input signal due to the low slope of the inverter characteristics. This reflects the low gain, $g_m$, of the transistors when the gate bias is low. Although circuits using the normal TFTs will in principle operate with a supply voltage of 8V, the noise margins are extremely small and are likely to result in unreliable operation.

The CMOS inverters fabricated using the SPC poly-Si process have p-type and n-type transistors of different sizes. The p-type device is three times the width of the n-type device in order to compensate to some extent for the difference in the on state current of the p channel transistors compared to the n channel. DC characteristics of the CMOS inverters are shown in Figure 4-4 and Figure 4-5 for the cases in which both the n and p type transistors are either normal or have threshold modifying implants. The inverter parameters obtained from these characteristics are given in Table 4-2.

![Figure 4-4 CMOS inverter DC characteristics](image1)

![Figure 4-5 CMOS inverter DC characteristics, TFTs with threshold shifting implants](image2)

The inverter with normal TFTs was found to have a high output voltage level which was lower than the supply voltage, whereas the inverter using devices with threshold controlling implants produced a high level equal to the positive supply voltage. This difference is indicated more clearly in Figure 4-6 which shows the variation in the high level output voltage, measured with an input voltage of VSS, as a function of the supply voltage, VDD.
VDD / V | High Level / V | Low Level / V | Noise Margin / V
---|---|---|---
Normal Transistors
14 | 11.0 | 0.0 | 0.6
16 | 12.7 | 0.0 | 1.0
Transistors with Threshold Shifting Implant
4 | 4.0 | 0.0 | 0.9
8 | 8.0 | 0.0 | 2.4
16 | 16.0 | 0.0 | 3.8

Table 4-2 SPC poly-Si CMOS inverter logic levels and noise margins

In the case of the inverter using TFTs with threshold controlling implants, the high voltage level simply follows the supply voltage for voltages above 4V. However, for the circuit using normal TFTs, the high level voltage is almost zero until the supply voltage reaches 10V. It then rises sharply and tracks changes in the supply voltage although not reaching the same level as the supply voltage.

The cause of this behaviour is a combination of the high drain current of the normal n-type devices at a gate-source bias of 0V and the gradual turn on of the p-type devices with increasing gate bias. The transfer characteristics of Figure 3-4 in chapter 3 indicate that under DC conditions a gate voltage of approximately -10V to -12V is required on a p-type transistor in order to achieve the same current level as an n-type device of the same size with zero gate bias. The output voltage of the inverter is determined by the potential divider action of the p and n-type transistors. It is not until the supply voltage becomes greater than 10V that the conductance of the p-type transistor becomes greater than that of the n-type device allowing the high level of the output voltage to increase. In addition to the poor high level output voltage, the inverter using normal devices has a very low value.
of threshold voltage, that is the point at which the input voltage is equal to the output voltage. A consequence of this is that the noise margins for the inverter are low making it susceptible to noise on low level input signals. The characteristics of the inverter circuit fabricated using TFTs with threshold controlling implants are very much better due to both a reduction in the off state current in the n-type device and an increase in the on state current in the p-type device. The threshold voltage of the inverter is still not equal to the ideal value for a CMOS inverter of half the supply voltage reflecting the asymmetry in the device characteristics.

The inverter characteristics shown in this section represent measurements under steady state conditions where the currents flowing through the thin film transistors have been allowed to settle at their DC values. It was shown in section 3.5 that the TFTs fabricated using the SPC process, in particular the p-type devices, show strong transient behaviour due to carrier trapping effects. This means that under dynamic switching conditions the effective transfer characteristics of the inverters will differ from those measured under DC conditions. This complicates predictions of CMOS circuit performance since the inverter behaviour will be affected by the frequency and duty cycle with which it is switched.

The electrical characteristics of poly-Si devices fabricated using laser crystallisation are superior to those of SPC TFTs and CMOS inverters fabricated using these devices show improved performance compared to their SPC counterparts. The transfer characteristics of a laser crystallised poly-Si CMOS inverter are shown in Figure 4-7 and the parameters of the inverter are summarised in Table 4-3. The gate length of the transistors in the circuit is 6μm, the n-channel devices include LDD and the gate width of both p and n-channel devices is 10μm. The noise margins of this inverter are larger than those of the SPC circuit and the threshold voltage of the inverter is close to the ideal value of half the supply voltage.

<table>
<thead>
<tr>
<th>VDD / V</th>
<th>High Level / V</th>
<th>Low Level / V</th>
<th>Noise Margin / V</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>5.0</td>
<td>0.0</td>
<td>1.8</td>
</tr>
<tr>
<td>10</td>
<td>10.0</td>
<td>0.0</td>
<td>3.7</td>
</tr>
<tr>
<td>15</td>
<td>15.0</td>
<td>0.0</td>
<td>5.0</td>
</tr>
</tbody>
</table>

Table 4-3 Laser crystallised poly-Si CMOS inverter logic levels and noise margins
Figure 4-7 Laser crystallised poly-Si CMOS inverter characteristics, L=6μm

The effect of transistor gate length on the performance of the inverters is shown in Figure 4-8 and Figure 4-9. The noise margin of the inverters decrease as the TFT gate length is reduced. This reflects a reduction of the slope of the transition region of the inverter characteristics due to the lower output impedance, and therefore lower gain, of the shorter channel devices. This effect is clearest at the highest supply voltage, 15V, and is relatively small at a supply voltage of 5V. The threshold voltage of the inverters is largely independent of the device gate length.

Figure 4-8 Laser crystallised poly-Si CMOS inverter noise margins

Figure 4-9 Laser crystallised poly-Si CMOS inverter threshold voltage
4.3.2 NMOS and CMOS Shift Registers

Shift register circuits form an important element of most drive circuits for AMLCDs and their performance gives an indication of the switching speeds which can be expected from other digital circuits fabricated using thin film transistors. The performance of three conventional shift register circuit designs[^Elmsry 1981] has been investigated, namely a two phase ratioed NMOS register, a four phase ratioless NMOS register and a two phase dynamic CMOS circuit. The circuits were fabricated using SPC poly-Si transistors which received channel implants for threshold voltage control. A two phase static CMOS shift register has also been fabricated using laser crystallised poly-Si TFTs.

Figure 4-10 shows the circuit for a single section of the ratioed NMOS register. It uses ratioed NMOS inverters in which the width of the driver transistor is 15 times that of the load device. Static operation is achieved by the addition of feedback transistors from the output of one inverter to the input of the preceding inverter. An output is taken from each section in the register via a third inverter. The complete shift register consists of ten sections. Examples of the waveforms seen at the fifth and tenth outputs of the register are shown in Figure 4-11 together with the test signal applied to the input and the clock c1. The operating conditions were a power supply voltage of 16V and a clock frequency of 400kHz.

The ratioless shift register, illustrated in Figure 4-12, uses transistors of a single size which are controlled by four clock signals. The output waveforms from this circuit are quite different from those of the other two shift registers because they are generated by a ratioless output circuit. This only produces a high output voltage when the clock cl and the signal from the shift register are at a high level. Ratioless NMOS circuits produce output signals which are only valid during certain parts of each clock period because they work by pre-charging the capacitance at their outputs and while this pre-charging is taking place the output voltage is not at a valid level. A consequence of this is that ratioless circuits are more difficult to design than ratioed circuits. A circuit made up of five register sections has been measured and the waveform at the fifth output of the register, the complement of the register input signal and the clock cl are shown in Figure 4-13. Operating conditions are a clock amplitude of 16V and clock frequency of 1MHz.

![Figure 4-12 Ratioless NMOS shift register](image1)

![Figure 4-13 Ratioless NMOS shift register waveforms](image2)

The third circuit is a dynamic CMOS register, shown in Figure 4-14. The widths of the p-type transistors in the circuit are approximately three times those of the n-type devices, in order to compensate to some extent for the lower currents from the p-channel devices. An
output is provided from each section of the register via an inverter. The CMOS test circuit consists of ten stages and waveforms appearing at the fifth and tenth outputs are shown in Figure 4-15 for a supply voltage of 16V and clock frequency of 1MHz.

![Figure 4-14 Dynamic CMOS shift register](image1)

![Figure 4-15 CMOS shift register waveforms](image2)

The maximum clock frequency of the shift registers is of particular importance for the column drive circuits of an active matrix display. Figure 4-16 shows how the maximum clock frequency of the three circuits varies as a function of operating voltage. This has been measured by observing the waveform at the last output of each of the registers using a low capacitance, 0.02pF, probe. The maximum frequency is defined as the clock frequency at which the carry input test signal is no longer transferred correctly to the final output.

The ratioless NMOS and CMOS circuits operate at frequencies approximately 2-5 times higher than the ratioed NMOS register, depending on the operating voltage. The relatively low speed of the ratioed NMOS circuit is due in part to the higher input capacitance of the ratioed inverter, calculated to be approximately 0.2pF compared to 0.06pF for the CMOS inverter and 0.01pF for the ratioless NMOS inverter. To obtain the best performance from the circuits in terms of operating frequency it is desirable to run the circuits with high supply voltages. However, for long term stable operation of the circuits the supply voltages must be limited. For circuits using SPC poly-Si TFTs with a gate length of 6μm, operation at supply voltages in excess of 16V can result in degradation of the transistors due to hot carrier effects.
A second consideration in the performance of the shift registers is the power consumption. A high power consumption is undesirable since it makes layout of the power lines in the circuit more critical and in extreme cases may result in excessive heating of the circuits. The variation of the power consumption/section of the shift registers as a function of clock frequency is shown in Figure 4-17 for operation at 16V.

The power requirement is highest for the ratioed NMOS circuit, the level being consistent with the current which flows in the ratioed inverters when they have a low output state and when both the driver and load transistors are conducting. The ratioless circuit uses an order of magnitude less power than the ratioed design. The value is again consistent with the currents which flow through the inverters when their output state is low although in this case the source of the current is the clock lines c3 and c4. The lower power in the ratioless circuit is due to the smaller size of the transistors and the fact that the load transistors are only turned on for a part of each clock period. In principle the power consumption can be reduced further by replacing the ground line with connections to the clocks c3 and c4 therefore eliminating the direct current path to ground within the inverters.

As would be expected the power taken by the CMOS circuit is proportional to the clock frequency since it is dominated by the current needed to charge and discharge the
capacitances within the circuit. At high frequencies the power of the CMOS circuit approaches that of the ratioless register, being only a factor of two lower at a clock frequency of 1MHz.

A figure of merit which is often used for digital circuits is the power delay product. A low value of power delay product is desirable since this implies that the circuit has both a low power requirement and high speed capability. The power delay product of the three shift registers has been estimated by considering the power consumption and maximum clock frequency at an operating voltage of 16V. The inverter delay is assumed to be equal to half the period of the maximum clock frequency while the figure for power consumption of the circuit is divided by the number of inverters. The results summarised in Table 4-4 illustrate the advantage of the CMOS and ratioless NMOS circuits compared to the ratioed NMOS.

<table>
<thead>
<tr>
<th>Ratioed NMOS</th>
<th>Ratioless NMOS</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 pJ/inverter</td>
<td>6.5 pJ/inverter</td>
<td>2.2 pJ/inverter</td>
</tr>
</tbody>
</table>

Table 4-4 Power delay product figures for SPC poly-Si shift register

Considering the properties of these three different shift register circuits, ratioed NMOS circuits look unattractive for display drive circuits because of their high power consumption and lower operating frequency. A comparable performance can be achieved from CMOS and ratioless NMOS circuits. However, as has already been suggested, there are a number of reasons why designing ratioless NMOS circuits is more difficult than CMOS. The outputs from a ratioless shift register are only valid during certain parts of the clock cycle complicating the interface of the register to other circuits such as output buffers. As in ratioed NMOS circuits, the output voltage of the ratioless register is limited by threshold voltage losses whereas the CMOS circuit will provide an output voltage equal to the supply voltage. Finally ratioless circuits are by nature dynamic circuits with the digital information being stored on the capacitances within the circuit. This makes them more vulnerable to noise and requires careful design of circuits operating at low frequencies. Despite these problems an advantage of the NMOS circuit, particularly for the active matrix display application, is the simpler processing which is possible. Compared to a CMOS process the number of mask steps can be reduced by two and the number of implant steps by one.

CMOS shift register circuits have also been fabricated using laser crystallised poly-Si devices. The shift register circuit is a static design illustrated in Figure 4-18. The complete
circuit is made up of 11 of the sections illustrated and the complementary output from the last section is fed back to the carry input to form a Johnson Counter.

The maximum operating frequency of circuits which use transistors having three different gate lengths is shown in Figure 4-19. The maximum clock frequency has been determined by operating the circuit as a divide by 22 Johnson counter and increasing the clock frequency until the frequency at the output of the circuit is no longer 1/22 of the clock frequency. The circuits can be operated at lower supply voltages than the SPC shift registers due to the lower threshold voltages of both the p-type and n-type laser crystallised poly-Si TFTs. Unlike the SPC devices the laser crystallised transistors do not have a self aligned gate structure and this results in an increase in the gate capacitance of the devices by a factor of two or more. Despite this the maximum clock frequency of the circuits is higher than the SPC registers due to the seven fold increase in the device field effect mobility. Direct comparison of the laser crystallised and SPC circuits is difficult due to the differences in design. However, the performance advantage of the laser crystallised devices is evident by comparing Figure 4-19 with Figure 4-16.

![Diagram of CMOS static shift register]

Figure 4-18 CMOS static shift register

The power delay product of the laser crystallised poly-Si circuits is shown in Figure 4-20. This has been calculated by measuring the average power consumption of the Johnson Counter when operating at the maximum clock frequency and taking the delay value as half of the reciprocal of the clock frequency. The power delay product increases with gate length.
because the increasing gate length reduces the device current and increases the gate capacitance. The increase is smaller than might be expected due to the significant overlap capacitance of the laser crystallised TFTs which is independent of channel length.

![Graph](image1)

![Graph](image2)

**Figure 4-19 Laser crystallised poly-Si CMOS shift register**

**Figure 4-20 CMOS shift register power-delay performance**

### 4.4 Measurement of Simple Analogue TFT Circuits

Two groups of analogue circuits which are of particular interest for large area electronics application, including AMLCDs, are analogue switches, or transmission gates, and analogue amplifiers. Analogue switches are a vital component in most designs of column drive circuit for AMLCDs. They are also fundamental to the operation of an AMLCD since in effect the transistor within each pixel of the display is acting as an analogue switch which is turned on to address the pixel and turned off to maintain the pixel voltage throughout the field period. In column drive circuits the switches are used within a multiplexer to sequentially select groups of columns and charge them to the appropriate video drive levels. The issues concerning the design of analogue switches for use in column drive circuits are addressed in section 5.4.4 and will therefore not be discussed further here.
The range of analogue signal processing which could be carried out using TFTs would be limited if it were not possible to buffer and amplify analogue signals. The analogue circuit environment is more demanding of TFT characteristics than the digital circuits described so far. In the remaining sections of this chapter the performance of simple CMOS amplifiers fabricated using laser crystallised poly-Si TFTs is described.

4.4.1 Two Stage CMOS Differential Amplifier

A number of simple two stage CMOS differential amplifiers have been measured to provide an indication of the open loop gain which can be achieved using laser crystallised poly-Si TFTs. The circuit is illustrated in Figure 4-21. Circuits using TFTs having a range of gate lengths from 6μm to 20μm have been fabricated.

![Two stage CMOS differential amplifier](image)

Figure 4-21 Two stage CMOS differential amplifier

The frequency response of a circuit having TFTs with a gate length of 15μm is shown in Figure 4-22. The power supply voltages were set at +10V and -10V and the bias voltage was set at -4.1V, resulting in a bias current for the input stage of 10μA. The load capacitance at the output of the amplifier was approximately 10pF. The low frequency gain of the amplifier is more than 60dB and the unity gain frequency approximately 500kHz, levels of performance which in principle would allow the design of amplifiers for use in column drive circuits. The low frequency gain is higher than that achieved for similar circuits fabricated using high temperature and SPC poly-Si devices. [A. Lewis 1988] [H-G Yang 1993]
Figure 4-22 Frequency response of CMOS differential amplifier $L=15\mu m$

The effect of TFT gate length on the low frequency gain is illustrated in Figure 4-23. When the circuits are operated with an input stage bias current of $50\mu A$ the circuits show an approximately linear dependence of the gain on the gate length. As would be expected, as the gate length is increased the gain also increases due to the higher output resistance of the devices. The gain of the circuits also depends on the bias current of the amplifiers. As the bias current is reduced the gain increases reaching a maximum value when the TFTs are biased close to or just below threshold. Figure 4-23 illustrates the increased gain which can be achieved by setting the bias current to $0.5\mu A$, such that the TFTs are operating in the subthreshold region. This behaviour is consistent with that of conventional MOS devices which also exhibit maximum gain when operated close to threshold. [P Gray 1982]
4.4.2 Single Stage CMOS Differential Amplifier

The most obvious use for amplifiers within AMLCD column drive circuits is to provide buffering of the analogue output signals. This would allow sample and hold circuits to be used for sampling the video drive signal rather than the current approach where the signal is sampled directly onto the columns of the display. Such an amplifier would normally be used with a gain of one and would be required to drive the relatively large capacitance of the columns of the display. One possible candidate for such an amplifier is the CMOS circuit shown in Figure 4-24. This design has the advantage that it achieves an acceptable open loop gain without requiring frequency compensation for stable unity gain operation.

The gate length of the transistors was fixed at 15μm. The bias current of the output stage was chosen on the basis of the slew rate of the output signal when driving a capacitive load of 20pF. The width of the output devices was then determined from consideration of the required output voltage range, chosen as 6V, and the need to maintain the output devices in saturation given a power supply voltage of 18V. The bias current of the input section was chosen to be 10μA and the input transistor width set to give an open loop gain of approximately 2000.
A limited number of measurements have been carried out on the circuit. The power supply voltages were set at \( V_{DD} = 9.5V \) and \( V_{SS} = -8.5V \). \( V_{bias} \) was adjusted to set the bias current of the input stage to 10\( \mu \)A and bias voltages of \( V_{BN} = 0.5V \) and \( V_{BP} = -1.0V \) were used. Low frequency gain and offset voltage measurements were made on a number of circuits located within an area of approximately 10mm by 10mm on the glass substrate. Large variations in both the gain and offset voltage were found, as indicated in Table 4-5.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Low Frequency Gain</th>
<th>Offset Voltage (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>914</td>
<td>-43</td>
</tr>
<tr>
<td>2</td>
<td>971</td>
<td>-119</td>
</tr>
<tr>
<td>3</td>
<td>1424</td>
<td>-139</td>
</tr>
<tr>
<td>4</td>
<td>1240</td>
<td>+66</td>
</tr>
<tr>
<td>5</td>
<td>2055</td>
<td>+17</td>
</tr>
<tr>
<td>6</td>
<td>1516</td>
<td>-69</td>
</tr>
<tr>
<td>7</td>
<td>1774</td>
<td>+210</td>
</tr>
<tr>
<td>8</td>
<td>1619</td>
<td>-105</td>
</tr>
<tr>
<td>9</td>
<td>853</td>
<td>-129</td>
</tr>
</tbody>
</table>

Table 4-5 Gain and offset voltage variation
The frequency response of a circuit having average gain was measured and the results are shown in Figure 4-25. The load capacitance during the measurement was 20pF which is typical of the column capacitance of a 4-6 inch diagonal AMLC display. The gain of the circuit falls to 3dB below its maximum value at a frequency of 100Hz and then decreases at a rate of 20dB/decade resulting in a unity gain bandwidth of approximately 160kHz.

![Figure 4-25 Open loop frequency response with 20pF load](image)

The transient performance of the circuit with the inverting input connected to the output is shown in Figure 4-26. The input signal was a square waveform with an amplitude of either 0.5V or 5V. The slew rate of the amplifier is approximately 1V/μs and is consistent with the bias current in the output stage of 20μA. The total power supply current of the amplifier was 50μA.

4.5 Summary

In the early stages of research into SPC poly-Si devices at PRL it was believed that NMOS circuit design would be necessary because of the poor DC characteristics of the p-channel devices. Ratioless NMOS row and column drive circuits were developed as these offered lower power consumption than ratioed NMOS designs.
From measurements of shift register circuits it was found that in practice the performance of the CMOS circuits does not reflect the DC characteristics of the p-channel TFTs due to their pronounced transient behaviour. The laser crystallised poly-Si TFTs are superior to the SPC devices in all respects except that the devices used in this work are not self aligned devices and therefore have additional gate-drain overlap capacitance. Despite this, the improved mobility achieved with laser crystallisation means that the operating speed of the circuits is higher than those using SPC transistors. The ability to produce well matched p-channel and n-channel TFT has meant that CMOS technology is preferred over NMOS due to its greater tolerance to variations in the TFT characteristics and the greater flexibility that it offers to the circuit designer.

Simple analogue circuits have been demonstrated using the laser crystallised devices, such circuits have not previously been reported using laser crystallised poly-Si. The levels of performance which can be achieved in terms of gain and frequency response are consistent with the requirements of signal buffering operations which might be implemented within the column drive circuit of a display. The uniformity of the devices appears to be an important issue for these poly-Si TFT amplifier circuits as significant localised variations in circuit performance have been observed. Laser crystallisation is currently a very immature technology and more work is required to investigate the causes of the variations in circuit performance before such circuits could be employed in the drive circuits for active matrix displays.
5 TFT Drive Circuits for AMLCDs

5.1 Introduction

The target which is driving the development of low temperature poly-Si TFT technology is the possibility of replacing the conventional crystalline silicon drive circuits which are currently used to address most active matrix LC displays with circuits integrated onto the display substrate using TFTs. Drive circuit integration using high temperature poly-Si TFTs is well established for small displays used in projection and viewfinder applications. However, low temperature poly-Si technology and the design of integrated drive circuits for larger displays is at a much earlier stage of development and is currently the subject of much research activity. The design of TFT drive circuits requires a different approach to that used in drive circuits fabricated with conventional silicon technologies. The lower performance of the TFTs, the use of relatively coarse design rules and the importance of achieving a high circuit yield mean that integrated drive circuit designs are generally much simpler in their operation than their crystalline silicon counterparts.

The use of poly-Si TFTs for the integration of the drive circuits of an AMLCD was reported as long ago as 1984 when Morozumi et al. described a small 180x210 pixel 1.51-inch diagonal display with integrated row and column drive circuits.\cite{Morozumi1984} The row drive circuit consisted of a shift register and the column drive circuit of a shift register controlling sampling switches. Since that time the fundamental operation of most poly-Si TFT drive circuits has remained largely unchanged. The details of the designs have developed as understanding of the display and circuit operation and the device performance has improved.

In 1994 level shifting circuits were implemented at the clock inputs of drive circuits so that the display could be operated with 5V control signals while the TFT circuits operated with a power supply voltage of 12V.\cite{Maekawa1994} In the same paper a shift register was presented which reduces the loading on the clock lines of the circuit. The use of a circuit to pre-charge the columns of the display for improved image uniformity was also described. In 1995 a display in which the shift registers of the row and column drive circuits operated with a power supply voltage of only 5V were described.\cite{Higashi1995} This was possible due to the low threshold voltage of the TFTs and it also meant that 5V signals could be used to control the display. The outputs of the shift registers were level
shifted to 12V to provide the higher voltages needed to address the display. In 1996 a column drive circuit in which the shift register was divided into a number of sections was described.\cite{Kobayashi1996} By applying clock signals to the individual blocks only when they were passing a carry pulse the power consumption of the shift register could be reduced.

A number of circuit designs have been published which depart from the mainstream analogue multiplexing approach. A four level digital column driver fabricated using NMOS devices was described by Ohwada et al. in 1989. The analogue column voltages were selected by one of four switches making it difficult to increase the greyscale resolution of the display without a large increase in circuit complexity.\cite{Ohwada1989} In 1990 a column drive circuit using a 5-bit digital to analogue converter for each column based on a switched ramp technique was described.\cite{Stewart1990} The success of this circuit has not been clearly demonstrated and it may be that it was too complex for the SPC poly-Si technology being used. More recently a 6-bit digital column drive circuit has been demonstrated \cite{Inoue1995,Matsumura1996} using laser crystallised poly-Si devices. This circuit also uses one digital to analogue converter for each column but in this case a converter using binary weighted capacitors is used. Towards the end of 1997 the first poly-Si column drive circuit to implement an analogue buffer amplifier was described.\cite{Seike1997} A key feature of this design is the use of external circuitry to correct for the offset voltage non-uniformities of the TFT amplifiers. The extended column charging times offered by this drive circuit are important for high resolution and large sized displays.

In this chapter the design of simple TFT drive circuits for active matrix displays is examined. In the first section the drive requirements of AMLCDs are reviewed and then the design of row drive circuits and column drive circuits based on the analogue multiplexing approach is presented. An important aspect of this work is consideration of the implications for the design of these circuits of the larger display sizes which are becoming possible using low temperature poly-Si technology. An example of a prototype display with integrated TFT drive circuits is presented at the end of the chapter.

### 5.2 Drive Requirements of TFT Active Matrix LC Displays

The basic operation of active matrix liquid crystal displays was described in chapter 2. In this section the drive requirements of the display will be examined in more detail with particular reference to those aspects which influence the design of the display drive circuits.
An electrical equivalent circuit for the pixels in a display is shown in Figure 5-1. The pixel capacitance is made up of the liquid crystal capacitance $C_{LC}$ and a separate storage capacitor $C_S$. The effect of the storage capacitor is to increase the value of the pixel capacitance bringing a number of advantages. It reduces the effect of leakage current through the TFT or the liquid crystal, it reduces the effect of parasitic capacitances within the pixel and improves the pixels dynamic performance by reducing the effect of changes in the liquid crystal capacitance. The storage capacitor can either be connected to a separate storage capacitor electrode, as shown on the left of Figure 5-1, or connected to the row electrode of an adjacent pixel, as illustrated on the right of the figure. Using the row electrode has the advantage that it results in a more efficient pixel layout which offers a higher aperture. The disadvantage of connecting the storage capacitor to the adjacent row electrode is that the current required to charge all of the storage capacitors in the row must be supplied via the row electrode. If the resistance of the row electrode or the output resistance of the row drive circuit is too large then horizontal crosstalk may become apparent in the displayed images.

The drive voltage requirements of an AMLCD are determined largely by the electrical characteristics of the pixel TFTs and the electro-optical characteristics of the liquid crystal. In general terms, the column drive waveforms are matched to the electro-optical characteristics of the LC while the row voltage waveforms are designed to provide adequate switching of the pixel transistors. The characteristic of a typical TN LC cell using crossed polarisers is shown in Figure 5-2. The rms drive voltage applied to the liquid crystal determines the transmission of each pixel. In this example the LC has a threshold voltage, $V_{th}$, of approximately $1.4V_{rms}$, and a saturation voltage, $V_{sat}$, of $4V_{rms}$.
The non-linear form of the transmission-voltage characteristic of the display must be taken into account if uniform grey scale reproduction is required. It may be necessary to gamma correct the video signal before it is applied to the display. In television systems the transmitted video signal is matched to the characteristics of a CRT which has a power law dependence of screen brightness on signal voltage. If a television signal is used to drive an AMLCD without gamma correction then the grey levels in light and dark areas of the picture become compressed degrading the image quality.

The basic addressing waveforms for a pixel in an active matrix display are illustrated in Figure 5-3. The pixel is addressed by first setting the column voltage at the appropriate value lying between $+V_{th}$ and $+V_{sat}$. The voltage on the row electrode is then taken to the select level which turns on the TFT and allows the pixel capacitance to charge to the column voltage. Once the pixel has charged the TFT is turned off by returning the row voltage to the non-select level. This isolates the pixel from the column and the voltage across the LC is maintained by the pixel capacitance until the pixel is addressed again in the following video field period. The polarity of the voltage applied to the pixel must be inverted each time that the pixel is addressed and this is achieved by inverting the polarity of the column addressing waveform.
The maximum column drive voltage needed to address the display is equal to twice the saturation voltage of the liquid crystal, $2V_{\text{sat}}$. The level of the row select and non-select voltages are determined by the switching behaviour of the pixel TFT. The non-select voltage must be set at a level which is sufficiently low to ensure that the pixel TFT remains in a non-conducting state for all possible values of the column voltage and pixel voltage. The row select voltage must be set at a level which is sufficiently high that the TFT is able to charge the pixel capacitance within the available charging time for all possible values of column voltage.

It is possible to reduce the drive voltage required by the columns of the display if part of the LC drive voltage is applied to the common electrode of the display. Implementation of this technique is illustrated in Figure 5-4. In the case of displays which have a separate pixel storage capacitor line the additional voltage waveform is applied to both the common electrode and the capacitor electrodes of the display. If the display has pixel storage capacitors which are connected to the adjacent row electrode then it is necessary to modulate the non-select output level of the row drivers with the same signal that is applied to the common electrode. If this was not done then the additional voltage applied to the common electrode would be reduced by the potential divider action of the LC and pixel storage capacitors. Modulating the common electrode of the display in this way allows the column voltage range to be reduced from a peak to peak value of $2V_{\text{sat}}$ to only $(V_{\text{sat}}-V_{\text{th}})$. For the LC characteristics shown in Figure 5-2 this represents a reduction from 8V to 2.6V.
An important consideration in the design of the column drive circuits is the required accuracy of the output voltage waveforms. The column voltage directly determines the brightness of the pixels in the display and therefore errors in the column voltage are translated into errors in the brightness of displayed images. In most cases an error in the output voltage of the column drive circuit will be applied to all pixels in that column of the display. The human visual system is particularly sensitive to regular structures and any lines or blocks of pixels with slightly different brightness will be highly visible. The maximum slope of the LC transmission characteristic gives an indication of the accuracy required for the signals used to address the columns of the display. For the characteristic shown in Figure 5-2, at the point of maximum slope the transmission changes by 1% for every 10mV change in the applied rms voltage. Transmission differences as low as 1% can be quite visible on a display and therefore the column driver rms output voltage accuracy should be better than 10mV. In practice gradual variations in brightness over a display are not easily detected by the eye and it is appropriate to specify two figures for voltage accuracy. The voltage error between two adjacent column drive outputs should be less than 10mV while the voltage error between any two columns on the display should be less than 100mV.

Errors in the mean level of the column drive waveforms can also be a source of display non-uniformity. The transmission of the pixel is relatively insensitive to changes in the dc voltage applied to it. This dc voltage is normally adjusted to zero by changing the mean level of the voltage applied to the common electrode of the display. If the dc voltage becomes too large then problems such as low frequency flickering, non-uniformity, image retention and
degradation of the LC material can result. To avoid these problems variations in the mean column voltage should be less than ±100mV for any two columns in the display.

The accuracy of the row drive circuit output voltages is not generally an issue for TFT AMLCDs since the row voltage simply controls the switching of the pixel TFTs. As long as the select voltage is high enough to turn the TFT on and the non-select voltage is low enough to turn the transistor off the correct voltage will be established on the pixel. A qualification to this statement is that when the pixel storage capacitors are connected to the adjacent row electrode any change in the row potential after the pixel has been charged and the pixel transistor turns off will be coupled onto the pixel via the storage capacitor and will alter its transmission.

It has already been indicated that the drive voltage applied to the pixels must be inverted periodically. In fact there are four different schemes for performing this inversion which are known as field inversion, row inversion, column inversion and pixel inversion. The difference between these methods is illustrated in Figure 5-5 which shows the polarity of the voltages applied to pixels in the display in odd and even field periods.

![Figure 5-5 TFT AMLCD drive polarity inversion schemes](image-url)
Field inversion is the method that was first used to address active matrix LC displays. In this scheme the polarity of the column signals is inverted at the end of each field of the video signal, as illustrated in Figure 5-3. Field inversion is not normally used today because with this drive scheme leakage currents through the pixel transistor or the liquid crystal results in non-uniformity, vertical crosstalk and large area low frequency flicker in the displayed images.

In row inversion the polarity of the column voltage is alternated after each row of pixels has been addressed in addition to the polarity change at the end of each video field. In this way alternate rows of pixels in the display are addressed with opposite polarity signals. This drive scheme is very effective at reducing the problems of non-uniformity, crosstalk and large area flicker associated with field inversion. The large area flicker is replaced by interline flicker which is much less visible and the non-uniformity and vertical crosstalk are replaced by a reduction in the peak contrast of the displayed image.

In column inversion the waveform appearing on an individual column of the display is the same as in field inversion, the column polarity inverts at the end of each field. However, alternate columns in the display are addressed with opposite polarity signals. This method removes the large area flicker associated with field inversion but does not reduce the non-uniformity or the crosstalk. Its main advantage is that the currents which flow in the common electrode and the row electrode or storage capacitor electrode as the pixels are charged are significantly reduced. This is because alternate pixels in the row are being charged with voltages of opposite polarity. Some charge can be transferred directly from a pixel to its neighbour reducing the maximum current flowing in the electrodes.

Pixel inversion is the inversion scheme which has the potential to provide the highest image quality. It combines the techniques of row inversion and column inversion so that alternate rows and columns in the display are addressed with signals of opposite polarity. This drive scheme brings the advantages of both line inversion and column inversion resulting in the lowest levels of crosstalk and low frequency flicker of the four schemes. A limitation of pixel inversion and column inversion is that it is not possible to use modulation of the voltage applied to the common electrode to reduce the amplitude of the column drive waveforms. This is because in these two inversion schemes pixels receiving both positive and negative drive voltages are addressed simultaneously and it is not possible to apply signals of opposite polarity to the pixels via the common electrode of the display.
Colour direct view active matrix displays are made by integrating a mosaic colour filter onto the passive glass plate of the display. Each pixel in the display becomes associated with one of the three primary colours and must be addressed with the appropriate colour video information by the column drive circuit. The most common colour filter arrangement used in displays intended for TV images is the staggered arrangement while for datagraphic applications a vertical stripe filter layout is used. These filter arrangements are illustrated in Figure 5-6. The staggered arrangement requires the video signal applied to the columns to be switched between two of the colours as successive rows are addressed. With the vertical stripe arrangement each column is associated with a single colour signal.

![Staggered Colour Filter Arrangement](image)

![Striped Colour Filter Arrangement](image)

Television signals and some data graphic video sources provide the video information in an interlaced format. In an interlaced video signal only half of the picture information is transmitted within each field period. In the even fields information is transmitted for the even numbered lines in the picture while in the odd field information is transmitted for the
odd numbered lines. If an active matrix LC display is addressed in an interlaced fashion so
that only half of the rows of pixels are addressed in any field then disturbing artefacts are
produced on moving images. The light output of the screen of a CRT decays rapidly after the
scanning electron beam has passed. In an AMLCD the capacitance of the pixel maintains the
voltage across the LC after it has been addressed resulting in an almost constant light output.
This causes artefacts in moving images when interlaced addressing is used as picture
information from two successive fields will be present on the display at the same time. This
problem can be avoided by using a sequential drive scheme in which each line of the video
signal is used to address two rows of pixels in the display. [A Kapp 1989]

An important characteristic of active matrix LC displays is that they are generally designed
to operate with only one video standard. This is because the number of pixels in the display
is fixed and must be matched to the resolution of the video signal to be displayed. In contrast
to this the CRT does not have a fixed pixel structure and can accommodate a wide range of
signal standards simply by altering the timing of the horizontal and vertical scanning of the
electron beam.

The row addressing frequency of an active matrix display is linked to the line frequency of
the video signal. If the signal is an interlaced one then the row addressing frequency is twice
the line frequency, if the signal is non-interlaced then the row and line frequencies are equal.
The operating frequency of the column drive circuits is related to the active line time of the
video signal and the number of columns in the display. For television signals the rate at
which the video signal is sampled by the column drive circuits is determined by dividing the
number of columns in the display by the active line time of the video signal. For example a
display having 720 columns operating with a PAL video signal having an active line time of
52μs would have a video sampling rate of 13.8MHz. For datagraphic displays there is a one
to one relationship between the pixels generated by the signal source and the pixels in the
display therefore the sampling of the column drive circuit must be linked to the pixel clock
of the video source. The time which is available to charge the pixels in the display depends
on the operation of the column drive circuit. Where the column driver charges all columns
simultaneously, the technique used with conventional column drive circuits, almost the full
video line period will be available for the pixel voltage to settle. Where the columns are
charged sequentially, as in the TFT column drive circuit described later in this chapter, the
pixel settling time is a fraction of the video line blanking period.
5.3 Design of Poly-Si TFT Row Drive Circuits

The function of the row drive circuits of an active matrix LC display is to select each row electrode in turn as the corresponding video data is applied to the columns of the display by the column drive circuit. The row drive circuit operates at the line frequency of the video signal and is therefore relatively undemanding of transistor performance.

The selection of successive rows is normally performed by a static shift register as shown in Figure 5-7. A bi-directional shift register is often used allowing the scan direction of the display to be reversed. Outputs are usually taken from both master and slave sections of the shift register as this reduces the number of shift register sections required. A consequence of this is that successive shift register output pulses overlap by half the clock period. Non-overlapping pulses are required to address the rows of the display and one method of generating these is to use NAND gates as shown in Figure 5-7. The shift register is normally designed using minimum size transistors. Therefore a chain of inverters of increasing size is needed to drive the relatively large row capacitance of the display.\cite{Mohsen1979} A number of shift register designs which have been used in row and column drive circuits are described in section 5.4.6.

An alternative to the use of a shift register for selecting the rows of a display is an address bus and decoders\cite{Harada1994} as shown in Figure 5-8. An advantage of this arrangement is that it does not rely on the propagation of a signal through a TFT circuit to select the successive outputs. A defect in a shift register is likely to prevent all succeeding stages from addressing the display correctly. With the decoder arrangement a defect in one of the
decoders, once isolated, is unlikely to affect other parts of the circuit making this design more tolerant of defects. A disadvantage of a drive circuit based on decoders is the area required to accommodate the address bus lines and the relatively complex decoder logic. For example a VGA resolution display with 480 rows would require a 9-bit address bus and 9-bit decoding logic. This approach for generating scanning signals has not been widely used.

![Diagram of row drive circuit using a decoder](image)

**Figure 5-8 Row drive circuit using a decoder**

In some TFT row and column drive circuit designs level shifting stages are introduced between the shift register or decoder and the output stages of the circuit. The output section of the circuits must be operated at the relatively high voltages required to address the display but by introducing level shifters the shift registers or decoders can be operated at a lower voltage. There are a number of circumstances where it may be necessary to consider the use of level shifters. Takafuli found it necessary to use dual gate transistors in the output stages of the circuits because of the relatively high bias voltages. Introducing level shifters between the output circuits and the shift registers allows single gate transistors to be used in the remainder of the circuit. Higashi makes use of level shifters to overcome a problem encountered with improving TFT performance. It was found that as the operating voltage of a shift register was increased, the sensitivity of the circuit to mistiming of the complementary clock signals, clock skew, also increased. Reducing the power supply voltage of the shift registers resulted in more reliable circuit operation and reduced power consumption. These advantages have to be balanced against the additional complexity of the level shifting circuits and the increased propagation delays which result from operating the circuits at lower power supply voltages.
Determining the size of the transistors in the inverters which form the output of the row drive circuit is an important aspect of the circuit design. These transistors must charge and discharge the row capacitance with acceptable rise and fall times. The equation below, which is derived in appendix A, can be used to estimate the 10%-90% or 90%-10% transition times of the signal at the output of a CMOS inverter.

\[
T_{ch} = C \left( \frac{-2(V_{DD} - |V_T| - 0.9V_{DD})}{(V_{DD} - |V_T|)^2} + \frac{1}{(V_{DD} - |V_T|)} \log \left( \frac{2(V_{DD} - |V_T|)}{0.1V_{DD} - 1} \right) \right)
\]  

where \( C \) is the load capacitance, \( V_{DD} \) is the power supply voltage, \( V_T \) is the transistor threshold voltage, \( B = \frac{W}{L} \) and \( C_{ox} = \frac{e_{ox}}{t_{ox}} \).

Rearranging this equation results in the transistor width required to achieve a certain transition time.

\[
W = \frac{CL}{C_{ox} \mu T_{ch}} \left( \frac{-2(V_{DD} - |V_T| - 0.9V_{DD})}{(V_{DD} - |V_T|)^2} + \frac{1}{(V_{DD} - |V_T|)} \log \left( \frac{2(V_{DD} - |V_T|)}{0.1V_{DD} - 1} \right) \right)
\]

Substituting values for the various parameters, power supply voltage \( V_{DD}=16 \) V, mobility \( \mu_p=80 \) cm²/Vs, \( \mu_n=100 \) cm²/Vs, threshold voltage \( V_{pth}=-5 \) V \( V_{nth}=5 \) V, gate capacitance \( C_{ox}=2.3 \times 10^{-4} \) F/m², gate length \( L_p=6 \) μm and \( L_n=6 \) μm.

\[
W_p = \frac{0.846C_{sw}}{T_{90\%-90\%}}
\]

\[
W_n = \frac{0.677C_{sw}}{T_{90\%-10\%}}
\]

Considering the charging of the pixels, it is important that the pixel TFTs are turned off before the voltages on the columns start to change to the new values required for the next row of pixels. A typical value for the 90%-10% fall time would be 2 μs, which ensures that the pixel TFTs can be turned off within the line blanking period of the video signal. To achieve this value of fall time the n-channel device in the output inverter should have a width of approximately 34 μm for each 100 pF of load capacitance. The rise time of the row select pulses is less critical than the fall time and it is often convenient to make the width of the p-channel device the same as the n-channel transistor.
The row capacitance of displays of different resolutions and sizes has been estimated in appendix B and the results are illustrated in Figure 5-9. It is assumed in these calculations that the pixel storage capacitors are connected to the adjacent row electrodes. As the display size increases the row capacitance also increases and therefore larger transistors are required in the output section of the row drive circuit. There is not an absolute limit on size of transistors which can be used in the drive circuits, but as their size increases the drive circuits will have a greater effect on the yield of the display. While considering what is a practical size for the output TFTs of integrated drive circuits S. Tomita[5 Tomita 1996] compares the size of the transistors to the pitch of the pixels in the display. An alternative approach which is more closely related to the effect of circuits on display yield is to compare the active area of the transistors in the output section of the drive circuit with the active area of the transistors used within the pixels of the display.

![Figure 5-9 Row capacitance of displays with different resolutions and diagonals](image)

If it is assumed that the total gate area of p-channel or n-channel output transistors should represent no more than 5% of the gate area of the pixel transistors then it is possible to calculate the maximum display size which satisfies this requirement. The results are summarised in Table 5-1 for colour datagraphic displays of three different resolutions. The results indicate that high resolution displays can be made at larger sizes than lower resolution displays. This simply reflects the fact that the display size limit has been based on the
relative area of the pixel and circuit TFTs. The higher resolution displays have a greater number of pixel transistors and therefore wider transistors can be used within the row drive circuit. In practice lower resolution displays would also be made at the larger sizes but the impact on display yield would be slightly greater. This result shows that in terms of the size of the output TFTs, it is quite practical to consider integrating the row drive circuits of displays up to 18-inches diagonal.

<table>
<thead>
<tr>
<th>Display Resolution</th>
<th>VGA (640x3)x480</th>
<th>SVGA (800x3)x600</th>
<th>XGA (1024x3)x768</th>
</tr>
</thead>
<tbody>
<tr>
<td>Columns x Rows</td>
<td>Total width of pixel transistors (m)</td>
<td>3.7</td>
<td>5.8</td>
</tr>
<tr>
<td>Maximum output TFT width (µm)</td>
<td>193</td>
<td>484</td>
<td>612</td>
</tr>
<tr>
<td>Maximum display diagonal (inches)</td>
<td>10</td>
<td>15</td>
<td>18</td>
</tr>
</tbody>
</table>

Table 5-1 Maximum display size based on width of row driver output transistors

The row capacitance of an active matrix display can be reduced if a separate electrode is used for forming the pixel storage capacitors. Figure 5-10 illustrates the reduction in row capacitance which is possible for a VGA display by using a separate storage capacitor electrode. The factor by which the row capacitance is reduced increases with the display diagonal. For a 6-inch display the capacitance is reduced by a factor of 3 while for a 15-inch
display it is reduced by a factor of 11. In estimating the row capacitance of the display, as described in appendix B, it has been assumed that the width of the row electrode is adjusted to maintain a minimum value for the row electrode RC time constant. For large displays this may not be practical because as the display diagonal increases the row electrode occupies an increasing fraction of the pixel area, therefore reducing the aperture of the display. In practice the RC time constant of the row will increase with display diagonal. This has been identified as an issue for displays fabricated using a-Si TFTs and may present similar problems for large low temperature poly-Si displays.

5.4 Design of Poly-Si TFT Column Drive Circuits Based on Analogue Multiplexers

The use of column drive circuits based on an analogue multiplexing approach is well established for small displays fabricated using high temperature poly-Si processing. This section describes the design of this type of column drive circuit and highlights some of the issues faced when extending this type of circuit for use with the larger displays which become possible with low temperature poly-Si processing.

Column drive circuits based on multiplexing the video signal connections to the columns of the display represent the simplest column drive circuit designs. An important feature is that the transistors within the circuit are used only as switches. It is their simplicity, combined with the fact that the circuits can be designed to be tolerant of variations in the TFT characteristics, which has resulted in their use in all of the current generation of high temperature poly-Si displays.

5.4.1 Principles of Multiplexer Operation

The multiplexing approach to column drive circuit operation is sometimes described as point at a time or block at a time addressing. This is because groups of columns are successively charged with video information during the active line period of the video signal. In contrast to this, conventional crystalline silicon column drive circuits charge all of the columns of the display simultaneously.

An example of an integrated column drive circuit based on multiplexing is shown in Figure 5-11, and waveforms illustrating its operation in Figure 5-12. The driver is made up of
multiplexing switches and selection logic. The switches can be implemented using NMOS TFTs, PMOS TFTs or CMOS transmission gates and the selection logic normally consists of one or more shift registers. The operation of the circuit is as follows. At the start of each video line period a signal is fed to the selection logic which causes it to produce a pulse at its first output. At the same time a group of m samples taken from the video signal are applied to the m video input lines. The signal g1 from the selection logic turns on the first group of multiplexing switches and the first m display columns are charged to the voltages on the corresponding video lines. When charging is complete the selection logic turns off the first group of switches and the voltages on the columns are maintained by the inherent capacitance of the column electrodes. The selection logic now turns on the second group of switches and the next group of samples taken from the video signal are applied to the video input lines. This process is repeated until all the columns in the display have been charged to the appropriate voltage level. At this point the voltages on the columns remain constant for a period T_{settle} which is equal to the line blanking period of the video signal. During this time the voltages on the pixels which are being addressed settle at their correct values.

Figure 5-11 TFT column drive circuit based on multiplexing

The main advantage of this type of column drive circuit is its simplicity. It uses a relatively small number of TFTs and its operating speed can be matched to the performance of the transistors by adjusting the number of video inputs. Two consequences of using such a simple circuit are the short time which is available for the pixel voltages to settle after the last columns have been charged and the overhead of external circuitry required to generate the parallel video signals.
The signals applied to the m video input lines can be generated by the external sampling circuit illustrated in Figure 5-13. The first group of sample and hold circuits sequentially take m samples of the input video signal. As the m\textsuperscript{th} sample is being taken the previous m-1 samples are transferred to a second set of sample and hold circuits so that the video information on the m output video lines changes simultaneously. The samples are then held on the video lines for m sample clock periods while the column drive circuit transfers them to the columns of the display.

**Figure 5-12 Timing of column drive circuit**

**Figure 5-13 External circuits required to generate parallel video signals**
An alternative to using sample and hold circuits for generating the video signals is the use of multiple digital to analogue converters. This technique is most suitable if the video information is already in a digital form, for example in data graphic applications. For an analogue signal source the additional circuits required to convert the analogue signal to a digital form would make this method unattractive.

The circuits described so far are suitable for addressing the display using a sequential video signal. If the display is used with an interlaced video source then a slightly more complex circuit is required. With an interlaced signal, each line of video information must be applied to two rows in the display. If the display is being driven with a field or column inversion drive scheme then it may be possible to achieve this simply by simultaneously selecting two rows in the display. However, displays will normally be addressed with row or pixel inversion and in this case the polarity of the column signals must be inverted before the second row of pixels is addressed. To do this the video information must be transferred to the columns of the display twice within each video line period. This can be achieved using the circuit shown in Figure 5-14. It makes use of two video line stores which effectively double the line frequency of the video signal by repeating each line of video information. As the video information is read out of the line store for the second time the polarity of the video signal is inverted so that alternate rows in the display receive opposite polarity signals.

Figure 5-14 External circuits required for use with interlaced video signal source
5.4.2 Factors Determining Multiplexer Operating Speed

One of the key performance indicators for TFT column drive circuits based on multiplexers is the number of parallel video inputs which are required since this directly reflects the operating speed of the multiplexer. For a given video standard the number of video inputs required is determined by the video signal sample frequency divided by the frequency at which video data can be transferred from the external circuitry to the columns of the display. An equivalent circuit which illustrates the main factors which limit the operating speed of the column drive circuit is shown in Figure 5-15.

The column of the display is represented by a distributed RC network. The resistors represent the resistance of the metal column electrode while the capacitance represents the capacitance between the column electrode and various other elements of the display such as the common electrode, the row electrodes and the TFTs. The multiplexer switch is represented by a resistor, the value of which will be voltage dependant. Within the column drive circuit the video information is distributed to the multiplexing switches via a video bus. These bus lines are also represented by a distributed RC network made up of the bus line resistance and the capacitance of the switches and the crossovers formed with other signal
lines within the circuit. The control signal which operates the multiplexer switch is derived from external signals and will be subject to a certain propagation delay.

This simple model of the display and column drive circuit illustrates the four factors which determine the minimum time required to charge the column electrode. The first of these is the time constant of the column electrode itself. When a voltage is applied to the top of the column it will take a certain time for the voltage at the bottom to reach the correct level due to the distributed nature of the resistance and capacitance. Secondly there is the time required for the multiplexer switch to charge the column capacitance. This will depend on the electrical characteristics of the transistors which form the switch. The third factor is the time constant of the video bus within the column drive circuit. When a video sample is applied to one end of the bus it will take a certain time for the voltage at the far end of the bus line to reach the same value. The fourth factor is concerned with the generation of the control signals for the multiplexer switches. The propagation delay of these signals will introduce a degree of uncertainty as to when data is latched from the video bus onto the columns.

A diagram illustrating the interdependence of the various aspects of the multiplexer design is shown in Figure 5-16. The four aspects of the circuits operation will each set a minimum value for the number of parallel video inputs which are required, represented by the values of N1 to N4. Three of these values are also dependent on the number of lines which are actually used in the circuit, N, making the design process to some extent iterative. The starting point for the design is to consider the effect of the column electrode RC time constant.

### 5.4.3 Column Electrode Time Constant

The importance of the time constant of the column electrode in designing a multiplexing column driver is that it will impose a certain minimum value on the time required to charge the columns, and therefore the number of video lines that the column drive circuit must have. The time constant can be estimated from the layout of the pixels, the sheet resistance of the column electrode and the thickness and dielectric constant of the various layers which isolate the column electrode from the other electrodes within the display. The size and resolution of the display will also affect the resistance and capacitance of the column electrodes and these have been estimated for displays of different sizes and resolutions in appendix B.
The distributed nature of the column resistance and capacitance means that when the multiplexing switch connected to the column turns on, the voltage at the top of the column will change quite quickly but it will take some time for the voltage at the bottom of the column to settle at the correct value. While the column is charging there will be a certain voltage distribution along the length of the column and this is illustrated in the simulated results shown in Figure 5-17. The column of the display has been represented by a chain of 20 resistors and capacitors. The effect of a step change in voltage from 0V to 1V applied to the top of the column is illustrated at times of 5, 10 and 20ns after the step. The column resistance and capacitance values were taken as 1152Ω and 18.5pF.

At the point when the multiplexing switch turns off the total charge on the column capacitance becomes fixed and the final column voltage can be determined. Any variation in the voltage along the length of the column will disappear as the charge on the column capacitance redistributes. The error in the column voltage after this redistribution takes place will be equal to the average voltage error along the length of the column at the time when the multiplexing switch turns off. This average error can easily be estimated from the simulated voltage distributions or using an equation which describes the voltage distribution.
An expression describing the voltage distribution along an RC line after application of a step change in voltage to one end is given below, equation 5-5. $V_C$ is the magnitude of the voltage step, $x$ is the position along the length of the line, $t$ represents the time since the step was applied, the total length of the line is $L_g$ and $R$ and $C$ are the capacitance and resistance per unit length.

$$V(x, t) = V_C \left( 1 - \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{1}{2n-1} \exp \left[ -\frac{(2n-1)^2 \pi^2 t}{4 R C L_g^2} \right] \sin \left[ \frac{(2n-1) \pi x}{2 L_g} \right] \right)$$

To determine the value of the voltage at which the column settles after the transmission gate has turned off the equation for the voltage distribution must be integrated along the length of the line.

$$V_{Col} = \frac{1}{L_g} \int_0^{L_g} V(x, t) \, dx$$

$$V_{Col} = \frac{V_C}{L_g} \left[ x - \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{1}{2n-1} \exp \left( -\frac{(2n-1)^2 \pi^2 t}{4 R C L_g^2} \right) \frac{-2 L_g}{(2n-1) \pi} \cos \left( \frac{(2n-1) \pi x}{2 L_g} \right) \right]_0^{L_g}$$
The error in the value of the column voltage as a percentage of the magnitude of the voltage step can be calculated using equation 5-9. Values of the voltage error have been calculated from the simulation results and calculated using equation 5-9 and the results are shown in Figure 5-18.

\[
V_{\text{Col}} = V_{\text{C}} \left(1 + \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{2}{(2n-1)^{2}} \exp \left(-\frac{(2n-1)^{2} \pi^{2} l}{4 R_{\text{Col}} C_{\text{Col}}} \right) \left(\cos \left(\frac{(2n-1) \pi}{2} \right) - 1\right) \right) \quad \text{(5-8)}
\]

\[
\text{Error} = 100 \left(1 - \left(1 + \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{2}{(2n-1)^{2}} \exp \left(-\frac{(2n-1)^{2} \pi^{2} l}{4 R_{\text{Col}} C_{\text{Col}}} \right) \left(\cos \left(\frac{(2n-1) \pi}{2} \right) - 1\right) \right) \right) \quad \text{(5-9)}
\]

Figure 5-18 Variation of column voltage error with normalised charging time

The voltage error is given as a percentage of the voltage step applied to the column electrode and the charging time is normalised with the product of the column resistance and capacitance. In calculating the voltage error using equation 5-9 the first ten terms in the series were included. Using this plot it is possible to relate the charging time required for a given voltage error to the product of the column resistance and column capacitance. Assuming a maximum voltage step of 10V and a maximum column voltage error of 10mV, equivalent to 0.1% of the voltage step, it can be seen that the ratio of the charging
time to $R_{\text{col}}C_{\text{col}}$ should be greater than three. If it is assumed that a period of $3R_{\text{col}}C_{\text{col}}$ is required for the column voltage to settle then the number of video lines required for each of the red green and blue video signals of a datagraphic display is $3R_{\text{col}}C_{\text{col}}f_{\text{pixel}}$, where $f_{\text{pixel}}$ is the pixel clock frequency of the video signal. The effect that changing the size and the resolution of the display has on the product of the column resistance and capacitance has been estimated in appendix B. This result can be used to calculate the minimum number of video lines required for a display of a particular size and resolution. The minimum number of video lines required for three different datagraphic display resolutions, VGA (640x480 pixels), SVGA (800x600) and XGA (1024x768) is shown in Figure 5-19. The corresponding pixel clock frequencies are 25MHz for VGA, 40MHz for SVGA and 65MHz for XGA.

![Figure 5-19 Minimum number of video lines based on column electrode time constant](image)

As the size and the resolution of the display increases the minimum number of video lines required increases. Only the smallest displays can be operated with a single video line for each colour, avoiding the need for external sampling circuitry. Integrating a column drive circuit at both the top and the bottom of the display, so that the column electrodes are charged from both ends, can be used to reduce the column time constant and the number of video lines required by a factor of four. The cost for doing this is the increased circuit complexity and the potential reduction in display yield since both circuits must work. The
kinks in the curves which can be seen at display diagonals of approximately 3, 4 and 5-inches correspond to the point at which the calculated width of the column electrode starts to increase from its minimum value.

5.4.4 Multiplexer Switch Design

The multiplexer switches are a key component of this type of column drive circuit. They can be formed either using individual NMOS or PMOS transistors or using CMOS transmission gates. The advantages of the transmission gate are that it provides a wider signal voltage range and lower offset voltage than an NMOS or PMOS switch. A switch formed from a single transistor is limited by the need to maintain the gate of the transistor at a voltage higher than the signal by at least the threshold voltage of the transistor. The disadvantage of using a CMOS transmission gate is that it requires two transistors and complementary signals for switching their gates. The design of both types of multiplexer switch is considered in this section starting with the use of a single transistor. The circuit of an NMOS multiplexing switch is shown in Figure 5-20. There are three important aspects to its operation, the time required to charge the load capacitance when the switch is on, the offset voltage produced when the switch turns off and the magnitude of leakage currents flowing through the switch while it is off.

![Figure 5-20 NMOS multiplexing switch](image)

An important aspect of the design of the switch is choosing the width of the transistors since this, in combination with the value of the column capacitance and the electrical characteristics of the TFT, will determine the switch performance. The charging time of a TFT switch can be estimated using the current voltage equations of a conventional MOS
transistor. An equation, derived in appendix A, relating the charging time to the electrical characteristics of the TFT, the column capacitance and the operating voltages is given below.

\[ T_{ch} = \frac{C}{\beta V_{gon}} \log \left[ \frac{2V_{gon}}{V_u - V_1} + 1 \right] \]

where \( \beta = C_{ox} \frac{W \mu}{L} \), \( C_{ox} = \frac{e_{ox}}{t_{ox}} \), \( V_{gon} = V_g - V_T - V_2 \), \( V_u \) is the voltage error at time \( T_{ch} \).

For an NMOS transistor the maximum charging time is required when \( V_2 \) represents the maximum value of column voltage and \( V_1 \) the minimum. The width of the transistor required from consideration of the charging time is given by the equation below in which \( V_{gmin} = V_g - V_T - V_2 \).

\[ W = \frac{LC_{col}}{C_{ox} \mu V_{gmin} T_{ch}} \log \left[ \frac{2V_{gmin}}{V_u - V_1} + 1 \right] \]

Substituting the values \( C_{ox}=2.3 \times 10^{-4} \text{F/m}^2 \), \( \mu=100 \text{cm}^2/\text{Vs} \), \( V_g=16 \text{V} \), \( V_T=5 \text{V} \), \( V_u=0.05 \text{V} \), \( V_T=8 \text{V} \), \( V_f=0 \text{V} \), \( L=6 \mu\text{m} \) gives the equation below in which \( f_{max} \) is the switching frequency of the multiplexer.

\[ W = 3.68 \frac{C_{col}}{T_{ch}} = 3.68 C_{col} f_{max} \]

The width of the transistor also affects the offset voltage produced when the multiplexer switch turns off. This is important because the offset introduces an error into the drive voltage applied to the columns of the display. Small differences in the mean voltage applied to the liquid crystal, less than \( \pm100 \text{mV} \), will have little effect on the display's performance but larger voltages can result in non-uniformity, low frequency flicker and image retention. Changes in the offset voltage from column to column and with the level of the signal voltage are more important from the point of view of the operation of the display than the absolute value of the offset voltage. This is because an offset voltage which is applied to all columns of the display and does not vary can be compensated for by adjusting the mean level of the video signal applied to the input of the multiplexer. There are two sources of variation in the offset voltage, the dependence of the offset on the signal voltage level and changes due to process variations such as gate oxide thickness non-uniformity or alignment variations. An
equivalent circuit for the switching transistor which illustrates the source of the offset voltage is shown in Figure 5-21.

![Equivalent Circuit of TFT](image)

**Figure 5-21 Equivalent circuit of TFT**

There are two components which make up the offset voltage of the multiplexer switch. The first results from the charge released from the channel of the transistor when it turns off. This charge divides between the source and drain terminals of the transistor with the fraction of the charge going to each terminal depending on a number of factors[^Wegmann 1987] which include the rate at which the gate voltage falls. For a rapid transition in gate voltage the channel charge divides approximately equally between the source and drain terminals. For the purposes of this simple analysis of the multiplexer switch equal charge division is assumed. The channel charge present within the transistor at the end of the charging period is given by the equation

$$V_{ch} = \frac{(V_g - V_T - V_2)C_{ox}WL}{2(C_{co} + C_{ol})}$$

The second component of the offset voltage results from the gate-drain overlap capacitance of the transistor, $C_{ol}$. This capacitance can be calculated as $C_{ol} = C_{ox}WL_o$ where $L_o$ is the overlap length. The Laser crystallised n-type TFTs developed at PRL are not self aligned devices and therefore have a relatively large overlap length. The minimum overlap which can be achieved is determined by the limits of the lithography used to define the gate of the transistor and the implanted regions. In the PRL devices the nominal overlap length is 3μm. In calculating the effect of this overlap capacitance on the offset voltage it is once again assumed that there is a rapid transition in the gate signal so that no charge is transferred from the output to the input of the switch as it turns off.

The gate drain overlap capacitance and the column capacitance form a potential divider and a fraction of the change in gate voltage is coupled onto the column. The change in the column voltage can be calculated using equation 5-14.

\[ V_{ol} = -\frac{V_g C_{ol}}{C_{ol} + C_{oi}} \]  

Combining this result with the offset due to the channel charge gives an estimate for the total output offset voltage of the switch.

\[ V_{offset} = V_{ch} + V_{ol} = -\frac{(V_g - V_T - V_s)C_{ox}WL}{2(C_{col} + C_{oi})} - \frac{V_g C_{ol}}{C_{col} + C_{oi}} \]  

\[ V_{offset} = -\frac{(V_g - V_T - V_s)C_{ox}WL + 2V_g C_{ox}WL_o}{2(C_{col} + C_{ox}WL_o)} \]  

\[ V_{offset} = \frac{(V_g - V_T - V_s) L + 2V_g L_o}{2\left(\frac{C_{col}}{C_{ox}W} + L_o\right)} \]  

The resulting expression shows that the offset voltage has a linear dependence on the signal voltage \( V_s \). To confirm that equation 5-17 provides an acceptable estimate of the offset voltage of a TFT multiplexing switch, measurements have been made using p-channel and n-channel transistors with and without LDD. Figure 5-22 shows the measured offset voltage of an NMOS switch with LDD as a function of signal voltage. For comparison the calculated offset voltage is also shown. The transition time of the gate signal used during the measurements was approximately 10ns.

The simple equation for the offset voltage provides a good estimate of the offset voltage of the switch. The offset varies linearly with the signal voltage and, as the signal voltage rises above 12V, the offset voltage starts to saturate because the gate source voltage of the TFT no longer exceeds the threshold voltage of the device. To achieve good agreement between the simple model and the measured data corrections must be made to the values of gate length and gate overlap used in the calculation. This is necessary because the channel length of the fabricated transistors is shorter than the channel length drawn on the masks from which the devices are made.
Measurement of devices with a range of gate lengths has shown that the effective channel length of the devices without LDD is shorter than that defined on the masks by approximately 1.5-2.5μm. The most likely cause for this is movement of the source and drain dopant into the undoped channel region during laser crystallisation. The corresponding reduction in channel length estimated for devices with LDD at both source and drain is less than 1μm. A possible explanation for this lower figure is the smaller difference in the dopant concentration between the n- region and the channel of the device with LDD compared to the difference between the n+ region and the channel region in the device without LDD. The effective movement of the edge of the intrinsic region will be higher in the case where the difference in the dopant concentration is greater.

In calculating the offset voltage for devices with LDD the lightly doped n- region should be considered as an extension of the overlap region rather than as part of the channel of the transistor. The presence of the dopant in the n- region means that the poly-Si is not fully depleted unless a large negative voltage is applied to the gate of the transistor. Under normal bias conditions the n- region remains conducting even when the TFT is turned off, adding to overlap capacitance of the device.
The operation of the CMOS transmission gate as a multiplexing switch is more complex than that of a single transistor. The resistance of the switch is made up of the parallel combination of the resistances of the n-channel and p-channel transistors. When a single transistor is used as the multiplexer switch it is always operated in the linear region, $V_{DS} < V_{GS} - V_T$. The transistors in the CMOS switch can be operated in the sub-threshold, linear and saturated regions. The operating regions of a CMOS transmission gate are shown in Figure 5-23.

<table>
<thead>
<tr>
<th>Region</th>
<th>n-channel transistor</th>
<th>p-channel transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>linear</td>
<td>linear</td>
</tr>
<tr>
<td>2</td>
<td>linear</td>
<td>saturated</td>
</tr>
<tr>
<td>3</td>
<td>linear</td>
<td>sub-threshold</td>
</tr>
<tr>
<td>4</td>
<td>saturated</td>
<td>linear</td>
</tr>
<tr>
<td>5</td>
<td>sub-threshold</td>
<td>linear</td>
</tr>
<tr>
<td>6</td>
<td>saturated</td>
<td>saturated</td>
</tr>
</tbody>
</table>

Figure 5-23 Operating regions of a CMOS transmission gate

The voltages on the input and output terminals of the switch are represented by $V_1$ and $V_2$. When the switch is turned on the gate of the n-channel transistor is held at the high supply voltage level, $V_{DD}$, and that of the p-channel device at the low supply voltage level $V_{SS}$. For values of $V_1$ and $V_2$ which lie between $V_{SS}$ and $V_{DD}$ six different operating regions can be identified depending on which of the transistors is operating in its sub-threshold, linear or saturated region.
An approach to sizing the transistors of the transmission gate is to calculate the charging time based on the approximation that the resistance of the transmission gate is constant and equal to the maximum value of the transmission gate resistance. It is shown in appendix C that the minimum conductance of a CMOS transmission can be approximated by the equation

\[ G_{\text{min}} = \beta_{\text{min}}(VDD-VSS+V_{TP}-V_{TN}) \]  

in which \( \beta_{\text{min}} \) is the smaller of the transconductance parameters of the two transistors, \( \beta_n \) and \( \beta_p \). The charging time can be calculated by using the exponential charging behaviour of a capacitor charged via a resistor.

\[ T_{ch} = RC\log\left(\frac{V_2-V_1}{V_u}\right) = \frac{C}{\beta_{\text{min}}(VDD-VSS+V_{TP}-V_{TN})}\log\left(\frac{V_2-V_1}{V_u}\right) \]

where \( \beta = \frac{C_{ox}W_L}{L} \), \( C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \), \( V_j \) is the initial voltage, \( V_2 \) is the final voltage and \( V_u \) is the voltage error at time \( T_{ch} \). This equation can be rearranged to give the transistor width required for a certain charging time.

\[ W = \frac{C_{col}L}{T_{ch}C_{ox}\mu_{\text{min}}(VDD-VSS+V_{TP}-V_{TN})}\log\left(\frac{V_2-V_1}{V_u}\right) \]

Substituting the values \( C_{ox}=2.3\times10^{-4}\text{F/m}^2 \), \( \mu_{\text{min}}=80\text{cm}^2/\text{Vs} \), \( V_{TP}=-5\text{V} \), \( V_{TN}=5\text{V} \), \( V_u=0.05\text{V} \), \( L=6\mu\text{m} \), \( V_2-V_1=8\text{V} \) gives the equation below in which \( f_{\text{max}} \) is the switching frequency of the multiplexer.

\[ W = 2.76C_{col}f_{\text{max}} \]

The offset voltage of the CMOS transmission gate will, like the NMOS or PMOS switch, consist of a component due to the channel charge and a component due to the overlap capacitances of the transistors. The fact that the voltage waveforms applied to the gates of the n-channel and p-channel transistors are complementary means that there will be some cancellation of the offsets produced by the two devices. A simple expression for the offset voltage can be derived if it is assumed that symmetrical gate drive signals are applied to the two transistors and that the gate signals switch sufficiently fast that the channel charge of the devices divides equally between the source and drain terminals.
The channel charge released from the NMOS transistor will be equal to
\[ Q_n = -\frac{1}{2} (VDD - V_{th} - V_2) C_{ox} W_n L_n \]
if \( V_2 \leq VDD - V_{th} \) otherwise it will be zero. The charge released from the p-channel device will be
\[ Q_p = \frac{1}{2} (-VSS + V_{tp} + V_2) C_{ox} W_p L_p \]
if \( V_2 \geq VSS - V_{tp} \) otherwise it will also be zero. From these equations the contribution to the offset voltage of the CMOS transmission gate due to the release of charge from the channel can be calculated.

For the condition \( VSS - V_{tp} \leq V_2 \leq VDD - V_{th} \)
\[
V_{ch} = \frac{Q_n + Q_p}{C_{coll} + C_{oln} + C_{olp}}
\]
\[
V_{ch} = \frac{-(VDD - V_{th} - V_2) W_n L_n + (-VSS + V_{tp} + V_2) W_p L_p}{2 \left( C_{col} + W_n L_{on} + W_p L_{op} \right)} \tag{5-22}
\]

For \( V_2 < VSS - V_{tp} \)
\[
V_{ch} = \frac{-(VDD - V_{th} - V_2) W_n L_n}{2 \left( C_{col} + W_n L_{on} + W_p L_{op} \right)} \tag{5-23}
\]

For \( V_2 > VDD - V_{th} \)
\[
V_{ch} = \frac{(-VSS + V_{tp} + V_2) W_p L_p}{2 \left( C_{col} + W_n L_{on} + W_p L_{op} \right)} \tag{5-24}
\]

Like the NMOS switch, the CMOS transmission gate has a linear dependence of the offset voltage on the signal voltage. However, in the case of the transmission gate the rate at which the offset voltage changes with input voltage has three possible values depending on whether one or both of the transistors are conducting. The contribution to the offset voltage from the gate overlap can be calculated using the following equation.
\[
V_{ol} = \frac{-(VDD - VSS) C_{oln}}{C_{col} + C_{oln} + C_{olp}} + \frac{(VDD - VSS) C_{olp}}{C_{col} + C_{oln} + C_{olp}}
\]
The combined offset voltage taking into account both the channel charge and the overlap capacitance for the region where both transistors are conducting is given by equation 5-26.

\[
\begin{align*}
V_{\text{offset}} &= \frac{(V_{DD} - V_{SS})(C_{col} - C_{alin})}{C_{col} + C_{alin} + C_{alp}} \\
&= \frac{-(V_{DD} - V_{Tn} - V_{T})W_{n}L_{n}}{2C_{col}} + \frac{-(V_{SS} + V_{Tp} + V_{T})W_{p}L_{p}}{2C_{col}} + 2(V_{DD} - V_{SS})(W_{n}L_{n} - W_{p}L_{p})
\end{align*}
\]

The measured offset voltage of a CMOS transmission gate and the value of offset calculated using equation 5-26 are shown in Figure 5-24. The p-channel and n-channel devices have the same channel length and channel width, the n-channel device has LDD regions at both source and drain and the p-channel device has its overlap length increased to compensate for the capacitance of the LDD regions in the n-channel TFT. Good agreement is obtained between the calculated and measured values of offset voltage.

![Figure 5-24 CMOS transmission gate offset voltage](image)

The leakage current passed by the CMOS transmission gate or the single NMOS or PMOS transistors must be sufficiently small that the column voltage does not change significantly during the periods while the switch is turned off. In the column multiplexer circuit the
maximum time during which the column voltage must be maintained is approximately equal to the line time of the video signal. The maximum value of leakage current which can be tolerated can be estimated by using equation 5-27 in which $\Delta V$ is the maximum change in column voltage and $T_{\text{line}}$ is the video line period.

$$I_{\text{leakage}} \leq \frac{C_{\text{col}} \Delta V}{T_{\text{line}}}$$  \hspace{1cm} 5-27

It is common to express the leakage current of TFTs in terms of the leakage current per unit width of the device. This can be done by dividing the leakage current by the width of the transistors calculated using equation 5-12 or 5-21. For the CMOS transmission gate the resulting equation is 5-28.

$$I_{\text{leakage}} \left( \frac{\text{A}}{\text{m}} \right) \leq \frac{\Delta V}{2.76 f_{\text{max}} T_{\text{line}}}$$  \hspace{1cm} 5-28

Substituting typical values of $\Delta V=10\text{mV}$, $f_{\text{max}}=5\text{MHz}$, $T_{\text{line}}=32\mu\text{s}$ gives a leakage current of $23\text{pA}/\mu\text{m}$. This is comparable to the maximum leakage current measured for the laser crystallised devices which were illustrated in figure 3-9 of chapter 3.

A factor which may set a limit on the minimum number of video lines required for a multiplexing column drive circuit is the width of the transistors making up the multiplexing switches. As the size and resolution of the display increases so does the column capacitance. In addition, higher resolution displays have a higher pixel clock frequency requiring data to be transferred more quickly to the columns of the display. These factors will increase the size of the transistors needed to charge the columns of the display. However, increasing the size of these transistors will tend to reduce the yield of displays and it may be appropriate to set a maximum figure on the size of the multiplexing transistors compared to the size of the transistors within the pixels of the display.

The number of video lines required to limit the active area of the n-channel or p-channel TFTs within the multiplexing switches to no more than 10% of the active area of the pixel transistors has been calculated. The values of the column capacitance, illustrated in Figure 5-25, and pixel transistor width have been calculated as described in appendix B. The width of the TFTs within the transmission gates has been calculated using equation 5-21. The minimum number of video lines that are required is shown in Figure 5-26.
Figure 5-25 Variation of column capacitance with display diagonal

Figure 5-26 Minimum number of video lines required based on multiplexer TFT size
The number of video lines required increases as the display size and resolution increases. The sudden change in the slope of the curves, occurring at a diagonal of just under 12 inches for the VGA display, reflects the point at which the width of the pixel transistor starts to increase above the minimum value of 4μm. In section 5.4.7 these results are compared with the number of video lines calculated by considering the column electrode RC time constant.

The offset voltage of the multiplexer switches has not been treated as a factor which limits the number of video lines required by the column drive circuit. However, if the variation in offset voltage from column to column is significant, greater than 100mV, then it may be necessary to reduce the width of the multiplexing transistors. As well as the voltage dependence of the offset voltage which has already been described, variations in the capacitance of the column electrodes, the gate dielectric thickness or the timing of the gate drive signals of CMOS transmission gates may also result in offset voltage variations.

### 5.4.5 Multiplexer Video Bus Design

There are two different ways in which the video lines and the multiplexer switch control lines within the column driver can be connected. These options are illustrated in Figure 5-27. The multiplexer switches are arranged into groups which charge a set of adjacent columns in the display. In the first arrangement of the multiplexer the switches in one group have a common control signal and are turned on simultaneously to charge one group of columns. Each switch within the group is connected to a separate video bus line and these carry voltages which represent successive samples taken from the video signal. In the second multiplexer arrangement the switches within a group are connected to a single video bus line and have separate control signals. The columns within a group are charged sequentially during the video line period. The preferred arrangement of the switches is the first one. The second arrangement has only rarely been used because it requires that the picture information in each line of the video signal is reordered before it is transferred to the display. This requires the use of a video line store and therefore adds to the complexity of the display drive circuitry.

The video bus lines in the most commonly used multiplexer arrangement run the length of the drive circuit. The resistance of these lines along with the capacitance of the multiplexer switches connected to them and the control signal lines which cross them, delays the transfer of the video signals to the columns of the display.
Choosing the correct layout for the video bus, in particular the optimum width of the bus lines, is an important part of the multiplexer design. For best performance the capacitive load on the bus lines should be minimised. If the column drive circuit is located beneath the passive plate of the LC cell then it is an advantage if the ITO electrode on the passive plate is removed from above the circuit. If the ITO is left in place then the capacitance between the video bus lines and the common electrode will significantly increase the RC time constant of the video bus and possibly limit the operating speed of the multiplexer.

The video bus line resistance can be calculated using equation 5-29 in which $W_{bus}$ and $L_{bus}$ are the width and length of the bus line and $R_s$ is the sheet resistance of the video bus metalisation. The capacitance of the video bus lines is made up of four components. These are the capacitance of the inputs of the multiplexer switches, the capacitance of the crossovers with other video lines, the capacitance of crossovers with the control signals for the multiplexer switches and the capacitance of one column electrode and the multiplexer switch which is charging it.

$$R_{bus} = \frac{W_{bus}R_s}{L_{bus}} \quad 5-29$$

The dependence of the capacitance on the number of video lines, $N$, and the number of columns in the display, $M$, is indicated in equation 5-30. In this equation $C_{sx}$ is the input capacitance of the multiplexer switch in the off state, $C_{xon}$ is the input capacitance of the multiplexer switch in the on state, $C_{xoc}$ is the capacitance of a crossover with the switch
control signal line, $C_{xov}$ is the capacitance of a crossover with another video bus line and $C_{col}$ is the capacitance of a column.

$$C_{bus} = C_{ax} \left( \frac{M}{N} - 1 \right) + C_{soc} \frac{2M}{N} + C_{xov} \frac{N-1}{N} + C_{xsn} + C_{col} \quad 5-30$$

Consider the example of a multiplexer using CMOS transmission gates as the multiplexing switches. Substituting expressions for the capacitances in which $t_{ox}$ is the thickness of the gate oxide, $t_{xo}$ is the thickness of the crossover oxide, $W_{xt}$, $L$ and $L_o$ are the gate width, gate length and gate drain overlap length of the transistors in the CMOS transmission gate, $W_{el}$ is the width of the switch control signal lines, $W_{vi}$ is the width of the video signal lines which connect to the multiplexer switches.

$$C_{bus} = \frac{2\varepsilon_{ox} W_{xt} \left( \frac{M}{N} - 1 \right)}{t_{ox}} + \frac{\varepsilon_{ox} W_{vi} W_{bus}}{t_{xo}} \frac{2M}{N} + \frac{\varepsilon_{ox} W_{el}}{t_{xo}} \frac{M(N-1)}{N} + \frac{2\varepsilon_{ox}(L+2L_o)W_{xt}}{t_{ox}} + C_{col} \quad 5-31$$

In section 5.4.4 an expression relating the width of the transmission gate transistors to the multiplexer operating frequency was obtained, equation 5-21. This can be substituted into the expression above with values of $t_{so}=0.3\times10^{-6}$m and $L_o=6\times10^{-6}$m.

$$C_{bus} = 1.15 \times 10^{-4} W_{bus} (2W_{el} + (N-1)W_{oi}) \frac{M}{N} + \frac{2.29 \times 10^{-4} f_{video} (2 + \frac{M}{N}) + 1}{N} C_{col} \quad 5-32$$

It was shown that in section 5.4.3 that because of the distributed resistance and capacitance of the column electrode a voltage settling time of $3R_{col}C_{col}$ was required for the column voltage. This same condition can be applied to the video bus so that a minimum figure for the number of video lines can be calculated from the resistance and capacitance.

$$N \geq 3R_{bus} C_{bus} f_{video} \quad 5-33$$

Substituting the expressions for the video bus resistance and capacitance into 5-33 results in a third order polynomial expression in $N$. This has been solved graphically by plotting the value of $3R_{bus} C_{bus} f_{video}$ as a function of $N$ and taking the point where the two values are equal. An example of the plot, which assumes a sheet resistance for the video bus metalisation of $R_s = 0.25 \Omega/\square$ and a column capacitance of 20pF for a VGA resolution display with a diagonal of 5-inches, is shown in Figure 5-28.
Figure 5-28 Minimum number of video bus lines 5-inch colour VGA

Figure 5-29 Effect of bus width on minimum number of video lines
The minimum number of video bus lines has been calculated for a number of different display sizes and resolutions as shown in Figure 5-29. As the size and resolution of the display increases the minimum number of video lines required also increases. Increasing the width of the video bus lines allows the number of video lines to be reduced, but the advantage diminishes as the bus width becomes large as the capacitance of the lines crossing the video bus becomes large compared to the capacitance of the transmission gates. In these calculations is has been assumed that the video bus is driven from only one end. The effective RC time constant of the bus can be reduced by driving it from both ends or by driving it from the centre. In both cases the time constant is reduced by a factor of four.

5.4.6 Multiplexer Control Circuit Design

The groups of multiplexer switches within the column drive circuit are controlled by one or more shift registers as indicated in Figure 5-30. By using a number of shift registers operating with clock signals having different phases the clock frequency of each individual shift register can be reduced.

![Figure 5-30 Combinations of shift registers and video lines](image)

Many different designs for CMOS shift registers exist. A number of designs which have been applied to the row and column drive circuits for AMLC displays are described here. Two basic CMOS static shift register circuits which provide scanning in a single direction are shown in Figure 5-31. The first circuit uses inverters and transmission gates\(^\text{[1]}\) and requires eight TFTs per section. The second design replaces the transmission gates with clocked inverters and requires ten TFTs per section.\(^\text{[2]}\)

\(^\text{[1]}\) Nishihara 1992
\(^\text{[2]}\) Maekawa 1992, Ohshima 1993
Figure 5-31 Shift registers for single scan direction

Figure 5-32 Shift registers for bi-directional scanning
Examples of shift registers which are capable of bi-directional scanning are shown in Figure 5-32. The circuit used by Asada\[\text{Asada 1996}\] is similar to the previous circuit which used clocked inverters, but in this arrangement the carry signal from one section to the next is passed via a transmission gate rather than an inverter so that it can pass in either direction. The scan direction is determined by the relative phase of the two clock signals. If $C_1$ and $C_2$ are in phase then the carry signal is shifted from right to left. If $C_1$ and $C_2$ are complementary then the signal is shifted from left to right. The number of TFTs used is only eight per section.

The bi-directional circuit adopted by Maekawa \[\text{Maekawa 1994}\] also uses transmission gates to route the carry signal from one section to the next. If the direction control signal $R$ is high then the signal passes from left to right, if it is low the signal is passed from right to left. The circuit uses sixteen TFTs per section and is combined with a method for reducing clock line loading which is described below. The shift register used by Takafuji \[\text{Takafuji 1993}\] is made up entirely from clocked inverters with sixteen transistors per section. The scan direction is controlled by complementary direction control signals which enable inverters passing the shift register signal from left to right if $R$ is high and enable inverters passing the signal from right to left if $R$ is low. There is no clear choice as to which shift register circuit is best. Although some circuits require a larger number of transistors these devices will generally be small and therefore the increase is unlikely to have a large effect on the yield or layout of the circuit.

![Shift register with reduced clock line loading](image)

**Figure 5-33 Shift register with reduced clock line loading**
As the size and resolution of displays increases, greater demands are placed on the performance of the shift registers. One problem is the increased load capacitance on the clock lines of the shift register as the number of register sections increases. A technique for reducing the clock line loading described by Maekawa [Maekawa 1994] is shown in Figure 5-33. In this circuit the clock signals used within each section of the shift register are isolated from the clock bus lines by two transmission gates. These transmission gates are normally turned off but when a high level appears at the input to the shift register section the transmission gates are turned on and the clock signals are passed to the clocked inverters. The transmission gates remain turned on until the output of the register section goes low. When the transmission gates are turned off the signal C is held low and its complement held high by high resistance load devices. The advantage of this circuit is that the input capacitance of the transmission gates when they are turned off is lower than the capacitance of the clock inputs of the clocked inverters. As a result the capacitive loading of the clock bus lines is reduced.

Another issue for the design of high performance shift register circuits is the effects of clock skew. Hashizume [Hashizume 1994] describes a shift register circuit in which a single clock line is distributed to the shift register sections and local complementary clocks are generated for each section as shown in Figure 5-34.

![Figure 5-34 Shift register with locally generated complementary clocks](image-url)
The timing of the operation of the multiplexer switches is an important aspect of the operation of the drive circuit. Two issues which must be considered are illustrated in Figure 5-35. The first is the timing of the operation of the multiplexer switches relative to the changing video information applied to the video lines.

There will be a propagation delay, $t_{pd}$, between the external control signals applied to the column drive circuit and the operation of the multiplexer switches. If this delay is not taken into account then the transmission gates would switch off after the voltages on the video lines had been changed to the levels required for the next group of columns in the display. The visual effect of this would be the presence of a double image on the display, the horizontal separation of the images corresponding to the width of one group of multiplexer switches. If the propagation delay is similar for all the multiplexer switch groups within the drive circuit then it can be compensated for by adjusting the phase of the video data relative to the column driver control signals. If the propagation delay is large compared to the video data periods or if it varies with the position in the drive circuit, for example due to clock skew, then it may not be possible to select a satisfactory clock phase for all parts of the circuit. In this case the number of video lines would have to be increased so that the video data periods could be extended.

A second potential source of error in the operation of the multiplexer is overlapping of the switching signals as indicated by $t_{oi}$ in Figure 5-35. The effect of this overlap is shown in an exaggerated form in Figure 5-36. The video bus line is represented by an RC transmission line. When the second multiplexer switch turns on the current which flows through the video line to charge the column capacitance causes the voltage at the first switch to fall, partially discharging the first column. If the first switch turns off before this
disturbance to the video bus voltage has settled then an incorrect voltage will be sampled onto the first column. This problem can be avoided by ensuring that the gate drive signals of switches which are connected to the same video line are non-overlapping.

Figure 5-36 The effect of overlapping multiplexer control signals

A change to the layout of the video bus which can be made to reduce the effect of overlapping switch control pulses is shown in Figure 5-37. In this arrangement multiplexer switches which are connected to the same video signal input, and may be simultaneously conducting, are connected to separate video bus lines. These lines are connected to a common video signal source outside the drive circuit. The main disadvantage of this approach is the increased width of the drive circuit due to the additional video bus lines which must be accommodated in the layout.

Figure 5-37 Divided video bus
A technique for preventing the control signals to adjacent multiplexer switch blocks from overlapping is to use NOR gates in the arrangement of Figure 5-38. The switch control signal from the previous multiplexer block is used to mask the output to the current block preventing it from going high until the previous output has gone low.

![Figure 5-38](image)

**Figure 5-38 Use of NOR gates to prevent overlapping pulses**

Other techniques for avoiding overlap of the multiplexer control signals are also possible such as tailoring the width of the transistors in the circuit so that the propagation delay for the signal turning on a switch is always longer than that for turning a switch off. Alternatively the control signals from the shift register can be masked using externally generated clock signals so that a known delay can be introduced between the control signals.

A further issue for multiplexers which use CMOS transmission gates is the generation of the complementary switching signals required to drive the gates of the p-type and n-type TFTs. Variations in the timing of these signals will result in variations in the offset voltage produced when the transmission gates turn off. Two circuits which can be used to generate symmetrical switching signals are shown in Figure 5-39.

![Figure 5-39](image)

**Figure 5-39 Generation of CMOS transmission gate control signals**
In the first technique the propagation delays through the chains of inverters used to buffer the positive and negative going switching signals are balanced by appropriate sizing of the transistors within the inverters. This approach has been successfully used with conventional silicon devices[^1] but as it relies on controlling the propagation of the switching signal through a number of inverters it will be sensitive to localised variations in the transistor characteristics which may be present in laser crystallised poly-Si devices. An alternative method is to synchronise the two signals using a pair of cross coupled inverters as shown on the right of Figure 5-39. If the complementary switching signals do not arrive at the cross coupled inverters at the same time then the transition of the first signal is delayed until the second signal switches. This technique is very effective at synchronising the complementary signals and has been used in the design of column drive circuits using high temperature poly-Si TFTs.[^2][^3][^4][^5][[^6]

### 5.4.7 Summary of Column Drive Circuit Design

One of the advantages of TFT column drive circuits based on analogue multiplexing is that their operation is relatively simple with all the TFTs operating as switches. A clear indication of the performance of the circuit is the number of parallel video inputs which are used as this directly reflects the operating speed of the multiplexer. The design of the circuit requires four main issues to be considered, the time constant of the column electrodes of the display, the sizing of the multiplexer switches, the time constant of the video bus lines within the circuit and the propagation delays associated with generating the multiplexer control signals. The minimum number of video inputs required by the circuit has been calculated based on the first three of these issues and the results are summarised in Table 5-1 for four different combinations of display size and resolution.

<table>
<thead>
<tr>
<th>Display</th>
<th>5&quot; VGA</th>
<th>12&quot; VGA</th>
<th>12&quot; SVGA</th>
<th>12&quot; XGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Column RC time constant</td>
<td>3</td>
<td>10</td>
<td>17</td>
<td>30</td>
</tr>
<tr>
<td>Multiplexer TFT width</td>
<td>8</td>
<td>29</td>
<td>35</td>
<td>39</td>
</tr>
<tr>
<td>Video bus RC time constant</td>
<td>4</td>
<td>9</td>
<td>14</td>
<td>21</td>
</tr>
</tbody>
</table>

Table 5-1 Summary of considerations for the minimum number of video lines per colour

The first point which can be seen from these results is that as the size and the resolution of the display increases the number of video lines also increases. The factor which imposes the greatest restriction on the minimum number of video lines is the width of the multiplexer TFTs. This calculation was based on limiting the size of the multiplexer TFTs in order to
avoid degrading the yield of working displays. In an established production environment where the defect mechanisms are well understood in may be possible to relax this restriction and increase the size of the TFTs used within the circuit. The design consideration which imposes the next limit on the minimum number of video lines for larger displays is the RC time constant of the column electrode. This limit reflects the time required for a voltage applied to one end of the column electrode to propagate to the far end and it will be a function of the detailed structure of the pixels in the display. For small displays the RC time constant of the video bus lines imposes a slightly higher limit on the minimum number of video lines. The propagation delay times of the circuits which generate the control signals for the multiplexing switches should be small compared to the video data periods. Overlapping of the control signals or delays between the switching of the video data and the multiplexer switches can result in crosstalk of information between groups of columns in the display unless sufficient time is allowed for the voltages on the video bus lines to settle.

5.5 Prototype Datagraphic AMLCD

A prototype display with integrated drive circuits has been designed based on the requirements of a 6-inch diagonal VGA resolution datagraphic display. The prototype has one third of the number of rows and columns of the full display and has a diagonal of 2-inches. The main properties of the display are summarised in Table 5-2.

<table>
<thead>
<tr>
<th>Number of Columns</th>
<th>640</th>
</tr>
</thead>
<tbody>
<tr>
<td>Column Pitch (µm)</td>
<td>63.5</td>
</tr>
<tr>
<td>Number of Rows</td>
<td>160</td>
</tr>
<tr>
<td>Row Pitch (µm)</td>
<td>190.5</td>
</tr>
<tr>
<td>Video Data Frequency (MHz)</td>
<td>25.175</td>
</tr>
<tr>
<td>Number of Video Inputs</td>
<td>6 x (RGB)</td>
</tr>
<tr>
<td>Video Line Period (µs)</td>
<td>31.8</td>
</tr>
<tr>
<td>Line Blanking Period (µs)</td>
<td>6.4</td>
</tr>
</tbody>
</table>

Table 5-2 Prototype VGA direct view display

5.5.1 Row Drive Circuit

The row drive circuit is illustrated in Figure 5-40. It consists of a shift register, NAND gates to control the timing of the row select pulses, level shifters and output drivers. Level shifters are used to allow the output voltages to be adjusted independently of the power supply voltage of the shift register.
The bi-directional shift registers consist of two inverters and four transmission gates for each section. The scan direction is determined by the levels applied to the complementary scan direction control signals DWN and DWN. A high level signal DWN turns on the transmission gate which passes the output of the shift register section to the right while a low level causes the output signal to be passed to the left. The width of all TFTs in the shift register is 10µm, the n-channel transistors used in the inverters have LDD at the drain end of the channel while those in the transmission gates have LDD at both ends of the channel.

The output pulses produced by the shift register overlap by half the clock period. In order to generate the non-overlapping pulses required to address the rows of the display the shift register signals pass through NAND gates which mask the pulses with externally generated output enable signals OE1 and OE2.
A diagram illustrating the row drive circuit in more detail is shown in Figure 5-41. Two stages of level shifting have been used to isolate both the high and low level output voltages from the power supply voltage used by the shift register. In the first level shifter the high level of the signal from the shift register is changed from VDD to the output voltage level VDDO and in the second the low voltage level is altered from VSS to VSSO. All of the control signals for the row drive circuit are at the levels of VDD and VSS. Two inverters are used at the output of the second level shifter to drive the row capacitance of the display.

The width of the output transistors was chosen to give rise and fall times of less than 2μs for a full 6-inch display. Separate power supply levels, VS and VNS, were supplied to the output inverter in order to allow the output voltage to be modulated if part of the drive voltage for the LC was applied via the common electrode of the display. Modulation of VNS would result in reversal of the drain source voltage across the n-channel device in the output
inverter. In order to prevent this causing hot carrier degradation LDD was incorporated at both ends of the channel of this transistor.

The layout of the row drive circuit is shown in Figure 5-42. Automated layout of TFT circuits is not yet established and therefore the transistors and circuits were built up by defining polygons in the various mask layers used during the fabrication of the displays. The main constraint on the layout is that the pitch of the outputs of the circuit must match the pitch of the rows in the display, 190.5µm. The large transistors which form the output inverter can be seen at the bottom of the picture and the shift register at the top. A second shift register was included in the layout, connected in parallel with the first, in order to provide a degree of redundancy. Defects in one of the registers can be isolated using laser cutting allowing the second register to function correctly. Probe pads are connected to nodes within the shift register and at the row drive outputs for use during inspection of the circuit. The total height of the circuit is 1400µm.
5.5.2 Column Drive Circuit

The column drive circuit of the display is illustrated in Figure 5-43. It consists of an arrangement of four shift registers which are operated at a frequency of 3.15MHz with four different clock phases. Each shift register output is used to control a group of three multiplexer switches and these simultaneously sample red, green and blue video information from three of the video lines. Six video lines are used for each colour and data is transferred from these lines at 4.19MHz giving the required overall data rate of 25.175MHz per colour.

![Figure 5-43 Schematic diagram of column drive circuit](image)

The timing of the transfer of video data to the columns of the display is illustrated in Figure 5-44. The clock signals applied to the four shift registers and the timing of the pulses at the outputs of the registers are shown at the top of the diagram. At the bottom of the diagram the timing of the periods when data is transferred from the six video lines to the columns of the display is shown. By using a number of video lines which is greater than the number of shift registers, the duration of the pulses generated by the shift registers becomes shorter than the video data period. This ensures the data transfer periods for a particular video line do not overlap and avoids the use of a NAND or NOR gate between the shift register and the multiplexer which would increase the propagation delay of the switching signals.
The time available for charging each column is 160ns, this is followed by a period of 80ns when no column is connected to the video line and the video voltage can be changed to that required for the next column. The period when data is transferred from the video lines is offset by 40ns for each successive video line. This simplifies the external sampling circuit as
the second set of sample and hold circuits which were illustrated in Figure 5-13 are not required with this arrangement of the drive circuit. A diagram illustrating the circuit for two sections of one of the shift registers is shown in Figure 5-45. In view of the higher operating speed of the column drive circuit the gate length of the TFTs was reduced from the value of 6µm used in the row driver to a value of 4µm. LDD was included at the drain of n-channel devices used in inverters and at the source and drain of devices used in transmission gates.

The circuit has been designed to minimise the propagation delay between the timing edges of the clock signals and the switching signals applied to the transmission gates within the multiplexer. Complementary gate drive signals for the multiplexer transmission gates are generated using a pair of cross coupled inverters to produce accurately timed signals. To minimise the propagation delays the cross coupled inverters are driven directly by the complementary signals on the clock buses via transmission gates. This eliminates the propagation delay through the shift register which would occur with a more conventional circuit design. The transmission gates connected to the clock bus are turned on only when the circuit must select the multiplexing switches at its output. This is achieved using the NOR gate and will reduce the load capacitance on the clock bus lines.

The operation of one section of the circuit is as follows. When the carry signal from the previous section goes high, this causes the output of the NOR gate to go low turning on the transmission gates connected to the clock bus. At the point when this happens the state of the bi-stable formed by the cross coupled inverters will correspond to the levels on the two clock lines. When the signals on the clock lines change state this change is coupled through the transmission gates to the cross coupled inverters. The edges of the clocks are synchronised by the cross coupled inverters and then the clock pulse is transmitted through the chain of inverters to turn on the group of transmission gates within the multiplexer. The selected group of columns is charged to the levels of the voltages on the video bus lines. At the same time as the pulse is applied to the multiplexer transmission gates the carry input signal from the previous section of the shift register will go low. To prevent the transmission gates connected to the clock bus from turning off when this happens a signal is fed back from the cross coupled inverters to the second input of the NOR gate. A further signal from the cross coupled inverters acts as the carry signal which is fed on to the next section of the circuit. An arrangement of four transmission gates is used to route the carry signals allowing for reversal of the scan direction depending on the state of the complementary control signals RGT and /RGT.
All inverters and transmission gates use p-channel devices of 10/4 and n-channel devices of 8/4 unless indicated otherwise.

Figure 5-45 Schematic diagram of column drive circuit shift register
A photograph of the circuit which shows one section from each of the four shift registers is shown in Figure 5-46. The four broken lines near the top of the picture are the carry signals passing from one shift register section to the next and below them are the transmission gates which control the scan direction. The large transistors of the inverter chains used to drive the transmission gates in the multiplexer and a number of the video bus lines can be seen towards the bottom of the picture. The pitch of one shift register section is three times the pitch of the columns in the display since each output drives three multiplexing switches. The total height of the circuit including the video bus lines and multiplexing switches is 3000μm.
The layout of the video bus lines and the multiplexer transmission gates is shown in Figure 5-47. Two p-channel and two n-channel transistors make up each transmission gate with the pairs of transistors arranged in such a way that any misalignment of the gate relative to the channel of the device does not alter the capacitance between the gate and the input or output nodes of the switch.

![Figure 5-47 Layout of column multiplexer transmission gates](image)

5.5.3 Test Multiplexers

One of the advantages of integration of the drive circuits onto the substrate of an active matrix LC displays is that it is possible to build additional testing circuits, or to use the drive circuits themselves, for testing the active plate of the display before the cell is
completed. In colour direct view displays the cost of the passive plate of the display, which includes the mosaic colour filter, is similar to the cost of the active plate. It is therefore an advantage if defective active plates can be rejected before the active and passive plates are assembled to form the liquid crystal cell.

![Diagram of display components](image)

**Figure 5-48 Location of test multiplexers**

Test multiplexers have been integrated onto the 2-inch prototype display. These are located between the integrated drive circuits and the active matrix as indicated in Figure 5-48. Each multiplexer consists of a static CMOS shift register the outputs of which control pairs of multiplexing switches as indicated in Figure 5-49. These are connected between one of the row or column electrodes and one of four output lines. By applying a
carry pulse and an appropriate number of clock cycles to the shift register it is possible to select each row or column and connect it to an external signal line. A number of tests can be carried out using this arrangement. The continuity of row and column electrodes can be tested by using the multiplexers at the two ends of the electrode to measure its resistance. Short circuits between electrodes can be detected using a single multiplexer to measure the resistance between adjacent electrodes. Examples of these measurements are shown in Figure 5-50. The display measured in this test has no defective row electrodes but contains a number of columns which are connected and one column electrode which is broken. Tests can also be performed to detect short circuits at the crossovers between the row and column electrodes and to measure the output signals of the integrated drive circuits.

![Figure 5-50 Row and column resistance measurements](image-url)
5.5.4 Display Operation

A photograph of a fabricated display substrate is shown in Figure 5-51. The column drive circuit is located at the top of the display with row drivers on both the left and the right to provide a degree of redundancy. The power supply and control signals are fed to the circuits via the contacts on the right hand side of the substrate. Process control monitors, transistors and test circuits are located around the display. Examples of images produced by the display are shown in Figure 5-52 and Figure 5-53. The display was operated with a VGA video signal and shows one ninth of the full video image. Grey scale images with good contrast and uniformity were obtained.

Figure 5-51 Processed substrate with active matrix and drive circuits
Figure 5-52 Image on the 640x160 pixel display

Figure 5-53 Image on the 640x160 pixel display
The shift register of the row drive circuit was operated with power supply voltages of 0V and 10V while the output section was operated with power supplies of 0V and 16V. The power consumption of the circuit, excluding the power required by the external circuits which drive the clock lines, was less than 0.05mW. A waveform measured on one of the rows of the display is shown in Figure 5-54. The rise time of the output signal is 0.5μs and the fall time 0.4μs.

![Row drive waveform](image)

**Figure 5-54 Row drive waveform**

The column drive circuit of the display was operated with power supply voltages of 0V and 16V. The power consumption of the column drive circuit, excluding the power consumed by the external clock line drive circuits, was 17mW. Waveforms measured at various points within one section of the circuit are shown in Figure 5-55. The propagation delay between the complementary clock signals and the pulses applied to the multiplexer transmission gates is 25ns.
The transmission of the display was observed to increase when the column voltage inversion scheme was changed from field inversion to row inversion. The cause of this is undercharging of the column capacitance by the column drive circuit and column voltage waveforms which illustrate this are shown in Figure 5-56. The image on the display was a uniform grey field and the polarity of the column drive voltages was inverted at the end of each video field period. The column is charged once during each video line period, every 32µs, and it can be seen that the first time that the column is charged after the polarity of the video signal has switched the column drive circuit is unable to charge the column to the final
voltage level within the 160ns charging period. In fact the change in column voltage is only 92% of the expected value. In successive charging periods the column voltage moves closer to its final value. The time constant for charging the column can be estimated by assuming that the column charges exponentially. The time required for the change in column voltage to reach 92% of its final value is \(-\log_2(1-0.92) = 2.5\) time constants. Since the charging time is 160ns the value of the time constant is 64ns.

![Column waveforms measured in field inversion](image)

**Figure 5-56 Column waveforms measured in field inversion**

The undercharging results from the column capacitance being higher than the value estimated during the design of the drive circuits. This is due to the significant contribution from edge effects. The measured value of column capacitance is 13pF. During the measurement of the column waveforms shown above a high input impedance amplifier with an input capacitance of approximately 5pF was connected to the column giving a total capacitance of 18pF. From the RC time constant of 64ns the resistance associated with charging the column capacitance is calculated as 3.5kΩ. This is consistent with the measured resistance of the CMOS transmission gate, 2.7kΩ, and the resistance of signal lines within the column drive circuit, approximately 800Ω.
The increased display transmission which results from undercharging of the column capacitance can be overcome by increasing the amplitude of the video signal. However two other problems which result from the undercharging are still present. The extent to which the columns reach their correct voltage depends on the resistance of the transmission gate. Variations in the transistor characteristics from switch to switch show up as variations in the voltages applied to the columns of the display and result in vertical lines in the images displayed using row inversion. In addition, incomplete charging of the column capacitance means that the video information applied to one row of pixels will to some extent affect the voltages applied to the following row of pixels. This shows up as crosstalk of video information from one row of pixels to the row below it. To overcome these problems the column charging time or the width of the transistors in the transmission gates would need to be increased by a factor of approximately two.

The dependence of the resistance of the transmission gates within the multiplexer on the signal voltage is shown in Figure 5-57 and the offset voltage is shown in Figure 5-58. The maximum value of the resistance is approximately 20% higher than the value estimated from measurements of the mobility and threshold voltage of TFTs located close to the column drive circuit.

![Figure 5-57 Column driver transmission gate resistance](image-url)
The leakage of the transmission gates in the non conducting state is shown in Figure 5-59. This shows how the leakage current through the transmission gate varies with the mean level of the video signal for the case where the voltage across the switch is 10V. A leakage current of 4nA would result in a voltage change of 10mV during the video line period given the column capacitance of 13pF. The leakage current of the switch is well below this value.
5.6 Summary

The row drive circuits for active matrix liquid crystal displays operate at relatively low frequencies and can easily be designed using low temperature poly-Si TFTs. The main consideration in the design of the circuit is determining the size of the output transistors which are required to drive the capacitance of the rows of the display.

The column drive circuits operate at much higher frequencies than the row drivers and because the column voltages determine the transmission of the display they must be more accurately controlled. The type of column drive circuit which has been used in all production displays is based on multiplexing of the column data. In this circuit the TFTs are used purely as switches making the circuit tolerant of variations in device characteristics. The main indicator of the performance of the circuit is the number of parallel video inputs which are used to transfer the video information to the columns of the display. Four main factors influence the number of video lines which are needed, the column electrode time constant, the multiplexer switch resistance, the time constant of the video bus lines within the circuit and the propagation delays of the switch control signals. Analysis of these four aspects of the circuit operation forms the main part of the design of this type of column drive circuit. The disadvantage of having a large number of video inputs is the increase in the interconnect complexity and the increased complexity of the external circuits required to generate the parallel video signals.

A prototype datagraphic display with integrated row and column drive circuits has been designed to demonstrate the use of the PRL laser crystallised poly-Si technology for direct view AMLCDs. The display is one third of the height and width of a 6-inch VGA resolution display but operates at the speeds required for the full VGA display with an overall data rate of 25MHz. Good images with high contrast and good uniformity are obtained when the display is operated in field inversion. In line inversion the contrast and uniformity are reduced due to undercharging of the columns. This degradation in performance could be corrected by increasing the width of the transistors within the column multiplexing switches by a factor of two. Test multiplexers have been demonstrated which allow various aspects of the display, such as row and column electrode continuity, to be tested before the LC cell is completed.
6 Pixel Level Digital to Analogue Conversion

6.1 Introduction

In conventional active matrix LC displays the function of the pixel circuit is a very simple one, that is to sample the video information carried on the column electrodes and to hold that information on the LC display element until the pixel is addressed again. The ability to integrate TFT circuitry within the pixels of a display means that in principle more complex functions can be carried out at the pixel level. This chapter describes a method of addressing a display with digital video data by performing a simple digital to analogue conversion within each pixel of the display. The chapter starts with a brief description of a number of techniques which could be used for data conversion within the pixels. One of these techniques, serial charge redistribution, has been investigated in more detail and the remaining sections of the chapter are concerned with the design of the pixels and the results of measurements made on small pixel arrays.

Integration of a digital to analogue converter circuit within each pixel of the display offers a number of advantages compared to conventional pixel designs. The video information is supplied to the pixel in a digital form, which means that the column drive circuits for the display are digital rather than analogue circuits. Digital circuits, whether integrated onto the display using TFTs or in the form of conventional silicon circuits, are simpler to design and less demanding with respect to circuit layout and device uniformity than analogue circuits. In addition digital circuits are likely to be more compact than circuits containing analogue amplifiers, thus simplifying the layout of TFT drive circuits and reducing the area and cost of drivers produced using conventional silicon technologies. In some AMLCD applications, such as displays for personal and hand held computers, the video information is generated in a digital form. For these applications a display which accepts digital video data will require less external circuitry than one which requires an analogue video signal.

6.2 Pixel D/A Conversion Techniques

Of the many different techniques which can be used to perform a digital to analogue conversion, only a few can practically be implemented within the pixels of an active matrix LC display. In assessing the suitability of various conversion techniques, the
main issues which need to be considered are the availability of components within the existing AMLCD technology, the complexity of the circuitry which is integrated within each pixel, the increase in the number of addressing electrodes required and the impact this will have on the optical aperture of the display and the display yield.

Low temperature poly-Si technology allows the fabrication of both capacitors and resistors for use in converter circuits. Capacitors can be formed using the gate metal, gate oxide and n+ poly-Si layers. The gate oxide thickness is typically 150nm giving the structure a capacitance of $0.23 \text{fF}/\mu\text{m}^2$. While local variations in the capacitance due to oxide thickness non-uniformity will be small, variations over the area of the display substrate may be significant. The liquid crystal cell can also be used to form capacitors, but consideration must be given to the fact that the LC capacitance will exhibit both a voltage and a time dependence. Where capacitors of equal value or capacitors with a fixed ratio of values are required, it is important that the difference in the rms voltages appearing across the capacitors is small as this determines the dielectric constant of the liquid crystal.

The range of resistor values which can be fabricated using a standard low temperature poly-Si technology is limited by the thin film materials which are available. The aluminium, chrome and ITO layers typically have low resistances, 0.1-50 $\Omega/\square$ while the highly doped p+ and n+ poly-Si layers used for the source and drain contacts of the TFTs have higher resistance values, 100-300 $\Omega/\square$. The resistance of the doped poly-Si layers will reflect variations in the mobility of the poly-Si. For laser crystallised devices short range variations in the mobility are typically less than $\pm10\%$.

6.2.1 Converter Using Binary Weighted Capacitors

The use of capacitors with binary weighted values is well known in MOS digital to analogue converter circuits, and the same technique can in principle be used within a pixel converter circuit. An example of a 4-bit pixel circuit using binary weighted capacitors is illustrated schematically in Figure 6-1. The capacitors are formed by dividing the pixel electrode and the pixel storage capacitor to form a number of sub-pixels. It would not be practical to integrate an amplifier within each pixel of the display, therefore the converted voltage is formed directly on the capacitance of the liquid crystal pixel elements. The area and therefore the capacitance of each successive sub-pixel is reduced by a factor of two.
compared to the previous one, resulting in the required binary weighting. Each sub-pixel is connected to one of four column electrodes by an input TFT. The column electrodes carry binary voltage levels (D0 to D3) which represent the individual bits of the digital data. Three further TFTs, which are controlled by a second row electrode, are required to provide connection between the sub-pixels during the charge sharing period when the analogue voltage is generated.

The pixel is addressed by first applying the digital data to the four column electrodes. Then the voltage on Row n is taken high, turning on the input TFTs and allowing the sub-pixels to charge to the voltage level on the corresponding column. When charging is complete, Row n is taken to a low voltage again, turning off the input TFTs. Then Row n+1 goes high, turning on the second group of TFTs. Charge sharing takes place between the sub-pixels and the pixel voltage settles at a value which represents the binary weighted average of the voltages applied to the four columns.

![Diagram of a pixel with weighted capacitors](image)

**Figure 6-1 Pixel performing a conversion using weighted capacitors**

The complexity of this circuit is directly related to the resolution of the conversion. For an N-bit conversion the scheme requires an increase in the number of column electrodes by a factor N compared to a conventional pixel and an increase in the number of TFTs within each pixel by a factor of (2N-1). It also requires the pixel capacitance to be divided into N
binary weighted elements. Although each converter circuit requires connection to two row
electrodes, each of the row electrodes can be shared between two rows of pixels so that the
total number of row electrodes required for the display only increases by one compared to a
conventional display. The main issues for this design of pixel converter are its complexity
and the need to accurately subdivide the pixel electrode.

6.2.2 Serial Charge Redistribution Converter

A second converter which makes use of capacitors for charge scaling is the serial charge
redistribution converter.\cite{Suarez1975} The main advantage of this circuit is its simple
construction, requiring only two equal valued capacitors and two transistors. A diagram
illustrating a pixel converter circuit using serial charge redistribution is shown in Figure 6-2.
The capacitors are formed by dividing the pixel electrode and pixel storage capacitor into
two equal parts.

![Waveforms](image)

**Figure 6-2 Pixel using serial charge redistribution conversion**

Digital video data is applied in a serial form to the column electrode. The two TFTs are
controlled by two separate row electrodes. When a high level is applied to ROW-I the first
half pixel electrode is charged to the voltage level on the column electrode. Applying a high
level to ROW-S connects the two half pixel electrodes together allowing charge sharing to
take place. To perform a conversion, serial digital data is applied to the column electrode
with the least significant bit first, and the two pixel transistors are alternately switched to charge the first half pixel with the input data and then share the charge with the second half pixel. At the end of the conversion the voltage on the pixel electrodes represents the binary weighted average of the serial input data.

The fact that the circuit is a serial data converter means that its complexity does not increase with the resolution of the conversion. The same number of components are required for a 4-bit conversion and an 8-bit conversion. However, as the resolution of the conversion increases, the accuracy required of the values of the two capacitors and the number of charging cycles required to perform the conversion increase. The main differences between a conventional AMLCD pixel and this design are the need to accurately divide the pixel capacitance into two equal parts, the introduction of a second transistor within the pixel and the need to make connection to a second row electrode. As in the previous pixel converter design, it is possible to share row electrodes between two adjacent rows of pixels so that the total number of row electrodes is only increased by one compared to a conventional display.

6.2.3 Sampled Ramp Converter

Another converter circuit which is very simple in its structure and operation is the switched ramp converter.\cite{Lee1990} In this circuit a reference ramp waveform is applied to a capacitor via a switching transistor. The transistor is turned on at the start of the ramp and initially the voltage on the capacitor follows the changing reference voltage. At some point during the ramp the transistor is turned off and the reference voltage at that moment is held on the capacitor. The duration of the pulse used to switch the transistor is controlled by the value of the digital data. An example of a pixel circuit using a switched ramp converter is illustrated in Figure 6-3.

This circuit has the simplest structure of those considered so far. Two TFTs are required within the pixel but there is no subdivision of the pixel electrode. One of the two TFTs has its gate connected to the row electrode, and this device is used to select the row of pixels which is to be addressed. The second TFT has its gate connected to the column electrode which carries the pulse width modulated digital signal. A third electrode is required to provide the reference ramp waveform, and this electrode is common to all the pixels in the display. Advantages of this converter compared to the previous ones are that it is possible to
use a non-linear ramp waveform allowing the output voltage of the converter to be matched to the non-linear transmission verses drive voltage characteristics of the liquid crystal, and that the value of the pixel capacitance is not critical.

![Diagram of Pixel using sampled ramp conversion](image)

Figure 6-3 Pixel using sampled ramp conversion

The resolution of the converter is determined by the number of discrete time intervals in the pulse width modulated column signal. One interval is required for each value of digital code so that a 6-bit resolution would require 64 time intervals. A possible limit on the resolution which can be achieved will be determined by the time constant of the display’s column electrode. The maximum resolution of the converter will also depend on the accuracy with which the pixel voltage follows the reference ramp voltage while both pixel TFTs are conducting. In practice there will be a voltage dropped across the two transistors during the charging of the pixel which will result in an error in the converted voltage. This error will be dependant on the transistor characteristics, the slope of the reference ramp waveform and the pixel capacitance. Compared to a conventional pixel this design has one additional TFT and a reference voltage electrode.

6.2.4 Time Weighted Digital Signal

Repetitive pulse width or pulse density modulated digital signals can be converted to an analogue voltage by simply passing them through a low pass filter. This filter can be formed within the pixels of a display using the pixel capacitance and a resistor connected in series.
with the pixel TFT as indicated in Figure 6-4. The column drive signals for this display would consist of complex two level voltage waveforms which have a time averaged value corresponding to the value of the digital video data. The repetition frequency of the pulse width or pulse density modulated column signal must be significantly higher than the bandwidth of the low pass filter in order to limit the amplitude of the switching signal on the pixel electrode. Charging the column capacitance between the two data voltage levels will consume considerable power and this could be avoided by introducing a resistance in series with the column electrodes so that the columns form part of the low pass filter.

![Waveforms](image)

**Figure 6-4 Conversion using time averaging of a digital signal**

This technique has been used in the design of a digital column drive circuit[Hi Okada 1995] fabricated using a conventional CMOS IC technology. Although this is not strictly speaking a pixel level data conversion, since the converted voltage is formed on the column electrode, the fact that the columns are addressed with digital signals means that it shares the advantages of a display in which the data is converted within the pixel. The resolution of this converter will depend on the number of discrete timing intervals which can be defined within the pixel addressing period.
6.2.5 Subdivided Pixel

An approach which is similar to the converter using binary weighted capacitors but does not require as many TFTs, is to divide the area of the pixel to form a number of sub-pixels and to provide separate drive signals for each of these sub-pixel so that they can be individually set to a dark or light state. This pixel is illustrated schematically in Figure 6-5 for the case of a four bit conversion. It relies on the eye interpreting the average transmission of the group of sub-pixels rather than generating an analogue signal within the pixel. The sub-pixels have binary weighted areas and are set either dark or light depending on the state of the corresponding bits of the digital data. The average transmission of the group of pixels therefore reflects the value of the digital code. The pixel requires one column electrode and one transistor for each sub-pixel.

![Figure 6-5 Pixel with electrode divided into four binary weighted areas](image)

6.2.6 Resistor Ladder Network

A 3-bit pixel converter circuit using a resistive ladder network is illustrated in Figure 6-6. The digital data from the column electrodes is applied to the inputs of the resistor network via TFTs. When the pixel is to be addressed the digital data is set up on the columns and then the row electrode is taken to a high voltage to turn on the input TFTs. The pixel
capacitance is charged by the resistor network and it settles at a voltage which represents the binary weighted average of the column data. The resistance of the TFTs must be small compared to the resistors making up the network.

Achieving a suitable value for the resistors within the network is difficult. The doped poly-Si layers provide the highest sheet resistance; however, their resistance will be comparable to that of the TFTs. To achieve a satisfactory ratio of resistance between the TFTs and the network would either require the use of very wide transistors or long resistors. From the point of view of the aperture of the pixel neither of these options is attractive. For example the resistance of a minimum sized pixel transistor in a conventional laser crystallised poly-Si display is of the order of 100kΩ. Assuming that the resistors within the resistor network should be two orders of magnitude higher than this, then a resistance of 10MΩ is needed. This would require a p+ resistor with a length of about 100,000 squares. Integrating such large resistors within the area of the pixel is not practical using the existing AMLCD technology.

![Pixel converter using resistor network](image)

**Figure 6-6 Pixel converter using resistor network**

### 6.2.7 Review of Conversion Techniques

The optical aperture is an important performance parameter for transmissive active matrix LCDs since it has a direct impact on the efficiency of the display. It is possible to estimate
the effect that the various converter architectures will have on the display aperture by considering the pixel layout using some simple design rules. The main elements of a conventional AMLCD pixel are shown in Figure 6-7. The aperture of the pixel can be estimated by subtracting from the area of the pixel the area of those parts which are not transmissive. That is the column electrode, the row electrode, the TFT and the pixel storage capacitor. It has been assumed in these calculations that the pixel size is 190μm by 190μm, a size appropriate for a small monochrome direct view display. The row and column line widths are taken as 10μm and a line separation of 10μm is assumed. The area required for each part of the pixel has been calculated as a percentage of the total pixel area and these values are summarised in Table 6-1.

Figure 6-7 Components of a conventional AMLCD pixel

The calculations do not take into account crossing of the row and column electrodes which will tend to reduce the loss of aperture as the number of electrodes increases. In addition the calculations do not include any loss of aperture which is likely to result from dividing the pixel electrode into a number of smaller electrodes. This division would almost certainly require masking of the gap between the separate electrode elements in order to block unmodulated light which would otherwise reduce the displays contrast. The aperture
of the pixels using the various conversion techniques has been estimated and the results are summarised in Table 6-2. The advantage of employing a simple circuit for performing data conversion within the pixels of a display can be seen in these results. The serial charge redistribution, sampled ramp and time weighted converter pixels have estimated apertures close or equal to that of a conventional pixel. The conversions based on binary weighted capacitors and the sub-divided pixel approach carry a large penalty in terms of aperture, particularly as the resolution of the conversion is increased. The reason for this is that the converters use the digital data in a parallel form requiring extra column electrodes to carry the data to the pixels.

<table>
<thead>
<tr>
<th>Component</th>
<th>Area as percentage of total pixel area</th>
<th>First occurrence</th>
<th>Subsequent occurrences</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row electrode</td>
<td></td>
<td>5%</td>
<td>10%</td>
</tr>
<tr>
<td>Column electrodes</td>
<td></td>
<td>5%</td>
<td>10%</td>
</tr>
<tr>
<td>TFT</td>
<td></td>
<td>1.3%</td>
<td></td>
</tr>
<tr>
<td>Storage capacitor</td>
<td></td>
<td></td>
<td>12%</td>
</tr>
</tbody>
</table>

Table 6-1 Estimated area required for components used within pixels

<table>
<thead>
<tr>
<th>Conversion technique</th>
<th>For N-bit conversion per pixel</th>
<th>Estimated Aperture</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TFTs</td>
<td>Columns</td>
</tr>
<tr>
<td>Binary weighted capacitors</td>
<td>2N-1</td>
<td>N</td>
</tr>
<tr>
<td>Serial charge redistribution</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Sampled ramp</td>
<td>2</td>
<td>1~2</td>
</tr>
<tr>
<td>Time weighted</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Sub-divided pixel</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Conventional pixel</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 6-2 Estimated apertures for D/A converter pixels

Considering other aspects of the converter pixel performance, the highest conversion resolution is likely to be possible using the serial charge redistribution converter, assuming that capacitors with sufficient accuracy can be produced. The binary weighted capacitor and sub-divided pixel approaches are unattractive for higher resolutions because of the increase in circuit complexity and the need to accurately define small sub-pixel electrodes. The effect of the different pixel designs with respect to display yield is likely to reflect their complexity. From this point of view the time weighted conversion is most...
attractive while the sampled ramp and serial charge redistribution converters are likely to result in some yield reduction but less than the binary weighted capacitor and subdivided pixel converters. The binary weighted and sub-divided pixel converters are particularly unattractive when the external drive circuitry is considered because of the large number of additional signal connections required. The properties of the various conversion schemes are summarised in Table 6-3.

<table>
<thead>
<tr>
<th>Converter type</th>
<th>Aperture</th>
<th>Resolution</th>
<th>Yield</th>
<th>Driving</th>
</tr>
</thead>
<tbody>
<tr>
<td>Binary weighted capacitors</td>
<td>✗ ✗</td>
<td>✗</td>
<td>✗ ✗</td>
<td>✗ ✗</td>
</tr>
<tr>
<td>Serial charge redistribution</td>
<td>✗</td>
<td>✗ ✗</td>
<td>✗</td>
<td>✓</td>
</tr>
<tr>
<td>Sampled ramp</td>
<td>✗</td>
<td>✓</td>
<td>✗</td>
<td>✓</td>
</tr>
<tr>
<td>Time weighted</td>
<td>O</td>
<td>✓</td>
<td>O</td>
<td>✓</td>
</tr>
<tr>
<td>Sub-divided pixel</td>
<td>✗ ✗</td>
<td>✗</td>
<td>✗ ✗</td>
<td>✗ ✗</td>
</tr>
</tbody>
</table>

Table 6-3 Summary of conversion methods

6.3 Matrix Addressing of NMOS Serial D/A Converter Pixels

This section describes in more detail the operation of the serial charge redistribution converter, the way in which it can be implemented within a pixel and how the pixels can then be combined in a matrix to form a display.

The circuit which is normally used to perform a serial charge redistribution conversion is shown in Figure 6-8. It consists of three switches and two equal valued capacitors. The waveforms below the circuit illustrate the sequence of events required to perform a conversion. At the start of the conversion any charge on the capacitor C2 is first removed by closing the switch S3. There then follow a number of charging and charge sharing cycles during which a serial digital code is applied to the input of the converter. A voltage, $D_1$, representing the least significant digit of the code is first applied to the input, then the switch S1 is closed and C1 charged to the input voltage level. Then S1 is opened and S2 is closed and the charge on C1 and C2 redistributes until the voltage on the two capacitors equalises; switch S2 then opens again.
This sequence of charging $C_1$ with a voltage representing one bit of the digital data and then sharing the charge with the second capacitor is repeated for each bit of the data in turn. Since $C_1$ and $C_2$ are of equal value, the effect of the charge sharing is to scale the input signal by a factor of $\frac{1}{2}$ each time that the sharing takes place. At the end of the conversion the voltage on the two capacitors represents a sum of the input data scaled by decreasing powers of $\frac{1}{2}$.

Suarez, Gray and Hodges indicated that the voltage on the capacitors at the end of an N-bit conversion can be described by an expression of the form.

$$V_{out}(N) = \sum_{i=1}^{N} D_i \left( \frac{1}{2} \right)^{(N-i+1)}$$  \hspace{1cm} (6-1)

In implementing the serial charge redistribution converter within the pixels of an active matrix display it is important to minimise the complexity of the circuit. Figure 6-9 shows an equivalent circuit for a single pixel in such a display. As only two transistors are used in the circuit, resetting of the voltage on $C_2$ before a conversion starts can be achieved by simultaneously turning on T1 and T2. This is carried out during an additional reset period when the input signal is set at the level representing a logic zero. The two equal capacitors, $C_1$ and $C_2$, are formed by dividing the pixel capacitance into two equal parts. Since most AMLCDs use pixel storage capacitors $C_1$ and $C_2$ are made up of a component due to the liquid crystal, $C_{LC}$, and a contribution from the storage capacitor, $C_S$. 

155
The signals required to control the conversion are fed to the pixels via row and column addressing electrodes. The digital input data is supplied by simply connecting the input of the pixel circuit to the adjacent column electrode. Two separate gate drive signals are required to control the conversion process. These could be provided by having two separate gate lines for each row of pixels in the display; however, such an increase in complexity would be undesirable. Instead, each gate line is used to control the transistors in two adjacent rows of pixels using the matrix arrangement illustrated in Figure 6-10.

In this arrangement the first transistor in each pixel is connected to the row electrode above the pixel and the second transistor to the row electrode below. Examples of the waveforms required to address the rows for an 8-bit pixel conversion are shown in Figure 6-11. At the start of each conversion one period is allowed for resetting the voltage on the pixel capacitors during which both pixel TFTs are turned on. Then eight data conversion periods follow as successive bits of the digital video data are applied to the column electrode.

The fact that each row is shared between two pixels has two consequences. Firstly the second transistor within each pixel will be switched during the row addressing period immediately following the conversion. This does not cause any problems since the first pixel TFT remains turned off during this period and therefore there will be no net transfer of charge to or from C1 and C2. Secondly the vertical scan direction of the display cannot be reversed with this pixel arrangement. Switching of the scan direction is sometimes required when displays are used in projection systems where the optical components of the projector invert the image on the display. With the matrix arrangement shown in Figure 6-10, reversing the scan direction would mean that T1 was turned on after the conversion had been completed resulting in an incorrect voltage on C1.
Figure 6-10 Matrix of NMOS D/A converter pixels

Figure 6-11 Row addressing waveforms for 8-bit pixel conversion
6.4 CMOS Serial D/A Converter Pixels

Conventional active matrix LC displays use transistors of only one type, normally NMOS, within the active matrix of the display. However, with poly-Si technologies both NMOS and PMOS transistors can be fabricated. This provides an opportunity for overcoming one of the limitations of the matrix arrangement illustrated in Figure 6-10, that is the fact that the vertical scan direction of the array cannot be reversed.

During the conversion process the two TFTs within the pixel are switched so that either one or the other device is turned on. This operation can be achieved very simply if one of the devices is an n-type TFT and the other is a p-type transistor. Figure 6-12 illustrates a new matrix structure in which a single row connection can be used to control the conversion process.

![Figure 6-12 CMOS D/A pixel array](image)

The first TFT within each pixel is an n-type device which is turned on by taking the row voltage to a positive potential. The second TFT is a p-type device which has its gate connected to the same row electrode as the first TFT. This second device is turned on by applying a negative voltage to the row. As each row electrode is associated with only one row of pixels it is possible to reverse the direction of the scanning signals on the rows without affecting the operation of the pixel conversion. The choice of an n-channel TFT as the first transistor in the pixel circuit reflects the superior leakage performance of these devices compared to the p-channel transistors. This first transistor is required to maintain the voltage on the pixel capacitance throughout the video field period, whereas the second TFT is only required to isolate the two halves of the pixel during the conversion process.
The use of a single control signal with both n-channel and p-channel devices to achieve a complementary switching action is similar to techniques for single phase clocking which have been developed for conventional silicon CMOS logic circuits. [Yuan 1989]

Figure 6-13 Addressing waveforms for CMOS pixel circuit

One consequence of the use of n-type and p-type TFTs is that both devices cannot be turned on at the same time to reset the voltages on the pixel capacitors at the start of the conversion. An alternative method of resetting the pixel voltage must be adopted. Figure 6-13 illustrates the row waveforms which are used with this array structure.Resetting of the pixel is achieved by setting the column voltage at the reset level and then switching the row signal between the high and low levels a number of times. When the row voltage is high, the first half of the pixel is charged to the reset level, then when the row voltage goes to the low level, the charge is shared with the second half of the pixel. Each charging and sharing cycle reduces the difference between the reset level and the pixel voltage by a factor of two.

It is possible to calculate the maximum error which results from resetting the pixel voltage in this way. In the case where the pixel voltage is reset to the low data level, V(0), the maximum initial voltage difference between the pixel and the reset level is equal to the maximum peak to peak drive voltage of the liquid crystal, $V_{bb}$. It should be noted that the voltage error at the end of the conversion will be reduced in magnitude by a factor $1/2^N$ compared to the value at the start due to the charge sharing that takes place during the conversion. The voltage error due to the initial pixel voltage after R reset charging cycles and N conversion cycles is given by the following equation.
This equation can be rearranged to give the number of reset cycles required for a given voltage error.

\[
R = \frac{\log\left(\frac{V_{bb}}{V_{reset\_error}}\right)}{\log(2)} - N
\]

To illustrate this calculation, consider the case where the voltage error at the end of the conversion resulting from the initial pixel voltage should be less than 12mV; this represents an error in the pixels transmission of approximately 0.5%. A typical value for \(V_{bb}\) is 10V, therefore it is required that \(R \geq 9.7-N\) so that for an 8-bit conversion two reset cycles are needed. This multiple reset method can also be applied to the NMOS pixels by appropriately modifying the row voltage waveforms.

### 6.5 Pixel Charging Time

The time which is available to perform a data conversion within the pixels is determined by the standard of the video signal which is being displayed. For a full resolution television display the time available to address each row is only half the video line period, typically about 30\(\mu\)s. Within this period the voltages on the two pixel capacitors must first be reset and then the first capacitor must be charged to the digital input level and the charge shared with the second capacitor \(N\) times for an \(N\) bit conversion. The time required for these operations depends on the pixel capacitance, the TFT characteristics and the voltage levels of the column data and the row drive waveforms. In this section the time required to perform a conversion using an NMOS pixel will be considered and two methods for increasing the available conversion time are described.

The charging performance of the pixel converter circuit will depend on the data voltages applied to its input. These must be matched to the drive requirements of the liquid crystal which are illustrated in Figure 6-14.
One of the features of the drive waveform required by the liquid crystal is that the polarity of the signal must be inverted each time that the pixel is addressed. For the converter pixels this could be achieved digitally by setting the voltage range of the converter to the maximum drive voltage required by the liquid crystal, twice the saturation voltage. The pixel voltage polarity could then be inverted by performing a logical inversion of the digital data applied to the column electrodes. The disadvantage of doing this is that a higher conversion resolution is required to achieve a given minimum voltage step within the pixel. A better approach is to change the voltages representing high and low digital data which are applied to the columns of the display. This method is illustrated in Figure 6-14.

When the pixel is to be addressed with a positive voltage, the voltage levels applied to the columns of the display are set at $+V(0)$ for a low data bit and $+V(1)$ for a high data bit. To address the pixel with a negative voltage the polarity of the data voltages is reversed so that $-V(0)$ is used for a low data bit and $-V(1)$ for a high data bit. The resulting voltage waveforms appearing on the pixel are illustrated for high and low values of digital code.

There are two distinct operations which take place during the digital to analogue conversion within the pixel. In one of these the first pixel capacitor is charged via the first TFT to a
voltage level determined by the signal on the column electrode. In the second operation the second TFT allows charge to redistribute between the two pixel capacitors. The time required to perform these two operations can be calculated by assuming that the electrical characteristics of the TFTs can be represented by the basic equations describing the conduction of a MOS transistor. It is shown in Appendix A that the time taken for the TFT to charge a capacitor $C$ from an initial voltage $V_i$ to a final voltage $V_T-V_u$, where $V_2$ is the column voltage and $V_u$ is the undercharging voltage, is given by the equation

$$T_{ch} = \frac{C}{BV_{gon}} \log \left[ \frac{2V_{gon}}{V_u} + 1 \right] \frac{V_u}{V_2 - V_1}$$

$6-4$

$B$ is the transconductance parameter of the TFT and $V_{gon} = V_g - V_T - V_2$. This equation can be used to determine the time required to charge the first pixel capacitor to the level of the column data. A similar expression can be derived for the time required for the voltages on two equal value capacitors, initially $V_1$ and $V_2$, to equalise to within a certain error voltage, $V_{eq}$. In this case the parameter $V_{gon} = V_g - V_T - (V_1 + V_2)/2$.

$$T_{ch} = -\frac{C}{2BV_{gon}} \log \left[ \frac{2V_u}{V_2 - V_1} \right]$$

$6-5$

This second equation can be used to determine the time required for the charge sharing to take place between the two pixel capacitors. In both equations the charging times depends on both the initial pixel voltage and the final pixel voltage. A useful way to view this dependence is by using a contour plot of the charging time.

The function $T_{ch}B/C$, the normalised charging time, has been plotted in Figure 6-15 as a function of the voltage applied to the column electrode and the voltage initially present on the first pixel capacitor. It has been assumed that the gate voltage of the TFT in the on state is equal to $V_T+8V$ and the charging time has been calculated for a final voltage error of $V_u=10mV$. The range of column voltages which are used to address the display are matched to the LC characteristics and can be superimposed on the plot of the normalised charging time. Consider as an example the charging of a pixel in a conventional AMLCD.
The column voltage in a conventional active matrix display will have a value which lies between the threshold and saturation voltages of the liquid crystal. A typical value for the threshold voltage would be $2V_{\text{rms}}$ and for the saturation voltage $5V_{\text{rms}}$. Each time that the pixel is addressed the polarity of the drive voltage is reversed so that when the pixel is first addressed the column voltage may lie within the range $+2V$ to $+5V$. The next time that the pixel is addressed the column voltage will lie between $-2V$ and $-5V$.

The operating region of the pixel when superimposed on Figure 6-15 therefore consists of two squares. When the pixel is addressed with a positive voltage during the positive video field period the column voltage will lie between $+2V$ and $+5V$ while the initial pixel voltage will be negative, lying between $-2V$ and $-5V$. When the pixel is addressed with a negative voltage during the negative video field period the column voltage will be between $-2V$ and $-5V$ while the initial pixel voltage will be positive, lying between $+2V$ and $+5V$.

Figure 6-15 Normalised pixel charging time $T_{\text{ch}}B/C$ for n-type TFT generated using equation 6-4
The operating regions of the converter pixel differ from the conventional one. The column voltage has four possible values, \(+V(0)=+5\text{V}\), \(+V(1)=+2\text{V}\), \(-V(0)=-5\text{V}\) and \(-V(1)=-2\text{V}\), corresponding to the data logic levels in positive and negative field periods. The operating region of the pixel consists of six horizontal lines. Two of these represent the resetting of the pixel voltage before the conversion starts. It is assumed here that the pixel is reset to the low data level, either \(+V(0)\) or \(-V(0)\). The voltage initially present on the pixel during the reset phase will be of the opposite polarity to the column voltage and will lie between the threshold and saturation values of the liquid crystal. For example, if the column voltage is \(+V(0)\) then the initial pixel voltage will lie between \(-2\text{V}\) and \(-5\text{V}\). During the rest of the conversion the initial pixel voltage and the column voltage will be of the same polarity. The initial pixel voltage will again lie within the range of \(2\text{V}\) to \(5\text{V}\) or \(-2\text{V}\) to \(-5\text{V}\).

A number of observations can be made from Figure 6-15. For both the conventional and converter pixels the charging times for negative column voltages, during the negative field period, are shorter than for positive voltages. This is because the NMOS TFTs have a lower gate-source voltage when the column voltage is positive, and as a result the positive field period is more important in determining the minimum charging time required by the pixels.

For the converter pixel the resetting of the pixel voltage to \(+V(0)\) requires the greatest charging time with a normalised value of 1.98, equal to the maximum normalised charging time for the conventional pixel. It is worth noting that the time required to reset the pixel voltage can be reduced if the pixel is reset to a voltage of \(+V(1)\) rather than \(+V(0)\). The normalised charging time in this case would have a maximum value of only 1.02.

Following the reset phase, subsequent charging of the first half of the pixel to one of the two data voltage levels requires less time since the difference between the initial pixel voltage and the column voltage is relatively small. The maximum value of the normalised charging time for this part of the conversion is 1.77, and it occurs when the initial pixel voltage is \(+2\text{V}\) and the column voltage is \(+5\text{V}\).

The second operation which must be considered in evaluating the charging time requirements for the converter pixels is the charge sharing. Figure 6-16 shows the normalised charging time for the charge sharing operation as a function of the initial voltages on the two pixel capacitors. The operating regions for the converter pixel are indicated by the
four vertical lines. The initial voltage on first pixel capacitor, $C_1$, has only four possible values corresponding to the four column voltage levels. The maximum value of the normalised charge sharing time is approximately 0.58 and occurs when $C_1$ or $C_2$ is charged to the most positive voltage level.

![Operating Regions for D/A Pixels](image)

**Figure 6-16 Normalised pixel charge redistribution time $T_{CB}/C$ for n-type TFT generated using equation 6-5**

From these plots it is possible to compare the charging time requirements of the converter pixel to the conventional pixel. It is assumed that the TFTs in the converter pixel have the same dimensions as in the conventional pixel, that the capacitance of each half of the converter pixel is half the value of the conventional pixel capacitance and that the second transistor of the converter is an n-channel device. The results are summarised in Table 6-4.

<table>
<thead>
<tr>
<th></th>
<th>Reset</th>
<th>Data</th>
<th>Share</th>
<th>Total Time</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1.98</td>
<td>0</td>
<td>1.98</td>
</tr>
<tr>
<td>Conventional pixel</td>
<td>1.98</td>
<td>1.77/2</td>
<td>0.58/2</td>
<td>6.68 9.03 11.38</td>
</tr>
<tr>
<td>Converter pixel reset to data 0</td>
<td>1.02</td>
<td>1.77/2</td>
<td>0.58/2</td>
<td>5.72 8.07 10.42</td>
</tr>
<tr>
<td>Converter pixel reset to data 1</td>
<td>1.02</td>
<td>1.77/2</td>
<td>0.58/2</td>
<td>5.72 8.07 10.42</td>
</tr>
</tbody>
</table>

**Table 6-4 Estimated relative charging times for conventional and converter pixels**
These results illustrate that the converter pixels are considerably more demanding of the TFTs charging ability than a conventional pixel design. The charging time required for a 4-bit conversion is more than three times that of the conventional pixel, while that required to perform an 8-bit conversion, the resolution needed for high quality video displays, is more than five times greater. There are however two techniques which can be employed to allow the time available to perform the conversion to be increased. The first method, which is described in the following section, is to multiplex the data applied to the column electrodes of the display. The second method, described in section 6.5.2, is to reduce the number of cycles required to perform the conversion by increasing the number of column voltage levels.

### 6.5.1 Multiplexed Column Data

If the row addressing period of the display is $T_{row}$ and assuming that equal time is allocated for charging and charge sharing within the pixel, then the maximum available charging time for each data input period of the converter is $T_{row}/(2N+2)$. During the serial D/A conversion digital data only needs to be present at the input of the converter during half of each conversion clock cycle, the period when the first TFT is turned on. We can take advantage of this fact by multiplexing the digital information on the column electrodes of the display so that they carry the data for pixels in two adjacent rows in an interleaved form. This approach is illustrated in the waveforms of Figure 6-17 where the gate and column signals required to address two NMOS pixels, a and b, are shown.

![Figure 6-17 Multiplexing of column data for two pixel conversions](image-url)
The conversion starts with the voltages on the two pixels being simultaneously reset. Then the least significant bit of the data for pixel \( a \), \( D_{1a} \), is applied to the column and the first transistor of pixel \( a \) is turned on. When charging is complete the transistor is turned off and the column data is changed to the least significant bit of the data for pixel \( b \), \( D_{1b} \), and the first transistor of pixel \( b \) is turned on. The process is repeated for each bit of the digital data in turn to complete the conversions.

Multiplexing the data on the column in this way allows the charging time of the pixels to be almost doubled to a value of \( 2T_{\text{row}}/(2N+3) \) since it is now possible to spread the conversion for the pair of rows over two row addressing periods. The number of charging periods becomes \( 2N+3 \) rather than \( 2N+2 \) as an additional charge sharing period is required for the second pixel at the end of the conversion. A disadvantage of adopting this technique is that there is an increase in the complexity of the display control circuit which must generate the interleaved digital data.

### 6.5.2 Multilevel Column Data

An \( N \)-bit conversion using two level input data requires \( N \) input data charging and charge sharing cycles to complete the conversion. This number can be reduced if the number of discrete voltage levels applied to the input of the converter is increased. Two possible schemes for reducing the number of charging cycles are presented here. In the first scheme, simultaneous bit conversion, the additional input voltage levels allow two or more bits of the digital data to be converted simultaneously. In the second scheme, the output voltage range of the converter is divided into a number of smaller intervals which are selected according to the most significant bits of the data.

Consider first the simultaneous bit conversion approach. In general if \( 2^M \) input voltage levels are used and there are \( N \) conversion cycles then the overall conversion resolution is \( MN \). Consider an example where an overall conversion with a resolution of 8-bits is needed. The possible combinations for the number of input voltage levels and the number of charging cycles is given in Table 6-5. The conversion could be achieved by carrying out an eight bit serial conversion using two level input data and requiring eight data charging periods. Alternatively the number of charging cycles could be reduced to 4 if four level input data were used in a simultaneous bit conversion scheme. The relative values of the input voltage levels required when two, four, eight and sixteen separate data levels are used are
summarised in Table 6-6. The values needed depend on the number of conversion cycles, N, of the serial digital to analogue conversion. The way in which the digital video data is used to select one of the column voltage levels for conversions where four or sixteen column data levels are used is illustrated schematically in Figure 6-18 for the case of eight bit video data.

<table>
<thead>
<tr>
<th>Column Voltage Levels</th>
<th>Data Charging Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2^8 = 256$</td>
<td>1</td>
</tr>
<tr>
<td>$2^4 = 16$</td>
<td>2</td>
</tr>
<tr>
<td>$2^2 = 4$</td>
<td>4</td>
</tr>
<tr>
<td>$2^1 = 2$</td>
<td>8</td>
</tr>
</tbody>
</table>

Table 6-5 Combbinations of column levels and charging cycles for an 8-bit conversion

<table>
<thead>
<tr>
<th>2-level data</th>
<th>4-level data</th>
<th>8-level data</th>
<th>16-level data</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$1 + 2^N$</td>
<td>$1 + 2^N + 2^{2N}$</td>
<td>$1 + 2^N + 2^{2N} + 2^{3N}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1 + 2^N$</td>
<td>$1 + 2^N + 2^{3N}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1 + 2^{2N}$</td>
<td>$1 + 2^{2N} + 2^{3N}$</td>
</tr>
<tr>
<td>0</td>
<td>$2^N$</td>
<td>$2^N + 2^{2N}$</td>
<td>$2^N + 2^{2N} + 2^{3N}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2^N$</td>
<td>$2^N + 2^{3N}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2^{2N}$</td>
<td>$2^{2N} + 2^{3N}$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>$2^{3N}$</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 6-6 Values of multilevel digital data for an N-bit simultaneous bit conversion scheme

With four level column signals the upper and lower four bits of the 8-bit video data are effectively processed in parallel with corresponding bit pairs being used to select the column voltage. For example the least significant bits, $B_5$ and $B_6$, are used to select the first column voltage level of the conversion. In the second period $B_6$ and $B_2$ control the column voltage in the third $B_7$ and $B_3$ and the fourth $B_8$ and $B_4$. 

168
A similar method is used to select the appropriate data voltage when sixteen voltage levels are used, but in this case two groups of four data digits are used to select one of the sixteen voltage levels as shown in Figure 6-18. A circuit arrangement for implementation of the conversion using four bit four level data is illustrated on the left of Figure 6-19. The number of conversion cycles is reduced by a factor of two at the cost of doubling the number of voltage selection switches and introducing a 2 to 4 line decoder to control the switches.

**Figure 6-19 Circuits for simultaneous bit conversion and divided range conversion**
In the second approach to reducing the number of cycles required to perform a conversion the output voltage range is divided into a number of separate intervals, 2, 4, 8 or 16, which are defined by a set of reference voltages. This technique is sometimes used with conventional digital to analogue converters in order to increase their output voltage resolution. The circuit requirements of this scheme are illustrated on the right of Figure 6-19. In the divided range conversion the most significant bits of the digital data are used to select a pair of reference voltage levels. One of these two levels is then applied to the input of the converter according to the state of the less significant bits of the data. As the most significant bits of the data are used to select the output voltage range, the number of bits used in the serial data conversion is reduced. If the output voltage range is divided into $2^M$ intervals and the serial digital to analogue conversion has a resolution of $N$ bits, then the overall conversion resolution is $M+N$ bits. For example, to perform a conversion with an overall resolution of 8 bits a serial conversion of the 6 least significant bits of the data could be performed with the 2 most significant bits of the data being used to select one of four output voltage ranges.

Compared to the simultaneous bit conversion scheme, the divided range approach does not provide as great a reduction in the number of charging cycles of the serial converter. In the example shown in Figure 6-19 the number of cycles is reduced from 8 to 6 for the divided range approach compared to a reduction from 8 to 4 for the simultaneous conversion. Dividing the output voltage range of the converter in this way does, however, offer the possibility of generating a non-linear output voltage which can be matched to some extent to the characteristics of the liquid crystal.

### 6.6 Pixel Capacitor Accuracy

In considering the pixel data conversion it has so far been assumed that the two halves of the pixel can be made to have exactly equal capacitance. In practice this is unlikely to be the case and it is therefore important to consider the consequences of errors in the capacitor values. A simple analysis of the errors which result from the effect of the parasitic capacitances of the TFTs and mismatch in the values of the pixel capacitors is presented in the following section. This is then used to estimate the accuracy required for the capacitance of the two halves of the pixels.
The pixel voltage at the end of a conversion can be estimated by considering the sequence of events which occur during the conversion process. The ith conversion cycle is started by the first transistor, T1 of Figure 6-9, being turned on and C1 being charged to the input voltage level, \( V_i \). Assuming that the capacitor charges fully, then the difference between the input voltage and the value of \( V_i \) after T1 turns off is due only to the charge released from the channel of T1 as the gate voltage falls. For simplicity it is assumed that the transistors have a self aligned gate structure and that the gate drain capacitance can be neglected when the device is not conducting. The effects of charge injection when a MOS transistor is turned off have been described amongst others by Wegmann et. al.\[^{171}\] As the transistor turns off, the charge within the channel is removed to either the source or drain terminal of the device. The way in which the charge is divided depends on a number of factors including the rate at which the gate voltage falls and the impedance at the source and drain terminals. For the purposes of this simple analysis it is assumed that the charge divides in such a way that a fraction \( K_{q1} \) of the channel charge is transferred to the drain of the device and onto capacitor C1. The voltage on C1 after T1 turns off can then be calculated.

\[
V_1(i) = V_i - \frac{K_{q1} \left(V_g - V_T - V_i\right) C_{g1}}{C_1} \quad 6-6
\]

\[
V_1(i) = V_i \left(1 + \frac{K_{q1} C_{g1}}{C_1}\right) - \left(V_g - V_T\right) \frac{K_{q1} C_{g1}}{C_1} \quad 6-7
\]

The next event in the conversion cycle is for T2 to turn on and for charge sharing to occur between C1 and C2. The voltage on C1 and C2 at the end of the charge sharing can be calculated by equating the charge present before and after charge sharing. \( V_2* \) represents the voltage on C2 after charge sharing has taken place but before T2 turns off.

\[
V_1(i) C_1 + V_2(i+1) C_2 = V_2*(i) (C_1 + C_2) + \left(V_2*(i-1) - (V_g - V_T)\right) C_{g2} \quad 6-8
\]

\[
V_2*(i) = \frac{V_2(i-1) C_2 + V_1(i) C_1 + \left(V_g - V_T\right) C_{g2}}{C_1 + C_2 + C_{g2}} \quad 6-9
\]

When T2 turns off at the end of the charge sharing period, charge will be released from its channel and this will again divide between the source and drain terminals. Assume that a fraction \( K_{q2} \) of the total charge is transferred onto C2, then the voltage on C2 at the end of the conversion clock cycle is given by the following expressions.
Using equations 6-7, 6-9 and 6-11 the final voltage on C2 can be related to the input voltage level. Three parameters, $K_1$, $K_2$ and $K_3$ are introduced in order to simplify the expression.

$$V_2(i) = V_2(i) - K_{q2}(V_g-V_T-V_2(i)) \frac{C_{g2}}{C_2}$$ \hspace{1cm} 6-10

$$V_2(i) = V_2(i) \left(1 + \frac{K_{q2}C_{g2}}{C_2}\right) - (V_g-V_T) \frac{K_{q2}C_{g2}}{C_2}$$ \hspace{1cm} 6-11

The output voltage of the converter after an N-bit conversion can be derived from 6-12 and is given by the equation below.

$$V_{out} = \sum_{i=1}^{N} V_i K_2 K_1^{(N-i)} - (V_g-V_T) K_3 K_1^{(N-i)}$$ \hspace{1cm} 6-16

This equation illustrates a number of points concerning the accuracy of the conversion. The voltage generated at the end of the conversion consists of two components, one of which is dependent on the digital input code and the other which is not. The second term acts as a constant offset error, the magnitude of which depends on the gate voltage applied to the TFTs, on the parameters $K_1$ and $K_3$, and on the number of conversion cycles, $N$. Considering the code dependant term of the output voltage, the parameter $K_2$ acts as a scaling factor determining the gain of the conversion. The gain is also affected by the value of $K_1$; but more importantly $K_1$ determines the linearity of the conversion. Each bit of the input digital data is scaled by powers of $K_1$ during the conversion process. The ideal value of $K_1$ is $\frac{1}{2}$ which is achieved if $C_1$ and $C_2$ are equal and the gate capacitance of T2 is negligible.
expressed in terms of the ideal step for a change in the least significant bit (LSB) of the digital code. The visual effect of a high value of differential non-linearity would be the presence of contouring in grey scale images. For the serial charge redistribution conversion the worst case transition occurs when the code changes from one where all but the most significant bit are 1 to the case where only the most significant bit is 1. That is from code 111...110 to code 000...001. For an N-bit conversion the DNL can be calculated from the expression below where \( V_{n} \) represents the output voltage for a digital input code \( n \).

\[
DNL = \left( V_{2^{(n-1)}} - V_{2^n} \right) - \frac{2^N - 1}{V_{2^n} - V_{0}} - 1 \tag{6-17}
\]

\[
DNL = \left( 1 - \sum_{i=1}^{N} K_i^{(n-j)} \right) \cdot \left( 2^N - 1 \right) - 1 \tag{6-18}
\]

Similarly expressions can be derived for conversions using the simultaneous bit conversion scheme by taking into account the different values of input voltage, for example the DNL for a conversion with four level data is given by the equation below.

\[
DNL = \left( 1 - \left( \frac{1}{2^N} + \sum_{i=1}^{N} \left( 1 + \frac{1}{2^N} \right) K_i^{(n-j)} \right) \right) \cdot \left( 2^N - 1 \right) - 1 \tag{6-19}
\]

The variation of the differential non-linearity for 8-bit, 6-bit, 4-bit and a 2x4-bit conversions as a function of \( K_1 \) is shown in Figure 6-20. Taking a limit for the acceptable differential non-linearity of \( \pm 1/2 \) LSB, the range of acceptable values for \( K_1 \) can be determined. From these figures the tolerance required for the values of \( C_1 \) and \( C_2 \) can also be calculated if the effect of the TFT gate capacitance is assumed to be negligible. The results are summarised in Table 6-7. As the resolution of the conversion is increased the value of \( K_1 \) must be controlled more accurately. The 2x4-bit conversion allows a slightly greater error in the capacitor values than the 8-bit conversion. The need to control the relative values of \( C_1 \) and \( C_2 \) to 0.2% or better is quite demanding, and in practice the accuracy of \( C_1 \) and \( C_2 \) may limit the conversion resolution that can be achieved. In conventional MOS processing capacitor ratios with standard deviations in the range 0.02% to 0.3% can be achieved allowing conversion resolutions of 8 bits or more.
### Table 6-7 Values of capacitor tolerance giving a differential non-linearity of ±½ LSB

<table>
<thead>
<tr>
<th>Conversion resolution</th>
<th>Value of $K_1$ for ±½ LSB DNL</th>
<th>Capacitor tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-bit</td>
<td>0.5 ± 0.0010</td>
<td>± 0.20%</td>
</tr>
<tr>
<td>2x4-bit</td>
<td>0.5 ± 0.0013</td>
<td>± 0.26%</td>
</tr>
<tr>
<td>6-bit</td>
<td>0.5 ± 0.0043</td>
<td>± 0.86%</td>
</tr>
<tr>
<td>4-bit</td>
<td>0.5 ± 0.021</td>
<td>± 4.2%</td>
</tr>
</tbody>
</table>

In this simple analysis of the conversion errors it was assumed that the TFTs had negligible gate-drain and gate-source overlap capacitance. However, the effect of the overlap capacitance on the converted voltage is quite straightforward. Firstly the overlap capacitance must be taken into account when calculating the values of $C_1$ and $C_2$. If the two transistors are of equal size and have a gate-drain overlap capacitance of $C_{o1}$ this means that the value of $C_2$ is increased by $C_{o1}$ while $C_1$ is increased by $2C_{o1}$. This difference in capacitance must be considered during the pixel design and can be compensated for by increasing the overlap length on one side of the second transistor, $T_2$, so that $C_1$ and $C_2$ are equal. The second effect of the overlap capacitance is to introduce an additional offset into the value of the converted voltage due to coupling of the switching signals on the gates of the two transistors. This offset is similar to the offset voltage normally present in the pixel of a conventional display caused when the pixel transistor turns off, and does not raise any additional issues.
6.7 Input Data Weighting

It is possible to correct for errors due to mismatch in the values of C1 and C2 by weighting the input voltages applied to the converter. This weighting is carried out by changing the voltages representing high and low digital data as each successive bit is fed to the converter. A limitation of this technique is that where multiple converters are being operated in parallel, for example within the pixels of an active matrix display, its use is only practical if the same errors are present within each circuit. The ability to correct for errors in the value of \( K_1 \) can be illustrated by replacing the input voltage levels, \( V_i \), by weighted values, \( V_{wi} \), described by the expression 6-20.

\[
V_{wi} = V_i \cdot W^{(N-i)}
\]  

The output voltage at the end of the conversion now becomes

\[
V_{out} = \sum_{i=1}^{N} V_{wi} \cdot K_2^{(N-i)} - (V_g - V_T) K_3 K_1^{(N-i)}
\]  

If the value of the weighting factor is chosen to make \( W K_1 \) equal \( \frac{1}{2} \) then the non-linearity introduced by errors in the value of \( K_1 \) is eliminated from the expression for output voltage.

\[
V_{out} = \sum_{i=1}^{N} V_i \cdot W^{(N-i)} K_2^{(N-i)} - (V_g - V_T) K_3 K_1^{(N-i)}
\]  

If the value of the weighting factor is chosen to make \( W K_1 \) equal \( \frac{1}{2} \) then the non-linearity introduced by errors in the value of \( K_1 \) is eliminated from the expression for output voltage.

\[
V_{out} = \sum_{i=1}^{N} V_i \cdot K_2 \left( \frac{1}{2} \right)^{(N-i)} - (V_g - V_T) K_3 K_1^{(N-i)}
\]  

6.8 Converter Circuit Using Discrete Capacitors and TFTs

The basic operation of the pixel digital to analogue conversion has been demonstrated by assembling the pixel circuit of Figure 6-9 using two separate SPC poly-Si TFTs and two discrete capacitors. The TFTs are large test devices (W/L = 1000\( \mu \)m/6\( \mu \)m) and the capacitance values have been scaled up (C1 \( \approx \) C2 \( \approx \) 55pF) to give a comparable charging time to that of a real pixel.
The waveforms used to control the circuit are shown in Figure 6-21. During the first two periods of the conversion the gates of both transistors are taken high and the input voltage is held at a low level in order to reset the voltages on the capacitors. Then the two gates are alternately taken to the high level to perform the conversion. The digital code represented by the input data waveform is 255 and waveforms with and without weighting of the data are shown. The choice of the value of 1.062 for the weighting factor will be described shortly. The voltage waveforms appearing at the two nodes of the converter circuit are also shown, illustrating the processes of charging the first capacitor and then sharing the charge with the second capacitor.

Figure 6-21 Converter circuit waveforms with data equal to 255
In order to assess the performance of the converter the voltage on the second node, \( V_2 \), at the end of the conversion has been measured as a function of the digital code. Figure 6-22 shows the measured output voltage for an 8-bit conversion. The output voltage range of 5.37V is consistent with the input data voltage levels of -5.03V and +0.3V. The output voltage has an offset which for codes of 0 and 255 is -200mV. There are discontinuities at the points where the more significant bits of the input code change, the largest being at the transition from code 127 to 128. This is shown more clearly in the plot of the differential non-linearity which indicates a maximum value of approximately 15½ LSB. The source of this non-linearity is a mismatch in the values of \( C_1 \) and \( C_2 \) resulting from a difference in the stray capacitances at the two nodes of the circuit.

Weighting of the input data can be used to compensate for this capacitor mismatch, and Figure 6-23 illustrates the effect that varying the weighting factor, \( W \), has on the differential non-linearity measured between codes 127 and 128. The value of the weighting which minimises the non-linearity lies between 1.06 and 1.08, and more precise measurements indicate a value of 1.062. The output voltage of the converter measured using this value of weighting is illustrated in Figure 6-24. The distinct steps associated
with the switching of the most significant bits have been removed and a residual non-linearity of less than ±1/2 LSB remains. The value of the parameter $K_1$, defined in equation 6-13, can be calculated using the relationship between $W$ and $K_1$ when the differential non-linearity is zero, $WK_1 = \frac{1}{2}$. Taking $W=1.062$ gives a value of $K_1$ equal to 0.471. This figure can be substituted into the equation for the differential non-linearity, equation 6-18, in order to check that the calculated non-linearity is consistent with that measured when no weighting of the input data is used. The calculated differential non-linearity is 15.4 LSB which is the same as that measured without weighting.

![Figure 6-23 Effect of W value on differential non-linearity](image)

The use of multilevel input data is illustrated in Figure 6-25. This shows the result of a conversion where four input data voltage levels are used combined with four conversion cycles to give a 2x4 = 8-bit conversion. The weighting factor was set at the same value of 1.062 as was used for the 8-bit conversion and the resulting differential non-linearity is less than ±1/2 LSB. This demonstrates the operation of the simultaneous bit conversion scheme described in section 6.5.2. If the weighting of the input data is not applied, then the change in output voltage with digital code shows marked steps at the transitions of the most significant digits of the input data, resulting in a differential non-linearity of 12 LSB. The differential non-linearity calculated using equation 6-19 and based on a $K_1$ value of 0.471 is 12.1 LSB, consistent with the value measured when no weighting is used.
Figure 6-24 8-bit conversion with W=1.062

Figure 6-25 2x4-bit conversion with W=1.062
6.9 Layout of Converter Pixels

In order to demonstrate the use of data conversion within the pixels of a display two, small test arrays have been designed. The first array was fabricated using the SPC poly-Si process and consisted of three columns and four rows of pixels as shown in Figure 6-26. The basic layout of the pixels was taken from an existing display design [5 Brotherton 1994] and was then modified to provide the transistor and capacitor arrangement required for the serial digital to analogue conversion. There was little optimisation of the layout in this array apart from an attempt to match the capacitance of the two half pixels.

![Figure 6-26 SPC poly-Si digital to analogue converter pixels](image)

The second array was fabricated using a laser crystallised poly-Si process and contained pixels of a number of different designs. The layout of several of these pixels is presented to illustrate some of the issues involved in their design. A plot showing the structure of one of the NMOS pixels is shown in Figure 6-27. The pixel pitch is 190μm vertically and 192μm horizontally, a size which is appropriate for a VGA resolution monochrome display with a diagonal of approximately 6 inches. The laser crystallised poly-Si process uses two layers of metalisation. The first forms the gates of the TFTs and the row electrodes, while the second is used for the source and drain contacts of the transistors and the column electrodes.
The ITO layer which forms the pixel electrode cannot be seen clearly in the plots as it overlaps both the row and column electrodes. The gap between the two halves of the pixel electrode can be seen running down the centre of the pixel. Two pixel storage capacitors are formed between the poly-Si layer and a storage capacitor line which runs horizontally through the pixels using the gate metalisation. The capacitance of the storage capacitors is approximately four times the LC pixel capacitance. The first TFT in the pixel circuit is located in the bottom left hand corner with its gate connected to the lower row electrode, while the second device is located at the top of the pixel and has its gate connected to the upper row electrode. Connection to the source and drain of the second TFT is made via contacts to the ITO pixel electrodes.

The layout of a CMOS pixel is very similar to the NMOS except that the second TFT is a p-type device and is located at the bottom of the pixel with its gate connected to the lower row electrode as shown in Figure 6-28. The n-type transistor uses a gate overlapped LDD structure and this means that the gate electrode is longer, 18μm, than that of the p-type device, 12μm. In order to match the capacitances between the gates of the two transistors and the overlying ITO pixel electrodes, the width of the gate of the p-type device was extended to give the same gate electrode area.
A potential problem with these first two pixel layouts is the presence of unmodulated light passing through the gap between the two halves of the ITO pixel electrode. This light will limit the contrast of the display. The gap between the two ITO electrodes is 4-6\,\mu m and is comparable to the separation of the two glass substrates making up the LC cell.

The unmodulated light can be removed at the cost of a small reduction in the pixel aperture by covering the gap between the pixel electrodes with a light blocking layer. Figure 6-29 shows the layout of a pixel which includes a bar of the gate metal beneath the gap between the two ITO electrodes. At the top and bottom of the pixel the gate metal is replaced by a short length formed in the column metalisation in order to avoid connecting to the two row electrodes. The central part of the bar is tied to the potential of the pixel storage capacitor while the short sections at the top and bottom of the pixel are electrically floating. A photograph showing pixels with and without the light masking between the two pixel electrodes is shown in Figure 6-30. The light leakage between the pixel electrodes which do not have light masking, at the top of the picture, can be seen quite clearly.
Figure 6-29 Light masking between pixel electrodes

In designing these pixels care has been taken to ensure that as far as possible the capacitances of the two halves of the pixel are equal. For example, misalignments of up to 3µm can occur between the poly-Si and row metalisation layers before it affects the value of the storage capacitor. However, misalignment of the ITO pixels is a potential source of mismatch between the two pixel capacitances as it changes the area of the overlap with the row and column electrodes. For example, a misalignment of the ITO layer causing a movement towards the left would increase the capacitance of the left half of the pixel, C1, while decreasing that of the right half, C2. This can be overcome by adopting a common centroid layout for the ITO. Pixel layouts which uses this approach are shown in Figure 6-31 and Figure 6-32.

In the common centroid pixel layout the ITO pixel electrode is divided through the centre in both the vertical and horizontal directions to produce four ITO electrodes of equal area. A crossover structure is formed in the centre of the pixel to link the diagonally opposite pixel electrodes. In the pixel of Figure 6-31 this crossover is formed using the poly-Si and column metalisation layers, while in the pixel shown in Figure 6-32 the column metalisation and the ITO layers are used.
Figure 6-30 Dark state of CMOS pixels with (lower) and without (upper) light masking

Figure 6-31 Common centroid CMOS pixel
6.10 Measurement of Pixel Circuit Performance

The performance of digital to analogue converter pixels has been measured in an optical system consisting of a microscope, an eyepiece with a fibre-optic probe and a photomultiplier as indicated in Figure 6-33. This system allows transmission measurements to be made within the area of one pixel. A computer is used to control the drive signals applied to the pixels and to record the transmission.
6.10.1 Measurements on First Generation Pixels

The operation of the first design of converter pixel, fabricated using the SPC poly-Si process, is illustrated by the results in Figure 6-34. This shows the variation in brightness of the pixel with digital code. The step in brightness between adjacent digital codes is also shown. The pixel was operated to perform a full 8-bit conversion with charging and charge sharing times of 14\(\mu\)s. The voltages used to address the array are summarised in Table 6-8.

<table>
<thead>
<tr>
<th>Rows</th>
<th>High</th>
<th>-12V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Low</td>
<td>-6V</td>
</tr>
<tr>
<td>Columns</td>
<td>+V(0)</td>
<td>+3.08V</td>
</tr>
<tr>
<td></td>
<td>+V(1)</td>
<td>+0.71V</td>
</tr>
<tr>
<td></td>
<td>-V(1)</td>
<td>-2.68V</td>
</tr>
<tr>
<td></td>
<td>-V(0)</td>
<td>-5.04V</td>
</tr>
<tr>
<td>Common Electrode</td>
<td></td>
<td>-2V</td>
</tr>
</tbody>
</table>

Table 6-8 Addressing voltages for SPC poly-Si pixel array

![Figure 6-34 SPC pixel design 8-bit pixel conversion](image)
The variation of pixel brightness contains large steps at the major transitions of the digital code. The step for the transition from digital code 127 to 128 is the largest and represents approximately -3.5% of the transmission range. Expressing this step height in terms of the ideal change in transmission for a 1LSB change in digital code is made difficult by the non-linear characteristic of the liquid crystal. An approximate figure for the differential non-linearity can be calculated by assuming that the ideal change in transmission for a 1LSB change in code is equal to the change in transmission between codes 126 and 127 where only the LSB changes state. This change is approximately +0.8% so that the differential non-linearity can be approximated as

\[
\text{DNL} \approx -1 + \frac{\text{step code 127 to 128}}{\text{step code 126 to 127}} \approx -1 + \frac{-3.5\%}{0.8\%} = -5.4 \text{ LSB}
\]

The most likely cause for this non-linearity is mismatch in the capacitance of the two halves of the pixel. The change in the performance of the pixel with different values of charging time is indicated in Figure 6-35. This shows how the transmission for digital codes of 0, 127, 128 and 255 change with the charging and charge sharing time.

![Figure 6-35 Effect of pixel charging time on pixel transmission](image.png)
As the charging time falls below approximately 10μs the effect of undercharging of the pixel capacitance can be seen. The transmission for a code of 127 increases, while that for 128 falls. In simple terms the effect of the undercharging is that the pixel voltage becomes dependant to some extent on the average value of the bits in the digital data rather than the binary weighted average.

Weighting of the input data can be used to correct for capacitor mismatches. By measuring the variation in the step height between codes 127 and 128 as a function of the weighting parameter applied to the input data, it was found that a parameter of W=0.9678 produces a step height which is close to the optimum value for 1 LSB transition. The full transmission measurement made using this weighting is shown in Figure 6-36. The steps in transmission at the major transitions of digital code are greatly reduced in amplitude and the step between code 127 and 128 is now +0.27% of the transmission range. However, the steps at the minor transitions show large variations suggesting that the non-linearity is not simply a result of capacitor mismatch.

Measurements of the transmission as a function of digital code of pixels at different vertical positions within the array reveal that there is a reduction in the slope of the characteristics moving down the array. In conventional TFT LCDs this degradation is indicative of high leakage currents in the pixel TFTs. Measurement of the DC characteristics of test TFTs similar to those in the array shows that the leakage currents are relatively high, suggesting that TFT leakage is likely to be contributing to the non-linearity. TFT leakage is an important issue for conventional active matrix LC displays as well as displays with pixel data conversion, and a key aspect of developing a TFT technology is controlling the device leakage.

The charging times required by the SPC poly-Si pixels are relatively long. Taking a minimum charging time of 10μs and allowing two conversion cycles for resetting the pixel voltage the total conversion time for 4, 6 and 8-bit conversions are 120μs, 160μs and 200μs. By multiplexing the column data these times could be reduced to 65μs, 85μs and 105μs. For the four bit conversion the conversion time is close to that needed for a half resolution PAL TV display which would have a row addressing time of 64μs. Some improvement in the charging times could be achieved by increasing the row drive voltage; however, for higher resolution displays and increased conversion resolutions it is unlikely that the performance of the SPC poly-Si TFTs would be adequate.
6.10.2 Measurements on Second Generation Pixels

The superior electrical properties of laser crystallised poly-Si TFTs are apparent in the performance of the second generation D/A converter pixels. In order to reduce the time required to make measurements on these pixels the resolution of the conversion has been reduced from 8-bits to 6-bits. Figure 6-37, Figure 6-38 and Figure 6-39 show the measured pixel transmission as a function of digital code and the resulting steps in transmission between adjacent codes for three of the second generation pixel designs. The first pixel uses NMOS TFTs, the second CMOS devices while the third has CMOS devices and a common centroid layout of the ITO pixel electrode. The voltages used to address the pixels are indicated in Table 6-9.
Figure 6-37 NMOS pixel, 6-bit conversion, 4μs charging time

Figure 6-38 CMOS pixel, 6-bit conversion, 4μs charging time
Figure 6-39 CMOS pixel with common centroid layout of ITO electrodes, 6-bit conversion, 4μs charging time

<table>
<thead>
<tr>
<th>Rows</th>
<th>NMOS</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>+12V</td>
<td>+10V</td>
</tr>
<tr>
<td>Low</td>
<td>-6V</td>
<td>-10V</td>
</tr>
<tr>
<td>Columns</td>
<td>+V(0)</td>
<td>+3.75V</td>
</tr>
<tr>
<td></td>
<td>+V(1)</td>
<td>+1.55V</td>
</tr>
<tr>
<td></td>
<td>-V(1)</td>
<td>-1.55V</td>
</tr>
<tr>
<td></td>
<td>-V(0)</td>
<td>-3.75V</td>
</tr>
</tbody>
</table>

Table 6-9 Addressing voltages for laser crystallised poly-Si pixels

Each of the pixels shows significant differential non-linearity, 1.6LSB, 1.4LSB and 2.3LSB respectively for the NMOS, CMOS and common centroid designs. The fact that the common centroid layout shows a high level of non-linearity indicates that this is not due to misalignment of the ITO pixel electrode causing errors in the values of the pixel capacitors. In fact the non-linearity has been identified as arising from the gate-source and gate-drain overlap capacitance of the TFTs and a parasitic capacitance between the two halves of the pixel electrode. This second capacitance was not considered in the earlier analysis of errors.
in the serial data conversion but it has the same effect as a mismatch in the values of the two pixel capacitors. An explanation of these errors and ways of reducing them is given in section 6.10.3.

The change in the transmission of the NMOS and CMOS pixels with charging time is illustrated in Figure 6-40 for four different values of digital code. The pixels show no effect of undercharging while the charging and charge sharing time is greater than or equal to approximately 2μs. This is consistent with a simple calculation of the required pixel charging time using the expressions derived in appendix A. Using the voltages listed in the table above and assuming an n-type threshold voltage of 6V, a transconductance parameter, $B$, for the pixel transistor of $1.8 \times 10^{-6}$ and a voltage error of 10mV the calculated charging time for the half pixel is approximately 0.8μs.

With a charging time of 2μs the times required to perform 4, 6 and 8-bit conversions are 24μs, 32μs and 40μs. These times are compatible with use of the display for NTSC and PAL resolution TV signals, and if the grey scale resolution is limited to 6-bits then the pixels could also be applied to a VGA resolution datagraphic display.

![Figure 6-40 Effect of pixel charging time on transmission for NMOS and CMOS pixels](image-url)
It has already been stated that non-linearity resulting from stray capacitance between the two pixel electrodes is similar to that caused by capacitor mismatch. In the same way that weighting of the input data could be used to correct for errors in the capacitor values it can also be used to correct for the effect of the capacitance between the pixels. Table 6-10 indicates the values of differential non-linearity measured for various pixel layouts and the values of weighting required to correct for this non-linearity. Figure 6-41, Figure 6-42 and Figure 6-43 show the measured pixel characteristics for the three main designs with weighting applied to the input data. The differential non-linearity is substantially reduced by weighting the input data. The residual value of non-linearity is 0.1 to 0.2 LSB which is much lower than was achieved with the first generation pixels.

<table>
<thead>
<tr>
<th>Pixel design</th>
<th>DNL no weighting</th>
<th>Required weighting</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS no light masking</td>
<td>1.6 LSB</td>
<td>1.023</td>
</tr>
<tr>
<td>CMOS no light masking</td>
<td>1.4 LSB</td>
<td>1.021</td>
</tr>
<tr>
<td>CMOS with light masking</td>
<td>2.2 LSB</td>
<td>1.033</td>
</tr>
<tr>
<td>CMOS common centroid no light masking</td>
<td>2.3 LSB</td>
<td>1.033</td>
</tr>
<tr>
<td>CMOS common centroid with light masking</td>
<td>2.1 LSB</td>
<td>1.032</td>
</tr>
</tbody>
</table>

Table 6-10 DNL values and required weighting for different pixel layouts

Figure 6-41 NMOS D/A pixel with input data weighting, W=1.023
Figure 6-42 CMOS D/A pixel with input data weighting, \( W=1.021 \)

Figure 6-43 CMOS D/A pixel with common centroid layout of ITO, input data weighting, \( W=1.033 \)
6.10.3 The Effect of Parasitic Capacitance Between Half Pixels

The effect that the parasitic capacitance between the two pixel electrodes has on the converter circuit can be estimated in a similar way to the effect of capacitor ratio errors considered earlier. The way in which this capacitance introduces an error into the final converted voltage can be illustrated with reference to Figure 6-44. During the conversion, when the transistor $T_2$ is turned off the voltage $V_2$ should remain constant. However the presence of the capacitance $C_C$ between the two halves of the converter couples any changes in the value of $V_1$ onto the second pixel, thus changing the value of $V_2$. The errors caused by $C_C$ can be quantified by determining the equation for $V_2$ which is iterated during the conversion. For simplicity it is assumed that the transistors are ideal switches with no parasitic capacitance and that the capacitances of the two halves of the pixel are equal.

![Figure 6-44 Pixel equivalent circuit including capacitance between two half pixels](image)

Consider the operations during one cycle of the conversion from the point at which $T_1$ has just turned on. The voltages on the two pixel capacitors are initially equal with a value of $V_2(i-1)$. The first capacitor now charges to the voltage representing the next bit of the input data $V_i(i)$. The change in voltage on the first capacitor is coupled onto the second by $C_C$ so that the new value of $V_2$, $V_2^*$, is given by the expression below.

$$V_2^* = V_2(i-1) + \left( V_i(i) - V_2(i-1) \right) \frac{C_C}{C_C + C} \quad 6-24$$

Next $T_1$ turns off and $T_2$ turns on so that charge sharing takes place between the two pixel capacitors. The resulting voltage, $V_2(i)$, can be calculated using the conservation of charge.
\[
V_2(i)2C = \left( V_2(i-1) + (V_f(i) - V_2(i-1)) \frac{C_c}{C_c + C} \right) C + V_f(i)C \quad 6-25
\]

\[
V_2(i) = V_f(i)\frac{1}{2} \left( 1 + \frac{C_c}{C_c + C} \right) + V_2(i-1)\frac{1}{2} \left( 1 - \frac{C_c}{C_c + C} \right) \quad 6-26
\]

The pixel voltage at the end of N conversion cycles can be derived by considering the effect of iterating equation 6-26 and is given by the equation below.

\[
V_{pixel} = \sum_{i=1}^{N} V_f(i) \frac{1}{2} K_{c1} \left( \frac{1}{2} K_{c1} \right)^{N-i}
\]

\[
K_{c1} = 1 - \frac{C_c}{C_c + C} \quad K_{c2} = 1 + \frac{C_c}{C_c + C}.
\]

The presence of capacitance between the two halves of the pixel affects both the gain and the linearity of the conversion. The differential non-linearity can be calculated for a 6-bit conversion using the equation below.

\[
DNL = \frac{\left( 1 - \frac{1}{2} \sum_{i=0}^{6} \left( \frac{1}{2} K_{c1} \right)^{6-i} \right) \cdot (2^6 - 1)}{\sum_{i=0}^{6} \left( \frac{1}{2} K_{c1} \right)^{6-i} - 1} \quad 6-28
\]

Figure 6-45 shows how the differential non-linearity varies with the ratio of the capacitance between the two half pixels to the capacitance of one half pixel. As the ratio of the capacitance between the half pixels to the pixel capacitance increases, so does the non-linearity. In order to improve the performance of the converter pixels it would therefore be possible to increase the value of the pixel storage capacitor or to reduce the value of the stray capacitance between the pixel electrodes.

Increasing the value of the storage capacitor is undesirable since the larger capacitor will occupy a greater fraction of the pixel area reducing the aperture of the display. The higher capacitance would also increase the charging time required by the pixels. The capacitance between the two pixel electrodes can be reduced by increasing their separation. Figure 6-46 shows schematically the arrangement of the electrodes within the display in cross section and plan views. The capacitance between the two pixel electrodes has been calculated using a layout simulation program “Fasterix” \(^\text{[Philips ED&T]}\)
Figure 6-45 Variation of differential non-linearity with pixel coupling capacitance

Figure 6-46 Cross section and plan views of pixel used for capacitance calculation
The variation of capacitance with electrode spacing is shown in Figure 6-47 and this can be used to calculate the spacing required to achieve a differential non-linearity of less than 0.5LSB. The value of $C_{JC}$ required is determined from Figure 6-45 and is < 0.009. The capacitance of the half pixels in the second generation design is approximately 0.65pF; therefore, the value of $C_C$ should be less than 6fF. Using the results shown in Figure 6-47, the gap between the two electrodes should be greater than approximately 12µm. Such a large separation is undesirable due to its impact on the displays aperture if the gap has light masking and its impact on the displays contrast if the gap has no light masking. Increasing the separation of the electrodes therefore looks unattractive as a method of reducing the differential non-linearity.

Errors in the capacitance of the two half pixels and the presence of the capacitance between the two half pixels both have the same effect on the performance of the converter. It is therefore possible to compensate for the capacitance between the pixel electrodes by deliberately introducing a difference in the values of the pixel capacitors. To establish the required pixel capacitance ratio it is necessary to calculate the combined effect of capacitance between the pixels and unequal values of pixel capacitance on the converted...
voltage. Consider again the voltages present during the data conversion. The voltage on C2 after C1 has been charged but before T2 is turned on is given by the expression

$$V_2^* = V_2(i-1) + (V_i(i)-V_2(i-1)) \frac{C_c}{C_c + C_2}$$

6-29

When T2 is turned on charge sharing takes place between the two pixel capacitors. The resulting voltage, $V_2(i)$, can be calculated from the conservation of charge.

$$V_2(i)(C_1 + C_2) = \left[ V_2(i-1) + (V_i(i)-V_2(i-1)) \frac{C_c}{C_c + C_2} \right] C_2 + V_i(i)C_i$$

6-30

$$V_2(i) = V_i(i) \frac{1}{(C_1 + C_2)} \left[ C_1 + \frac{C_cC_2}{C_c + C_1} \right] + V_2(i-1) \frac{1}{(C_1 + C_2)} \left[ C_2 - \frac{C_cC_2}{C_c + C_2} \right]$$

6-31

By considering the effect of iterating this equation the voltage at the end of the conversion can be obtained. The pixel voltage after N conversion cycles is given by the equation below.

$$V_{pixel} = \sum_{i=1}^{N} V_i(i) \frac{1}{2} K_{C_1} \left( \frac{1}{2} K_{c} \right)^{N-i}$$

6-32

$$K_{C_1} = \frac{2}{C_1 + C_2} \left( C_2 - \frac{C_cC_2}{C_c + C_2} \right)$$

6-33

$$K_{C_2} = \frac{2}{C_1 + C_2} \left( C_1 - \frac{C_cC_2}{C_c + C_2} \right)$$

6-34

To eliminate the differential non-linearity the parameter $K_{C_1}$ must be made equal to 1.

$$\frac{2}{C_1 + C_2} \left( C_2 - \frac{C_cC_2}{C_c + C_2} \right) = 1$$

In order to simplify the equation the capacitance values can be related to the total pixel capacitance $C_T$ by making the substitutions $C_1 = K_c C_T$, $C_2 = (1-K_c)C_T$ and $C_c = K_c C_T$. This yields the relationships between $K_c$ and $K_c$ indicated by the equations below and illustrated in Figure 6-48.

$$K_c = 1 - 3K_r + 2K_r^2$$

6-35

$$K_r = \frac{3}{4} - \frac{1}{\sqrt{16 + \frac{1}{2} K_c}}$$

6-36
Figure 6-48 Difference in C1 and C2 values required to compensate for Cc

The pixel designs which do not include light masking between the pixels have a 4μm gap between the half pixels resulting in a capacitance of 11fF between the electrodes. The total pixel capacitance is approximately 1.3pF, therefore the value of $K_c$ is 0.017 and the required value of $K_r$ to compensate for the capacitance between the pixels is 0.484. The capacitance of C1 would need to be decreased by 1.6% and C2 increased by 1.6% in order to provide this correction. This could most easily be achieved by changing the area of the pixel storage capacitors or the overlap capacitance of the TFTs.

To confirm the validity of the analysis of the effect of the capacitance between the half pixels it is useful to compare the calculated value of differential non-linearity with the value measured. The differential non-linearity of the NMOS pixel design was 1.6LSB. The gate-drain overlap capacitance of the TFTs used in the pixel is approximately 5fF, ($C_{ox}=2.3E-4$, $W=4μm$, $L_o=6μm$). The capacitance of a half pixel is approximately 650fF giving values for C1 and C2 of 660fF and 655fF. The capacitance between the half pixels is 11fF resulting in a value for $K_{C1}$ calculated using equation 6-33 of 0.98. The differential non-linearity can be calculated using equation 6-28, and is 2.2LSB which compares well with the measured result given the uncertainty of the values of the capacitance within the pixel.
6.11 External Drive Circuit Requirements of Display with Pixel Data Conversion

The row drive circuit required for a display using serial digital to analogue conversion is very similar to that of a conventional display. A schematic diagram of a row driver which could be used with a CMOS pixel converter is shown in Figure 6-49. The circuit consists of a shift register which provides selection of successive rows, and NAND gates which allow the shift register outputs to be masked with an externally generated control signal.

Figure 6-49 Row driver for use with pixel conversion

Waveforms illustrating the operation of the circuit are shown in Figure 6-50. As the output level of the row drive circuit must be switched a number of times during the row addressing period, the rise and fall times of the row drive signals may need to be lower than for a conventional row drive circuit. If an NMOS pixel converter is used or if multiplexed column data is implemented then a slightly more complex row drive circuit is required, allowing two or three rows to simultaneously receive addressing pulses.

Figure 6-50 Row driver waveforms
A schematic diagram of a column drive circuit for the pixel converter display is shown in Figure 6-51. Digital video data is transferred to a first set of latches during the active video line period. The output signals from the shift register cause each latch in turn to sample the data from the video data bus. At the end of the video line period, when the first latches have been filled, the data is transferred simultaneously to a second set of latches. The individual bits of data from these second latches are selected sequentially and used to control the voltage applied to the output of the column drive circuit. A high bit results in the voltage $V(1)$ being applied to the column while for a low bit the voltage is $V(0)$.

If operation with multiplexed column data is required, then an additional two sets of latches would be needed. This is because when the display is addressed with multiplexed column data, two rows of pixels are addressed simultaneously and the pixel conversion is extended over two video line periods. While two sets of latches are providing column data for the conversion, a second pair must be loaded with the next two lines of video information.

A particularly simple column drive circuit can be used if the video data is reordered using an external line memory before it is transferred to the display. The circuit illustrated in Figure 6-52 requires only two bits of data storage for each column output. The bits of the data for each column are transferred serially rather than in parallel and are transferred only as they are required during the pixel conversion. The reduction in the amount of data stored on the display results in a significant reduction in the number of transistors in the
circuit. This would be a particular advantage for a TFT column drive circuit. In order to reduce the clock frequency required to transfer the digital data to the display the circuit is divided into a number of blocks, each with its own shift register and video data input. The video data is transferred to these blocks simultaneously.

![Simple column drive circuit for serial pixel conversion](image)

**Figure 6-52 Simple column drive circuit for serial pixel conversion**

### 6.12 Summary

Integration of a digital to analogue converter circuit within each pixel of a display allows a display having grey scale capability to be addressed with digital column drive signals. The circuits addressing the columns of the display can be digital rather than analogue circuits, with the potential advantages of more compact and lower cost column drivers. The most likely application for this technique would be low cost, low resolution displays, where grey scale capability and high contrast are required.

The serial charge redistribution conversion technique is an attractive method of performing the data conversion as it requires few components within the pixel and requires no increase in the pixel circuit complexity to achieve higher conversion resolutions. The main issues for this type of converter are control of the capacitance values of the sub-pixels and the time required to carry out the charging and charge sharing cycles required during the conversion process. The need for rapid charging of the pixel capacitance means that laser crystallised poly-Si TFTs, which have high values of field effect mobility, are particularly suitable for this application.
To demonstrate the pixel conversion technique small pixel arrays have been designed and measured. The performance of the pixels in terms of the required conversion times is consistent with simple calculations of the pixel charging times. With laser crystallised poly-Si devices conversion times of 32μs can be achieved for 6-bit conversion resolution. This is compatible with displays for TV and VGA datagraphic applications. The differential non-linearity achieved from the pixel converter circuits was relatively poor, 1.5LSB to 2.5LSB for a 6-bit conversion. The cause of this non-linearity is stray capacitance between the pixel electrodes and a difference in the capacitance of the two halves of the pixel due to the overlap capacitance of the TFTs. Two methods for reducing or eliminating the effect of the capacitance between the pixel electrodes have been proposed.

A potential application for this technique is in displays for hand held computers where the video information is generated in a digital form and the resolution of the display is not too demanding. The next steps for this work would be to fabricate a display using these pixels in order to demonstrate that acceptable uniformity of the converters can be achieved over a large area. In addition the potential benefits of this scheme should be investigated in more detail, in particular the potential cost savings in the external circuitry required by the display.
7 Circuit Yield and Fault Tolerance

7.1 Introduction

The yield of working circuits is an important issue for large area electronics. In the case of integration of the drive circuits for active matrix displays, any significant reduction in the yield of working devices would negate one of the key advantages of drive circuit integration which is to reduce the cost of the displays. Conventional silicon drive circuits are tested before they are connected to the displays and defective circuits are therefore avoided. However, TFT drive circuits are fabricated on the same substrate as the display making a process of testing and selection more difficult.

This section puts the issue of circuit yield into perspective and reviews a number of published techniques which can be used for enhancing the yield of AMLC displays and TFT circuits. Some of these approaches require external intervention to repair the defects, while others provide a degree of inherent fault tolerance. A self testing approach to redundancy is described\[6\] and a simple analysis of its effect on circuit yield presented.

7.2 A Perspective on the Issue of Yield

While considering the importance of yield in TFT circuits for driving AMLC displays, it should be kept in mind that the active matrix of the display is itself an extensive electronic circuit consisting of thousands of row and column addressing electrodes and a million or more transistors. Only a very small number of defects can be tolerated within the active matrix, although redundancy or repair techniques can be used to increase yield by correcting the most common and serious types of defect.

A simple approach to considering the relative effect on yield of defects within the active matrix and the drive circuits is to compare the active area, the area occupied by the channel region of the transistors, within the two structures. As an example the total area of the poly-Si TFTs within the pixels of a full resolution projection TV display (640x480 pixels with pixel transistors having W/L = 4μm/12μm) is approximately 15 mm². This should be compared to the area of the transistors within the drive circuits which might typically be about 2-3 mm², less than 20% of that of the matrix. In practice other factors will also
influence the relative yields. The density of the transistors within the drive circuits is higher and the line separations smaller than within the matrix. These differences make the circuits more vulnerable to photolithographic defects than the active matrix. The question of whether the use of redundancy and fault tolerance offers a significant advantage in terms of overall yield will be dependant on the types of defect which are most common for the manufacturing equipment and processes involved.

7.3 Repair with Redundant Circuit Elements

The simplest approach to drive circuit redundancy [Y Matsueda 1989] is to apply drive signals to both ends of the display addressing electrodes by using two separate drive circuits, as illustrated in Figure 7-1. This method not only provides a degree of redundancy to the drive circuits, if one circuit is faulty it can be isolated from the display by cutting the appropriate addressing electrodes with a laser and the other drive circuit can then be used, but when both drive circuits are functioning correctly this arrangement is tolerant of single breaks within the row and column electrodes of the display. The degree of protection against circuit defects provided by this method is limited. The row and column drive circuits generally depend on the transmission of a selection pulse through a shift register and therefore a single defect within the shift register can cause all succeeding sections of the driver to fail. With this type of drive circuit it is necessary that at least one of the two circuits should contains no defective shift register sections.
An alternative to the shift register for generating sequential selection signals is the use of address lines and decoders. This approach has the advantage that it does not rely on the propagation of a signal through the circuits, and therefore defects within the decoders can be localised resulting in only a small group of defective outputs. [K Kimura 1988][N Harada 1994]

The use of redundancy and repair can be extended to increase the number of defects which can be tolerated within the drive circuit. By including redundant shift register elements within the circuit, as illustrated in Figure 7-2, defective sections can be isolated by laser cutting and then replaced by the parallel redundant elements which are connected into the circuit using laser welding. [H Asada 1990] The location of the defects must be determined by measuring voltage waveforms at the outputs of the circuit or by using specialised testing techniques developed for flat panel displays. [F Henley 1992]

![Figure 7-2 Redundancy using laser repair](image)

**7.4 Fault Tolerant Circuits**

The repair of circuits requires a procedure for testing and then physically altering connections within the circuit so that signals bypass defective sections. A more efficient solution is to have circuits which are inherently tolerant of defects. An example of a scheme which is tolerant of certain types of defects has been described by Takafuji et al. [Y Takafuji 1992] and is illustrated in Figure 7-3. Rather than using a single shift register the drive circuit is divided into a number of blocks, each block containing two parallel shift registers. The carry signals from the two shift registers are combined by a NOR gate before passing to the inputs.
of the shift registers in the next block. The parallel outputs from the two shift registers within a block are combined using NAND gates.

This circuit is inherently tolerant of a defect in one of the two shift registers which causes the parallel outputs of the register to become stuck in a high state. When this occurs, the signal from the second shift register will still be passed to the outputs of the circuit by the NAND gates. The carry outputs of the shift register are inverted and therefore if the parallel outputs of a register are stuck high then the carry output is stuck low. In this case the NOR gate is still able to pass a carry signal from the working register to the input of the next shift register block.

![Figure 7-3 Circuit with limited fault tolerance](image)

The circuit is not tolerant of defects which cause the parallel shift register outputs to become stuck in a low state. In this case the shift register containing the fault must be located by probing the carry signals at the output of each block. Then laser cutting is used to disconnect the incorrect signals from the inputs of the NAND and NOR gates. The inputs of these gates include pull-up and pull-down devices respectively, so that once the inputs are isolated from the fault the circuit is able to function correctly.

A more complex fault tolerant arrangement which can correct for stuck high and stuck low defects within shift register sections without the use of a laser has been described by H Asada et al. Two blocks of the circuit are shown in Figure 7-4. Each block consists of a main shift register section, a redundant register section and an error-correcting circuit. The error-correcting circuit includes an XNOR gate which compares the signals A
and C. If the logic levels of A and C are the same, then the output of the XNOR gate is high and the signal at A is passed on to the next stage of the circuit. If a defect is present within the main shift register section, indicated by the signal A being different to C, then the output of the XNOR gate goes low and the signal B is passed on to the next block.

![Diagram of fault tolerant circuit](image)

**Figure 7-4 More complex fault tolerant circuit**

This circuit has clear advantages over the previously described arrangement in that it can cope with a wider range of defects. However, one factor which may reduce its effectiveness is that during the feedback clock phase, when ck is low and /ck is high, the signal C which is compared with the output of the main register section is determined by the redundant register section. This means that a defect within the redundant shift register section would cause the XNOR gate to switch the signal at B, which is defective, through to the output at the time when the next stage in the circuit is latching this output signal.

### 7.5 Self Testing Circuits

The concept of self testing circuits\[M Edwards P1\] is one which allows the automatic correction of a wide range of defects in many different types of circuit. This technique differs from those described previously as external signals are used to co-ordinate the testing operation and the result of the test, working or defective, is stored within the circuit. This self testing redundancy scheme can be applied to a wide range of circuits, including analogue circuits,
by developing appropriate testing procedures. The principle of the self testing redundancy is illustrated in Figure 7-5. As in the schemes described previously, parallel circuit paths are provided so that if a defect occurs in one circuit then others can be used in its place. Which of the circuits is used is determined by a Testing Circuit. This circuit inspects the output waveforms from the three circuits in order to determine which, if any, is defective. This is similar to the function of the XNOR gate in the shift register circuit described by H. Asada; however, in this self testing scheme the testing circuit is controlled by an externally applied signal and the result of the test is stored by a memory element. This allows the scheme to be applied to a wide range of circuits, not just shift registers, and also allows a trade-off between the relative complexity of the redundant circuits and the testing circuits.

![Figure 7-5 General self testing circuit](image)

The strategy used in this scheme is that each time that the circuit is turned on, the response of the redundant circuits to known input signals is tested. The result of the test, whether or not a circuit produced an incorrect output and therefore contains a defect, is stored in the testing circuit and is then used to select the redundant circuit sections which are used when the circuit is operating normally after the tests. In the case of digital circuits the testing circuit simply has to detect whether a high or low logic level is produced by the redundant circuits at appropriate times during the tests. If the redundant circuits are analogue, then it may be necessary to perform more complex tests, for example using a comparator to compare the output signal levels with a reference value.
The application of the self testing redundancy scheme to the shift registers used in row and column drive circuits is illustrated in Figure 7-6. As in the circuit described by Takafuji the shift register is divided into shorter blocks and each block includes parallel shift register elements. However, in this design there is also a testing circuit associated with the shift registers. This circuit tests the level, high or low, of the signal at the carry output of the shift registers, and in response to these tests generates a signal which controls which of the parallel outputs from the shift registers are fed to other stages of the circuit, for example the output drivers in the case of a row drive circuit.

Figure 7-6 Self testing shift register circuit

Figure 7-7 Shift register testing circuit
A circuit diagram showing the testing circuit constructed using NMOS TFTs is given in Figure 7-7. The inputs to the circuit are the carry signals from the shift registers, Carry A and Carry B, and two control signals, Test High and Test Low. The outputs of the circuit are two complementary signals AOK and BOK which are used to control the switches at the outputs of the shift registers and the carry signal, Carry Out, which is fed to the next shift register block. The circuit consists of a bistable, T1-T4, with additional transistors, T5-T12, which allow the state of the bistable to be set or reset according to the results of the testing operations. The outputs of the bistable are used to select one of the two input carry signals using the circuit T13-T17. If AOK is high then Carry A is passed to the output alternatively if BOK is high then Carry B is selected.

When the circuit is powered up, the state of the bistable element is arbitrary and a sequence of tests must be performed in order to ensure that only working shift register elements are selected. The arrangement of the testing circuit is such that the carry signal from that shift register which is selected by the bistable is the one which will be checked during a testing operation. To perform a test on the drive circuit, the carry signal at the input of the driver is first set at a low level and time is allowed for the signal to be clocked through the length of the shift register to the final section. Then the Test Low signal is taken to a high level.

Considering the case where at power up AOK is high and BOK is low, this change in the level of Test Low causes a low level test to be performed on Carry A. If Carry A is at a low level during the test then T5 will be conducting but T6 will not. Under these conditions the state of the bistable remains unchanged. If however the signal at Carry A is a high level then both T5 and T6 will be turned on. The resistance of T5 and T6 is much lower than that of the load device T2 with the result that the voltage at node AOK is pulled low causing the bistable to change state. AOK becomes low and BOK becomes high.

The second part of the test procedure is to feed a high level into the two shift registers, again allowing time for the signal to be clocked through the circuit. Then the Test High signal is taken low. Assuming again that AOK is initially high, taking Test High low causes T10 to turn off. If the input Carry A is high then T9 remains conducting so that the state of the bistable is unchanged. If however Carry A is low, then since both T9 and T10 are turned off, the voltage at node BOK rises due to the load device T1. This causes the bistable to flip state and AOK becomes low and BOK high.
The sequence of Low Test followed by High Test must be repeated once for each block in the drive circuit. This is necessary because an incorrect carry signal generated in one block will propagate through to the following blocks causing their test circuits to detect a fault when in fact there may be no fault present within that particular block.

An NMOS row drive circuit using this self testing redundancy approach has been designed and demonstrated by addressing a small test array. The circuit consists of five shift register blocks each providing twenty row drive outputs. Figure 7-10 shows a photograph of part of the circuit in which the two shift registers, the output circuits and two testing circuits can be seen. To demonstrate the operation of the testing circuits a node within one of the shift registers was grounded with a probe to simulate a defect. When the display was first turned on the grounded probe prevented the row selection pulse from progressing through the row driver so that only the top half of the display was addressed, as shown in Figure 7-9. When the test operation has been performed the second shift register within the defective block is selected allowing the complete display to be addressed as shown in Figure 7-8.

![Figure 7-10 One block in a self testing row drive circuit](image)

![Figure 7-9 Display before test operation](image)

![Figure 7-8 Display after test operation](image)
In principle this self testing scheme can be applied to any part of a circuit, for example two output drivers could be provided for each row in the display and a testing circuit could be used to deselect drivers with defective outputs. However, the overhead of circuitry needed to provide both the parallel circuit elements and the testing circuits would make the layout of the circuit difficult.

7.6 Simple Yield Analysis for Self Testing Circuit

In order to estimate the yield of a redundant circuit it is necessary to have information both of the types of defect which occur during fabrication, and the probability that they will occur. This information only becomes available when the factory in which fabrication is to take place is running and the resulting defects can be analysed. In the absence of this information it is still possible to draw some conclusions about the effectiveness of the redundancy schemes by carrying out a simple yield analysis based on the active area of the devices within the circuit.

In order to illustrate how the yield can be estimated, consider the example of a shift register to be used within a row drive circuit. The shift register is divided into a number of blocks and each block contains two redundant shift registers and a testing circuit. The drive circuit will fail under two conditions, 1) if there is a defect within both redundant shift registers in any block of the circuit, 2) if there is a defect within a test circuit which causes it to select a shift register which is also defective. Consider the probability of these two conditions occurring.

1) Let the probability of fabricating a shift register within a block which contains no defects be \( P_{ndSR} \), then the probability that both shift registers within a block of the circuit will be defective is given by

\[
(1-P_{ndSR})(1-P_{ndSR}) = (1-P_{ndSR})^2.
\]

2) The second condition can be broken down into two situations. a) the testing circuit is defective and selects the first redundant shift register, which is also defective, while the second register contains no defects, b) the testing circuit is defective and selects the second shift register, which is also defective, while the first register operates correctly. Note that the
condition where both the shift registers and the testing circuit are defective is already covered in condition 1).

The probability of only one of the two shift registers being defective is given by the equation

\[ P = (1 - P_{ndSR}) P_{ndSR} + (1 - P_{ndSR}) P_{ndSR}^2 = 2(1 - P_{ndSR}) P_{ndSR}. \]

Let the probability of fabricating a testing circuit with no defects be \( P_{ndTC} \) then the probability of the testing circuit having a defect is \( (1 - P_{ndTC}) \). The probability of the testing circuit also selecting a single defective shift register, situation a) and b) above, is therefore

\[ P = 0.5(1 - P_{ndTC})2(1 - P_{ndSR}) P_{ndSR} = (1 - P_{ndTC})(1 - P_{ndSR}) P_{ndSR}. \]

The probability of a block within the drive circuit failing is obtained by combining the probabilities of condition 1) or 2) occurring, so that the probability of a defective block is

\[ P = (1 - P_{ndSR})^2 + (1 - P_{ndTC})(1 - P_{ndSR}) P_{ndSR}. \]

The overall circuit yield is given by the probability of producing a circuit which contains no failed blocks. For a circuit made up of \( NB \) blocks the following expression results.

\[ \text{Yield} = 100(1 - (1 - P_{ndSR})^2(1 - P_{ndTC})(1 - P_{ndSR}) P_{ndSR})^{NB} = 100(1 - P_{ndTC}(1 - P_{ndSR}) P_{ndSR} + P_{ndSR})^{NB} \% \]

In order to illustrate the effect of defect density, \( D \), and circuit complexity on yield assume, that the probability of a circuit element which has an active area of \( A \) containing no defects is given by Poisson's distribution. [C Stapper 1989]

\[ P_{nd} = \exp(-DA) \]

Assume that all the transistors within the shift registers and testing circuits have a width of 10\( \mu \)m and a gate length of 10\( \mu \)m. Assume that each section of the shift register requires 8 transistors and that the testing circuit contains 26 transistors, and consider the effect of varying the number of shift register sections within a circuit block, \( NSRS \), for a shift register circuit having 480 outputs. The variation of circuit yield as a function of defect density for different values of \( NSRS \) is shown in Figure 7-11. For comparison the yield of the active matrix of the display is also shown, assuming that none of the 640x480 pixel transistors is defective and that the active area of the pixel TFTs is 12\( \mu \)m x 4\( \mu \)m.
For defect densities in the range of 30 cm$^{-2}$ to 300 cm$^{-2}$, the use of redundancy offers a significant improvement in circuit yield. The improvement becomes greater as the number of shift register sections in each block of the circuit is reduced, this is despite the increase in the number of testing circuits required. This can be explained by the fact that although the number of testing circuits is increasing, the probability of a defective testing circuit resulting in a defective circuit block is decreasing since it is less likely that the shift registers within the block will contain defects. While increasing the number of circuit blocks may be advantageous from the point of view of yield, it will tend to increase the area occupied by the circuit making the layout more difficult.

The result in Figure 7-11 also indicates quite dramatically that the shift registers are much less sensitive to defects than the active matrix of the display. This is an important result since it indicates that if the defects are purely related to the active area of the devices, then the yield of complete displays will be limited by the active matrix and not the drive circuits.

The variation of circuit yield as a function of defect density with the number of TFTs within the testing circuit as a parameter is shown in Figure 7-12. It is assumed that each block of the circuit contains 20 shift register sections. Increasing the number of TFTs within the testing circuit has a relatively small effect on the circuit yield until the number of TFTs in
the testing circuit becomes large. This is because a defect within the testing circuit does not in itself cause the circuit to fail. The circuit will only fail if this causes the testing circuit to select a defective shift register.

![Graph showing the effect of number of TFTs in the testing circuit on yield.](image)

**Figure 7-12** Effect of number of TFTs in the testing circuit on yield

### 7.7 Summary

One of the factors which determines the cost of active matrix LC displays is the yield of working devices. In displays using conventional silicon drive circuits, one of the potential yield limiting steps is the bonding of the drive circuits to the edge of the display. An important advantage of displays with integrated drive circuits is the elimination of this step. Although integrating the drive circuits adds to the complexity of the display, it is unlikely to have a severe impact on the display yield. The reason is that the active area of the circuits will normally represent only a fraction of the active area of the transistors within the matrix of the display. While there may initially be an advantage in implementing redundancy and repair techniques to boost the yield of working drive circuits, during the life of a factory it would be expected that defect levels would be reduced to the point where this is no longer necessary.
8 The Future for Display System Integration

One of the possibilities that comes with the development of low temperature poly-Si AMLCDs is extension of circuit integration from the displays drive circuits to complete systems. System integration is a development which can be seen in many electronic products. Reducing the number of components within the system by designing increasingly complex integrated circuits is allowing a reduction in the size and cost of hand held products such as portable telephones.

Low temperature poly-Si is a large area technology, and the area available around the edge of a display for further circuit integration is surprisingly large. For example a border 1mm wide around the edge of a 10-inch diagonal display has an area of 4cm². The resolution of the lithography used in fabricating TFT circuit is considerably lower than that used in conventional IC processing, but this area could in principle accommodate circuits consisting of more than ten thousand TFTs. The most obvious extension of drive circuit integration is to construct other elements of the display drive system using TFTs. The drive system requirements of an active matrix LC display based on an analogue video signal source are shown in Figure 8-1.

The analogue video signal, which could be from a television or computer source, first has its amplitude and black level adjusted to set the contrast and brightness of the displayed image. It then passes to a circuit which inverts the polarity of the signal as required to
generate the ac drive voltage needed by the LC. The processed video signal is then sampled and transferred to the parallel video inputs of the column drive circuit. The timing of the display drive system is controlled by the video sync signal. A Phase Locked Loop (PLL) is used to generate a sample clock signal which is a multiple of the video line frequency, the multiplying factor being determined by the number of columns in the display. A control circuit generates the timing signals needed to control the row and column drive circuits, the sampling of the processed video signal and to control the drive voltage polarity.

Most of the circuits making up the drive system are required to operate at high frequencies. Maintaining the bandwidth of the video signal up to the point where it is sampled and generating the sample clock are likely to be the most critical issues. For television displays the video signal bandwidth would typically be 6MHz with a sample clock frequency of 12MHz. For datagraphic displays the pixel clock frequency ranges from 25MHz for a VGA resolution display to 65MHz or more for an XGA display. For the complete drive system to be integrated onto the display it will be necessary to develop TFT circuits which can operate at these high frequencies. The circuits presently constructed using TFTs are switching circuits which are relatively undemanding of the transistor characteristics. An important step towards full drive circuit integration will be a demonstration that practical analogue circuits can be fabricated using TFTs.

Figure 8-2 Digital AMLCD system for hand held computing

Displays for hand held computing applications provide a second possible route towards system integration. Key components of a hand held computing product are shown in
Figure 8-2. It consists of the processor, input devices such as a keyboard, touch screen or voice input device, video memory and control circuits. It is possible to imagine that a number of these functions could be integrated onto the display. The resolution of the display will be lower than desktop computing applications and refresh speed and grey scale performance are likely to be lower for hand held products. For this reason it may be possible to integrate both the video memory and control circuits onto the display. Integration of the input devices may also be possible since these operate at relatively low frequencies, in particular for a touch input device it would be appropriate to integrate this within the display itself.

While the processor could in principle be integrated using TFTs the degree of complexity and the need for high speed operation mean that this is unlikely. Use of the displays substrate as a carrier for the processor would be an option, and it is possible to imagine a situation where the complete system is assembled on the display substrate. Conventional silicon integrated circuits would be used for the most demanding operations, and these would be bonded to the display substrate using techniques such as the chip on glass technology which is currently used for bonding silicon drive circuits to active matrix LC displays.
9 Conclusions

The work described in this thesis is concerned with the design of circuits using thin film transistors for use in active matrix liquid crystal displays. The main application of the circuits is to replace the conventional silicon integrated circuits which are normally used to address the rows and columns of active matrix displays with circuits which are integrated onto the glass substrate of the display using thin film transistors. The first part of this thesis describes the performance of devices and simple circuits fabricated using two different low temperature poly-Si technologies.

The electrical characteristics of transistors formed using solid phase crystallisation and laser crystallisation were described in chapter 3. The SPC transistors have relatively poor characteristics. The field effect mobility of the transistors is approximately thirty times lower than typical crystalline silicon devices and the threshold voltages are relatively high. The p-channel SPC transistors show a strong carrier trapping related transient behaviour which severely degrades the DC characteristics of the devices and makes it difficult to predict the performance of SPC CMOS circuits. Transistors produced by laser crystallisation exhibit much higher values of field effect mobility, approximately four times lower than conventional silicon devices. They also show little transient behaviour and well matched p-channel and n-channel transistors can be fabricated.

The differences in the electrical characteristics of transistors fabricated with the two processes are also reflected in the performance of inverters and shift registers, as described in chapter 4. Laser crystallised CMOS inverters provide higher noise margins and more symmetrical switching characteristics than those using the SPC devices. Shift registers fabricated using laser crystallised devices operate at higher maximum clock frequencies and at lower power supply voltages than those of the SPC technology. A consequence of the superior results obtained with laser crystallisation technology is that this has now become the mainstream route for fabricating low temperature poly-Si TFTs. Simple CMOS amplifiers have been fabricated with the laser crystallised transistors and have been shown to provide basic levels of performance which would allow them to be used within the column drive circuits of active matrix displays. Uniformity of the laser crystallised transistors appears to be an issue for these devices as large variations in the low frequency gain and input offset voltage of the amplifiers were found. A more detailed investigation of device uniformity would be needed to determine if this is a fundamental
issue or whether future technology developments, particularly in techniques of laser crystallisation, will bring improvements in uniformity.

The main application for TFT circuits is integration of the drive circuits for AMLC displays onto the display substrate. The design issues which arise in extending the integration of TFT row and column drive circuits to larger display sizes were described in chapter 5. An example of a prototype display with integrated drive circuits was also presented. The design of the row drive circuits is straightforward using poly-Si TFTs. The operating frequency of the shift register which scans the rows of the displays is low. The width of the output transistors which are needed to charge and discharge the row capacitance increases with the size and resolution of the display. However, the gate area of these transistors remains a relatively small fraction of the total gate area of the transistors within the pixels of the display, even for displays approaching 20-inches diagonal.

The design of the column drive circuits is more demanding as they operate at high frequencies. Since the column voltage levels determine the brightness of the display the errors in the output voltages must be low. Column drive circuits based on multiplexers are used because of their simple operation which allows the column voltages to be accurately determined. The operating frequency of the column drive circuit can be traded off against the number of parallel video input signals which are used. It is an advantage to keep this number as low as possible, but as the size and resolution of the display increases a number of different factors may impose a minimum value of the number of video inputs which are required. This number is determined by the rate at which video information can be transferred from external circuitry to the columns of the display. During the design of the column drive circuit the factors which can limit the operating speed are the electrical properties of the columns in the display, the size of the transistors in the multiplexer switches which charge the column capacitance, the time constant of the video bus lines within the column drive circuit and the propagation delay of the signals used to control the multiplexer switches. Which of these aspects of the design determines the minimum number of video lines needed for the drive circuit depends on the detail of the design. In the examples given in chapter 5, the decision to set a limit on the maximum size of the transistors in the multiplexer switches was the factor which determined the number of video lines which are needed. If this restriction was removed, then for larger displays the time constant of the column electrode becomes the limiting factor, while for smaller
displays it is the time constant of the video bus lines within the drive circuit which set the minimum number of video lines required.

A prototype datagraphic display with integrated row and column drive circuits has been designed using low temperature poly-Si thin film transistors. The display had good contrast and uniformity, and the performance of the drive circuits was consistent with that estimated using simple design equations. Test multiplexing circuits have been used to perform an inspection of the display, detecting short and open circuits in the row and column electrodes. The display demonstrates that the laser crystallised poly-Si technology developed at PRL can be used to fabricate high quality active matrix liquid crystal displays.

The ability to integrate circuits onto the substrate of the display using TFTs leads to consideration of what other use could be made of such circuits. An example of signal processing within the pixels of an active matrix liquid crystal display was described in chapter 6. By integrating a simple digital to analogue converter within each pixel of the display, it is possible to use digital rather than analogue column signals simplifying the operation of the column drive circuit. The serial charge redistribution conversion technique was used because of the simplicity of the circuitry required within the pixel. Test pixels were designed and measurements carried out which demonstrated that this adaptation of a conventional active matrix pixel could be implemented practically. The measured differential non-linearity of the pixel converter circuits was relatively high, approximately 2 LSB for a 6-bit conversion. The cause of this was identified as the capacitance between the two half pixel electrodes which make up each converter pixel. The non-linearity could be corrected in a redesigned pixel by modifying the layout of the pixel either to reduce the value of the capacitance between the electrodes or by changing the ratio of the capacitance of the two half pixels. The time required to perform the pixel data conversion is an important aspect of the operation of the pixels as this must be consistent with the line frequency of the video signal source. The performance of the test pixels indicated that conversion times can be achieved which are compatible with a 6-bit conversion resolution in television and VGA data graphic displays using laser crystallised poly-Si transistors. Two methods for reducing the amount of time required for the conversion were proposed, using multi-level column data to reduce the number of conversion cycles required for a given resolution and interleaving the digital data applied to the column for two adjacent rows in the display.
With increasing integration of circuits on to the substrate of an active matrix display, the issue of circuit yield becomes important. A number of techniques for improving circuit yield were described in chapter 7, including a self testing approach to redundancy. This scheme involves the introduction of special testing circuits which test the operation of the redundant circuit elements and select one which passes the tests. To demonstrate the scheme a row drive circuit with self testing redundancy within its shift registers was designed and used to address a small display. The ability of the circuit to correct for short circuits within the shift registers of the row driver was demonstrated. The advantage of redundancy and repair techniques depends on the relative yield of the drive circuits compared to the yield of the active matrix of the display. A very simple yield analysis, based on the gate area of the transistors in the row drive circuit and in the pixels of the active matrix, indicated that for the circuit design considered, the yield of the shift registers without redundancy was higher than the yield of the active matrix. This suggests that while redundancy techniques are useful in a research laboratory where defects can be accepted within the display, in a production environment the need to achieve a high yield within the active matrix may result in a high yield of drive circuits without the need for redundancy techniques.

The work described in this thesis has covered a number of different aspects of circuit design using thin film transistors for active matrix liquid crystal displays. In the future some of these areas would benefit from further investigation. Laser crystallised poly-Si is currently a very immature technology. There is scope for optimisation of the structure of the transistors for use in circuits such as reducing parasitic capacitances, reducing device geometry, reducing the threshold voltage, increasing the field effect mobility and improving device uniformity. Such changes should increase the performance of TFT circuits, broadening the range of applications to which they could be applied. The issues of analogue circuit design using TFTs have not yet been widely investigated. The ability to produce high quality analogue TFT circuits would greatly enhance the possibilities for signal processing on displays or other large area electronics devices. As the technology develops integration of additional circuits onto the display substrate, such as those described in chapter 8, will become more practical.
Appendix A. Estimation of TFT charging times

Thin Film Transistors are often used as switches both in circuits and within the pixels of an active matrix display. It is possible to derive simple expressions for the charging time for such TFT switches by making the assumption that the drain current of the TFT can be approximated by the conventional MOS transistor equations. In most circumstances such an assumption will give acceptable results.

Consider first the case of a transistor used to charge a capacitor as indicated in Figure A-1. The initial voltage on the capacitor is $V_1$, the charging voltage is $V_2$, and the voltage on the gate of the TFT is $V_g$. Assuming that the TFT is operating in the linear region and $V_2 > V_1$ then the drain current when the voltage on the capacitor is equal to $V_c$ is given by:

$$ I_D = B \left( (V_g - V_c - V_e)(V_2 - V_c) - \frac{(V_2 - V_c)^2}{2} \right) $$

where $B = \frac{\varepsilon_{ox} \mu W}{L t_{ox}}$

The time required for the error in the voltage on the load capacitor to fall to $V_u$ is obtained by integrating the charging current.

$$ I_D = C \frac{dV_c}{dt} $$

therefore the charging time is given by the equation

$$ T_{ch} = \int_{V_1}^{V_u} \frac{C}{I_D} dV $$

Figure A-1 Pixel charging circuit
using the standard integral

\[
\int \frac{dx}{ax + x^2} = -\frac{1}{a} \log\left(\frac{a + x}{a}ight)
\]

\[
T_{ch} = \int_{V_1}^{V_2-V_u} \frac{C}{B((V_g-V_c-V_T)(V_2-V_c)-(V_2-V_c)^2/2)} dV_c
\]

\[
T_{ch} = \int_{V_1}^{V_2-V_u} \frac{2C/B}{2(V_g-V_2-V_T)(V_2-V_c)+(V_2-V_c)^2} dV_c
\]

\[
T_{ch} = \frac{C}{B} \left[ \frac{1}{(V_g-V_2-V_T)} \log\left(\frac{2(V_g-V_2-V_T)}{(V_2-V_c)}+1\right) \right]_{V_1}^{V_2-V_u}
\]

setting \( V_{gon} = V_g - V_T - V_2 \)

\[
T_{ch} = \frac{C}{B} \left[ \frac{1}{V_{gon}} \log\left(\frac{2V_{gon}}{(V_2-V_c)}+1\right) \right]_{V_1}^{V_2-V_u}
\]

\[
T_{ch} = \frac{C}{BV_{gon}} \log\left[ \frac{2V_{gon}}{V_u} + 1 \right]
\]

If \( V_2 < V_1 \) then the expression becomes

\[
T_{ch} = \frac{C}{BV_{gon}} \log\left[ \frac{2V_{gon}}{V_u} - 1 \right]
\]

A similar expression can be obtained for the case of a TFT connected between two equal valued capacitors as shown in Figure A-2. If the initial voltages on the capacitors are \( V_1 \) and \( V_2 \), assume that \( V_2 < V_1 \), then the voltages on the capacitors during the charge sharing process can be written as \( V_a-V_c \) and \( V_a+V_c \), where \( V_a = (V_1 + V_2)/2 \) and \( V_c = (V_1 - V_2)/2 \). The current flowing through the transistor and the time required for the error in the voltage on the capacitors to reach a value \( V_e \) can be evaluated from the expressions below.
\[ V_A - V_C = V_2 \quad \text{at} \ t = 0 \]
\[ V_A^+ V_C = V_1 \quad \text{at} \ t = 0 \]

\[ V_A = \frac{V_1 + V_2}{2} \]

**Figure A-2 Pixel charge redistribution**

\[ I_D = B((V_R - (V_A - V_C) - V_T)2V_C - \left(\frac{2V_C}{2}\right)^2) \quad \text{A-6} \]

\[ I_D = C \frac{d}{dt}(V_A - V_C) = -C \frac{dV_C}{dt} \quad \text{A-7} \]

\[ T_{ch} = -\int_{\frac{V_C}{2}}^{V_C} \frac{C}{I_D} dV_C \]

\[ T_{ch} = -\int_{\frac{V_C}{2}}^{V_C} \frac{C}{B((V_R - (V_A - V_C) - V_T)2V_C - \left(\frac{2V_C}{2}\right)^2)} dV_C \]

\[ T_{ch} = -\int_{\frac{V_C}{2}}^{V_C} \frac{C/B}{(V_R - V_A - V_T)(2V_C)} dV_C \]

\[ T_{ch} = \frac{C}{2B} \left[ \frac{1}{(V_R - V_A - V_T)} \log(V_C) \right]_{\frac{V_C}{2}}^{V_C} \]

define \( V_{gon} \) as \( V_g - V_T - V_A \) then:

\[ T_{ch} = -\frac{C}{2BV_{gon}} \log \left[ \frac{2V_{gon}}{V_1 - V_2} \right] \quad \text{A-8} \]
If $V_2 > V_I$ then the expression becomes

$$T_{ch} = -\frac{C}{2BV_{gon}} \log \left[ \frac{2V_u}{V_2 - V_I} \right]$$

A charging situation which is common in digital circuits is shown in Figure A-3. The circuit shows a NMOS transistor discharging a load capacitance which is initially at a voltage $V_I$ relative to the lower power supply rail. The transistor could for example be the pull down device in a digital inverter.

![Figure A-3 Discharge of a load capacitor](image)

The current flowing through the transistors is described by one of the two standard MOS device equations depending on whether it is operating in the saturated or linear regions.

When $V_c > V_g - V_T$

$$I_D = \frac{B(V_g - V_T)^2}{2}$$

When $V_c \leq V_g - V_T$

$$I_D = B \left( (V_g - V_T)V_c - \frac{V_c^2}{2} \right)$$

The charging time can be determined by integrating the current separately for the two operating regions. Since $V_c$ is decreasing for positive $I_D$

$$I_D = -C \frac{dV_c}{dt}$$
This equation can be applied to n-channel devices discharging a load or p-channel TFT charging a load by appropriately modifying the parameter values.
Appendix B  AMLCD Design Equations

The resistance and capacitance of the row and column electrodes in an active matrix display are needed in the design of the display drive circuits. In this section the electrical properties of a display and their dependence of the display size are estimated using the generalised pixel layout illustrated in Figure B-1.

![Simple pixel layout](image)

**Figure B-1 Simple pixel layout**

Most displays for computer and video applications have a 4:3 aspect ratio, that is the ratio of the picture width to the picture height is 4/3 and the ratio of the picture diagonal to the picture height is 5/3. The pitch of the row and column electrodes in the display can therefore be related to the display diagonal, d, by the equations below in which $N_{\text{row}}$ and $N_{\text{col}}$ are the number of rows and columns in the display.

\[
P_{\text{row}} = \frac{3d}{5N_{\text{row}}} \quad \text{B-1}
\]

\[
P_{\text{col}} = \frac{4d}{5N_{\text{col}}} \quad \text{B-2}
\]
The capacitance of a pixel in the display is made up of the liquid crystal capacitance and the pixel storage capacitance. Usually the value of the pixel storage capacitance is taken as a multiple of the liquid crystal capacitance and in this calculation it is assumed that \( C_{\text{storage}} = 3C_{\text{liquid\_crystal}} \). The liquid crystal capacitance can be estimated by assuming that the ITO pixel electrode occupies a constant fraction of the pixel area, assumed here to be 75%. Using the capacitance per unit area of the liquid crystal, \( C_{\text{LC}} \), the total pixel capacitance can be calculated.

\[
C_{\text{pixel}} = 0.75 \times 4 \times C_{\text{LC}} \times P_{\text{row}} \times P_{\text{col}}
\]

B-3

In Appendix A a charging equation was derived which allows the width of the pixel TFT required to charge the pixel capacitance to be calculated.

\[
T_{\text{ch}} = \frac{C_{\text{pixel}}}{BV_{\text{gon}}} \log \left[ \frac{2V_{\text{gon}}}{V_s} + 1 \right]
\]

\[
\left[ \frac{2V_{\text{gon}}}{V_s - V_t} + 1 \right]
\]

where \( V_{\text{gon}} = V_g - V_T - V_2 \) and \( B = \mu C_{\text{OX}} W_{\text{TFT}} / L \)

Taking \( V_g = 16 \text{V}, V_2 = 10 \text{V}, V_t = 0 \text{V}, V_T = 5 \text{V}, V_s = 0.01 \text{V} \)

\[
W_{\text{TFT}} = \frac{5.12 \times C_{\text{pixel}} L}{\mu C_{\text{OX}} T_{\text{ch}}}
\]

B-4

For smaller displays and high mobility transistors the calculated width of the transistor will be less than the minimum width which can be fabricated. In this case it is assumed that a device with a minimum width of 4\( \mu \text{m} \) is used.

The resistance of the column and row electrodes can be calculated from the sheet resistance of the column and row metalisation \( R_{\text{Scol}} \) and \( R_{\text{Srow}} \).

\[
R_{\text{col}} = \frac{3d R_{\text{Scol}}}{5W_{\text{col}}}
\]

B-5

\[
R_{\text{row}} = \frac{4d R_{\text{Srow}}}{5W_{\text{row}}}
\]

B-6
The capacitance of the column electrode is made up of four elements. The overlap capacitance between the column electrode and the row electrodes, the capacitance between the column electrode and the common electrode, the capacitance between the column electrode and the adjacent pixel electrodes and the capacitance at the source of the pixel transistors connected to the column. The first and last of these elements can be estimated quite easily using the overlap area of the row and column electrodes and the overlap capacitance of the pixel TFT.

The capacitance of the crossover between the column and row can be estimated using the capacitance per unit area of the crossover insulator $C_{XO}$:

$$C_{\text{crossover}} = C_{XO} W_{\text{col}} W_{\text{row}}$$  \hspace{1cm} B-7

The overlap capacitance of the pixel TFT can be calculated using the value of the gate overlap length $L_o$:

$$C_{\text{TFT\_overlap}} = C_{XO} W_{\text{TFT}} L_o$$  \hspace{1cm} B-8

The capacitance between the column and the common electrode and between the column and the adjacent pixels are more difficult to estimate since edge effects play a major role in determining their values. The capacitance per unit length of a column electrode located between two pixel electrodes has been simulated using a layout simulation program, "Fasterix". The structure which was modelled and the resulting capacitance values are illustrated in Figure B-2. For comparison the capacitance between the column and the common electrode calculated using a parallel plate approximation is also shown. As the width of the column electrode becomes comparable to the separation of the common electrode and the column electrode, the significance of the contribution to the capacitance from edge effects increases. With a column electrode width of 5$\mu$m the capacitance is almost twice the value calculated using a simple parallel plate approximation. This indicates the importance of taking edge effects into account when designing an active matrix LC display. The dependence of the capacitance between the column electrode and the common electrode on the column width can be approximated by the equation

$$C_{\text{column\_to\_common\_electrode}} = 35.2 \times 10^{-12} + W_{\text{col}} 10.35 \times 10^{-6} \hspace{1cm} \text{pF/m}$$  \hspace{1cm} B-9
The capacitance between the column electrode and the adjacent pixels represents a significant fraction of the column capacitance when the column width is small. Its value does not have a strong dependence on the column width and for simplicity it can be assumed that it has a constant value. In fact this capacitance will appear in series with the pixel capacitance but since its value will be much lower than the pixel capacitance it is a reasonable approximation to use its full value.

\[ C_{\text{column to pixel}} = 40 \times 10^{-12} \text{ pF/m} \]

Figure B-2 Calculated column capacitances including edge effect

The capacitance of the row electrode is made up of five elements. The capacitance between the row electrode and the common electrode, the capacitance between the row electrode and the adjacent pixel electrode, the capacitance between the row electrode and the column electrodes the capacitance of the gates of the TFTs and the capacitance of the pixel storage capacitors connected to the row. The first two elements can be approximated using similar expressions to those used for the column electrode, equations 9 and 10.
above. The capacitance between the row electrode and a column electrode has already
been given by equation 7 while the gate capacitance of the pixel transistor can be
approximated by the equation below.

\[ C_{TFT_{\text{gate}}} = C_{OX} W_{TFT} (2L_o + L) \] B-11

The load capacitance on the row electrode resulting from the connections to the pixel
storage capacitors in the adjacent row of pixels has two possible values depending on
whether or not the storage capacitor is being charged by its associated pixel TFT. When
the TFT is turned off the storage capacitor appears in series with the liquid crystal
capacitance, which is one third of the value of the storage capacitor, resulting in an
effective capacitance of \(3C_{\text{pixel}}/16\). When the pixel is being charged the full value of the
storage capacitor, \(3C_{\text{pixel}}/4\), is applied to the row.

Using the equations above, the resistance and capacitance of both the row and column
electrodes can be calculated once the row and column widths are known. Simple rules can
be used to determine the required widths. In the case of the column electrode, the width
has been set equal to 15% of the column pitch. If this value is less than the minimum line
width, 5μm, then a value of 5μm is used. The row electrode width can be selected to give
a row RC time constant which is lower than a certain value. A figure of 1μs has been
chosen and this is calculated using the lower value of the additional capacitance from the
pixel storage capacitors. If the calculated row width is less than the minimum line width
then a value of 5μm is assumed. The display properties calculated using these rules are
illustrated in the following figures. The values of the parameters used are summarised in
Table B-1.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Liquid crystal thickness (μm)</td>
<td>4.5</td>
</tr>
<tr>
<td>Liquid crystal dielectric constant</td>
<td>4.6</td>
</tr>
<tr>
<td>TFT gate oxide thickness (μm)</td>
<td>0.15</td>
</tr>
<tr>
<td>TFT gate oxide dielectric constant</td>
<td>3.9</td>
</tr>
<tr>
<td>Crossover oxide thickness (μm)</td>
<td>0.3</td>
</tr>
<tr>
<td>Crossover oxide dielectric constant</td>
<td>3.9</td>
</tr>
<tr>
<td>Pixel TFT gate length (μm)</td>
<td>6</td>
</tr>
<tr>
<td>Pixel TFT gate-drain overlap (μm)</td>
<td>6</td>
</tr>
<tr>
<td>Pixel TFT mobility (cm²/Vs)</td>
<td>100</td>
</tr>
<tr>
<td>Pixel storage capacitor ratio C_S/C_LC</td>
<td>3</td>
</tr>
<tr>
<td>Sheet resistance of column metalisation (Ω/□)</td>
<td>0.15</td>
</tr>
<tr>
<td>Sheet resistance of row metalisation (Ω/□)</td>
<td>0.15</td>
</tr>
<tr>
<td>Maximum value of R_ROW*C_ROW (μs)</td>
<td>1</td>
</tr>
<tr>
<td>Fraction of pixel area covered by ITO electrode (%)</td>
<td>0.75</td>
</tr>
<tr>
<td>Minimum value of pixel TFT width (μm)</td>
<td>4</td>
</tr>
<tr>
<td>Column width/Column pitch</td>
<td>0.15</td>
</tr>
<tr>
<td>Minimum column width (μm)</td>
<td>5</td>
</tr>
<tr>
<td>Minimum row width (μm)</td>
<td>5</td>
</tr>
<tr>
<td>VGA display rows</td>
<td>480</td>
</tr>
<tr>
<td>VGA display columns</td>
<td>640x3</td>
</tr>
<tr>
<td>VGA display pixel clock frequency (MHz)</td>
<td>25.175</td>
</tr>
<tr>
<td>VGA display pixel voltage settling time (μs)</td>
<td>4</td>
</tr>
<tr>
<td>SVGA display rows</td>
<td>600</td>
</tr>
<tr>
<td>SVGA display columns</td>
<td>800x3</td>
</tr>
<tr>
<td>SVGA display pixel clock frequency (MHz)</td>
<td>40</td>
</tr>
<tr>
<td>SVGA display pixel voltage settling time (μs)</td>
<td>4</td>
</tr>
<tr>
<td>XGA display rows</td>
<td>768</td>
</tr>
<tr>
<td>XGA display columns</td>
<td>1024x3</td>
</tr>
<tr>
<td>XGA display pixel clock frequency (MHz)</td>
<td>65</td>
</tr>
<tr>
<td>XGA display pixel voltage settling time (μs)</td>
<td>4</td>
</tr>
</tbody>
</table>

Table B-1 Parameters used in calculating display resistances and capacitances

Figure B-5 shows how the width of the column and row electrodes and the pixel TFT vary with the display size for a VGA resolution display. The column width increases linearly...
with the display diagonal above a value of 5μm as it represents a constant fraction of the column pitch. The width of the pixel transistor increases with the square of the display diagonal since it is proportional to the capacitance of the pixel and therefore its area. The row electrode width has a complex dependence on the display diagonal and increases approximately exponentially.

Figure B-3 Variation of column, row and TFT width with VGA display diagonal

Figure B-4 Variation of row and column resistance with VGA display diagonal
The resistance of the column electrode shown in Figure B-4 becomes constant as its width increases above 5\( \mu \)m as both the width and the length increase in proportion to the display diagonal. The row resistance increases to a maximum value after which it decreases in proportion to the increase in row capacitance in order to maintain the RC time constant at a value of 1\( \mu \)s.

Figure B-5 Variation of column and row capacitance with VGA display diagonal

The capacitance of both the row and column electrodes shown in Figure B-5 has a complex dependence on the display diagonal which is approximately exponential for displays larger than 4 inches.
Appendix C. CMOS switch maximum resistance

Figure C-1 Operating regions of a CMOS transmission gate

The operating regions of a CMOS transmission gate are shown in the figure above. The maximum resistance of the transmission gate can be estimated by assuming that the behaviour of the transistors can be described by the conventional MOS device equations. Shoji [M. Shoji 1988] analysed the conductance of a CMOS transmission gate and showed that the conductance of a symmetric transmission gate, $\beta_n = \beta_p$, is independent of $V_1$ and $V_2$ in the region where neither device is saturated if back-bias effects are ignored. In this appendix the value of the minimum conductance of the transmission gate is obtained for $\beta_n \neq \beta_p$ and for values of $V_1$ and $V_2$ within the range $VSS$ to $VDD$.

The symmetry of the transmission gate means that it is only necessary to consider the operation in the region where $V_2$ is greater than or equal to $V_1$. For transistors operating in the sub-threshold region assume that

\[
I_n = 0, \quad G_n = 0
\]

\[
I_p = 0, \quad G_p = 0
\]
For operation in the linear region the standard MOS device equations are used

\[ I_n = \beta_n \left( (VDD - V_{tn} - V1)(V2 - V1) - \frac{(V2 - V1)^2}{2} \right) \]

\[ G_n = \frac{I_n}{(V2 - V1)} = \beta_n \left( VDD - V_{tn} - \frac{(V2 + V1)}{2} \right) \quad \text{C-1} \]

\[ I_p = \beta_p \left( (-VSS + V_{tp} + V2)(V2 - V1) - \frac{(V2 - V1)^2}{2} \right) \]

\[ G_p = \frac{I_p}{(V2 - V1)} = \beta_p \left( -VSS + V_{tp} + \frac{(V2 + V1)}{2} \right) \quad \text{C-2} \]

For devices in saturation

\[ I_n = \frac{\beta_n}{2} (VDD - V_{tn} - V1)^2 \]

\[ G_n = \frac{\beta_n (VDD - V_{tn} - V1)^2}{2(V2 - V1)} \quad \text{C-3} \]

\[ I_p = \frac{\beta_p}{2} (-VSS + V_{tp} + V2)^2 \]

\[ G_p = \frac{\beta_p (-VSS + V_{tp} + V2)^2}{2(V2 - V1)} \quad \text{C-4} \]

The conductance of the CMOS transmission gate is simply the sum of the conductance of the n-type and p-type transistors. Consider operation in region 1 where both the n-channel and p-channel devices are operating in the linear region. The conductance of the CMOS transmission gate is

\[ G = \beta_n \left( VDD - V_{tn} - \frac{(V2 + V1)}{2} \right) + \beta_p \left( -VSS + V_{tp} + \frac{(V2 + V1)}{2} \right) \quad \text{C-5} \]
Taking the derivative of $G$ with respect to $V_1$ and $V_2$ reveals how the conductance of the transmission gate varies within region 1.

$$\frac{\partial G}{\partial V_1} = \frac{\beta_p - \beta_n}{2}, \quad \frac{\partial G}{\partial V_2} = \frac{\beta_p - \beta_n}{2}$$

This result shows that for ideal transistors if $\beta_n = \beta_p$ then the conductance of the transmission gate in region 1 is constant, independent of $V_1$ and $V_2$, with a value given by

$$G = \beta(V_{DD} - V_{SS} + V_{tp} - V_{tn})$$

However if $\beta_n \neq \beta_p$ then the conductance changes linearly with respect to $V_1$ and $V_2$ with a slope of $0.5(\beta_p - \beta_n)$.

If $\beta_n > \beta_p$ then the conductance will decrease as $V_1$ and $V_2$ increase resulting in a minimum value for the conductance when $V_1 = V_2 = V_{DD} - V_{tn}$ and given by the equation

$$G_{\text{min}} = \beta_p(V_{DD} - V_{SS} + V_{tp} - V_{tn}).$$

If $\beta_n < \beta_p$ then the conductance will increase as $V_1$ and $V_2$ increase leading to a minimum value of conductance when $V_1 = V_2 = V_{SS} - V_{tp}$ and given by the equation

$$G_{\text{min}} = \beta_n(V_{DD} - V_{SS} + V_{tp} - V_{tn}).$$

To establish whether these minimum values represent the minimum value of conductance over all operating regions consider how the conductance varies within the other regions. Moving from region 1 to region 3 the conductance is determined by the sub-threshold behaviour of the p-channel transistor and the linear behaviour of the n-channel device so

$$G = \beta_p\left(V_{DD} - V_{tn} - \frac{(V_2 + V_1)}{2}\right) + 0 \quad C-6$$

Clearly as $V_1$ and $V_2$ decrease the conductance in region 3 increases therefore the conduction in region 3 will not be lower than that in region 1. A similar argument can be applied to region 5 so that this region will also not encompass a conductance value which is lower than the minimum in region 1.
In region 6 both transistors are operating in saturation therefore the conductance of the switch can be written as

\[ G = \frac{\beta_n (V_{DD} - V_{tn} - V_1)^2}{2(V_2 - V_1)} + \frac{\beta_p (-V_{SS} + V_{tp} + V_2)^2}{2(V_2 - V_1)} \quad (C-7) \]

Can it be shown that this value of conductance is always greater than or equal to the minimum value within region 1? The relationship to be proved is given below where \( \beta_{min} \) is the smaller of \( \beta_n \) and \( \beta_p \).

\[ \frac{\beta_n (V_{DD} - V_{tn} - V_1)^2}{2(V_2 - V_1)} + \frac{\beta_p (-V_{SS} + V_{tp} + V_2)^2}{2(V_2 - V_1)} \geq \beta_{min} \left( V_{DD} - V_{SS} + V_{tp} - V_{tn} \right) \]

Make the substitutions

\[ V_1 = V_{SS} - V_{tp} - \tilde{V}_i \quad \text{so that in region 6 } \tilde{V}_i \geq 0 \]

\[ V_2 = V_{DD} - V_{tn} + \tilde{V}_2 \quad \text{so that in region 6 } \tilde{V}_2 \geq 0 \]

\[ V_x = V_{DD} - V_{tn} - V_{SS} + V_{tp} \quad \text{and set the condition that } V_x \geq 0 \]

then show that

\[ \frac{\beta_n (V_x + \tilde{V}_i)^2 + \beta_p (V_x + \tilde{V}_2)^2}{2(V_x + \tilde{V}_i + \tilde{V}_2)} \geq \beta_{min} V_x \]

\[ \beta_n (V_x + \tilde{V}_i)^2 + \beta_p (V_x + \tilde{V}_2)^2 - \beta_{min} V_x \frac{2(V_x + \tilde{V}_i + \tilde{V}_2)}{2} \geq 0 \]

\[ (\beta_n + \beta_p - 2\beta_{min})V_x^2 + 2(\beta_n - \beta_{min})\tilde{V}_i V_x + 2(\beta_p - \beta_{min})\tilde{V}_2 V_x + \beta_n \tilde{V}_i^2 + \beta_p \tilde{V}_2^2 \geq 0 \]

Since \( \beta_n \) and \( \beta_p \) are greater than or equal to \( \beta_{min} \) all terms on the left of this equation are positive or zero and therefore the condition is satisfied within region 6. The conductance in region 6 is therefore no lower than the minimum value in region 1.

Apply the same approach to the conductance in region 2 where the p-channel device is saturated and the n-channel transistor is operating in the linear region. The conductance of the transmission gate in this region is given by
The condition to be proved is that

\[ G = \beta_n \left( VDD - V_{tn} - \frac{(V_2 + V_1)}{2} \right) + \frac{\beta_p \left( -VSS + V_{tp} + V_2 \right)^2}{2(V_2 - V_1)} \geq \beta_{mn} \left( VDD - VSS + V_{tp} - V_{tn} \right) \]

Make the substitutions

\[ V_1 = VSS - V_{tp} - \bar{V}_1 \quad \text{so that in region } 2 \bar{V}_1 \geq 0 \]
\[ V_2 = VSS - V_{tp} + \bar{V}_2 \quad \text{so that in region } 2 \bar{V}_2 \geq 0 \]
\[ V_x = VDD - V_{tn} - VSS + V_{tp} \quad \text{and set the condition that } V_x \geq 0 \]

then show that

\[ \beta_n \left( V_x - \frac{(\bar{V}_2 - \bar{V}_1)}{2} \right) + \frac{\beta_p \bar{V}_2^2}{2(\bar{V}_1 + \bar{V}_2)} \geq \beta_{mn} V_x \]

\[ \beta_n 2(\bar{V}_1 + \bar{V}_2) \left( V_x - \frac{(\bar{V}_2 - \bar{V}_1)}{2} \right) + \beta_p \bar{V}_2^2 - \beta_{mn} V_x 2(\bar{V}_1 + \bar{V}_2) \geq 0 \]

\[ 2(\beta_n - \beta_{mn})(\bar{V}_1 + \bar{V}_2)V_x - \beta_n (\bar{V}_2^2 - \bar{V}_1^2) + \beta_p \bar{V}_2^2 \geq 0 \]

\[ 2(\beta_n - \beta_{mn})(\bar{V}_1 + \bar{V}_2)V_x + \beta_n \bar{V}_1^2 + (\beta_p - \beta_n) \bar{V}_2^2 \geq 0 \]

All the terms on the left of this equation are positive if \( \beta_n \) is less than \( \beta_p \). If \( \beta_n \) is greater than \( \beta_p \) then \( \beta_{mn} \) is equal to \( \beta_p \) therefore

\[ 2(\beta_n - \beta_p)(\bar{V}_1 + \bar{V}_2)V_x + \beta_n \bar{V}_1^2 + (\beta_p - \beta_n) \bar{V}_2^2 \geq 0 \]

\[ (\beta_n - \beta_p)(2(\bar{V}_1 + \bar{V}_2)V_x - \bar{V}_2^2) + \beta_n \bar{V}_1^2 \geq 0 \]
All terms on the left of the equation are positive if \( 2(\bar{V}_1 + \bar{V}_2)V_x - \bar{V}_2^2 \geq 0 \). The worst case is if \( \bar{V}_1 = 0 \) when the equation can be simplified to \( 2V_x - \bar{V}_2 \geq 0 \). Within region 2 the value of \( \bar{V}_2 \) ranges from 0 to \( V_x = VDD - V_{jn} - VSS + V_{jn} \) therefore this equation is satisfied and the minimum value of conductance within region 2 is less than that within region 1.

Within region 4 the p-channel device operates in the linear region and the n-channel transistor is saturated and by the same arguments it can be shown that in this region the minimum conductance is higher than the minimum value in region 1.

In summary the minimum conductance of the CMOS transmission gate based on the basic MOS transistor current equations has a value of \( G_{\text{min}} = \beta_{\text{min}}(VDD - VSS + V_{Tp} - V_{jn}) \) where \( \beta_{\text{min}} \) is the smaller of \( \beta_n \) and \( \beta_p \). If \( \beta_n = \beta_p \) then the minimum conductance occurs while both transistors are operating in the linear region, \( VSS - V_{Tp} < V1 < VDD - V_{Tn} \) and \( VSS - V_{Tp} < V2 < VDD - V_{Tn} \). If \( \beta_n > \beta_p \) then the minimum conductance occurs when \( V1 = V2 = VSS - V_{Tp} \) while if \( \beta_n < \beta_p \) the minimum conductance occurs when \( V1 = V2 = VDD - V_{Tn} \).
References


M Edwards P3  M J Edwards, “Improved pixel D/A circuit”, United Kingdom patent application, 9525638.4


<table>
<thead>
<tr>
<th>Year</th>
<th>Author(s)</th>
<th>Title and Details</th>
</tr>
</thead>
</table>


Y Morimoto 1995  

T Morita 1995  

S Morozumi 1984  

H Nakamura 1994  

Nikkei Microdevices 1996  

Y Nishihara 1992  

Y Oana 1996  

H Okada 1992  

H Okada 1995  

T Ohori 1996  

H Ohshima 1993  

J Ohwada 1989  

Philips ED&T  

PRL  
C Reita 1994  

I De Rycke 1990  

J Salerno 1992  

M. Schadt 1971  

H Sekine 1997  

K Sera 1994  
K Sera, “Low Temperature Poly-Si TFTs and Their Application for the Fluorescent Light Sources”, International Workshop on Active Matrix Liquid Crystal Displays, AM-LCD 94, November 1994, pp100-103.

T Shima 1995  

M Shoji 1988  

J Smith 1996  
J Smith, “Who dares to challenge the CRT?”, Proceedings of 16th IDRC, Euro Display’96, pp5-6

C Stapper 1989  

R Stewart 1990  

R Stewart 1995  

E Suarez 1975  

S Sze 1981  


