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To cite this article: Shun Chan *et al* 2019 *J. Phys. D: Appl. Phys.* **52** 505108

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Investigation into the current loss in InAs/GaAs quantum dot solar cells with Si-doped quantum dots

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Received 29 August 2019

Accepted for publication 4 September 2019

Published 4 October 2019



Abstract

Our previous studies have shown that introducing Si doping in quantum dots (QDs) can help QD solar cells achieve higher voltage. However, this improvement came at the cost of current loss. In this work, we continue to investigate the cause of the current loss and propose a method to recover it without compromising the voltage. Photoluminescence measurements have confirmed that optimizing the thickness of the GaAs layers in the i-region can lead to strong current gain (~14%) with minimal voltage loss (<3%) and alteration of the QD quality. The capacitance–voltage measurement results support that the current gain mainly originates from the increased depletion width.

Keywords: MBE, QDSC, current recovery

(Some figures may appear in colour only in the online journal)

1. Introduction

There is no doubt that recent discoveries with CdSe quantum dot (QD) solar cells (SCs), polymer SCs, and in particular, perovskite SCs have made a huge impact on the photovoltaic research field, merited by their cost-effectiveness and environmental-friendliness. However, there is one significant feature which keeps traditional GaAs SCs in the competition—stability—despite their high cost of production. Furthermore, the theory of intermediate band solar cells (IBSC) can be readily applied to GaAs SCs and has the potential to exceed the Shockley-Queisser limit by one fold—63% [1, 2]. Nano-scaled QDs exhibit discrete energy levels and zero density of state and hence are a suitable material to implement the intermediate band [3]. Although much attention has been drawn towards the novel SCs in recent years, QD solar cells (QDSC) have made solid progress towards their theoretical maximum efficiency [4–8].

In the early stage of our research, InAs QDs were embedded in the GaAs SC to fabricate a QDSC [9, 10]. The cell performance was very promising as the InAs QDs promoted sub-bandgap absorption and hence a large enhancement in current density [11, 12]. However, such an improvement was undermined by the voltage loss; the formation of wetting layers below the QDs can increase the dimensionality of the QDs to quantum wells (QWs) thus leaving the device susceptible to thermal carrier escape [13, 14]. To this end, our more recent works explored solutions to eliminate the wetting layers or to suppress the thermal carrier escape [15–19]. For example, introducing Si doping in InAs QDs resulted in voltage recovery of up to 72 % (0.105 V) of the lost voltage (0.145 V). Yet, the voltage enhancement by QD Si doping was accompanied by depletion width shrinkage [16].

The width of the depletion region is typically associated with the doping levels, via the following equation [20]:

$$W = \sqrt{\frac{2\varepsilon}{q} V_0 \left(\frac{1}{N_A} + \frac{1}{N_D} \right)}, \quad (1)$$

where W is the width of the depletion region, N_A and N_D are the acceptor and donor concentration, which in this case are

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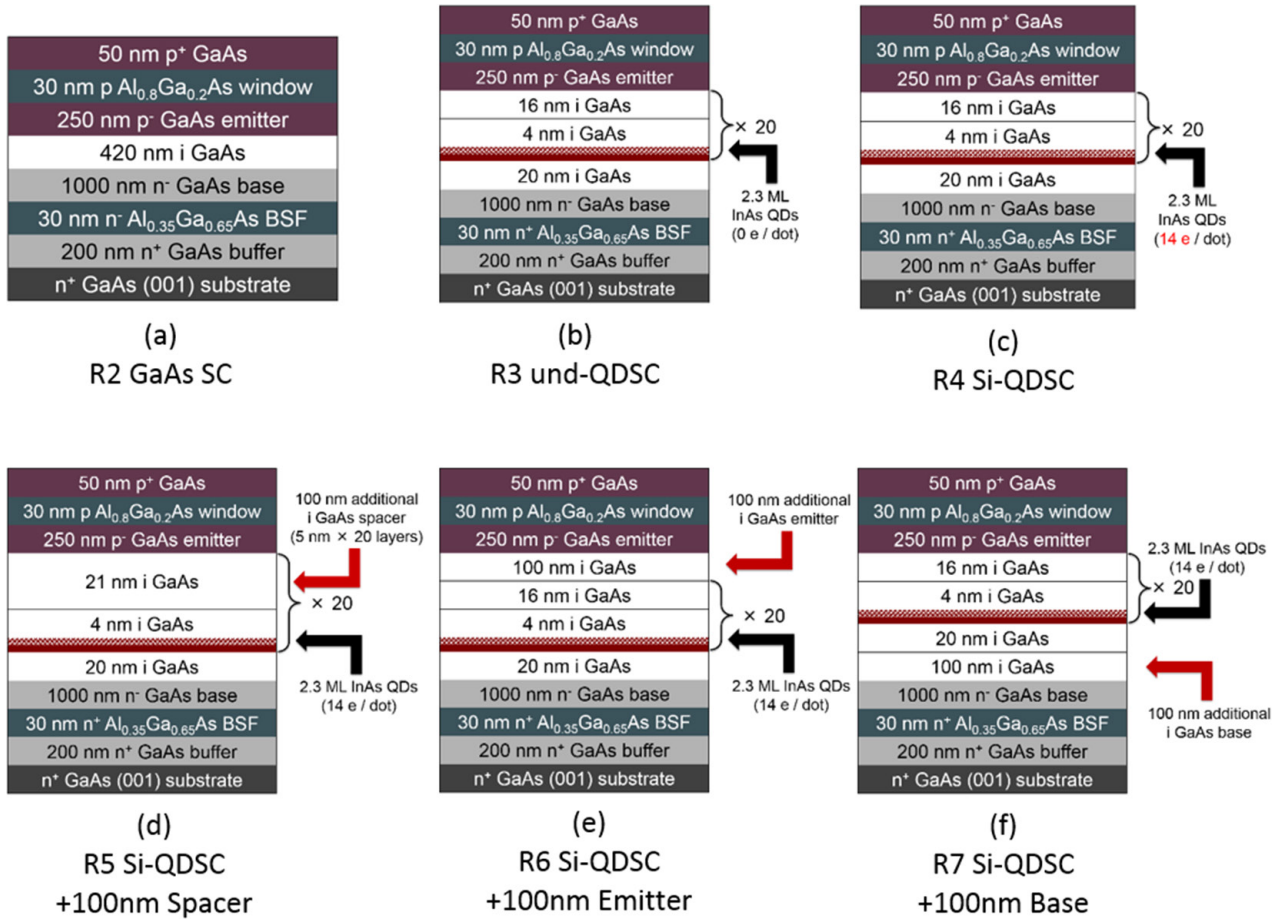


Figure 1. Schematics of p-i-n SC structures.

directly related to the doping level. ϵ , q and V_0 are less relevant constants and hence are omitted here.

Equation (1) suggests that the introduction of Si dopants would lead to an increase in N_D and a shrinkage in W . As the effective area of absorption of SCs are proportional to W , this in turn decreases the current output of the SCs.

In this work, we continue to investigate the current loss caused by QD Si doping in InAs/GaAs QDSCs, and propose a solution to maintain a high level of Si doping without reducing the width of the depletion region. To achieve this, extra i-GaAs layers have been inserted in the i-region of the p-i-n GaAs SC in an attempt to recover the width of the depletion region lost to the high level of QD Si doping. Current density–voltage (J – V) characteristics have shown notable current gain (14%) with minimal voltage loss (<3%) and external quantum efficiency (EQE) data confirmed the current gain originates from the additional intrinsic layers. Furthermore, capacitance–voltage (C – V) measurements have provided solid evidence for the shrinkage of the depletion width after Si doping (500 nm to 176 nm) and the lengthening of the depletion width with additional intrinsic layers (176 nm to 260 nm).

2. Experimental work

Figure 1 presents the p-i-n SC structures. All SC samples were grown by molecular beam epitaxy on n^+ GaAs (001) substrates. The original GaAs SC structure (R2) consists of a 200 nm n^+ GaAs buffer ($2 \times 10^{18} \text{ cm}^{-3}$), 30 nm n^-

$\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ back surface field ($2 \times 10^{18} \text{ cm}^{-3}$), 1000 nm n^- GaAs base ($1 \times 10^{17} \text{ cm}^{-3}$), 420 nm i GaAs, 250 nm p^- GaAs emitter ($2 \times 10^{18} \text{ cm}^{-3}$), 30 nm $p \text{ Al}_{0.8}\text{Ga}_{0.2}\text{As}$ window ($2 \times 10^{18} \text{ cm}^{-3}$) and 50 nm p^+ GaAs ($1 \times 10^{19} \text{ cm}^{-3}$). For the undoped QDSC (R3), a 420 nm i GaAs layer is replaced by 20 layers of 2.3 monolayer InAs QDs with a (4 + 16) nm spacer layer [17, 21]. The Si-QDSC (R4) differs by introducing Si dopants into the InAs QD layers at a doping density of $1 \times 10^{13} \text{ cm}^{-3}$ which is equivalent to 14 electrons per dot.

The thicker QDSCs (R5, R6, R7) contain an additional 100 nm i GaAs layer with respect to the Si-QDSC (R4). The thick spacer QDSC (R5) gain an additional layer by increasing each spacer layer by 5 nm ($20 \times 5 \text{ nm}$) whereas the thick emitter (R6) and thick base (R7) QDSCs increase thickness by inserting the additional layer above or below the InAs QD layers, respectively.

Device fabrication procedures involved sample cleaning and ultrasonication in acetone and isopropanol solution for 10 min each, followed by surface deoxidation in dilute ammonia (1:19) solution for 50 s. Ni/Au–Ge (88:12)/Ni/Au layers (10/100/30/200 nm) were thermally evaporated onto the backside of the samples to form n-type contacts. In similar procedures for the p-type contacts, a 200 nm Au–Zn (95:5) layer was thermally evaporated through a shadow mask to define the SC grid patterns. All devices underwent thermal annealing at 400 °C for 60 s to further enhance the ohmic contacts [22]. No anti-reflective coating or surface passivation was applied.

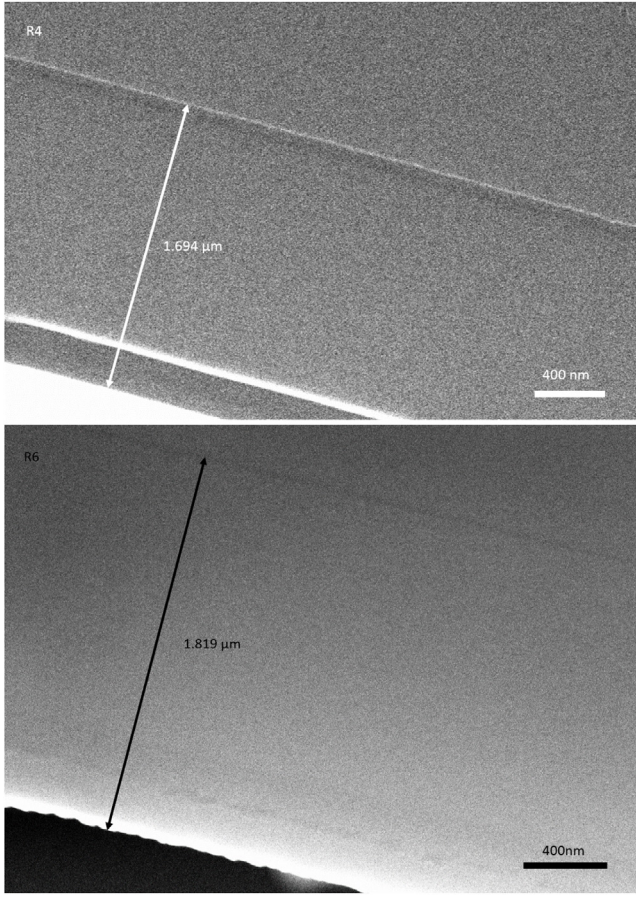


Figure 2. Cross-sectional scanning electron microscopy of (a) R4 and (b) R6.

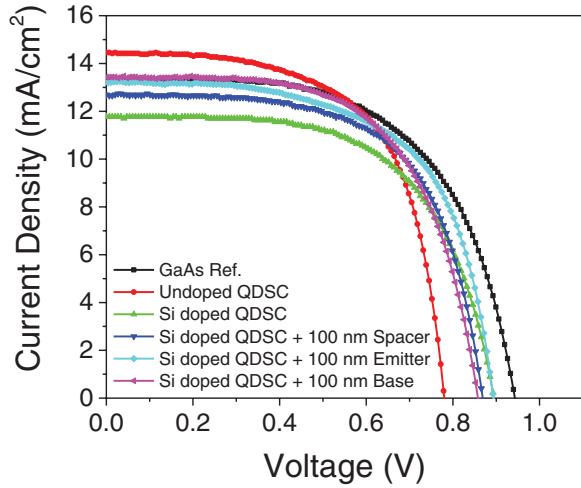


Figure 3. Current density–voltage characteristics of GaAs SC and QDSCs under 1 sun (AM1.5G) illumination.

Photoluminescence (PL) measurements were performed using 532 nm excitation from a diode-pumped solid-state laser, at 10 K and 300 K which was controlled by a He-cooled cryostat during the measurement. The J – V characteristics were obtained using a LOT calibrated solar simulator with a xenon lamp under 1 sun AM1.5G illumination at room temperature. Photocurrent measurements were carried out using a halogen

Table 1. J – V characteristics.

Device	J_{sc} (mA cm ^{−2})	V_{oc} (V)	FF (%)	η (%)
GaAs	13.37	0.942	59.70	7.52
Undoped	14.42	0.779	62.73	7.05
Si doped	11.74	0.894	61.06	6.41
Thick spacer	12.70	0.869	63.09	6.96
Thick emitter	13.20	0.892	60.52	7.13
Thick base	13.45	0.857	61.47	7.09

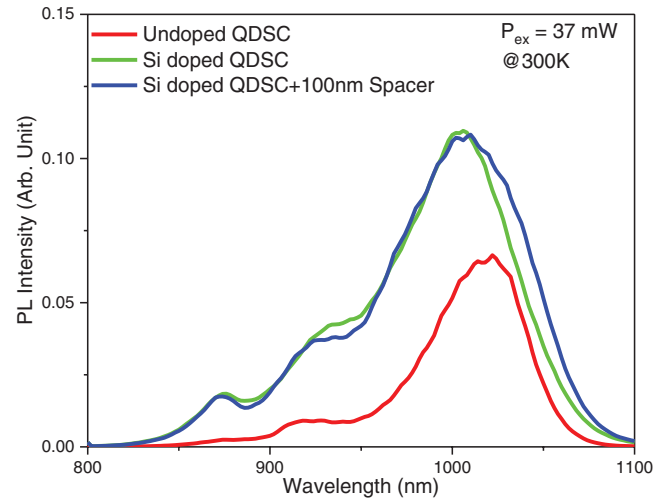
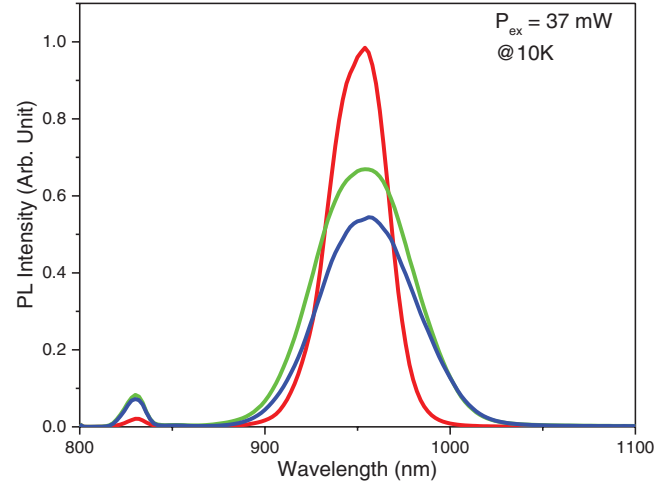


Figure 4. PL spectra of QDSCs at (a) 10 K and (b) 300 K.

lamp with a light beam chopped at a frequency of 188 Hz through a Newport monochromator. The monochromatic beam was calibrated to a GaAs photodiode and data were processed to obtain the EQE. The C – V characteristics were measured using a four-point probe station connected to a Keithley 4200 sourcemeter.

3. Results and discussion

Figure 2 illustrates the cross-sectional SEM image of the Si-doped QDSC (R4) and the thicker Si-doped QDSC (R6). The thickness of the samples were 1.694 μ m and 1.819 μ m, respectively, measured from the AlGaAs back surface frontier

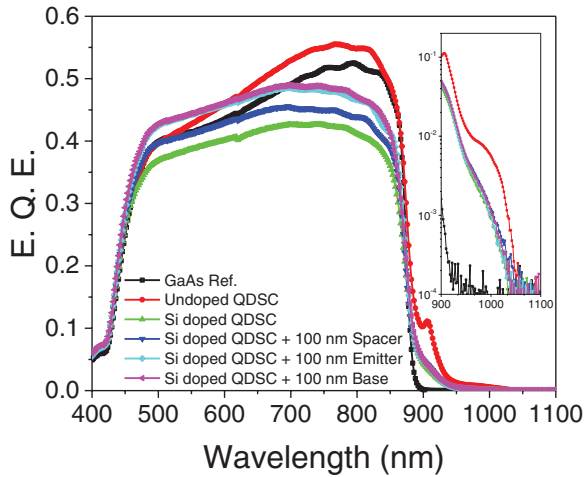


Figure 5. EQE of SCs.

layers. This confirms that the grown samples thicknesses are accurate and that the thickness of the additional intrinsic layers was 100 nm.

Table 1 and figure 3 show the J - V characteristics of the samples. The GaAs SC (R2) has achieved 0.942 V open-circuit voltage (V_{oc}) and 13.37 mA cm^{-2} short-circuit current density (J_{sc}). By inserting 20 layers of QDs, the undoped QDSC (R3) increased J_{sc} by 1.05 mA cm^{-2} however the V_{oc} decreased significantly. This observation was commonly reported in the early stage of research and the cause of this behaviour was due to the thermal communication between the IB and conduction band (CB), through wetting layers where the energy levels are continuous instead of discrete. Such energy level configuration provides multiple paths for carriers to be excited or relaxed, some 'easier' or 'shorter' paths require less energy for transmission. In other words, carriers with lower energy are able to be excited, which in turn reduces the effective energy bandgap and thus results in a lower voltage output [23].

To recover V_{oc} , Si dopants have been introduced into the QDs, such a technique has enabled Si-doped QDSC (R4) to regain V_{oc} back to 0.894 V but with a slight decrease in J_{sc} . The recovery in voltage was due to the thermal decoupling of the IB and CB, the Si dopants which were embedded within the QDs can create an energy barrier at the interface of the QD and carriers; in this way, the lost voltage is retrieved. The reduction in J_{sc} was due to the Si dopants also having an influence on the depletion region width and hence reducing the effective absorption area. From equation (1), Si dopants are regarded as donor carriers hence increasing the Si concentration would decrease the depletion region width. As most of the photon absorptions occur in the depletion region, a shorter depletion width would no doubt reduce the amount of absorption and thus cause the current density to decrease.

Here commences the main focus of our investigation, to counter the J_{sc} reduction, an additional 100 nm intrinsic layers have been inserted into the spacer, emitter or base region. The V_{oc} of the thicker QDSCs (R5, R6, R7) are analogous to the Si-doped QDSC ($\sim 0.87 \text{ V}$) indicating negligible voltage loss through the additional intrinsic layers; minor voltage differences are within the wafer inequality tolerance ($<3\%$). In

Table 2. C - V characteristics.

Device	Capacitance (nF)	Area (cm^2)	Depletion width (nm)
GaAs	6.53	0.336	496
Undoped	6.76	0.351	500
Si doped	19.1	0.348	175
Thick spacer	12.6	0.306	233
Thick emitter	11.5	0.311	261
Thick base	13.8	0.371	259

terms of J_{sc} , all three thicker QDSCs have achieved higher J_{sc} than Si doped QDSC, indicating that additional intrinsic layers have increased effective absorption area. Among the thicker QDSCs, the thick emitter QDSC (R6) has a very similar J_{sc} with respect to the thick base QDSC (R7), demonstrating that inserting the intrinsic layer above or below the QD layers has the same impact on the effective absorption area. On the other hand, the thick spacer QDSC (R5) has achieved slightly less J_{sc} compared to the other two— 12.69 mA cm^{-2} . This result is below our expectation, as increasing the spacer layer thickness should improve the QD quality as well as the effective absorption area hence we expected the J_{sc} to be the highest amongst all.

To understand the cause of this unexpected outcome, PL measurements were carried out. Figures 4(a) and (b) compare the PL spectra of the samples at 10 K and 300 K. The attributes of QDs are reflected by the intensity, position and full width at half maximum (FWHM) of the peaks. At 10 K, the Si doped QDSC is analogous to the thick spacer QDSC in terms of peak position (955 nm) and FWHM (59 nm). At 300 K, these two samples also show similar attributes, i.e. peak positions at 1010 nm and FWHM at 65 nm and 70 nm respectively. It appears that the changes of QD attributes under different temperature conditions are identical, hence we assume that increasing the spacer layer thickness has not altered QD size nor QD distribution; perhaps the increase in layer thickness (by 5 nm) is either not large enough to show a clear enhancement or the QD quality has already reached its optimum condition with a 16 nm spacer layer thickness, thus the additional thickness makes no improvement. Nonetheless, this set of data has ruled out the possibility of QD quality improvement via a thicker spacer QDSC from our last hypothesis; thence, we no longer expect R5 to achieve the highest J_{sc} but should, at least, achieve the same improvements as R6 and R7.

EQE measurements, shown in figure 5, allow us to identify which range of spectrum the current density originates from and the amount of contribution they have on the current output. QD absorption is illustrated in the inset of figure 5 (900 nm–1100 nm). The sharp drops seen at a 870 nm wavelength are related to the GaAs bandgap. GaAs SCs show strong inter-bandgap (400 nm–870 nm) absorption but minimal absorption beyond the sub-bandgap region (900 nm–1100 nm) whereas QDSCs show reasonable absorption across the inter- and the sub-bandgap region. Within the inter-bandgap region, thicker QDSCs show greater current contribution than Si-doped QDSC, which is consistent with the J - V measurements (figure 3) in terms of J_{sc} , where the thick emitter QDSC has exactly

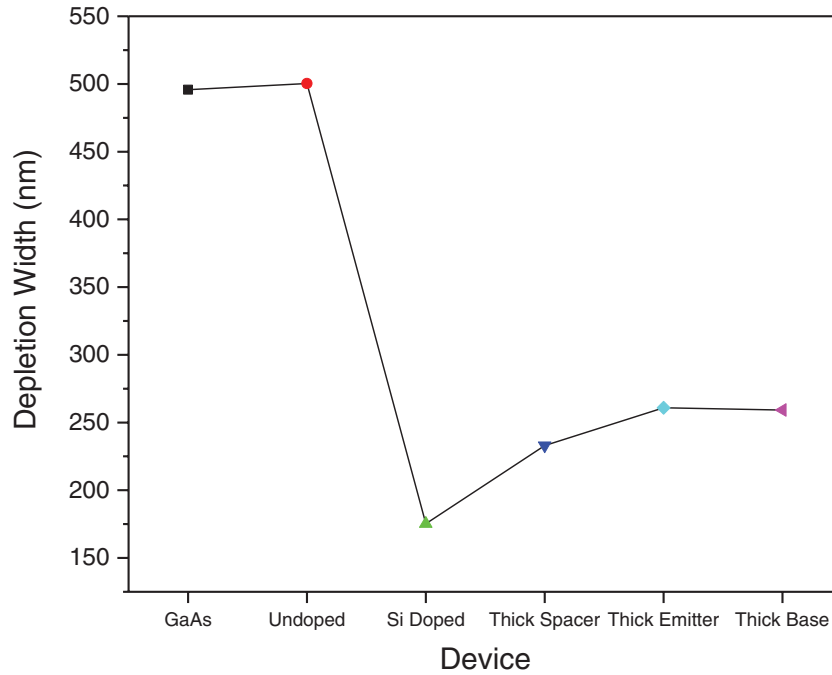


Figure 6. Depletion width of the SC devices.

the same EQE trend as the thick base QDSC; while the thick spacer QDSC has an intermediate level of EQE between them and the Si-doped QDSC. Furthermore, from the inset of figure 5, it is evident that all Si doped QDSCs (R4–R7) have the same QD absorptions, which also agrees with our previous findings (figure 4) that additional intrinsic layers do not alter the QD quality therefore should not increase the QD absorption. Although this EQE data matches the former results very well, it has yet to explain the reason why R5 has less J_{sc} than R6 or R7. In fact, all we can derive from the EQE data, regarding this issue, is that the current density difference is definitely correlated to their inter-bandgap material (GaAs) qualities, rather than their QD qualities.

Therefore, the quality of the GaAs material was further examined, more specifically, the width of the depletion region was analysed. The C – V characteristics of the SCs were obtained to determine the width of depletion region [24]. The capacitance of the device can be expressed as a function of the depletion width:

$$C = \frac{\varepsilon A}{d}, \quad (2)$$

where ε is the permittivity constant of the device, A is the area of the device and d is the separation distance between the parallel plates, in this case, equal to the depletion width (which is equivalent to W in equation (1)).

The capacitances of the SC devices are converted into the depletion widths in table 2 and illustrated in figure 6. The GaAs SC and undoped QDSC have a depletion width near 500 nm. For the Si-doped QDSC, the inclusion of Si dopants has significantly reduced the depletion width (by 320 nm); this was anticipated (to a certain extent) from equation (1) that increasing the donor concentration (N_D) would shrink the width of the depletion region (W), however, the amount of reduction (65%) was beyond our anticipation. It is possible to

calculate, using the same equation (1), the width of the depletion region knowing that the Si doping level is at 14 electrons per dot but that would be beside our primary focus. What we are most interested in is the behaviour of the depletion width after the insertion of the 100 nm intrinsic layer. Indeed, the results have shown reasonable improvements: R5, R6 and R7 have lengthened their depletion width by 58, 85 and 85 nm, respectively. Although the width extensions were not as long as 100 nm, this outcome supports our previous assumption on the insertion of intrinsic layers above or below the QD layers having the same influence on the width.

The thick spacer QDSC (R5) has only increased the width by 58 nm, which does explain the reduced current density for this particular device, but the reason for the shorter increase remains undiscovered and may require more fundamental characterisations. Our best deduction here is that during carrier transportation, carrier movements through the alternating layers of QDs and the thicker spacer layers (100 nm divided into 20 layers) are less mobile, as if they were traveling through a pure intrinsic layer; hence the EQE data showed less current contribution from the GaAs material. To explain in terms of material quality or growth difficulty, it should be *relatively* more straightforward to grow 100 nm layer at once (hence the higher quality) than growing 20 layers of extra 5 nm material (because of the inconsistency of multiple growth precision) *regardless* of how accurate the MBE is; thus greater GaAs material quality for R6 and R7, resulting in higher carrier mobility.

As well as theoretical analysis, numerical data has also shown a clear trend of improvement. Following post-doping with 14 electrons per dot, the depletion width has reduced by 320 nm (65%) and the current density decreased by 2.68 mA cm^{-2} (19%); after the insertion of additional intrinsic layers, the current density has recovered up to 1.71 mA cm^{-2} , which is 64% of the lost current density. This is a remarkable

accomplishment as the thickness of the additional intrinsic layer was only 100 nm (even less for the actual depletion width gain); if the thickness was 200 nm or 400 nm, which should be enough to match the depletion width of the undoped QDSC (R3). We would certainly expect the J_{sc} to achieve at least the same amount as R3. Hence, the numerical data encourage us to deploy thicker intrinsic layers for future SC designs.

While this work has provided evidence that increasing the thickness of the intrinsic layer can improve the current density, we should also be aware of the fact that there is an upper limit for the thickness of thin film solar cells, as over-extending the intrinsic layer may reduce the strength of the internal electric field and increase the transportation length; otherwise the current density might be reduced instead of increased [25].

4. Conclusion

The purpose of introducing an additional intrinsic layer to Si doped QDSCs was first elucidated. Such device configurations were subsequently grown by MBE and further investigated in conjunction with the regular Si doped QDSCs. Assumptions drawn from J - V , PL and EQE measurements were supported by a fundamental characterization. C - V characterizations, have provided clear evidence of the shortening and lengthening of depletion region width before and after the insertion of intrinsic layers. During analysis, one deduction was made in order to explain an unexpected outcome, which refers to the growth difficulty of material quality in the case of multiple growth precision. Furthermore, the additional 100 nm intrinsic layer has enhanced the depletion width up to 85 nm which recovered 64% of the lost current; this result suggests further increases in thickness may give rise to a stronger improvement in current density.

Acknowledgments

The authors acknowledge the financial support of EPSRC Grant No. EP/K029118/1, Grant No. EP/P000886/1, and EPSRC National Epitaxy Facility. H Liu would like to thank The Royal Society for funding his University Research Fellowship.

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