1.2V Energy-Efficient Wireless CMOS Potentiostat for Amperometric Measurements

Virgilio Valente, *Member, IEEE,* Nazanin Neshatvar, *Member, IEEE,* Evdokia Pilavaki, Matthew Schormans, *Member, IEEE* and Andreas Demosthenous, *Fellow, IEEE*

***Abstract*—Wireless biosensors are playing a pivotal role in health monitoring, disease detection and management. The development of wireless biosensor nodes and networks strongly relies on the design of novel low-power, low-cost and flexible CMOS sensor readouts. This paper presents a CMOS potentiostat that integrates a control amplifier, a dual-slope ADC and a wireless unit on the same chip. It implements a novel time-based readout scheme, whereby the counter of the dual-slope ADC is moved to the receiver and the sensor current is encoded in the timing between two wireless pulses transmitted via pulse-harmonic modulation across an inductive link. Measured results show that the potentiostat chip can resolve a minimum input current of 10pA at a sampling frequency of 125 Hz and a power consumption of 12 μW.**

***Index Terms*—Amperometry, biosensors, dual-slope ADC, potentiostat, pulse harmonic modulation, wireless.**

I. Introduction

WEARABLE and implantable biosensors are poised to play a critical role in clinical diagnostics, disease prevention, monitoring and management. Electrochemical biosensors, in particular, are widely used as label-free, real-time, quantitative, sensitive and CMOS-compatible devices. CMOS instrumentation for electrochemical biosensors has received wide attention in the last decade as it supports the development of complex miniaturized sensing platforms that can readily interface with disposable sensors and be operated remotely [1]. Since their introduction in 1987 [2], CMOS potentiostats have been developed for numerous applications, including biosensors [3], neurotransmitter sensing [4], glucose monitoring [5] and protein and DNA sensor arrays [6].

The choice of the readout electronics is conventionally based on three topologies, including current-to-voltage (I/V) conversion, or a current conveyor (CC) followed by an ADC [7], [8], a current-to-frequency (I/F) conversion [5], [9] or a current-input ADC [10]. A signal conditioning stage before the digitisation helps to increase the readout SNR at the cost of limited input current range due to the amplifier swing [8]. To circumvent this issue, input modulation has been adopted after the current-conveyor, to extend the input current-dynamic range [7]. The use of a CC, however, results in a power consumption penalty. Direct I/F conversion using relaxation oscillators has been recently demonstrated as a power saving alternative solution achieving good linearity and extended dynamic range [11]. This configuration, however, cannot be easily adapted to different applications since the design of the oscillator is usually tailored to specific input current ranges. Additionally, a limited number of CMOS potentiostat implementations fully integrate the control, conversion and wireless units on the same chip and often result in large current consumption [9].

This paper presents a novel energy-efficient wireless potentiostat architecture based on a dual-slope (DS) ADC combined with an innovative wireless unit [12]. The conventional counter used in DS ADC architectures has been moved to the receiver end, while a pulse modulation scheme has been adopted to encode ADC conversion time into two wireless pulses that can be easily detected by the receiver. In addition, the ADC is input-modulated in order to extend its dynamic range between pA to μA.

This paper expands on a previous publication [13], by presenting details on the design and implementation of the wireless potentiostat with experimental measurements. Section II presents the novel architecture of the wireless potentiostat. Section IV discusses the circuit-level implementation of the potentiostat. Section V presents the measured results of the functional performance of the chip and electrochemical measurements performed with it. Section VI draws conclusions and comparison with state-of-the-art implementations.

II. Potentiostat Principle of Operation

Fig. 1(a) shows the architecture of a conventional current-mode wireless potentiostat readout. A DS ADC operates in two phases. During the first phase the input current, I_{IN}, is integrated onto the integrator capacitor, while during the second phase the capacitor is discharged by a reference current, I_{REF}. This operation effectively converts the input current to a pulse, whose duration is proportional to the ratio between I_{IN} and I_{REF}. A local counter is used to measure the duration of the pulse. The

Manuscript received –, 2019; revised –, –.

This work was supported by the Engineering and Physical Sciences Research Council under Grant EP/K031953/1.

N. Neshatvar, Evdokia Pilavaki, M. Schormans and A. Demosthenous are with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, UK. (e-mail: a.demosthenous@ucl.ac.uk)

V. Valente was with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, UK. He is now with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands. (e-mail: v.valente@tudelft.nl)

output of the counter is modulated by a local oscillator (LO) and sent over the wireless link. The presence of an LO and a counter decreases the energy efficiency of the front-end unit and the transmitter.

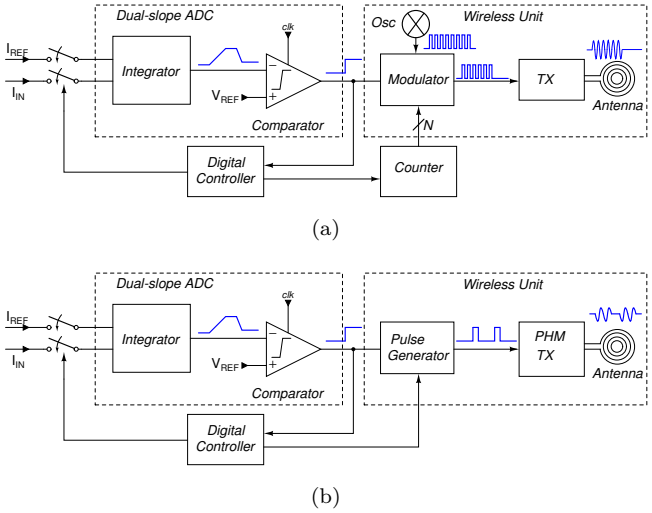

Fig. 1. Wireless potentiostat architecture. (a) Conventional and (b) proposed system.

Here we propose a new strategy based on a modified pulse harmonic-modulation scheme [12], whereby only two pulses are sent via the wireless link, one at the start and one at the end of the capacitor discharge period, as shown in Fig. 1(b). These pulses inherently encode the capacitor discharge time, which can be determined at the receiver end. This approach greatly reduces the complexity and power requirements of the readout circuit.

III. System Architecture

The block diagram of the potentiostat chip is shown in Fig. 2. The chip consists of a 4-channel potentiostat and a wireless unit.

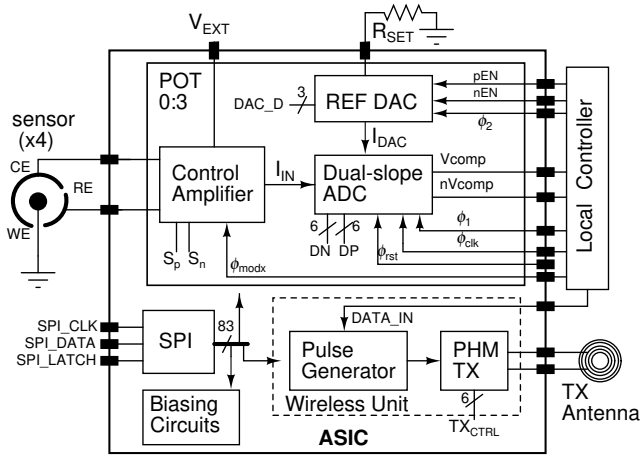

Fig. 2. Chip block diagram.

Each potentiostat comprises a control amplifier, a dual-slope ADC and a reference DAC. The potentiostat can be programmed via an on-chip 7-register 20-bit SPI interface. Two SPI registers are used to enable and address individual potentiostat channel. One register stores the settings of the wireless unit and 4 registers are used to individually calibrate the offset of individual channels. The local controller is used to set the polarity of the channel, the operation mode and the timing pulses. The timing sequence is implemented on an FPGA unit, whereas the selection switches are implemented directly on the PCB.

IV. Circuit Implementation

The schematic of each potentiostat readout channel is shown in Fig. 3. A dual-mode current-mirror-based control amplifier is used to set the electrochemical cell potential V_{RE-WE} to a fixed value. The control amplifier can set a positive V_{RE-WE} or negative V_{RE-WE}, depending on whether a reduction or oxidation current is measured during the chemical reaction. In the former case the working electrode (WE) is connected to ground, whereas in the latter case WE is connected to the supply potential V_{DD}.

The core of the DS ADC consists of a switched-capacitor integrator featuring correlated-double sampling and a dynamic comparator. The wireless unit consists of a pulse generator (PG), a pulse harmonic modulation (PHM) transmitter (TX) and a coil antenna for inductive data transfer. Details on the design and simulated performance of individual blocks of the potentiostat can be found in [13]. Extensive detail on the design and measured performance of the wireless unit are available in [12].

The operation of the potentiostat channel can be described with the aid of the timing diagram in Fig. 4 in conversion and calibration modalities.

1) Conversion mode: After a global reset phase, ϕ_{rst}, the output of the integrator, V_{int} is held at V_{REF}. During the integration phase, ϕ_1, the input current, I_{IN}, is integrated on the capacitor C_i for a fixed time, t_1 by closing switch S_1. During t_1, V_{int} increases or decreases from V_{REF}, depending on the direction of I_{IN}. During the discharge phase, ϕ_2, the reference DAC is enabled forcing V_{int} to decrease (or increase) toward V_{REF}. As the threshold is crossed the output of the comparator, V_{comp}, toggles and the conversion is completed. The amplitude of the input current can be determined as: $I_{IN} = \alpha \cdot k \cdot (t_2/t_1) \cdot I_p$, where k is the input current modulation index equal to t_1/T_{mod} and α is a gain factor due circuit non-idealities and I_p is the programmable current from the reference DAC.

The PG generates two short pulses (ns), one triggered by the rising edge of ϕ_2 and one at the rising edge of the comparator output (see ϕ_{PG} in Fig. 4(a)). The integrator discharge time, t_2, is then encoded in the delay between the PG pulses. These two pulses are modulated by two PHM pulses generated by the TX at a frequency of approximately 200 MHz.

2) Calibration mode: : The comparator complementary outputs are connected to the inputs of the DAC via the local controller. In this modality the ADC is run as a 1^{st}-order $\Sigma\Delta$ modulator. The integrator capacitor is charged and discharged by the complementary REF DAC

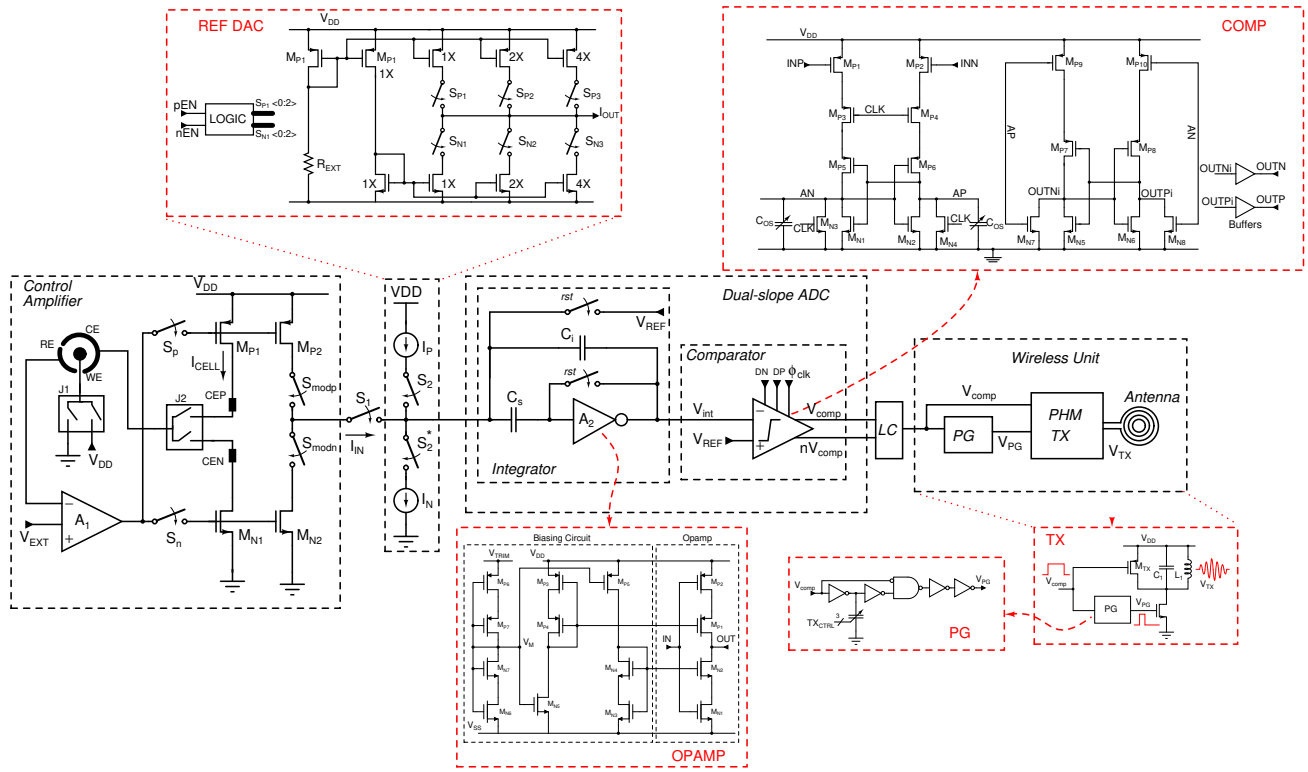

Fig. 3. Detailed schematic of a potentiostat channel. The polarity of the potentiostat is selected manually via J1, J2 and static switches S_n and S_p.

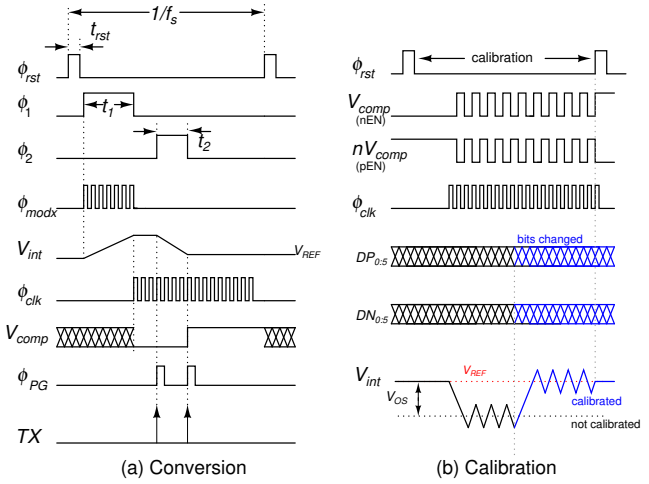

Fig. 4. Detailed timing diagram of the operation of the potentiostat channel in (a) conversion and (b) calibration mode.

currents. The average value of V_{int} equals $V_{REF} \pm V_{OS}$. The offset can be reduced by digitally trimming the load capacitance at the outputs of the comparator by changing the calibration bits DP and DN (Fig. 4b).

V. Experimental Results

The chip was designed in a 0.35 μm CMOS process. The chip microphotograph is shown in Fig. 5. The chip was wire-bonded to an LQFP64 package and soldered to an adaptor board. This was connected into a mother board providing the required supply and bias signals and was directly connected to an FPGA board (Xilinx Artix 7).

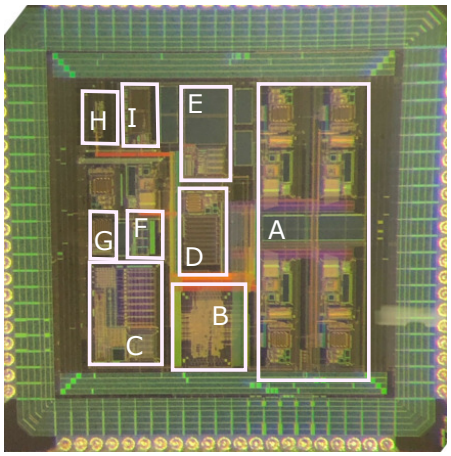

Fig. 5. Chip Layout. **A**. 4-channel dual-slope ADC with control amplifier; **B**. 8-register SPI; **C**. Bandgap; **D**. 1.2V voltage regulator; **E** Bias cell; **F**. Power-on reset; **G**. Beta multiplier; **H**. TX; Unlabeled blocks represent test structures.

The ADC current range was measured at a sampling rates between 5 kHz and 20 kHz with a clock frequency of 10 MHz. The values of t_2 were measured from 3 consecutive conversion cycles. Figure 6 shows the linearity of t_2 for an input current range between (a) 10 nA and 100 nA and (b) 100 nA and 1 μA. The worst error was

1.58% between 10 nA and 100 nA and 5.4% between 100 nA and 1 .

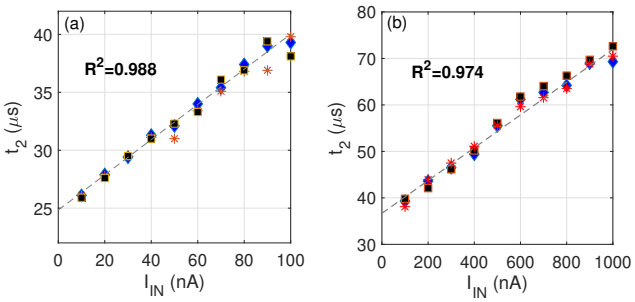

Fig. 6. Linearity of the ADC for a input current range between (a) 10nA and 100nA and (b) 100nA to 1μA.

Fig. 7(a) shows the measured RMS input noise current, $I_{n,in}$ of the ADC for different sampling frequencies. At a sampling frequency of 125Hz, $I_{n,in}$ equals 10 pA_{RMS}. For an integrator output scale of 0.55V, the SNR of the ADC is approximately 39 dB, resulting in an ENOB of 6.2bits.

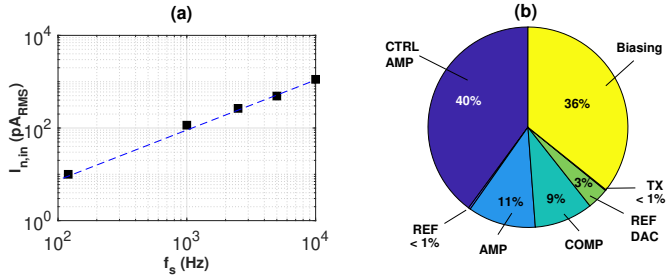

Fig. 7. (a) RMS input current noise for different sampling frequencies and (b) potentiostat channel power breakdown estimated at a sampling frequency of 1 kHz and equal to 12 μW from a 1.2V supply.

Fig. 7(b) show the potentiostat channel power breakdown. The total estimated power at a sampling frequency of 1 kHz was 12 μW. Most of the power is consumed by the control amplifier and the biasing circuits. The ADC consumes less than 2.5 μW resulting in 34 pJ/conversion. The TX unit consumes 16 nW.

1) Offset calibration: Figure 8 shows the transient operation of the calibration scheme. The complementary outputs of the dynamic comparator are connected to the reference DAC. The DAC complementary currents were set to equal values of 80 nA. The ADC operates as a 1st-order $\Sigma\Delta$ modulator. The traces in the figure show the integrator output voltage without calibration and after calibration. The comparator offset due to transistor mismatches causes the comparator threshold voltage to be V_{OS} below V_{REF}. By varying the value of the 6-bit capacitor array, the offset was reduced by 100 mV.

2) Wireless transmission: The output of the comparator was connected to the TX unit at pinout. The input current was set to 100 nA, k to 10 and the sampling frequency to 10 kHz. Fig. 9 shows the operation of the wireless transmission. One pulse is generated at the start of the integrator discharge phase (ϕ_2 in Fig. 4(a)).

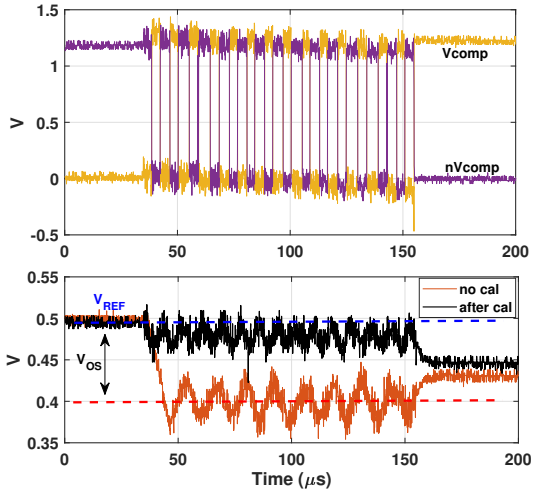

Fig. 8. Calibration of ADC offset.

The integrator voltage increases towards the comparator threshold voltage, V_{REF}, which then toggles its state, driving the generation of another short pulse. The timing between the two pulses encodes t_2 (and hence I_{IN}). The PHM pulses were transmitted across an inductive link. The TX power was 1.6 mW with the receiver coil at a distance of 10 mm . As the properties of the link do not vary during a conversion cycle, the time t_2 can be faithfully recovered at the receiver end.

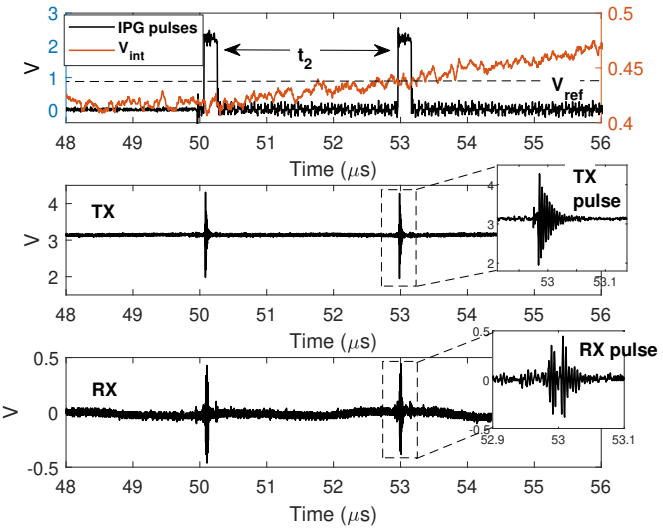

Fig. 9. Operation of the wireless unit.

3) Electrochemical experiments: The potentiostat was interfaced to a 3-terminal screen printed carbon electrode (Metrohm DropSens) and used to measure different concentrations of ferrocyanide, $[FE(CN)_6]^{4-}$ diluted in 20 mL of PBS (1X). The concentration was varied between 1 mM and 100 mM and t_2 was measured from 3 consecutive conversion cycles with results shown in Fig. 10.

TABLE I
PERFORMANCE COMPARISON. DS:DUAL-SLOPE; PHM: PULSE HARMONIC MODULATION; CC: CURRENT CONVEYOR; ASK: AMPLITUDE SHIFT KEYING; FSK: FREQUENCY SHIFT KEYING; UWB: ULTRA WIDE BAND

Parameter	This work	[4]	[14]	[8]	[15]	[7]	[16]	[10]	[11]
Technology/Supply	0.35 μm	0.18 μm	0.35 μm	65nm	0.18 μm	0.5 μm	0.13 μm	0.25 μm	0.18 μm
Supply	1.2 V	1.8 V	1 V	1.2 V	1.8 V	5 V	1.2 V	2.5 V	1.8 V
Readout	DS ADC	DT/buf TIA	n/a	I/V & SAR ADC	I-to-pulse	CC & $\Sigma\Delta$ ADC	CC	DS ADC	I/F
Max Input Current	1 μA	50 nA	2.6 μA	430 nA	1 μA	16 μA	350 nA	110 nA	800 nA
Sensitivity	10 pA*	n/a	70 nA	92 pA	n/a	100 fA	8.6 pA	240 pA	3.3 pA
CTRL Amp	yes	n/a	yes	yes	yes	yes	n/a	yes	yes
Wireless	PHM	n/a	n/a	UWB	n/a	n/a	n/a	n/a	n/a
μW/channel	12	12	22	30	CA: 60	241	4	n/a	4.4

*Measured at a sampling frequency of 125 Hz

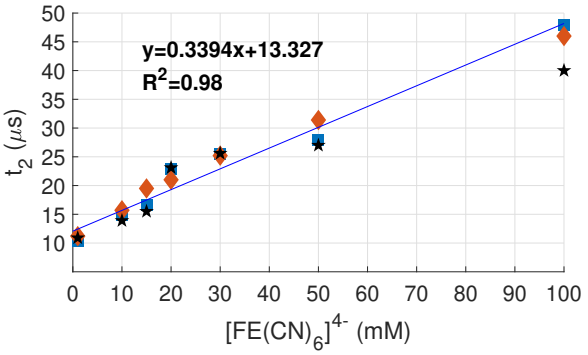

Fig. 10. Measurements of different t_2 for different concentrations of $[FE(CN)_6]^{4-}$ diluted in PBS 1X solution.

VI. CONCLUSION

The work presented in this paper defines a novel strategy to reduce the circuit complexity and power consumption of a biosensor readout system. The key innovation lies in a time-domain conversion and wireless transmission of the input current. This approach allows to remove the counter from the sensor node and use an energy-efficient PHM scheme to encode the value of the input current in the time delay between two pulses. Measured results show that the potentiostat compares favourably with state-of-the-art implementations, in terms of dynamic range, power consumption and functionality as reported in the performance comparison in Table I. The potentiostat chip integrates the control amplifier, the ADC stage and the wireless unit. Only a limited number of CMOS potentiostat offer such level of integration but they often consume significant power in the wireless transmission [9] or have limited input current range [14]. The proposed architecture lends itself to the development of future low-power multichannel systems based on time-domain multiplexing schemes, where the conversion is initiated at the sensor node and completed at the receiver end.

REFERENCES

[1] H. Li, X. Liu, L. Li, X. Mu, R. Genov, and A. Mason, "CMOS Electrochemical Instrumentation for Biosensor Microsystems: A Review," *Sensors*, vol. 17, no. 12, p. 74, Dec 2016.

[2] H. P. Baltes and R. Turner, "A CMOS potentiostat for amperometric chemical sensors," *IEEE Journal of Solid State Circuits*, vol. SC-22, no. 3, June, 1987.

[3] S. S. Ghoreishizadeh, I. Taurino, G. De Micheli, S. Carrara, and P. Georgiou, "A differential electrochemical readout ASIC with heterogeneous integration of bio-nano sensors for amperometric sensing," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 5, pp. 1148–1159, 2017.

[4] J. Guo, W. Ng, J. Yuan, S. Li, and M. Chan, "A 200-channel area-power-efficient chemical and electrical dual-mode acquisition IC for the study of neurodegenerative diseases," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 3, pp. 567–578, 2016.

[5] M. M. Ahmadi and G. a. Jullien, "A wireless-implantable microsystem for continuous blood glucose monitoring." *IEEE Transactions on Biomedical Circuits and Systems*, vol. 3, no. 3, pp. 169–80, Jun 2009.

[6] C. Yang, Y. Huang, B. L. Hassler, R. M. Worden, and A. J. Mason, "Amperometric electrochemical microsystem for a miniaturized protein biosensor array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 3, no. 3, pp. 160–168, 2009.

[7] H. Li, C. S. Boling, and A. J. Mason, "CMOS amperometric ADC with high sensitivity, dynamic range and power efficiency for air quality monitoring," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 4, pp. 817–827, Aug 2016.

[8] C. I. Dorta-Quinones, X. Y. Wang, R. K. Dokania, A. Gailey, M. Lindau, and A. B. Apsel, "A wireless FSCV monitoring IC with analog background subtraction and UWB telemetry," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 2, pp. 289–299, Apr 2016.

[9] M. R. Haider, S. K. Islam, S. Mostafa, and S. Member, "Low-power low-voltage current readout circuit for inductively powered implant system," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 4, pp. 205–213, 2010.

[10] P. M. Levine, S. Member, P. Gong, R. Levicky, and K. L. Shepard, "Active CMOS Sensor Array for Electrochemical Biomolecular Detection," *IEEE Journal of Solid State Circuits*, vol. 43, no. 8, pp. 1859–1871, 2008.

[11] J. H. Tsai, C. Y. Kuo, S. H. Lin, F. T. Lin, and Y. T. Liao, "A wirelessly powered CMOS electrochemical sensing interface with power-aware RF-DC power management," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 9, pp. 2810–2820, 2018.

[12] M. Schormans, D. Jiang, V. Valente, and A. Demosthenous, "Short-range quality-factor modulation (SQuirM) for low power high speed inductive data transfer," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 9, pp. 3254–3265, Sep. 2019.

[13] V. Valente, M. Schormans, and A. Demosthenous, "An energy-efficient 1.2V 4-channel wireless CMOS potentiostat for amperometric biosensors," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, May 2018.*

[14] L. Zuo, S. K. Islam, I. Mahbub, and F. Quaiyum, "A low-power 1-V potentiostat for glucose sensors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 2, pp. 204–208, 2015.

[15] S. S. Ghoreishizadeh, C. Baj-Rossi, A. Cavallini, S. Carrara, and G. De Micheli, "An integrated control and readout circuit for implantable multi-target electrochemical biosensing," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 6, pp. 891–898, Dec 2014.

[16] H. M. Jafari and R. Genov, "Chopper-stabilized bidirectional current acquisition circuits for electrochemical amperometric biosensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1149–1157, May 2013.