# Integrated Devices for Micro-Package Integrity Monitoring in mm-Scale Neural Implants

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***Abstract*—Recent developments in the design of active implantable devices have achieved significant advances, for example, an increased number of recording channels, but too often practical clinical applications are restricted by device longevity. It is important however to complement efforts for increased functionality with translational work to develop implant technologies that are safe and reliable to be hosted inside the human body over long periods of time. This paper first examines techniques currently used to evaluate micro-package hermeticity and key challenges, highlighting the need for new, *in situ* instrumentation that can monitor the encapsulation status over time. Two novel circuits are then proposed to tackle the specific issue of moisture penetration inside a sub-mm, silicon-based package. They both share the use of metal tracks on the different layers of the CMOS stack to measure changes in impedance caused by moisture present in leak cracks or diffused into the oxide layers.**

## I. Introduction

Continual breakthroughs in science and engineering, together with the persistent advancements in manufacturing technology, have made it possible to implant electronic devices inside the human body with minimal disruption. The aim of such devices has to date predominantly been to stimulate tissue to achieve a desired modulation. Next generation devices are now bringing sensing capability by recording and extracting information from the body's internal bio-signals [1]. In the last decades there have been successful therapeutic applications of these devices, for example pacemakers, cochlear implants, and closed loop deep brain stimulators for Parkinson's disease patients. Alongside such devices that have been established clinically, there is a wide range innovative implant devices being developed thanks to the efforts of universities, research centres, and industry. Non-medical companies have also been showing a growing interest in this field, as implantable devices show the potential to spread out of the medical context and expand towards more generic consumer applications.

Ideally an implantable device should have no undesired interaction with the surrounding tissue. This translates into a series of constraints that must be considered during the design phase. In particular, it is highly desirable to keep the overall dimensions of the implant as small as possible, to minimise the effects of foreign-body reaction (FBR) and to allow for a higher degree of bio-compatibility. Although scaling down sizes is compatible with current trends in microelectronic fabrication, it poses several challenges from the mechanical point of view [2], [3]. Manufacturing methods can be leveraged from economies of scale such as MEMS microfabrication, however these are not all directly compatible for implantable devices, since they often cannot satisfy the strict requirements needed for medical applications [3], [4]. In order to reliably function within the environment of the human body, implantable devices need to withstand the constant presence of moisture and to avoid contamination to and from the surrounding tissue, as well as to tolerate the mechanical stresses caused by body movements. Furthermore, the induced temperature increase due to the device's power dissipation must remain within standard safety limits. Even in the event of a functional failure, implants should not pose a health risk for the patients, and they must remain safe at least for the time needed to guarantee an explantation intervention. Moreover, since the implantation procedure presents the same risks as traditional surgery, and given the constant overall aging of the world's population, these devices should be designed to last for years, possibly decades, inside the body.

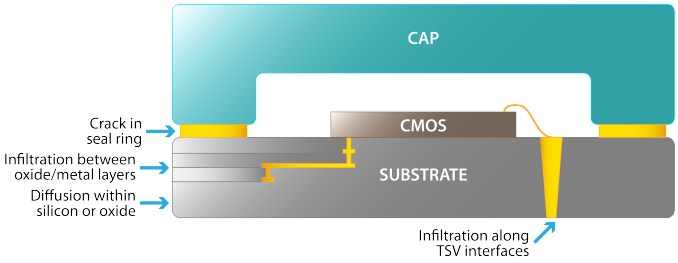


Fig. 1. Possible routes to failure due to moisture penetration in a silicon based micro-package with active CMOS circuits (dimensions not to scale).

Scaling down dimensions is even more crucial in this specific case of neural implants, because of the delicate environment of the brain, and the limited space if compared to, for example, the chest cavity. Furthermore, given the complexity and the higher risk associated with brain surgery, the requirements on implant reliability and expected lifetime extend further [5].

The objective of this paper is to first present the challenges associated with the down-scaling of implantable devices, particularly with regards to the issue of moisture penetration, and then to propose the use of on-board circuits for the detection of moisture ingress in an active silicon substrate. The remainder of the paper is organised as follows: Section II introduces the issue of hermeticity in mm-scale active implantable devices, and gives an overview of the current test methods used to assess encapsulation of micro-packages; Section III presents

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two novel design concepts for integrated instrumentation for the detection of moisture through the substrate; finally Section IV concludes this work.

## II. Hermeticity of mm-Scale Micro-Packages

For implantable devices the ability to be hermetically sealed is an essential feature to guarantee reliable and long-term operation. In fact, the presence of water inside the micro-package would lead to the corrosion of electronic components and therefore to the eventual failure of the device [6]. The choice of materials used to encapsulate the device plays a central role in the hermeticity of the package, however this choice is also constrained by the desired functionality. For example, semiconductor substrates are needed when it is necessary to integrate electronic circuits, or complete metal casing cannot be used where wireless powering is employed.

An example of sealed micro-package is reported in Fig. 1. The active CMOS circuit is protected by a cap (glass, ceramic, sapphire, or any other material with extremely low moisture permeability), which in turn is connected with a silicon substrate by mean of a metallic seal ring, e.g. [7], [8]. The substrate can either act as a passive re-distribution layer, hosting the electrical connections between the CMOS circuits and the outside environment, or can be an active component and directly host the circuitry within itself. In this example, the main causes of failure in the encapsulation are the following: (1) the presence of cracks in the seal ring, caused by imperfect adhesion during seal creation or by mechanical stress; (2) moisture ingress at the interface between the alternating oxide and metal layers of a CMOS process; (3) moisture diffusion in the substrate material; (4) moisture penetration at the boundary between substrate and metal where feed-through connections are present (in the example a through-silicon via is used, but it might apply to different sort of connections). It is usual for this type of implantable micro-packages to have an additional polymer encapsulation (silicone, PDMS, Parylene-C). This extra layer can prolong the lifetime of the device, but does not guarantee hermeticity on its own due to the permeability of polymers [9]. It can however be beneficial in protecting the outside tissue from the products of internal corrosion [6].

Numerical modelling of both the mechanisms of water penetration in small scale micro-packages and of moisture effect on dies is actively under research [10], however there is still the need for a reliable way to assess hermeticity in sub-millimetre implantable devices.

### A. Test Methods for Monitoring Encapsulation

Different methods have been developed over time to evaluate the hermeticity of micro-packages [11]. The military standard MIL-STD-883, Method 1014.10 describes various procedures to measure fine leaks [12]. The most common method employs a mass spectrometer to detect a tracer gas leaking from the package, and in the majority of cases helium is used because of its scarce presence in normal atmosphere. However, the lower limit indicated in the standard is suitable for volumes two order of magnitude higher than standard MEMS package sizes [13]. A variation of the fine leak test uses radioactive tracer gas to enhance the sensitivity of the detector, however it is not safe for implantable devices.

Another approach is given by the optical spectrometry methods: Fourier Transmission Infrared Spectrometry (FTIR) and Raman spectroscopy. The first relies on the optical absorption properties of a tracer gas; on the other hand the second uses the interaction between monochromatic light and phonons of the device under test to determine the type and the quantity of the gas inside the micro-package. The sensitivity of such tests can measure leakage in cavities down to 5 $mm^3$, however they require the package to be transparent for the specific wavelengths used by each technique [11].

A further category of tests comprises deformation tests. When the device to be evaluated is placed in a chamber with a pressure significantly different from the one inside the cavity, a deflection of the cap will occur. This deformation can be measured by mean of an optical interferometer. The results of this test are very dependent on the size of the device, and on the thickness and stiffness of its materials, however, as an advantage, they can be performed at wafer level [14].

Apart from the limitations in detection of leaks in sub-$mm^3$ cavity sizes, all the methods presented thus far require external instrumentation to evaluate the presence of a leak and therefore they are not suitable for the long-term monitoring of the status of the encapsulation. Hence the need to employ *in situ* test structures built inside the micro-package. An example is the use of structures such as resonators or cantilevers whose Q-factor changes with the pressure inside the cavity. However, these structures require MEMS fabrication capabilities, and thus they cannot be easily integrated in a standard CMOS process. A viable alternative is the use of built-in sensors to monitor quantities such as pressure or humidity, and infer the hermeticity status of the device under test from their readings.

As indicated in [13], *in situ* methods have proven to have the highest sensitivity for the detection of leaks, and they also allow for the detection of outgassing products from within the device. Thanks to the possibility of integration within a CMOS die without the need for further post-processing, the use of integrated humidity sensor has been explored. However, at the moment, in order to achieve the desired sensitivity, the sensors' dimensions are still too large to be conveniently used in sub-mm micro-packages [15].

## III. Design Concepts for Integrated Instrumentation

Among all the test methods presented in the previous section, *in situ* tests have proven to be not only the most accurate tests for small size cavities, but also the only option to monitor hermeticity over time. These can additionally provide the feature of detecting a failure in real time. However, all current methods only tackle the presence of free molecules of water vapour in the cavity, and do not account for the infiltration of moisture from the side of the silicon substrate. This types of infiltration may not cause any build up of moisture inside the cavity, but they can lead to the corrosion of the metal tracks and they might compromise the operation of the device.

To answer this specific need, we propose two circuits to directly measure and detect changes in the dielectric stack. Both solutions take advantage from the presence of the die seal ring, that is usually present in CMOS circuits to protect the active devices placed inside it. The die seal ring is formed by

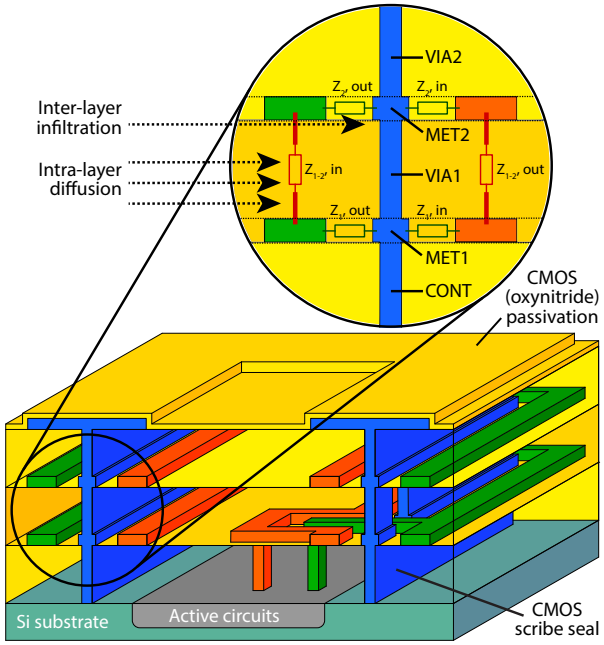


Fig. 2. Cross-section of a CMOS die showing the proposed structure to measure moisture ingress. The red and green metal tracks run around the perimeter, parallel to the die seal ring (dimensions not to scale).

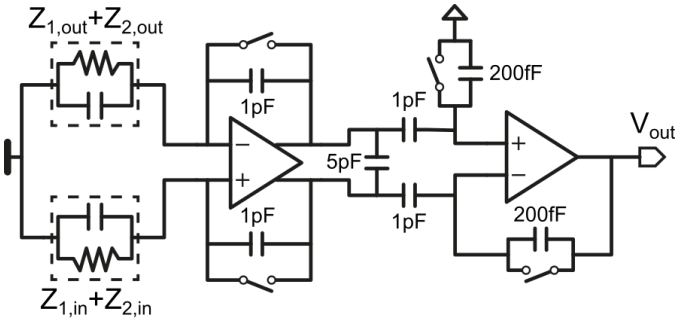


Fig. 3. Schematic of the proposed TIA configuration for the measurement of impedance between metal tracks and die seal ring.

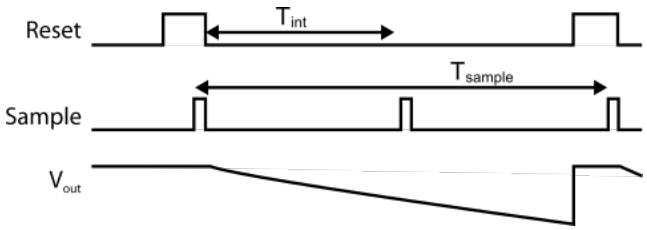


Fig. 4. Timing diagram of the TIA-based circuit in Fig. 3.

continuous parallel metal tracks on all available metal layers, all shorted together through vias, and it also connects to the silicon substrate. It usually runs about 100 µm from the scribe line, i.e. edge where the dicing saw separates the individual dies from the wafer.

Both circuits deal with the issue of moisture infiltration from the side of the silicon die by performing an impedance measurement, however each circuit has been designed to assess specific features. The concept is illustrated in Fig. 2. Along all the metal layers available in the CMOS process, a set of parallel metal tracks (drawn in orange in the figure) run around the die inside the the seal ring (drawn in blue), at a set distance from it. Similarly, another set of metal tracks (pictured in green) run at the same distance on the outside of the die seal ring. This allows for a differential measurement between the external tracks, which are the first ones affected by any ingress of moisture, and the internal ones, that are protected by the presence of the die seal ring. Both sets of metal tracks have contacts with the active part of the substrate. For the outer set, minimal apertures are made in the die seal ring to allow for the connection.

The two proposed circuits can be implemented on the same die, by having the possibility to either connect or not the metal tracks together using programmable switches, so that the instrumentation can alternate between one configuration or the other whenever needed. This gives also the possibility to either use all of the metal traces as sensing terminals to enhance sensitivity, or to select a specific layer, for example Metal2, to localise at which depth the failure has occurred.

### A. *Inter-layer infiltration*

In this scenario we expect moisture penetration at the interface between the different silicon dioxide inter-layer dielectrics (ILDs). This may be caused by defects during the fabrication phase, or by cracks induced by mechanical or thermal stress. Moisture continues to infiltrate deeper along the interface of ILDs, and eventually shorts the outer metal tracks with the die seal ring. In this case an impedance measurement along the horizontal direction is necessary to determine if the infiltration has reached the die seal ring. This corresponds to comparing the parasitic impedances $Z_{1,out}$, $Z_{2,out}$ and $Z_{1,in}$, $Z_{2,in}$ in Fig. 2.

Fig. 3 shows the proposed circuit to achieve this comparison. The first stage is capacitance based, connecting to a discrete time differential trans-impedance amplifier (TIA), whose two inputs are connected respectively to the inner and outer metal tracks. The output of the first stage is then fed into the second stage which is based on a switched-capacitor inverting amplifier. The second stage also implements correlated double sampling (CDS) in order to subtract the effect of the offset of the operational amplifiers from the signal [16]. Compared to conventional current sensing circuits [17], the signal bandwidth in the proposed system is near DC with magnitude in the range of 1 to 100 pA. A smaller amplification bandwidth is preferred to reduce the noise bandwidth and aliasing. This requires a lower sampling frequency, which is lower than the corner frequency of the flicker noise. This also allows a low duty cycle for power saving. Considering the noise aliasing [17], the noise density in the low frequency band can also include the flicker noise in the sampling harmonics. Therefore a larger PMOS pair (600 µm/1 µm) is used in the first stage folded cascode amplifier, with 1 pF capacitors used as feedback capacitors to minimise the effect of input parasitic capacitance for noise reduction. The simulated transfer function and noise spectrum is shown in Fig. 5, with total power consumption of 4.76 µA at 3 V power supply.

### B. *Intra-layer diffusion*

In this case we assume the moisture diffuses in the oxide layers. If sustained for a sufficient amount of time, this phenomenon can also lead to the dissolution of the silicon dioxide [18]. The diffusion of moisture does not guarantee the

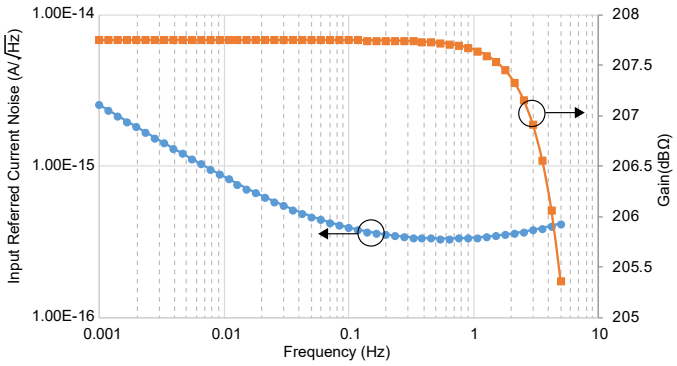


Fig. 5. Simulation results for the TIA frequency response and noise profile.

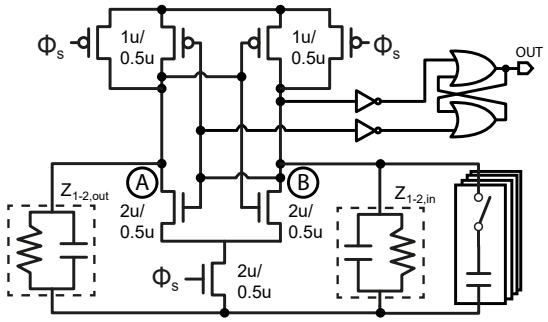


Fig. 6. Schematic of the circuit for sensing moisture diffusion by measuring impedance between metal tracks on different layers.

creation of a short circuit between metal traces, but it causes a change in the permittivity of the silicon dioxide, that can be sensed with an impedance measurement, this time along the vertical direction. With reference to Fig. 2, the objective is to compare the magnitude of the impedances $Z_{1\text{-}2,out}$ and $Z_{1\text{-}2,in}$, since we expect the diffusion to affect at first only the capacitance between the outer metal tracks.

The goal of the sensing circuit is not to characterise these impedances, but instead to warn if the difference between the inner and the outer impedance is greater than a given threshold. For this reason the proposed circuit employs a latch-based comparator, with a simple cross-coupled inverter pair. When the measurement is triggered during the phase $\phi_S$, the output will be evaluated by the pull-down strength due to mismatch and the total capacitance seen at the two input nodes A and B. To suppress the comparator noise and compensate the mismatch for both drive strength and parasitics, a 4-bit trimming circuit with unit capacitor of 20 fF is included on the reference side.

## IV. Conclusion

This paper has presented two distinct circuits for the monitoring of moisture penetration inside the silicon substrate of an implantable micro-package. They could act not only as useful on-board diagnostic devices for commercial devices, but also as a novel research tool to better understand the mechanism of water ingress in active silicon-based packages. The circuits employ design methodologies to reduce the power consumption and allow for an integration into low-power implants. It is in fact envisioned to incorporate these circuits into a new generation of wireless, mm-scale, cortical neural implants [19]. In order to validate the proposed architectures, a practical implementation will be proposed and evaluated in accelerated life tests.

## Acknowledgments

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