

A Power-Efficient Current Generator with Common Mode Signal Autozero Feedback for Bioimpedance Measurement Applications

Yu Wu¹, Dai Jiang¹, Peter Langlois¹, Richard Bayford² and Andreas Demosthenous¹

¹Department of Electronic and Electrical Engineering, University College London, Torrington Place, London WC1E 7JE, UK

²Department of Natural Sciences, Middlesex University, The Burroughs, London, NW4 4BT, UK

e-mail: yu.wu.09@ucl.ac.uk; a.demosthenous@ucl.ac.uk

Abstract—This paper describes the design of fully differential sine pulse-width-modulation (SPWM) wave current generator for bioimpedance measurement applications. The current generator has been designed in a 0.18- μm CMOS technology. Its analog front-end operates from ± 1.65 V and has a current consumption of $I_{\text{out}} + 22 \mu\text{A} + (f_{\text{clk}} \times 1.7 \text{ pA})$ where I_{out} is the output current and f_{clk} is the operating frequency. It can provide outputs from $50 \mu\text{A}_{\text{pp}}$ to 1 mA_{pp} of SPWM current up to 98 kHz with a maximum voltage compliance of ± 1.25 V. Using linear current feedback, the current generator has a designed transconductance of 1 mA/V . Feedback also enables cancellation of common mode signals and a high output impedance.

I. INTRODUCTION

Electrical bioimpedance is a low-cost, non-invasive and simple method for characterization of biological tissues. Biological tissue has electrical properties, which relate to both its cell structure and frequency characteristics [1]. Electrical bioimpedance is applied to electrical impedance tomography (EIT) e.g. in lung respiration monitoring [2], and in electrical impedance spectroscopy (EIS) for characterization of tissue e.g. for skin cancer detection [3]. The current generator is an important building block of any electrical bioimpedance system. The conventional method is implemented with a voltage controlled current source with a specified transconductance [4]. This type of current generator although it provides good performance it suffers from high power consumption due to multiple biasing current paths. For very low power designs, square or pseudo-sinewave current generators are used [5], [6]. They are implemented using an H-bridge with digital-to-analog converter (DAC) based current mirrors to source or sink the current to the load directly from the open-drain transistors. They have no feedback loop and mismatch between source and sink currents results in unwanted common mode voltage at the load.

This paper describes the design of an H-bridge based current generator with linear feedback that regulates the output source current to achieve a high output impedance and wide voltage compliance. A common mode controlled feedback current sink minimizes common mode voltage drift and saturation at the output due to source/sink current mismatch. Operated from ± 1.65 V supply, the circuit has a current consumption of $I_{\text{out}} + 22 \mu\text{A} + (f_{\text{clk}} \times 1.7 \text{ pA})$ where I_{out} is the output current and f_{clk} is the operating frequency. The circuit is based on a sine pulse-width-modulation (SPWM) controlled H-bridge. It outputs a PWM based sinewave at

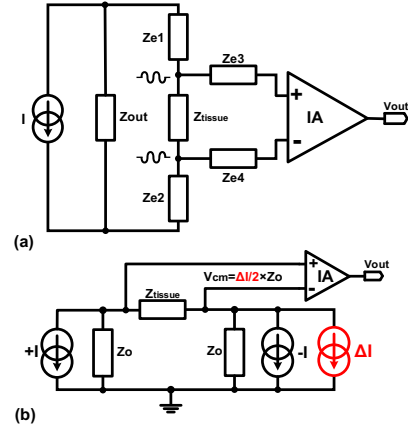


Fig.1. (a) Basic arrangement for tetrapolar bioimpedance measurement; (b) Common mode error due to current generator mismatches.

frequencies up to 98 kHz and provides a maximum I_{out} of 1 mA_{pp} with a transconductance of 1 mA/V .

The paper is organized as follows. Section II presents the system architecture and Section III describes the circuit design. The simulated performance of the current driver is presented in Section IV and conclusions are drawn in Section V.

II. CIRCUIT ARCHITECTURE

One of the main challenges when designing a current generator is to drive the load differentially [7] with the tetrapolar measurement scheme as shown in Fig. 1(a) where Z_e is the electrode impedance. Fig. 1(b) shows the implementation of this type of current generator. Ideally, with such implementation, the signals across the load are fully differential and there is no common-mode across the load. However, because of the unavoidable current mismatch between the two current generators creating a ΔI current which has a return current path to ground through the high output impedance Z_o [see Fig. 1(b)]. This generates a large common mode voltage unless a common mode feedback is implemented. Suppression of the common mode signal relaxes the required common mode rejection ratio (CMRR) needed for the instrumentation amplifier (IA) when measuring the induced voltage due to the tissue impedance (Z_{tissue}).

For a conventional current generator, common mode reduction techniques have been proposed [8], [9]. The H-bridge

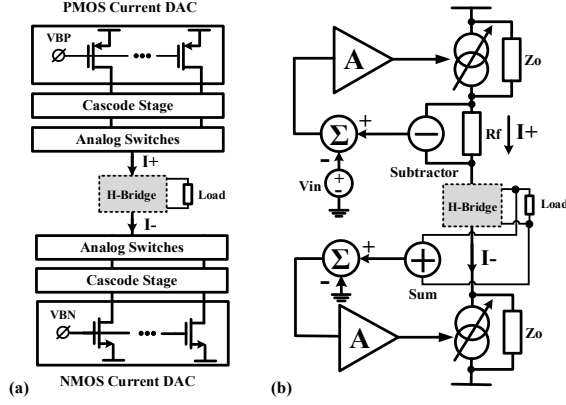


Fig. 2. (a) Conventional H-bridge based current generator with current mirror DAC; (b) Circuit architecture of the proposed current generator.

based current generator is often implemented using two independent carefully matched PMOS and NMOS current mirrors to source and sink the current across the load as shown in Fig. 2(a) with no common mode feedback; this approach suffers from ΔI current mismatch due to process variations [10]. Some electrical bioimpedance systems use micro-electrodes which have high contact impedance (up to a tens of $k\Omega$); whereas the tissue impedance is only few hundred Ohms and decreases to a few $m\Omega$ at high frequency. To provide good system accuracy the current generator requires large currents and large voltage compliance.

The proposed current generator architecture is shown in Fig. 2(b). It is derived from the system used in [9] which cancels common mode effects and offers high output impedance without the use of cascodes. The source of the current generator is controlled by a linear feedback loop. It measures the current through the resistor R_f and regulates the source output I_+ by comparing the measured voltage to an input voltage V_{in} . The sink of the current generator is also controlled by similar feedback, but it measures the common mode voltage across the load compared to a zero-reference level. The bottom current generator adjusts its output to sink a current I_- which is equal to

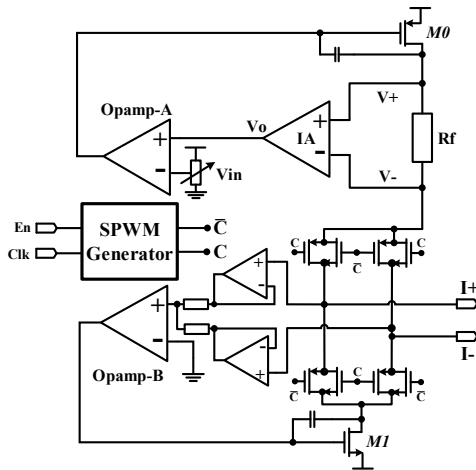


Fig. 3. Circuit implementation of the proposed current generator.

$-I_-$. As a result of having matched currents, the voltage across the load is fully differential with an autozeroed common mode signal. The current into the load is a PWM sinewave through the switched H-bridge.

III. CIRCUIT DESIGN

A. Current Generator

The detailed circuit implementation of the proposed current generator is shown in Fig. 3. The source current is provided by a single PMOS transistor $M0$ in the linear current feedback loop. The subtractor in Fig. 2(b) is a current feedback IA. Opamp-A provides the feedback with a high loop gain to adjust the gate voltage of $M0$ towards a ‘virtual short’ which causes the feedback voltage across R_f to be equal to V_{in} . The transconductance for the source current generator is:

$$Gm_{source} = \frac{A_{ol} \times Gm_{M0}}{1 + A_{ol} \times Gm_{M0} \times A_{IA} \times R_f} \approx \frac{1}{R_f \times A_{IA}} \quad (1)$$

where A_{IA} is the IA gain, A_{ol} is the open loop gain of Opamp-A, and Gm_{M0} is the transconductance of transistor $M0$. As a result of the feedback loop, the output impedance of the source current generator is $A_{ol} \times Gm_{M0} \times R_f \times ro_{M0}$ which is much larger than a simple cascode current mirror [used in Fig. 2(a)] while offering a wider voltage compliance of $V_{CC} - V_{ov,M0} - I_{out} \times R_f$. The sink current is also provided by a single NMOS transistor $M1$ offering a voltage compliance of $V_{SS} - V_{ov,M1}$. The voltages across the load are measured by the buffer and summed into Opamp-B for common mode feedback. When Opamp-B achieves the ‘virtual short’, the common mode voltage is effectively zero, hence the source and sink currents are made equal. The sizing of the output transistors $M0$ and $M1$ are chosen so that the desired maximum output current can be achieved within the maximum output voltage range of Opamps A and B. In addition, the sizing should be optimized to ensure a small V_{ov} to maximize voltage compliance.

B. Current Feedback IA and Opamp

The current feedback IA is based on [11], and its circuit schematic is shown in Fig. 4. An N-type input stage is employed since the IA measures only positive voltages. Transistors $M7$ to $M10$ form a feedback loop that equalizes the drain currents of transistors $Min-1$ and $Min-2$ by adjusting the currents I_1 and I_2 . Hence, the input voltage difference appears across resistor R_1 . These currents are mirrored to I_3 and I_4 to create the same current difference in R_2 . Opamp OP1 forces the drain currents of $M11$ and $M12$ to be the same; since the gate voltage of $M11$ is at ground, drain current equalization can only be achieved when $V_o = (R_2/R_1) \times V_{in}$. The feedback resistor R_f is set to 100Ω ; the transconductance is 1 mA/V providing a maximum 1 mA output. The required maximum positive input linear range of the IA, which is defined as $I_{bias} \times R_1$, is 100 mV and is achieved by setting $I_{bias} = 2 \mu\text{A}$ and $R_1 = 50 \text{ k}\Omega$. The gain of the IA is set to 10 to minimize the error due to the input offset from Opamp-A for small current outputs.

For feedback loop stability, Opamp-A and B in Fig. 3 are constructed using single-stage symmetrical operational transconductance amplifiers (OTA). The output transistors $M0$ and $M1$ are seen as the second stage which can be Miller

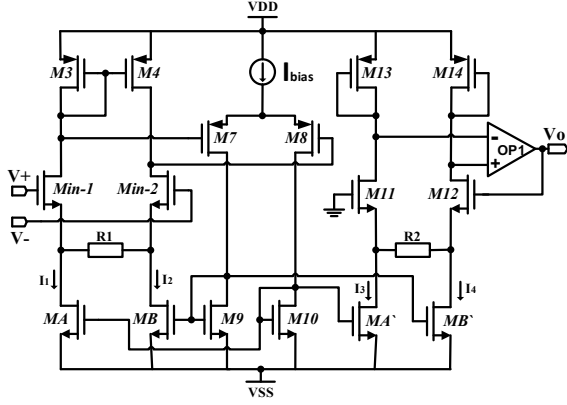


Fig. 4. Current feedback IA.

compensated to improve loop stability (see Fig. 3). To provide the full voltage compliance, the buffers at the inputs of Opamp-B require rail-to-rail swings. The buffer opamp is implemented using a bulk-driven input pair in combination with a level shifter based on [12]. The source and sink currents are connected to the load through the H-bridge controlled by a SPWM generator.

C. SPWM Generator

Fig. 5 shows the architecture of the SPWM generator. It contains a 9-bit counter, whose lowest three bits, *Amp_cnt*, control the duty cycle modulation, and the highest six bits, *Smpl_cnt*, address a look-up table (LUT) to read out pre-stored samples of a sinusoidal wave. There are 16 samples stored in the LUT, representing the first quarter of a sinusoidal cycle. The size of the LUT is 32-bit. After address mapping and data reconstruction, a 64-sample sinusoidal wave with 3-bit resolution per sample is constructed. When enabled, *Smpl_cnt* updates on every eight cycles of the operating clock, \overline{CLK} , to read out a new sample from the LUT. Within these eight \overline{CLK} cycles, *Amp_cnt* is compared to the reconstructed sample. The comparator output *C* is Logic 1 while the *Amp_cnt* value is less than or equal to the sample value and flips to logic 0 when *Amp_cnt* goes beyond. When operating at 50 MHz, the SPWM generator generates two complementary square waves at a fixed frequency of 6.25 MHz, whose duty cycle is modulated by a 98 kHz sinusoidal wave at a 3-bit resolution. The output SPWM square waves drive the H-bridge, as shown in Fig. 3.

IV. SIMULATION RESULTS

A. Spectral Purity

The spectral purity of the SPWM output has been modelled in Matlab (R2014a, Mathworks). Its spectrum is shown in Fig. 6 and is compared with spectra of a 98 kHz pseudo-sinewave generated from a 4-bit DAC at 64 samples per cycle, and a 98 kHz 50% duty-cycle square wave. As shown the injecting current contains harmonic noise in the high frequency band. Spectral purity is important for bioimpedance measurements. Applying a second-order 300 kHz Butterworth lowpass filter at the measuring end, e.g. after the IA in Fig. 1, to all three types of waveform, the high frequency harmonics can be suppressed. The spurious-free dynamic range (SFDR) of the SPWM after filtering is 33.1 dB, compared to 48.2 dB for the pseudo-sine and 12.3 dB for the 50% duty cycle square wave. These results

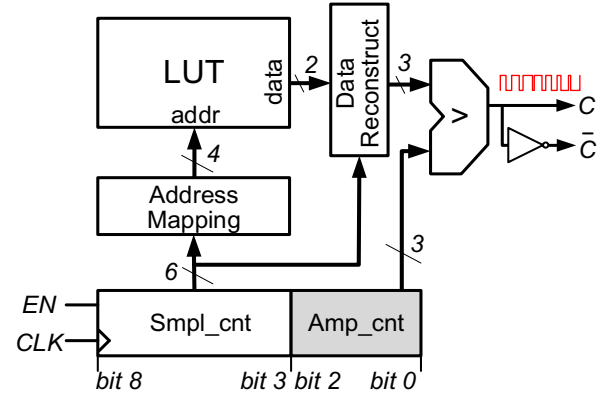


Fig. 5. Architecture of the SPWM generator.

suggest that the SPWM achieves a good trade-off between signal quality and circuit simplicity. Compared with the pseudo-sine solution that has been widely used in EIT and EIS designs [2] [6], SPWM provides acceptable SFDR with the advantage of eliminating the need of one or more multi-bit DAC implementations. The SPWM generator is fully digital where the LUT only contains 32 bits. On the other hand, SPWM provides significantly better SFDR than the square wave, which is also commonly used in EIS systems [10], [13].

Table I. Comparison with other current generators.

Parameter	This Work	[10]	[6]	[5]
Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Supply voltage	± 1.65 V	1.2 V	1.8 V	1 V
Architecture	Feedback controlled	Open-loop	Open-loop	Open-loop
Modulation	SPWM	Square	Pseudo-sine	Semi-ramp
Max. frequency	98 kHz	1 MHz	20 kHz	2 kHz
Current output	0.05 – 1 mA _{pp}	0.01 – 0.2 mA _{pp}	10 – 40 μA_{pp}	0.1 – 1 μA_{pp}
Max. impedance	50 k Ω	-	4.4 k Ω	3.3 k Ω
CMFB (SNR*)	YES (56.5 dB)	NO	NO	NO

*SNR as defined in [7].

B. Circuit Performance

The current generator has been designed in a 0.18- μm CMOS process and operates from ± 1.65 V power supplies. The IA consumes 16 μA while other opamps consume 1 μA each to give a total current consumption of $I_{out} + 22 \mu\text{A}$, where I_{out} ranges from 50 μA to 1 mA (smaller current outputs are possible, when M0 and M1 are biased in sub-threshold region). The output frequency is defined as $f_{CLK}/512$, the power consumption of the SPWM digital control is dynamic with respect to f_{CLK} . For $f_{CLK} = 50$ MHz, the current outputs a SPWM current at 98 kHz when the digital circuit consumes 154 μW using a 1.8 V supply. The digital current consumption is about $f_{CLK} \times 1.7$ pA where f_{CLK} is the operating frequency. The current generator has a maximum voltage compliance of ± 1.25 V that is limited to $V_{CC} - V_{ovM0} - V_{switch_{ds}} - I_{out} \times R_f$. For $I_{out} = 50 \mu\text{A}$, the current generator can drive a maximum load of up to 50 k Ω . At maximum current output, it can drive 2.4 k Ω . Under this condition, Monte-Carlo simulations suggest that the

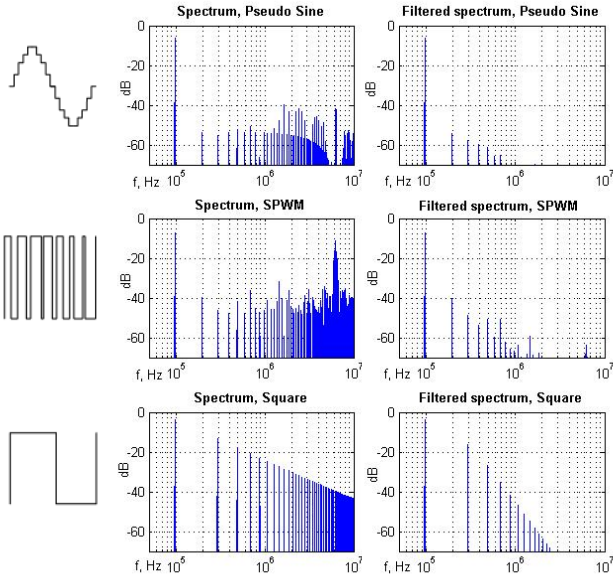


Fig. 6. Spectra of 98 kHz pseudo sine wave (upper row), SPWM wave (middle row) and 50% duty cycle square wave (lower row), and their respective spectra after a 300 kHz second-order lowpass Butterworth filter.

mean output current is 0.99 mA and a mean differential signal to common mode signal noise ratio is 56.5 dB.

Fig. 7 shows the layout of the current generator; it occupies $350 \mu\text{m} \times 320 \mu\text{m}$. Compared with the DAC type current generator, the layout of the proposed current generator is less sensitive to mismatches. At 98 kHz, the post-layout simulation SPWM current output waveform is shown in Fig. 8, alongside the voltage measured across a resistive load, after being further filtered by first- or second-order low-pass filters with a cut-off frequency at 300 kHz. Comparison with other current generators is provided in Table I.

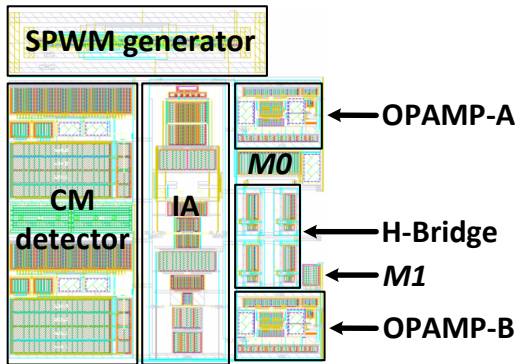


Fig. 7. Layout of the current generator.

V. CONCLUSION

A fully differential SPWM wave current generator for bioimpedance applications has been presented. Benefiting from feedback control, the circuit has high output resistance while

offering a maximum voltage compliance of $\pm 1.25 \text{ V}$. It outputs a maximum 1 mA_{pp} adjustable SPWM current up to 98 kHz with only one output branch. Using a common mode feedback current sink circuit, the current generator's sensitivity to current mismatches is minimized; it is able to autozero the common mode signal to provide a SNR of 56.5 dB.

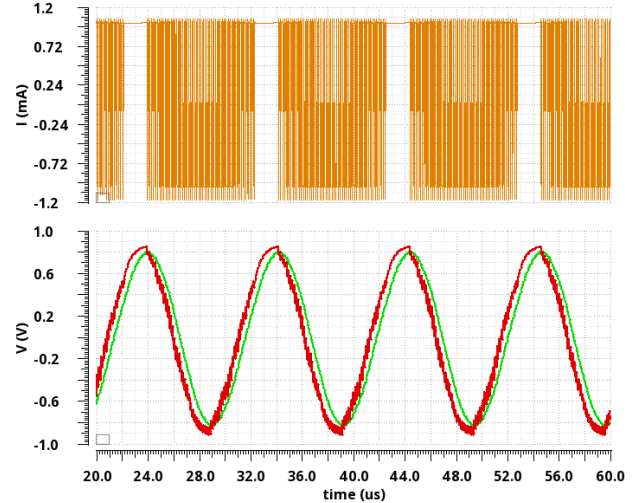


Fig. 8. The PWM sine current output and voltage across a resistive load further filtered by a first-order (red) and second-order (green) lowpass filters.

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