InP DHBT Distributed Amplifiers with up to 235 GHz Bandwidth

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***Abstract*—Three wideband amplifiers in InP double-heterojunction bipolar transistor (DHBT) technology have been designed and measured. The amplifiers use different types of distributed amplifier (DA) topologies, all based on cascode gain cells. A single-stage DA design achieves 7.5 dB gain and 192 GHz bandwidth and a 2-cascaded single-stage DA achieves an average gain of 16 dB with a bandwidth of 235 GHz. The third circuit is a conventional DA with more than 10 dB gain from 70 kHz up to 180 GHz. To the authors' best knowledge, the single-stage DA and the 2-cascaded single-stage DA are the widest band amplifiers in any technology reported to date. Furthermore, the conventional DA has a record bandwidth for circuits in conventional DA topology with gain from near dc.**

***Index Terms*—Distributed amplifiers, heterojunction bipolar transistors (HBTs), indium phosphide (InP), noise figure, wideband amplifiers**

I. Introduction

DISTRIBUTED amplifiers (DAs) in bipolar transistor technology have shown to offer high gain, wide bandwidth and high linearity [1], [2]. Such amplifiers have found applications in optical communication systems and wideband pulse systems with their design basis and fundamental limitations been studied and reported in the late 1990s [3]-[5]. More recently, ultra wideband amplifiers, in both distributed and non-distributed topologies, using heterojunction bipolar transistor (HBT) technology have been reported by several research groups and have shown that bandwidths up to and beyond 100 GHz with more than 10 dB gain are possible. These amplifiers have been fabricated in technologies that range from SiGe [6] to InGaP [7] and InP HBT [2], [8], [9]. Due to the impressive cutoff frequencies of advanced InP-based HBT processes, this is a very suitable technology to achieve DAs with extremely large bandwidths [2], [10].

In [11], we presented amplifiers with record bandwidth utilizing a state-of-the-art InP DHBT process with 250 nm emitter width. The circuits were designed in single-stage and 2-cascaded single-stage DA topologies based on a cascode gain cell. The 2-cascaded single-stage DA design demonstrated a 3-dB bandwidth of 235 GHz with an average gain of 16 dB and thus achieved a gain-bandwidth product (GBW) of 1480 GHz. The high bandwidth and GBW make this amplifier suitable for picosecond pulse applications and future high-speed optical communication systems.

In this paper we extend the analysis of InP DHBT DAs and also present noise figure measurements of the state-of-the-art DAs reported in [11]. Furthermore, we demonstrate a new circuit using the same process but in conventional DA topology in order to compare the differing DA topologies. This new amplifier has a record bandwidth, 180 GHz, for circuits in conventional DA topology with gain from near dc.

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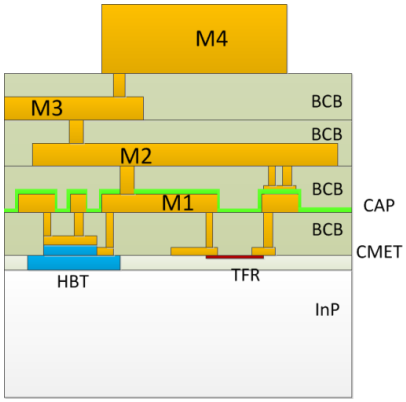


Fig. 1. Schematic view of the multilayer interconnect back-end process.

II. Technology

The circuits presented in this paper use an InP DHBT process with 250 nm emitter width from Teledyne Scientific. The unity-gain cutoff frequency (f_T) is 350 GHz and the power-gain cutoff frequency (f_{max}) is 600 GHz. The process is described in detail in [12].

The process has a multilayer interconnect back-end process with four metal layers (M1 to M4) separated by 1 µm benzocyclobutene (BCB) dielectric. A schematic cross-section view of the back-end is shown in Fig. 1. The thickness of M1−M3 is approximately 1 µm, whereas M4 is 3 µm thick to support higher current densities. The process includes thin-film resistors (TFRs) and metal-insulator-metal (MIM) capacitors. The substrate thickness is 100 µm. In the circuits presented in this paper, thin-film microstrip lines are used. The topmost layer, M4, is utilized for signal and the second metal layer, M2,

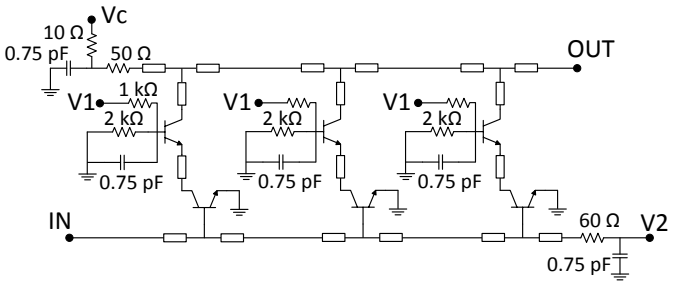


Fig. 2. Circuit schematic of the conventional distributed amplifier.

as ground plane. This allows low inductive connection between emitter and ground which is highly important for achieving high gain when operating up to frequencies close to f_{max}. Furthermore, the first metal layer, M1, is shielded from the RF signal by M2 and can be used for dc connections without disturbing the RF signal lines on M4.

III. Conventional Distributed Amplifier

The schematic diagram of the designed conventional DA is shown in Fig. 2. It comprises one input artificial transmission line (ATL) and one output artificial transmission line with three gain cells in between. The ATLs incorporate the input and output capacitances of the gain cells and the inductive elements are realized using narrow microstrip lines. Each gain cell is a cascode stage with a common-emitter transistor and a common-base transistor. As the RF signal propagates along the input ATL, it is amplified and transferred to the output line by the gain cells. Part of the input power is absorbed by the terminating resistor. On the output ATL the signals from the gain cells add in phase in the forward direction if the phase velocity of the input and output ATLs are equal. Waves travelling in the backward direction on the output line will not add in phase and will eventually be absorbed in the terminating resistor.

The number of gain cells in a conventional distributed amplifier is limited by the attenuation in the input and output ATLs. Every additional gain cell results in longer input and output ATLs with increasing attenuation and it will eventually result in losing the gain advantage of a higher number of gain cells. The attenuation along the input base line results in lower input power to each successive gain cell. Similarly, the attenuation on the output collector line will reduce the power from the first cell to the circuit output. This limits the achievable gain and, since the attenuation increases with frequency, also the bandwidth of a conventional distributed amplifier [13], [14].

The attenuation of the ATLs is a function of not only loss in the microstrip lines but also the input and output impedances of the gain cells. The input line can be modeled by the equivalent circuit in Fig. 3(a), where L_I is the inductance in the microstrip line, r_b is the base resistance of the common-emitter device, r_π the input shunt resistance, and C_π the device input capacitance. The equivalent circuit can be transformed into the circuit in Fig. 3(b) where the device components are replaced by two parallel components r_{eq} and C_{eq}, which are find by the relation

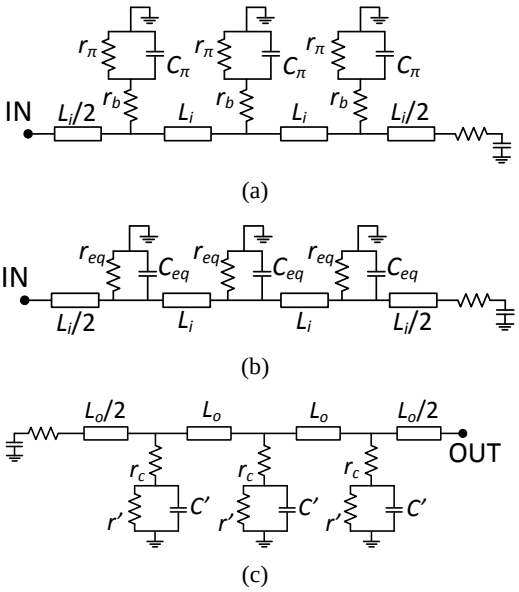


Fig. 3. Models for ATLs of the conventional DA. (a) Equivalent circuit of input ATL. (b) Parallel impedance transformation of input ATL. (c) Equivalent circuit of output ATL.

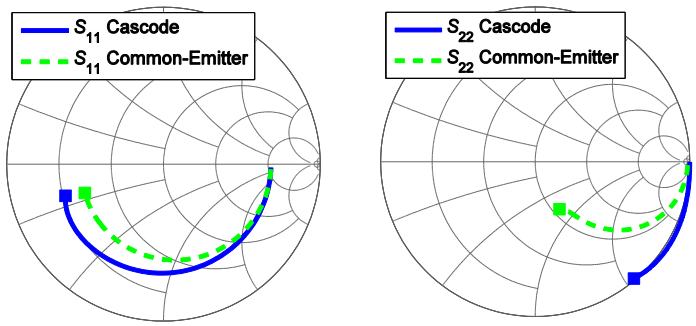


Fig. 4. Simulation of (a) S_{11} and (b) S_{22} for the cascode cell and a comparable common-emitter cell between 1 and 200 GHz, the squares mark the high frequency end.

$$\frac{1}{r_{eq}} + j\omega C_{eq} = \frac{1}{r_b + r_\pi || j\omega C_\pi} \tag{1}$$

where ω is the angular frequency. Neglecting resistive loss and capacitance in the microstrip line, the attenuation constant for one section of the input ATL can be expressed as

$$\alpha_I = \frac{1}{2}\sqrt{\frac{L_I}{C_{eq}}}\frac{1}{r_{eq}} \tag{2}$$

By inserting r_b, r_π, and C_π and assuming $r_b << r_\pi$ and $(\omega r_b C_\pi)^2 << 1$ the attenuation constant can be approximated by

$$\alpha_I \approx \frac{1}{2}\sqrt{\frac{L_I}{C_\pi}}\left(\frac{1}{r_\pi} + \omega^2 r_b C_\pi^2\right) \tag{3}$$

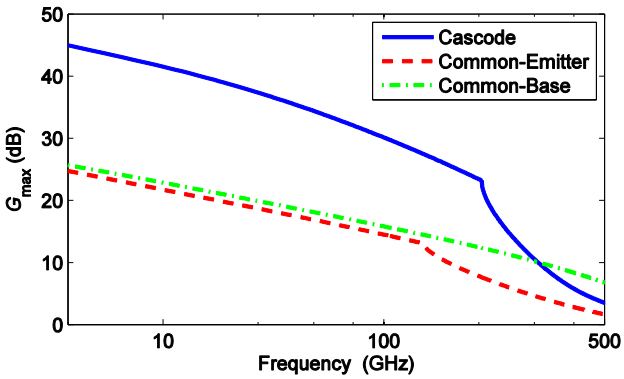


Fig. 5. Simulation of maximum gain versus frequency for cascode cell, common-emitter cell, and common-base cell.

For the output ATL the attenuation is more complex to derive. A simplified equivalent circuit of the output ATL is shown in Fig. 3(c), where r_c is the parasitic collector resistance of the common-base device, r' and C' are mainly determined by the collector to emitter resistance and the collector to base capacitance, respectively, of the two devices in the cascode cell [14]. As r_c is very small, the output ATL attenuation constant per section is approximated analogous to the input line attenuation by

$$\alpha_O = \frac{1}{2}\sqrt{\frac{L_O}{C'}}\frac{1}{r'} \tag{4}$$

The cascode cell has a high output resistance r' compared to a common-emitter cell which reduces the output ATL attenuation and thereby increases the gain-bandwidth performance [15].

The simulated scattering parameters for the input, S_{11}, and output, S_{22}, of the cascode cell and a comparable common-emitter cell are shown in Fig. 4(a) and 4(b), respectively. Although the behavior is somewhat similar, the input of the cascode configuration displays slightly lower losses than its common-emitter counterpart. On the output is the cascode considerably better with $|S_{22}|$ close to unity whereas S_{22} for the common-emitter cell approaches 50 Ω at high frequencies. The simulated scattering parameters indicate that the input ATL attenuation is larger than the output ATL attenuation and consequently that the input resistance of the HBT is the major limitation on the gain-bandwidth performance.

The bandwidth of the distributed amplifier is also limited by the cutoff frequency of the ATLs. The cutoff frequency is limited by the input and output capacitance of the gain cell and can be given, to a good approximation, by

$$f_C = \frac{1}{\pi\sqrt{CL}} \tag{5}$$

where L is the inductive component of transmission line and C the capacitance of the respective input or output ATL [16]. The cutoff frequency is lower for the input line than the output line since the input capacitance C_π is larger than the output capacitance as is visible in Fig. 4. The capacitance C_π is a function of the emitter area and the bias current. The emitter

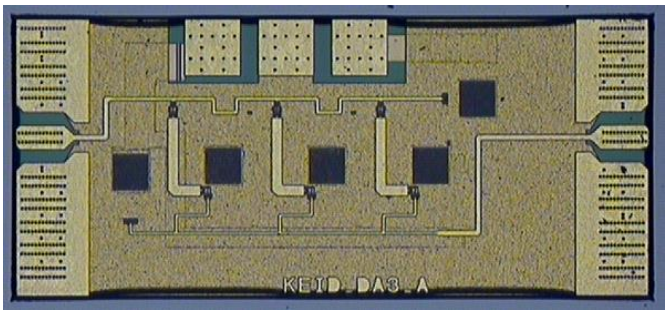


Fig. 6. Microphotograph of the fabricated conventional distributed amplifier. The circuit size is 0.86 mm × 0.37 mm.

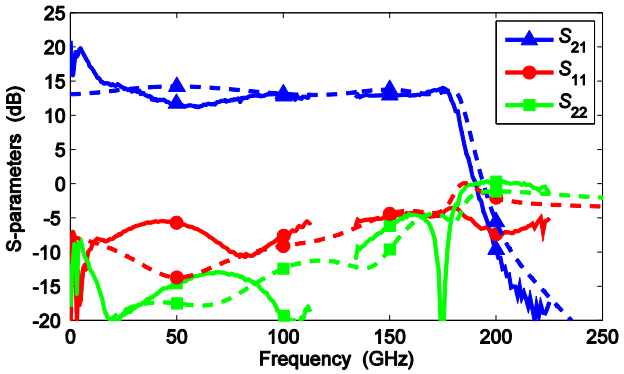
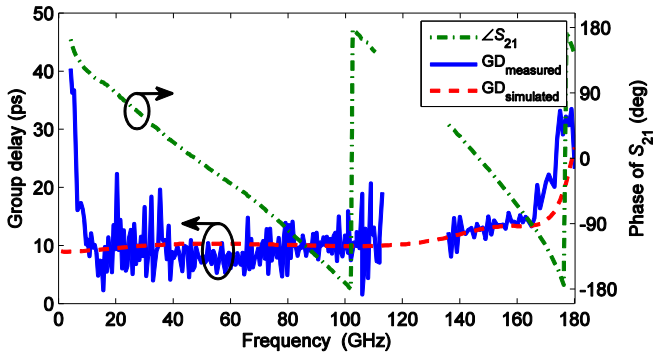


Fig. 7. Measured (solid lines) and simulated (dashed lines) S-parameters of the conventional distributed amplifier.

area in the cascode cell transistors is thus a trade-off where a smaller emitter area reduces the input capacitance which increases the bandwidth, but at the expense of lower gain and lower output power [16]. In similar will a lower bias current reduce the input capacitance but also the gain and output power. In the conventional DA, an area of 6 µm × 0.25 µm was chosen for all devices. The devices are biased at I_B = 0.26 mA, V_{CE} = 1.6 V, and I_C = 7.1 mA/µm^2. The bias is supplied through the input and output transmission lines with two independent voltage sources, V_1 and V_2. The collector voltages and the base currents of the common-emitter devices are supplied directly from these lines. The base current to the common-base devices is supplied from V_1 via a resistive voltage divider at each gain cell.

The maximum available gain, G_{max}, is significantly higher for the cascode cell than what can be obtained from a single common- emitter cell or a single common-base cell. In Fig. 5, simulations of G_{max} versus frequency for the cascode cell used in the amplifier, a common-emitter cell and a common-base cell are shown and clearly indicate the gain advantage of the cascode cell.

The circuit was simulated using the circuit simulator Agilent ADS. In order to have a high inductance, the width of the microstrip lines in the input and output ATLs were chosen as narrow as the process tolerances allow, which resulted in a characteristic impedance of 70 Ω. The distance between each gain cell is 138 µm. The simulated loss of the microstrip lines is 1.2 dB/mm. The lengths of the input and output lines are close to identical in order to have equal phase difference between the



ig. 8. Measured (solid line) and simulated (dashed line) group delay ariation of S_{21} versus frequency for the conventional distributed mplifier.

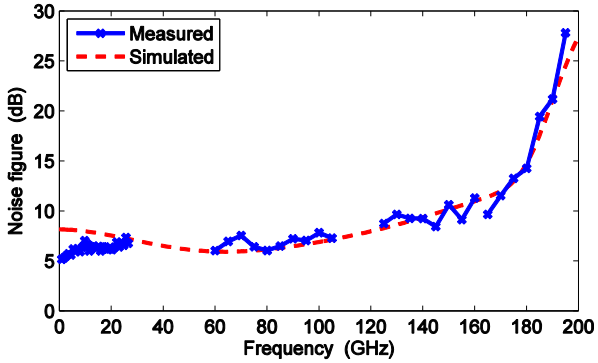


Fig. 9. Measured and simulated noise figure for the conventional distributed amplifier.

gain cells. The lengths were manually optimized to achieve high bandwidth, flat gain, and good input and output matching. A high impedance microstrip line, Z_C = 70 Ω, was used at the output of each gain cell to improve the bandwidth. The length of these peaking lines are critical for the gain roll-off characteristic and the circuit stability. The size of the terminating resistor on the input ATL determines the input matching and gain flatness, primarily below 50 GHz. The connections from the input transmission line to the common-emitter devices were designed to be as short as possible since any inductance here reduces the gain and the bandwidth. The two devices in each gain cell are connected with a low impedance-low loss microstrip line. Three gain cells were found to be optimal and simulations showed no improvement in terms of bandwidth and gain when adding a fourth cell.

Fig. 6 shows a microphotograph of the fabricated circuit. The circuit size is 0.86 mm × 0.37 mm. The common-emitter devices are visible on top of the "L"-shaped transmission lines and the common-base devices are seen on the lower right of the same line.

Due to the very large bandwidths of the DAs in this paper, there are no measurement systems available that can measure the S-parameters over the entire bandwidths. Therefore, the circuits were measured in three separate frequency bands, using three different network analyzers. LRRM probe tip calibration was used in all frequency bands. Between 70 kHz and 115 GHz, an Anritsu VectorStar MS4647A network analyzer with Anritsu 3743A frequency extenders were used. For 130 to 220 GHz and 220 to 300 GHz, an Agilent N5222A PNA with OML WR-05 and WR-03 frequency extenders, respectively, were utilized. Below 115 GHz, 1-mm coaxial probes were used and in the higher bands waveguide probes were used. Unfortunately, no measurements were done between 115 and 130 GHz due to non-availability of test equipment in this band.

The measured and simulated S-parameters of the conventional DA are shown in Fig. 7. The amplifier demonstrates more than 10 dB gain from 70 kHz up to 180 GHz. At 180 GHz and above, the gain drops sharply. Below 15 GHz, the gain increases as the frequency approaches dc. This is due to limitations in the capacitive decoupling at the dc lines and influence of dc probe inductance. Simulations show that larger capacitors would improve the gain flatness in this region.

The phase of S_{21} and the group delay of the amplifier are shown in Fig. 8. The average delay is close to 10.2 ps from 6 to 170 GHz which is close to simulation except at the lower frequencies.

The conventional DA was also characterized in terms of noise figure. The noise figure was measured in four different frequency bands using the Y-factor method [17]: 10 MHz−26 GHz, 60−105 GHz, 125−160 GHz, and 165−195 GHz. The bandwidths are limited by the mixer and/or the LO source used in each measurement setup. Eccosorb at room temperature and immersed in liquid nitrogen were used as hot and cold load at the frequencies above 75 GHz. In the lowest measured frequency band, a solid state noise source was utilized. The measured noise figure is shown in Fig. 9 together with the simulated one. The simulation agrees well with the measurements except for the lower frequencies where the measured noise figure is considerably lower than the simulated due to the higher gain. The noise figure is below 10 dB up to approximately 150 GHz.

IV. Cascaded Single-Stage Distributed Amplifier

To overcome the fundamental limit in terms of gain for the conventional distributed amplifier and to increase the bandwidth, two circuits based on the same basic building block were designed: a single-stage distributed amplifier and a 2-cascaded single-stage DA. A cascode gain cell, similar to the one in the conventional DA, was used in these two circuits.

A. Single-Stage Distributed Amplifier

The circuit schematic of the single-stage DA is shown in Fig. 10. The circuit consists of one of the three sections in the conventional DA, but with the base of each device in the gain cell biased separately to enable more testing and tuning flexibility. The decoupling capacitors terminating the input and output ATLs are larger than those in the conventional DA and were chosen to have flatter gain at low frequencies. A microphotograph of the single-stage DA is shown in Fig. 11. The circuit size is 0.52 mm × 0.46 mm.

The S-parameters of the single-stage DA are shown in Fig. 12 together with the simulated ones. The devices were biased at I_B = 0.5 mA, V_{CE} = 2.1 V, and I_C = 11 mA in the measurement.

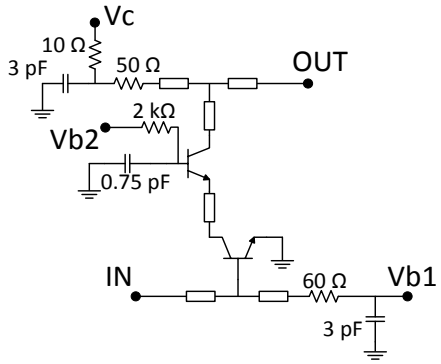


Fig. 10. Circuit schematic of the single-stage DA.

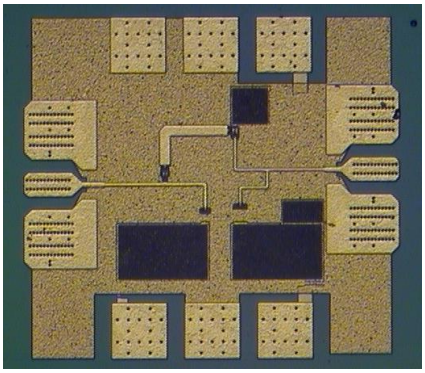


Fig. 11. Microphotograph of the fabricated single-stage DA. The circuit size is 0.52 mm × 0.46 mm.

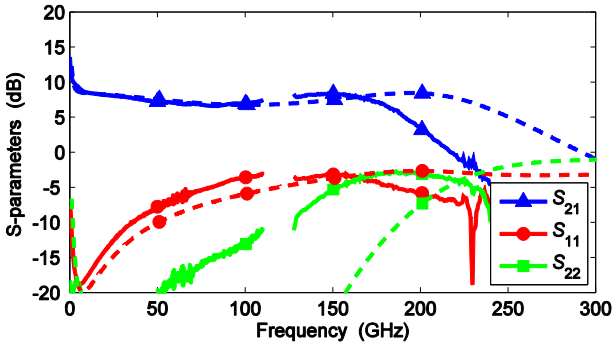


Fig. 12. Measured (solid lines) and simulated (dashed lines) S-parameters of the single-stage DA.

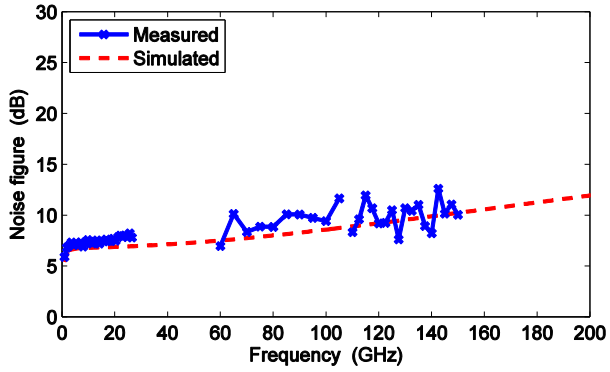


Fig. 13. Measured and simulated noise figure for the single-stage DA.

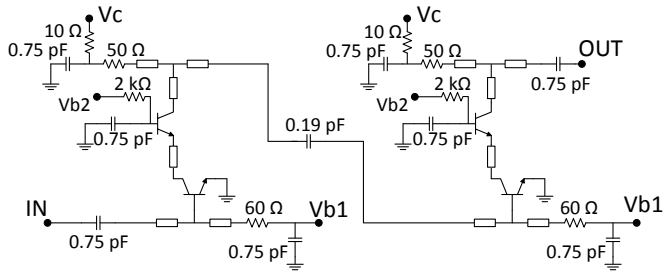


Fig. 14. Circuit schematic of the 2-cascaded single-stage DA.

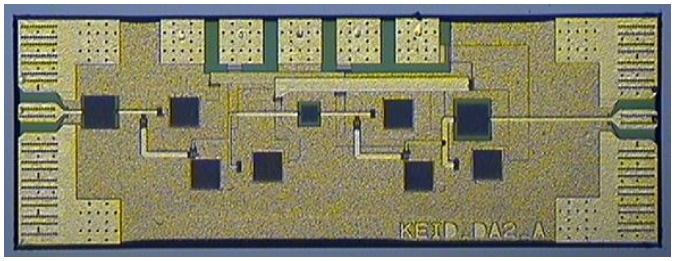


Fig. 15. Microphotograph of the fabricated 2-cascaded single-stage DA. The circuit size is 1.09 mm × 0.38 mm.

The simulation is slightly modified from [11] to account for the inductance in the connection from the input microstrip line to the base of the common-emitter device. The measured average gain is 7.5 dB with a gain ripple of ±1 dB from 1.3 GHz up to 194 GHz. Although very large, the bandwidth is smaller than expected from the simulations. Compared to the conventional DA, the gain is lower, due to the single gain cell, but the bandwidth is slightly larger, as expected since the input ATL attenuation at higher frequencies is less with only one stage. The input and output return loss values are below 0 dB over the entire measurement range. The measured and simulated noise figure is shown in Fig. 13. The D-band noise figure measurement setup was slightly improved, using a different LO source compared to previous measurements, which shifted this measured band to 110–150 GHz. The variations of the measured noise figure in the higher measured frequency band are due to measurement difficulties resulting from the low gain of the amplifier. We were due to this unable to measure in the frequency band 160−195 GHz.

B. 2-Cascaded Single-Stage Distributed Amplifier

To attain higher gain and wider bandwidth than the single-stage DA and the conventional DA, a 2-cascaded single-stage DA amplifier with two stages in a distributed amplifier topology was designed. Each of its two cascaded stages is similar to that of the single-stage DA described above. The gain of such an amplifier can be significantly higher than that of a conventional DA with an equal number of transistor cells. For an ideal lossless conventional DA, the gain is a function of the square of number of stages *n*, whereas it for a cascaded single-stage DA it is an exponential function of *n* [13]. Furthermore, no limit in the number of gain cells in a cascaded single-stage DA, additional stages can be added in cascade in order to increase the gain. The circuit schematic of this amplifier is

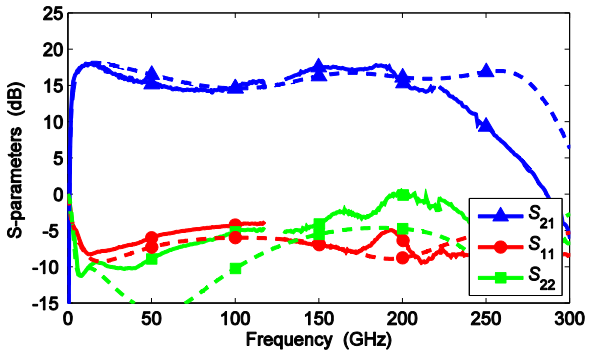


Fig. 16. Measured (solid lines) and simulated (dashed lines) S-parameters of the 2-cascaded single-stage DA.

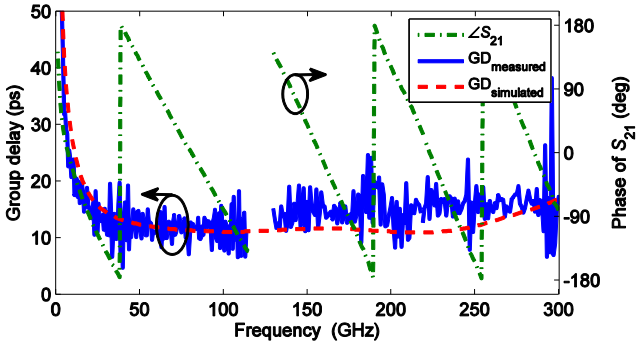


Fig. 17. Measured (solid line) and simulated (dashed line) group delay variation of S_{21} versus frequency for the 2-cascaded single-stage DA.

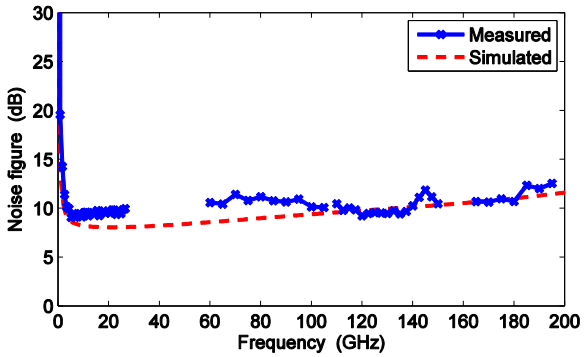


Fig. 18. Measured and simulated noise figure for the 2-cascaded single-stage DA.

shown in Fig. 14. The bias arrangement of the two cascaded stages necessitated some interstage dc isolation which was done using a dc blocking MIM capacitor. This capacitor limits the operation of the amplifier at lower frequencies with zero gain as the frequency approaches dc. The size of the capacitor is inevitably a compromise between low frequency and high frequency responses and was chosen to have a value close to 200 fF resulting in a low frequency cut-off below 2 GHz. Due to this cut-off, it is not necessary that the decoupling capacitors terminating the input and output ATLs are as large as in the single-stage DA. The microstrip lines were slightly modified compared to the conventional DA, with shorter and wider lines on the input and output, in order to improve the bandwidth and to have flattest possible gain. A chip microphotograph of the 2-cascaded single-stage DA is shown in Fig. 15. The size of the circuit is 1.09 mm × 0.38 mm.

In Fig. 16, the S-parameters of the 2-cascaded single-stage DA are shown. An average gain of 16 dB with less than ±2 dB gain ripple is demonstrated over a bandwidth from 2.0 to 237 GHz. The measured phase of S_{21} and the derived group delay of the 2-cascaded single-stage DA is shown in Fig. 17. The phase varies linearly across the band from 10 GHz to 280 GHz, which results in a nearly constant average group delay of 14 ps (with ±9 ps measured variation) in this band. The average group delay is close to that predicted from simulation. This indicates the potential of the 2-cascaded single-stage DA for low intersymbol interference and low bit error rates at high data rates. Fig. 18 shows simulated and measured noise figure of the 2-cascaded single-stage DA. The noise figure is less than 10 dB between 112 and 138 GHz, but higher than that expected from simulation below these frequencies.

V. Discussion

Table I shows a comparison of our results with those of similar reported wideband amplifiers. The gain is defined as the average small-signal gain over the bandwidth. To our best knowledge, the single-stage DA and the 2-cascaded single-stage DA presented in this paper surpass the bandwidth of all other amplifiers reported to date. The conventional DA presented in [18] has slightly higher bandwidth than the conventional DA demonstrated in this paper. It has however no significant gain below 40 GHz whereas the conventional DA in this paper has gain to 70 kHz. Each of the three amplifiers has a dc power consumption below 120 mW and an area less than 0.41 mm^2, which is very competitive when compared to other similar amplifiers.

VI. Conclusion

A conventional distributed amplifier, a single-stage DA, and 2-cascaded single-stage DA have been designed and measured. All three circuits use a cascode gain cell unit and were fabricated in an InP DHBT process. The conventional DA demonstrates more than 10 dB gain from 70 kHz up to 180 GHz and the 2-cascaded single-stage DA have an average gain of 16 dB from 2 to 237 GHz. To the authors' best knowledge, these are largest bandwidths for amplifiers reported so far in any technology. In addition, the 2-cascaded single-stage DA has a gain bandwidth product of 1480 GHz, which is one of the largest for amplifiers operating above 50 GHz. Comparing the conventional DA and the cascaded single-stage DA topologies, it becomes clear that the cascaded single-stage DA topology can offer larger bandwidths and higher gain than the conventional DA topology. To the authors' best knowledge, this is also the first time that the cascaded single-stage DA topology is used with InP-based HBT technology. By trading off some gain in the single-stage DA to improve the bandwidth it should be possible to have a 3-cascaded or 4-cascaded single-stage DA with even greater bandwidth. Another interesting alternative is to include an emitter-follower in the gain cell to reduce the input ATL attenuation and thereby improve the gain and the bandwidth of the circuit.

TABLE I
COMPARISON TO SIMILAR REPORTED WIDEBAND AMPLIFIERS

Ref.	Gain (dB)	Bandwidth (GHz)	GBW (GHz)	DC Power (mW)	Area (mm^2)	Topology	Technology
[6]	13	81	362	495	1.17	Differential conventional DA	- SiGe HBT
[7]	16	80	504	265	1.2	Emitter follower and cascode conventional DA	1.4 µm InGaP HBT
[19]	11	90	320	210	1.28	Cascode conventional DA	120 nm SOI CMOS
[20]	14.5	94	500	-	2.75	Cascode conventional DA	130 nm InP HEMT
[20]	7.5	110	>260	-	2.75	Cascode conventional DA	130 nm InP HEMT
[21]	20.5	100	1060	145	0.21	Differential emitter-follower and Cherry-Hooper cell	250 nm InP DHBT
[22]	10	102	323	73	0.29	Emitter follower and cascode conventional DA	120 nm SiGe HBT
[8]	30	43	1360	500	0.70	Differential emitter-follower and Cherry-Hooper cell	1 µm InP HBT
[2]	21	120	1350	610	2.0	Emitter follower and cascode conventional DA	700 nm InP DHBT
[23]	24	95	1500	247.5	0.65	3-cascaded cascode conventional DA	130 nm SiGe BiCMOS
[18]	10	182	575	105	0.33	Cascode conventional DA	250 nm InP DHBT
This work	12.8	180	724	110	0.32	Cascode conventional DA	250 nm InP DHBT
This work	7.5	192	455	40	0.24	Cascode single-stage DA	250 nm InP DHBT
This work	16	235	1480	117	0.41	Cascode 2-cascaded single-stage DA	250 nm InP DHBT

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