An Energy-Efficient 1.2V 4-Channel Wireless CMOS Potentiostat for Amperometric Biosensors

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***Abstract*—Point-of-care (PoC) diagnostics rely on the design of low-power and miniaturized readout units that can offer rapid and accurate test results, replacing the need for specialized equipment. CMOS technology can be exploited in order to design complex systems while achieving high energy efficiency for suitable operation in a mobile settings. This paper presents the design of a novel energy-efficient 4-channel wireless potentiostat chip, based on a dual-slope ADC architecture, that features a low-complexity wireless unit and a calibration approach that does not require additional circuitry. The chip was designed in a 0.35μm CMOS process. The simulated results suggest that each potentiostat channel can achieve an estimated energy efficiency of 2.5 pJ/bit from a 1.2 V supply.**

I. Introduction

Point-of-care (PoC) diagnostics promise to improve the management of infectious diseases by offering rapid and accurate test results, especially in low-resource settings, allowing for a timely initiation of appropriate interventions [1]. The development of handheld platforms with functionality comparable to laboratory-based equipment is a key aspect to enable widespread adoption of PoC devices.

Electrochemical sensing is an attractive method to provide label-free, real-time quantitative detection and monitoring of target analytes. Electrochemical methods rely on the use of a feedback circuit, a potentiostat, which regulates a current flowing between a working and a counter electrode (WE and CE) in order to keep a desired potential between the WE and a reference electrode (RE).

CMOS electrochemical platforms have been developed for numerous applications, including biosensors for neurotransmitter monitoring [2] and air quality control [3]. In order to obtain high energy efficiency, current-mode dual-slope or $\Sigma\Delta$ ADC architecture have been successfully adopted [3] to digitize the sensor current as early as possible, thus avoiding power hungry signal conditioning and amplification stages and achieve power consumptions in the order of tens to few hundreds of μW/channel. This paper presents the design and operation of a novel energy-efficient wireless potentiostat architecture based on a dual-slope ADC architecture, with 4 independently configurable channels. Simulated results show that each potentiostat channel can achieve an energy efficiency in the order of pJ/bit. The ADC is input-modulated in order to extend its dynamic range between pA to μA and features a novel wireless transmission strategy that greatly reduces the complexity of the wireless unit.

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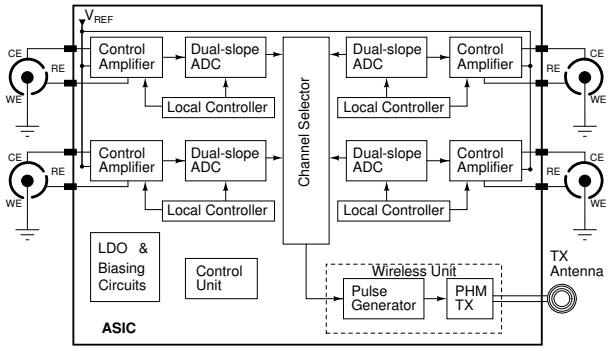

Fig. 1: Architecture of the 4-channel wireless potentiostat.

II. Potentiostat Channel Design

The architecture of the 4-channel wireless potentiostat system is shown in Fig. 1. Each potentiostat channel consists of a dual-mode control amplifier, a dual-slope ADC and a local controller. The wireless unit can be connected to each channel via an off-chip channel selector.

Conventional dual-slope ADCs, however, rely on the use of an on-chip counter and a fast clock, to determine the discharge time of the integrator capacitor, as shown in Fig. 2(a). If a wireless unit is then employed, the counter output needs to be encoded into a data stream via a modulation scheme and sent over a wireless link.

The proposed strategy is based on a modified pulse-harmonic modulation (PHM) scheme [4], whereby only two pulses are sent via the wireless link, one at the start and one at the end of the capacitor discharge period, as shown in Fig. 2(b). These pulses inherently encode the capacitor discharge time, which can be determined at the receiver end. This approach greatly reduces the complexity and power requirements of the wireless link. A pulse generator (PG) generates two short pulses and drive the PHM transmitter (TX) and the antenna. The detailed description of the wireless unit is found in [4].

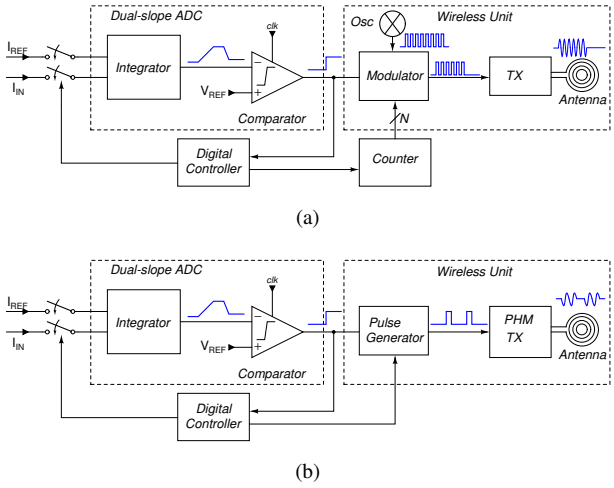

Fig. 2: Wireless potentiostat architecture. (a) Conventional and (b) proposed

A schematic of the channel is shown in Fig. 3. A dual-mode current-mirror-based control amplifier is used to set the electrochemical cell potential V_{RE-WE} to a fixed value. The control amplifier can set a positive V_{RE-WE} or negative V_{RE-WE}, depending on whether a reduction or oxidation current is measured during the chemical reaction. In the former case the working electrode (WE) is connected to ground, whereas in the latter case WE is connected to the supply potential V_{DD}.

The ADC is input-modulated by switches S_{modp} and S_{modn} in order to extend its dynamic range. The core of the dual-slope ADC consists of a switched-capacitor integrator featuring correlated-double sampling and a clocked comparator. The operation of the potentiostat channel can be described with the aid of the timing diagram in Fig. 3. After a global reset phase, ϕ_{rst}, the output of the integrator, V_{int} is held at V_{REF}. During the integration phase, ϕ_1, the input current, I_{IN}, is integrated on the capacitor C_i for a fixed time, t_1 by closing switch S_1. During t_1, V_{int} increases or decreases from V_{REF}, depending on the direction of I_{IN}. During the discharge phase, ϕ_2, the reference DAC is enabled forcing V_{int} to decrease (increase) toward V_{REF}. As the threshold is crossed the output of the comparator, V_{comp} toggles and the conversion is completed. The amplitude of the input current can be determined as:

$$I_{IN} = \alpha \cdot k \cdot \frac{t_2}{t_1} \cdot I_p, \tag{1}$$

where k is the input current modulation index equal to t_1/T_{mod} and α is a gain factor due circuit non-idealities and I_p is the programmable current from the reference DAC.

A. Integrator

The sensor current is integrated directly onto a 6.8 pF capacitor, V_i. The choice of the capacitance value implies relatively long conversion times but results in low thermal noise performance. Correlated double sampling (CDS) is implemented by capacitor C_s, which stores the difference between the output amplifier and a reference voltage V_{REF} and biases amplifier A_2.

The integrator opamp, A_2, was implemented by the inverter-based class-AB amplifier shown in Fig. 4, together with the biasing circuit. An inverter-based architecture was chosen for high-efficiency, rail-to-rail output and low-voltage operation. The simulated performance of the opamp resulted in a low frequency gain of 89 dB and a bandwidth of 27 MHz (100 fF load) at a power supply of 1.2V. The simulated quiescent current was 680 nA with a total current consumption of 920 nA. This results in a figure-of-merit (FOM) of 2930 MHz·pF/mA. The simulated input-referred RMS noise was 7.7 μV in a bandwidth between 10 Hz and 20 kHz.

B. Comparator

A clocked-comparator was adopted for low power consumption. The schematic of the comparator is shown in Fig. 5. It comprises an input latched stage (M_{N1-4} and M_{P1-6}), followed by an SR-latch (M_{N5-8} and M_{P7-10}) and output buffers. In order to reduce the comparator offset, the load capacitance of the input stage, C_{OS}, was implemented by a 6-bit capacitor array. The layout of the capacitor array is shown in Fig. 6. Custom unit capacitors have been designed with minimum sizes to minimize the area of the array. The extracted capacitance of the unit capacitor is approximately 630 aF, resulting in a total C_{OS} of approximately 40 fF. Post-layout simulations have shown that this value accommodates comparator offsets up to 20 mV.

III. Chip Operation

The chip was designed in a 0.35μm 4-metal CMOS technology. It consists of 84 pads for a total area of 2.8-by-2.8 mm^2. The chip layout is shown in Fig. 7 together with the layout of a pixel in the inset of the figure. The performance of the chip was simulated in Cadence Spectre. The key performance parameters are summarized in Table I.

TABLE I: Summary of Simulated Performance.

PARAMETER	UNITS	VALUE
Technology	-	0.35μm CMOS
Number of pads	-	84
Chip area (incl.pads)	mm^2	7.84
Supply voltage	V	1.2
Number of channels	-	4
Channel area	μm^2	670x200
P_{conv}/ch @ 20 kHz	μW	12.06
Resolution	bits	12-16

A. Conversion

Fig. 8 shows the transient operation of the potentiostat channel during one conversion. The ADC clock was set to 10 MHz and the integration time to 409.6 μs, resulting in a resolution of 12 bits. A 1μA cell current I_{CELL} was modulated with an index k of 100 resulting in an average input current, I_{IN} of 10 nA. This current is integrated on the capacitor C_i

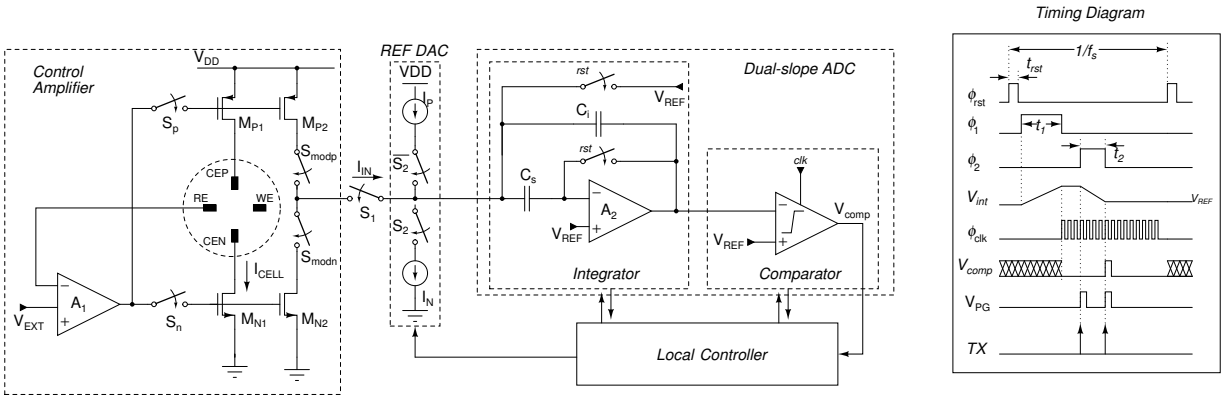

Fig. 3: Detailed schematic of a potentiostat channel.

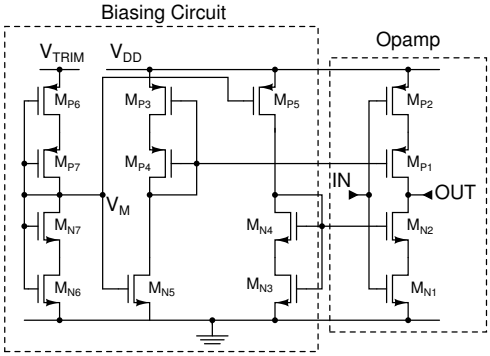

Fig. 4: Implementation of the integrator inverter-based opamp (A_2 in Fig. 3) with biasing circuit.

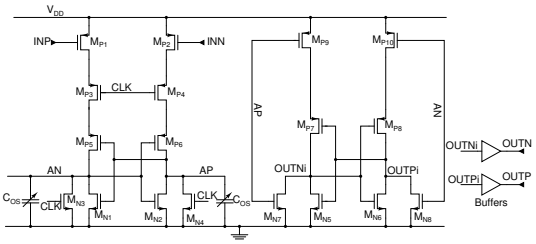

Fig. 5: Schematic of the clocked comparator with trimming capacitors C_{OS} for offset compensation.

resulting in V_{int} ramping up toward the supply voltage. After the end of the integration phase, C_i is discharged back to the reference voltage by a 10 nA (nominal) DAC current. The overall conversion takes approximately 0.8 ms and consumes 12.06 μW resulting in an energy consumption of 2.35 pJ/bit.

B. Calibration

A calibration step is needed in order to derive a gain factor, α, in Eq. 1, which is mainly associated with variations in the nominal values of the REF DAC current, and to remove offset and non-idealities of the comparator. In the former case, a known current can be applied to the ADC and varied until t_1 equals $k{\cdot}t_2$ and hence the reference DAC current, I_p, equals the externally applied current. In the latter case, offset calibration

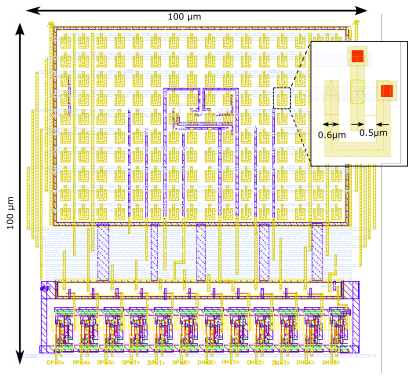

Fig. 6: Layout of implementation of C_{OS}.

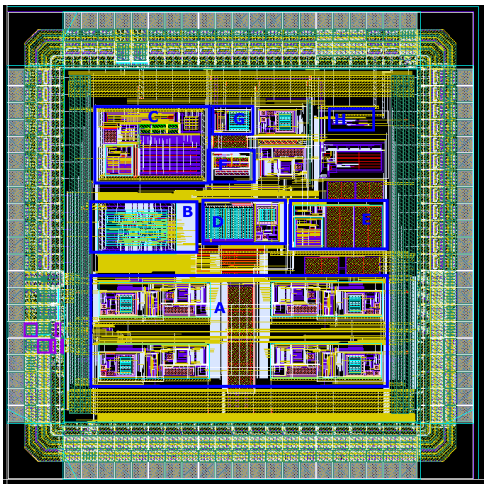

Fig. 7: Chip layout. **A**.4-channel dual-slope ADC with control amplifier **B**. 8-register SPI. **C**. Bandgap. **D**. LDO. **E** Bias cell. **F**. POR. **G**. Beta multiplier. **H**. TX. Unlabeled blocks represent test structures.

can be performed at system level, as illustrated by the transient simulations in Fig. 9.

The operation is similar to that of a first order sigma-delta modulator. The reference DAC current is integrated until the integrator output, V_{int} crosses V_{REF}+V_{OS}, at which point the comparator toggles and the reference DAC current changes

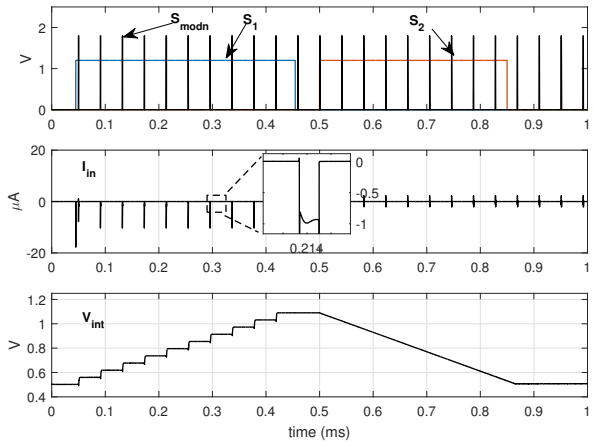

Fig. 8: Transient simulation of potentiostat channel operation.

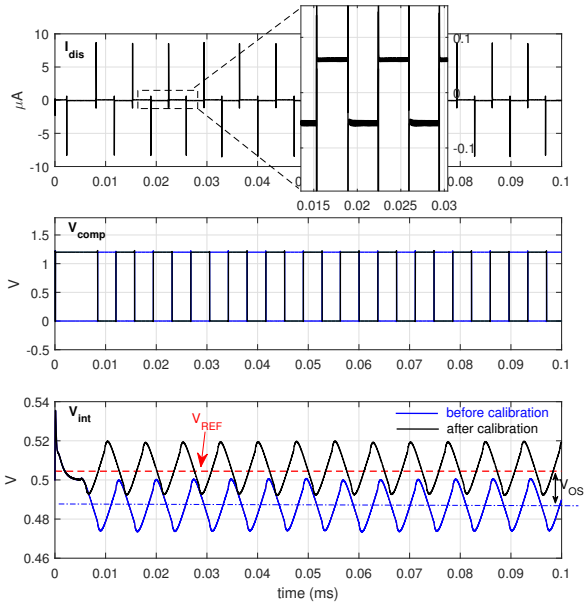

Fig. 9: Transient simulation of calibration of the potentiostat channel.

direction. The offset voltage, V_{OS} can be determined by measuring the average of V_{int} (with a simple first-order external RC filter). The offset can then be reduced by digitally trimming the offset capacitors C_{OS} as described in the previous section. Simulation results have shown that the overall system offset can be reduced to a nominal value of 156 μV.

C. Wireless transmission

Fig. 10 shows the operation of the wireless unit. The PG generates two UWB-like pulses, one at the start of the conversion period, T_{conv} and one at the end of this period, when V_{int} has crossed V_{REF} and the comparator has toggled. The PG drives the transmitter, TX, which excites an external antenna coil at a resonant frequency of approximately 350 MHz. The 2 pulses are then transferred wirelessly to a receiver unit where they are reconstructed by the receiver front-end. The conversion time of the reconstructed pulses, $T_{conv,rec}$, can then be determined with the aid of a counter at the receiver end and the sensor current, I_{CELL} can be derived by setting t_2 equal to $T_{conv,rec}$ in Eq. 1. The simulated efficiency of thr PHM transmitter is 1.49 pJ/bit.

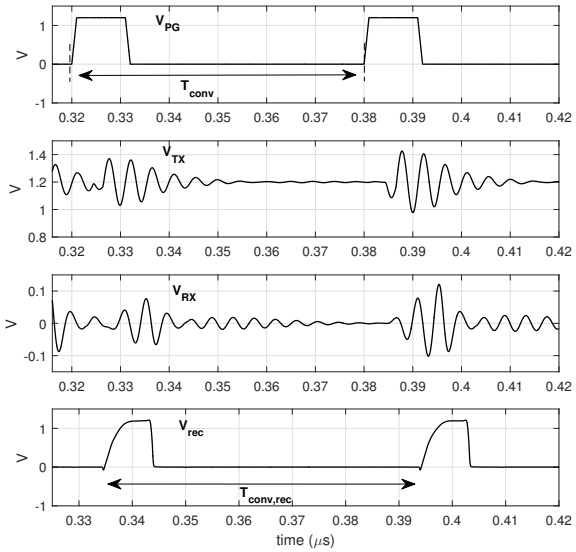

Fig. 10: Simulated transient operation of the wireless unit. Due to prohibitive simulation times the time scale of the wireless operation is much shorter than that of the dual-slope ADC.

IV. Conclusion

This paper has presented the design of an energy-efficient 4-channel wireless potentiostat with reduced complexity, featuring a calibration strategy that does not require additional circuitry. Each channel can be operated independently and interfaced to disposable 3-terminal electrochemical sensors. The potentiostat features a novel wireless transmission architecture that can significantly reduce the energy consumption, which was simulated to be lower than 5 pJ/bit per wireless channel. The potentiostat chip lends itself to the development of hand-held multi-sensor platforms for multiplexed PoC diagnostics.

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