A 4-Wire Interface SoC for Shared Multi-Implant Power Transfer and Full-duplex Communication

Sara S. Ghoreishizadeh*†, Dorian Haci*†, Yan Liu*†, Timothy G. Constandinou*†
*Dept. of Electrical & Electronic Eng., †Centre for Bio-Inspired Technology, Imperial College London, UK
Email: {s.ghoreishizadeh14, d.haci14, yan.liu06, t.constandinou}@imperial.ac.uk

***Abstract*—This paper describes a novel system for recovering power and providing full-duplex communication over an AC-coupled 4-wire lead between active implantable devices. The target application requires a single *Chest Device* be connected to a *Brain Implant* consisting of multiple identical optrodes that record neural activity and provide closed loop optical stimulation. The interface is integrated within each optrode SoC allowing full-duplex and fully-differential communication based on Manchester encoding. The system features a head-to-chest uplink data rate (1.6 Mbps) that is higher than that of the chest-to-head downlink (100 kbps) superimposed on a power carrier. On-chip power management provides an unregulated 5 V DC supply with up to 2.5 mA output current for stimulation, and a regulated 3.3 V with 60 dB PSRR for recording and logic circuits. The circuit has been implemented in a 0.35 μm CMOS technology, occupying 1.4 mm^2 silicon area, and requiring a 62.2 μA average current consumption.**

I. Introduction

Neural Prostheses and Brain Machine Interfaces (BMIs) have experienced significant progress in the last two decades [1]. This is in part due to advances in microtechnology, now allowing integrated *implantable medical devices* (IMDs) to be ultra compact and require ultra low power [2]. Even so, in order to realize a viable implantable device, the energy source remains a challenge; either requiring a large capacity battery, or wireless power transmission. Furthermore, such devices require reliable means for wireless data transfer for calibration and real-time control purposes and/or communicating sensor/actuator/stimulation data.

There has been much work focusing on wireless power and data telemetry [3], however it remains a challenge how to improve efficiency (such that thermal dissipation to be within safe limits) for large-scale brain stimulation applications. Alternatively, a conventional wired link can provide a reliable transmission channel, also avoiding challenges with local heating. However, tunnelling wires subcutaneously poses different challenges, where any electric fields accelerate corrosion leading to leakage currents and eventual failure [4]–[6].

This work proposes a new protocol for wired power and data transmission and develops an integrated circuit for interfacing to a 4-wire lead connecting between the chest and brain implants. The system concept is shown in Fig. 1. The chest implant contains the energy source (rechargeable battery) and processor, thus powering and controlling the brain implant. The brain implant records the neural activity, communicates this via the uplink to the chest unit, this then processes the data, and sends optical stimulation commands back via the downlink to the brain implant.

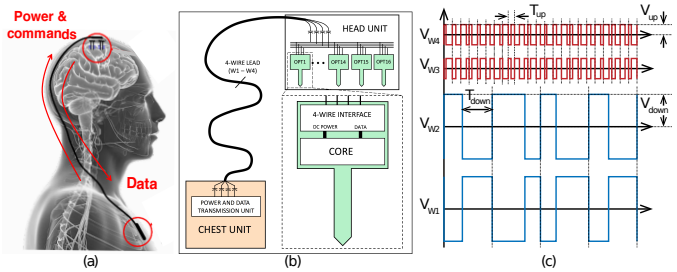

Fig. 1: System concept. (a) subcutaneous lead between implanted chest and head units; (b) Detail of 4-wire connectivity at each end of the lead; (c) how voltage waveforms on the 4-wire look like.

In order to reduce the risk of corrosion to lead-insulation due to the static electric fields, and eliminate any potentially hazardous DC leakage in case of failure, the implants are connected through an AC-coupled multi-wire lead with DC-blocking capacitors placed in series with the lead. Since existing medically-approved leads are typically unshielded [7], a fully-differential power and data transmission scheme is designed to remove the effect of common-mode noise and interferences on the lead. Furthermore, to minimise the number of wires and save energy (i.e. chest implant battery-life), the power transmission and downlink (i.e. chest-to-head) are combined on a single pair of wires. The second pair of wires is used for the uplink (i.e. head-to-chest). Within the brain implant these 4-wires are connected in parallel to multiple identical optrode devices. The system presented herein is monolithically integrated within the optrode to interface between the shared 4-wire lead and the optrode core [8]. This interface receives from the downlink (i.e. recovers/provides a stable DC power supply, generates an upscaled clock and decodes control data), and sends to the uplink (encoding the recorded data). The chest implant requires a complementary 4-wire interface to drive the downlink (encoding control data with power carrier) and receive/decode the uplink data.

This paper is organised as follows: Section II introduces the system architecture; Sections III and IV describe the power management and communication subsystems; Section V presents simulation results and Section VI concludes.

II. 4-wire Interface System Architecture

Both the down- and uplink communications use baseband digital modulation due to the relatively low bandwidth of the communication channel. Manchester coding was chosen in

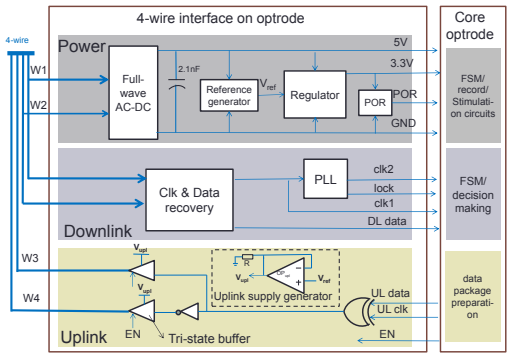

Fig. 2: Top-level system architecture for the 4-wire interface.

order to avoid having sequences of ones (or zeroes) as this would pose a challenge in the receiver hardware after the AC-coupled transmission channel. The top level architecture of the 4-wire interface is shown in Fig. 2, divided into three main blocks: *(i)* Power management; *(ii)* Downlink; and *(ii)* Uplink.

Key design parameters here are the frequency and amplitude of the voltage waveforms on each wire. These are determined as follows: first, to ensure minimal energy loss in the wires, both frequency and amplitude are minimised. Then, since the power and downlink data are combined, the power transmission frequency is chosen based on the downlink datarate requirement, which is 100 kbps. For the uplink however, since a higher datarate is required (≈1.6 Mbps), a higher frequency clock is needed. This is generated using a Phase-Locked Loop (PLL) that is driven by (and synchronised to) the recovered downlink clock. The sections that follow describe the circuit implementation of both the power recovery, and data communication subsystems.

III. Power Management

This consists of a full-wave voltage rectifier generating the required 5 V DC-supply for driving the LEDs (within optrode) that can operate from an unregulated supply. A voltage regulator generates the 3.3 V regulated supply for powering the optrode core circuits. This is gated by a *power-on-reset* (POR) circuit (adapted from the AMS C35B4 A_CELLS library) such that the regulator output is disconnected from the load during startup, and in the event of large voltage drops. A duplicate of the reference generator and voltage regulator (not shown for simplicity) generates a second 3.3 V supply voltage that is used sensitive analogue circuits such as the recording front-end.

A. Full-wave Voltage Rectifier

The system uses square waveforms for power transmission. Key advantages here (over sinusoidal) are: *(i)* this makes it possible to use an on-chip smoothing capacitor to suppress the output ripply; *(ii)* this is easier to generate, thus reducing complexity of the chest unit interface.

The implemented circuit uses a passive rectifier. This is preferable because: *(i)* An active rectifier would require extremely fast (thus power hungry) comparators to recover the square wave; *(ii)* the risk of potential instability here on the fast transitions of the square wave. The passive rectifier circuit is based on the topology used in [9], consisting of a diode-connected PMOS pair and cross-coupled NMOS pair. The rectifier output is smoothed using a 2.1 nF on-chip capacitor that is formed by stacking MIM and MOS capacitors.

B. Voltage Regulator

This is designed to provide a stable 3.3 V DC voltage from the unregulated 5 V supply provided by the rectifier. The circuit schematic is shown in Fig. 3. This is based on a telescopic amplifier driving a pass-transistor that provides the negative feedback, using Miller compensation to eliminate the forward zero by connecting the Miller capacitor to the cascode device. A second compensation capacitor (CC_2) is used to improve the symmetry within the telescopic amplifier, thus improving the *Power Supply Rejection Ratio* (PSRR).

The voltage reference used has been adopted from [10] to provide a high PSRR. Here, the negative feedback around the NMOS devices ensures that output voltage (V_{ref}) remains constant over a wide range of supply voltage.

IV. Full-Duplex Communication

The amplitude of the voltage waveform that is generated at the chest unit to drive the head unit (through the connecting lead) is dynamically determined by the load (i.e. head unit) requirements. Since it is the 5 V unregulated supply that dominates the power consumption of the optrode, V_{chest} is calculated in the following way:

$$V_{chest} = 5\ V + V_{drop,rect} + 2R_{wire}I_{wire} \quad (1)$$

$$I_{wire} = NI_{op,nrm} + I_{op,stim} \quad (2)$$

where $V_{drop,rect}$ is the voltage drop across the rectifier (simulated 0.7 – 1.1 V), N is the number of optrodes, R_{wire} is the lead conductor resistance (for example, 220 Ωm^{-1} for an implantable, medically-approved lead [7]), $I_{op,nrm}$ is the current consumption of each optrode when not stimulating (about 0.2 mA), and $I_{op,stim}$ is the peak stimulation (LED bias) current (1.5 – 2 mA depending on stimulation intensity); The stimulation phase is such that only one LED (on one optrode) is on at any given time, though the stimulating optrode may change during the stimulation time.

In the chest unit, the downlink communication is combined with power transmission as follows: *(i)* downlink (command) data is Manchester encoded using a 100 kHz clock; *(ii)* the encoded data amplitude is scaled to V_{chest}; *(iii)* the amplified waveform is AC-coupled onto $W1$; and *(iv)* inverted and AC-coupled onto $W2$. The uplink communication similarly uses a fully-differential 2-wire ($W3$ and $W4$) channel, that is shared among multiple optrodes. The channel access time is determined by using a unique identifier (ID) that is defined on each optrode using a one-time programmable (OTP) fuse.

A. Downlink System

This consists of two key blocks for recovering the data and clock from $W1$ and $W2$: *(i) Clock and Data Recovery* (CDR) converts the signal for 5 V differential, to 3.3 V single-ended, and recovers the data and downlink clock (clk1@100 kHz); *(ii)* a PLL generates a higher frequency clock (clk2@1.6 MHz) from clk1 to drive the uplink as well as optrode core.

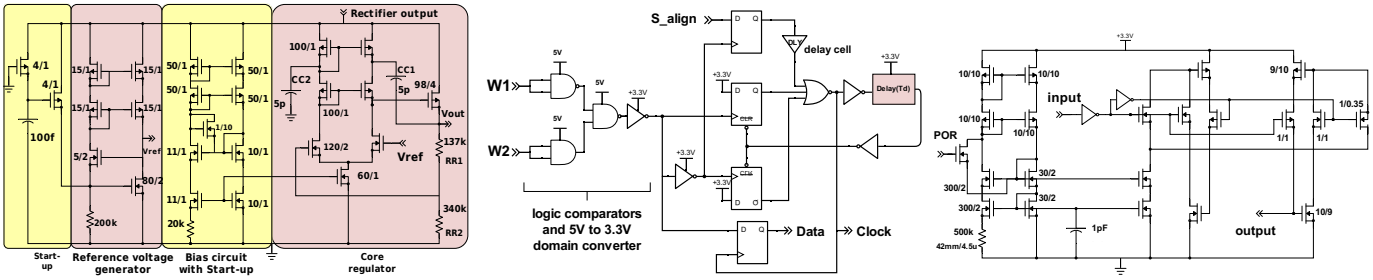

Fig. 3: Voltage regulator circuit (left); Clock and data recovery circuit (middle); Delay (T_d) generator circuit in CDR (right);

1) Clock and Data Recovery (CDR): The CDR circuits are shown in Fig. 3. The differential voltages at $W1$ and $W2$ are fed into a non-hysteretic comparator consisting of two NAND and one AND gates. An inverter (with thick oxide transistors) powered from the 3.3 V supply then shifts the signal level from 5 V to 3.3 V. An edge detector, consisting of two edge-triggered DFF and delay cell detects both the rising and falling edges of the signal. The DFFs reset is driven by a delayed version of the pulses generated on either DFFs. Therefore, a delay of T_d within $T_{Dl}/2$ and T_{Dl} (the period of the downlink clock) is needed to recover the clock correctly.

A thyristor-based delay circuit generates a delay of T_d shown in Fig. 3. To ensure that T_d remains within $T_{Dl}/2$ and T_{Dl} the resistor and transistors within the delay circuit are carefully sized and smoothing capacitor added to reduce any switching feedthrough. Robust data and clock recovery has been confirmed through corner simulations across a 10% supply variation, 30 – 80°C temperature range, and through typical, fast and slow corners.

To align the recovered data to $W1$, a one-off alignment-correction method is embedded within the CDR through a DFF driven by an active-high signal S_{align}. S_{align} is activated after start-up by the *Finite State Machine* (FSM) for a total time of at least T_{Dl}. The following delay cell (DLY) produces a non-critical delay of 2 ns with digital gates to ensure correct transition time with respect to other DFFs.

2) Phase-Locked Loop (PLL): This is shown in Fig. 4, consisting of a phase and frequency detector, charge pump, voltage-controlled oscillator (VCO) and a low-pass filter. The charge pump is adopted from [11], supplying a nominal current of 1 μA to the low-pass filter. The VCO is implemented using a five-stage current-starved ring oscillator.

A lock-detector is embedded within the PLL, through DFF_7, DFF_8 and two delay cells, to acknowledge lock of phase in the PLL. The lock signal is used to reset the optrode core circuits together with the POR signal. The lock-detector inserts the lock signal when PLL has reached a periodic steady-state condition. This is when activity period of the charge-pump is smaller than the delay created by the delay-cells (i.e. 300 ns).

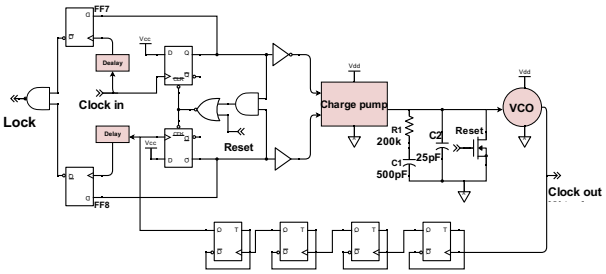

Fig. 4: Phased-locked loop and lock generation circuit.

B. Uplink System

The Manchester encoding is implemented by an XOR gate which combines the uplink data, UL_{data} with uplink clock UL_{clk}. UL_{clk} is decided by the FSM and can be as high as 1.6 MHz as generated by the PLL. A tristate buffer is used to drive the encoded data to the channel when FSM asserts an EN. To reduce the power consumption of the uplink, the tristate buffer supply voltage is reduced to V_{uplink}. The minimum V_{uplink} is estimated from simulations to be 2 V in order for the differential voltage received at Chest implant to settle within the fastest uplink clock frequency. Therefore, a buffer amplifier is designed to generate V_{uplink} from the existing reference voltage described in Section III-B.

C. Heat dissipation consideration

The maximum rise in the temperature of the lead conductor, ΔT_{cnd}, in every second during stimulation is (assuming the tissue temperature remains constant):

$$\Delta T_{cnd} = \frac{2R_{wire}I_{wire}^2 - \frac{\Delta T_{cnd}\alpha_{ins}A_{ins}}{d_{ins}}}{2m_{cnd}C_{cnd}} \quad (3)$$

Where α_{ins}, A_{ins}, and d_{ins} are the thermal conductivity, area and the thickness of the lead insulator. m_{cnd} and C_{cnd} are the mass and thermal capacity of the conductors. The maximum temperature rise in the tissue (ΔT_{tis}) can also be calculated assuming all the power loss on the wire is transferred to a thin layer (e.g. $1mm$) of tissue that surrounds the lead. Replacing the parameters with their values for a $0.5\ m$ biocompatible lead from [7], and assuming the number of optrodes (N) is eight, ΔT_{cnd} and ΔT_{tis} are 2 and $0.8\ mK$, respectively. The maximum number of optrodes is determined from Eq. 2 and 3 to be 16 for a ΔT_{cnd} of $0.5K$ during a 2-minute stimulation.

V. Simulation Results

The 4-wire interface has been implemented in AMS 0.35 μm 2P4M CMOS technology, and validated though full transistor-level simulation using Cadence IC 6.1.6 using foundry-supplied BSIM3v3 models. The total area and average current consumption are 1.4 mm^2 (Layout is shown in Fig. 5) and 62.2 μA, respectively. Thick oxide transistors have been used for all circuits that interact with $W1$ and $W2$. Key circuit

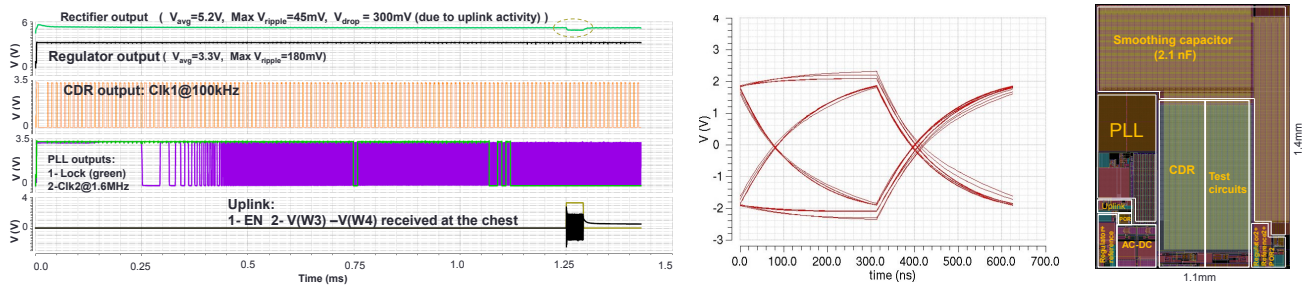

Fig. 5: Simulated waveforms at 4-wire interface system when a 6 V, 100 kHz square-wave is applied to W1 (W2) (left); The eye diagram of the Uplink received at the chest unit (middle); Layout of the 4-wire system in 0.35 μm technology (right).

TABLE I: Achieved (simulated) Circuit Specifications

Circuit	Key Parameters	Value
Rectifier	V_{out}, $I_{out,max}$, $V_{ripple,max}$	≈5 V, 2.5 mA, 0.5 V
Reference generator	I_{DD}, V_{out}, PSRR@0.2 MHz	8 μA, 2.09 V, -65 dB
Regulator	PSRR@1, 200 kHz, I_{DD}, Line Reg.	-76, 46 dB, 21 μA, 0.2 mV/V
CDR, PLL, Uplink	$I_{DD,avg}$	1.2 μA, 10.5 μA, 21.5 μA
Total*	$I_{DD,avg}$, area	62.2 μA, 1.4 mm^2

* excluding secondary regulator

specifications that have been determined through simulation are summarised in Table I.

Simulations indicate that the rectifier can source up to 2.5 mA with peak-to-peak voltage ripple of less than 0.5 V when transient time of the input square-wave is within 5% of its period. The entire 4-wire interface has been simulated by driving W1 and W2 with an ideal square-wave voltage source. Results to the transient analysis are shown in Fig. 5. It can be observed that the maximum voltage-ripple on the regulated 3.3 V driving the CDR and PLL (and a 30 pF capacitor modelling the parasitics of the optrode core circuits) is 180 mV. The PLL locks within 1.2 ms of system start-up and the output of the PLL (i.e. 1.6 MHz) is used directly to drive the uplink system to transmit a 32-bit data package through W3/W4. The received uplink waveform at the other end of the 0.5 m lead, and at 20 pF input capacitance of the chest unit, settles within 90% of the voltage within 300 ns. The eye diagram of the received uplink waveform is shown in Fig. 5 where an ideal source is used to generate the UL_{data} pattern.

VI. Conclusion

This paper has presented a fully-integrated 4-wire interface for transmitting power and full-duplex communication in intrabody implantable devices. The target application is an implantable neural prosthesis with single chest unit wired (using link presented herein) to a head unit consisting of multiple optrode devices connected in parallel. On-chip power management recovers a smooth unregulated 5 V and regulated 3.3 V DC supplies for powering the optrode core circuits with current output of up to 2.5 mA. Full-duplex communication between the chest unit and multiple optrodes is achieved providing a datarate of 100 kbps for downlink and 1.6 Mbps for uplink. The system additionally generates a higher frequency clock (1.6 MHz) for driving the optrode cores. A robust CDR circuit ensures reliable communication between the implants. Table II compares the proposed system with state-of-the-art systems for wired communication.

TABLE II: Comparison with the State-of-the-Art

Feature	This work	[5]	[6]
#wires	4	4	2
#implants	2 – 16	2	2
AC-coupled	Y	N	Y
Power transmission	Y	Y	Y
External components	N	Y	N
Communication	Full-duplex	Full-duplex	Semi-duplex
Encoding (up-, downlink)	Mnctr, Mnctr	Pulse-coding, Mnctr	LSK, PWM
Datarate (up-, downlink)	1.6 Mbps, 100 kbps	100, 600 kbps	– , 222 kbps

VII. Acknowledgement

The work is supported by Wellcome Trust/EPSRC Innovative Engineering for Health Initiative (CANDO project) and the Imperial College Junior Research Fellowship scheme.

References

[1] M. D. Serruya *et al.*, "Brain-machine interface: Instant neural control of a movement signal," *Nature*, vol. 416, no. 6877, pp. 141–142, 2002. [Online]: http://dx.doi.org/10.1038/416141a

[2] W.-M. Chen *et al.*, "A fully integrated 8-channel closed-loop neural-prosthetic cmos soc for real-time epileptic seizure control," *IEEE JSSC*, vol. 49, no. 1, pp. 232–247, 2014. [Online]: http://dx.doi.org/10.1109/JSSC.2013.2284346

[3] G. Bawa and M. Ghovanloo, "Active high power conversion efficiency rectifier with built-in dual-mode back telemetry in standard cmos technology," *IEEE Trans. BioCAS*, vol. 2, no. 3, pp. 184–192, 2008. [Online]: http://dx.doi.org/10.1109/TBCAS.2008.924444

[4] J. Yang *et al.*, "A charge-balanced 4-wire interface for the interconnections of biomedical implants," in *Proc. IEEE BioCAS*, 2013, pp. 202–205. [Online]: http://dx.doi.org/10.1109/BioCAS.2013.6679674

[5] N. Tran *et al.*, "A complete 256-electrode retinal prosthesis chip," *IEEE JSSC*, vol. 49, no. 3, pp. 751–765, 2014. [Online]: http://dx.doi.org/10.1109/JSSC.2014.2298037

[6] L. H. Jung *et al.*, "Design of safe two-wire interface-driven chip-scale neurostimulator for visual prosthesis," *IEEE JSSC*, vol. 48, no. 9, pp. 2217–2229, 2013. [Online]: http://dx.doi.org/10.1109/JSSC.2013.2264136

[7] P. E. Donaldson, "The cooper cable: an implantable multiconductor cable for neurological prostheses," *Med. & Bio. Eng. & Comp.*, vol. 21, no. 3, pp. 371–374, 1983. [Online]: http://dx.doi.org/10.1007/BF02478508

[8] H. Zhao *et al.*, "A cmos-based neural implantable optrode for optogenetic stimulation and electrical recording," in *Proc. IEEE BioCAS*, 2015, pp. 1–4. [Online]: http://dx.doi.org/10.1109/BioCAS.2015.7348357

[9] S. Ghoreishizadeh *et al.*, "An implantable bio-micro-system for drug monitoring," in *Proc. IEEE BioCAS*, 2013, pp. 218–221. [Online]: http://dx.doi.org/10.1109/BioCAS.2013.6679678

[10] A. M. Sodagar *et al.*, "Fully-integrated cmos power regulator for telemetry-powered implantable biomedical microsystems," in *Proc. IEEE CICC*, 2006, pp. 659–662. [Online]: http://dx.doi.org/10.1109/CICC.2006.320862

[11] J. M. Ingino and V. R. Von Kaenel, "A 4-ghz clock system for a high-performance system-on-a-chip design," *IEEE JSSC*, vol. 36, no. 11, pp. 1693–1698, 2001. [Online]: http://dx.doi.org/10.1109/4.962289