Poisson-Schroedinger-Continuity Two-dimensional Analysis of both short (ballistic) and long (drift-diffusion) III-V FETs.

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Abstract

It was recently shown that the quantum mechanical results of the Landauer theory of conduction, applied to a simple one-layer channel FET, can be recast in the traditional drift-diffusion form but with the mobility and injection velocity redefined in a new context. Based on that, we have performed two-dimensional Poisson-Schrödinger-Continuity calculations for both long drift-diffusion and short ballistic quantum well FETs. Very good agreement with many-layer, state-of-the-art InGaAs devices has been achieved provided that only one parameter, the saturation velocity υ_{sat} of the mobility function, is rescaled so that our calculated drain current agrees with the experimental value at very large gate voltages V_G. This single value of υ_{sat} has been used at all other V_G. Our calculations are not only a test of the equivalence described above but valuable information about the sub-threshold regime and especially the leakage currents is obtained. This information is usually absent in rigorous Landauer-type -or equivalently non-equilibrium Green functions- calculations which are performed in simplified FET systems.

Introduction

MOSFETs with III-V channels -also called Quantum Well FETs (QW-FETs) are expected to be the dominant technology in the post-Si area. Such expectations are based on the superior mobilities of these materials as summarized in detail in [1]. The research activity in these type of devices has been intense [2-17]. Originally the focus was on inversion type devices [2-3] but very soon these type of III-V FETs were abandoned in favor of devices with intrinsic channels filled with electrons from a supply layer [4-12]. Furthermore long-gate FETs [4] were quickly substituted with nanometric gate FETs [5-17] and indeed, at the moment, 30-60nm gate length QW FETs with InGaAs channels exist having superior performance such as a subthreshold slope of 96mV/dec and a peak transconductance of 2.4mS/μm [9-10].

Compared to the experimental work, the theoretical work on this type of devices is scarce. There have been two publications dealing with gate leakage [15-16]. One of these uses the tight binding basis to calculate the effective mass [15] and the other ones uses the pseudopotential method [16] both tackling a tunneling problem only. There exists only one paper that analyzes a complete device –i.e. with all its constituent layers. It is by Hwang et.al [17] and uses the Poisson and Continuity equations i.e. they do not use the Schroedinger equation, so any confinement effects are not accounted for. In this paper we will use the full set of the Poisson, Schroedinger and Continuity equations to analyze QW-FETs. The method is a well-established one. It was originally applied successfully to Si MOSFETS [18-19] and then -accordingly modified- to HEMTS [20-21] and to simple surface channel QW-FETs [22]. It is presented in detail in the next section but an initial justification for its use in nanoscale QW-FETs (as opposed to long-gate ones) is given immediately

below. We note that this type of modelling is not available in commercial simulation packages.

The physics of charge transport in nanometer gate length transistors is very different from the drift-diffusion driven long-gate (e.g Lg=200nm) FETs. Transport in the former is ballistic necessitating a quantum approach such as the Landauer theory, to analyze it. However, recently, it has been recognized that the results of the Landauer theory for a simple channel connected to a source and a drain reservoirs can be recast in a drift-diffusion form for both the linear and the saturation regions, provided that the mobility and saturation velocity can be reinterpreted as apparent mobility and injection velocity respectively [23].

However, the above equivalence was derived using as a model a simple channel while state-of–the-art QW-FETs are composed of many layers (excluding the ones needed for mechanical stability). The computational labor needed to perform a full Landauer method – or equivalently a non-equilibrium Green's function method-analysis is by no means trivial. In this paper we examine proposed state of the art QW-FETs with InGaAs channels. We show that the traditional analysis of the Poisson-Schroedinger-Continuity model can be employed also for short gate QW-FETs provided that the numerical value of the saturation velocity of each layer of the multilayer transistor is altered in accordance with the equivalence ansatz or principle described above [23]. More details are given in the method section.

The present work does not constitute only a numerical experiment. Valuable information about the QW-FET, especially in the sub-threshold region can be obtained by utilizing much of the existing software. In particular the leakage currents-usually occurring below the channel layer- and the subthreshold slope can be

evaluated and used to optimize the III-V FETs. This information is lost in strict quantum mechanical calculations which are usually restricted to a one- layer- FET.

Method

We have examined two QW devices. One long gate [4] with Lg=200nm and one nanometric one [8] with Lg=30nm. These are shown in figure 1. Our method follows our previous work on HEMTs [21]. This method is based on solving the fundamental equations of semiconductor physics and –as already stated-was originally applied extensively to Si-MOSFETs [18-19] but has not as yet been employed to multiple layer III-V FETs. These equations are the Poisson-Schroedinger and Continuity equations and are solved as a system of three differential equations for the three unknowns: the potential U, the charge density n and the Fermi level E_{Fn}. They read as follows:

a) the Poisson equation $\nabla^2 U = -\frac{\rho}{\varepsilon_o \varepsilon_r}$ where ρ is the charge density,

b) the Continuity equation $\nabla J_n = 0$ with $J_n = n \cdot \mu_n \nabla E_{fn}$

where J_n is the current density and E_{Fn} the Fermi level and

c) the Schroedinger equation $\left(-\frac{\hbar^2}{2 \cdot m_n^*}\nabla^2 + U_{tot}\right)\Psi(r) = (E - E_C)\Psi(r)$

where E_C is the bottom of the conduction band and m_n^* is the conduction band effective mass. All remaining symbols in the above equations have their conventional meaning.

The above equations are solved in 2 dimensions, i.e. along the depth and length of the device where quantization effects are important. Along the 3rd direction, the width, the device is considered to be of a macroscopic dimension so that eigenstates along this direction are taken care by a one-dimensional density of states function.

In solving the Schrödinger and Poisson equations we must note that the charge density n inside the quantum well is obtained (at each stage of the iteration) by dividing the energy spectrum of the Schrödinger equation into two parts:

a) below the top of the barrier E_{top}, it is obtained quantum mechanically by:

$$n = \sum_i |\Psi_i|^2 * P_{FD}(E_i) * D_{1D}(E_i) \qquad (1)$$

where Ψ_i are the eigenfunctions, P_{FD} is the Fermi-Dirac occupation function and $D_{1D}(E_i)$ is the one dimensional density of states mentioned above;

b) above E_{top} , n behaves as 3D in nature and is obtained by the usual Fermi integral of order one half.

$$n = F_{1/2}(E_F - E_C) \qquad (2)$$

Furthermore, the QW is not taken to be just the channel layer. Additional layers below the oxide layer are included in which the wavefunction Ψ_i decreases exponentially inside them. Also, the QW extends a few nm (typically 5) inside the drain and the source area.

In employing the formula for the current density $J_n = n \cdot \mu_n \nabla E_{fn}$ we note that this formula includes drift, diffusion and thermionic emission currents. When it is applied to a one layer MOSFET channel it delivers the well-known voltage-current characteristics [23].

$$I_{DLIN} = \frac{W}{L} \mu_{eff} Q_n V_{DS} \qquad (4.a)$$

$$I_{DSAT} = W Q_n \upsilon_{sat} \qquad (4.b)$$

where L and W are the length and width of the QW FET, μ_{eff} is the effective mobility and Q_n is the charge below the gate. On the other hand, if the Landauer

theory is applied to a simple MOSFET channel we get the corresponding equations [23].

$$I_{DLIN} = T_{LIN} W Q_n(V_{GS}, V_{DS}) \frac{\upsilon_T}{2\left(\frac{k_B T}{q}\right)} V_{DS} \qquad (5.a)$$

$$I_{DSAT} = \left(\frac{T_{SAT}}{2 - T_{SAT}}\right) W Q_n(V_{GS}, V_{DS}) \upsilon_T \qquad (5.b)$$

where T_{LIN} and T_{SAT} are the transmission coefficient for the linear and the saturation regime respectively and υ_T is the thermal velocity of the electrons. Again the remaining symbols have their conventional meaning.

It can be seen that the two expressions become equivalent if the following assignments are made:

$$\mu_{eff} = T_{LIN} * \frac{\upsilon_T}{2\left(\frac{k_B T}{q}\right)} \qquad (6.a)$$

$$u_{sat} = \left(\frac{T_{SAT}}{2 - T_{SAT}}\right) * \upsilon_T \qquad (6.b)$$

Hence both the linear and saturation regimes can still be treated by the traditional expressions provided that μ_{eff} and u_{sat} are reassigned new values. This equivalence is valid for a system with a single layer (being the channel) to which voltages V_S and V_D are applied at its two ends. We expect that this equivalence will hold true for real QW-FETs which are composed of 3-5 layers at least (excluding the layers for mechanical stability). When the device length is shorter than the mean free path then T_{SAT} is very near the value of one and hence the prefactor is also one, so that this assignment takes care of the ballisticity for short-gate devices. Therefore provided that we can treat u_{sat} as a parameter we choose to continue using the following standard expressions [25] for the field dependent mobility:

$$\mu_n(F_n) = \frac{\mu_{n0} + \upsilon_{sat,n} * \frac{F_n}{F_0^2}}{1 + \frac{F_n^2}{F_0^2}} \qquad (7.a)$$

$$F_n = |\nabla U| \qquad (7.b)$$

where μ_{n0} is the low field mobility, U is the potential and F_0 is a constant equal to $3.1*10^5$ V/m [25]. The quantity υ_{sat} has been fitted only for the short gate device so as to give the correct current I_D at high gate voltages V_G. It amounts to a multiplication of the usual drift velocity by a factor of 10. We note that by the same amount Hwang et al [17] –to be discussed immediately below- have fitted the velocity of their model. Once fitted at high V_G, the same value has been used at all other V_G. For the long-gate device no fitting has been employed and standard values [25] from the literature have been used.

It is worth pointing out that the above approach of fitting the saturation velocity and the mobility to take account of ballistic effects has also been by Hwang et.al [17] but as has been described above they only solve the Poisson and Continuity equations (and not the Schroedinger also) so their approach will not be good enough for nanoscale QW-FETs. We also note that they applied their method to much earlier forms of III-V devices. Furthermore Kotlyar et al [24] have used an approach similar to ours. They have also described ballistic effects by a drift-diffusion formalism but have taken a step further in their analysis of stressed nano-P-MOSFETs and have defined a ballistic mobility which is position dependent. We have not adopted such an approach but have followed the theoretical ground work of [23] as already presented above.

The band-edge offsets have been obtained from Palankovski [25] while the Schottky barriers of the oxides have been obtained from Robertson and Falabretti [26]

and slightly adjusted by 0.2-0.3eV. Their values are still however near the half band-gap of the corresponding oxide. Note that the Schottky barriers can only move the transconductance curves rigidly and do not affect their shape. The same band edges have been used for both devices as their channel and supply materials are the same. We found that it was not necessary to simulate the whole of the device but only 3-5 layers near the channel. The domain of simulation for both devices is shown in figure 1.

Results

Our calculated 2-dimensional charge density inside the simulated domain of the long-gate device is shown in figure 2 for V_D=1V and V_G=1V. Notice the overdoped source and drain regions whose charge density spills below them and the formation of the channel which is pinched at the drain end of the device. The I_D-V_G transconductance characteristics are shown in figure 3. A representative transconductance curve for the linear regime, i.e. V_D=0.1V, is shown in figure 3a. It can be seen that reasonably good agreement with the experimental result is obtained without the need of any fitting. We stress again that all parameters have been obtained from the literature without any fitting (except for u_{sat} for the 30nm FET only). The saturation regime is shown in figure 3b. Three curves are shown in this figure: one is the experimental curve and the remaining two are our calculations for two different depths of the substrate area below the supply channel. It can be seen that very good agreement is obtained, provided that the chosen depth of the simulated device is large enough. As we go into smaller and smaller currents (and consequently smaller and smaller V_G) a larger portion of the substrate needs to be included in the simulated

region to get agreement with experiment. No such problem arises in the low V_D regime due to the absence of parasitic currents as will be explained immediately below.

From the transconductance characteristics we see that the device turns on slowly at large V_D. This is due to parasitic currents below the channel region as can be seen from figures 4a and 4b where we show the charge and current density respectively along the depth (x direction) of the device at the middle of the gate at V_D=1V. Two curves are shown on each diagram, one for V_G=2V and another for V_G=1V. We observe in figure 4a that for V_G=1V a tail below the depth x=15nm appears (the channel is between 10 and 15nm) which gives a parasitic current below the channel as it is seen figure 4b. In fact this parasitic current at V_G=1V does not decay fast with depth which is the reason why in the I_D-V_G characteristics an increasingly higher depth of the domain of simulation is needed for good accuracy as V_G decreases. The obvious explanation of this is that at low V_G the gate is not able to "lift" the electrons from the dopants in the supply layer (below the channel). This disadvantage of this device has been corrected in subsequent work by these authors by the addition of AlAsSb (high band-gap) layers above and below the channel layer [9-10].

We now turn our attention to the Lg=30nm device described in [8]. The I_D-V_G characteristics of this device together with our simulation are shown in figure 5. A representative transconductance curve for the linear regime, i.e. V_D=0.05V, is shown in figure 5a. It can be seen that good agreement with the experimental results is obtained but this time however we have employed the fitting of u_{sat} described in the Method section. Note that no such fitting was employed for the long gate device. The transconductance curve for the saturation regime is shown in figure 5b. Here however

the agreement is much better. This difference we attribute to the more difficult convergence at smaller currents occurring at small V_D. The same commented can be made about the previous long-gate device. It should be obvious that this nanometric device exhibits a much faster turn on compared to the previous one. This is due in fact to the absence of any parasitic charge below the channel. The charge density and the longitudinal current along the depth of the device at the mid-point of the gate are shown in figure 6.a and 6.b respectively for V_D=0.5V. It should be clear that no charge or current density is observed below the x=80nm mark. We remind the reader that the channel is between x=70nm and x=80nm for this device.

At this point the question arises as to the different behavior of the two devices studied in this paper. It is worthwhile pointing that, usually, the shrinking of the length of the channel decreases the SS as the gate loses control over the channel. However, in this case, the improvement in SS in the short-gate FET is due to the disappearance of the leakage current below the channel. Given that the supply and channel layer materials are the same in both long and short gate FETs one may wonder why should there be a leakage in the long-gate FET and not in the short-gate one. The answer lies in two factors: a) the dopants of the supply layer in the long-gate FET are positioned immediately below the channel layer whereas the in the short-gate FET they are positioned 10nm away from the channel /supply interface and b) the doping level in the long-gate FET is an order of magnitude greater that the short-gate FET.

Conclusions

We have shown that the Poisson-Schrödinger-Continuity calculations may be extended to apply for multi-layer nanometric-gate QW FETs by altering one

parameter, the saturation velocity at high gate voltages V_G but keeping it constant- once changed- at all V_G. Then valuable information for the design of the QW FET is obtained that is normally not available in present quantum mechanical calculations that consist of one layer due to numerical limitations.

Figure Captions

Figure 1: Cross Section of the experimental devices examined in our paper. The domain of simulation for each device is shown by the black dashed lines. a: the long gate device [4], b: the short gate device [8].

Figure 2: Two dimensional charge density of the device of figure 1a at V_G =1V and V_D=1V.

Figure 3: Experimental and Simulated I_d-V_G curves for the long-channel FET [4]:
a) V_D=0.1V. The curve with the squares is the experimental one while the curve with the circles is our simulation.
b) V_D=1V. The two simulations are for two different device depths. The curve with the squares is the experimental one. The curve with triangles is for a depth of device equal to 40nm and the curve with the circles is for a depth of device equal to 250nm.

Figure 4a: The charge density along the depth of the device at the middle of the gate at V_D=1V. The dashed curve is for V_G=1V and the solid curve is for V_G=2V.

Figure 4b: The longitudinal current density along the depth of the device at the middle of the gate at V_D=1V. The thick curve is for V_G=1V and the thin curve is for V_G=2V.

Figure 5: Experimental and Simulated I_D-V_G curves for the short - channel FET [8]. The curve with the squares is the experimental one and the curve with circles is our simulation. The linear regime is shown in figure (a) and the saturation in (b).

Figure 6a: The charge density along the depth of the device at the mid-point of the gate at V_D=0.5V. The dashed curve is for V_G=1V and the solid curve is for V_G=2V.

Figure 6b: The longitudinal current along the depth of the device at the mid-point of the gate at V_D=0.5V. The thick curve is for V_G=1V and the thin curve is for V_G=2V.

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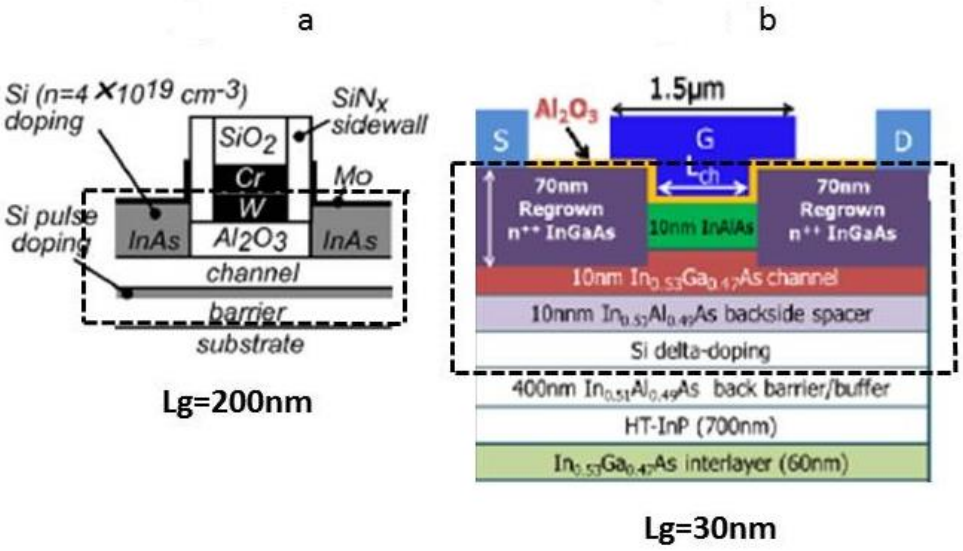

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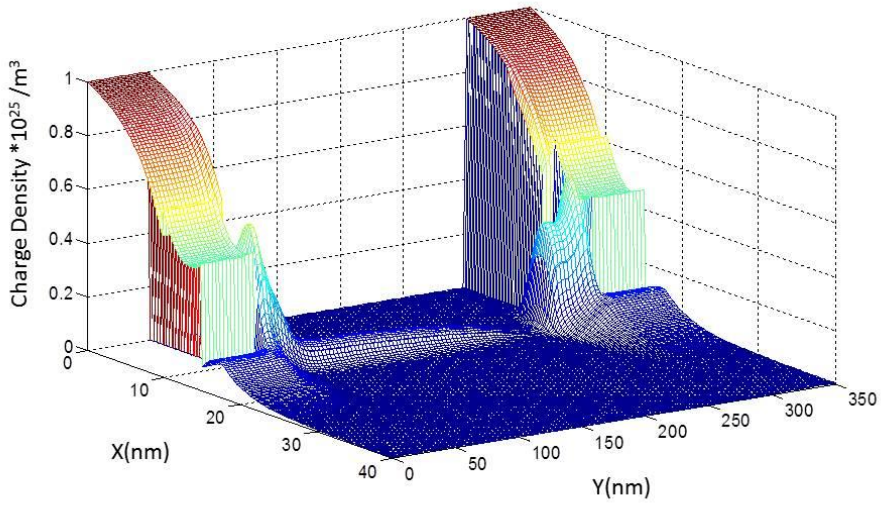
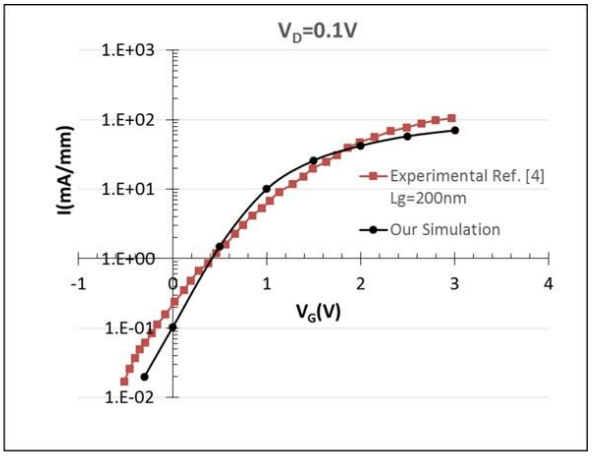


Figure 2.

Figure 3.a



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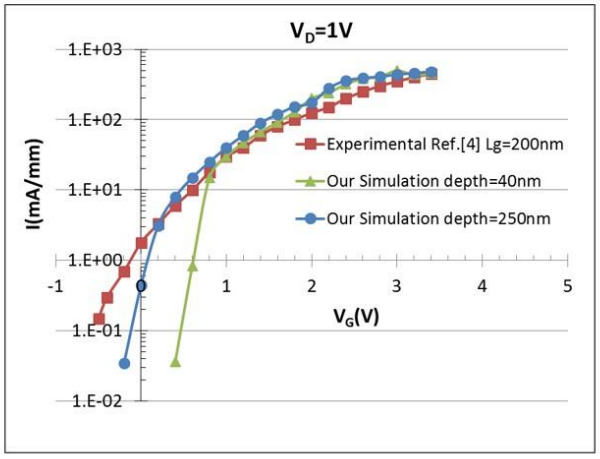

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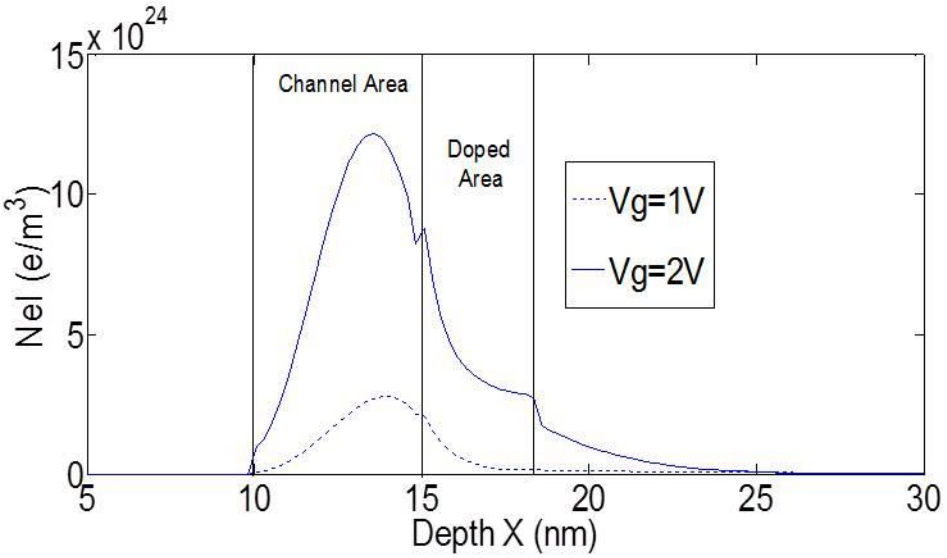


Figure 4a.

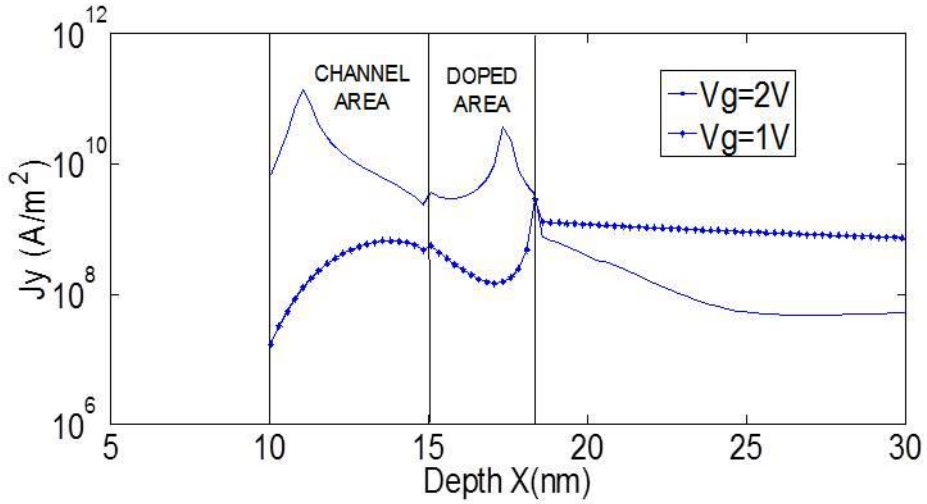
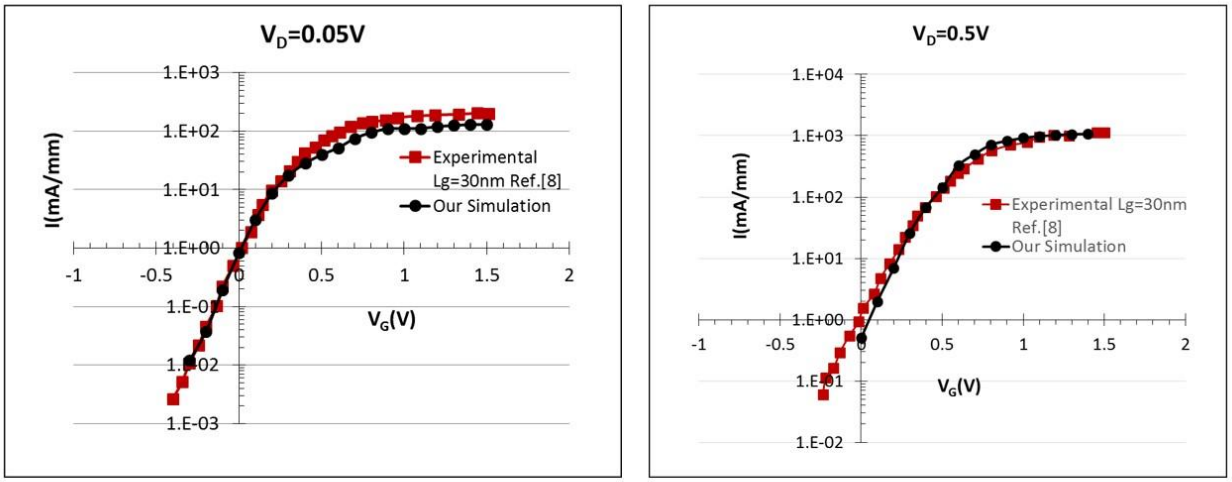


Figure 4b.

Figure 5.a

Figure 5.b



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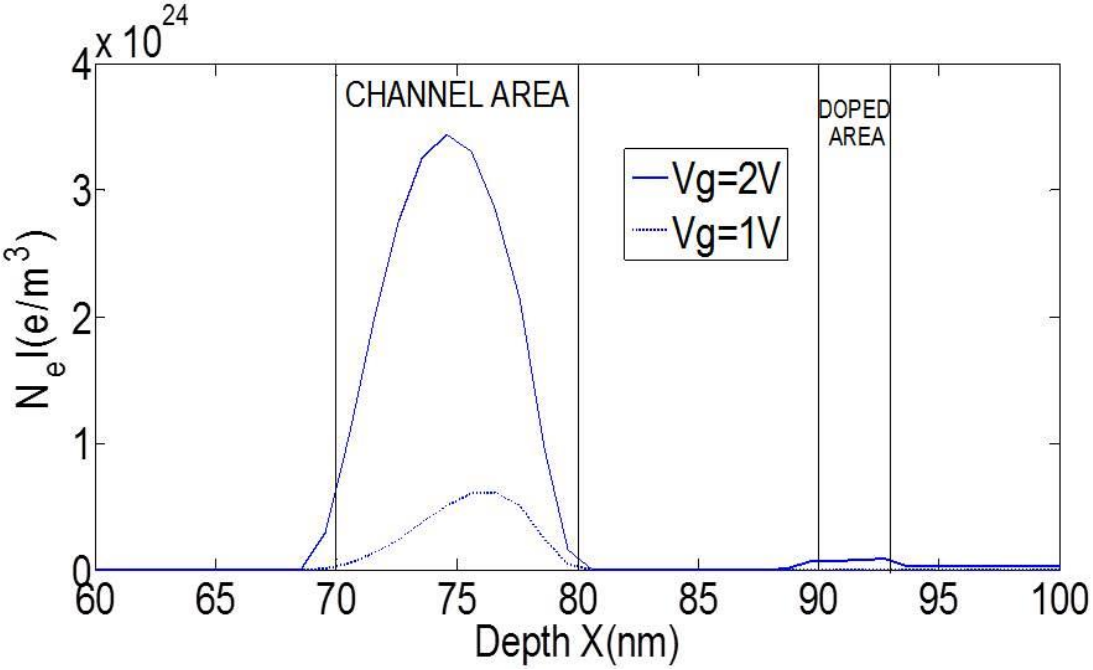

Figure 6a.

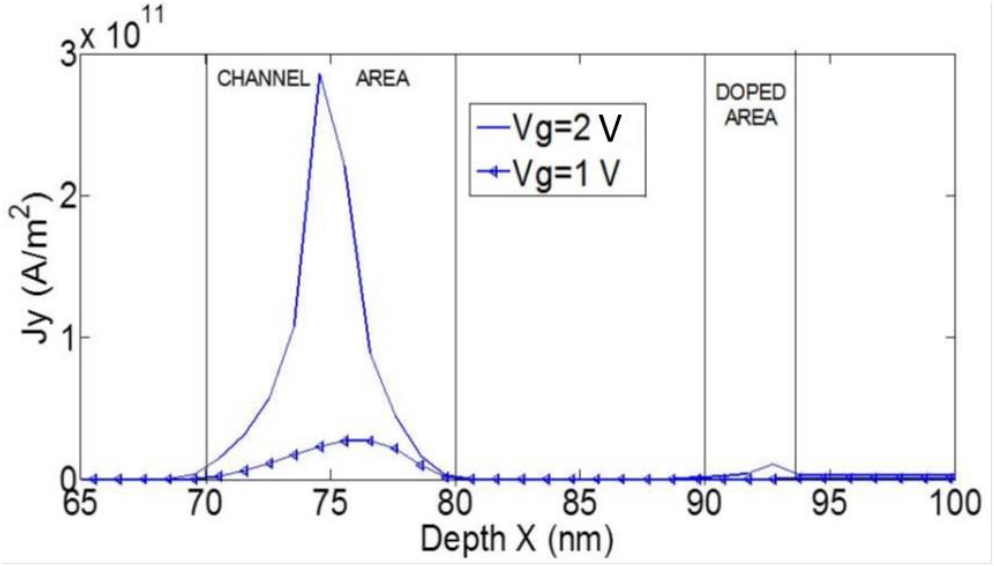

Figure 6b.