A capacitance-to-digits readout circuit for an integrated humidity sensor for monitoring the in-package humidity of ultra-small medical implants

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***Abstract*—Integrated humidity sensors, especially the capacitive type, are increasingly used for implanted electronic devices for assessing the hermeticity of implant packages and monitoring the in-package environment in which delicate electronics are operating. We have developed a simple capacitance-to-digits readout circuit for a capacitive humidity sensor that is used for monitoring the in-package humidity of ultra-small medical implants. The proposed readout circuit provides a larger dynamic range than conventional capacitance readout circuits by removing the parasitic capacitance from the measured capacitive input. Its simple circuit structure and low-power consumption make it suitable for implant applications.**

Keywords— Humdity sensor, implant package, capacitance-to-time converter, capacitance-to-digits readout circuit, hermeticity.

I. INTRODUCTION

Last decade has witnessed the rapid advance of active implanted devices for treating various disabling conditions which cannot be effectively addressed by conventional drugs or surgeries. For example, spinal cord stimulator implants are used for restoring lower limb and upper limb functions [1]; deep brain stimulators are applied for treating Parkinson [2] and epilepsy [3]; implant systems with intra-cortical recording are now used to drive neuroprosthetic arms or help individuals to communicate with the outside world [4]. In contrast to standard consumer electronics, active implanted devices are surrounded by body fluid for many years. If the moisture penetrates an implant package and the humidity inside the implant package starts to build up, the implant may stop working and it may cause detrimental effect to the neural system. For example, condensation may bridge unintended circuit paths, causing short circuit [5] and toxic metal ions, such as Cu+, may be released to the neural system during the corrosion process [6]. This is why active implanted devices are designed to last longer than their intended operational time or they should outlast the lifetime expectancy of the patient.

Conventional implant packages, such as ceramic package and wielded metal packages using titanium alloy [7], have a proven track record in hermetically seal electronics for many years and they have been used in commercial implants, such as pacemakers and cochlear implants. The hermeticity of such packages is usually tested by a method called gas leak test in which the implant package under test is filled with inertial gas, such as helium. If the implant package is not hermetical, it will leave a fine trace of helium which can then be detected by sensors outside the implant package. However, the gas leak test only works for those implants with an inner cavity bigger than 50 mm^3 [8]. There is currently a great drive to push individual implanted devices to the millimeter scale so they can form an intra-body network [9] or can be distributed as dusts for electrophysiological neural recording [10]. However, such ultra-small implanted devices with inner cavities of a few mm^3 or even sub-mm^3 mean that the conventional packaging methods will either not work or become too hard to validate. Recently it becomes increasingly popular to use humidity sensors to directly assess the in-package humidity, especially by using integrated humidity sensors [11] as they can be integrated with the rest of implant circuits and bear little overhead to the entire implant size.

Typical integrated humidity sensors are either capacitive or resistive. The former is more popular as it tends to consume less power than the resistive type. Integrated capacitive-type humidity sensors can be implemented by either compatible processes [12] or incompatible processes to standard CMOS [13]. The latter usually offers higher sensitivity to humidity variation at the expense of additional fabrication steps.

II. READOUT CIRCUITS FOR INTEGRATED CAPACTIVE HUMIDITY SENSORS

A. Challenges

Fig. 1a shows a typical capacitive relative humidity (RH) sensor implemented on a Si substrate using interdigitated electrodes covered by a hydrophilic layer. The main sensing capacitance is formed between the interdigitated electrodes,

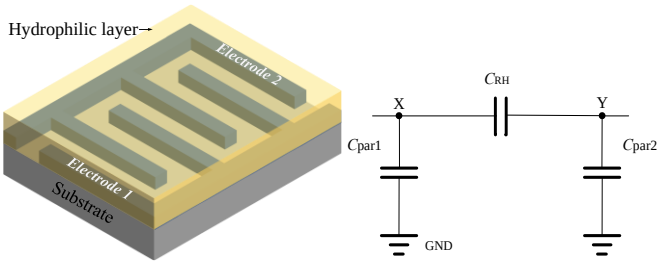

Fig. 1 A capacitive humidity sensor implemented on a Si substrate: (a) the physical structure, (b) the circuit model.

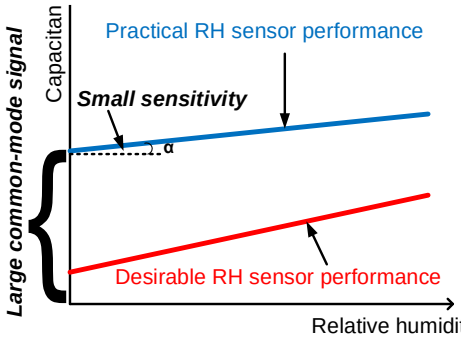

Fig. 2 The design challenges: desirable vs. practical RH sensor performance.

Electrode 1 and Electrode 2. Since the permittivity of the hydrophilic layer varies with the RH, the sensing capacitance is a function of RH. Fig. 1b shows the simplified circuit model for the on-chip capacitive RH sensor. C_{RH} is the sensing capacitor whose capacitance is sensitive to humidity while C_{par1} and C_{par2}, are the parasitic capacitance associated with the two terminals of C_{RH}. C_{par1} and C_{par2} are lumped parasitic capacitance coming from the substrate, input of the readout circuit and nearby circuits. If C_{RH} is probed directly by off-chip apparatus, capacitance from the IO pads and measurement probes will also be added to C_{par1} and C_{par2}. Since C_{RH}, C_{par1} and C_{par2} are all strongly dependent on the sensor area on the horizontal plane, their values are often comparable. Since C_{par1} and C_{par2} are physically further away from the hydrophilic layer than C_{RH}, they are less sensitive to the humidity variation. Thus, the presence of parasitic capacitance reduces the sensitivity of the humidity sensor to the RH and adds a large common-mode signal which limits the dynamic range of the RH sensor, as illustrated in Fig. 2.

B. Existing readout circuits to capacitive sensors

The readout circuits to capacitive RH sensors can be classified as capacitance-to-voltage (C2V) [14], capacitance-to-frequency (C2F) [15] and capacitance-to-time (C2T) transducers [16], all of which are based on charging and discharging C_{RH}. To reject the large common-mode signal (see Fig. 2), differential sensing which measures the C_{RH} against a reference capacitance, C_{REF}, is popular. C_{REF} is typically having the same physical pattern as C_{RH}, but is isolated from the humid environment. Hence C_{REF} is more or less constant at different RHs. However, C_{REF} leads to complex manufacturing process as it needs to be isolated from the humid sensor and increases the size of the entire sensor.

C. Proposed readout circuit for parasitics cancellation

The C2V and C2F tend to offer faster measurement speed than C2T. However, the humidity inside an implant package is unlikely to change significantly in hours, or even in days. Therefore we have chosen C2T for measuring capacitive RH sensors, trading the measurement time for accuracy. Another advantage of the C2T transducer is its simplicity in converting analog signals to digital signals. For example, the capacitance-to-digits information can be obtained by counting the number of clock cycles within the counting period. For counting purpose, a reliable and accurate clock signal which itself is stable over various temperature and humidity conditions is needed.

Fig. 3 shows the operating principle of the proposed readout circuit based on the C2T principle. There are five switches S_0~S_4 in the circuit to control the charging and discharging for C_{RH}, C_{par1} and C_{par2}. Its operation consists of four main phases.

Phase 1 (Reset phase): S_0 is off while S_1 - S_4 are on. Residual charge on all capacitors is removed.

Phase 2 (Pre-charge phase): S_0 - S_2 are on while S_3 and S_4 are off. C_{par1} and C_{pas2} are charged until V_X and V_Y in Fig. 3 reaches a pre-defined voltage level, V_{REF}. All switches are designed to have very small *ON* resistance. Hence, the voltage across the switches is negligible.

Phase 3 (Parasitic elimination phase): S_0, S_1, S_2 and S_3 are off while S_4 is on. C_{par2} is discharged. At the end of this phase, V_Y returns to 0 and the charge which was on C_{par1} from the pre-charge phase is now shared between C_{RH} and C_{par1} with

$$V_X = \frac{C_{par1}V_{REF}}{C_{par1}+C_{RH}} \quad (1)$$

The net charge at the Node *X* at the end of the Phase 3 is

$$Q_{Phase3} = C_{par1}V_{REF} \quad (2)$$

Phase 4 (Measurement phase): S_0, S_1 and S_4 are on while S_2 and S_3 are off. I_{charge} continues to charge C_{par1} and C_{RH} until V_X comes back to V_{REF}. The net charge at the Node *X* at the end of the Phase 4 is

$$Q_{Phase4} = (C_{par1} + C_{RH})V_{REF} \quad (3)$$

If the duration of the Phase 4 is denoted as t_{meas},

$$t_{meas} = \frac{Q_{Phase4}-Q_{Phase3}}{I_{charge}} = \frac{C_{RH}V_{REF}}{I_{charge}} \quad (4)$$

Hence if V_{REF} and I_{charge} are predetermined, t_{meas} will be linearly proportional to C_{RH}, independent of C_{par1} and C_{par2}. If t_{meas} is measured by a counter against a known frequency, f_{REF}, the number of counts, *N*, bears the relative humidity information.

$$N = t_{meas}f_{REF} \quad (5)$$

III. CIRCUIT DESIGN

We are interested in designing a readout circuit which can detect small capacitance change of integrated capacitive humidity sensor and provide reasonably good resolution, i.e., in 1%RH. For example, we have designed an integrated CMOS-compatible humidity sensor in [11], its capacitance can be modelled as

$$C_{RH} = C_0(1 + \alpha \cdot \Delta RH) \quad (6)$$

where C_0=21.54pF is the sensor capacitance at 0%RH and α= 0.04% is the normalized sensitivity per 1%RH. C_{par1} and C_{par2} have been modelled in COMSOL Multiphysics and are 17.09pF each. The sensor was implemented using the top metal layer of XFAB's XC06 process and measured 2x2 mm^2. Assuming the sensor capacitance is linear to relative humidity, to achieve 1% resolution in measuring RH, the following condition needs to be met

$$N_{100\%RH} - N_{0\%RH} \geq 100 \quad (7)$$

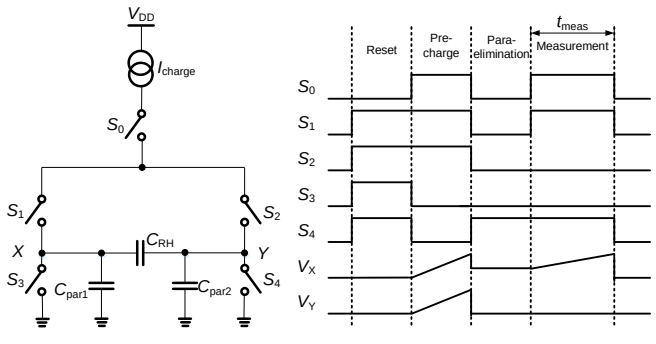

Fig. 3 The proposed readout circuit: (a) the circuit diagram; (b) control signals and expected voltage waveforms at key nodes.

where $N_{100\%RH}$ and $N_{0\%RH}$ are the counter output at RH=100% and RH=0%, respectively.

Combining (4), (5), (6) and (7), we get

$$\frac{100\alpha C_0 \cdot V_{REF}}{I_{charge}} f_{REF} \geq 100 \quad (8)$$

By having a large V_{REF}, I_{charge} can be kept small, leading to low power consumption. For V_{REF}=4.5V and f_{REF}=13.56MHz, I_{charge}≤526nA. For the actual design, we chose I_{charge}=500nA. To minimize the temperature impact on the sensor output, V_{REF} and I_{charge} are designed to achieve very small temperature coefficient (TC). Temperature-insensitive V_{REF} and I_{charge} are useful as: i) although the implant temperature is expected to be stable in general, it may still be subject to small temperature variations, such as due to high or low body temperature at certain conditions and self-heating of the implant device; ii) an implant device is likely to be exposed to high temperature cycles during the manufacturing, testing and characterization.

Fig. 4 shows the reference generator circuit modified from [17]. It provides the temperature-insensitive V_{REF} and I_{charge}. The start-up circuits are not shown for simplicity. Q_1 and Q_2 are parasitic BJTs available in most CMOS processes. M_1 ~ M_4, and M_5, M_6, M_{10} and M_{11} are cascode current mirrors which suppress the channel-length modulation, making currents in Q_1 and Q_2 identical. Both I_{Q1} and I_{Q2} show a positive TC and they are complemented by currents with negative TC in R_2 and R_3, respectively.

$$I_{ptat} = \frac{\mathrm{n}V_T \cdot ln\mathrm{H}}{R_1} \quad (9)$$

where $\frac{(W/L)_{M6}}{(W/L)_{M5}} = \mathrm{n}$, V_T is the thermal voltage, the size of Q_1 is H times of Q_2. Since $V_T = \frac{kT}{q}$ where k is the Boltzman Constant, T is the temperature and q is the charge of an electron, I_{ptat} has a positive TC. The currents through R_2 and R_3 are the same and

$$I_{ctat} = \frac{V_{BE2}}{R_3} \quad (10)$$

where V_{BE2} is the emitter voltage of Q_2. Since V_{BE2} has a negative TC and R_3 was implemented by low-TC and high-resistivity polysilicon, I_{ctat} has a negative TC. The temperature-insensitive current is

$$I_{stable} = I_{ptat} + I_{ctat} \quad (11)$$

TABLE I. CORNERS

	C_{RH}	V_{REF}	I_{charge}	N
Typical	C_{typ}	V_{typ}	I_{typ}	$\mathbf{N_{typ}}$
Corner 1	115%×C_{typ}	105%×V_{typ}	85%×I_{typ}	**1.42N_{typ}**
Corner 2	115%×C_{typ}	105%×V_{typ}	115%×I_{typ}	**1.05N_{typ}**
Corner 3	115%×C_{typ}	95%×V_{typ}	85%×I_{typ}	**1.29N_{typ}**
Corner 4	115%×C_{typ}	95%×V_{typ}	115%×I_{typ}	**0.95N_{typ}**
Corner 5	85%×C_{typ}	105%×V_{typ}	85%×I_{typ}	**1.05N_{typ}**
Corner 6	85%×C_{typ}	105%×V_{typ}	115%×I_{typ}	**0.78N_{typ}**
Corner 7	85%×C_{typ}	95%×V_{typ}	85%×I_{typ}	**0.95N_{typ}**
Corner 8	85%×C_{typ}	95%×V_{typ}	115%×I_{typ}	**0.70N_{typ}**

Ignoring the TC of resistors as they are implemented by polysilicon with extremely low TC, the temperature behavior of I_{stable} is

$$\frac{\partial I_{stable}}{\partial T} = \frac{1}{R_1}\left(\mathrm{n}\frac{k}{q} ln\mathrm{H} + \frac{\partial V_{\mathrm{BE2}}}{\partial T}\frac{1}{\mathrm{M}}\right) \quad (12)$$

where R_2=R_3=M·R_1. For a zero TC, we chose n=1, H=5, M=15.25. The temperature-insensitive voltage

$$V_{REF} = I_{stable} R_4 \quad (13)$$

Combining (9), (10), (11) and (13), we get

$$V_{REF} = \mathrm{L}\left(\mathrm{n}V_T ln\mathrm{H} + \frac{V_{BE2}}{\mathrm{M}}\right) \quad (14)$$

where R_4=LR_1. As shown in (11), I_{stable} depends on the exact resistance of R_1 which is difficult to control. Hence I_{stable} is subject to large variations due to process variations. In contrast, V_{REF} is independent of R_1 and its value is mainly dictated by the relative ratios. Hence V_{REF} is subject to transistors and resistors mismatches. It is reasonable to assume that a good layout practice will be able to confine the 3σ values of I_{stable} and V_{REF} within the ±15% and ±5% of the nominal values, respectively.

Table I lists the corners when C_{RH}, V_{REF} and I_{charge} are at either maximum or minimum values. The two worst-case corners lead to the maximum and minimum counter output to 1.42N_{typ} and 0.70N_{typ}, respectively. Corners can be compensated by the 5-bit trim current in Fig. 4.

$$I_{trim} = (D_4 \times 16 + D_3 \times 8 + D_2 \times 4 + D_1 \times 2 + D_0) I_{LSB} \quad (15)$$

where I_{LSB} is the unity current through M_{24}. By default, D_4 ~ D_0 is set to 01101 and the trim current can be either increased or decreased for compensating for mismatches and process variations.

There is no need to have a dedicate on-chip clock generator for the counter as an accurate clock signal can be easily demodulated from the data and power carrier for the inductive

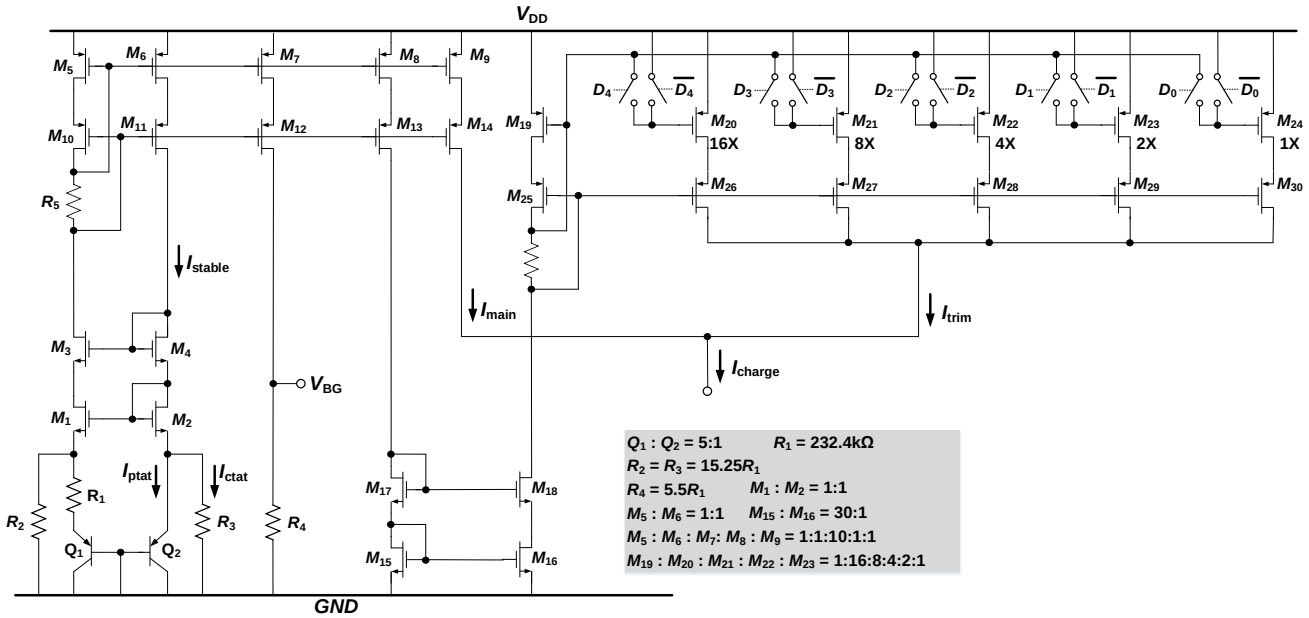

Fig. 4 The reference generator circuit which provides V_{REF} and I_{charge}.

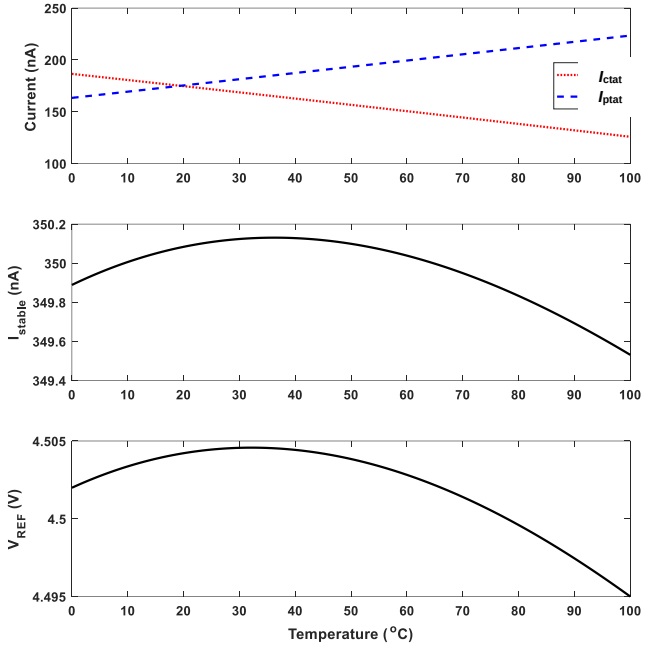

Fig. 5 The temperature performance of I_{ptat}, I_{ctat}, I_{stable} and V_{REF}.

link to the implant [18]. In this design, we used f_{REF}=13.56MHz as it is the approved medical frequency for wireless implants.

Switches in Fig. 3 are designed with dummy switches to minimize the charge injection.

IV. SIMULATION RESULT

The proposed readout circuit was simulated in the Cadence ADE environment using XFAB's 0.6µm CMOS process.

Fig. 5 shows the temperature performance of I_{ptat}, I_{ctat}, I_{stable} and V_{REF}. The maximum TC in the 0 ~ 100°C range for I_{ptat}, I_{ctat}, I_{stable} and V_{REF} are 607pA/°C, -625pA/°C, -16.9pA/°C, and -258µV/°C, respectively.

Fig. 6 shows the operation of the proposed readout circuit when the RH is 30%. It took 196µs to complete the measurement phase, which corresponds to a counter output of 2653.

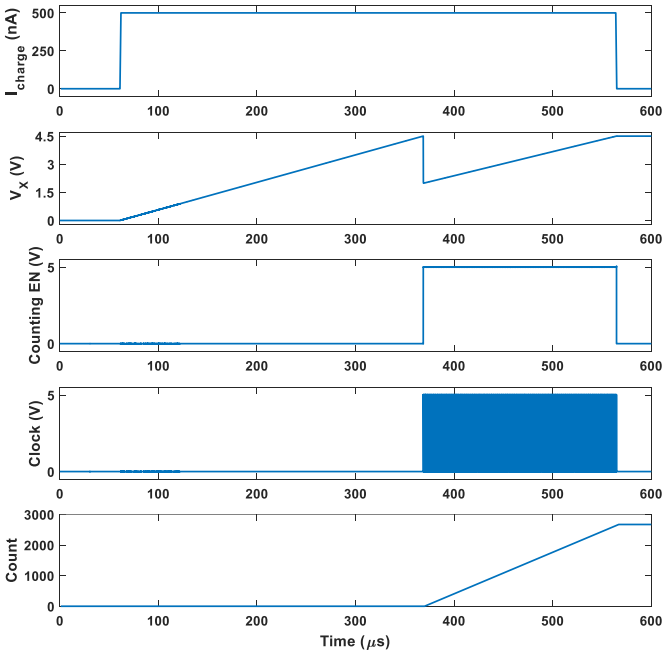

Fig. 6 The simulation result of the readout circuit.

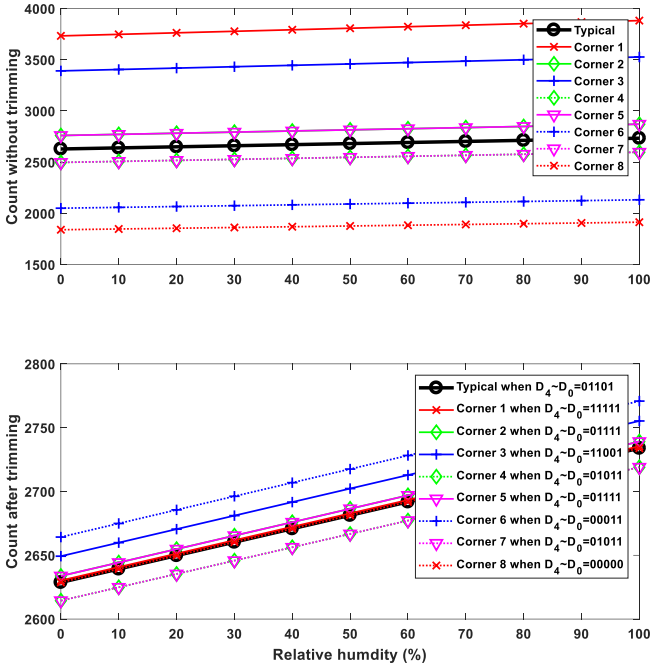

Fig. 7 (a) Top: Counter output at various corners without compensation; (b) Bottom: Counter output at various corners with compensation.

Fig. 7(a) shows that large spreads of the sensor output, i.e., the count, at various corners. Fig. 7(b) shows the compensated counter output which are close to the desirable value ('Typical' in the figure).

V. CONCLUSIONS

We presented a simple readout circuit suitable for integrated capacitive RH sensors which tend to suffer from large common-mode capacitance, low sensitivity to RH and large parasitic capacitance. It does not need a dedicated on-chip reference clock for analog to digital conversion as an accurate clock can easily be recovered from the carrier which is used for sending wireless power and data to the implant.

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