A Microchannel Neural Interface ASIC

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***Abstract*—This paper presents an application specific integrated circuit (ASIC) for use in a three-dimensional microchannel neural interface. The device is assembled with seven stacked ASICs with silicone microchannels instrumented in between. Each ASIC comprises tripolar electrodes for seven channels allowing recording or stimulation from any one of the 49 microchannels. The ASIC is implemented in 0.35-µm high-voltage CMOS technology and occupies an active area of 4 mm². The device has been tested demonstrating recording of 1 mV signals, and current controlled stimulation in the range of 5 µA to 500 µA (with 40 V compliance) and up to 50 kHz stimulation frequency. The device overcomes limits on numbers of connected microchannels in previous designs.**

***Keywords*—Bioelectronics, electrodes, microchannels, neural interfaces.**

I. Introduction

Upper limb amputees report dissatisfaction with current commercial prostheses [1]. Complaints include limited degrees of freedom and unintuitive control [2]. Interfacing with residual peripheral nerves may make intuitive control of amputation prostheses possible [3]. Many devices for recording from and stimulating the peripheral nervous system have been investigated [4], and one key approach to re-establishing intuitive sensory and motor function is using highly selective neural interfaces [5]. The challenges for such neural interfaces include the interference between channels during multi-channel stimulation, the small magnitude of the extracellular action potential in fragile, dynamic environment, and the signal stability often degraded by scar tissue and fibrosis formed around the electrodes.

Microchannel neural interfaces (MNIs) are one solution to providing a highly selective interface with the nervous system. MNI design helps overcome some of the challenges of nerve interfaces, including low signal amplitude and cross-talk [6]. MNIs comprise an array of small diameter microchannels (typically ø < 200 µm and up to 5 mm in length) into which peripheral nerve axons are placed or encouraged to regenerate. The electrically insulating microchannel acts to: increase signal amplitude by restricting the extracellular space [7]; reduce cross-talk by physically separating axons; increase the length of axon from which signals can be recorded, making recordings independent of node of Ranvier position; amplify the magnitude of the action potential by the narrow channel; and reduce the required stimulus currents. Evidence from *in-vivo* results also suggests minimal fibrosis and inflammation [7]-[9]. Selectivity in MNI devices partly depends upon the number of microchannels. To achieve high numbers of channels, MNIs have been manufactured in three-dimensions (3D) by several methods [6], [8], [9].

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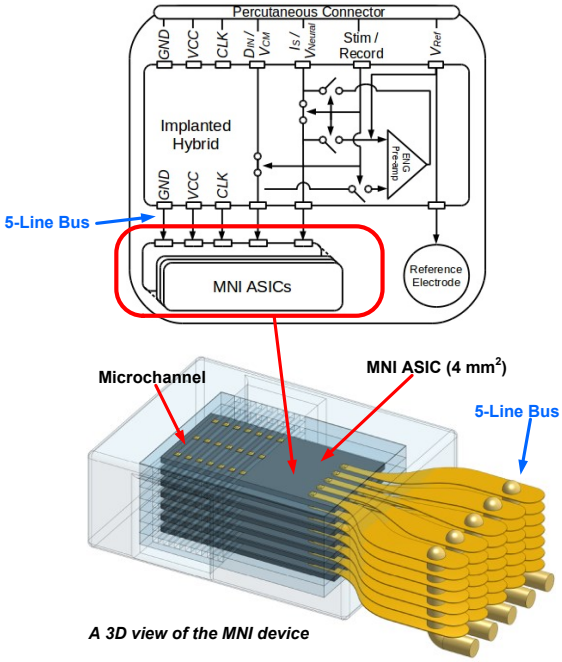

Figure 1. Overall architecture of the MNI implant.

To date MNIs have used passive conductors within the microchannel array, which sets a limit on the number of channels, since each channel will require at least one connecting wire. We propose to use ASICs in place of passive conductors to significantly reduce the number of connections required by multiplexing electrode sites. This paper describes the MNI ASIC developed comprising on-chip electrodes, formed from the standard bonding pads, for seven microchannel arrays and the associated multiplexing circuits. Multiple ASICs are used to construct a MNI device with 49 microchannels providing interface to 49 possible axon bundles. This is a significant increase in the number of channels despite the fact that the number of connecting wires is reduced to a 5-line bus. Circuit design and device fabrication procedures are described.

II. System and ASIC Architecture

A. Overall System

The system architecture is shown in Fig. 1 alongside a 3D view of the final MNI device, where seven MNI ASICs are

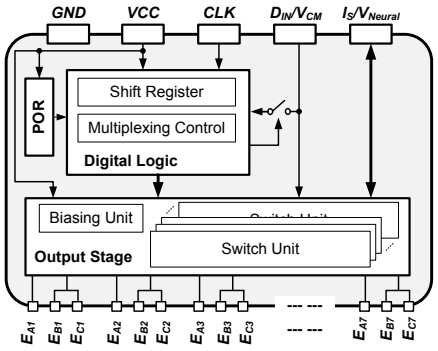

Figure 2. System diagram of the MNI ASIC.

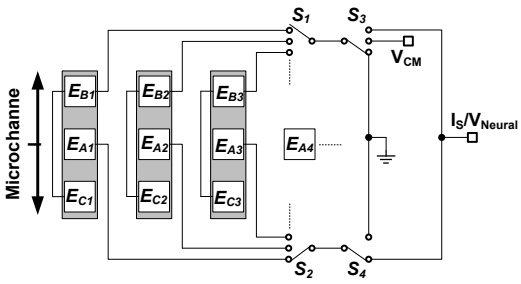

Figure 3. Illustration of the electrode multiplexing.

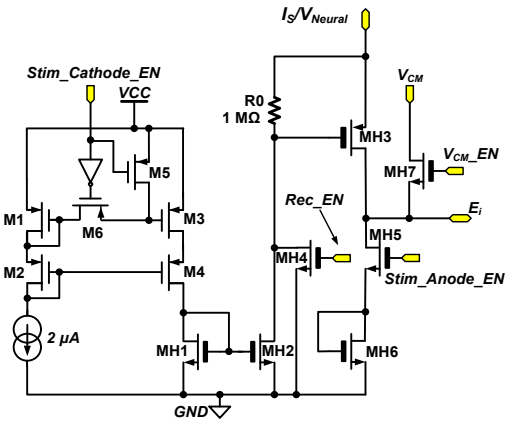

Figure 4. Schematic of the switch unit.

stacked with a silicone layer in between. Each ASIC consists of seven tripolar electrode arrays, upon which seven microchannels are formed. The ASICs provide bidirectional multiplexing to each microchannel, and are powered and controlled by an implanted hybrid via a 5-line parallel bus. During stimulation, the hybrid provides a dc stimulation current, I_S, to the MNI, where I_S is converted into biphasic pulses by the switching activities in the MNI. During recording, the hybrid amplifies the received action potentials from the MNI by its built-in ENG preamplifier before forwarding the signals to the external controller. The hybrid connects to an external controller (not shown) via a percutaneous connector where commands are sent at a rate between 35 kbit/s and 1.1 Mbit/s. Switching from stimulation to recording reroutes lines I_S/V_{Neural} and D_{IN}/V_{CM} to the inputs of the differential amplifier in the hybrid. Seven MNI ASICs are arranged in parallel with the 5-line parallel bus (*GND, VCC, CLK,* D_{IN}/V_{CM}, I_S/V_{Neural}). During recording a remote reference electrode and I_S/V_{Neural} are biased to V_{Ref} = 1.65 V (midpoint of *VCC* at 3.3 V); the reference electrode acts to bias D_{IN}/V_{CM}.

B. ASIC Design

1) ASIC Architecture: The system diagram of the MNI ASIC is shown in Fig. 2. Each ASIC is connected to the 5-line parallel bus through five pads, where D_{IN}/V_{CM} is used as both the data input, and the output for the common reference voltage, V_{CM}, for recording. Another shared pad, I_S/V_{Neural}, is used as current input during stimulation and neural signal output during recording. When powered up, an on-chip power-on-reset (POR) unit sets D_{IN}/V_{CM} as the data input and disconnects all electrodes. Commands coming in from the data communication pads, *CLK* and D_{IN}, are shifted into the digital logic where the multiplexing control activates the switch units in the output stage to connect the electrodes in the specified microchannels for either stimulation or recording.

2) Multiplexing Control: Each microchannel on the MNI ASIC comprises three electrode pads: E_{Ai}, E_{Bi} and E_{Ci}, arranged in a tripole, where E_{Ai} is located at the centre of the microchannel, and E_{Bi} and E_{Ci} on both sides at an equal pitch, as shown in Fig. 3. E_{Bi} and E_{Ci} are connected together to reduce inter-channel interference. The multiplexing operates in three modes: stimulation, recording and channel leak test. In the stimulation mode, one microchannel is activated at a time with the inner electrode E_{Ai} and the outer electrodes E_{Bi}/E_{Ci} switching alternately between the input current I_S and *GND*, to create biphasic stimulus pulses. In the recording mode, the activation is also one microchannel at a time with E_{Ai} connected to the output, V_{Neural}, and the outer electrodes to the common voltage output, V_{CM}, with the connection between the D_{IN}/V_{CM} pad and the digital logic turned off. Both V_{Neural} and V_{CM} are biased to 1.65 V and lead to the amplifier inputs in the hybrid. To exit the recording mode, a POR is needed to restore the connection between D_{IN}/V_{CM} and the logic. In the channel leak test mode, two adjacent channels are activated at a time, with (E_{Ai}, E_{Bi}, E_{Ci}) connected to I_S and (E_{Ai+1}, E_{Bi+1}, E_{Ci+1}) to *GND*. This mode is for testing current leakage between the microchannels after the MNI assembly. Multiplexing is commanded by data frames via the communication pads.

3) Output Stage: The output stage consists of a biasing unit and 14 identical switch units (7 for E_{Ai}, 7 for E_{Bi} and E_{Ci}) for flexible channel multiplexing. The schematic of the switch unit is shown in Fig. 4. Four control signals operate a switch network to connect the electrode pad, E_i, to either I_S or *GND* in the stimulation and channel leak test modes, or to either V_{Neural} or V_{CM} in the recording mode. The switches are implemented with high voltage MOSFETs in AMS HV 0.35-µm CMOS technology. In the stimulation mode, high compliance voltage (≤ 40 V) may be required at I_S due to the high impedance in a microchannel. As a result, conventional complementary CMOS switches are not suitable because the maximum allowed gate-source voltage is only 18 V for these HV MOSFETs. To ensure the safety of the transistors, a current-biased level shifter is implemented [10]. As shown in Fig. 4, once E_i to this switch unit is specified as a cathode for stimulation, the control signal *Stim_Cathode_EN* turns on transistor M3 allowing a current of

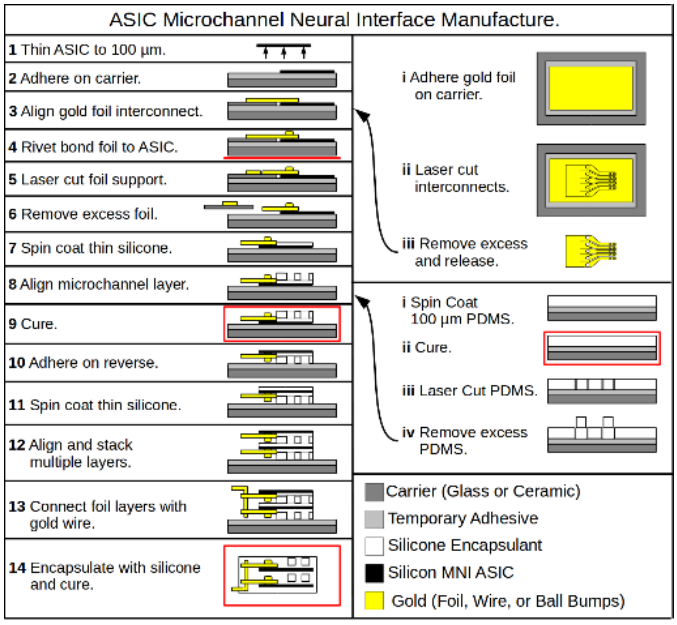

Figure 5. MNI manufacture from stacked MNI ASICs.

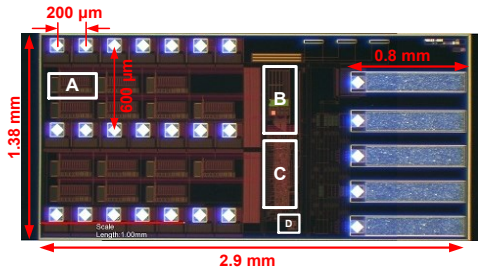

Figure 6. Die microphotograph of the MNI ASIC, including 14 identical switch unit (A), the biasing unit (B), the digital logic (C), the POR (D), five connecting pads and 21 electrode pads for 7 microchannels.

2 µA to pass through MH2, which generates a 2 V drop across R0, thus MH3 is safely turned on. If E_i is specified as an anode, MH5 is turned on by *Stim_Anode_EN* to allow the stimulation current to flow to *GND*. In the recording mode, both MH2 and MH5 are turned off. For the switch unit to the inner electrodes, since the voltage at V_{Neural} is biased at the midpoint of the 3.3 V supply, MH3 is directly turned on by connecting its gate to *GND* through MH4. For the outer electrodes, both MH3 and MH4 are turned off, and the electrodes are connected to V_{CM} through MH7. The biasing unit generates a 2 µA bias current for each of the switch units.

C. Stacked Microchannel ASIC Assembly

The complete MNI is assembled following a method used previously for passive conductors [8], [11]. The details of the procedure are summarized in Fig. 5. In general, the ASICs were first thinned to 100 µm and attached to a carrier where the electrode pads was electroplated with gold, and laser-cut gold foil ribbons were rivet bonded to the five connection pads. The ASICs were then silicone encapsulated by spin coating with the electrode pads exposed. A silicone microchannel layer was formed by laser-cutting 100 µm PDMS on a carrier. After removing excess PDMS, the microchannel layer was aligned

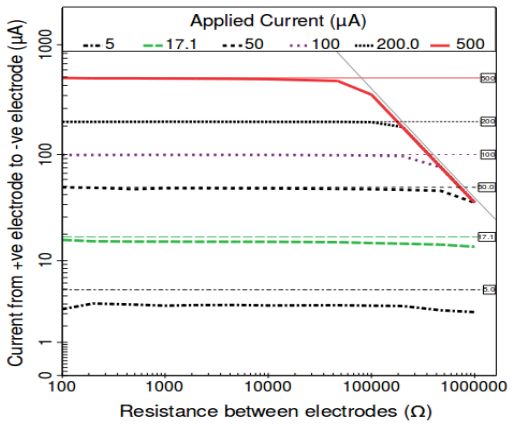

Figure 7. Current controlled stimulation. The observed current (µA) between the cathode and anode during stimulation with a range of resistances between the electrodes (discounting saturation due to the 40 V voltage limit imposed).

with a MNI

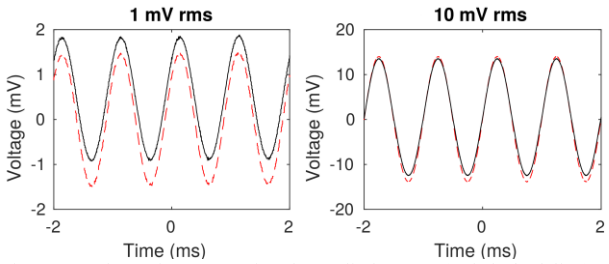

Figure 8. 1 kHz sine wave signals applied at E_{Ai} (red dashed line) and recorded at I_s/V_{Neural} (black line).

to the ASIC and bonded. After curing, the bottom side of the MNI ASIC was also coated with thin silicone. By repeating this process, multiple layers of microchannels can be formed, as shown in steps 1 – 12 in Fig. 5. Once the desired number of layers were achieved, vertical interconnections were formed between the gold foil ribbons using wire to form a vertical parallel bus, and then the MNI was silicone encapsulated to insulate the 5 connection lines, as shown in steps 13 – 14. The red rectangle in Fig. 5 indicates a curing temperature of 150 °C.

III. Measurements

The prototype ASIC is implemented in the AMS 0.35 µm high-voltage CMOS technology (H35B4D3). Fig. 6 shows the microphotograph of the ASIC. The total size of the die is 2.9 mm × 1.38 mm, including a length of 0.8 mm for the five extended connection pads. Seven microchannels are fabricated on the ASIC with three electrode pads per channel in a pitch of 600 µm. The size of each electrode pad is 94 µm × 94 µm. The pitch between adjacent microchannels is 200 µm. A comparison with other chip designs for active electrodes is shown in Table I.

A. Power Consumption

The power consumption of a single MNI ASIC in POR mode is 143 µW (43.3 µA with a 3.3 V supply), where all electrodes are connected to *GND*. When switched to stimulate on one channel (cathodically or anodically), power consumption is 149 µW. When all channels are connected for stimulation power

TABLE I COMPARISON WITH OTHER WORK

Reference	CMOS Process	No. of electrodes	Die area (mm^2)	Electrode density	No. of wires	Compliance voltage (V)	Channel multiplexing	Power consumption
[6]	0.18 µm	5	1.753	2.85 /mm^2	3	up to 25	unidirectional	114 µW
[14]	1.5 µm	8	4.84	1.65 /mm^2	N/A	13	unidirectional	500 µW
[15]	1.5 µm	64	21.16	3.02 /mm^2	2	5	unidirectional	8.25 mW
[16]	0.6 µm	12	27.3	0.44 /mm^2	5	18	unidirectional	30.11 mW
This work	0.35 µm	21	4	5.25 /mm^2	5	up to 40	bidirectional	149.49 µW

consumption is 237 µW, however this mode is not intended for use in practice. The recording and impedance test modes both consume 143 µW; thus power consumption for 7 stacked ASICs for a 49 channel MNI should be 1 mW to 1.1 mW, dependent upon the mode.

B. Stimulation

The setup for nerve stimulation was tested. Current response under direct currents is shown in Fig. 7. The supply voltage was set to 40 V with six different levels of stimulation current at I_S/V_{Neural}. Variable resistors were used as dummy impedance between electrodes in a microchannel. It is shown in Fig. 7 that 1.44±0.55 µA of the current supplied at I_S/V_{Neural} is used to switch on the stimulating circuit and is therefore lost at the electrodes.

C. Recording

The electrodes were biased to V_{Ref} (1.65 V, i.e. VCC/2) using an external bias source. The outer guard electrodes (E_{Bi}/E_{Ci}) were biased by a 10 kΩ bias resistor representing a remote reference electrode, and a 47 kΩ impedance from E_{Ai} to E_{Bi}/E_{Ci} was assumed. I_S/V_{Neural} was also biased to V_{Ref}. 1 kHz sinusoids signals were applied at the electrodes and the outputs at I_S/V_{Neural} and D_{IN}/V_{CM} were recorded, as shown in Fig. 8.

IV. DISCUSSION AND CONCLUSION

An ASIC design suitable for use in MNIs has been presented for stimulation and recording of peripheral nerve action potentials. Currents in the range required for stimulation in microchannels can be achieved with the MNI ASIC. Here, transfer of 1 mVp-p signals through the MNI ASIC has been shown. For use in reversible kilohertz frequency nerve conduction blocking when treating pain and incontinence, biphasic stimulus pulses of 1 kHz to 100 kHz are required [12]. With the current control system a maximum stimulus frequency of 50 kHz is achievable; to achieve a 100 kHz stimulus pulse a data rate in excess of 2 Mbit/s is required.

This ASIC makes possible an MNI comprising 7 layers and a total of 49 addressable microchannels, enabling recording and stimulation from 49 possible axon bundles. This represents an important increase in instrumented channel number over previous designs while reducing the number of connecting wires. Previous designs have electrodes present in up to 20 microchannels [6]. The assembled MNI will be tested on a regenerated nerve to demonstrate that it can both stimulate and record neural activity. In addition, such implant tests will help understand the materials aspects of using integrated circuits in intimate contact with body fluid and what device lifetime may be possible in the absence of a hermetic package [13].

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