Matrix Single Stage Distributed Amplifier Design for Ultra Wideband Application

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***Abstract*—This paper proposes a new amplifier topology, the matrix single stage distributed amplifier (M-SSDA). The amplifier employs only multiplicative gain, hence, potentially offering a higher gain-per-device than both the conventional DA and matrix amplifier. Functionally similar to the cascaded single stage distributed amplifier (C-SSDA), the M-SSDA has advantages in smaller circuit footprint, a potential for lower transmission line losses and better noise performance. A 2-tiered common-emitter (CE) M-SSDA based on a full foundry double heterojunction bipolar transistor (DHBT) model is presented, demonstrating the viability of the proposed design. The S-parameter performance of the proposed circuit is compared with that of a C-SSDA with two gain cells to show the similarity in their gain and bandwidth performance. To further demonstrate the utility of the proposed design concept, a practical 3×1 M-SSDA circuit is presented. In this circuit, improvement in bandwidth performance is achieved by scaling down the inductance on the input and intermediate transmission lines and introducing a high frequency peak on these lines through shunt capacitance. A cascode configuration with negative resistance attenuation compensation is applied in the gain cells to achieve a flat gain profile. Simulations predict a gain of 20dB at 324GHz bandwidth; more than threefold bandwidth improvement compared to the basic CE M-SSDA design.**

***Index Terms*—Distributed amplifier; Matrix amplifier; Single stage distributed amplifier (SSDA); bandwidth extension; transmission line scaling; attenuation compensation; common-emitter; cascode**

I. Introduction

The concept of the matrix amplifier was introduced by Niclas and Pereira in 1987 [1]. It is a multi-tiered distributed amplifier (DA) connected by intermediate transmission line which simultaneously forms the output transmission line of a lower stage and the input transmission line of the stage above it. The amplifier combines the processes of additive and multiplicative amplification in the same module, resulting in higher gain-bandwidth (GBW) performance relative to a conventional DA, which features only additive gain [2]. Furthermore, the matrix amplifier exhibits inherently good reverse isolation over wide bandwidths at reduced footprint [3]. To improve the performance of the matrix DA, techniques such as: applying predesigned low pass filters based on classic linear analogue filter approximation functions, such as Butterworth and Chebyshev, to transmission line synthesis [4]; employing an active feedback cascode topology for GBW optimization [5]; second tier shifting to improve signal propagation [6]; and a matrix DA that features high electron-mobility transistors (HEMTs) on the lower tier and heterojunction bipolar transistors (HBTs) on the tier above [7], have been reported.

This paper proposes the first matrix-single stage distributed amplifier (M-SSDA) circuit. A major merit of the proposed circuit is that it employs multiplicative gain only, such that with an appreciable single-cell gain, a higher overall gain will be achieved than from a multi-staged matrix DA with equal number of gain cells. While possessing a gain mechanism similar to the cascaded single stage distributed amplifier (C-SSDA) [8], [9], the M-SSDA inherits the advantages that the matrix amplifier has over the cascaded DA. These merits are: a smaller circuit footprint and more compactness due to the sharing of intermediate transmission lines (a major advantage in monolithic circuits); potentially lower transmission line losses; and better noise performance [1].

The concept of the M-SSDA is demonstrated with a 3×1 matrix amplifier based on a full foundry double heterojunction bipolar transistor (DHBT) process model, TSC250, by Teledyne Scientific Company [10]. The input line of the SSDAs that make up the tiers of the matrix is designed using the line scaling and capacitive peaking technique to achieve wider bandwidth, with attenuation compensation applied on the output line to achieve overall gain flatness. The proposed design employs heterojunction bipolar transistor (HBT) because they offer higher gains and better linearity and lower $1/f$-noise performance than field effect devices of a similar generation [11], [12], [13], [14].

In this paper, section II describes the fundamental concept of the M-SSDA and presents a comparison between the M-SSDA and C-SSDA, demonstrating the similarity in performance. In Section III, a 3 tiered M-SSDA, optimized for bandwidth and gain flatness is presented. Section IV concludes the paper.

II. Design Concept

The M-SSDA is essentially two or more single stage distributed amplifiers (SSDA) connected by intermediate transmission lines, forming a *m × 1* matrix structure (Fig.1).

Fig. 2 shows the schematic and equivalent circuits of the input, intermediate and output transmission lines of a basic common-emitter (CE) M-SSDA with two tiers. The lines are made up of intrinsic capacitance C_π and C_{ce} and inductive lines L_B, L_{CB} and L_C; with the lines coupled by the transistor

The authors would like to acknowledge the Petroleum Technology Development Fund (PTDF) of Nigeria for sponsoring Temitope Odedeyi's PhD program.

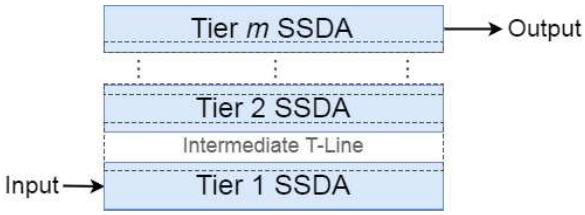


Fig. 1: Structure of M-SSDA

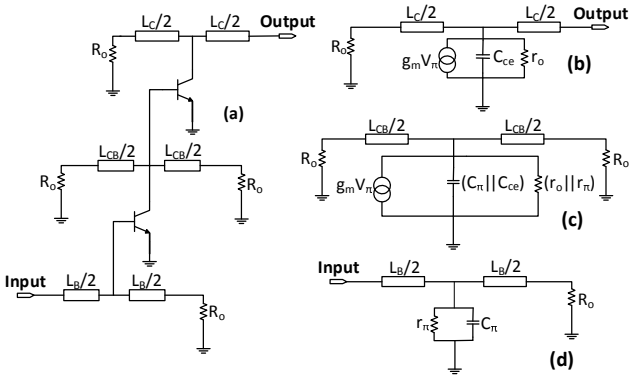


Fig. 2: 2×1 CE HBT M-SSDA (a). Simplified equivalent circuits of: The output (b), Intermediate (c) and Input (d) transmission lines.

transconductance g_m. r_π and r_o are the transistor base-emitter junction resistance and output resistance, respectively and R_o is the terminating resistance.

The gain of a M-SSDA with equal line impedances is given, to a good approximation by

$$Gain = \left(\frac{g_m Z_o}{2}\right)^m, \tag{1}$$

with Z_o being the image impedance of the amplifier transmission lines; and *m,* the number of tiers.

Eqns (2), (3) and (4) describe the line impedances of the input (Z_{in}), intermediate (Z_{int}) and output (Z_{out}) transmission lines, respectively of the simplified CE M-SSDA:

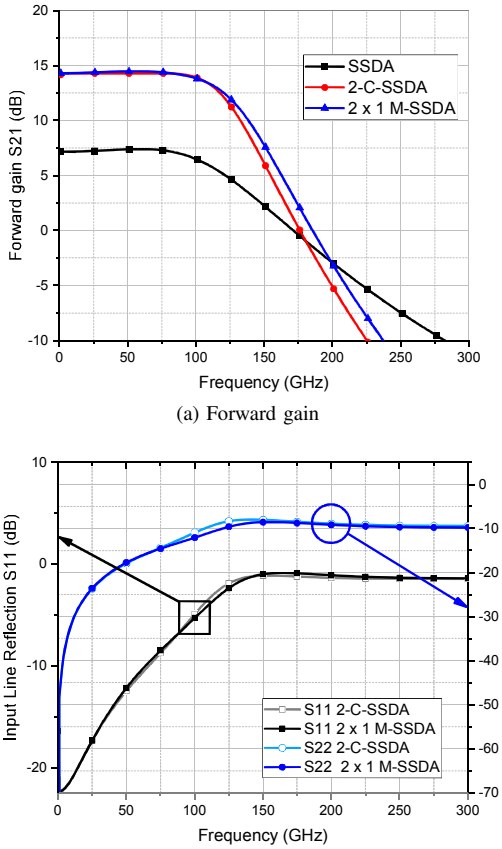
$$Z_{in} = \frac{j\omega L_B}{2} + \frac{r_\pi \left(j\omega \frac{L_B}{2} + R_o\right)}{r_\pi + \left(R_o + j\omega \frac{L_B}{2}\right)\left(1 + j\omega r_\pi C_\pi\right)}; \tag{2}$$

$$Z_{int} = \frac{j\omega L_{CB}}{2} + \frac{r_\pi \| r_o \left(j\omega \frac{L_{CB}}{2} + R_o\right)}{r_\pi \| r_o + \left(R_o + j\omega \frac{L_{CB}}{2}\right)\left(1 + j\omega \left(C_\pi + C_{ce}\right) r_\pi \| r_o\right)}, \tag{3}$$

$$Z_{out} = \frac{j\omega L_C}{2} + \frac{r_o \left(j\omega \frac{L_C}{2} + R_o\right)}{r_o + \left(R_o + j\omega \frac{L_C}{2}\right)\left(1 + j\omega r_o C_{ce}\right)}; \tag{4}$$

with $L_B = Z_o^2 C_\pi$; $L_{CB} = Z_o^2 (C_\pi + C_{ce})$ and $L_C = Z_o^2 C_{ce}$ [15], [16].

Expectedly, the bandwidth of the M-SSDA is dominated by the cut-off frequency of the intermediate transmission line $f_{c(int)}$,



(a) Forward gain

(b) Input and output line reflection

Fig. 3: S-parameter comparison of a 2×1 M-SSDA with a 2-C-SSDA.

$$f_{c(int)} = \frac{1}{\pi\sqrt{L_{CB}\left(C_\pi + C_{ce}\right)}}. \tag{5}$$

However, as under usual bias conditions C_π is significantly larger than C_{ce}, the cutoff frequencies of both the input line and intermediate transmission lines are close [15], [17].

A. *Performance prediction and comparison*

The described amplifier is demonstrated in simulation using a full foundry model of TSC250; an Indium Phosphide foundry DHBT process by Teledyne Scientific Companies. The device offers f_t/f_{max} of 350/600 GHz while maintaining a CE breakdown voltage of more than 4V. Detailed descriptions of this process is available in [10].

Fig. 3 compares the s-parameters simulation results of the 2×1 M-SSDA with a 2 cascaded SSDA (2-C-SSDA) using Keysight's *Advanced Design System* (ADS) software. A plot of the SSDA forward gain is included as a reference of single stage gain. All circuits employ CE gain cells. For meaningful performance comparison, the circuits are simulated using the same process model and the identical HBT devices operated at the same bias. Lossless transmission lines and ideal circuit elements were used, with elements individually optimized for best two stage amplifier performance.

In Fig. 3, the close similarity between the s-parameter performance of the 2-C-SSDA and the 2 tiered M-SSDA can be observed. This demonstrates the viability of the M-SSDA as a design option for high gain distributed amplifiers, with the added advantage of reduced circuit footprint.

III. Bandwidth Optimized 3×1 M-SSDA

To improve bandwidth performance of the M-SSDA while maintaining a flat gain profile, modifications to the transmission lines and gain cell of the proposed amplifier similar to [18] are subsequently described.

A. Input and intermediate line modification

From the foregoing discussion, it is clear that extending the cutoff frequency (f_c) of the intermediate and input transmission line is crucial to improving M-SSDA bandwidth performance. The technique proposed to achieve the bandwidth extension involves scaling down the input and intermediate line inductance (L_B and L_{CB}); and creating a high frequency peak through the introduction of a shunt capacitance.

Intermediate transmission line: The intermediate line is scaled by a factor ζ (with ζ <1). The effect of the input line scaling is such that the resulting cut-off frequency $f_{c'}$ becomes

$$\frac{1}{\pi\sqrt{L_{CB}(C_\pi + C_{ce})}} < f_{c'} < \frac{1}{\pi\sqrt{\zeta L_B(C_\pi + C_{ce})}}. \quad (6)$$

(For $f_{c'} = {}^1/_{\pi\sqrt{\zeta L_B(C_\pi+C_{ce})}}$, the terminating impedance must be reduced from the conventional 50Ω to a value, $R_o = \sqrt{{}^{\zeta L_B}/_{(C_\pi+C_{ce})}}$; however, this would lead to a corresponding reduction in gain - from (1)).

From 3, the impedance Z^*_{int} of the scaled intermediate line is

$$Z^*_{int} = \frac{j\omega\zeta L_{CB}}{2} + \frac{r_\pi \| r_o \left(j\omega\frac{\zeta L_{CB}}{2} + R_o\right)}{r_\pi \| r_o + \left(R_o + j\omega\frac{\zeta L_{CB}}{2}\right)\left(1 + j\omega\left(C_\pi + C_{ce}\right) r_\pi \| r_o\right)}. \quad (7)$$

To further increase the bandwidth of the intermediate line, a shunt capacitor C_{peak} is added, resulting in a high frequency resonant peak (f_{peak}), given to a good estimation by

$$f_{peak} = \frac{1}{2\pi\sqrt{\zeta L_{CB} C_{peak}}}. \quad (8)$$

Significant improvement in the 3 dB bandwidth of the input line can be obtained by optimizing the value of C_{peak} and ζ. The impedance Z^{**}_{in} of the resulting transmission line is

$$Z^{**}_{in} = \frac{Z^*_{in}}{1 + j\omega C_{peak} Z^*_{in}}. \quad (9)$$

The addition of a shunt capacitance effectively increases the order of the input line filter leading to a sharper roll off.

To illustrate the described concept, Fig. 4 compares the bandwidth (in terms of transmission loss) of a conventional image impedance line with a 50% scaled line; a peaked line and a line which features both 50% scaling and peaking for a transmission line with capacitance of 50 fF and 50Ω termination. In both cases where peaking is applied, the value of the peaking capacitor is individually optimized to yield the best bandwidth performance.

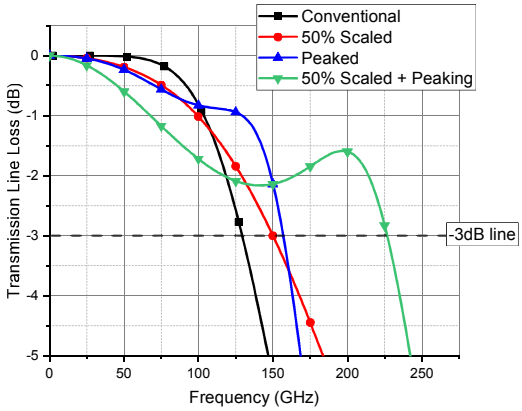


Fig. 4: Line losses for a conventional transmission line; 50% scaled transmission line; and a 50% scaled transmission line with peaking.

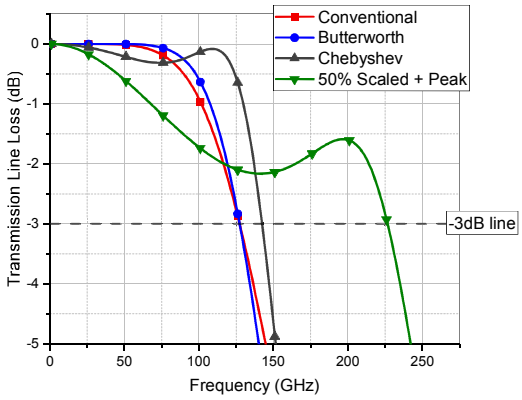


Fig. 5: Line losses for a conventional; Butterworth; Chebyshev and the proposed transmission line

As can be observed in Fig. 4, scaling the transmission line as described only marginally increases the line f_c, however, it alters the line response in a manner that makes the peaking more effective. An added merit of transmission line scaling is that with the resulting shorter transmission lines, attenuation due to line losses is reduced.

The bandwidth of the new transmission line significantly exceeds that of transmission lines designed based on Butterworth and Chebyshev functions as proposed in [19], [4].

Input transmission line: Due to the fact that the cutoff frequencies of the input and intermediate lines ($f_{c(in)}$ and $f_{c(int)}$) are close, to achieve significant improvement in the amplifier bandwidth performance, it is essential that $f_{c(in)}$ also be increased. Scaling the input line inductance line by a different factor ζ_2, where

$$\zeta_2 = \zeta \left(\frac{C_\pi + C_{ce}}{C_\pi} \right), \tag{10}$$

would make the scaled values of L_{CB} and L_B equal, and slightly increase $f_{c(in)}$. The peaking capacitor C_{peak2} - on the input line is chosen to obtain a frequency response similar to the intermediate line response as

$$C_{peak2} = C_{peak} \left(\frac{C_\pi}{C_\pi + C_{ce}} \right). \tag{11}$$

To reduce reflection on the input line an emitter-follower (EF) buffer may be added.

B. Gain cell modification

The cascode pair gain cell is considered adequate as this provides wider bandwidth and better input-output isolation than the CE, such that the bridge capacitance C_μ has a negligible effect.

The effect of increasing the ratio of C_π to L_B and $(C_\pi + C_{ce})$ to L_{CB} is that the transmission line would have higher reflection at high frequencies leading to a dip in the gain profile. To counteract this, the gain compensation techniques described in [20] and [21] is adapted to achieve flat gain.

The key feature of this technique is the introduction of two inductive lines, L_{cb} (at the base of the common-base (CB) transistor) and L_{ce} (between the CE and CB transistors) to a cascode gain cell. With this, the output impedance Z_{out} is

$$Z_{out} = \left(\frac{(Z_{ce} + j\omega L_{ce})}{(Z_{ce} + j\omega L_{ce}) + (Z_{be} + j\omega L_{cb})} \right) \times \left(\frac{g_m Z_{ce}}{j\omega C_{be}} + Z_{be} + j\omega L_{cb} \right) + Z_{ce}, \tag{12}$$

where Z_{ce} is the impedance between the collector and the emitter of the CE transistor and Z_{be} is the impedance between the base and the emitter of the CB transistor.

As in [21], the value of L_{ce} is adjusted to increase the negative resistance generated in the circuit and achieve the desired high frequency gain. L_{cb} is also modified appropriately to maintain stability.

To further improve gain flatness, an inductance L_{cc} is added between the collector terminal of the common base transistor and line L_{CB} and L_C. This creates an m-section type filter [15], for which $m = {}^{C_{ce}}/_{\zeta C_\pi}$ for delay synchronization; and

$$L_{cc} = \frac{1 - m^2}{4m} \zeta L_B. \tag{13}$$

Due to the complexity of the analysis involved, optimal values for L_{cb} and L_{ce} may be more easily obtained through computer aided optimization.

The cascode gain cell featuring the descibed gain cell modification is shown as an inset in Fig. 6.

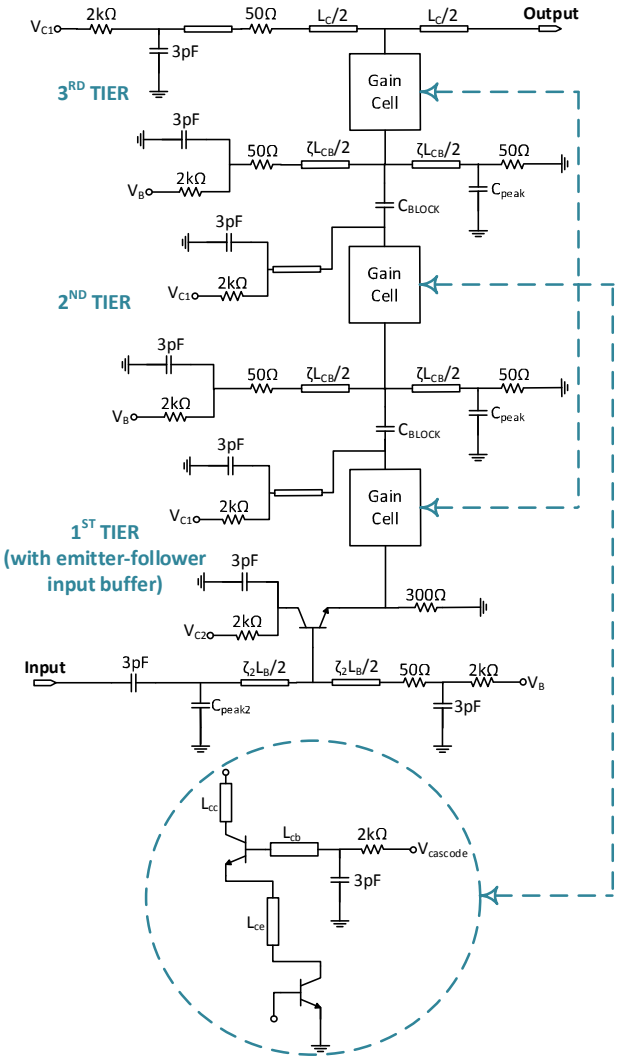


Fig. 6: 3-tier M-SSDA schematic with scaled input and intermediate transmission lines. Inset shows the modified gain cell.

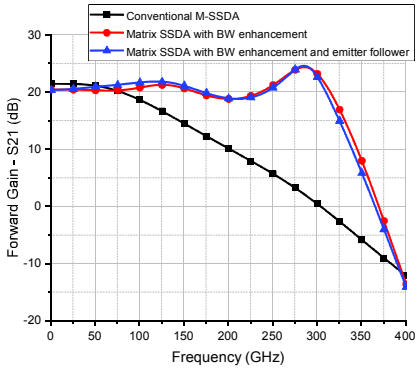
C. Performance assessment and verification

The schematic of a practical three-tier matrix single stage distributed amplifier (M-SSDA) based on the proposed design technique and featuring an EF input buffer is presented in Fig 6. The proposed design is based on the TSC250 DHBT foundry process model.

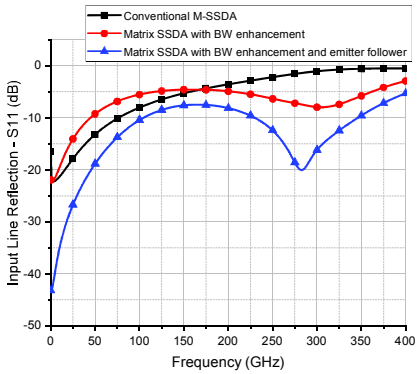
Fig. 7 compares the S-parameter performance of the bandwidth optimised M-SSDA with EF input buffer and a 3 tiered CE M-SSDA. S-parameter results of the bandwidth optimised M-SSDA without an EF buffer is also included to show its effect particularly on the input line (Fig. 7b).

For fair comparison, all circuits are simulated using the same process model and operate at the same bias conditions. Lossless transmission lines and ideal circuit elements were used in simulations.

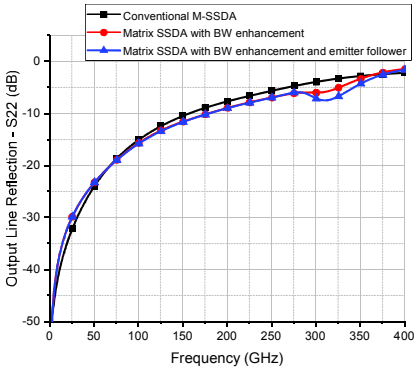
Circuit simulations predict a 324 GHz 3dB bandwidth for the new technique; more than three times the bandwidth of a basic CE M-SSDA with equal number of tiers (Fig. 7a).



(a) Forward gain S21 (dB) comparison.



(b) Input line reflection S11 (dB) comparison.



(c) Output line reflection S22 (dB) comparison

Fig. 7: S-Parameter comparison of three M-SSDA designs.

It can also be observed that, with the addition of a common collector input buffer, there is significant reduction in the input reflection (S11) of the M-SSDA (Fig. 7b).

IV. Conclusion

The M-SSDA - a multi-tiered single stage amplifier - is proposed as a more compact high gain alternative to the cascaded-SSDA with smaller circuit footprint, potentially lower transmission line losses and better noise performance. By employing only multiplicative gain, the amplifier offers more gain-per-device than both the conventional DA and matrix amplifier. A 3×1 M-SSDA circuit optimized for bandwidth and gain flatness is also presented. This design features scaled input and intermediate transmission lines and high frequency peaking is introduced through shunt capacitance. Negative resistance attenuation compensation is applied in the gain cells to achieve a flat gain profile. Simulation results based on a full foundry DHBT process predict a gain of 20dB at 324GHz bandwidth; this is more than a threefold bandwidth improvement compared to the basic CE M-SSDA.

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