Bandwidth Enhancement Technique for Bipolar Single Stage Distributed Amplifier Design

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***Abstract*—This work reports a novel approach to extending the bandwidth of single stage distributed amplifiers (SSDAs). The three-stepped technique involves scaling down the inductance on the input artificial transmission line (ATL); creating a high frequency resonance peak by the addition of shunt capacitance on the input ATL; and compensating for the resulting increased reflection with adapted negative resistance attenuation compensation techniques. Compared with the inductive-peaked cascode technique applied in the SSDA which currently has the highest reported bandwidth, simulation results, based on full foundry transistor models, predict up to 30% improvement in gain-bandwidth (GBW) performance for the same active device at the same bias. In addition, the reduction in the length of the input ATL effectively reduces transmission line losses, thereby improving the overall gain performance.**

***Index Terms*—Single stage distributed amplifier (SSDA); transmission line scaling, attenuation compensation; Indium Phosphide (InP); double heterojunction bipolar transistor (DHBT); inductive peaking**

I. Introduction

Distributed amplification was initially proposed as a means of improving the robustness of thermionic valve circuits in terms of bandwidth and bias voltage [1]. This improvement is achieved by separating the inter-electrode capacitance of individual vacuum tubes while adding their transconductance. Since its introduction, the concept has been applied in the design of amplifiers with very broad bandwidth; the highest reported being 235 GHz using a transistor with 350 GHz transition frequency (f_T) [2].

To achieve substantial gain, the distributed amplifier (DA) was conceived as a multistage amplifier [1], [3]. The concept and practicability of single stage distributed amplifiers (SSDAs) was demonstrated in [4]. Furthermore, it has been established that due to the multiplicative gain achieved from cascading two or more SSDAs with moderate gain; higher gain can be achieved than with a conventional DA having the same number of gain cells [5]. This has made the cascaded SSDA (CSSDA) a preferred option for high gain wideband amplifiers.

Bipolar transistors are attractive for DA designs because they offer higher gains and better linearity than field effect transistors (FETs) of a similar generation[6]. However, the resistive input characteristics of bipolar transistors directly translates to higher losses on their input artificial transmission line (ATL) and to a complex characteristic impedance that makes the design of line termination more challenging [7]. This effectively introduces higher attenuation with each additional stage of the DA, meaning that fewer stages can be realised before the overall gain begins to drop [7], [8]. These considerations make bipolar transistors better suited in SSDAs than in multistage distributed amplifiers.

Several techniques have been proposed to extend the bandwidth of distributed amplifiers, including those which employ bipolar transistors [9], [10], [11], [12]. The work presented here extends such techniques to achieve further bandwith improvement using ATL optimization methods.

The outline of this paper is as follows: section II describes the fundamental design concept as a three step process: increasing the 3dB cutoff frequency of the input line by scaling down the line length; introducing a high frequency peak through a shunt capacitance on the input line; and applying attenuation compensation on the output line to improve overall gain profile. Section III demonstrates the applicability of this concept through simulation studies based on full circuit models of an Indium Phosphide InP double heterojuntion bipolar transistor (DHBT) and compares the bandwidth and gain performance of the new technique to the technique adopted in the SSDA with the widest reported bandwidth [2]. Section IV concludes the paper.

II. Design Concept

Fig. 1 shows simplified equivalent circuits of the input and output ATLs of an HBT SSDA. The lines are made up of intrinsic capacitance C_π and C_{ce} and inductive lines L_B and L_C; with both lines coupled by the transistor transconductance g_m. r_π and r_o are the transistor base-emitter junction resistance and output, resistance respectively and R_{TERM} is the terminating resistance.

The design technique proposed and verified in this paper is a three-stepped process involving two modifications to the input line of the conventional SSDA; and one to the output line.

A. Input Line Modification

It has been established that the bandwidth performance of a DA is determined by the cutoff frequency of the input line [13],

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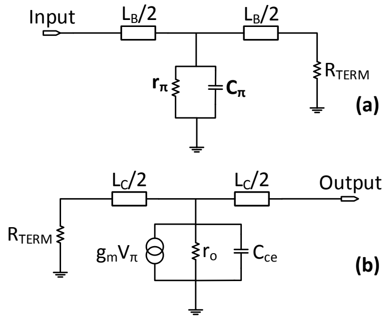

Fig. 1. Simplified equivalent circuits of (a) input transmission line of a conventional HBT SSDA and (b) Output Transmission Line of a conventional HBT SSDA.

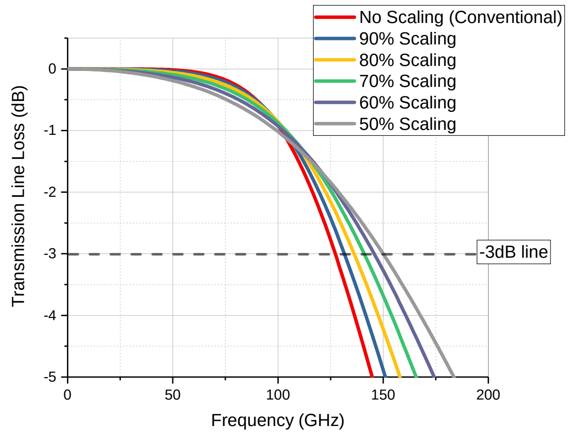

Fig. 2. Bandwidth improvement from line scaling.

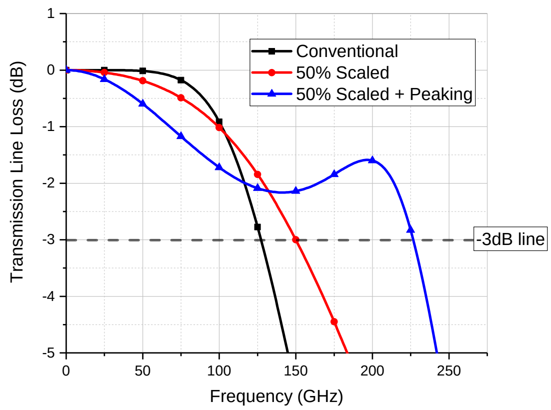

Fig. 3. Comparison of line losses for a conventional transmission line, 50% scaled transmission line and a 50% scaled transmission line with peaking.

[3]. This is due to the fact that the input capacitances of both bipolar and field effect transistors is usually larger than their output capacitances. Hence, by the image impedance design approach employed in conventional DA, the input line would have a lower cutoff frequency which will dominate the DA bandwidth performance.

Therefore, to achieve higher bandwidth, the cutoff frequency of the input artificial transmission line (ATL) must be increased. This is achieved in two steps:

Step 1: Increase the 3dB cutoff frequency of input line by scaling down the line length (inductor value, if discrete components are used): Recall that the image impedance of the input transmission line (Z_{o-in}) is given by

$$Z_{o-in} = \sqrt{\frac{L_B}{C_\pi}\left(1 - \frac{4\pi^2 f^2 L_B C_\pi}{4}\right)} \qquad (1)$$

with C_π being the base-emitter capacitance of the common emitter amplifier; L_B being the inductance value required to achieve the distributed effect; and ω being the angular frequency. With the cutoff frequency of the line, $f_c = {}^1/_{\pi\sqrt{L_B C_\pi}}$ (for ideal lossless lines). At this frequency, the image impedance transitions from being purely real to being purely imaginary if the line is terminated with the DC value of Z_{o-in}, denoted by Z^*_{o-in} such that

$$Z^*_{o-in} = \sqrt{\frac{L_B}{C_\pi}}. \qquad (2)$$

We extend the cutoff frequency by scaling L_B by a factor, ζ (with ζ<1), while keeping the terminating impedances R_{TERM} at the value of Z^*_{o-in}. This results in cut-off frequency $f_{c'}$ that is

$$\frac{1}{\pi\sqrt{L_B C_\pi}} < f_{c'} < \frac{1}{\pi\sqrt{\zeta L_B C_\pi}}. \qquad (3)$$

For $f_{c'} = {}^1/_{\pi\sqrt{\zeta L_B C_\pi}}$, the terminating impedance must be reduced such that $R_{TERM} = \sqrt{{}^{\zeta L_B}/_{C_\pi}}$. However, this would lead to a corresponding reduction in gain, as

$$Gain = N g_m \frac{\sqrt{Z_{o-in}.Z_{o-out}}}{2}, \qquad (4)$$

where g_m is the transistor transconductance; Z_{o-in} is the input line impedance; Z_{o-out} is the output line impedance and N is the number of gain stages. By terminating with Z^*_{o-in}, the gain is kept at the same level as will be obtained from a conventional DA.

Fig. 2 shows the gain in bandwidth with incremental scaling for a hypothetical HBT with C_π of 50 fF and 50Ω termination.

Step 2: Introduce a high frequency peak through a shunt capacitance: The addition of shunt capacitance C_{peak} at the input line would result in an LC resonant peak given to a good approximation by

$$f_{peak} \approx \frac{1}{\pi\sqrt{\zeta \frac{L_B}{2}(C_\pi + C_{peak})}}. \qquad (5)$$

By optimising the value of C_{peak} and ζ, the peak frequency, amplitude and bandwidth can be used to significantly improve the 3dB bandwidth of the input line.

To illustrate the concept, Fig. 3 compares the bandwidth of a conventional image impedance line with a 50% scaled line and a line which features both 50% scaling and LC peaking from an hypothetical HBT with C_π of 50 fF and 50Ω termination. This is shown in terms of transmission loss of three different ATLs.

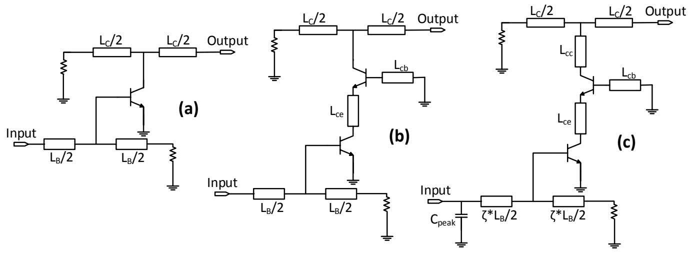

Fig. 4. Schematic circuits of (a) conventional SSDA; (b) SSDA with inductive-peaked cascode [15]; and (c) new SSDA with scaled input line, shunt capacitance and adapted loss compensation.

B. Output Line Modification

Step 3: Apply negative resistance attenuation compensation technique to improve the overall gain profile: The effect of increasing the ratio of C_π to L_B is that the transmission line would have higher reflection at high frequencies leading to a dip in the gain profile. To counteract this, the HBT version of the attenuation compensation techniques described in [11] and [10] is modified to achieve a flat gain profile.

The key feature of this technique is the introduction of two additional transmission lines, L_{cb} (at the base of the common base transistor) and L_{ce} (between the common emitter and common base transistors) to a cascode gain cell. For this circuit, the output impedance Z_{out} is

$$Z_{out} = \frac{(Z_{ce} + j\omega L_{ce})}{(Z_{ce} + j\omega L_{ce}) + (Z_{be} + j\omega L_{cb})} \times \left(\frac{g_m Z_{ce}}{j\omega C_{be}} + (Z_{be} + j\omega L_{cb}) \right) + Z_{ce} \quad (6)$$

where Z_{ce} is the impedance between the collector and the emitter of the common collector and Z_{be} is the impedance between the base and the emitter of the common base forming the cascode pair. The value of L_{ce} is adjusted proportional to ζ to increase the negative resistance generated in the circuit and maintain the desired high frequency gain. The resulting inductance value, is denoted by L'_{ce} in (7). L_{cb} is also modified appropriately to maintain stability (the resulting value is denoted by L'_{cb} in (7)).

The resulting output impedance is given by

$$Z_{out} = \frac{(Z_{ce} + j\omega L'_{ce})}{(Z_{ce} + j\omega L'_{ce}) + (Z_{be} + j\omega L'_{cb})} \times \left(\frac{g_m Z_{ce}}{j\omega C_{be}} + (Z_{be} + j\omega L'_{cb}) \right) + Z_{ce} \quad (7)$$

Fig. 4(a) shows the schematic circuit for a conventional SSDA; Fig. 4(b) shows the loss compensation circuit presented in [14]; while Fig. 4(c) shows the new SSDA schematic featuring the scaled input line, the shunt capacitance for input line peaking and the adapted loss compensation for gain flatness.

Due to the complexity of the analysis involved, the optimal values for L'_{cb} and L'_{ce} may be more easily obtained through computer aided optimisation. For extra degree of tunability, an inductance L_{cc} is added between the collector terminal of the common base transistor and line L_C.

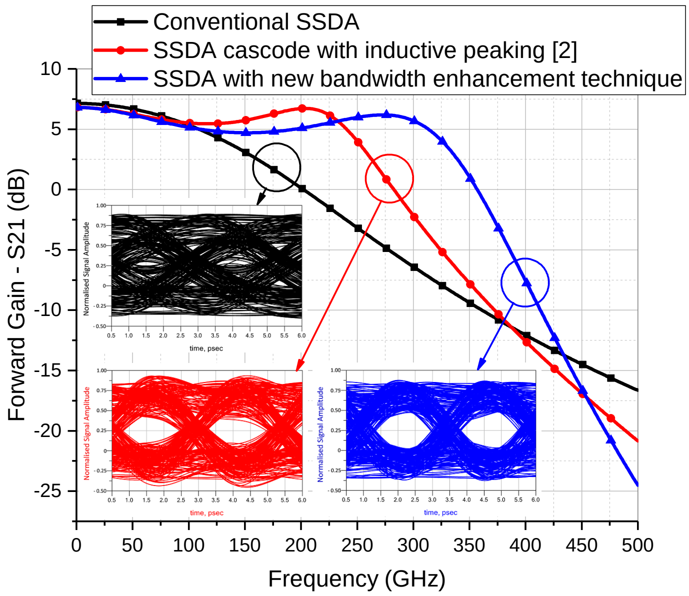

Fig. 5. Forward Gain S21(dB) with corresponding simulated eye diagrams at 500Gbit/s (inset): Conventional - 3dB-bandwidth 132GHz/ 7dB gain; SSDA with inductive-peaked cascode - 3dB-bandwidth 253GHz/7dB gain; and SSDA with new bandwidth enhancement technique - 3dB-bandwidth 328 GHz/7dB gain.

It is interesting to note that either of steps 1 or 2 may be combined with output line attenuation compensation to achieve improved bandwidth performance. However combining the two steps expectedly yields the optimum result of maximum bandwidth.

III. Performance Assessment and Verification

The aforementioned technique is demonstrated in simulation using the full circuit model of TSC250; an Indium Phosphide foundry heterojunction bipolar transistor process by Teledyne Scientific Companies. The device offers f_t/f_{max} of 350/600 GHz while maintaining a common-emitter breakdown voltage of more than 4V. Detailed descriptions of this process is available in [16].

Figures 5, 6 and 7 compare the forward gain (S21), the input line reflection (S11) and the output line reflection (S22) respectively, of a conventional SSDA (Fig. 4a); SSDA with the inductive-peaked cascode technique used in [15] (Fig. 4b); and a SSDA that features the proposed bandwidth extension technique (Fig. 4c). For fair comparison, all three circuits are simulated using the same process model and operate at the same bias conditions. Lossless transmission lines and ideal circuit elements were used in simulations.

Circuit simulations predict a 328 GHz 3dB bandwidth for the the new technique. This is nearly two-and-a-half times the bandwidth of an otherwise equivalent SSDA designed using conventional means and 30% higher than what is achieved with the technique adopted in [15] (Fig. 5). The input line modifications result in a gain ripple of ±1dB (Fig. 5). The phase response of the new design was tested and shows linear

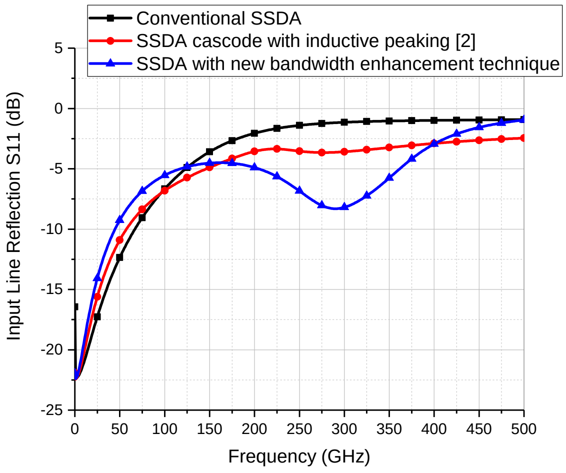

Fig. 6. Input Line Reflection S11(dB) Comparison.

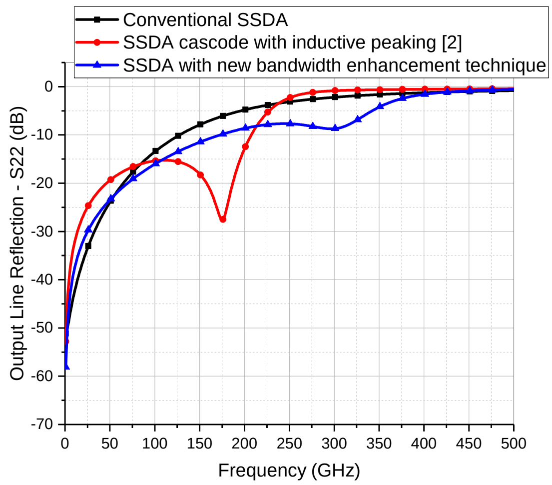

Fig. 7. Output Line Reflection S22(dB) Comparison.

phase up to the 3dB gain of the amplifier, leading to good pulse response which is indicated by an open eye shown in the inset of the figure and simulated assuming 500 Gbit/s data stream of $2^{12}-1$ pseudo random binary sequence. The open eye for the new design furthermore show its advantage when compared to the fully closed eye diagram of the conventional design and the less open one of the design following [15].

Additionally, the design improves the input and output matching behaviour as shown, respectively in Figs. 6 and 7. The design is unconditionally stable, as both the Edwards-Sinsky stability parameter (μ) and the Rollett's stability factor (K) are greater than 1 from DC up to 500 GHz. Furthermore, the new design displays better phase linearity and smaller delay variation than the conventional design. The group delay is simulated to be approximately 4 ± 1 ps from low frequencies to 500 GHz, which leads to the good pulse response observed in the eye diagram of Fig. 5. The power consumption of the amplifier is expected to be below 12 mW.

The transmission line scaling technique has the added advantage of reducing the attenuation associated with transmission lines, however, it is noteworthy that this technique will not be well suited to multi-stage distributed amplifiers as the effects of improper distribution from line scaling become more pronounced with additional stages. To meet higher gain requirement, SSDAs based on this bandwidth enhancement technique can be suitably applied as units of high-gain-block wideband amplifiers through cascading or in a single stage matrix topology.

IV. Conclusion

A new design technique for bipolar based SSDAs is introduced through which significant improvement in bandwidth can be achieved. It involves purposely scaling down the inductance and introducing a high frequency LC peak (through a shunt capacitance) on the amplifier's input line; and negative resistance attenuation compensation on the output line. This technique can be used to achieve distributed amplifiers with significantly wider bandwidth and with improved time domain response and input and output matching behaviour.

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