

MBE growth of 1.7eV $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ and 1.42eV GaAs solar cells on Si using dislocations filters: an alternative pathway toward III-V/Si solar cells architectures

Arthur Onno¹, *Student Member, IEEE*, Mingchu Tang¹, Mu Wang¹, Yurii Maidaniuk², Mourad Benamara², Yuriy I. Mazur², Gregory J. Salamo², Lars Oberbeck³, Jiang Wu¹, Huiyun Liu¹

¹Department of Electronic and Electrical Engineering, UCL, London, WC1E 7JE, United Kingdom

²Institute for Nanoscience and Engineering, University of Arkansas, Fayetteville, AK 72701, USA

³Total Gas, Renewables & Power, Paris La Défense, 92069, France

Abstract — Metamorphic epitaxial growth of III-V solar cells on Si has attracted significant interest for the development of III-V/Si photovoltaic architectures. In this work, we present an alternative pathway – using MBE growth techniques – based on the direct nucleation of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ materials on Si, followed by the growth of a 1.7eV $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ or a 1.42eV GaAs solar cell. Dislocation Filter Layers (DFLs), in conjunction with Thermal Cycle Annealing (TCA), have been used to reduce the Threading Dislocation Density (TDD) below 10^7cm^{-2} in the base of the cell; close to the best results demonstrated with metamorphic buffers.

Index Terms — III-V on Silicon, Molecular Beam Epitaxy, Threading dislocation density, Photovoltaic solar cells.

I. INTRODUCTION

Silicon-based hybrid photovoltaic devices have gained substantial academic interest in the recent years, with a wide range of absorber materials and fabrication techniques being investigated in order to overcome the efficiency limitations of crystalline silicon (c-Si) single junction photovoltaic technologies [1-2]. Among these approaches, epitaxial growth of III-V cells on a c-Si substrate, the latter potentially acting as a bottom cell, represents an elegant pathway. This technique – on top of taking advantage of the robust supply chain and low cost associated with market-dominant c-Si photovoltaic technologies – potentially enables the formation of the different p-n junctions of a multijunction solar cell in a single growth reactor and the use of a 2-terminal contacting architecture, leading to a possibly straightforward deposition and fabrication process.

The main challenge associated with the epitaxial growth of III-V compound semiconductors on Si for photovoltaic applications lies in the difference of lattice parameters between Si and III-V materials of interest. Indeed, there is no nitrogen-free direct bandgap III-V material lattice-matched to Si. Consequently lattice-mismatched approaches are needed in order to grow III-V solar cells on Si, resulting in an accumulation of strain in the grown film. Relaxation of the epilayers occurs through the formation of Misfit Dislocations (MDs) and Threading Dislocations (TDs). While MDs are confined to plans parallel to the growth surface, TDs

propagate vertically through the epilayers to the active region of the device, where they act as recombination centers, thus strongly impacting the minority carrier lifetime. Reducing the Threading Dislocation Density (TDD) to a minimum is thereby essential in order to achieve high performance minority-carrier-dominant devices such as photovoltaic cells.

Metamorphic pathways have so far led to the most compelling results. This approach consists in the growth of a lattice-matched nucleation layer – such as GaP [3] or Si [4-5] – on the Si substrate, followed by a gradual adjustment of the epilayers' lattice-parameter through alteration of their composition – for example by adding As to $\text{GaAs}_x\text{P}_{1-x}$ epilayers [3] or Ge to $\text{Si}_x\text{Ge}_{1-x}$ epilayers [4-5]. Due to the limited differences in lattice parameters throughout the metamorphic buffer, the TDD is kept low within the epitaxial film. High bandgap ($E_g > 1.6\text{eV}$) III-V solar cells epitaxially grown on Si with TDDs below $5 \times 10^6\text{cm}^{-2}$ have been demonstrated, leading to bandgap-voltage offset (W_{oc}) values under 0.55V [6-7]. Using $\text{Si}_x\text{Ge}_{1-x}$ buffers, a V_{oc} above 1.0V ($W_{oc} < 0.4\text{V}$) and a TDD below 10^6cm^{-2} have even been reported for GaAs solar cells [4], although these results have not been replicated with higher bandgap cells.

Using Molecular Beam Epitaxy (MBE) growth techniques, we present an alternative non-metamorphic pathway – similar to the approach developed by Yamaguchi *et. al.* [8] – based on the direct nucleation of materials from the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ system on Si substrates. A high TDD is thus obtained at the III-V/Si interface, due to the 4% lattice-mismatch between $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and Si. Dislocation Filter Layers (DFLs), consisting of an iteration of spaced Strained Layer Superlattices (SLSs) [9], are then grown in order to reduce the TDD by 2 to 4 orders of magnitude. Excellent results have recently been achieved on MBE-grown quantum dot lasers using this approach [10], with the demonstration of a TDD below 10^6cm^{-2} . In this work, transfer of this technique to III-V solar cells monolithically grown on Si – in the present case 1.7eV $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ solar cells for dual-junction $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}/\text{Si}$ applications and 1.42eV GaAs cells for use in stand-alone single junction devices or as middle subcells in an $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}/\text{GaAs}/\text{Si}$ triple-junction architectures – is presented.

II. EXPERIMENTAL METHODS

A. Samples growth

For both absorber materials investigated ($\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ and GaAs), two samples have been grown: one reference sample grown lattice-matched on GaAs and one sample grown on Si using Dislocation Filter Layers (DFLs) and Thermal Cycle Annealing (TCA). The four samples were grown in a Veeco GEN 930 Solid State Molecular Beam Epitaxy (SSMBE) system.

Temperatures were controlled using an infrared pyrometer and a thermocouple mounted on the back of the substrate-holder. Reflection High Energy Electron Diffraction (RHEED) was used to in-situ monitor the evolution of the growth surface during deposition as well as during the pre-growth high-temperature oxide removal step. The lattice-mismatched growth runs on Si were performed on n-type Si (100) wafers offcut 4° towards the [01-1] plane in order to avoid the formation of Anti-Phase Domains (APDs) due to polar-on-nonpolar epitaxy [11]. Standard n-type GaAs wafers were used for the lattice-matched reference samples.

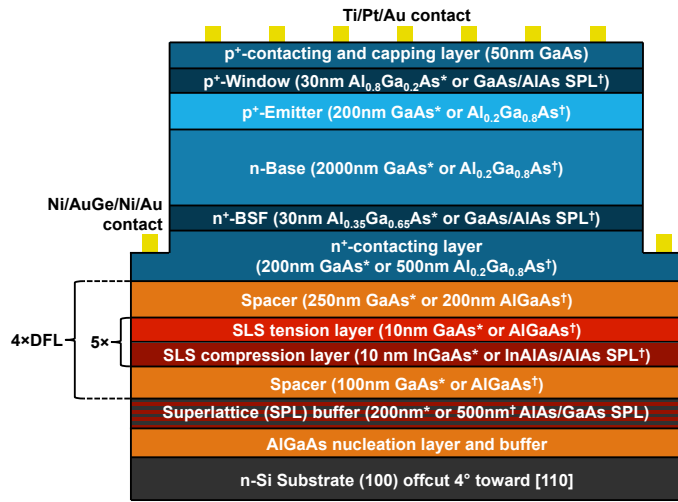


Fig. 1. Structure of the samples grown on Si. The DFL buffer is in orange/red, the active layers of the devices are in blue. The differing parameters between the two batches of samples are indicated by the “†” symbol for the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ cells and by the “*” symbol for the GaAs ones. The reference samples grown lattice-matched on GaAs present an identical device structure (in blue), the DFL buffer (in orange/red) being replaced by a 200nm-thick GaAs buffer.

The structure of the samples grown on Si is presented in Figure 1. The DFL buffer is depicted in orange/red, the active layers of the devices are in blue. The reference samples grown on GaAs have an identical device structure, the DFL buffer being replaced by a 200nm-thick GaAs buffer. As only one Al source was available at the time of growth, the Al deposition rate was fixed throughout the growth runs. As a result, the structure of the DFL buffer, Back Surface Field (BSF) and

window layers were adapted for the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ cells and differ from the GaAs samples.

The DFL buffer consists in an $\text{Al}_x\text{Ga}_{1-x}\text{As}$ nucleation layer followed by an AlAs/GaAs superlattice (SPL) in order to smooth out the growth surface [12] before deposition of the four DFLs. Each DFL is comprised of a Strained-Layer Superlattice (SLS) made of alternating compression and tension layers [9] inserted between two $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ or GaAs spacers. The TCA cycles were performed immediately following the growth of each SLS DFL. Details about the annealing sequence can be found in Ref. [10].

The $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ and GaAs cells have a similar device structure consisting in a bottom n⁺-type contacting layer – 200nm-thick for GaAs devices, 500nm-thick for $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ devices – followed by a 30nm-thick n⁺-type BSF, a 2000nm-thick n-type base, a 200nm-thick p⁺-type emitter, a 30nm-thick p⁺-type window layer and finally a 50nm-thick p⁺-GaAs contacting and capping layer. For the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ cells, AlAs/GaAs SPLs have been used for the BSF and window layers. Conversely, for the GaAs cells, $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ and $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$ layers have been used the BSF and window layers, respectively.

B. Devices fabrication

Patterning was performed by standard photolithography techniques prior to device separation by wet etching and metal contacts deposition. The samples were first selectively etched in a $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (1:10:80) solution in order to define $3\times 3\text{mm}$ individual mesa-structures and to access the bottom n⁺-contacting layer, as shown on Figure 1. The contact to the n-type region consists in a Ni/AuGe/Ni/Au (5nm/100nm/30nm/200nm) metal structure thermally evaporated and annealed at 390°C for 60 seconds under N_2 atmosphere. The same contact structure was also evaporated on the full back of the two samples grown on GaAs in order to improve the lateral conduction of charge carriers to the base of the devices. As the wafers used for the growth on Si were low-doped (1 to $10\ \Omega\cdot\text{cm}$), no contacts were deposited on the back of these samples. A Ti/Pt/Au (20nm/50nm/400nm) front grid contact to the p-type region was finally deposited by sputtering.

It is to be noted that the top GaAs p⁺-contacting layer was not etched in order to protect the underlying Al-rich layers from oxidation. Furthermore, no anti-reflection coating was applied to the samples. As a result, sizeable optical losses arise from reflection at the front surface of the devices and absorption in the top GaAs contacting layer. For $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ devices, using OPAL2 software [13], the short-circuit current density losses due to reflection and absorption are evaluated at about $8.8\text{mA}\cdot\text{cm}^{-2}$ and $5.0\text{mA}\cdot\text{cm}^{-2}$, respectively. For GaAs devices, these losses are evaluated at about $12.6\text{mA}\cdot\text{cm}^{-2}$ and $5.3\text{mA}\cdot\text{cm}^{-2}$, respectively. As the coverage of the top metal grid contact has not been optimized, resulting in a non-negligible shadowing (2.93mm^2), the current densities presented hereafter refer to the 7.07mm^2 active area of the devices.

C. Characterization

Cross-sectional Transmission Electron Microscopy (TEM) was used to characterize the structural properties of the samples and, in particular, to calculate the Threading Dislocation Density (TDD). The samples were first prepared by mechanical polishing and ion milling in a Fischione 1010 ion mill. TEM imaging was then carried out at 300keV in a FEI Titan 80-300S TEM system fitted with a CEOS image corrector.

Optoelectronic characterization of the samples and devices included Current density versus Voltage (J-V) curve tracing under AM1.5G illumination, Illumination versus Open-circuit voltage (Suns- V_{oc}) characterization and External Quantum Efficiency (EQE) measurement. J-V characteristics of the devices were acquired at 25°C using a Keithley 2400 sourcemeter coupled with ReRa Tracer 3.0 software. 1-sun AM1.5G spectrum illumination was obtained from a LOT solar simulator equipped with a filtered xenon lamp and calibrated at 100mW.cm⁻² using a GaAs calibration cell. Suns- V_{oc} characteristics were acquired using a Sinton Instruments Suns- V_{oc} system. Given the substantial difference between the absorption spectra of the c-Si reference cell used to monitor illumination and of the higher bandgap measured III-V cells, filters were placed in front of the reference cell in order to reduce the spectral mismatch to a minimum [14]. A Schott KG3 filter was used to measure the Al_{0.2}Ga_{0.8}As cells while a Techspec longpass filter with an 875nm cutoff wavelength was used to measure the GaAs cells. The 1-sun V_{oc} difference between the J-V measurements and the Suns- V_{oc} measurements was thus reduced to under 20mA.cm⁻². An additional spectral mismatch coefficient was then calculated for each device in order to match the J-V and Suns- V_{oc} measurements [14]. Room-temperature EQE of the best cells was measured with a ReRa SpeQuest quantum efficiency system.

III. RESULTS

A. Impact of the DFL on the TDD

TEM imaging of the DFLs of the GaAs sample grown on Si is shown on Figure 2. TDs are bent into MDs when they intersect with the DFLs. These MDs can then coalesce, mutually annihilate or bend back into TDs and progress upward. Annealing of the SLS increases the mobility of the TDs and MDs, improving the chances of coalescence or mutual annihilation [15].

As shown on Figure 2, each individual DFL reduces the TDD by a factor of two to six. The overall TDD is thus reduced by two full orders of magnitude, from $1 \times 10^9 \text{cm}^{-2}$ at the III-V/Si interface to $8.3(\pm 2) \times 10^6 \text{cm}^{-2}$ just after the 4th DFL. Not shown on Figure 2, the TDD in the base of the cell is further reduced to $5(\pm 2) \times 10^6 \text{cm}^{-2}$, close to the best results achieved using metamorphic approaches [3-7].

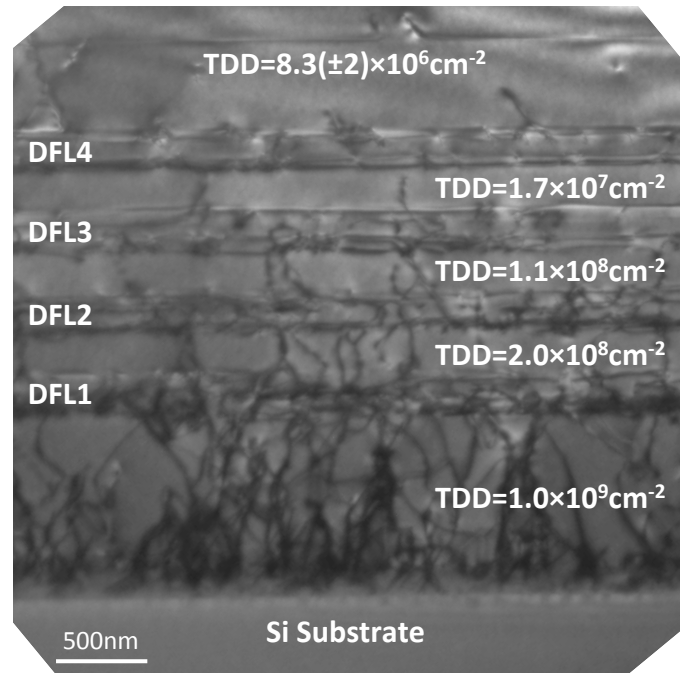


Fig. 2. Transmission Electron Microscopy (TEM) imaging of the buffer and Dislocation Filter Layers (DFLs) of the GaAs sample grown on Si. Threading Dislocations (TDs) are bent into Misfit Dislocations (MDs) in the DFL, where they can merge, mutually annihilate or bend back into TDs and resume their progression upward.

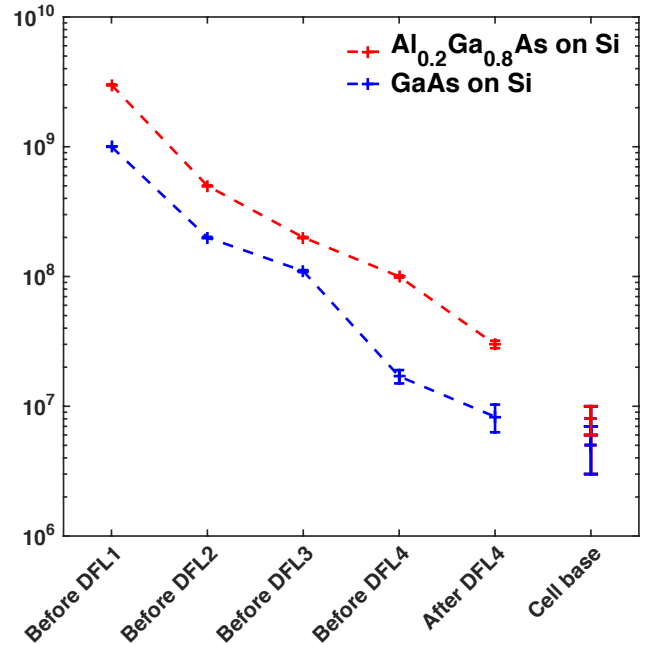


Fig. 3. Evolution of the TDD in the samples grown lattice-mismatched on Si.

Similar reductions in TDD are demonstrated for the Al_{0.2}Ga_{0.8}As sample grown lattice-mismatched on Si, as shown

on Figure 3. The TDD in the base of the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ cell grown on Si has been evaluated at $8(\pm 2) \times 10^6 \text{cm}^{-2}$.

B. 1.7eV $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ solar cells

J-V characteristics, acquired under illumination, of the best devices from both 1.7eV $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ samples are presented in Figure 4 (full lines). The pseudo-J-V curves, extracted from Suns- V_{oc} measurements, are also displayed in dashed lines.

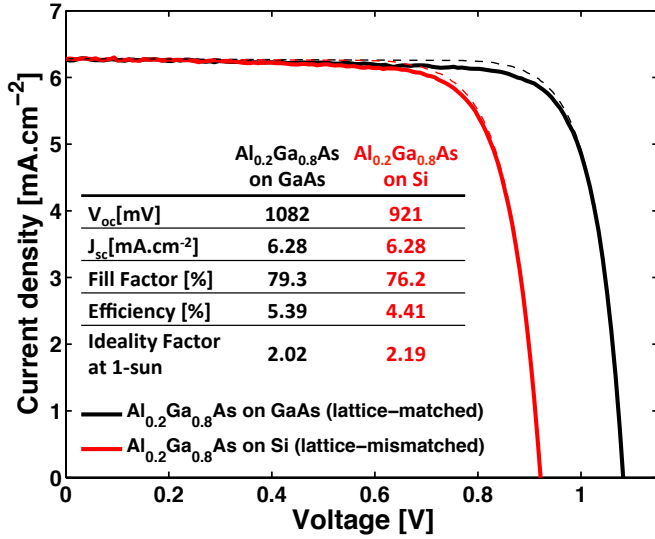


Fig. 4. J-V characteristics acquired under illumination (full lines) and pseudo-J-V curves extracted from Suns- V_{oc} measurements (dashed lines) of the best $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ devices grown on GaAs (black) and on Si (red). The impact of the presence of TDs on the performances of the cells is apparent, in particular on the V_{oc} .

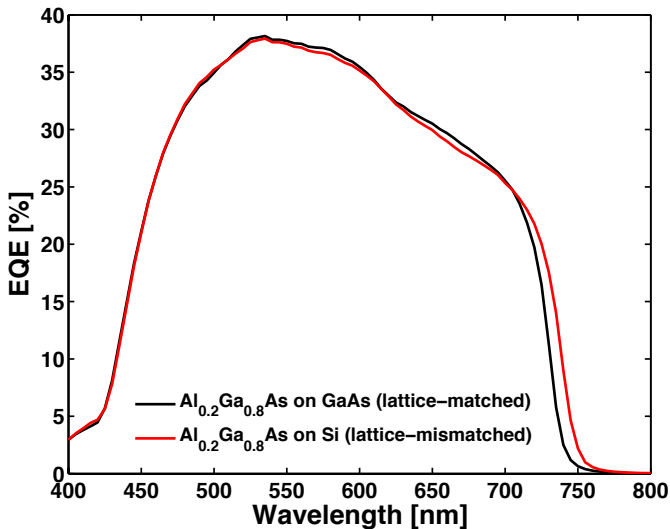


Fig. 5. External Quantum Efficiency (EQE) measurements of the best devices from the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ samples grown on GaAs (black) and on Si (red).

The impact of the TDD on the performances of the device is apparent, with a 161mV reduction in V_{oc} from the sample grown lattice-matched on GaAs to the sample grown lattice-mismatched on Si. This is in agreement with the presence of TDs shown by TEM, leading to a stronger non-radiative recombination rate and a reduced minority carrier lifetime. Ideality factors, extracted from Suns- V_{oc} measurements, also indicate a stronger non-radiative recombination rate on Si, with an increase of the 1-sun ideality factor from $n=2.02$ on GaAs to $n=2.19$ on Si.

The V_{oc} values measured are nevertheless relatively low in regard of the high bandgap of the material ($\approx 1.7\text{eV}$), even for the reference sample grown lattice-matched on GaAs. The bandgap-voltage offset W_{oc} , defined as $W_{oc} = E_g/q - V_{oc}$, thus deviates notably from the semi-empirical value of 0.4V expected from high material quality devices. The ideality factors – higher than 2 for both devices, indicating non-radiative recombinations in the depletion zone as the dominant recombination pathway – confirm this relatively low material quality. The performance of our devices, in particular the V_{oc} is consequently primarily limited by the bulk material quality of the grown $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$, independent of the presence of TDs.

Both devices present very close J_{sc} values, indicative of a limited impact of the TDs on the carrier collection efficiency. This is confirmed by the similar EQE curves presented in Figure 5. The bulk $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ material quality thus appears to be the limiting factor in the diffusion length of minority carriers in the base of the solar cells, a higher TDD being needed to impact the collection efficiency of the devices and thus their J_{sc} and EQE.

C. 1.42eV GaAs solar cells

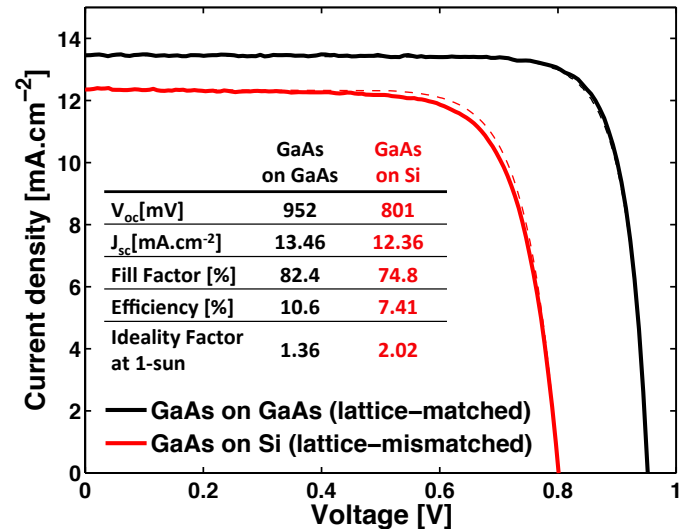


Fig. 6. J-V characteristics acquired under illumination (full lines) and pseudo-J-V curves extracted from Suns- V_{oc} measurements (dashed lines) of the best GaAs devices grown on GaAs (black) and on Si (red). The impact of the presence of TDs on the performances of the cells is apparent on the V_{oc} and on the J_{sc} .

IV. DISCUSSION

The J-V characteristics acquired under illumination (full lines) and pseudo-J-V curves extracted from Suns- V_{oc} measurements (dashed lines) of the best 1.42eV GaAs devices grown on both substrates are displayed in Figure 6. Similar to the $Al_{0.2}Ga_{0.8}As$ samples presented above, the impact of the presence of TDs is apparent with a comparable reduction in V_{oc} (151mV) between the samples grown lattice-matched on GaAs and lattice-mismatched on Si. The 1-sun ideality factors n of the cells also illustrate the impact of TDs, with an increase from $n=1.36$ – characteristic of a balance between recombination pathways – on GaAs to $n=2.02$ – characteristic of recombinations dominated by SRH recombinations in the depletion zone – on Si.

The lower ideality factor for the sample grown lattice-matched on GaAs, compared with the $Al_{0.2}Ga_{0.8}As$ sample grown on GaAs, indicates a better bulk material quality. This is confirmed by the lower W_{oc} value: 469mV for the best lattice-matched GaAs device versus 618mV for the best lattice-matched $Al_{0.2}Ga_{0.8}As$ device.

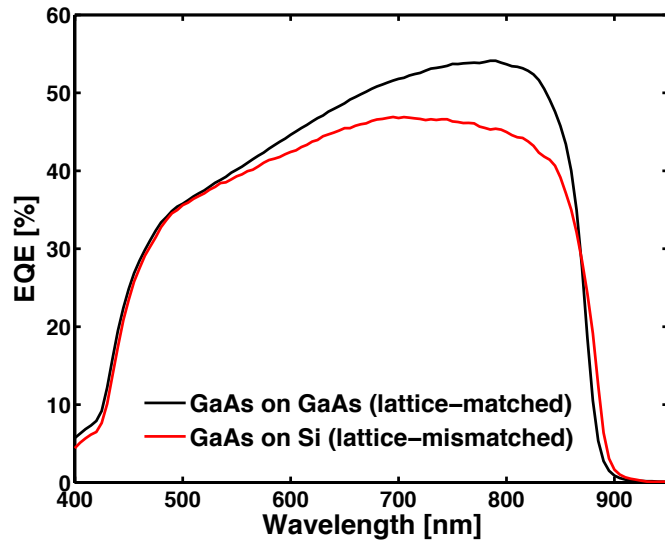


Fig. 7. External Quantum Efficiency (EQE) measurements of the best devices from the two GaAs samples grown on GaAs (black) and on Si (red).

Contrary to the $Al_{0.2}Ga_{0.8}As$ devices, the impact of the presence of TDs on the J_{sc} is apparent, with a J_{sc} reduction of $1.10mA.cm^{-2}$ between the sample grown on GaAs and the one grown on Si. The EQE measurements, displayed in Figure 7, confirm the lower collection efficiency for the cell grown on Si, especially at longer wavelengths. This can be directly related to a lower diffusion length of minority carriers in the presence of TDs, with in particular a reduced carrier collection in the base of the cell, away from the depletion zone. As a result, the solar cell grown on Si exhibits a poorer EQE at longer wavelengths absorbed in the back of the cell. As opposed to the $Al_{0.2}Ga_{0.8}As$ samples, the diffusion length is not limited by the bulk material quality and TDs directly affect the J_{sc} and the EQE in a non-negligible way.

Prototypes of $Al_{0.2}Ga_{0.8}As$ and GaAs solar cells have been grown on Si substrates using direct nucleation of $Al_xGa_{1-x}As$ on Si followed by dislocation filters in order to reduce the TDD. The $Al_{0.2}Ga_{0.8}As$ devices exhibit a bandgap of 1.7eV, making them suitable for current-matched III-V/Si tandem dual junction solar cells. A TDD below 10^7cm^{-2} has been demonstrated in the base of the cell.

The main limitation of our 1.7eV $Al_{0.2}Ga_{0.8}As$ solar cell prototypes lies in the bulk material quality of the $Al_{0.2}Ga_{0.8}As$, for the sample grown lattice-mismatched on Si as well as for the sample grown with a negligible TDD on GaAs. This poor material quality is confirmed by the low W_{oc} values and high ideality factors measured for both $Al_{0.2}Ga_{0.8}As$ samples while this issue is not as significant for GaAs samples. Growth of high material quality $Al_{0.2}Ga_{0.8}As$ is known to be challenging, with oxygen contamination a main concern leading to a strong deterioration of the performances of the devices [16]. This issue has been highlighted in previous publications by the authors [17-18].

Recent work has focused on the improvement of the $Al_{0.2}Ga_{0.8}As$ material quality by improving the growth conditions and in particular the substrate temperature. This optimization study has yielded a strong improvement of performances with increasing the growth temperature from $580^{\circ}C$ to $620^{\circ}C$, with a V_{oc} over 1.21V demonstrated [19]. $Al_{0.2}Ga_{0.8}As$ solar cells epitaxially grown on Si with a V_{oc} exceeding 1.0V are likely achievable by transferring this optimized $Al_{0.2}Ga_{0.8}As$ growth recipe on Si. Further optimization of the buffer and DFLs, in order to achieve a material quality and a TDD similar to the ones demonstrated with laser devices [10], can potentially yield V_{ocs} above 1.1V on Si substrates.

Optical optimization of the $Al_{0.2}Ga_{0.8}As$ cells front surface is also needed in order to improve the current density produced by the cell. Replacement of the current AlAs/GaAs SPL window layer with a state-of-the-art AlInP window layer would allow the removal of the GaAs contacting layer between the front contact grid fingers, the AlInP layer being used as an etch stop. Further improvement would include the deposition of a broadband Anti-Reflection Coating (ARC). Such enhancements should increase the J_{sc} of the cell to values close or above $20mA.cm^{-2}$ and allow current-matching with an underlying Si bottom subcell.

Finally, in addition to the perspective of achieving high material quality with a TDD below $1 \times 10^6cm^{-2}$ [10], a key benefit of this alternative pathway lies in the use of a thin buffer ($2.1\mu m$ to $2.8\mu m$), reducing the amount of III-V materials required and potentially the growth time needed. Additionally, a c-Si cell can be used as a bottom cell; in comparison with the Si_xGe_{1-x} subcell required using a metamorphic Si_xGe_{1-x} approach [5,7].

V. CONCLUSION

1.7eV $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ and 1.42eV GaAs solar cells have been grown on Si by Molecular Beam Epitaxy (MBE), using direct nucleation of lattice-mismatched $\text{Al}_x\text{Ga}_{1-x}\text{As}$ material on the Si substrates. Dislocation Filter Layers (DFLs), along with Thermal Cycle Annealing (TCA) steps, have then been used in order to reduce the Threading Dislocation Density (TDD). TDDs of $8(\pm 2) \times 10^6 \text{cm}^{-2}$ and $5(\pm 2) \times 10^6 \text{cm}^{-2}$ have been reached in the base of the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ and GaAs cells, respectively.

As expected, the presence of Threading Dislocations (TDs) directly impacts the V_{oc} of the cells for both absorber materials investigated, with a reduction in V_{oc} of about 150-160mV from the reference samples grown lattice-matched on GaAs to the samples grown lattice-mismatched on Si.

However, the J_{sc} and the EQE are only impacted by the presence of TDs for the GaAs solar cells. This is due to a relatively low material quality for the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ cells, leading to high W_{oc} values on both substrates and limited bulk minority carrier diffusion length, independently of the presence of TDs. As a result the carrier collection efficiency of the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ is similar on Si and on GaAs substrates.

Optimization of the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ growth parameters have since been carried out, yielding a strong improvement in the V_{oc} and J_{sc} of reference samples grown lattice-matched on GaAs with increasing the growth temperature from 580°C to 620°C. Transfer of this optimized $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ growth recipe on Si substrates is expected to yield a V_{oc} above 1V and pave the way toward the achievement of high efficiency 1.7eV $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ solar cells on Si suitable for dual junction III-V/Si tandem architectures.

ACKNOWLEDGEMENT

This work was supported by Total S.A. The authors acknowledge the support of the National Science Foundation of the U.S. (EPSCoR Grant #OIA-1457888).

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